Dynamic Voltage Rise Control, the Most Efficient Way to Control Turn – off Switching Behaviour of IGBT Transistors

Piotr Luniewski, Uwe Jansen, Michael Hornkamp

Abstract— **The goal of this paper is to present a new approach for the control strategy of Trench-/Field-Stop IGBTs which results in optimised turn-off behaviour. Significant U_{CE} overvoltages across stray inductances, as a result of very high di/dt during turning-off and collector current oscillations caused by the absence of tail current, are key challenges in the control of this new IGBT structure. This article contains detailed analysis of Dynamic Voltage Rise Control and experimental results for the high current IGBT 1200V- and 1700V- families.**

Index Terms— **intelligent IGBT drivers, EiceDRIVER™, active gate control, insulated gate bipolar transistor (IGBT), parallel connection.**

I. Introduction

THE main challenge for most engineers working in the power electronic field is to design a converter with an efficiency close to one. As far as only hard switching is considered, this idea requires that the device be applied as a current switch with transition times as short as possible and with low collector–emitter saturation voltage. Therefore, the use of Trench-/Field-Stop technology in IGBTs enabled a significant reduction in on-state voltage without increasing turn-off losses. The turn-off losses of these IGBTs are at least as low as previous generations, but the waveforms observed at turn-off, under some conditions, can cause severe concerns for the inverter design. For turn-off at high DC-link voltage, high current and low temperature either U_{CE} overvoltages or oscillations of the collector current limit the useful range of operation. Problems are especially severe if the parallel connection of IGBTs is applied.

Contrary to earlier generations of IGBTs, the turn-off behaviour cannot be controlled by the application of a higher R_G value at the expense of slightly higher turn off losses [8]. Turn-off behaviour is only influenced if the gate resistor is chosen significantly higher than the nominal value. Hence, the increase in delays and switching losses usually is beyond acceptable limits.

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Other approaches use some kind of feedback from the load side, either Active Clamping, du/dt, di/dt or a combination of these.

All of these solutions suffer from the fact, that the IGBT shows a delayed reaction to the gate signal [1]-[5].

Also these methods tend to be successful only if the switching is slowed down significantly and a substantial increase in turn-off losses is accepted.

Dynamic Voltage Rise Control (DVRC) [6] uses the du/dt as a mean to sense the turn-off of the IGBT and to initiate a recharging of the gate to avoid U_{CE} overvoltages. Due to this unique mode of operation it is possible to achieve smooth switching without significant drawbacks.

The driver system used in the tests consists of a board containing a DVRC-circuit as well as a fast bipolar booster stage directly mounted on top of the IGBT-module and a standard eupec *EiceDRIVER™*-Board 2ED300C17-S for supplying power, isolating the control signal and providing U_{CEsat}-protection. With this approach the DVRC-circuit does not suffer from design restrictions due to parasitic inductances in the gate circuit. Furthermore, this setup allows for easy paralleling since every module is driven by an individual booster-stage and protected against overvoltages by an individual DVRC-circuit.

In this paper, a new gate drive strategy is presented, explained in theory and experimentally validated for two cases:

- single switch based on eupec module FZ2400R17KE3
- two modules in a phase leg configuration connected in parallel (eupec FF1200R12KE3).

II. Chip Technology

Chip technology is mainly driven by loss and cost considerations. Thanks to the Trench-/Field-Stop structure shown in Fig. 1 reduction of steady state and switching losses are possible. When the additional n+ layer in between collector and n- substrate, shown dappled in the drawing, is applied, significant chip thickness reduction with the same collector-emitter voltage endurance is achieved. This leads to lower saturation voltage and decreased switching losses by reduction of stored charge. The trench - gate cell shape in comparison to planar cell gives increases carrier concentration

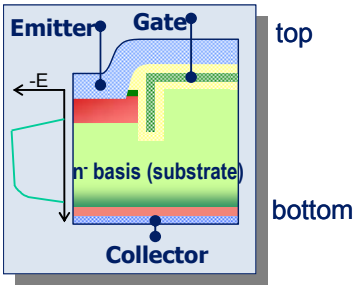

Fig. 1. Vertical cross-section of Trench-/Field-Stop IGBT structure.

and improves distribution from the top to the bottom of the chip with the result of further reduction of on-state losses. Due to reduced losses, the chip area for a given current rating can be significantly reduced compared to previous technologies. Since a large part of the cost of the chip itself as well as that of the module is related to the chip area this shrinking leads to a reduction of cost. Despite the obvious advantages given by the described structure, there can be severe problems with the di/dt controlled by the gate voltage and collector voltage oscillations can appear.

When gate voltage changes polarity from plus to minus the IGBT turns off, electrons from the n- substrate are extracted in the emitter and collector direction. The rectangular electric field inside a chip is created in a way shown in the left of Fig.1. As long as overvoltages during turn-off are moderate, as it is in low- and medium- power applications with low inductance design, the electrical field does not punch into the Field-Stop layer and the device shows a soft turn-off behavior. Especially in the case of high current modules the parasitic inductances can lead to a large overshoot of the collector voltage. When the field punches into the Field-Stop area, all charge is removed and the current stops immediately resulting into a high overvoltage and oscillation. Fig. 2 shows the switching behaviour of 1700V IGBT module at turn-off when a standard voltage gate drive and 3.6Ω gate resistor is applied. Therefore, it is necessary to use a larger gate resistor value or look for another method for collector current limitation and oscillation suppression.

III. The Strategies

A. Variation of the Gate Resistor Value

The most common method to limit di/dt, when standard voltage drivers are used, is to apply bigger gate resistor values. Applied to Trench-/Field-Stop IGBTs an influence on di/dt can only be observed if the gate resistor is increased significantly. From the cost point of view this seems to be attractive, but this solution suffers from unacceptable losses when used for high power Trench-/Field-Stop IGBTs. Fig. 3 shows the changes in switching performances in theory, when different values of gate resistors are applied. Generally, the energy losses during turn-off can be divided into three sections and calculated using formula (1). In the first section when collector voltage rises from zero up to the DC link

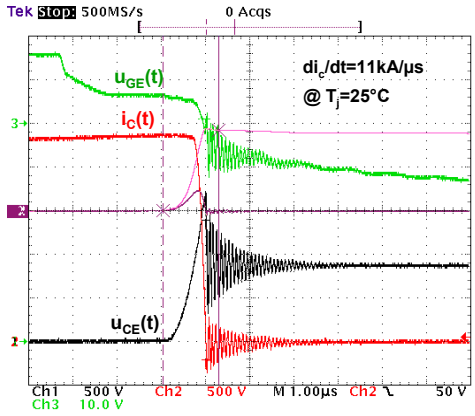

Fig. 2. Waveforms of FZ2400R17KE3 during turn-off, U_{DC}=900V, I_C= 2.4kA, E_{OFF}=920mJ, U_{CEmax}=1.72kV, R_G=3.6Ω, L_Q=50nH

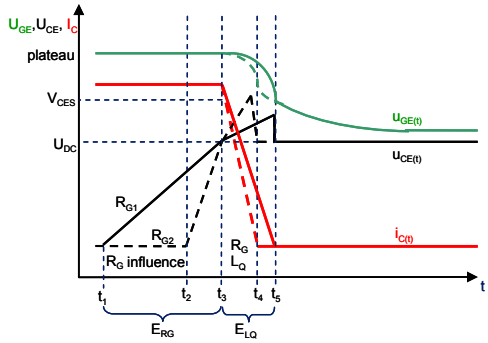

Fig. 3. Influence of gate resistor value on turn-off performances in theory when R_{G1}>>R_{G2}

voltage, energy is determined mainly by the gate resistor (2). In the second section when collector current goes down from the established value to zero the stray inductance (3) and the gate resistor, when it is markedly large, are the main parameters. The third part of the formula (1) called E_{TAIL} are losses generated by tail collector current and has been omitted since Trench/Field-Stop-IGBTs do not show tail current under the conditions under investigation.

$$E_{OFF} = E_{RG} + E_{LQ} + E_{TAIL} \quad (1)$$

$$E_{RG} = \int_{t_1}^{t_3} u_{CE}(t) \cdot i_C(t) = f(R_G) \quad (2)$$

$$E_{LQ} = \int_{t_3}^{t_5} u_{CE}(t) \cdot i_C(t) = f(L_Q, R_G) \quad (3)$$

where:

u_{CE} collector – emitter voltage

i_C collector current

The equations shown above are valid when the gate resistor R_{G1} is used. In the event of gate resistor R_{G2} << $R_{G1,}$ as can be concluded by simple assumptions and shown in Fig. 3, energies in both sections are decreased. However, overvoltages across the stray inductance are certainly increased and the voltage and collector current oscillations are not suppressed. The E_{off} dependence of the high power transistor as a function of the gate resistor value at 125°C operation is presented in Fig. 4.

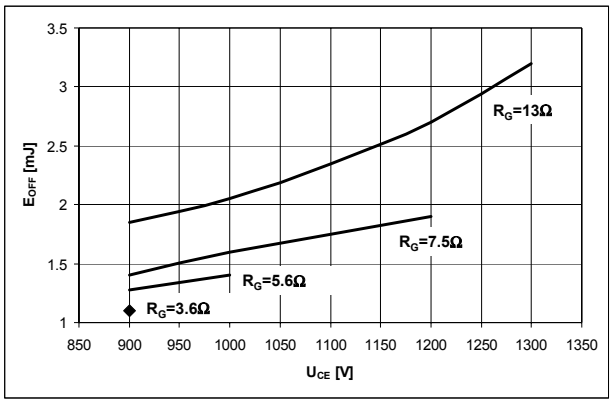

Fig. 4. Comparison of energy losses during turn-off transients of FZ2400R17KE3 versus value of the gate resistor and DC voltage link when: I_C=const=2400A, T_J=125°C, L_Q=50nH

The minimum value of gate resistor which can be used to obtain the maximum operating values for the FZ2400R17KE3 module with a simple gate voltage driver without any kind of feedback is 3.6Ω. In the application the nominal DC-link voltage may be higher than the DC-link voltage referenced in the datasheet (900V for 1700V IGBTs) and additionally voltage fluctuation of the DC-voltage link have to be taken into account. Therefore, IGBTs have to switch properly with voltages and currents higher than the reference operating values provided in the datasheet. For this reason the range of test voltage used in Fig. 4 has been extended to 1300V. The proper IGBT operation in this case requires a gate resistor with a value of 13Ω and leads to high switching losses. Operation with a gate resistor this high is only done for reference purpose and should be avoided in real applications.

B. Dynamic Voltage Rise Control – the Proposed Strategy

For the reasons described above the approach of using a voltage driver with gate resistor for di/dt limitation seems to be an old fashioned strategy, especially in modern, high power converters. Already for high current modules equipped with IGBT chips of previous generations most engineers have chosen more sophisticated methods of driving. Usually they apply some kind of feedback. Active Voltage Clamping (AVC) and variations applied for overvoltage limitation are well known and are the most used method in practice [1]. These methods use collector–emitter voltage as feedback to sustain the IGBT in conduction within a time mainly determined by stray inductance given by the high power circuit. Proper AVC operation forces the gate voltage to rise up and the collector–emitter voltage is limited as a result of the di/dt limitation. This mechanism works correctly if the collector current responds immediately to the gate voltage. Due to the large delay between the dropping of gate voltage below the Miller Plateau and the rise of collector-emitter voltage observed in Trench-/Field-Stop IGBTs methods which use collector–emitter voltage as direct signal for gate control cannot be employed.

The idea of DVRC (Dynamic Voltage Rise Control) [6] presented in Fig. 5 is a form of AVC where one part of

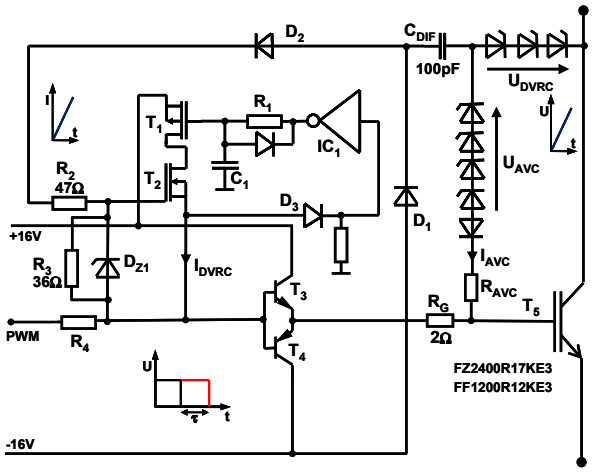

Fig. 5. Operational circuit diagram of DVRC function

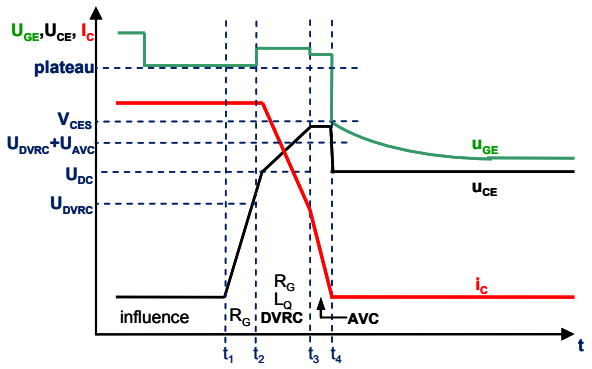

Fig. 6. Theoretical waveforms of DVRC functionality

feedback signal goes directly into the gate of the IGBT but a second part is sensed by the capacitor and is used as the control signal to an additional source [1] [2]. As presented in Fig. 5, two voltages called U_{AVC} and U_{DVRC} can be distinguished and the levels can be adjusted independently. When this IGBT starts to switch-off at t_1 in Fig. 6, the collector-emitter voltage rises with a slope defined by R_G until the first level called U_{DVRC} is reached (t_2). This is the starting point for the proportional current conducted by C_{DIF} and given by formula (4).

$$i_{CDIF}(t) = C_{DIF} \cdot \frac{du_{CE}(t)}{dt} \quad (4)$$

Voltage drop across resistor R_3 opens transistor T_2 and current called I_{DVRC} causes a voltage drop proportional to iC_{DIF} on resistor R_4. This voltage boosted by T_3 forces the IGBT back into the active region. The slight collector current slope reduction results in a significant du_{CE}/dt limitation as a main feature of DVRC function. If the limitation is not sufficient, the U_{CE} voltage crosses the AVC activation point, calculated as U_{AVC}+U_{DVRC} at time t_3, and I_{AVC} reacts to the gate directly. Between t_3 and t_4 DVRC-operation is already terminated but U_{CE} is limited by the AVC function. The maximum value of this current can be approximated by equation (5).

$$I_{AVC} = \frac{U_{CES} - (U_{DVCR} + U_{AVC})}{R_{AVC}} \quad (5)$$

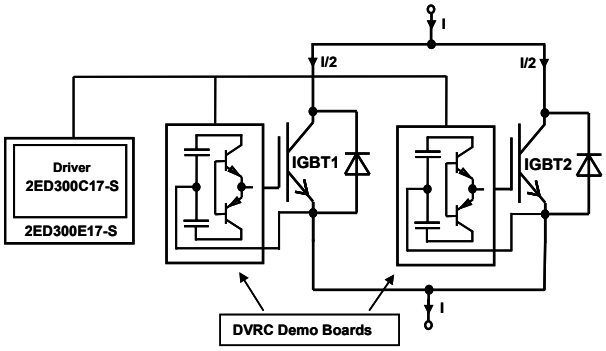

Fig. 7. Block diagram for IGBT paralleling using DVRC technology.

Here in:

U_{CES} is the present collector-emitter voltage.

Under normal operation, when the DC-link voltage and I_C do not exceed the referenced operating conditions of the datasheet, the AVC is not in operation because the U_{CE} voltage will not reach the AVC activation point.

The DVRC function presented in Fig. 5 is fully independent from the AVC and enabled only after the turn-off command in a time period determined by the time constant of R_1 and C_1. This feature protects the IGBT against unnecessary DVRC operation when significant voltage spikes across U_{CE} appear caused by other effects such as diode turn-off.

C. *Driving paralleled IGBTs with individual boosters*

For most circuits in Power Electronics, especially in the high power range, the half-bridge is the elementary building block. Many design engineers have already recognised that overvoltages can be avoided more effective if the half-bridge consists of dual modules instead of single IGBT modules. This approach enables the reduction of stray inductance in the commutation loop. But since the current rating of dual modules is usually limited to one third of the rating of single IGBT modules this approach often makes module paralleling necessary.

To drive paralleled IGBTs two different strategies may be applied. Either one large driver may be used to drive all the paralleled IGBTs or each IGBT may be driven by an individual driver. Both approaches have their merits, but both suffer also from severe drawbacks.

Single driver:

- ☺ low part count
- ☺ simple protection
- ☹ long gate connections
- ☹ requires symmetrical gate circuit layout
- ☹ circulating currents in the auxiliary emitter circuit

Individual gate drivers:

- ☺ short gate connections
- ☺ may be realised with standard drivers
- ☹ high parts count
- ☹ deviation in propagation delay will lead to asynchronous switching of the paralleled IGBTs
- ☹ protection functions need to be coordinated

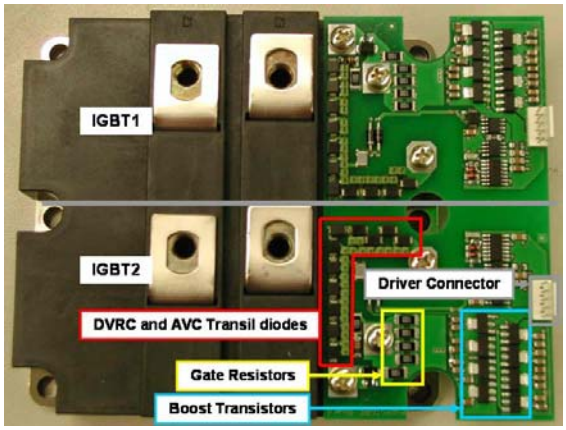

Fig. 8. FF1200R12KE3 - half bridge module equipped with suitable DVRC demo board.

Successful implementation of the DVRC-circuit requires a booster stage to be located on the PCB mounted directly on top of the IGBT. This configuration also allows the driving of paralleled IGBTs and avoids the drawbacks of the approaches presented previously. The 2ED300C17-S driver, with it's own booster stage left unconnected, provides isolated power supply, control signal isolation and protection for all the paralleled modules. Each of the modules has its own DVRC-board mounted on top containing the DVRC-circuit itself, the booster stage and buffer capacitors for the power supply. Due to the booster being directly on top of the IGBT gate circuit the inductance is no longer a problem. This approach avoids the redundancy inherent in the system using individual drivers and reduces complexity and circumvents the problems resulting from tolerance and drift of propagation delay. The idea of this approach is shown in Fig. 7.

IV. Experimental Validation

The experimental validation of the DVRC function has been carried out for the FZ2400R17KE3 single power switch and two FF1200R12KE3 dual power modules connected in parallel. In both cases the investigated modules were connected in a half-bridge configuration, where the bottom transistor was investigated and the top switch was used as a FWD diode. To minimize gate stray inductance and to provide better heat dissipation of the driver output stage, the investigated transistors have been equipped with dedicated PCB demo boards shown in Fig 8. This approach requires isolated PWM signals and power supplies for boost transistors. This function was provided by a 2ED300C17-S driver board. By using transil diodes connected in series and bypassed by jumpers, the flexibility in adjusting threshold voltage independently for DVRC and AVC has been reached. All investigations were done with a fixed 2Ω gate resistor value.

A. *Investigation of Single Module FZ2400R17KE3*

The target of this investigation was to reduce the E_{OFF} energy to an acceptable level as well as avoid oscillations. The setup with the large gate resistor will be used as a reference.

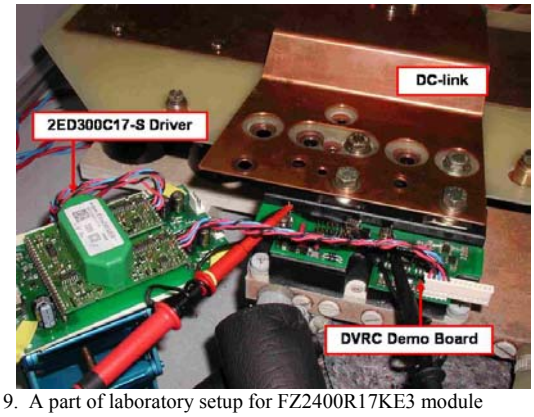

Fig. 9. A part of laboratory setup for FZ2400R17KE3 module investigation

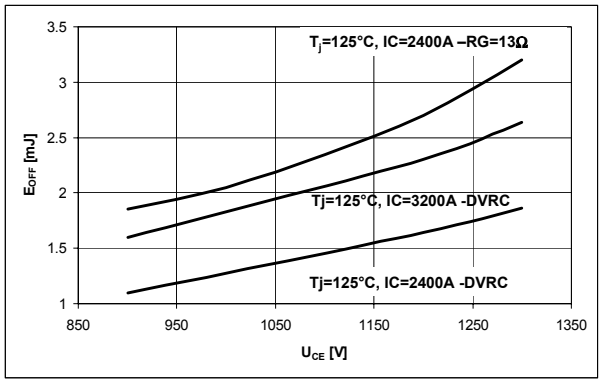

Fig12. Comparison of energy losses during turn-off of FZ2400R17KE3 between DVRC and gate resistor method versus DC voltage link at: I_C=2400A/3200A, T_J=125°C, L_Q=50nH

The laboratory setup with module, DC-link capacitors, DVRC demo board and driver is shown in Fig. 9. The main focus was to get the best performances when the reference operation values for the modules are significantly exceeded. Therefore, the presented results refer to a situation at which the collector current is greater than 2400A and U_{CE} is varied in a range from 900V up to 1300V. Fig. 10 and Fig. 11 present typical curves for I_C=3200A, U_{CE}=900V and I_C=3200A, U_{CE}=1300V respectively. The U_{DVRC} was set to a value of 700V and U_{AVC} was equal to 800V. In this situation when the DC link voltage was 900V the U_{CE} slope was changed from 2kV/µs to 1kV/µs and voltage stopped at 1.48kV. In the case of a 1300V DC link voltage, the U_{CE} slope limitation is similar to the previous situation, but additionally, it has been clamped to 1.68kV as a result of the AVC action. In both cases the maximum permissible collector–emitter voltage has not been exceeded and oscillations are suppressed. Fig. 12 presents the E_{off} obtained for nominal collector current and for overcurrent with DVRC and also for nominal I_C and a standard voltage driver with a gate resistor of 13Ω. It can be seen that DVRC saves approximately 60% of E_{off} and provides smooth curves in contrast to the gate resistor method.

B. *Investigation of Two FF1200R12KE3 Modules Connected in Parallel*

To check if the DVRC provides safe limitation under severe operating conditions a test with two paralleled dual modules

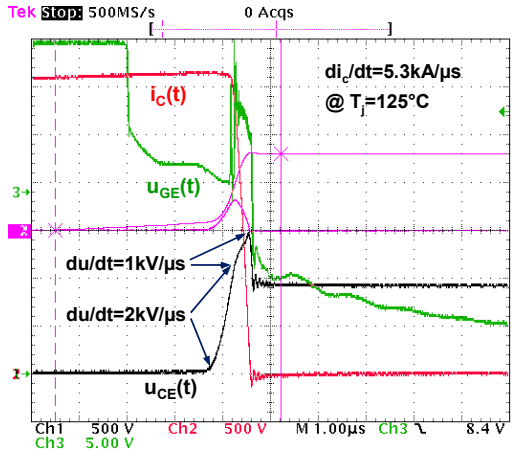

Fig. 10. Waveforms of FZ2400R17KE3 during turn-off, U_{DC}=900V, I_C= 3.2kA, E_{off}=1.6J, U_{CEmax}=1.48kV, R_G=2Ω, L_Q=50nH

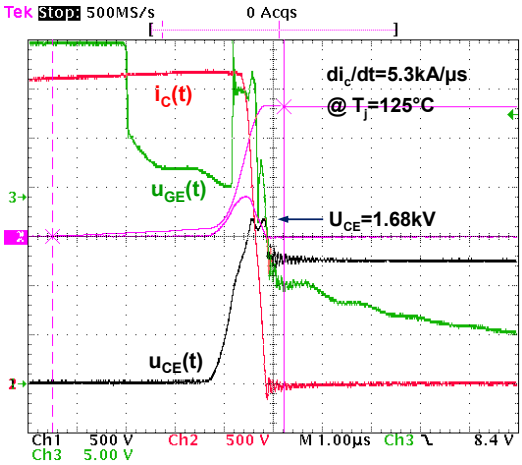

Fig11. Waveforms of FZ2400R17KE3 during turn-off, U_{DC}=1300V, I_C= 3.2kA, E_{off}=2.64J, U_{CEmax}=1.68kV, R_G=2Ω, L_Q=50nH

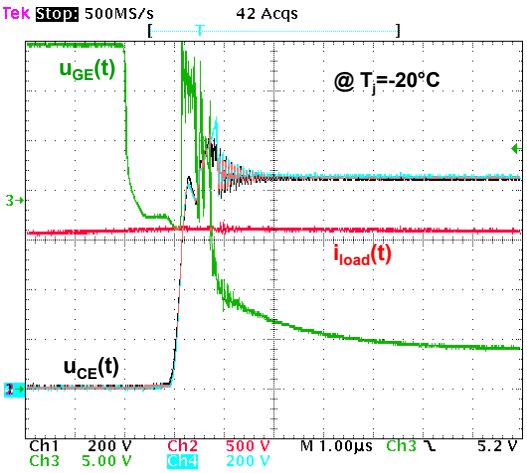

Fig. 13. Waveforms of FF1200R12KE3 connected in parallel during turn-off, U_{DC}=900V, I_C=1680A, U_{CEmax}=1100V, R_G=2Ω, L_Q=50nH

FF1200R12KE3 was set up. To allow testing at low junction temperatures, where switching behaviour is most critical, the modules were mounted on a cold plate connected to a refrigeration machine. Each IGBT is equipped with its own DVRC-board as described in Fig. 7 and shown in Fig 8. Collector voltages of both modules are measured to check if there is appropriate overvoltage protection provided for both

of the modules. Fig. 13 shows the waveforms observed on this setup switched at 900V, 1680A and -20°C. Although both collector voltages are not exactly identical this test shows that the circuit does not suffer from variations in propagation delays and that the maximum collector-emitter voltage is not exceeded by any of the modules. The almost identical collector-emitter voltage indicates that the dynamic collector current sharing between both IGBTs under turn-off should be acceptable.

V. Conclusion

In this paper it has been demonstrated that the challenges imposed by using Trench-/Field-Stop IGBTs in IHM modules can be coped with by using advanced driving strategies. With the methods presented here the power electronic designers working in the high power range can take full advantage of the low forward voltage drop of the newest generation of IGBT chip technology without drawbacks in switching performance.

References

[1] H.P. Rothwangl, H. Schamböck, "Advanced IGBT Control Strategies Improvement of Switching Characteristic via Active Gate Control," *EPE2003* Toulouse.

[2] Patrick R. Palmer, Haile S. Rajamani, "Active Voltage Control of IGBTs for High Power Applications," *IEEE Transaction on Power Electronics,* vol. 19 no. 4, July 2004.

[3] H. G. Eckel, L. Sack, "Optimisation of the Turn-off Performance of IGBT at Overcurrent and Short-Circuit Current," *EPE1993* Brighton.

[4] Christian Gerster, Patrick Hofer, "Gate-Controlled dv/dt- and di/dt-Limitation in High Power IGBT Converters," *EPE Journal*, vol. 5 no. 3/4, January 1996.

[5] Ulrich Schwarzer, Rik W. Doncker, Rainer Sommer, Georg Zaiser, "Snubberless Operation of Series Connected 6.5 kV IGBT's for High-Power and High-Voltage Applications," *EPE2003* Toulouse.

[6] M. Hornkamp, "Circuit Arrangement for Control of Semiconductor Circuit", WO Patent Application 002003085832A1, October, 2003.

[7] Dorin O. Neacsu, "Active Gate Drivers for Motor Control Applications", *Tutorial presented at IEEE PESC 2001*, Available at: http://www.ewh.ieee.org/soc/pels/Comm/Education/Tutorials/pesc01_gatedrive.pdf

[8] Application note, "Switching Behavior and Optimal Driving of IGBT[3] modules"*AN2003-03,* Available at: *http://www.eupec.com/gb/2_PRODUCTS/2_5_ApplicationsNotes/pdf/an_2003_03_e.pdfht*

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