Part II: Using the LLC calculator with Rules of Thumb (ROT) and fast verification with LTspice

A guide for adapting the LLC calculator to design rules based on exact mode analsyis of LLC converter

About this document

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Scope and purpose

This document is intended to give guidance in the application of Rules of Thumb (ROT) based on exact non-linear analysis of the LLC converter for using the LLC calculator as a design synthesis tool to develop the basic LLC tank parameters based on the SMPS specification requirements. The overall target is minimizing the conduction losses in the LLC by minimizing the RMS currents on both the primary side and secondary side of the LLC converter for a given output power and voltage regulation range requirement (either input or output referred).

- Conventional usage of First Harmonic Approximation (FHA) in the design process appears to result in higher than desirable current on both the primary and secondary sides, especially in low-line conditions, due to the Cr sizing, overall Q of the Cr/Lr network, and generally larger than desirable inductance m-ratio due to FHA simplifications.
- It is possible to develop working alignments which lower both the primary- and secondary-side RMS current, with better overall efficiency over the full load range, and with a more functional control span over the line voltage regulation range.
- Comparisons of different optimization targets and strategies will be presented with analsys of results over line and load range.

Also discussed are issues of dimensioning the tank and transformer gain in consideration of the transition between buck and boost mode, and how that affects both efficiency and the required span of control operation. MathCAD techniques for RMS current factor vs normalized switching frequency are shown, as well as a MathCAD technique for calculating the maximum possible output power for a given tank alignment vs normalized switching frequency.

Intended audience

This application note is intended for anyone interested in and working on the design of the resonant LLC converter at any power level or application type.

It is a companion to Part II in the LLC Design Webinar series from PMM Academy.

The primary tools discussed are “no-cost” tools such as the vector-based LLC calculator running in Excel, and a parameterized LTspice simulation circuit for tank parameter verification developed for easy configuration and fast simulation (tens of seconds, not tens of minutes). Additional capabilities are described using more expensive tools such as MathCAD and MatLAB with specialty software.

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1 Myth-busters for the FHA technique

FHA is a widely used design method for developing the resonant LLC converter. [1] It will produce an operable design, but the question now being heard more often is, does it produce an optimum design? And based on which considerations? Regulation? Efficiency?

Also, does it provide enough information to inform the designer accurately of how much margin and capability the design has to handle corner cases that may arise? Is there a chance that efficiency and regulation performance might be improved just by a better tank design, with the same semiconductor complement? Not seeking that extra performance margin could be viewed as leaving money on the table from a design engineering viewpoint.

1.1 Typical design process using FHA – is GIGO the limiting factor?

Many suggested variants exist for incorporating the use of FHA into a design synthesis process – the original FHA technique itself merely purports to analyze and describe the operational characteristics of a specific proposed LLC tank configuration, based on certain simplifications, not to specify the means for arriving at that configuration. [2, 3]

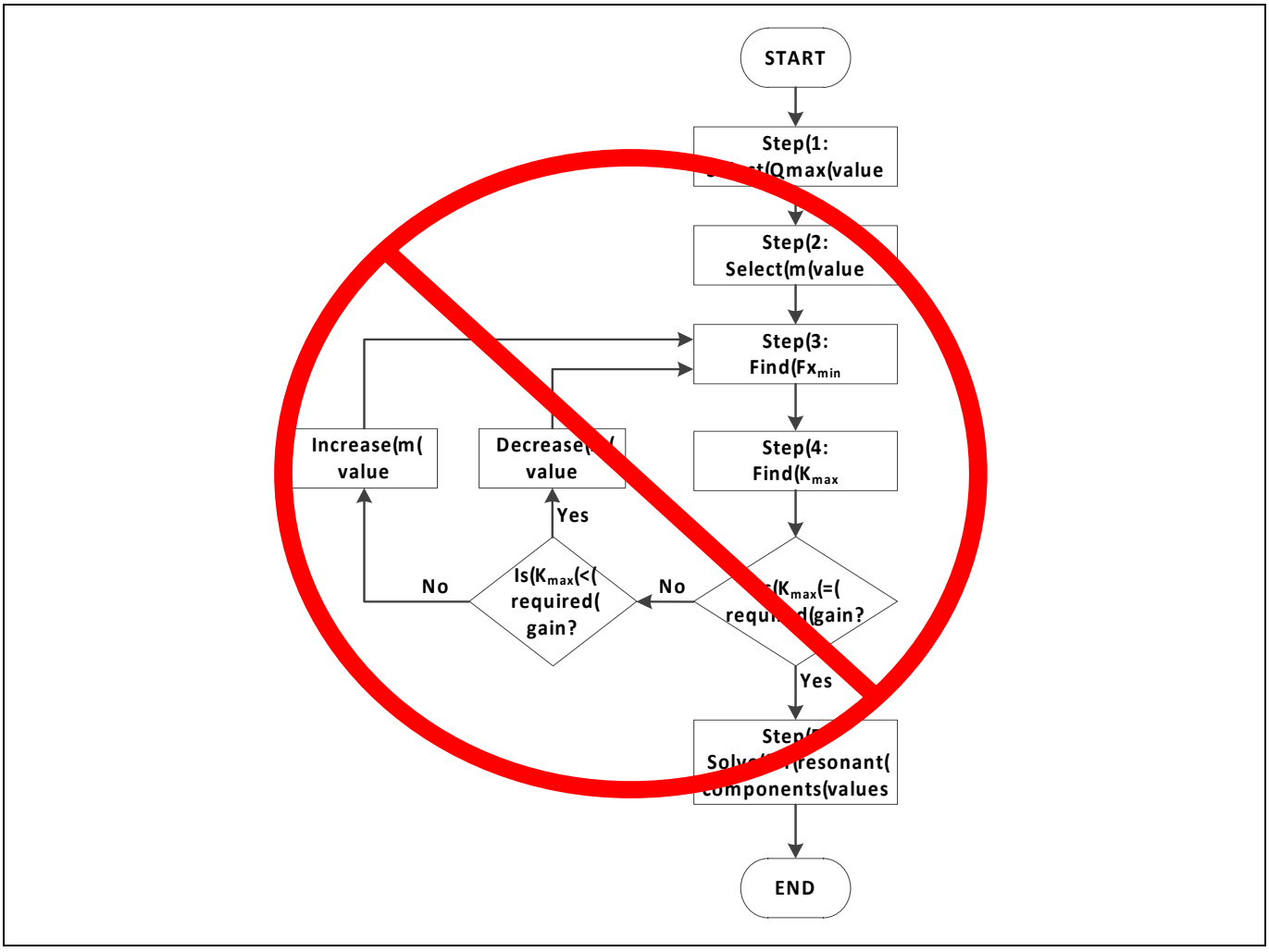

Figure 1 Example of the iterative process for using FHA for LLC design

It can be argued that many of these alternative published procedures may be useful and in some sense "correct" – in the sense of reaching an optimized result within the boundaries of the simplifications of FHA. However, the case can be made that this is only so if the results calculated by the FHA technique are both accurate and sufficient to assess the design being considered. If that is not the case, due to the simplifications and shortcomings of FHA, then the potential for GIGO must be considered carefully. Or an alternative design process must be used, using accurate time-domain based techniques and iterative solutions, which have been published and discussed as early as 2001, but seem largely ignored. [4]

1.2 What is the primary question for optimizing the LLC converter?

"One of the really tough things is figuring out what questions to ask… Once you figure out the question, then the answer is relatively easy." – Elon Musk

1.2.1 What is the fundamental design goal for the LLC tank?

The basic requirements for an LLC converter are generally very similar to any other voltage regulator circuit:

- Achieve the necessary output voltage regulation vs load current
- Accomplish the above over the necessary line input voltage range, including input voltage drop-outs or surges

As the LLC converter is a regulation topology that can greatly reduce or nearly eliminate switching loss, when properly designed (there is more about this in Part III) then it is also the designer's responsibility to configure the LLC converter to accomplish the above with the minimum RMS current on the primary and secondary sides. If we've essentially eliminated switching loss, then the remaining key to efficiency is minimizing conduction loss from $I^2 \times R$ losses.

This is presumed straightforward to do, if the converter is operating at or just below resonance all the time, but an examination of line regulation-related issues and the common requirement for systems such as telecoms, battery charges and lighting to have a significant range of output voltage adjustment will show that there are often reasons why this is not possible or desirable. This is due to the requirements for input voltage span and output voltage adjustment. In particular, this may become an issue for higher voltage outputs, and for cases when a required voltage control span is coupled with a need to limit the frequency modulation span due to component or system requirements, while avoiding techniques such as burst mode in order to prevent or limit capacitive mode behavior.

Within these criteria, there may be multiple possible "optimum solutions" depending on the overall system performance targets, including factors such as overall power density and efficiency over a wide load range. The intention of this guide is to highlight factors contributing to optimization in several possible paths; it is up to the designer and specifier to decide which set of trade-offs is optimal for a given commercial application.

Let's take a closer look at some conditions where FHA may not deliver the feedback and information needed by the designer to optimize the system performance.

1.3 Does linear AC analysis fall short in predicting LLC RMS current?

This is a fundamental issue, and one on which overly simplistic viewpoints still often prevail. In principle, if operating just at resonance, variations on the tank components and Q should not cause significant differences in operating currents. (This ignores for the moment the impact of I-Lm.) But how often is this ideal input voltage the case for a real-world application, such as off-line operation from a PFC front end, with significant line frequency voltage ripple and slow regulation response?

And while for AC-DC off-line applications, the primary-side current is generally not very high, for LV outputs the secondary-side current may be quite large even for mid-range power output requirements (500 W to 600 W). Under these conditions the RMS to average current ratio has considerable bearing on efficiency – and hence, the actual operating normalized switching frequency in relation to the tank resonant frequency.

1.3.1 Mistaken assumption about estimating RMS currents in the tank or output rectifiers – variable frequency sine wave is not the reality

Let's consider the basic line regulation scenario – nominal input vs low-line. There are less severe variations of line regulation which are also normally encounted even under nominal conditions – for example, a typical PFC regulator may have up to +/-5 percent line frequency ripple voltage under nominal full-load operation. This can be handled in several ways – such as tuning the LLC for exact resonance at the average, and having it back and forth between buck and boost mode, or considering the peak input voltage, and taking this as the nominal value for operationg at Fr(Hz) (the converter resonant frequency) and going into some value of boost-up in the rest of the "nominal" range.

But for now, let's consider a simpler case, just assuming a pure DC nominal line input voltage of 380 V, and a nominal low-line voltage of 350 V. FHA postulates a variable frequency sine wave for the converter analysis, and so shows no difference for the secondary-side RMS to average current between these two cases. But what do things really look like?

Figure 2 shows the output current time diagrams for a 12 V/50 A LLC converter running at full load for both line voltage levels – at 380 V and 350 V. Note that the time domain response of the resonant Lr/Cr network does not result in variable frequency sine waves (as for FHA with linear AC analysis), but rather haversine waves at a fixed period defined by the resonant network. As described in the first application note in this series, as the square-wave primary-side drive is lowered in frequency, the converter enters discontinuous or boost mode, and due to the charge pump effect of the primary magnetizing inductance Lm charges up the resonant capacitor so that a higher half-wave resonant current pulse can be delivered each half-cycle.

This results in the peak current at the output rising from 81 A to 103 A, and the output RMS current (for the same average current of 50 A) rising from 56.23 A to 63.18 A, due to Discontinuous Current Mode (DCM) operation. It would be preferable to minimize this additional RMS current and the $I^2 \times R$ losses it induces on the secondary side.

FHA will not predict this variable RMS factor, as it assumes a variable frequency sine wave exciting the resonant network. So, FHA cannot be used to estimate the RMS output current factor and the variation in conduction loss with different tank designs when not operating exactly at resonance.

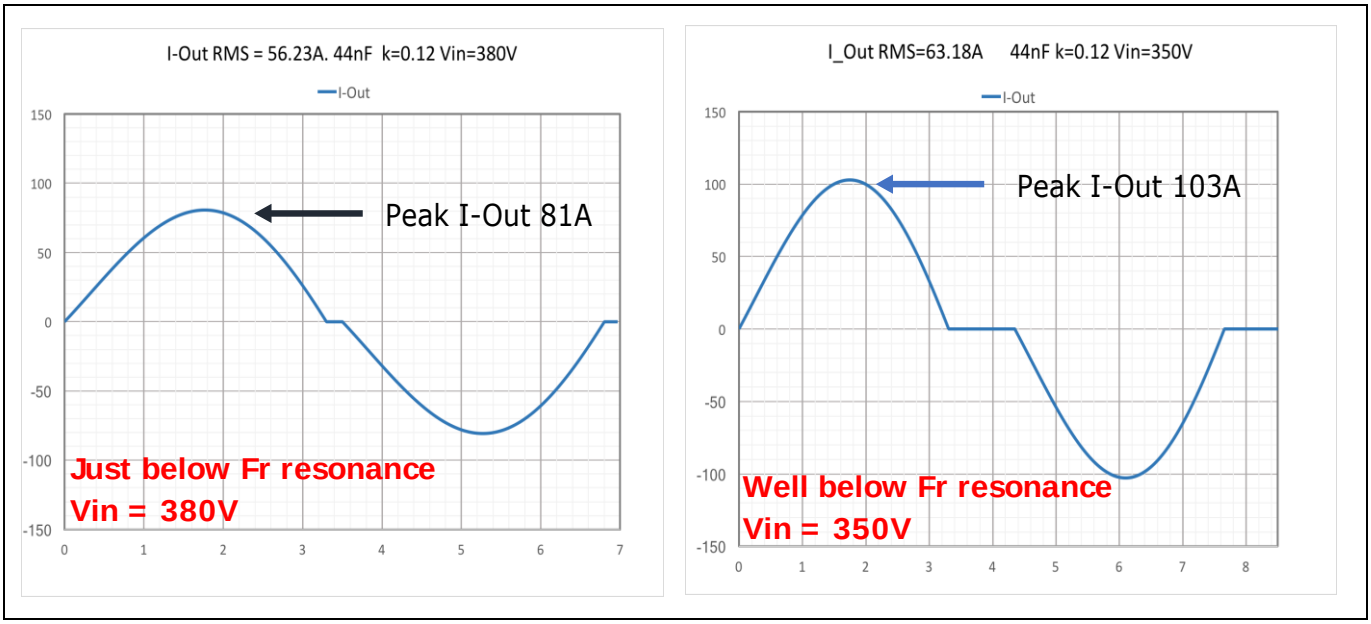

Figure 2 Comparison of secondary-side current waveforms for 50 A average output current for V_{in} of 380 V and 350 V for a 12 V LLC converter

When considering these facts, there are several points to investigate further:

- Viewing the LLC converter with variable frequency linear AC analysis seems to have the potential to miss some important characteristics with regards to predicting the converter behavior and being able to assess and analyze a design prior to construction and testing.
- Charging the resonant capacitor Cr from the square-wave input on the primary side and understanding the impact from the perspective of time-domain behavior may be key to predicting performance capabilities of a given tank design – particularly the true maximum gain achievable and the power delivery capability for a specific m-ratio.
- Engineers love to be able to create nice-looking gain plots vs frequency for varied load conditions with various configurations of FHA calculators – but is it possible to "game" or modify the design inputs and target criteria so that a FHA-based tool will produce results that more nearly resemble the results from time-consuming exact mode analysis or simulation (or actual hardware)?
- Once such a design is formulated, is it possible to have a low-cost tool that can do calculations or simulations in only tens of seconds to verify the fundamental tank performance in the time domain for gain vs frequency, output current and power margin, incorporating the necessary non-linear characteristics and complexity for a realiastic basic behavioral analysis of the tank?

These are the targets of this work which, will be addressed in the following application note.

2 Design review of the Infineon/Finepower 12 V 600 W LLC converter

2.1 Overview of the Infineon/Finepower 12 V 600 W LLC converter

For the purpose of this investigation, we chose to use the Infineon 12 V 600 W LLC design, which is available in several different configurations with different primary-side MOSFETs and either mixed signal control with the ICE2HS01G or digital control with the XMC™ 4200. Options for primary-side MOSFETs have included CoolMOS™ IPP60R190P6 and IPP60R280C7, and now IPP60R170P7. The basic design is the same for these configurations, as shown in **Figure 3**. [5]

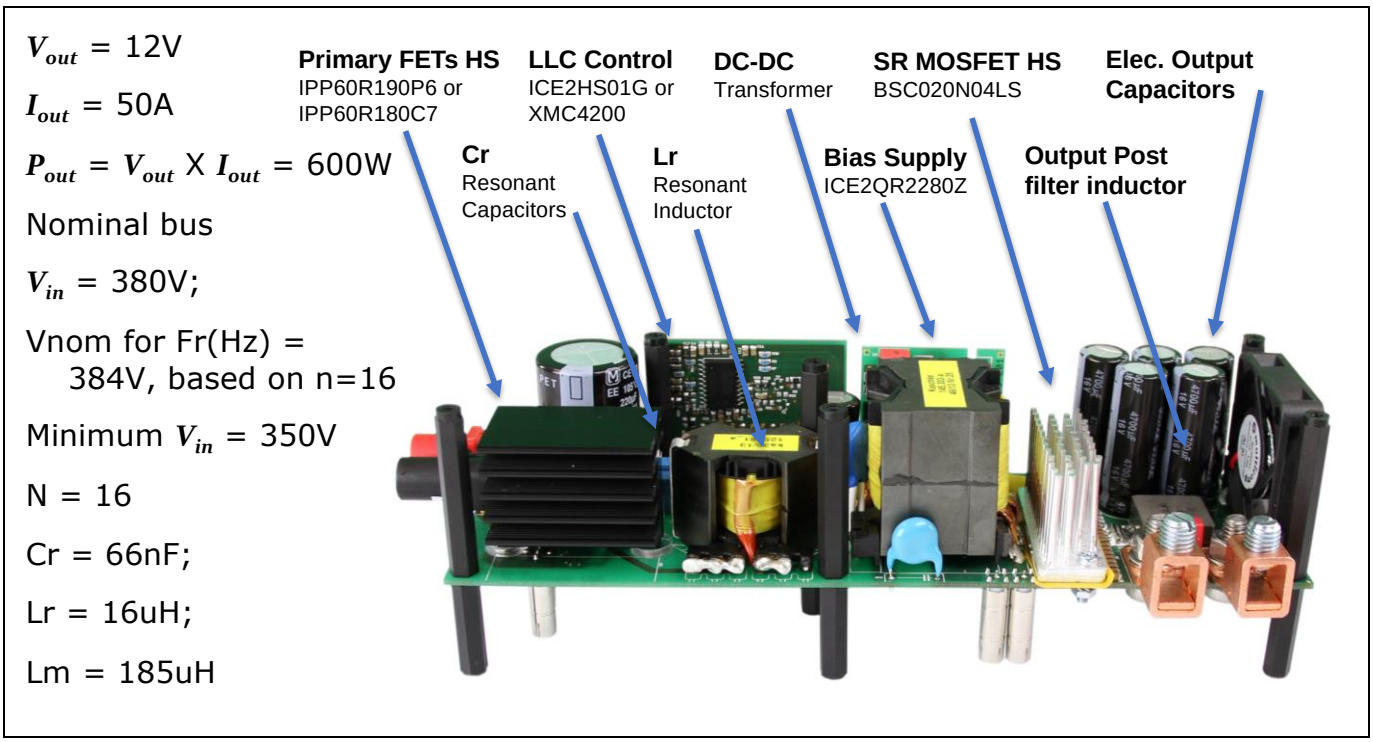

Figure 3 Infineon/Finepower 12 V 600 W LLC converter, for design review

2.2 Supply specifications and LLC tank parameters

Table 1 Design parameters/specifications

Description	Minimum	Nominal	Maximum
Input voltage	350 V DC	380 V DC	410 V DC
Output voltage	11.9 V DC	12.0 V DC	12.1 V DC
Output power			600 W
Efficiency at 50 percent P_{max}	97.5 percent		
Switching frequency	90 kHz	150 kHz	250 kHz
Dynamic output voltage regulation (0 to 90 percent load step)			Max. overshoot = 0.1 V Max. undershoot = 0.3 V
V_{out_ripple}			150 mV_{pk-pk}

2.3 FHA predicted gain curves and F_{min}, with Fr(Hz) = 155 kHz and Cr = 66 nF, m = 12.5

The Excel LLC calculator tool described in the first paper of this series [6, 7] was used to plot FHA gain curves for the Infineon/Finepower 12 W 600 V SMPS design shown in **Figure 3**. This could be called a mixed-mode design, as for the nominal input voltage range it must operate both in boost mode (for input voltage below 384 V) and in buck mode (for input voltage between 385 V and 410 V). The M_{nom} curve is the predicted full power gain curve for the converter as designed, with the LLC resonant tank values for Cr, Lr and Lm and transformer turns n = 16, as shown in **Figure 4**. Marker lines are used to define the required gain boundaries:

- M_{max} is the peak boost-up gain needed for operation/regulation at minimum V_{in} = 350 V
- M_{min} is the gain attenuation needed for operation up to 410 V.

Because the gain roll-off in buck mode is quite variable depending on the operating load current (and other parameters, such as the transformer parasitic parallel capacitance) buck mode behavior should be examined carefully under a range of load conditions. In the plot of **Figure 4**, the dashed orange curve for “fixed load” was set to 60 percent load, and under these conditions, the calculated/predicted F_{max} for V_{in} = 410 V is 1.5 × the Fr(Hz) tank resonant frequency, or about 230 kHz.

- FHA predicted gain curves for 66nF, Fr(Hz)=155kHz, m=12.5 design
- Given buck mode operation, turns ratio, etc, at 60% load, Fmax = 1.5 X Fr(Hz)
- Fmin = 0.57 X Fr(Hz) = 88kHz (predicted by FHA)

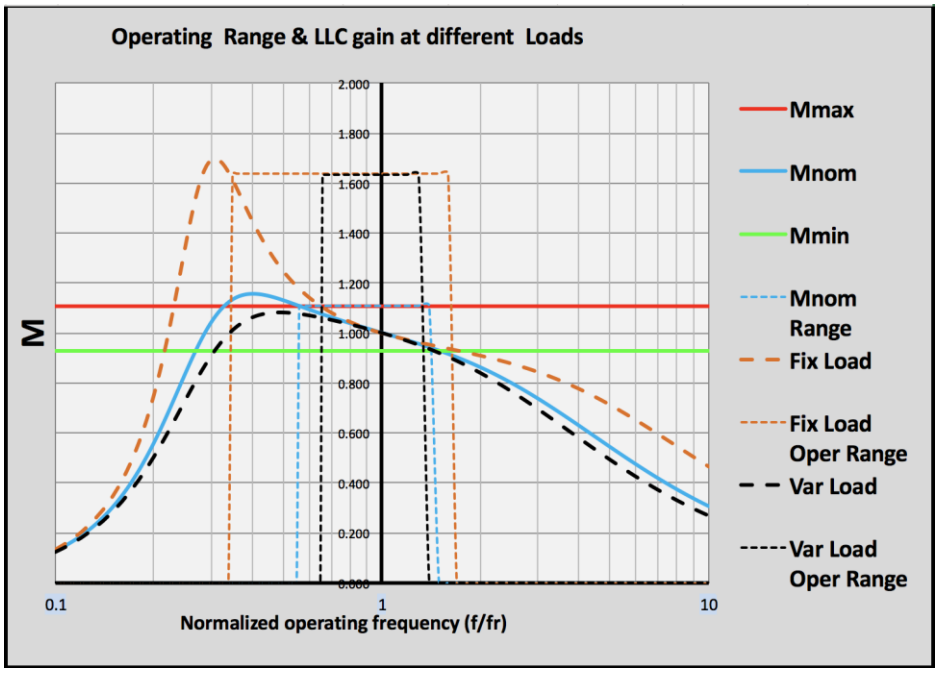

Figure 4 Predicted operating range curves for the Infineon/Finepower 12 V 600 W LLC converter

2.4 Analysis of operating point transitions (boost to buck mode) and impact on F_{max} at 10 percent load

At 15 percent load the predicted operating frequency rises to 1.9 × Fr(Hz), which is approximately 294 kHz. It can go even higher for lighter load values such as 10 percent: see **Figure 5**. For silicon power MOSFETs such as CoolMOS™, this will generally dictate using a lower maximum frequency (250 kHz max.) and switching to burst mode operation, and taking some care to avoid or limit capacitive mode operation, which may be possible every time a burst starts up.

- FHA predicted gain curves for 66nF m=12.5 design
- Given buck mode operation, turns ratio, etc, at **10% load**, Fmax ~ 3X Fr(Hz) ~ 450kHz!
- Not feasible- mandates use of burst mode considering approach to input voltage range
- Burst mode requires care, for Cr configuration (HB) and entering and leaving burst mode to minimize capacitive mode operation

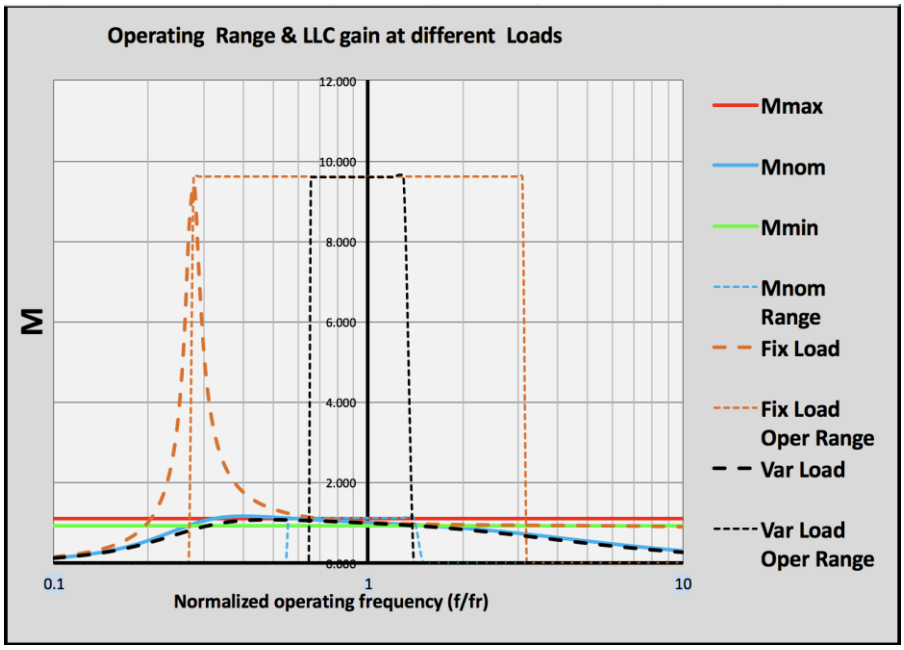

Figure 5 **Calculated F_{max} for 10 percent or less load for the Infineon/Finepower 12 V 600 W LLC converter**

2.5 FHA reverse analysis of system parameters to verify operational capability for regulation at low-line

A common design check is to verify a proposed LLC tank design for regulation capability by using what amounts to reverse mode analysis with FHA to calculate the expected minimum operation frequency for regulation at low-line input, and to verify the necessary boost-up gain. This process is shown in **Figures 6 and 7**, using MathCAD, for the Infineon/Finepower 12 V 600 W LLC converter from **Figure 3**.

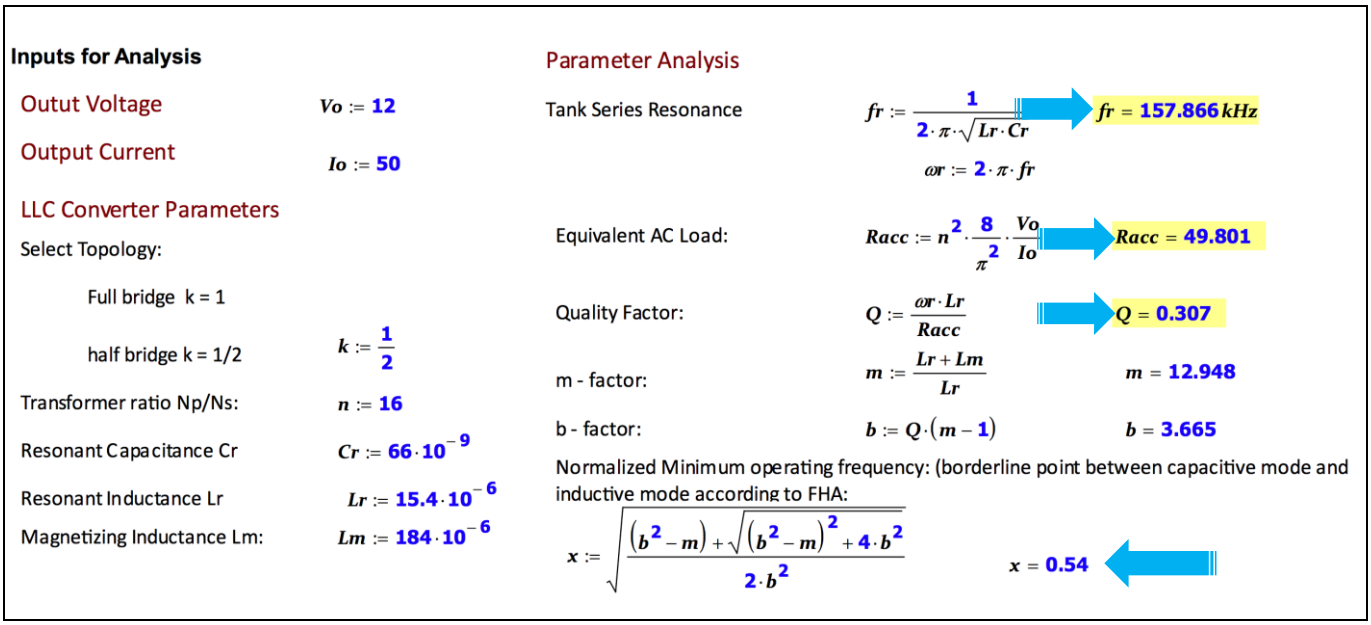

Figure 6 LLC converter definition and calculation of basic LLC parameters from tank values

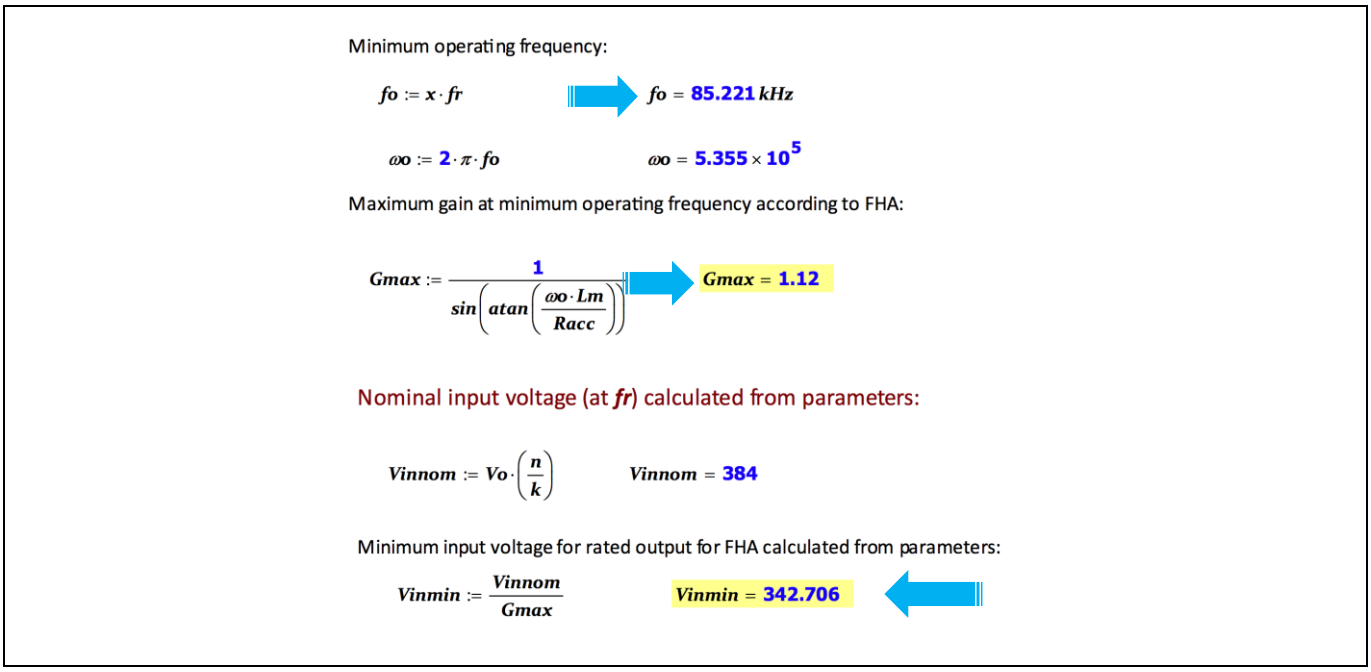

Figure 7 FHA reverse analysis of converter regulation capabilities confirming V_{in} = 350 V capability

In this calculation series, we verify a number of parameters from the tank configuration:

- The tank resonant frequency ***Fr(Hz)*** Fr(Hz) = 157.8 kHz
- The effective primary-side reflected impedance/resistance seen by the tank, R_{acc} = 49.8 Ω
- The tank quality factor at full load, ***Q*** = 0.307
- The predicted minimum operating frequency at full load ***fo*** = 85 kHz
- The maximum gain factor G_{max} = 1.12
- The nominal input voltage when the tank is at unity gain: V_{innom} = 384 V
- The predicted minimum V_{in} for which the proposed LLC tank system should be able to provide enough boost-up gain to achieve output regulation, V_{inmin} = 342.7 V

Reverse FHA analysis predicts that the Infineon/Finepower design fulfills the regulation range requirements for input voltage at low-line V_{in} = 350 V.

The question to pose, though, is does it do so in an optimal manner, considering a primary goal of minimizing the RMS currents on the primary and secondary side of the converter in order to minimize the conduction losses under most operating conditions?

2.6 MatLAB as a platform for SMPS design – LLC exact mode analysis with exact transient mode time diagrams and power margin analysis

What appears to be necessary and desirable is to have a baseline of accurate data from simulation or exact mode analysis, which can quantify the true potential behavior of the non-linear LLC tank design with output rectifier – not its approximate behavior using a highly simplified linear model. To this end, software for LLC analysis that runs under MatLAB (**Figure 8**) was obtained from power consultant Patrick Smeets in the Netherlands, based on time-domain analysis, as discussed earlier.

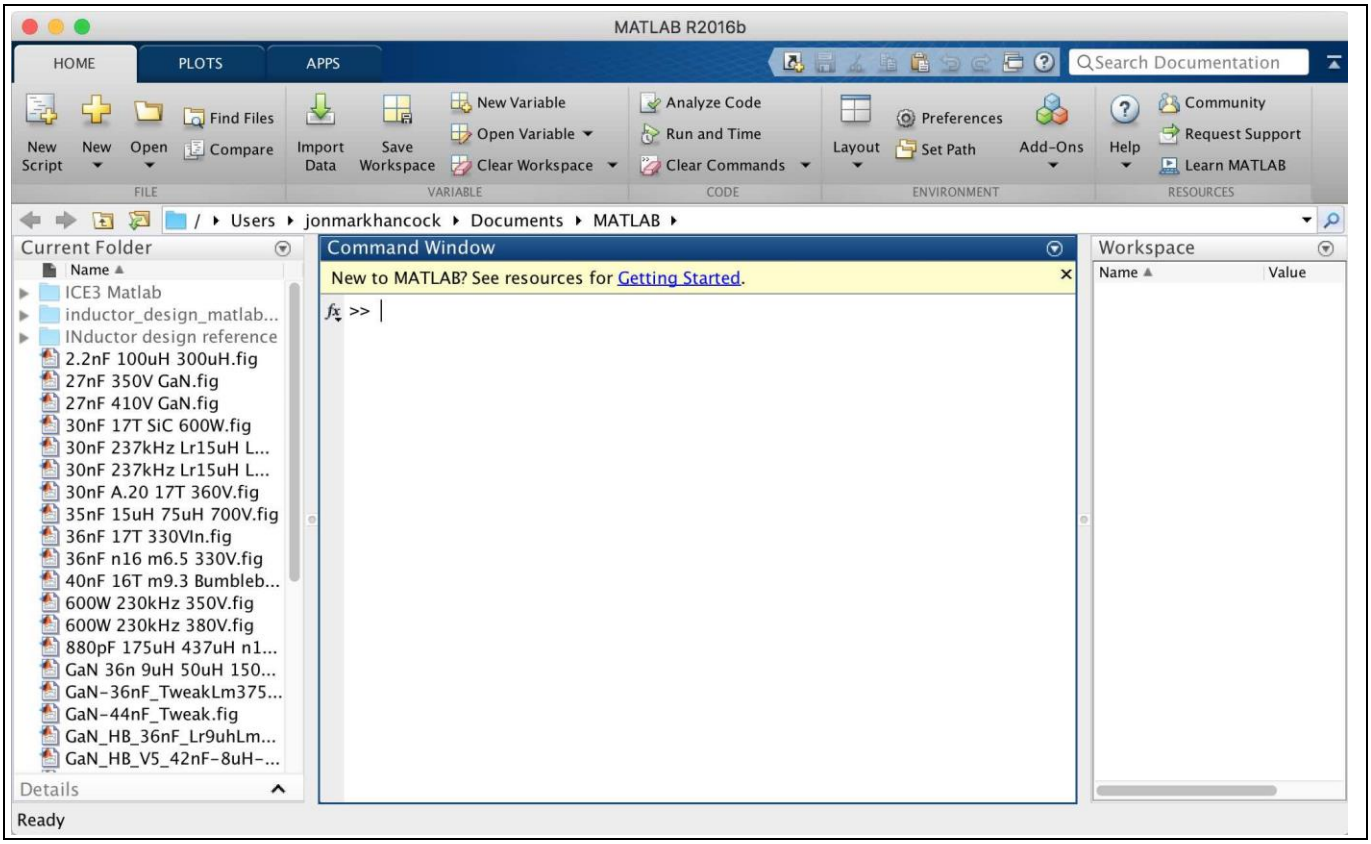

Figure 8 MatLAB environment for calculations and programming

This software supports closed-form exact mode analysis in the DCM region at resonance and below. Ideal components are assumed; the program makes no attempt to model losses in semiconductor switches or magnetic components. The behavior of the resonant tank and transformer on power capability and waveform analysis are the primary concern.

The operational behavior is somewhat different because of the necessity to provide full accurate operating point analysis – so the operating points for load, input voltage and tank characteristics are specified, and the swept parameter is the excitation frequency of the LLC tank, with a typical normalized range of 0.5 of Fr(Hz) to 1 (**Figure 9**).

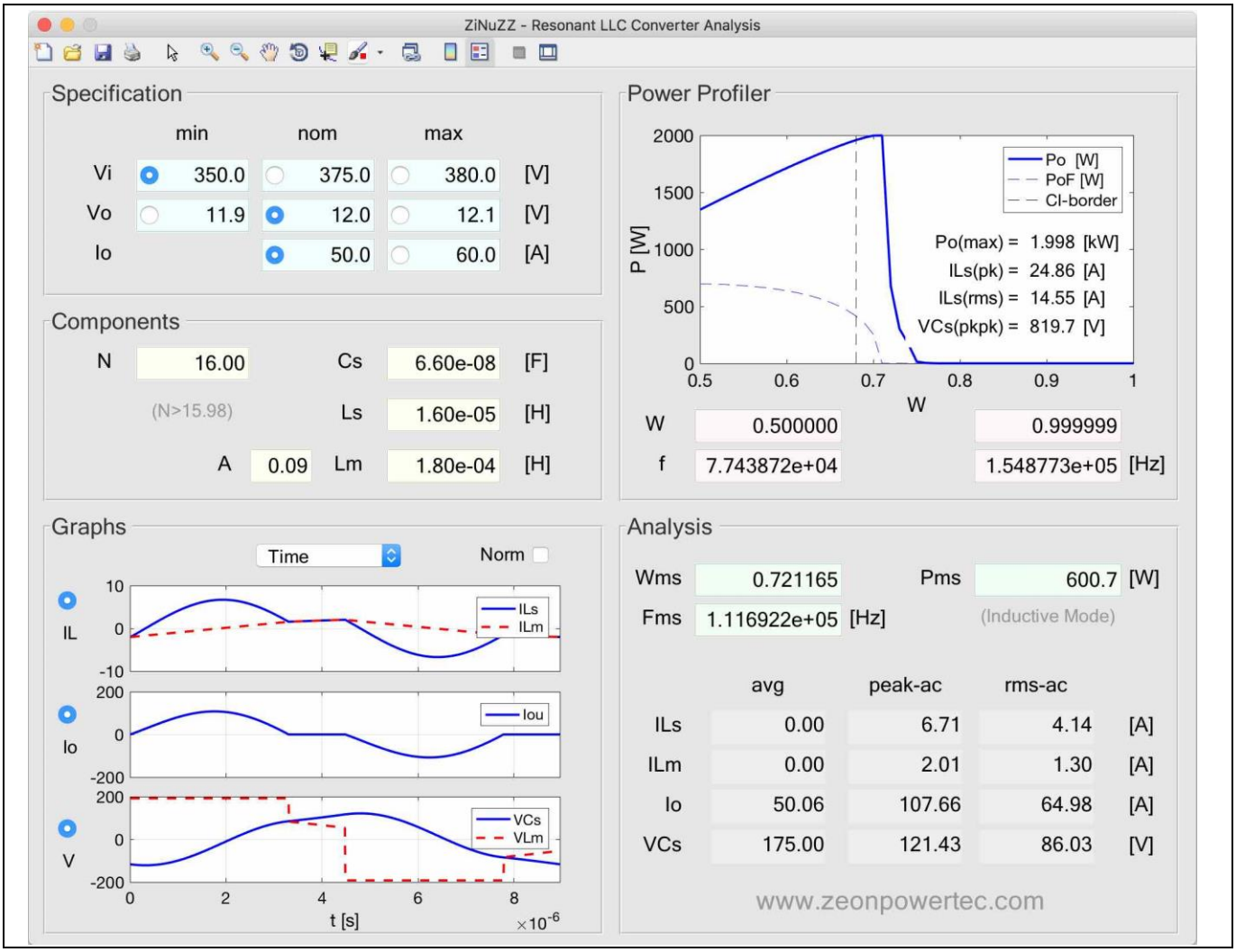

Figure 9 Single-pane panel for ZiNuZZ resonant LLC converter analysis software running on MatLAB

Two panes are used for data entry: “Specification” for the basic input and output voltage and load current parameters, and “Components” for the tank component values (Cs = Cr), (Ls = Lr), Lm, n = transformer turns ratio, and A, the direct ratio of Ls to Lm (not to be confused with the commonly used m-ratio, which would be (Ls+Lm)/Ls. Lm or A may be calculated or entered values. N is shown as a minimum value based on the specification entry, but may be raised to a higher value (such as rounding up for integer turns ratio).

Key operating features and capabilities include:

- Power capability at a given operating point as a function of FSW swept from 0.5 to 1 × Fr(Hz) or a sub-set thereof, with FHA mode and capacitive mode boundary plotted
- Instant operating point waveform analysis:
  - Relevant currents and voltages
  - State plane trajectories
  - Frequency spectrum of output current
  - Normalized and absolute scaling
- Instant operating point signal characteristics:
  - Relevant currents and voltages including I-Ls (I-Lr), I-Lm, I-O
  - Average, peak AC, and RMS AC values

2.7 The importance of the resonant capacitor behavior on line and load regulation

The resonant capacitor Cr serves more than one role. While, along with the resonant inductor Lr, it does define the resonant frequency and Q of the LLC tank, it is also in essence part of a resonant charge pump that defines the output capability of the complete LLC tank for each switching cycle, in conjunction with the magnetizing inductance Lm, which charges it up during the DCM mode dead-time.

Let's look at the LLC time diagrams at both just below the the nominal Fr(Hz) tank frequency, and in low-line boost-up operation.

2.7.1 Full-load nominal V_{in} = 380 V operating condition

First, for nominal input voltage of 380 V, the tank resonant current from the inductor (I-Lr) and the magnetizing inductance of the transformer (I-Lm) are shown in **Figure 10**, operating at full load at about 155 kHz. There is a short available dead-time interval calculated here of 200 ns, for the resonant switching transition. With the typical programmed dead-time interval of 300 to 350 ns, depending on the CoolMOS™ type, the LLC stage would likely be just nudging into the start of buck mode at this input voltage, depending on the exact value of Cr and Lr, considering the typical component tolerances.

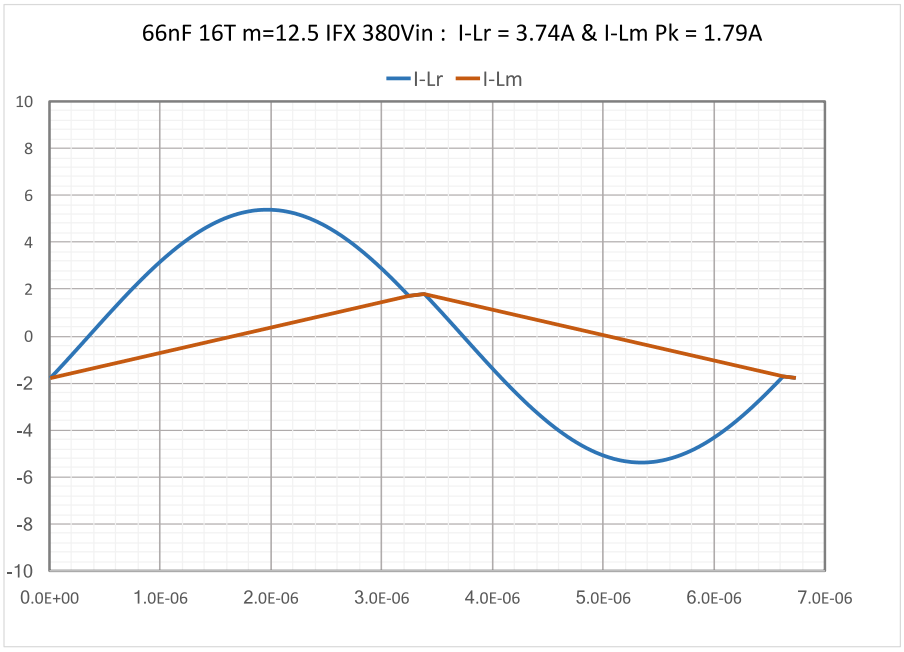

Figure 10 I-Lr, I-Lm for V_{in} = 380 V and FL

Figure 11 shows additional waveforms, including the voltage across Cr, the resonant capacitor, and the output current I-Out. Due to the very short DCM interval, Cr voltage and I-Out are fairly close to sine waves. In this very short DCM/dead-time interval, there is very little time for the magnetizing inductance current to charge up the resonant capacitor, and the gain transfer function of the Cr/Lr tank is essentially unity.

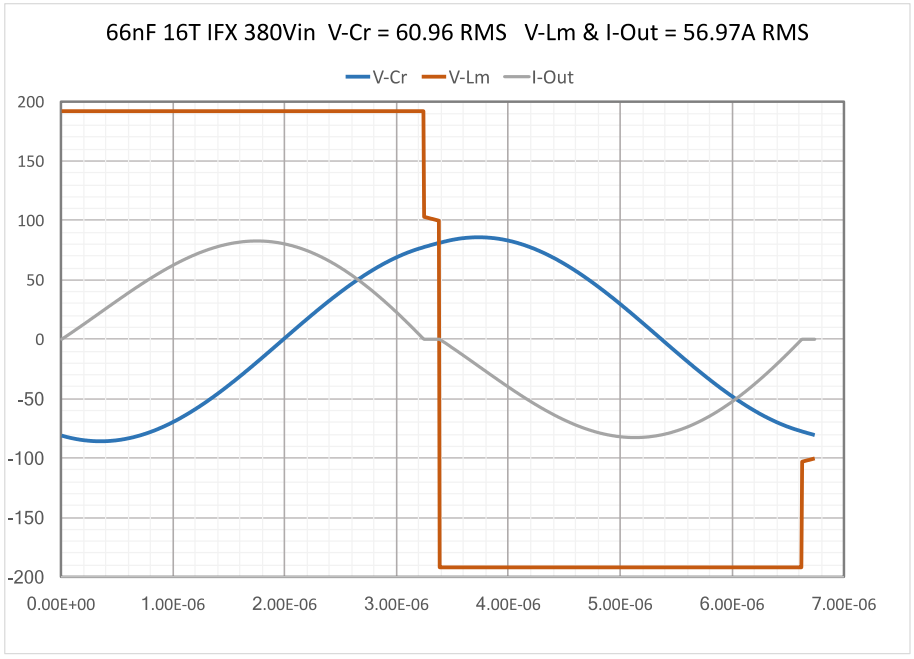

Figure 11 V-Cr, V-Lm, I-Out for V_{in} = 380 V and FL

2.7.2 Full-load low-line V_{in} = 350 V operating condition

At low-line condition, with V_{in} = 350 V, the situation looks quite different for the primary-side resonant tank current, as shown in **Figure 12**.

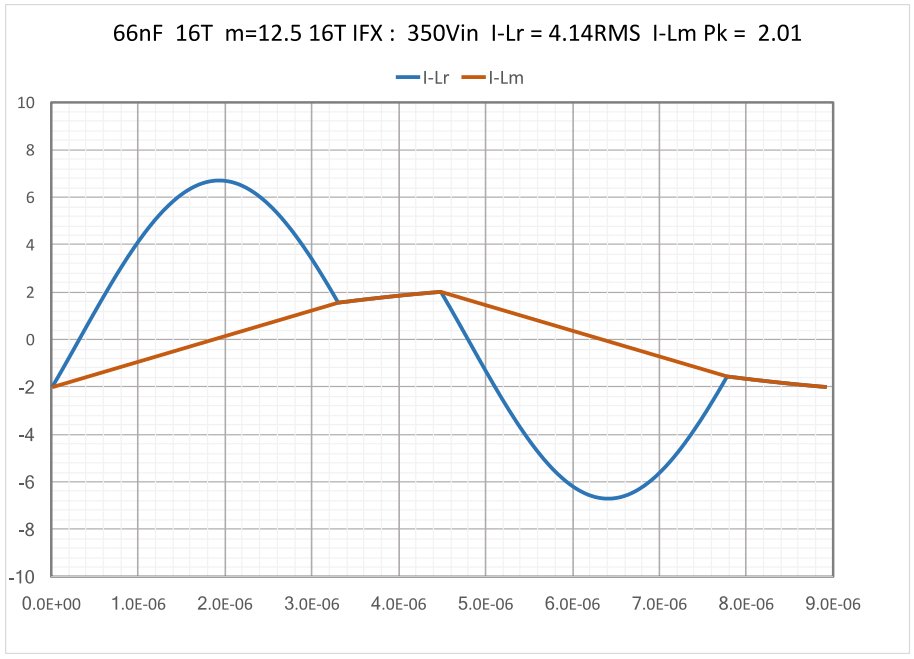

Figure 12 I-Lr, I-Lm for V_{in} = 350 V and FL

Now the DCM interval is fairly long, reflecting a drop in the normalized switching frequency to about 70 percent of Fr(Hz), and the peak I-Lm has risen somewhat, to about 2 A. The peak I-Lr has risen to about 6.8 A, from about 5.6 A at V_{in} = 380 V.

Figure 13 shows clearly the charge pump effect on Cr during the DCM interval, boosting the voltage across Cr by about 60 V, from 80 V to 140 V. This enables a higher power transfer to the secondary side, with a peak current of about 110 A at the output in order to deliver 50 A average, with the RMS output current increasing from 57 A to 65 A.

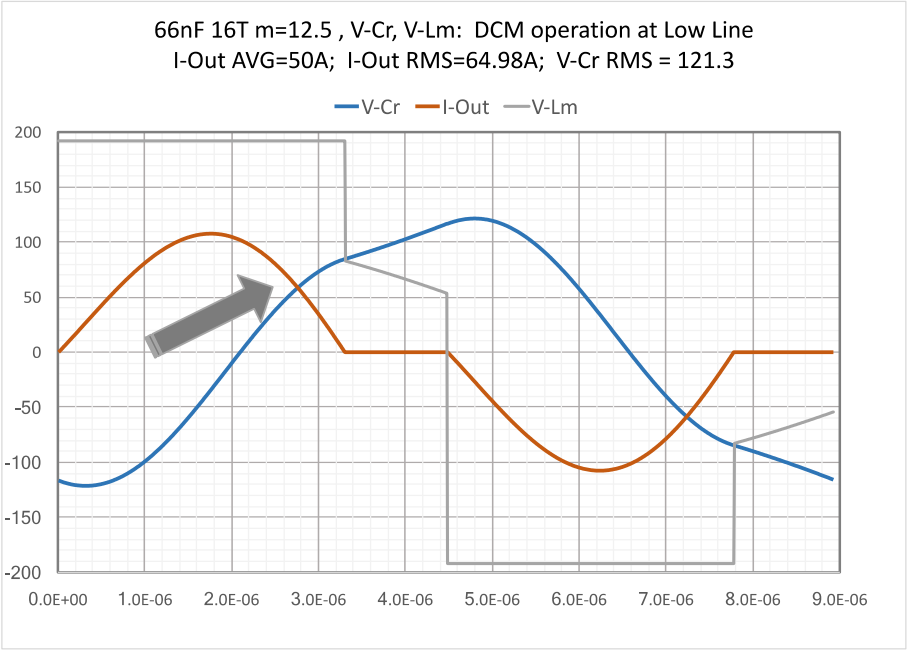

Figure 13 V-Cr, V-Lm, I-Out for V_{in} = 380 V and FL

2.8 Examining the RMS operating currents over the load range for V_{in} = 380 V and V_{in} = 350 V

A more detailed way to look at this difference in nominal-line vs low-line operating currents is to do an analysis for a multiplicity of operating points, at defined power intervals, from 25 W to 600 W output, and plot the results for both V_{in} = 380 V and V_{in} = 350 V.

The results of this are shown in **Figure 14**, which highlights the differences in RMS current for I-Lr, I-Lm Pk and I-Out over the load range, on both the primary and secondary sides. The impact of I-Lm also shows up in the total I-Lr value, which as expected, shows a tip-up at the lower power range due to the relatively fixed current requirement for I-Lm. This is why reducing I-Lm can be important for improving light-load efficiency.

Note that I-Out is plotted on the right-hand side Y-axis to preserve clarity for the lower current data on the primary side, which is plotted on the left-hand Y-axis.

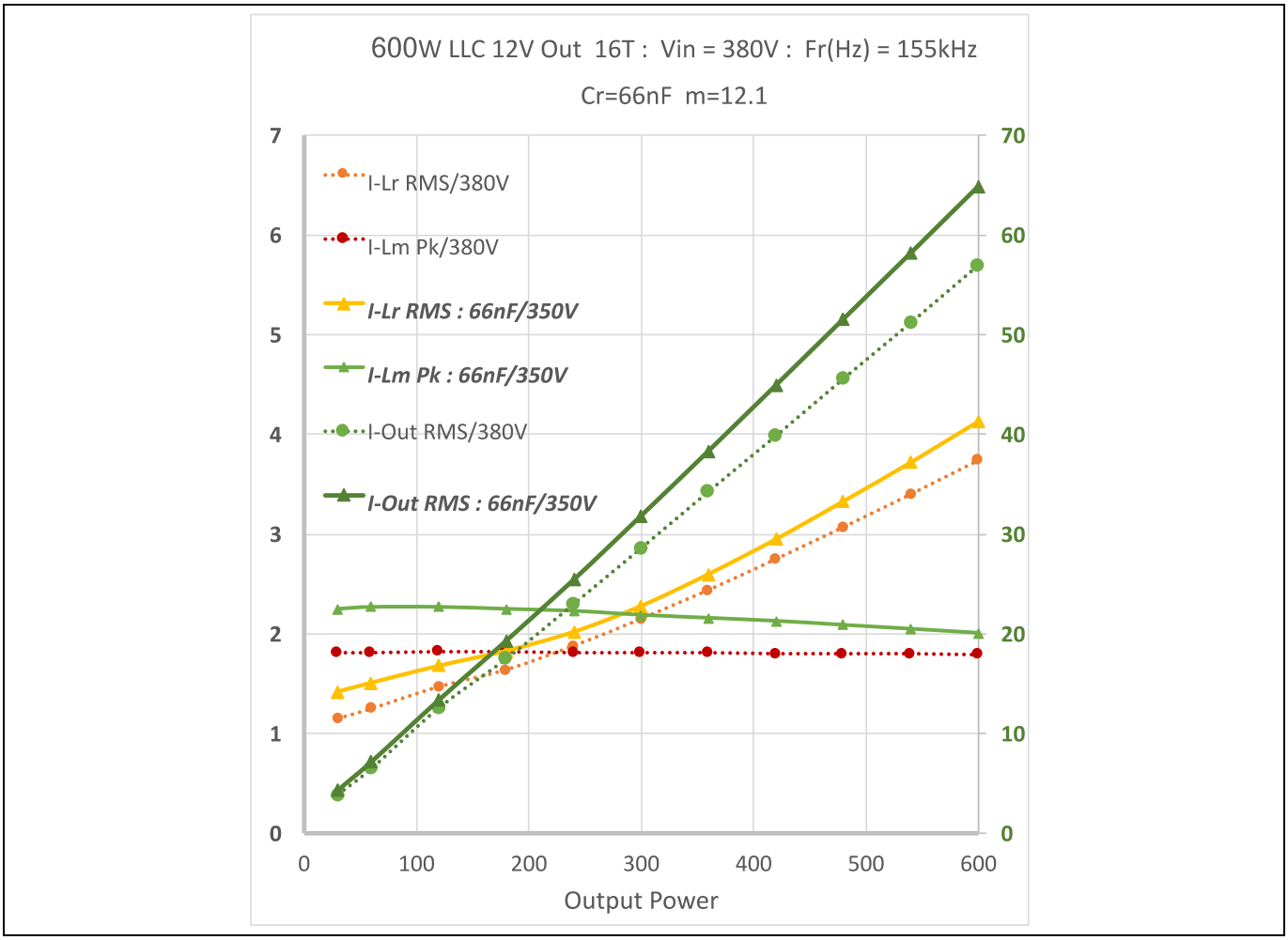

Figure 14 Operating load current for I-Lr, I-Lm-Pk and I-Out over 25 W to 600 W output range for 380 V (dotted) and 350 V (solid)

2.9 Comparing the power margin and output capability prediction of FHA vs exact calculation

Finally, for our review of the existing 12 V 600 W design, let's take a look at the power margin capability of this design, comparing FHA and exact calculation, as plotted in **Figure 15**. The FHA power capability shows good agreement with the previoiusly calculated reverse FHA analysis, showing an adequate power delivery capability in the area around a normalized switching frequency of 0.55, though not any appreciable extra margin.

On the other hand, exact mode calculation predicts a nearly 2 kW peak power capability in the area of normalized FSW = 0.7, and hardware simulation bears out this number. One might question whether power capability of three times the required nominal output power is really necessary, and if this impacts other aspects of performance. Are there possible benefits to a design which is tuned more accurately for the required output power, with a reasonable safety margin? This question will be explored further in section 2.11.

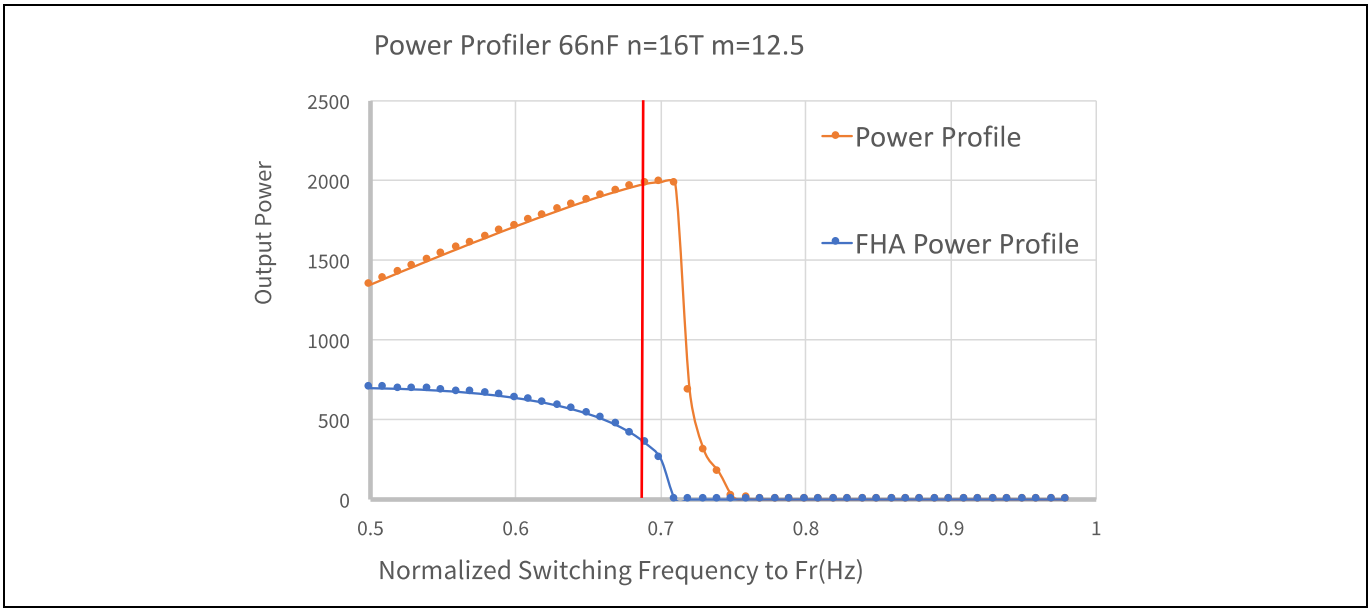

Figure 15 V-Cr, V-Lm, I-Out for V_{in} = 380 V and FL

2.10 Key points and principles for consideration after review and comparison of FHA calculated alignments with alignments optimized based on exact mode calculation

From this and many other calculation and simulation examples which time and space preclude from being included in this paper, some useful principles have emerged to be considered for LLC converter design.

- For a given Fr(Hz) tank resonant frequency, the value of the resonant capacitor Cr directly bears on the power capability of the LLC converter.
- While these results point to the possibility of substantial reductions in the value of Cr, with several attendant benefits, there are practical issues such as power margin and RMS voltage capability of the resonant capacitor Cr, which also should be considered.
- As an arbitrary choice, two power margin levels have been chosen for potential designs:
  - "Conservative," with a 100 percent power margin analysis – i.e., for a 600 W converter, a tank alignment theoretically capable of 1200 W at low-line input voltage is recommended.
  - "Aggressive," with just a 50 percent power margin capability at the rated operating point. This typically results in higher stress on Cr, as well as larger inductor requiements for Lr.
- Component issues around Cr and Lr selection are discussed in Part III of this series.
- Substantial reduction in the value of Cr requires an increase in the value of Lr, which is followed by a comparable increase in Lm for the same tank alignment. This reduces the primary-side I-Lm, with potential efficiency benefits on the primary for light-load operation.
- Reducing the RMS factor on the secondary side requires reducing the m-ratio, to shorten the DCM interval. This in turn decreases the value of Lm, increasing the primary-side loss at light load. However, this may be largely off-set by the reduction of Cr and increase in the value of Lr that are possible with an understanding of usable tank Q based on exact mode analysis instead of FHA.
- Decreasing m-ratios also drive higher charging of Cr, which supports higher output power for a given Cr, and hence, lowering the value of Cr; the drawback is requiring a capacitor technology suited to higher working AC RMS voltage capabilty.

Two conclusions emerge which suggest a useful test to evaluate:

- Conventional usage of FHA in the design process appears to result in higher than desirable current on both the primary and secondary sides, especially in low-line conditions, due to the Cr sizing and overall Q of the Cr/Lr network.
- It should be possible to develop working alignments which lower both the primary and secondary-side RMS current, with better overall efficiency over the full load range, and with a narrower control span over the line voltage regulation range.

This last assumption will be implemented and evaluated in the rest of this application note.

2.11 Alternative proposed tank alignments optimizing either light-load RMS current or low-line input RMS current

Two alternative alignments for the Infineon/Finepower 12 V 600 W LLC converter will be evaluated here – for one, the focus is primarily on improving light-load efficiency, while not compromising any other performance parameter – i.e., low-line efficiency must be as good or better than the original design, full-load nominal-line input performance as good or better, etc. The proposed alignment with m = 9.3 is focused on light-load efficiency, and the m = 6 alignment is focused on low-line efficiency. For these examples, the transformer ratio and operating range for boost mode vs buck mode are not altered.

Table 2 Tank parameters for original Infineon/Finepower 12 V 600 W LLC converter and two alternative alignments

LLC parameters	m = 12.5	m = 9.3	m = 6
Cr	66 nF	40 nF	32 nF
Lr	16 µH	27 µH	32 µH
Lm	185 µH	225 µH	160 µH
Transformer turns ratio n	16	16	16

2.11.1 Target: improving light-load efficiency

For this application target, the design direction is to increase the Cr/Lr tank Q to a more suitable target value (~0.5) while reducing the value of Cr by about 40 percent. While only doing this, and keeping the same m-ratio, would also have reduced I-Lm by 40 percent, a preferred compromise target for the m-ratio for relatively narrow input range that is required (350 V to 384 V in DCM range). An m-ratio of 9.3 was used, cutting the reduction in I-Lm current to just 20 percent, but with some attendant reduction of the RMS factor for output current to be expected at V_{in_min} = 350 V. If light-load efficiency is prioritized over low-line behavior, then an m-ratio of 10 to 12 could be considered.

These changes will result in alteration of the tank Q at full load from about 0.31 to 0.522, which by typical FHA calculations probably can’t meet low-line regulation. This will be checked along with the actual power magin potential at low-line input.

2.11.2 Target: improving low-line efficiency

For this alternative application target, the design requirement is to reduce the RMS current factor of I-Out for minimum V_{in} = 350 V, while desiring to match as nearly as possible the nominal input voltge RMS current values, and compromising light-load efficiency minimally.

This requires a more aggressive m-ratio in the range of 6 to 7, which also allows further reduction in the value of Cr while still being able to meet regulation targets. Detailed analysis shows that this smaller value for Cr does result in a higher AC RMS voltage and frequency capability, and requires taking more care in component selection. Analysis and simulation show 150 VRMS at 133 kHz for the 32 nF alignment at full load and V_{in} = 350 V, vs 86 VRMS at 111 kHz. More details will be discussed about this in Part III for component selection.

2.11.3 Reverse FHA regulation analsyis of light-load efficiency optimized design

Reverse analysis using FHA was done for the 40 nF alignment, to confirm the basic calculated parameters for Fr(Hz), R_{acc}, Q, and m-ratio.

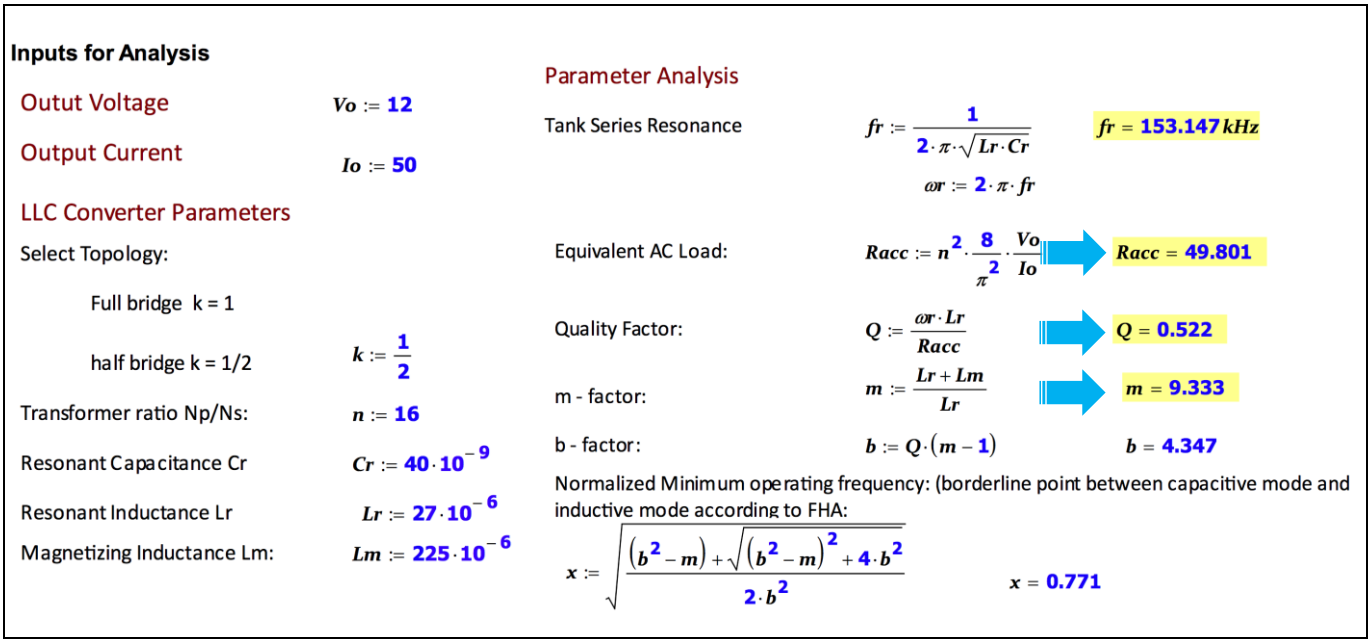

Figure 16 LLC converter definition and calculation of basic LLC parameters from tank values for alignment for enhanced light-load efficiency

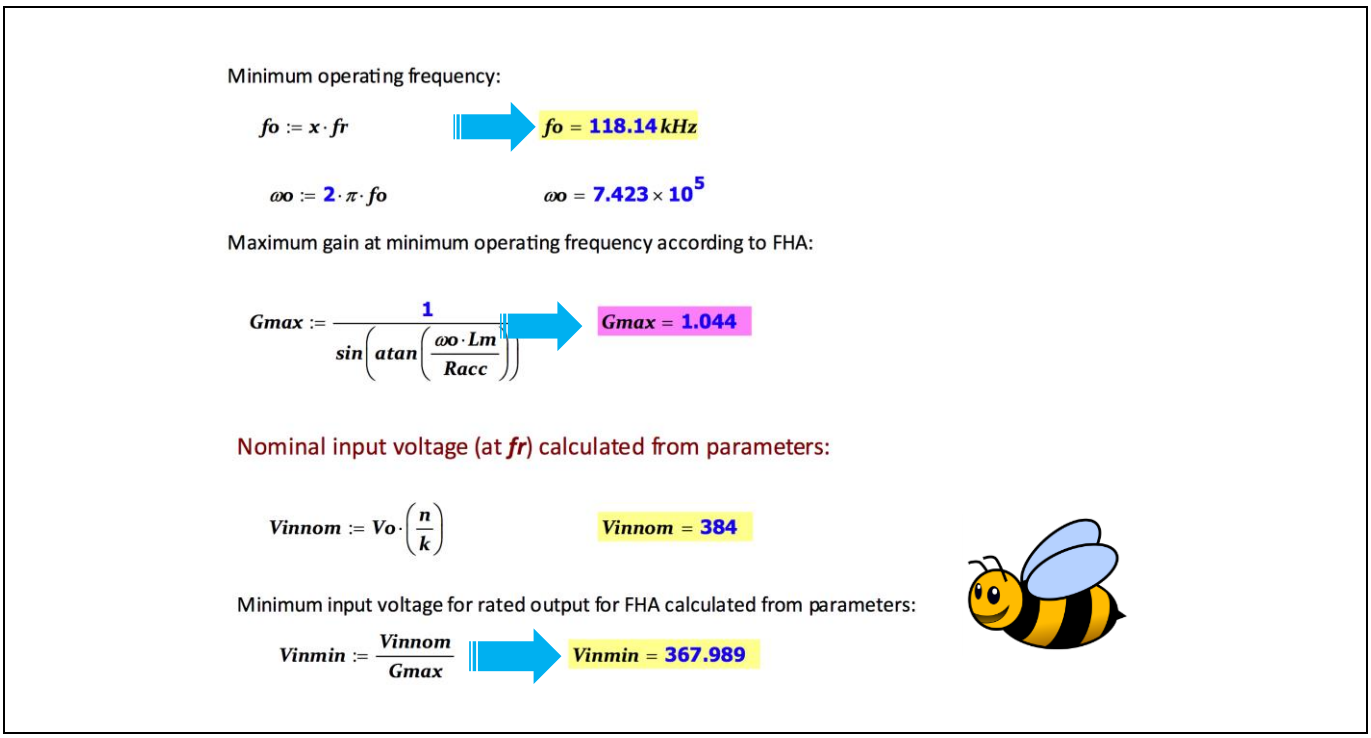

Figure 17 FHA reverse analsyis of converter regulation capabilities for V_{in} = 350 V indicates this alignment can't meet regulation targets. The bumblebee cannot fly … or can it?

In this reverse FHA calculation for the 40 nF alignment, with m = 9.3, we can verify a number of parameters from the tank configuration:

- The tank resonant frequency ***Fr(Hz)*** Fr(Hz) = 153 kHz
- The effective primary-side reflected impedance/resistance seen by the tank, R_{acc} = 49.8 Ω
- The tank quality factor at full load, Q = 0.522
- The minimum operating frequency at full load ***fo*** = 118 kHz (?)
- The predicted maximum gain factor G_{max} = 1.044 – does not meet requirements
- The nominal input voltage when the tank is at unity gain: V_{innom} = 384 V – is as expected
- The minimum V_{in} for which the proposed LLC tank system should be able to provide enough boost-up gain to achieve output regulation, V_{inmin} = 368 V – does not meet requirements

Reverse FHA analysis predicts the 40 nF/m = 9.3 design doesn't meet the regulation range requirements for input voltage at low-line V_{in} = 350 V.

Next, we'll look at the predicted capability with exact analysis.

2.11.4 Exact power margin analysis for Cr = 40 nF tank design

A power profile was prepared for the 40 nf/m = 9.3 alignment including predicted FHA capability. While this tool also confirms that FHA predicts a shortfall in meeting 600 W output requirement, exact analysis shows a theoretical capability (before component losses) of over 1300 W peak, which meets the desired conservative 100 percent margin capability for a 600 W design. This capability was duplicated in full non-linear simulation in LTspice.

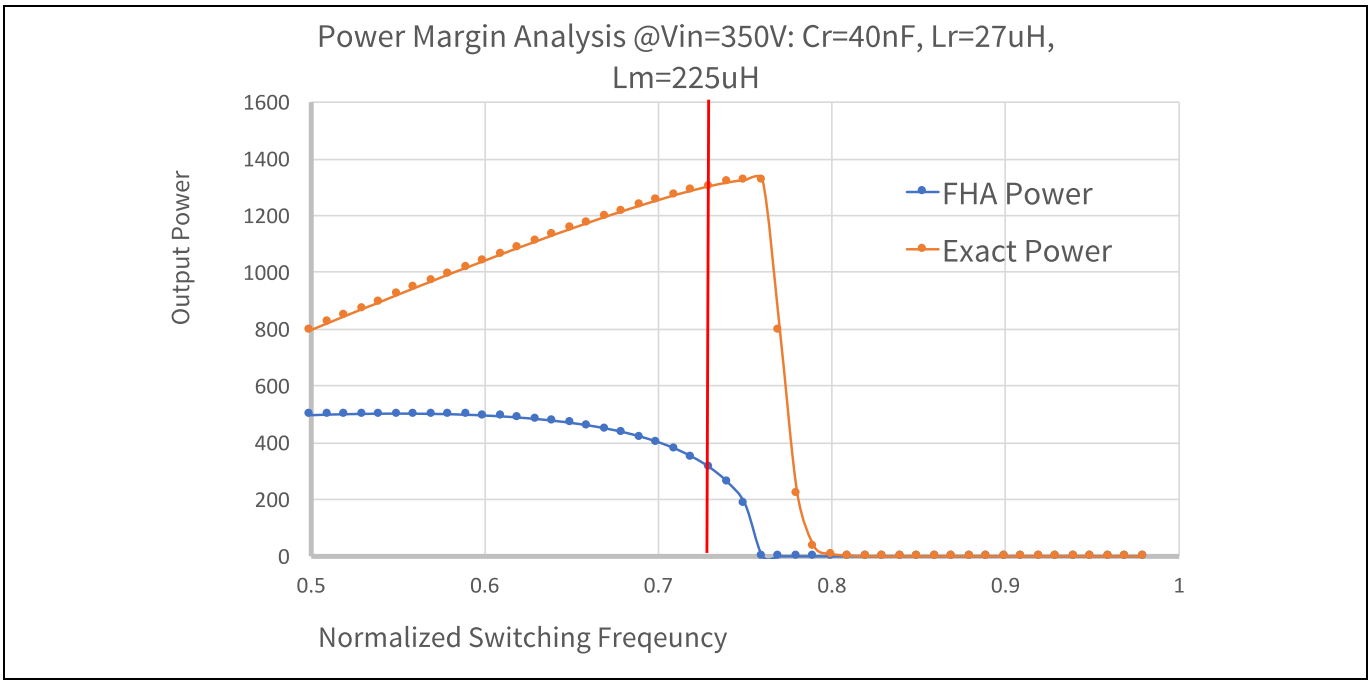

Figure 18 Power margin at V_{in} = 350 V for tank configuration with Cr = 40 nF, m = 9.3

2.11.5 Comparison of RMS currents for the three-tank configurations at V_{in} = 380 V RMS

The next step is to compare the RMS currents for each tank alignment at operating power points from 25 W to 600 W, as was done in **Figure 14** for the original design at V_{in} = 380 V and V_{in} = 350 V.

Figure 19 shows this for V_{in} = 380 V for the three alignments.

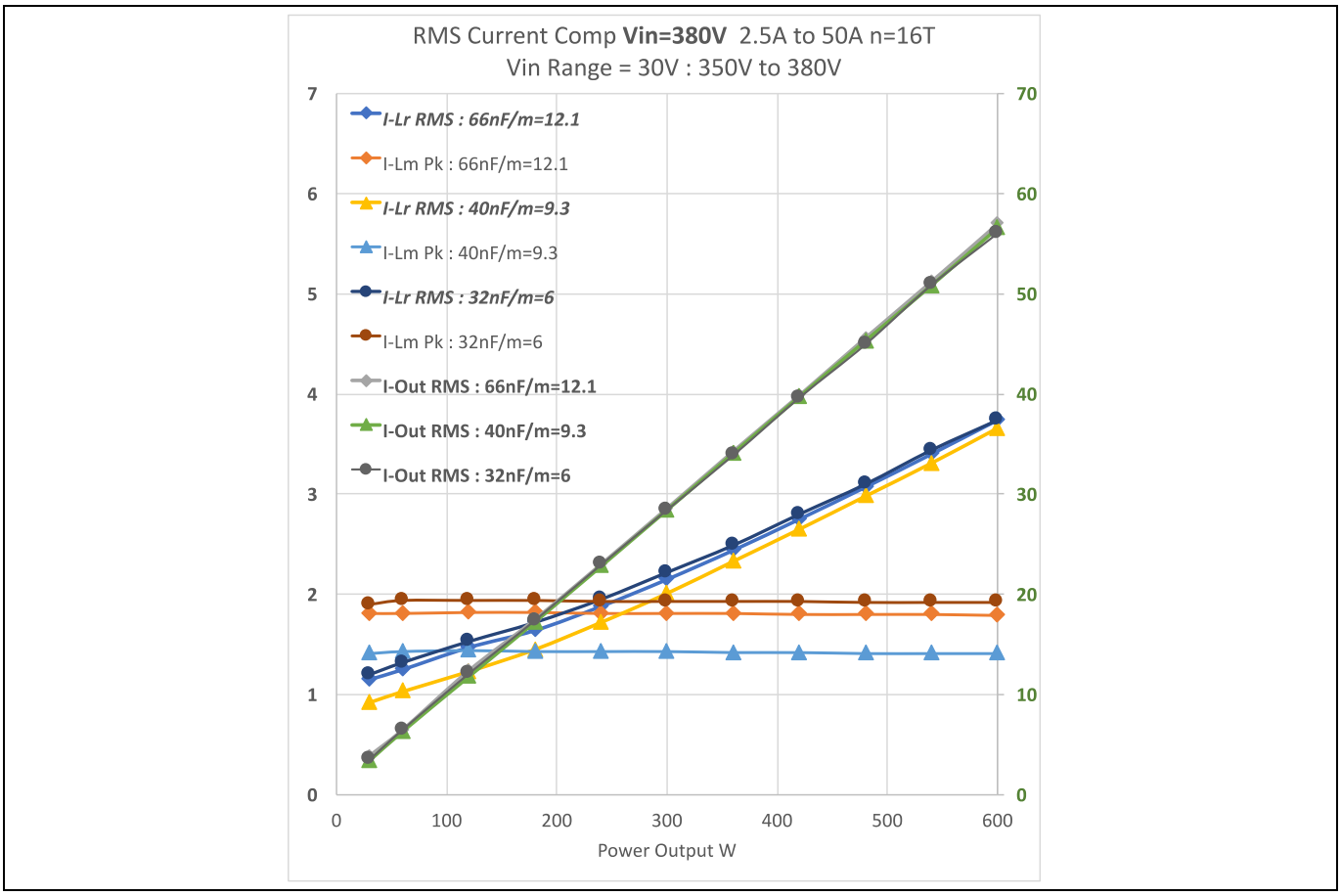

Figure 19 RMS current comparison at V_{in} = 380 V

A few points should be noted when interpreting the results:

- Because the input voltage puts the operating frequency nearly at the Fr(Hz) resonance for all alignments, I-Out tracks very closely, as the RMS factor is nearly identical.
- Peak I-Lm tracks as would be expected for the variation in magnetizing inductance Lm, and as expected the 40 nF alignment has the lowest value, and the lowest value for I-Lr RMS current over the entire input voltage range, by about 25 percent.
- The 32 nF tank design tracks just a tiny bit higher on I-Lr current than the nominal 66 nF Cr design, but the I-Out RMS current is calculated as very slightly lower.
- The values are summarized to two decimal places in **Table 3**. The lowest RMS current values are in **bold face**. As might be expected for V_{in} = 380 V, the 40 nF alignment outperformed the original 66 nF alignment by varying amounts over the full output range, but especially at light-load conditions. Hoever, at full load and V_{in} = 380 V, the 32 nF had the lowest I-out current by nearly 0.5 A compared to 40 nF alignment, and nearly a full ampere compared with the 66 nF alignment.

Table 3 RMS current comparison of alignments for LLC alignments at V_{in} = 380 V

Operating condition	66 nf m = 12.5	40 nF m = 9.3	32 nF m = 6
50 A output: I-Out RMS	56.97 A	56.45 A	**56.03 A**
50 A output: I-Lr RMS	3.74 A	**3.66 A**	3.74 A
50 A output: I-Lm Pk	1.79 A	**1.41 A**	1.92 A
20 A output: I-Lr RMS	1.88 A	**1.72 A**	1.95 A
10 A output: I-Lr RMS	1.47 A	**1.23 A**	1.53 A
10 A output: I-Lm Pk	1.82 A	**1.44 A**	1.94 A
2.5 A output: I-LR RMS	1.15 A	**0.92 A**	1.2 A
2.5 A output: I-Lm Pk	1.81 A	**1.41 A**	1.9 A

2.11.6 Comparison of RMS currents for the three-tank configurations at V_{in} = 350 V RMS

Figure 20 graphs and compares the RMS current results for the low-line condition, V_{in} = 350 V. The general trends are similar, but now the I-Out differences for RMS factor are quite pronounced.

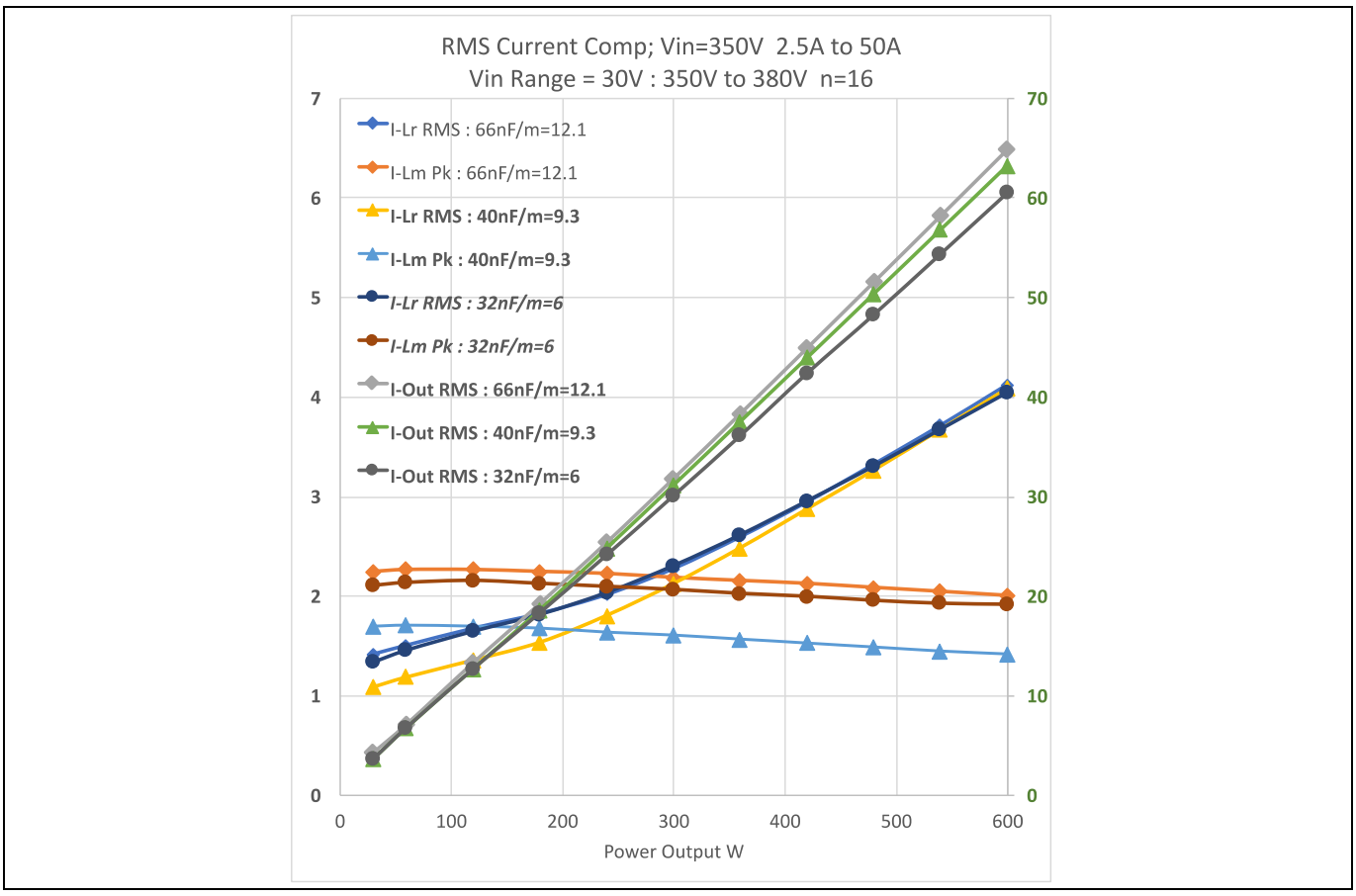

Figure 20 RMS current comparison at V_{in} = 350 V

- Peak I-Lm tracks similarly, but is higher overall due to the lower operating frequencies, as each design is now operating at F_{min}.

- The 32 nF tank design tracks about the same now for I-Lr current as the nominal 66 nF Cr design, but the I-Out RMS current comes in much lower, about 7 percent less current, which translates to nearly 14 percent less power dissipation due to $I^2 \times R$.
- Even the 40 nF design ostensibly optimized for light load comes in 2.5 percent lower on RMS output current at full load, amounting to nearly a 5 percent lower power dissipation if the output-side resistance is equivalent.
- The values are summarized to two decimal places in **Table 3**. The lowest RMS current values are **in bold face**. As might be expected for V_{in} = 350 V, the 32 nF alignment out-performed the original 66 nF alignment by a solid percentage for output RMS current over the whole output range, but especially at heavy-load conditions.
- Under light-load conditions, from 1/3 load and less, both the 40 nF and 32 nF alignments have lower predicted RMS current than the original 66 nF alignment.
- In no case did the original FHA-based alignment have lower RMS current than the alternatives at either 380 V input or 350 V input for any output current value.

Table 4 RMS current comparison of alignments for LLC alignments at V_{in} = 350 V

Operating condition	66 nF m = 12.5	40 nF m = 9.3	32 nF m = 6
50 A output: I-Out RMS	64.9 A	63.3 A	**60.55 A**
50 A output: I-Lr RMS	4.13 A	4.09 A	**4.05 A**
50 A output: I-Lm Pk	2.01 A	**1.42 A**	1.92 A
20 A output: I-Lr RMS	25.45 A	24.89 A	**24.19 A**
10 A output: I-Out RMS	13.37 A	12.77 A	**12.76 A**
10 A output: I-Lm Pk	2.27 A	**1.70 A**	2.16 A
2.5 A output: I-Lr RMS	1.42 A	**1.09 A**	1.34 A
2.5 A output: I-Lm Pk	2.25 A	**1.70 A**	2.11 A

2.11.7 Power profile check of 32 nF alignment and FSW_{min} comparison of the three alignments

One last cross-check was run, to check the power profile of the 32 nF I-Out optimized alignment, as shown in Figure 21. The results meet the "conservative" alignment criteria with 100 percent power margin, and also highlights that FHA would not show this alignment as regulation capable.

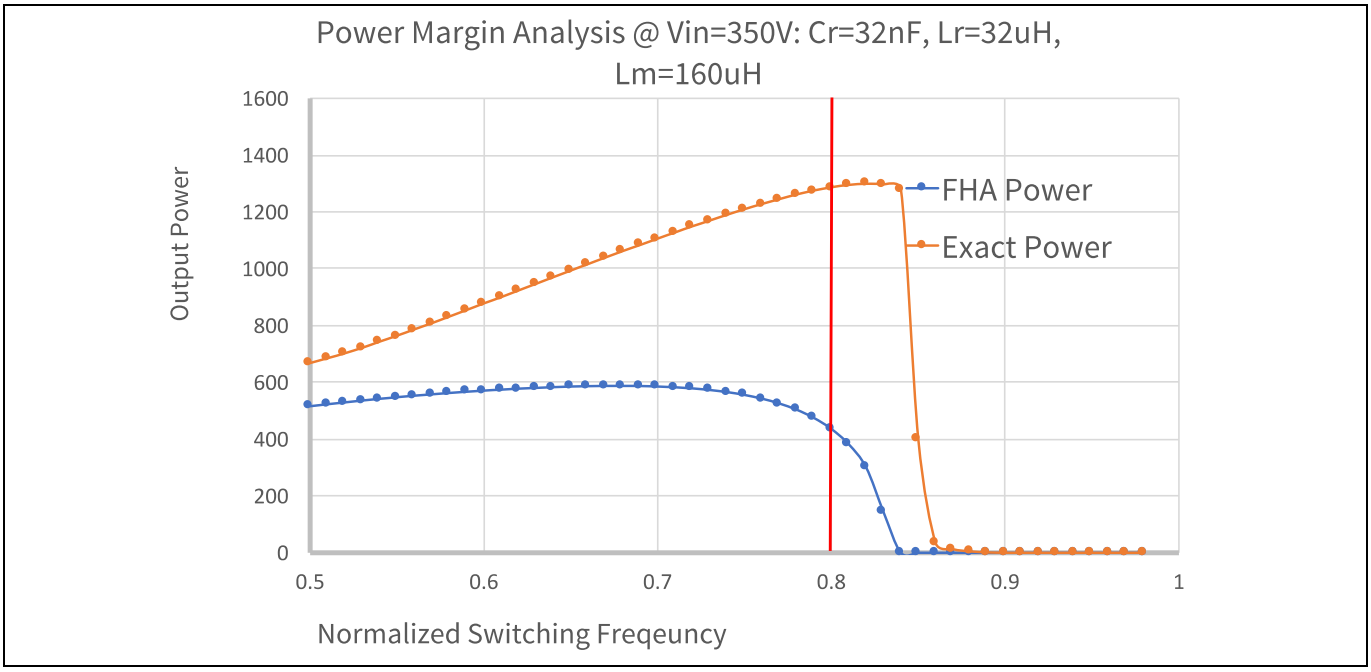

Figure 21 Power margin analysis at V_{in} = 350 V for tank configuration with Cr = 32 nF, m = 6

The normalized and nominal low-line switching frequencies are shown in **Table 5** for each alignment. The F_{min} moves as expected based on the different m-ratios. Given a higher RMS voltage capability for the resonant cap Cr, the 32 nF alignment can cover a wider input range.

Table 5 Minimum normalized FSW for regulation of three alignments at V_{in} = 350 V

Operating condition	66 nF m = 12.5	40 nF m = 9.3	32 nF m = 6
50 A output: I-Out RMS	FSW_{min} = 111 kHz	FSW_{min} = 118 kHz	FSW_{min} = 133 kHz
	Normalized FSW = 0.72	Normalized FSW = 0.77	Normalized FSW = 0.84

3 Using a more effective LLC design process to optimize power density and input range capability

A closer look at operating gain and power capability targeting a wide input range 12 V 600 W design

A design process which utilizes the LLC tank more effectively also has potential for addressing performance requirements besides optimized efficiency. A common plea from SMPS customers is not for ever higher efficiency, beyond a point, but for greater output power in the same size box. With existing designs already using single-turn windings in some cases, such as the Infineon/Finepower 12 V 600 W LLC converter, conventional approaches with reduction of magnetics component sizes by frequency are not likely to enable the desired improvement in density. How can we reach these system design targets though better LLC tank fundamentals?

3.1 Target issues and other problems…

There are a number of concerns and issues that should be discussed in the context of a high-performance LLC design realizable with a more realistic design approach than FHA. Such designs should be applicable in the real world – a majority of LLC evaluation boards on the market seem designed to operate from high-power DC lab supplies, with a narrow input voltage range, and not from an active power factor unit. There are some concerns and requirements that need to be addressed:

- For LV output designs, we are coming up against limitations in transformer size reduction because single-turn output designs are already in use, and the required window area to control conduction losses leaves little opportunity for core volume reduction.
- Other components, such as bulk input caps and EMI filters, are now tending to dominate the volume requirements for AC-DC supplies. Can the design of the LLC converter be leveraged at all to reduce the size of these components?
- Are there ways to usefully optimize the LLC converter design with Wide Band Gap (WBG) switches? Higher frequency by itself is not necessarily a useful feature.
- Output filter size and allowable ripple voltage is another factor that can limit density, depending on the operating frequency range of the converter – large m-ratios don't serve this requirement well, as operating at minimum V_{in} may increase the voltage ripple at the output substantially compared with operating at Fr(Hz).

Some potential issues and solutions…

- In the low to medium power area, it may be a challenge to use matrix transformer construction with series windings and paralleled secondaries, but at higher powers this may pay off in reducing primary-side dissipation, and give better ratios of core volume to cooling area.
- Bulk capacitors must smooth the AC ripple current from the active PFC filter, and provide hold-up during a skipped cycle line event. With relatively narrow input voltage range, such as 350 V to 384 V in DCM/boost, to 410 V with buck, larger capacitors are required. If an extended input range is possible, such as 300 V or 330 V to 405 V while purely in DCM/boost mode, then capacitor size can be adjusted **or** greater power can be delivered from the same volume.
- WBG switches reduce the I-Lm requirements and dead-time, allowing more latitude in the transformer and tank efficiency trade-offs, and safer operation at high frequency in protection modes.
- High-power WBG LLC designs with LL normalized FSW of 0.575 at 350 V stress the output filter capability for smoothing at high frequency with heavy DCM operation due to the much lower ripple frequency. Limiting the control frequency span to a more workable range is mandatory for both filter performance and efficiency.

3.1.1 Typical core loss and turns count issues affecting transformer size

Figure 22 highlights the transformer design challenge, showing an overview of approaches that could be considered for 12 V output LLC in the range of 600 W to 1 kW [2]. More turns (32T primary, 2T secondary) will lower the core excitation losses, cutting them in half for a moderate switching frequency below 100 kHz, but will quadruple the winding resistance, due to double the turns and half the wire cross-section. Moving to a PQ40-40 format core will help with the core window area available for windings, but will also increase the core volume, and reduce the cooling surface area in proportion to core and winding losses. This can be a primary argument for at least reducing the primary-side winding requirements by using a series connection of two transformers, and cutting the volt-seconds support requirements for each core in half.

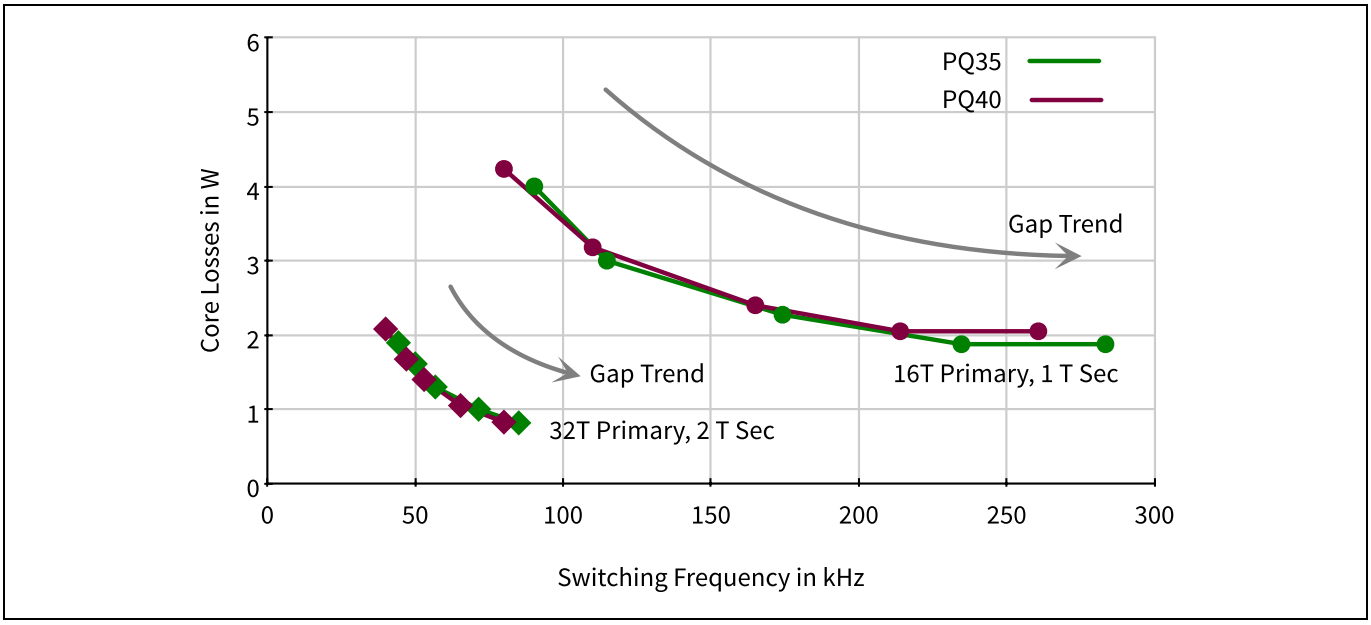

Figure 22 Core loss comparison for PQ cores for 2T secondary and 1T secondary

3.2 Guidelines and boundary conditions for ROT approach

The boundary conditions and guidelines are intended to inform and modify the use of the LLC calculator program to achieve optimum results for both minimizing RMS currents on the primary and secondary sides and optimizing the frequency control range span and line regulation performance. Topics include:

- a detailed look at the RMS to average current behavior, and how it may inform the ratio of minimum operating frequency to Fr(Hz) resonance frequency
- power margin at minimum V_{in} for a given LLC tank configuration
- recommended targets for F_{min}.

3.2.1 RMS current to average current ratio at low-line input

The inability to identify and predict the true RMS factor for output and input current vs frequency is one of the key weaknesses of FHA-based tools, due to their simplified assumption of a variable frequency sine wave. Let's look at this in detail, regarding its roots in the DCM mode waveforms of the LLC converter operating anywhere below resonance. This was highlighted earlier in **Figure 12** and **Figure 13**, showing the time diagram for input current and output current for the Infineon/Finepower 12 V 600 W LLC converter with V_{in} = 350 V.

A function in MathCAD shown in **Figure 23** can be used to plot and verify the average and RMS current factor for haversine waveforms with variable haversine period duty cycle in relation to the total period, and a specific average output current Io:

$$isx(x, p, Io) := \begin{cases} \left(\frac{Io \times p \times \pi}{1 - \cos(p \times \pi)} \times \sin(p \times x)\right) & \text{if } \left(x \le \frac{\pi}{p}\right) \wedge (p < 1) \\ \left(\frac{Io \times p \times \pi}{2} \times \sin(p \times x)\right) & \text{if } x \le \frac{\pi}{p} \\ 0 & \text{otherwise} \end{cases}$$

Figure 23 Function for plotting RMS current for haversine wave as a function of ratio of total period to haversine period

If we use this function and plot we can see the analogous effect of DCM mode operation on the peak current for the same average current in **Figure 24**. What is not equivalent to the LLC is that the total period here is fixed, and the haversine wave period is varied; in the LLC, the haversine is fixed and the total period varies. But the RMS factor calculated is the same for the same ratio of haversine period to total period. The period multiplier for the plots is varied from 1 (essentially a sine wave, both periods equal) to 1.8, which corresponds to heavy DCM mode, equivalent to a normalized switching frequency of 0.55 of the resonance frequency Fr(Hz).

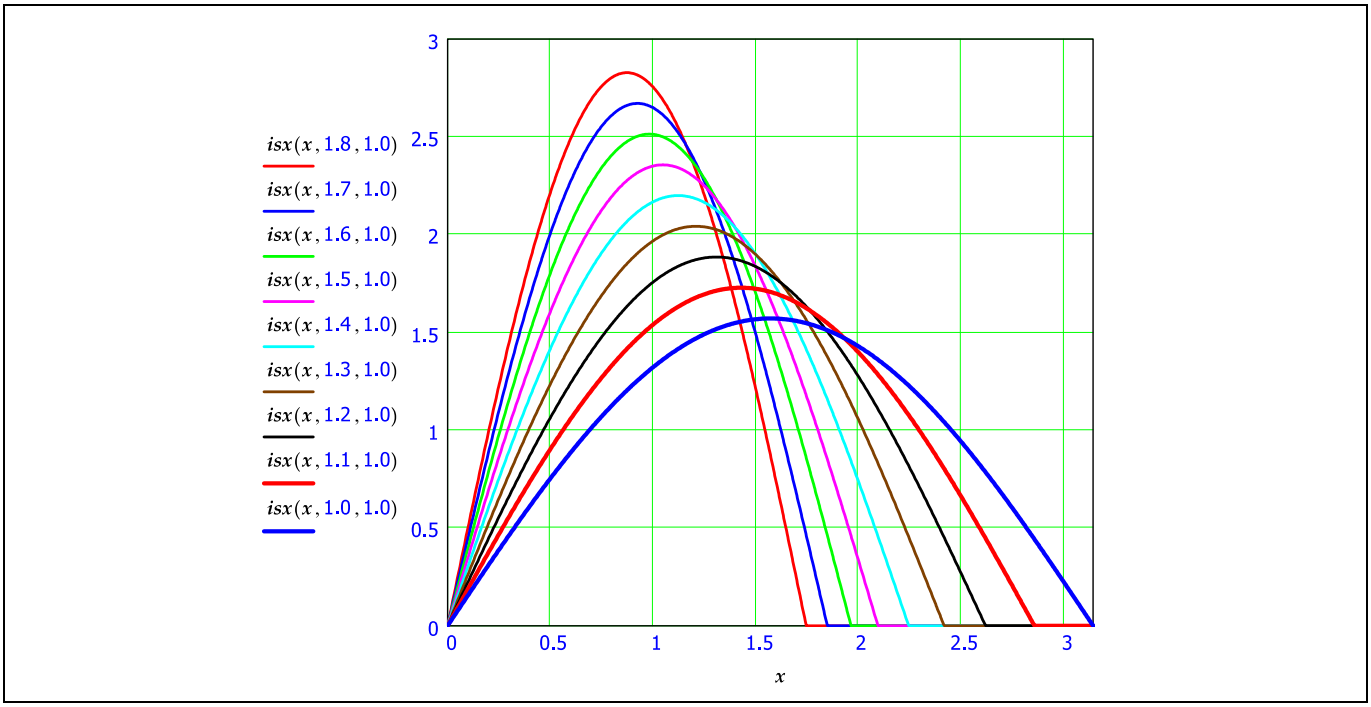

Figure 24 Plots of haversine waveforms with variable total period ratio to haversine ratio from 1 to 1.8

The average current Iav and the RMS current $Irms$ can be calculated from these waveforms using two related functions in MathCAD shown in **Figure 25**, to verify that the displayed waveforms are all equivalent to the same average current, and to calculate the RMS current factor increase as a function of the period duty cycle, which impacts the efficiency due to increase of power losses for the same output current. The RMS current defines the true heating factor for the operating current.

$$\text{Average Current: } iav(x, Ipk) := \frac{1}{x \times \pi} \times \int_0^{\pi} f(\alpha, Ipk)\, d\alpha$$

$$\text{RMS Current: } Irms(x, Ipk) := \sqrt{\frac{1}{x \times \pi} \times \int_0^{\pi} f(\alpha, Ipk)^2\, d\alpha}$$

Figure 25 Calculation of average and RMS current from haversine waveforms of I_{pk} with variable DCM interval

The average current for each parameter set and the RMS current are shown in **Figure 26**, verifying that each waveform dataset for varying duty cycles represents the same average output current, and the RMS current factor is calculated for comparison and plotting in **Figure 27**.

Average Current	RMS Current
$iav(1.0,1.571) = 1$	$Irms(1.0,1.571) = 1.111$
$iav(1.1,1.728) = 1$	$Irms(1.1,1.730) = 1.166$
$iav(1.2,1.885) = 1$	$Irms(1.2,1.885) = 1.217$
$iav(1.3,2.042) = 1$	$Irms(1.3,2.042) = 1.266$
$iav(1.4,2.2) = 1$	$Irms(1.4,2.2) = 1.315$
$iav(1.5,2.357) = 1$	$Irms(1.5,2.357) = 1.361$
$iav(1.6,2.514) = 1$	$Irms(1.6,2.514) = 1.405$
$iav(1.7,2.671) = 1$	$Irms(1.7,2.671) = 1.449$
$iav(1.8,2.828) = 1$	$Irms(1.8,2.828) = 1.49$

Figure 26 Average current and RMS current results for total period to haversine period ratios of 1 to 1.8 for waveforms created from the function of Figure 23

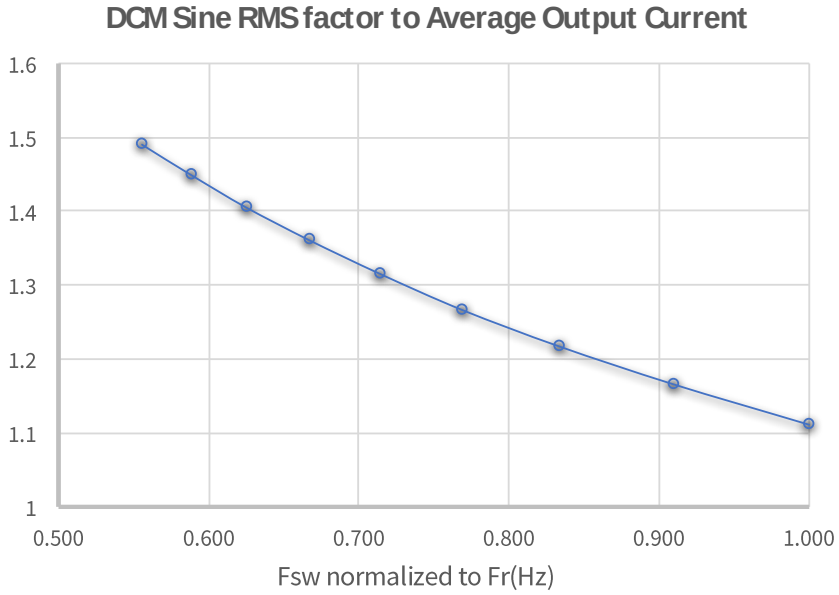

Figure 27 RMS current factor increase as a function of reducing normalized switching frequency

The best-case RMS factor ratio occurs at resonance, with an RMS to average current ratio of 1.111, or 11 percent greater. At a normalized FSW of 0.55, this rises to 49 percent greater, and at a normalized FSW of 0.5 is about 57 percent greater. For high-output current converters, this should be a clear disincentive to using large m-ratios with a low normalized switching frequency, even for just a fixed output with occasional input under-voltage. For appications such as battery chargers or telecom systems which must regulate over a significant output voltage range, the RMS current factor as a function of normalized switching frequency should be considered carefully in choosing the tank alignment. For higher efficiency, limiting F_{min} to 0.7 or above is a good strategy.

3.2.2 M-ratio for normalized F_{min} at low-line input

Adjustment of the m-ratio has a first order effect on achieving a specific tank gain and normalized F_{min}. How does this relate to the examples for the Infineon/Finepower 12 V 600 W LLC converter discussed in the section 2 design review? The RMS factor for the V_{in} = 350 V condition is about the same at 26 to 27 percent, for the original design (**Figure 15**) with F_{min} at 0.74 and the light-load optimized design (**Figure 18**) at 0.77. This RMS factor is about 15 percent over the value at the Fr(Hz) resonance.

The difference comes in with the tank Q at the full-load operating point: ~0.3 for the original design with Cr = 66 nF, and ~0.5 for the light-load optimized version with Cr = 40 nF, and which is off-set by the optimized version using a lower m-ratio of 9.3 instead of 12.5. This moves the F_{min} up in frequency, reducing the RMS current factor, and increases the M_{nom} gain level.

The design with an m-ratio of 6 and Cr = 32 nF has an operating normalized FSW of about 0.84, as shown in **Figure 21**. This does result in a 7 percent reduction in RMS current for the optimized design, and output current-related conduction power dissipation that is 13 percent lower compared with the original version.

While using a wider input voltage range for minimum normalized FSW can have some potential power density benefits for dealing with hold-up times, for a steady-state variation of regulation range such as in battery charger systems such as telecoms or other applications, restricting the normalized FSW to a range of 0.75 or higher may have clear efficiency benefits, and may be a wiser trade-off than optimizing for light-load efficiency. It depends on the desired overall system target. With informed analysis, making that decision is the choice of the designer.

Lower m-ratios than often calculated via FHA optimization will have several benefits:

- They will result in lower RMS factors for output current, due to higher F_{min} at $V_{in} = V_{min}$
- They will result in a wider margin from capacitive mode, due to higher F_{min} at $V_{in} = V_{min}$
- They will result in more attenuation at light and no load in the buck region

Suggested ROT starting points for m-ratio and light-load efficiency optimization:

- For a line input range of 10 percent in DCM, (such as 350 V to 385 V) recommended m-ratio is no more than 9 to 10
- For a line input range of 15 percent, (such as 330 V to 390 V) recommended m-ratio is in the range of 7.5 to 8.5
- For a line input range up to 20 percent, (such as 315 V to 395 V) recommended m-ratio is in the range of 6.5 to 7.5
- For a line input range up to 25 percent, recommended m-ratio is in the range of 6 to 7, depending on the need for light-load optimization and the RMS voltage capability of Cr. In this case, the performance focus would be bulk capacitor sizing to optimize supply power density, not light-load efficiency, as the I-Lm value wil be higher in order to get the boost-up capability.

For suggested approaches for m-ratio and low-line RMS current factor optimization, much lower m-ratios may be used in some cases, depending on targets for light-load efficiency and low-line efficiency, using m-ratios in the range of 6.5 to 7.5 even for somewhat narrow input range requirements such as 35 V to 40 V. This also may be the preferred choice if some range of output voltage adjustment is required, as for a battery charging system, as the low m-ratio will intrinsically give a greater total regulation range, regardless of how it's distributed at the input or output.

Tank alignments with smaller values of Cr for the same V_{in_min} and F_{min} will result in significantly higher values of RMS voltage on Cr. This can be verified in simulation at $V_{in} = V_{in\_min}$, and should be taken into account in

selecting the capacitor technology and voltage rating. This will be discussed in more detail in Part III, where component technologies for LLC converters are discussed in detail with application requirements.

3.2.3 Impact of quality factor of Lr+Cr tank and V-Cr limits

The quality factor of the Cr-Lr resonant network has a direct bearing on the achievable output power – the higher the capacitance, and hence the lower the Q, the greater the power capability. Cr is key to the output power capability. But using a higher Cr value than necessary sets the inductive components (Lr and Lm) to lower values and increases the I-Lm current, which does not contribute directly to delivered output power near resonance at Fr(Hz). Hence, it is a conductive power loss on the primary.

At larger m-ratios (typically 8 and upward) and moderate input voltage span (with the difference between nominal line and low-line about 10 percent of the nominal line value), using FHA the usable Q to achieve line regulation is about 0.3. In the real world, higher Q can be used and still have good power margin, typically 0.45 to 0.55. Reducing the value of Cr in this way allows corresponding increases in the value of Lm for the same m-ratio, allowing the improvement in light-load efficiency. The reduction in calculated Cr may be from 30 percent up to 40 percent, as seen in the previous example reducing Cr from 66 nF to 40 nF.

At the lower end of generally useful m-ratios, 6 to 7, FHA methods will calculate a higher Q and the potential reduction in Cr may only be 20 percent. This still has a useful impact on reducing I-Lm, and keeping F_{min} in a higher range more favorable for efficiency than FHA predicts.

Moving in this direction requires care in the selection of the Cr capacitor, as the RMS voltage requirements increase as the value is decreased. For example, in the case of the two additional 155 kHz 12 V 600 W alignments, comparing RMS currents and V-Cr RMS voltage in **Figures 27 to 30**, the smaller Cr requires a 25 percent increase in RMS voltage capability. In typical cases, this may simply require using a HV rating of the same general technology and capacitor value, such as moving from a metalized film capacitor at 630 V DC to the same technology at 1000 V DC or 1200 V DC. This will be examined in more detail in Part III of this series.

3.2.4 Design power margin

Power margin cannot be accurately assessed by FHA. As already shown in section **2.11**, it predicts that the LLC tank cannot deliver required power at low-line for designs that are shown capable of delivering up to two times the required power. Simulation or exact mode analysis should be used. In this paper, we describe two general cases for power margin ROT:

- **Conservative power margin:** with a two-times theoretical capability (100 percent) over nominal full load.
- **Aggressive power margin:** with only 50 percent theoretical capability over nominal full load, using a smaller value of Cr and higher Lm for the same Fr(Hz), and requiring greater RMS voltage capability for the Cr capacitor.

Power margin, light-load optimization and Cr as well as V-Cr operating limits are intrinsically linked:

- Aggressive optimization of Cr also means higher V-Cr operating voltage requirements and smaller power margin.
- This optimization can be used to minimize light-load I-Lm or to minimize RMS factor by raising F_{min} for the operating range through using a lower m-ratio.

3.2.5 Using WBG switches to advantage – managing an optimal control frequency span for switches, magnetics and output filter

WBG switches are in some cases capable of very high switching frequencies, but using that capability indiscriminately may not benefit overall system performance. It is quite possible to develop a 400 kHz nominal Fr(Hz) at 390 V DC input converter, while optimizing for primary-side current using conventional techniques, and arrive at a design with a very wide m-ratio (15 to 17) and a very wide frequency control span requirement. Such a design might support 350 V low-line, but with a normalized FSW of 0.58 (~230 kHz) with a nominal V_{in} of 380 V for normalized FSW of 0.84 (332 kHz), and be operating at the threshold of buck mode and degraded SR behavior at V_{in} = 390 V. Over-current conditions or PFC bulk over-shoot then require switching well over 600 kHz. We will show that this is not an optimal design path.

Where WBG switches can excel is in reducing the energy needed for resonant transitions, and then tuning the converter to optimize system performance. Possible approaches include:

- Designing for a narrower frequency control range with a lower Fr(Hz) in line with realistic dead-time (set by I-Lm and Q_{oss})
- Tuning for a narrower frequency control range with a higher minimum FSW for minimum line input voltage, better RMS factor on output current (0.675 to 0.7 for 330 V LL) and lower HF ripple voltage on output filter
- Designing for nominal Fr(Hz) at 405 V, to stay away from AC-line ripple voltage effects from PFC running at full power at nominal 385 V to 390 V
- Selecting an operating frequency range that can be supported by existing secondary-side synchronous rectifier switching characteristics

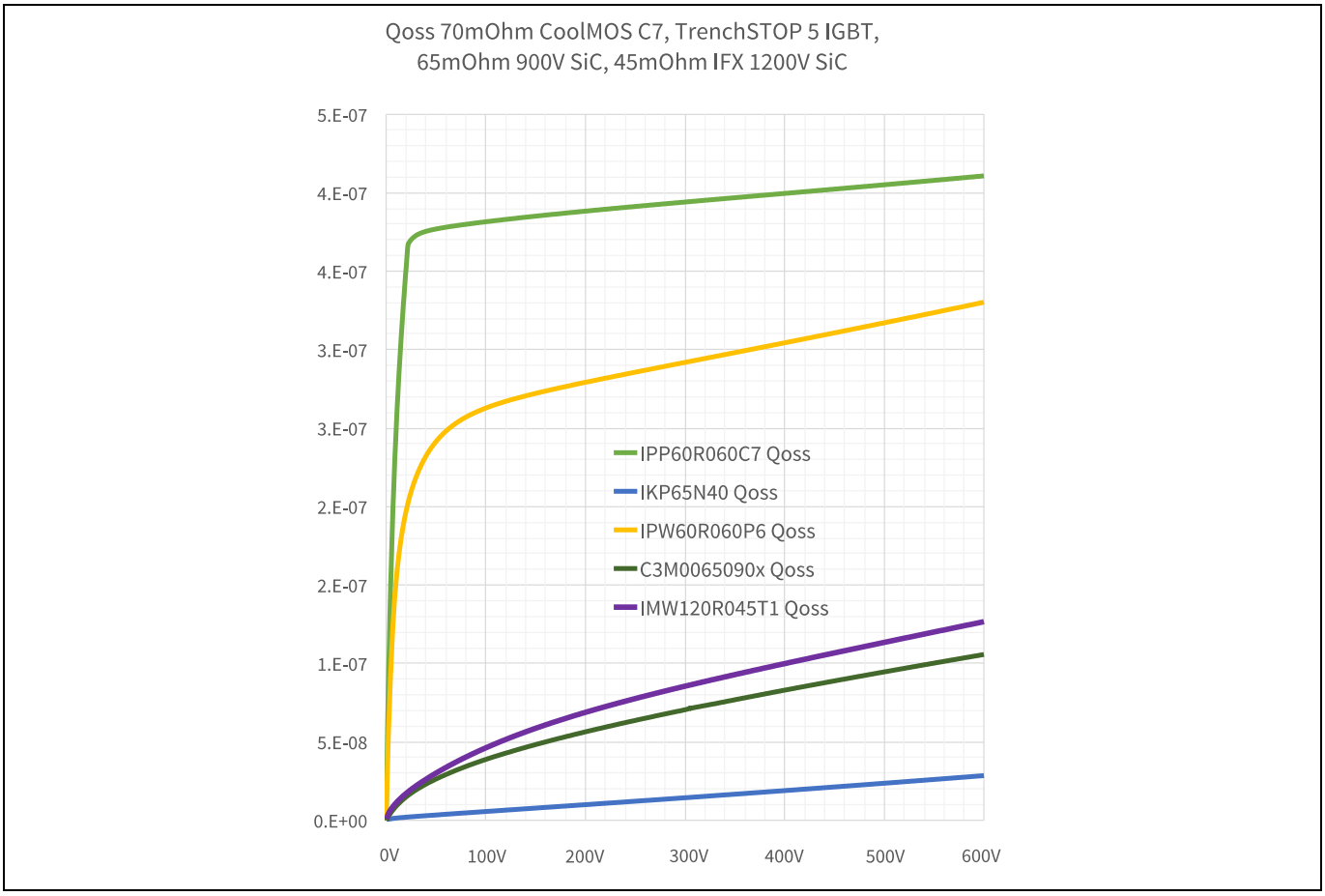

Figure 28 Q_{oss} comparisons of 45 to 70 mΩ class HV switches – 600 V and higher

3.2.6 Using a wider input range LLC tank design to reduce bulk capacitor size and volume (target: improved converter power density)

In modern SMPS it's already becoming the case with silicon switches that components not thought of as directly being affected by switching frequency have a great impact on the total volume and achievable power density. While it may not be obvious at first that the converter design can be optimized to reduce the size of those components, such as the bulk hold-up capacitors, this approach is needed to make real progress for both improving density and reducing cost.

Considering the original case study chosen here, the Infineon/Finepower 12V 600 W LLC converter, to what degree can the bulk capacitor size be addressed? A key parameter for selection of the bulk capacitor is the capacitance value needed to provide 10 ms of hold-up time during the loss of AC input power. In turn, this depends heavily on the supported input voltage range for delivering rated output – the wider this input range can be, the smaller the cap value size, as long as other capabilities such as RMS current capability are met.

The required bulk capacitor size can be estimated from the PFC output power, the hold-up time required, the nominal output voltage, and the minimum output voltage:

$$C_{Bulk} = \frac{2 \times Pfc_{Power\_out} \times T_{Holdup}}{V_{Out^2} - V_{min^2}}$$

In **Table 6**, we compare the operating range possibilities and calculated bulk capacitor values for some new potential design alignments, with different alignment trade-offs for wide input range vs light load efficiency. These are not the only possible solutions, but they highlight in several steps the potential for reducing bulk capacitor value and size.

Table 6 Hold-up time 10 ms and bulk capacitor size

LLC converter description	V_{in} nominal	V_{in} minimum	Calculated bulk cap value	Bulk cap value in commercial sizes
Original 12 V/600 W LLC n = 16 Cr = 66 nF; Fr(Hz) = 155 kHz; m = 12.5	380 V DC	350 V DC	640 µF	680 µF
Modified alignment for best light-load Cr = 27 nF; Fr(Hz) = 230 kHz; m = 7.5; n = 17	395 V DC	350 V DC	418 µF	470 µF
Modified alignment 1 for wide range Cr = 30 nF; Fr(Hz) = 230 kHz; m = 7.5; n = 17	395 V DC	330 V DC	298 µF	300 µF
Modified alignment 2 for widest input range Cr = 40 nF; Fr(Hz) = 230 kHz; m = 7.5; n = 17	395 V DC	300 V DC	212 µF	220 µF

The bulk capacitor value must be selected from the commercial value equal to or or greater than the calculated value required. For the smaller values, using two capacitors or more in parallel at half the value may be necessary to meet the RMS current requirements at line frequency.

3.3 Alternative wide input range designs and their transfer functions

Some design examples with variations will now be explored, using many of these concepts, to highlight how the LLC calculator may be of use in that process, and to show the achievable correlation in gain parameters between using the LLC calculator with ROT, and exact mode analysis. This wide input range example presents more of a challenge to the LLC design process than a typical 30 V to 40 V line input range example.

This is introduced as a preamble to the walk-through on the ROT procedure in section 4 for using the LLC calculator as a design visualization and synthesis tool.

3.3.1 Design using LLC calculator with FHA with no modification

First, let's take a look at the entry and results for using the LLC calculator with only small modifications of input procedure. Consider first the user data entry, as shown in **Figure 29**:

- Nominal input voltage is set to 405 V – this sets the desired range for operating at the tank resonance Fr(Hz), and any input capability above that is handled in buck mode. This also defines the operating point for turns ratio in relation to the specified output voltage, at essentially n = 17T.
- Minimum input voltage is set to 300 V, output current is in the normal range with a small buffer, and as this is assuming a WBG switch design for now, as a starting point Fr(Hz) is set 50 percent higher than the original 12 V/600 W design, at 230 kHz. From **Figure 22**, this puts core losses at the lowest possible level for a 1T secondary design, whether using a PQ3535 or PQ4040. A similar tank design can be done at lower Fr(Hz) (125 kHz to 150 kHz) with CoolMOS™.
- The maximum M_{max} boost gain required is ~1.35; the variable minimum frequency is adjusted for Cr to fall on an available commercial value (2 × 20 nF), resulting in a slightly modified m-ratio of 7.5, and a tank Q of 0.33. Lr is taken as 12 µH, and Lm as 80 µH, rounding from the values in the LLC calculator.

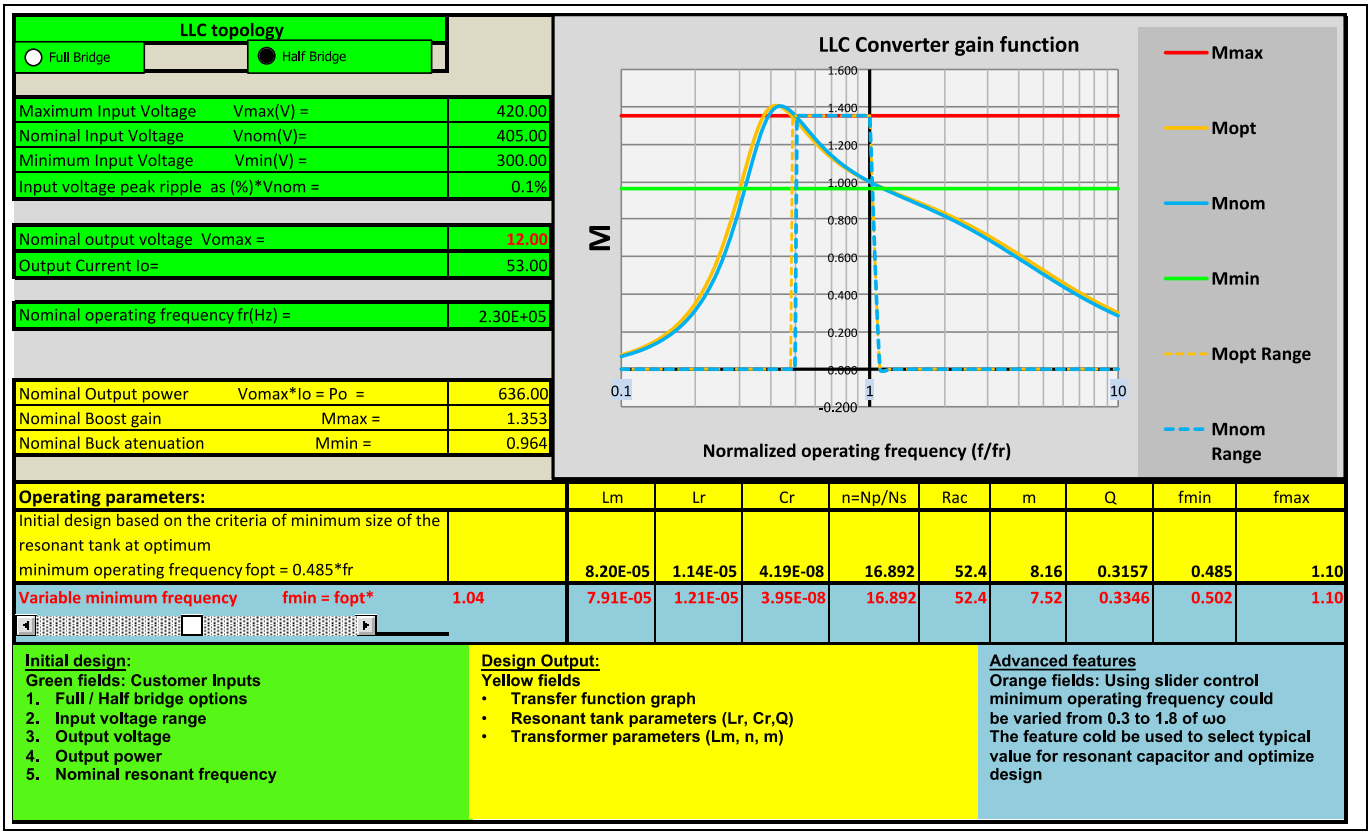

Figure 29 LLC calculator for 50 A wide input range design with Fr(Hz) = 230 kHz; Cr = 40 nF

Gain vs FSW graphs were prepared this time as a check against the LLC calculator, using exact mode analysis, in addition to the RMS operating current and voltage as a function of the normalized FSW. This is time-consuming compared with the LLC calculator, as each operating point has to be calculated individually and then combined in a single graph.

Comparing the LLC calculator and an exact mode gain plot created with MatLAB and Excel, the general similarity is apparent, but the specifics of F_{min} are clearly different, with the LLC calculator showing a low normalized frequency of 0.5, and the exact mode calculation showing the required M_{nom} at Normalized Switching Frequency (NFSW) = 0.613 (**Figure 30**).

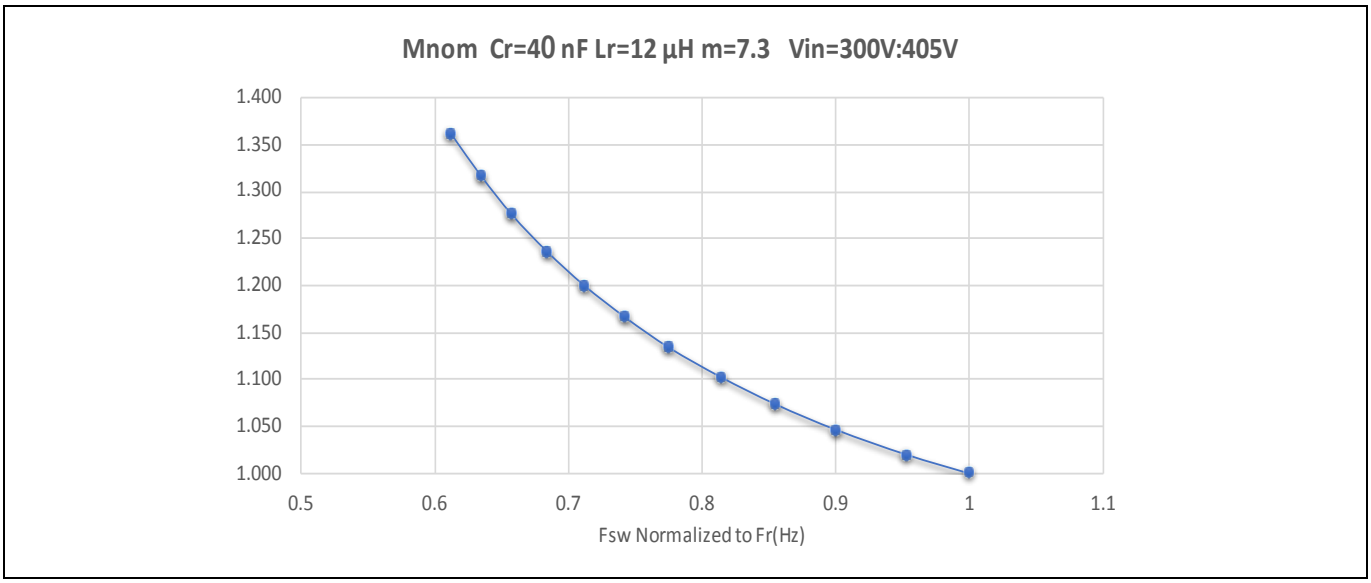

Figure 30 M_{nom} gain plotted for Cr = 40 nF as function of NFSW

An additional plot was prepared showing the actual switching frequency – in normal operation with n = 17T, FSW will be around 195 kHz to 200 kHz for nominal V_{in} = 380 V and about 140 kHz for minimum V_{in}. This is still a good sweet spot for core losses with a single-turn secondary.

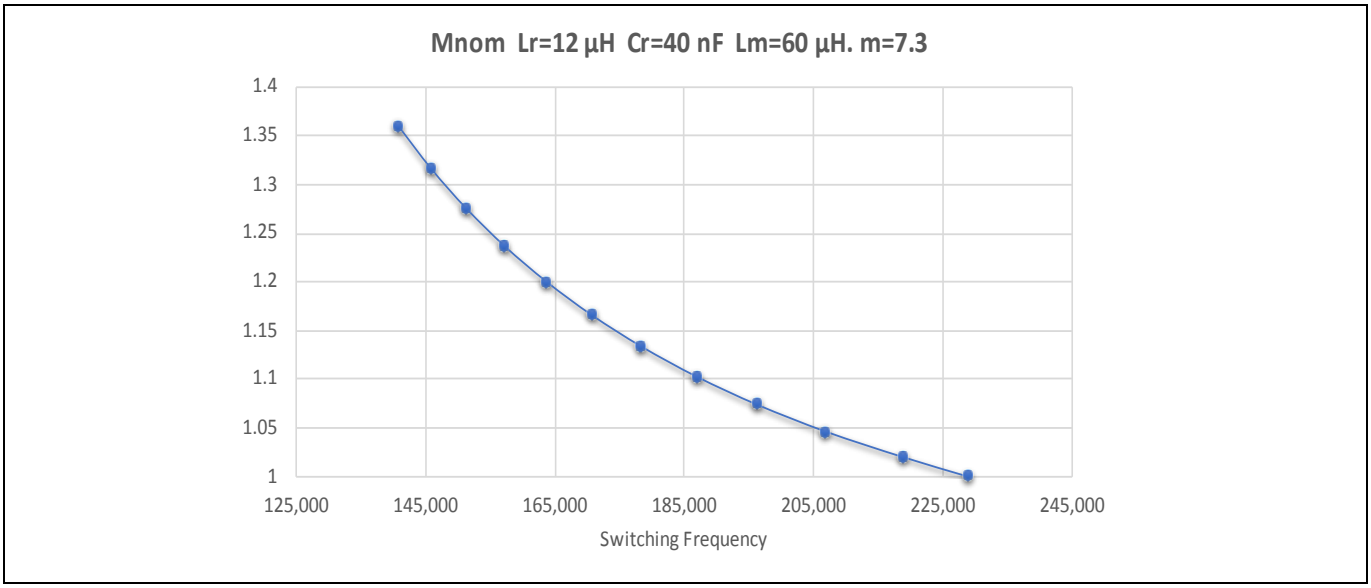

Figure 31 M_{nom} gain plotted for Cr = 40 nF as a function of actual FSW

For this tank alignment with Cr = 40 nF, full-load operating currents as a function of normalized FSW are plotted in **Figure 32**. V-Cr and I-Out are plotted against the right-side alternative Y-axis, while other values are plotted against the left-side Y-axis. Because of the relatively low value of Lm, the primary-side current is higher for I-lr and peak I-Lm at nominal input voltage.

The question naturally arises, though, is it subject to further optimization compared with these results? The low m-ratio naturaly increases peak I-Lm and total I-Lr, but in this case, it's evident that the tank Q is on the low side at 0.33 (from **Figure 29**) and so it seems reasonable (based on the previous optimization experiments for the 155 kHz design) to try a design for which the Q at 50 A output will be around 0.4 to 0.5, and then determine if it can meet the low-line regulation requirements while delivering higher light-load efficiency.

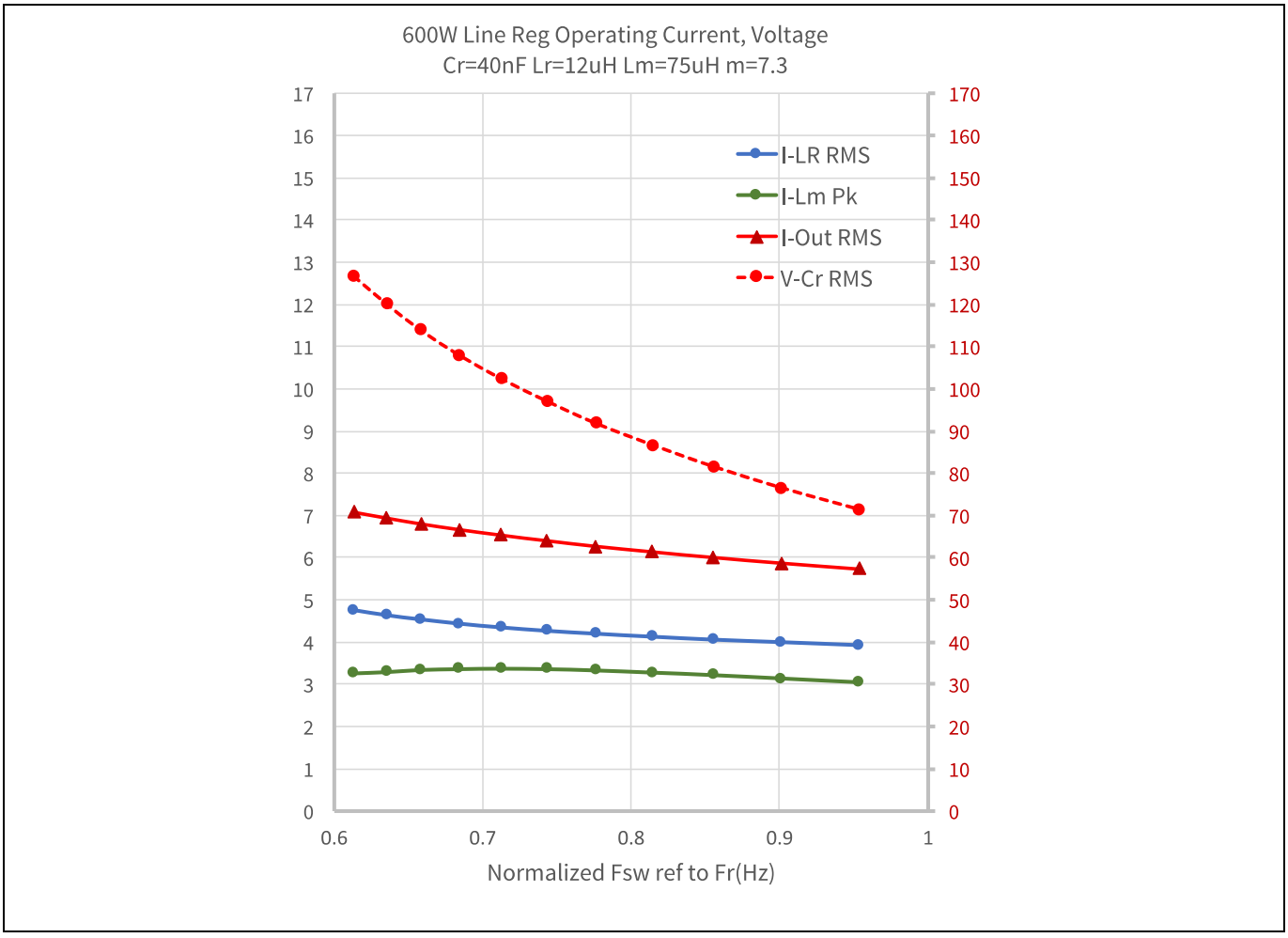

Figure 32 40 nF design operating currents and voltage as a function of NFSW at FL

3.3.2 Design using the LLC calculator with ROT modification of Q/load current

Another pass was made using the LLC calculator, but this time reducing the specified full-load current, as shown in **Figure 28**, so that at full load we will have an effective Q in the range of 0.4 to 0.5.

- Nominal input voltage is again set to 405 V – this sets the desired range for operating at the tank resonance Fr(Hz), and any input capability above that is handled in buck mode. This also sets the requirement for turns ratio, at essentially n = 17T.
- Minimum input voltage is set to 300 V, output current was reduced to 40 A. This is a way to "game" the calculator so that it results in a higher Q at the actual target load current. Other parameters for resonant operating frequency Fr(Hz) were kept the same.
- The maximum M_{max} boost gain required is ~1.35; the variable minimum frequency is adjusted for Cr to fall on an available commercial value (2 × 15 nF in this case), resulting in a slightly modified m-ratio of 7.7, and a tank Q of 0.33 at the reduced load current.
- Tank values calculated are 30 nF for Cr, Lr is taken as 16 µH, and Lm as 100 µH, dropping the m-ratio just slightly. The calculated F_{min} is just under 0.5, at 0.498. These are FHA parameters, not real word parameters (apart from m-ratio).

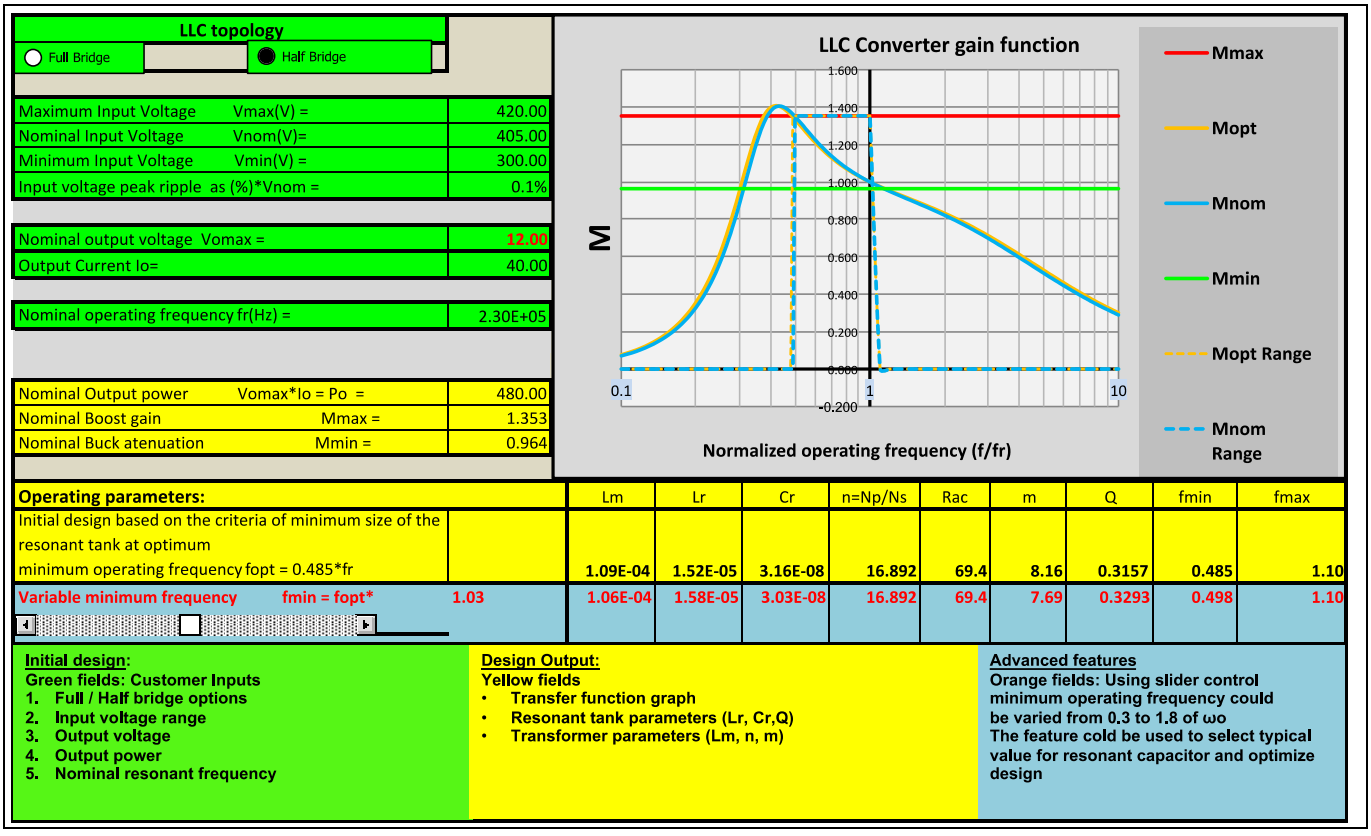

Figure 33 LLC calculator using ROT to modify Q, with Fr(Hz) = 230 kHz, Cr = 30 nF

For this tank design with Cr = 30 nF, operating point gain for a range of normalized FSW was evaluated at the actual full-load value, and plotted in **Figure 34**. This shows a maximum gain of 1.4 just at the capacitive mode boundary in the MatLAB program for 300 V input and meeting the regulation requirement for 600 W just above the normalized FSW of 0.6 and gain of 1.35, with somewhat over a 50 percent power margin. This would be considered an "aggressive" design for V_{in} = 300 V, but conservative for 330 V. **Figure 35** shows the RMS operating currents, for which peak I-Lm is significantly reduced compared with the 40 nF alignment. This improves light-load efficiency and reduces I-Lr RMS current across the board, so primary-side efficiency is clearly improved.

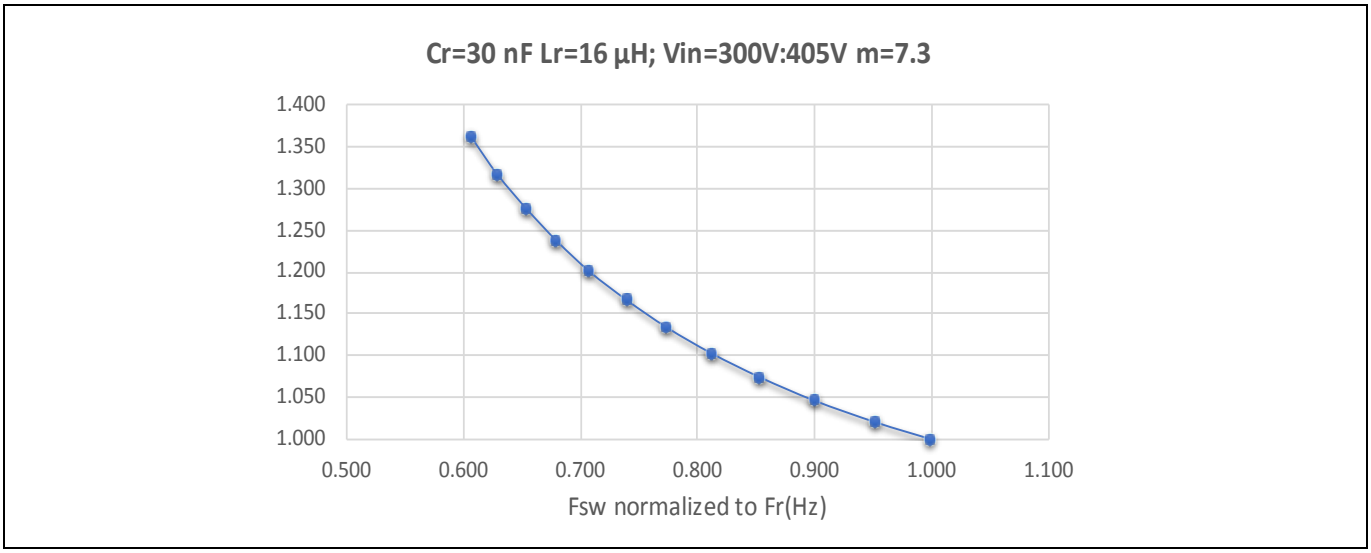

Figure 34 M_{nom} gain plotted for Cr = 30 nF as a function of NFSW

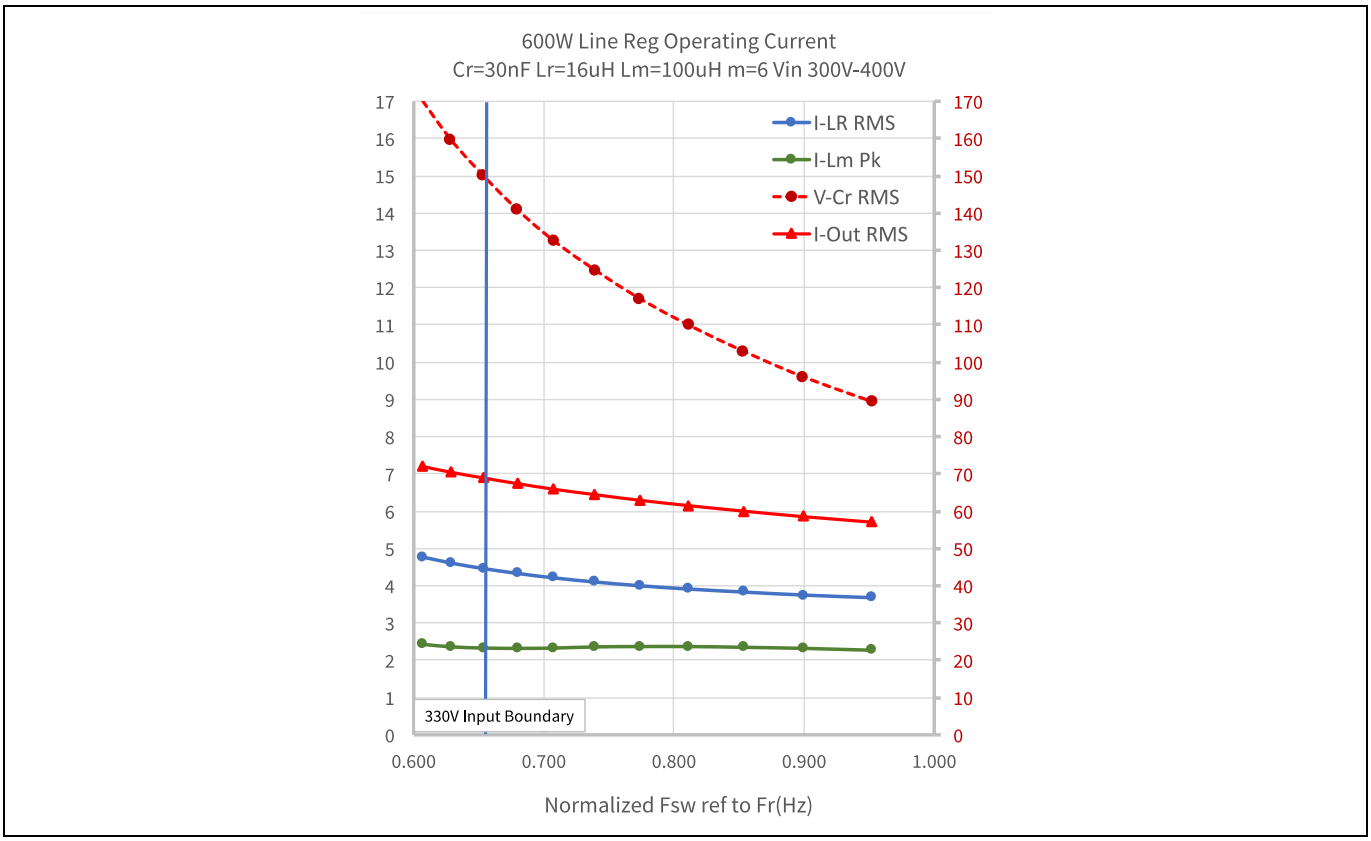

Figure 35 30 nF design operating currents and voltage as a function of NFSW at FL

3.3.3 Power margin anaylsis at V_{in} = 300 V, 330 V

For an input range of 300 V to 405 V in DCM mode, the 30 nF alignment would be considered “aggressive” because of only having a 50 percent power margin, and also having the peak boost-up point lying close to the capacitive mode boundary (**Figure 36**). However, what if the minimum V_{in} is raised from 300 V to 330 V? This would still result in a relatively wide DCM mode input range: 75 V, about double that of many published server class designs in DCM. This corresponds to the example in Table 6 for nominal V_{in} = 395 V, and minimum = 330 V.

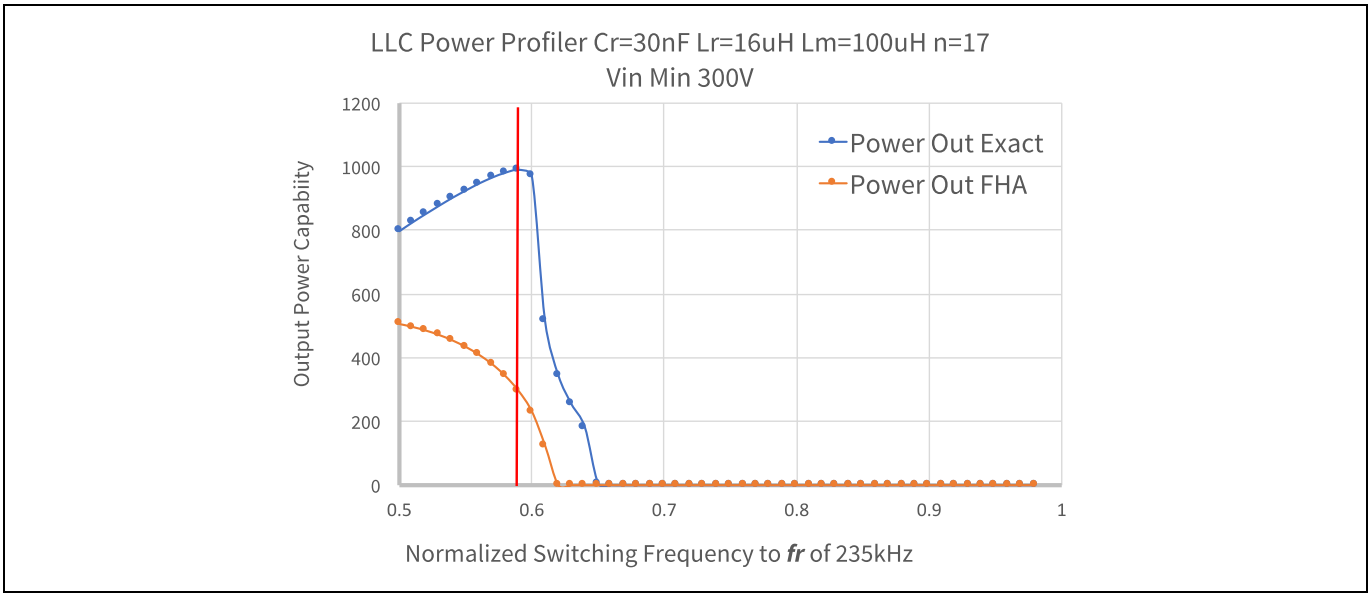

Figure 36 Power margin analysis for V_{in_Min} = 300 V for Cr = 30 nF

The power margin analysis for Cr = 30 nF, Lr = 16 µH, and Lm = 106 µH with V_{in} = 330 V is shown in **Figure 37**. Now we see an operating normalized F_{min} of about 0.68, translating to about 155 kHz, and a reasonable margin from the capacitive mode boundary with a power margin slightly over 100 percent. As one would expect, the calculated FHA capability is just hitting 600 W at a normalized FSW of 0.5, corresponding to 115 kHz. This is a good example of why FHA calcluations should not be relied on for selecting controller programming parameters for minimum operating frequency.

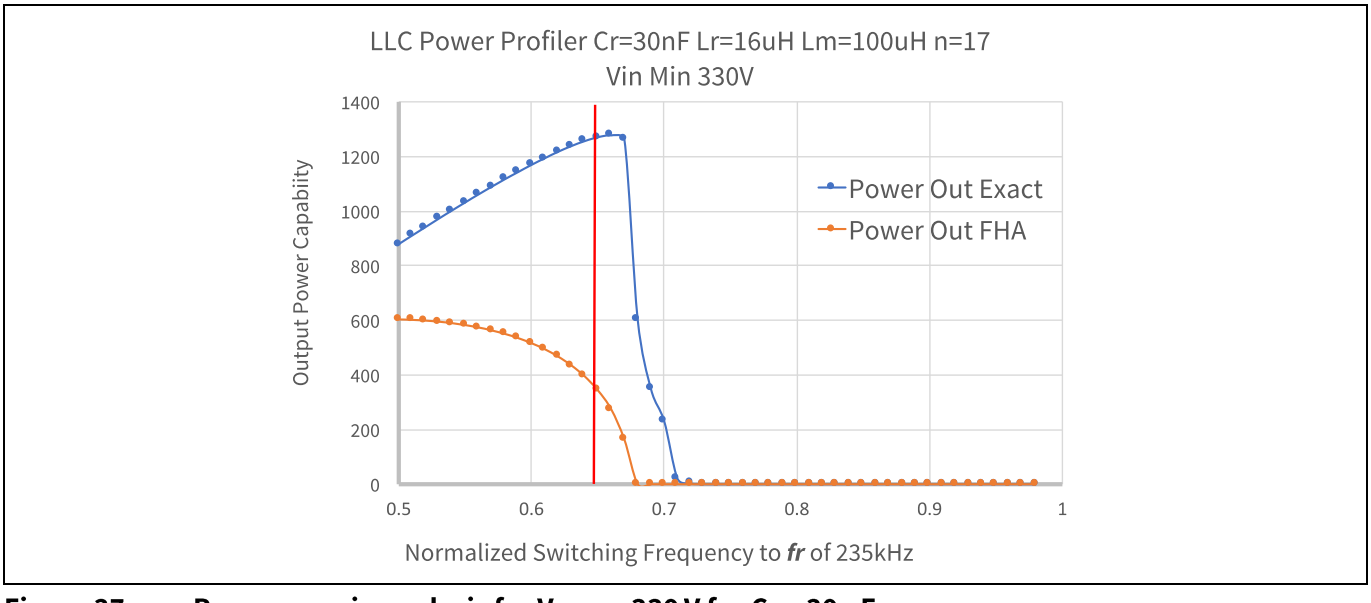

Figure 37 Power margin analysis for V_{in_Min} = 330 V for Cr = 30 nF

3.3.4 Comparison of gain and F_{min} for wide input range tank designs

Table 7 below was prepared with data to summarize this comparison of wide input range alignments and the correlation of the LLC calculator gain plots with exact mode analysis. Two alignments were developed using the LLC calculator, one directly, resulting in Cr = 40 nF, and one with a ROT modification to game the system Q at the intended full load of 50 A, and resulting in Cr = 30 nF.

To summarize:

- The LLC calculator may be described as being able to develop a similar peak gain curve for regulation purposes, but with a lower calculated F_{min} frequency than reality.
- The LLC calculator and other FHA techniques can underestimate the achievable output power at low-line by 2:1 or more.
- FHA calculation completely misses the difference in output current RMS factor because it models as a variable frequency sine wave, instead of a fixed frequency haversine wave driven by a charge pump dependent on both the charging current from I-Lm and the available DCM charging time.
- Optimization of the Cr value can consistently achieve 30 percent lower I-Lm and better light-load efficiency without compromise of other parameters (unless high I-Lm is needed for resonant switching, due to high Q_{oss} in the semiconductor switches).
- An additional LLC calculator curve was prepared at full load for the 30 nF case using the LLC calculator and plotted, resulting in a best-case gain of only 1.18 at a normalized F_{min} of 0.5, shown in **Figure 38** below. This also illustrates an example where FHA does not work accurately enough.
- This combination of gain curve plots for the alignments and test conditions in **Table 7** is shown in **Figure 38**.
- Finally, in **Figure 34**, the M_{nom} plot for a load of 40 A for the Cr = 30 nF alignment is shown in light blue, along with a -50 percent fixed-load plot (which is very close below F_{min} to matching the exact mode plot) and a +25 percent load (50 A) plot, where as expected FHA predicts failure in meeting the regulation requirements.
- Wide input range is the more challenging case, but then, it may be necessary if other design goals (such as desire to eliminate burst mode and capacitive mode operation) are prioritized.

Table 7 Wide input range LLC configuration evaluation for DCM range from 300 V to 405 V

Configuration	Cr value	Lr value	Lm value	m-ratio	Test load	Q at FL	Effective R_{acc}	Max. gain	Norm. F_{min}
LLC calculator 40 nF FL	40 nF	12 µH	80 µH	7.6	50 A	0.48	55.9	1.412	0.482
LLC calculator 30 nF ROT	30 nF	16 µH	106 µH	7.6	38 A	0.31	73.6	1.4	0.482
LLC calculator 30 nF FL	30 nF	16 µH	106 µH	7.6	50 A	0.59	55.9	1.18	0.5
Exact analysis 30 nF FL	30 nF	16 µH	100 µH	7.3	50 A	**0.59**	**55.9**	**1.41**	**0.6**

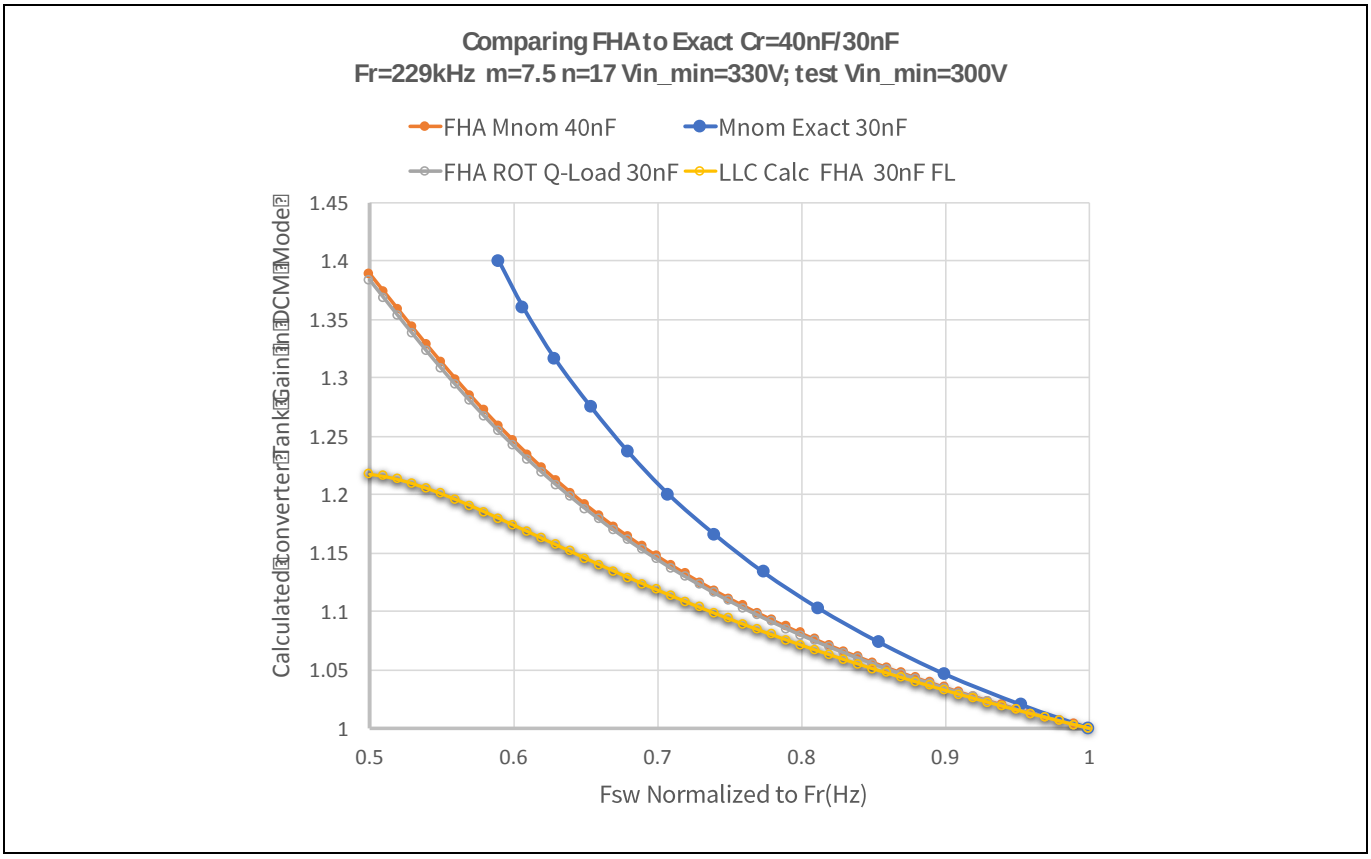

Figure 38 M_{nom} gain comparison of LLC calculator and exact mode analysis

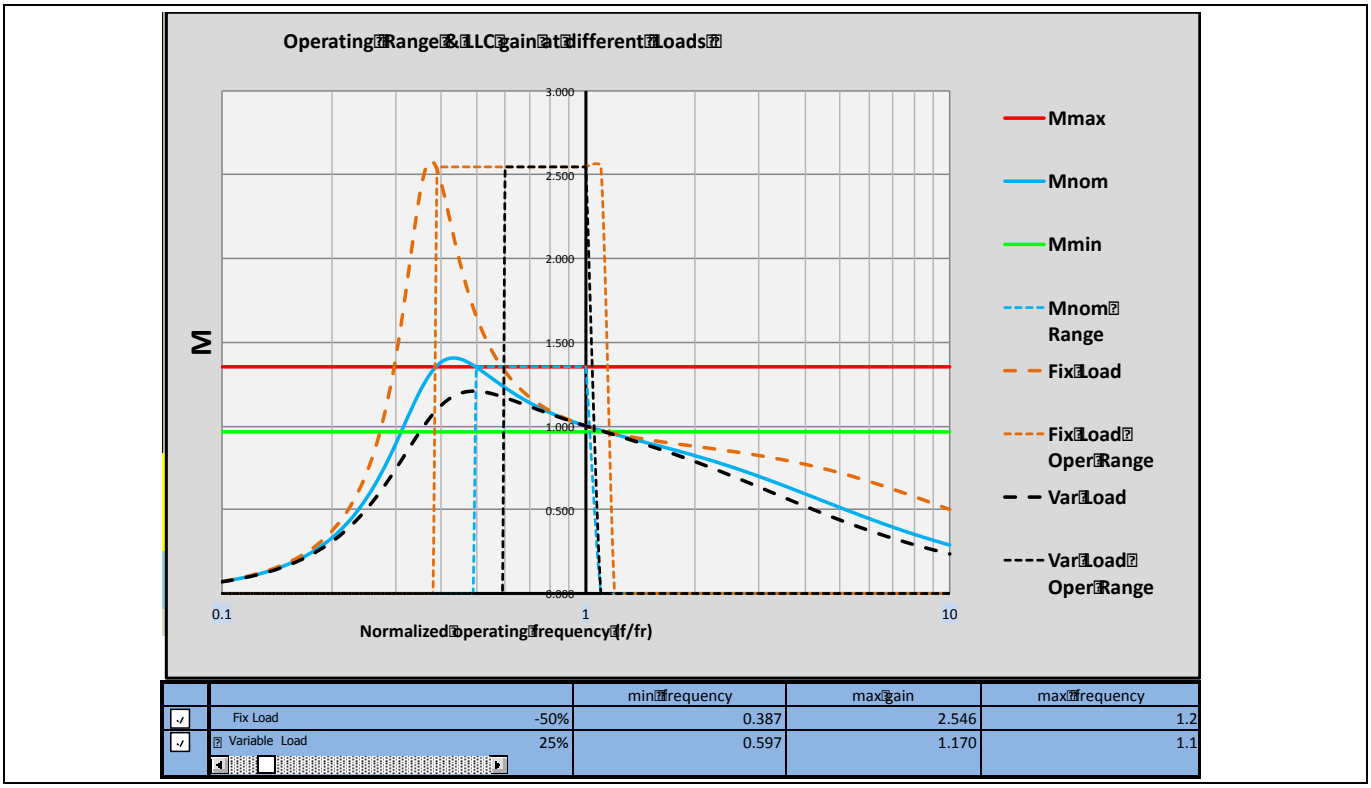

Figure 39 Matching exact gain arbitrarily with further Q modification (20 A load)

3.3.5 Comparison of power margin, RMS current and V-Cr for the examined alignments

To push into the “aggressive” category, an alignment was prepared with Cr = 27 nF, and either an m-ratio of 7.6 or 6.6. It does produce the lowest light-load (20 percent) I-Lr RMS current value (1.60 A) due to the lowest peak I-Lm (2.06 A), if coupled with an m-ratio of 7.5. For full-load nominal line input, the tank for Cr = 30 nF edges out the other three configurations, and is very close for the peak I-Lm value, as is the I-Lr. Reduction of Cr below 30 nF for this wide input range design seems to be of questionable value.

Table 8 Comparison of FSW, power margin, I-Lr current and V-Cr voltage

Cr	Q	m-ratio	FSW 300 V	PM 300 V	FSW 330 V	PM 330 V	Peak I-Lm 395 V	I-Lr 395 V	V-Cr 330 VRMS	I-LR 20 percent
27 nF	0.46	6.6	0.63	50 percent	0.70	50 percent	2.31	3.72	151 VRMS	1.76 RMS
27 nF	0.46	7.5	0.60	47 percent	0.67	46 percent	**2.06**	3.73	156 VRMS	**1.60 RMS**
30 nF	0.41	7.5	0.59	100 percent	0.67	100 percent	**2.16**	**3.68**	144 VRMS	**1.67 RMS**
40 nF	0.33	7.5	0.6	100 percent	0.67	160 percent	2.91	3.89	**109 VRMS**	2.0 RMS

3.4 Summary: takeways for alignment design guides for ROT and operating characteristics, and some potential component limitations

A number of key points should be kept in mind from these exact mode investigations, particularly the wide input range example. Their application supports using the LLC calculator as a convenient design input, definition (especially for transformer turns ratio) and visualization tool, as long as the behavioral differences are understood and the variation in equivalances are noted between the FHA approximation and the exact mode analysis. These differences can be identified and actual capabilities understood by means of the LTspice simulation for power and frequency verification, as presented in section 5 of this application note.

- Selecting the V_{nom} input voltage is a critical design point, as it will specify the input voltage, which when based on the transformer turns ratio will run right at the resonant frequency Fr(Hz).
- A second key factor for AC-powered off-line supplies is the PFC ripple factor (which is just the low-frequency rectified line voltage on the bulk input capacitor) – ripple voltage will be present even for lower-power designs that do not use PFC. This percentage determines how much the LLC calculator buffers the input voltage specifications in order to account for this variation even at nominal input voltage. At heavy load, this ripple voltage may be +/- 2 percent to 5 percent, depending on the value of the actual HV bulk capacitor. It will be taken into account in calculations for the transformer turns ratio using the LLC calculator tool.
- The higest-efficiency operating point for LLC will occur for designs operating as close to Fr(Hz) as is feasible, with minimal frequency shift – this is the operating point with the minimum degradation of output RMS current factor, where the average current is about 0.637 of the peak of the sine wave value, and the RMS (heating) factor is 11 percent over the average current.
- Operating below resonance incurs some additional losses from the change in the RMS factor, as the current is not a variable-frequency sine wave, as modeled in FHA, but is a DCM mode set of haversine pulses with varying dead-time. The RMS factor over average current varies from 11 percent higher at resonance to 57 percent higher at normalized FSW of 0.5.
- Frequency shift above Fr(Hz) will result in buck mode operation, increasing switching losses, and possibly inducing further losses due to diode Q_{rr} behavior in the synchronous rectifiers. The higher the switching frequency, the more pronounced the impact of these losses.
- Opeating above Fr(Hz) may present significant issues in light- or no-load conditions, as with large m-ratios, often used to minimize the peak I-Lm, the amount of attenuation is quite low at light load, and may necessistate burst mode operation to reduce output. Burst mode can trigger intermittent operation in capacitive mode, even if a balanced half-bridge configuration is used for the resonant capacitor Cr. Digital start-up techniques can mitigate this. [9]
- Using a design approach based on understanding of exact mode behavior may enable reduction of the size of Cr by 30 to 40 percent, which in turn increases the size of Lr and Lm, and allows using a lower m-ratio for the same light-load RMS currents.
- Selection of m-ratio should be based on setting the minimum normalized FSW to a range that will result in an acceptable RMS factor for current at V_{in_min}. If low RMS factor for low-line is desired, in practice this means using an m-ratio to achieve a normalized FSW in the range of 0.75 to 0.8, whatever the line voltage spread actually is. For a more balanced optimization and better light-load behavior, an F_{min} target of 0.7 to 0.75 will work well, with a somewhat higher value of Lm.

4 Recommended design procedure for LLC calculator with ROT

4.1 Where the LLC calculator fits in the design process

Figure 35 gives an overview of how we see the LLC calculator fitting into the design process. The key electrical specifications are the prime inputs, conveyed with only minor modification based on ROT as inputs, considering the necessary modification by topics such as practical selection of Cr, desired over-load margin, the V_{in} range considering line frequency ripple, the planned regulation span, considering both input voltage and operating frequency, and adjustment of Q_{max}.

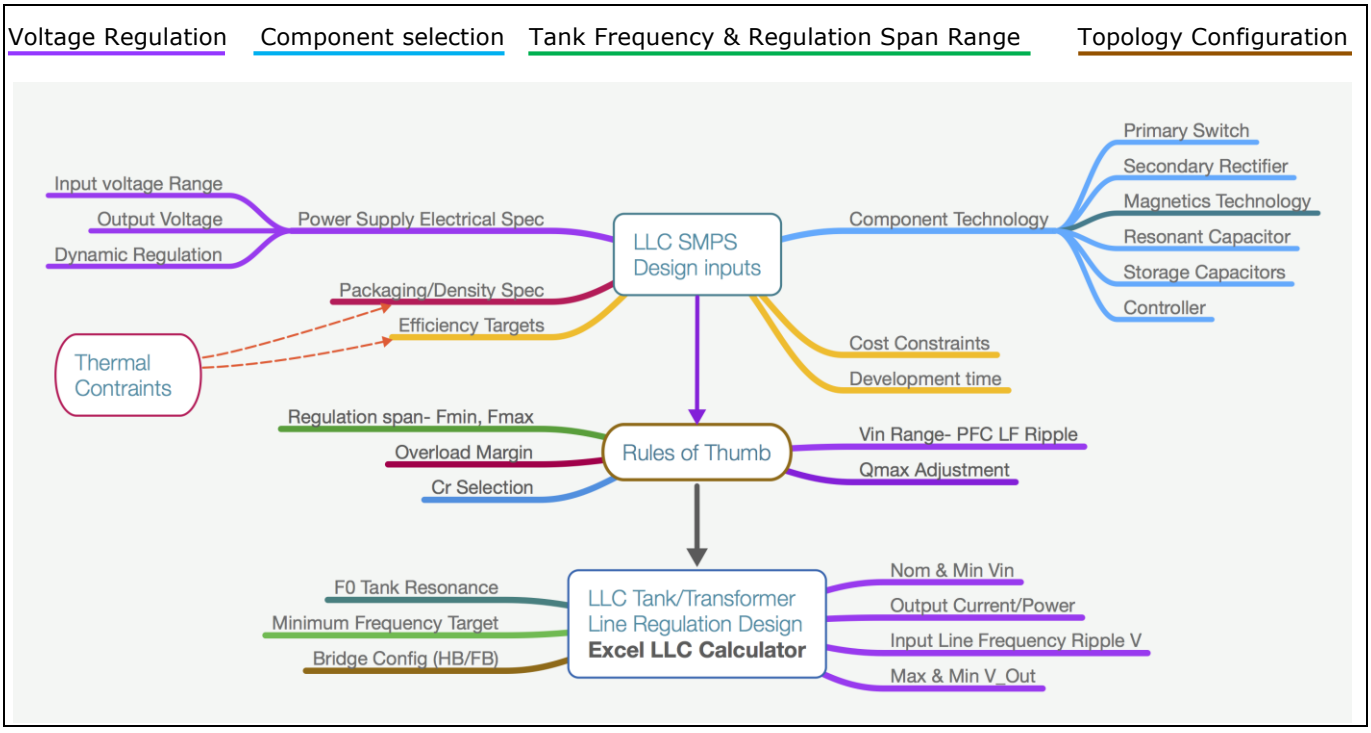

Figure 40 Mind map showing the role of the LLC calculator in the design process

The tank resonance operating frequency is chosen in consideration of component technologies and targets for system density and the planned regulation control frequency span. As F_{max} might range from 50 percent over the resonant frequency to as much as 2.5 to 3 times the resonant frequency, these choices are clearly inter-related, including with the use of buck mode, which has its own attenuation issues at light to zero load above Fr(Hz). The need for very high multiples for F_{max} or burst mode operation can often be avoided through specific choices (described below) in the configuration of the LLC converter.

To summarize these guidelines:

- Substantial use of the buck range except for the highest of input voltage transient conditions should be avoided – in the buck range, attenuation curves for light-load or no-load conditions become quite weak, and regulation may only be achieved by methods such as burst mode, which may bring their own operational challenges, such as intermittent capacitive mode operation if conventional PWM techniques are used.
- Operation in buck mode as part of “normal” load regulation results in a much larger frequency span for “normal” operation under varied loads, as can be seen in a simulation presented in section 4.3.

- High m-ratios should also be avoided if minimizing F_{max} and achieving good buck attenuation is desired, as the attenuation curves above resonance are much weaker at light load and no load.
- A high F_{max} is also undesirable because of the issues around dead-time – with increasing frequency, less energy is available to drive resonant transitions, so they become longer, and dead-time must be frequency-adaptive or set to cover the value expected at F_{max} with the available I-Lm at that frequency. This results in wasted dead-time at resonance and below.

4.2 Complete sequence of steps and verification process

Next is a complete walk-through of using the LLC calculator with ROT to develop a design for verification with LTspice or other tools. ROT will be used to modify inputs to the LLC calculator, including the use of controls such as the F_{min} slider, for the purpose of achieving a design meeting regulation requirements and with lower RMS currents as needed in the desired operating ranges.

4.2.1 Navigation of the LLC calculator main pane

First, let's take a quick overview of the LLC calculator main pane, and review the functional areas:

- **Topology selection:** to adjust the overall gain parameters correctly, select whether a full-bridge toplogy on the primary or a half-bridge topology will be used.
- **Regulation inputs:** to input the nominal input voltage, defining the operating point for Fr(Hz) and minimum and maximum input voltage, as well as peak ripple voltage on input, plus the output voltage and output current requirements.
- **Tank Fr(Hz):** to input the target for the tank resonant frequency, around which the Cr, Lr and Lm will be calculated.
- **Nominal power and boost/buck summary:** Displays the calculated output power, the M_{max} boost gain required, and the nominal buck attenuation based on maximum V_{in} to nominal V_{in}.
- **Calculated tank parameters:** displays the calculated LLC tank, transformer ratio, equivalent primary-side resistive load at full load, the m-ratio, the tank Q at full load, and the normalized F_{min} and F_{max}.
- **Update F_{min} slider:** gives the opportunity to over-ride the F_{opt} (optimum frequency) calculation of the vector FHA algorithm by adjusting F_{min}, and displaying the impact on tank component values, the m-ratio, Q, F_{min}, and F_{max}. F_{max} changes because shifting the m-ratio will also impact the attenuation slope above Fr(Hz).

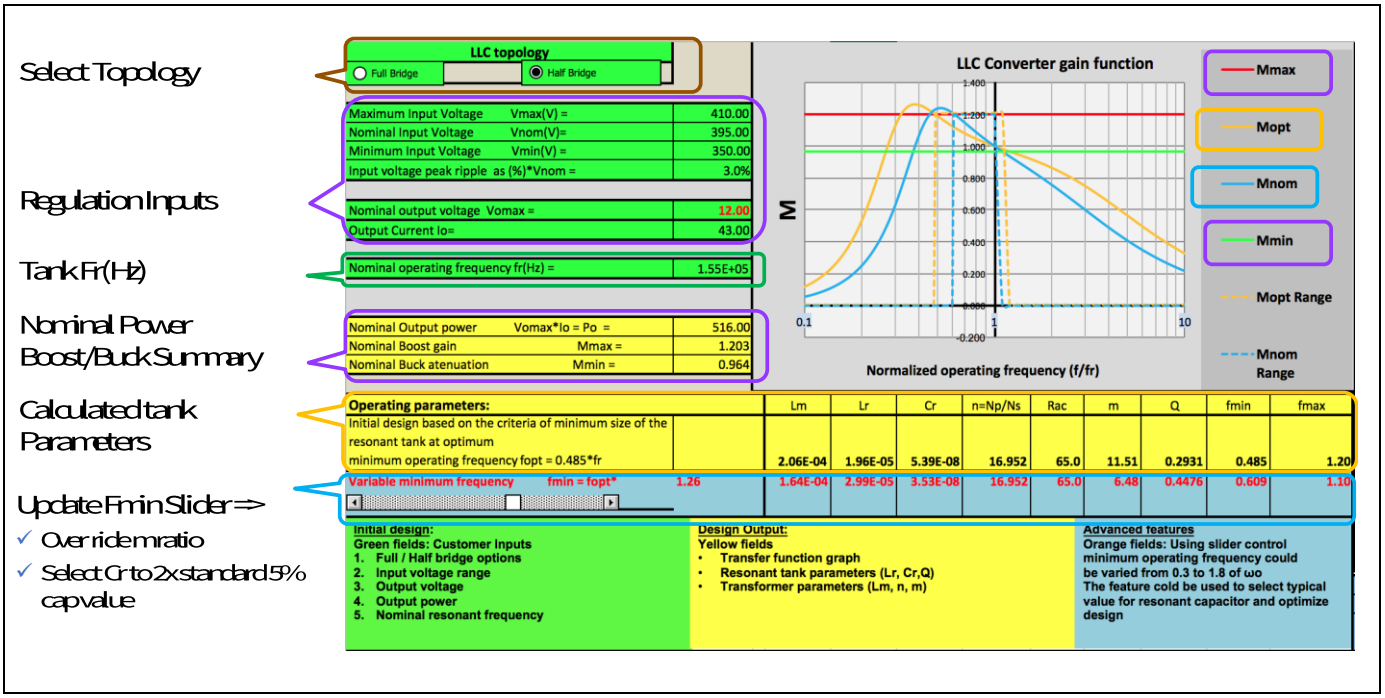

Figure 41 LLC calculator main pane layout

4.2.2 Topology and voltage inputs

The intial inputs can be accomplished fairly quickly:

- Set the topology for either full-bridge or half-bridge – for this example, a half-bridge configuration is used, similar to the Infineon 12 V 600 W server SMPS.
- Specify the $V_{o\text{-}max}$ – the maximum output voltage is one of the conditions to establish the maximum boost gain required, M_{max}.
- Next, specify the output current Io. This is where we will first apply a ROT over-ride. In this case, what is desired is to change the effective full-load Q model, which is most easily done by simply reducing the output current requirement by between 20 percent and 40 percent. The amount that puts things close to the optimum range is proportional to the eventual m-ratio used; for m-ratios in the 8 to 10 range, 35 to 40 percent maybe be useful; for m-ratios in the 6 to 7 range, the coupling from Lm changes and Q does not need to be modified as much, and a reduction of around 15 to 20 percent works well.
- Set the nominal operating frequency. This is dependent on the cost targets for semiconductors and magnetics materials – those will be discussed more in Part III. This may need to be adjusted after evaluation of the calculated normalized F_{max} – a high value may lead to reducing the switching frequency, but other measures, such as burst mode or reducing the m-ratio or the extent of the operating range in buck, should also be considered.

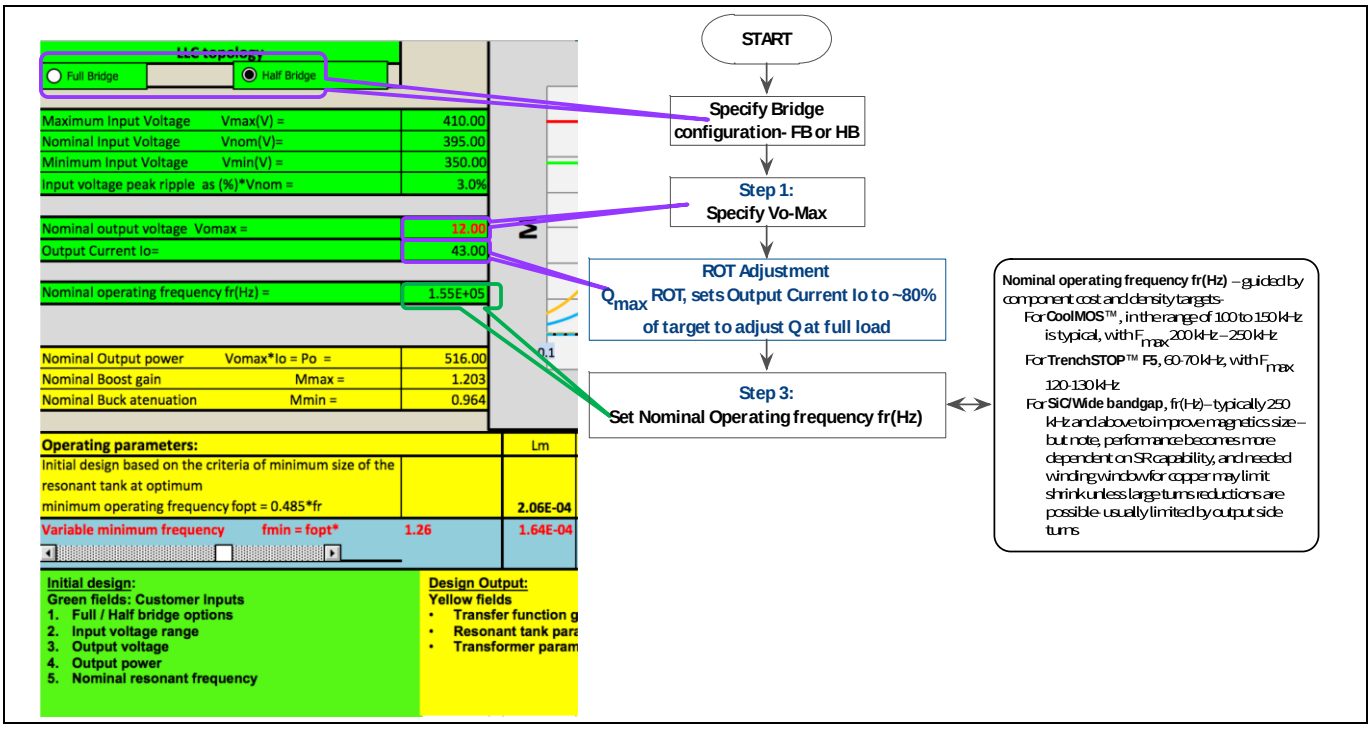

Figure 42 Initial entries for set-up

4.2.3 To buck or not to buck? This is the question…

Many LLC converters will work well with a mixture of buck and boost operation. But there are points to consider in aligning these choices with the rest of the system design. They tie in with other system design choices, including:

- the need to adjust output voltage as well as operate from a varying input voltage, which may require the flexibility of buck mode

- using synchronous rectification (SR) with higher output voltages and medium voltage silicon MOSFETs, which will incur more switching loss if used in buck mode at high frequencies, both due to hard switching and SR body diode Q_{rr} – this may dictate a design staying in DCM for most consistent results, especially at light load
- high output voltage at lower output current may permit reasonable efficiency and behavior if using WBG rectifiers while in buck mode
- the desire for very high operating frequency with high efficiency with output SR is feasible with lower output voltages in mild buck operation.

If the decision is made to avoid buck mode, then the nominal Input volage and maximum input voltage should be set to the same value.

Otherwise, set the maximum input voltage and the minimum, and set the nominal to split up the range between boost (DCM) and buck operation. The portion of the gain range for each will be displayed in the top yellow block, with both the nominal maximum boost gain, and the nominal buck attenuation. It is a good idea to check the calculated response in the load region in the secondary pane for estimating nominal F_{max} and deriving at what load percentage to switch to burst mode operation in order to achieve the necessary attenuation with maximum input voltage.

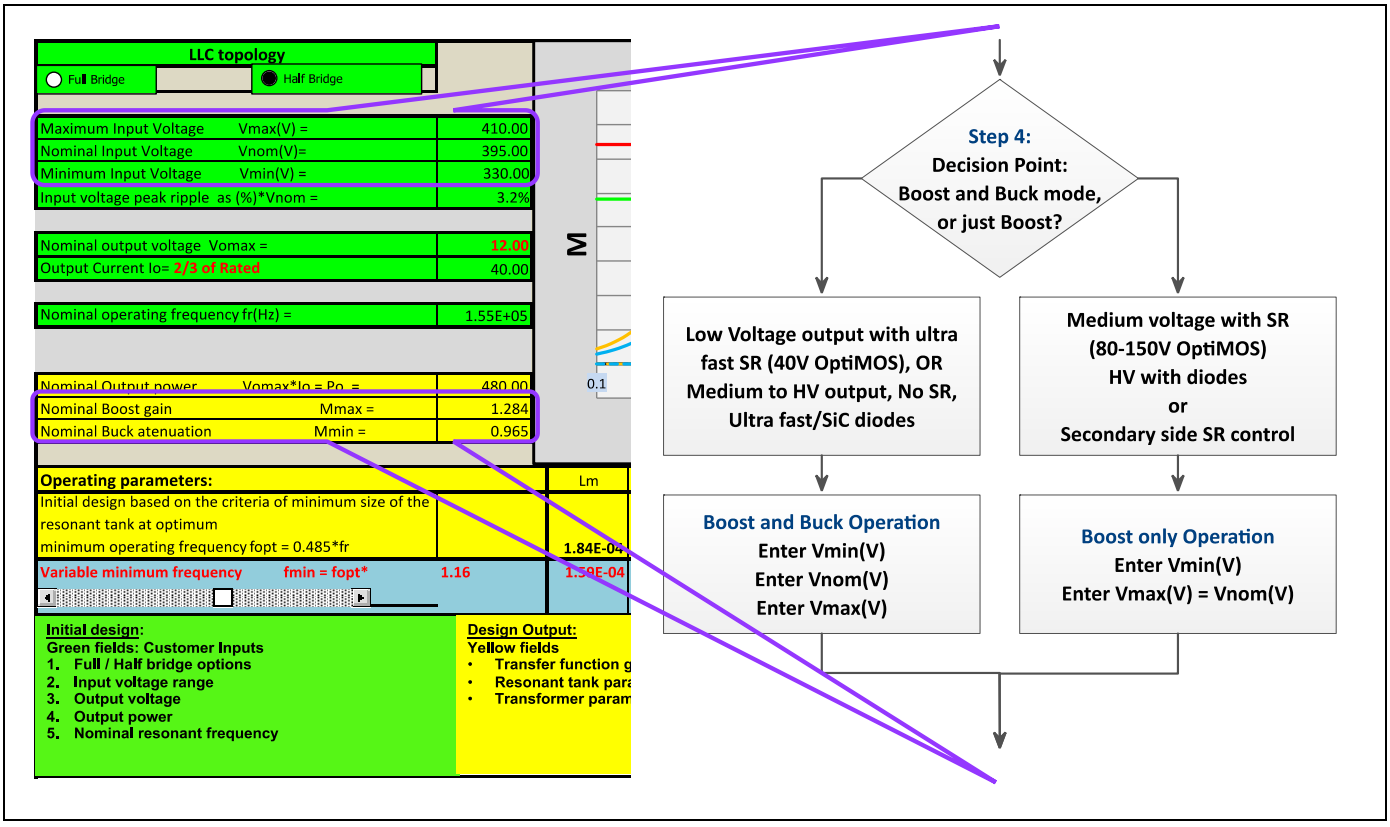

Figure 43 Choosing the V_{nom} setting to allow or exclude buck mode operation

4.2.3.1 Comparing trade-offs in two 12 V 600 W designs, one with V_{nom} chosen to optimize light load but having greater buck mode operation at nominal V_{in}

An example is presented of the impact of different optimizations with regards to turns ratio and the resulting use of buck mode vs mostly DCM mode.

Design 1: First 12 V 600 W prototype design

- Cr = 94 nF; Lr = 20 µH; Lm = 180 µH;
- n = 15; np = 30T; ns = 2T
- V_{in} = 350 V – 410 V; V_{innom} = 380 V; V_{in} at Fr(Hz) = 360 V
- Fr(Hz) = 115 kHz; F_{min} = 87 kHz; F_{max} = 200 kHz

Design 2: Final 12 V 600 W evaluation board design

- Cr = 66 nF; Lr = 16 µH; Lm = 195 µH;
- n = 16; np = 16T; ns = 1T
- V_{in} = 350 V – 410 V; V_{innom} = 380 V; V_{in} at Fr(Hz) = 385 V
- Fr(Hz) = 157 kHz; F_{min} = 90 kHz; F_{max} = 210 kHz

Efficiency plots of these design variants are shown in Figure 44. While I^2R losses in the transformer design explain some of the behavior (as secondary resistance is four times higher in Design 1, due to twice the number of turns in the same winding window), what do the operating waveforms look like? What information may be conveyed by them?

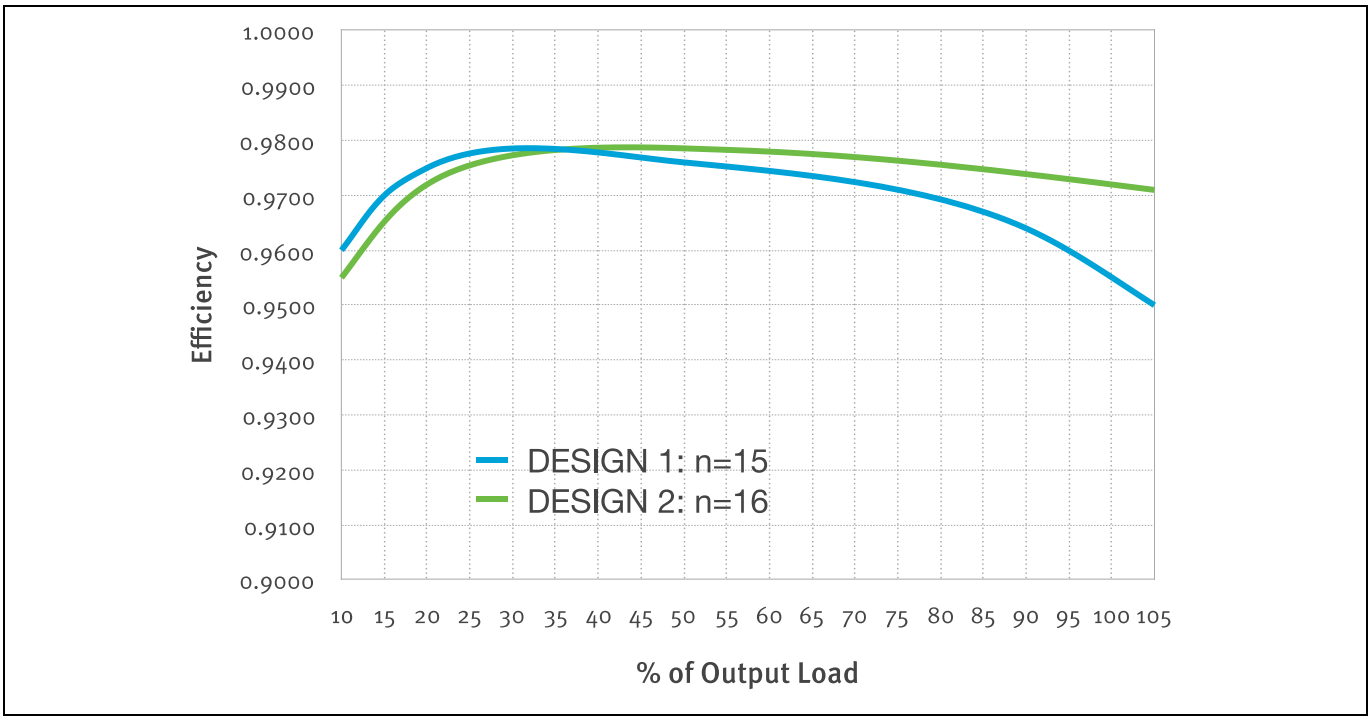

Figure 44 Comparing efficiency curves of two versions of the Infineon/Finepower 12 V 600 W LLC converter

4.2.3.2 LTspice simulation for LLC with n = 15 or n = 16

An equivalent circuit simulation was developed for LTspice including the SR concept used in both prototypes, as shown in **Figure 45**. Native LTspice VDMOS models were developed for the 60R190P6 on the primary side,

and the BSB014N04LX3 as SR rectifier on the output. A simplified equivalent model for the power transformer and output filter configuration was employed. Simulation was performed for nominal V_{in} = 380 V.

The purpose of the simulation was to compare the operating waveforms of two configurations, in particular to examine the degree of difference in hard-switching at turn-off and loss of ZCS. This simulation was run at half power, an output load of 25 A, where efficiency peaking is normally desired and expected for N = 1 redundant power supplies. The measured efficiency curves on the hardware show that there is already a drop-off in efficiency at this point for the Design 1 configuration.

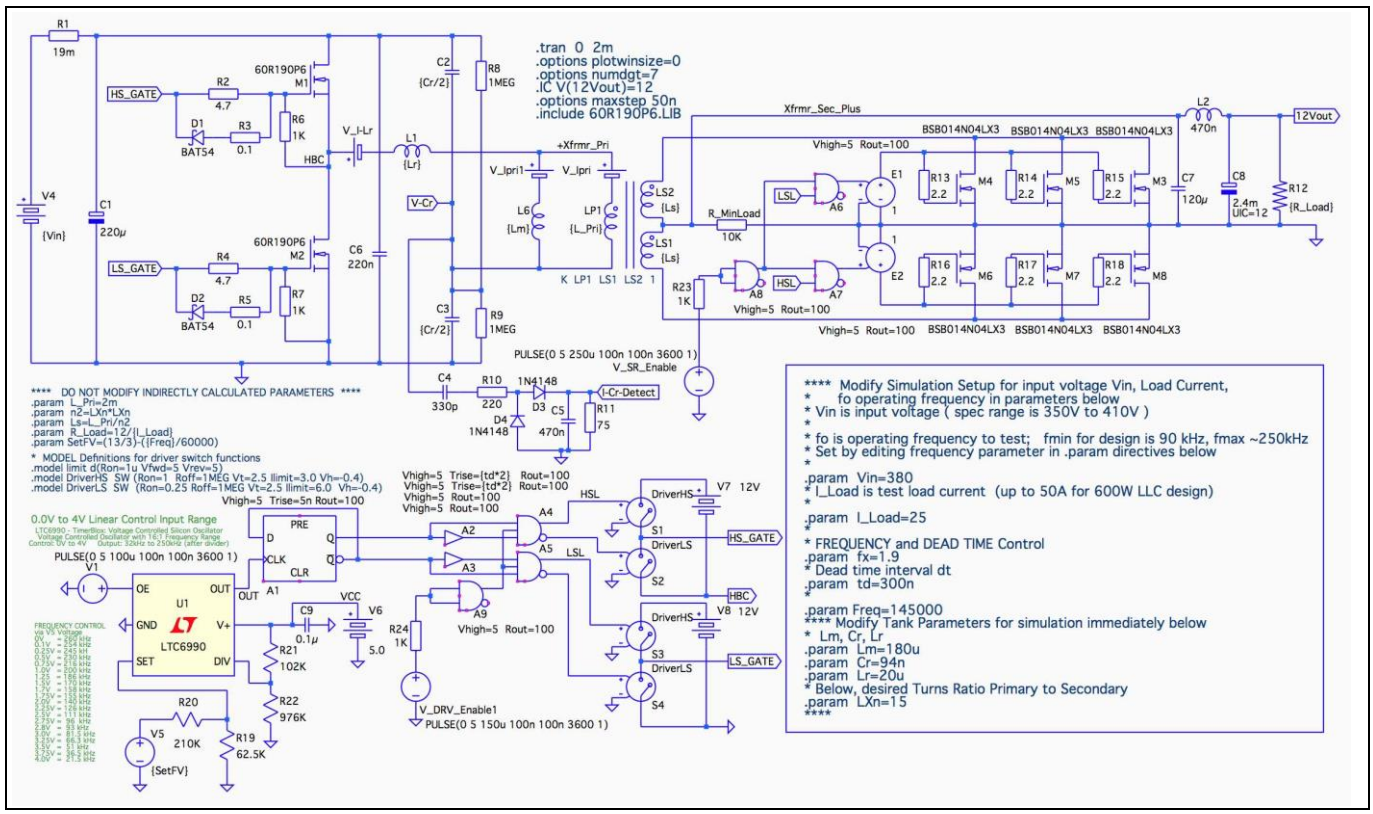

Figure 45 LTspice simulation circuit for 12 V 600 W LLC converter with SR

4.2.3.3 Simulation results for LLC with Fr(Hz) = 115 kHz, n = 15 at V_{in} = 380 V

A detail display of simulation waveforms is shown in **Figure 46**, with key traces:

- **I(L1):** the current through the resonant inductor L1
- **I(V_ipri1):** the current through the magnetizing inductance for the transformer model
- **V(hbc):** the center-point voltage of the MOSFET half-bridge
- **V(12Vout):** the output voltage at the output filter into the load
- **V(n005), V(n019):** the outputs from the secondary-side windings connected to the synchronous rectifiers

The current waveform for I(L1) shows substantial hard-switching at turn-off, as might be expected, given that the input voltage for Fr(Hz) is 360 V, and with V_{in} = 380 V, the LLC tank is switching at 145.6 kHz in order to get the buck attenuation necessary to regulate to 12 V output.

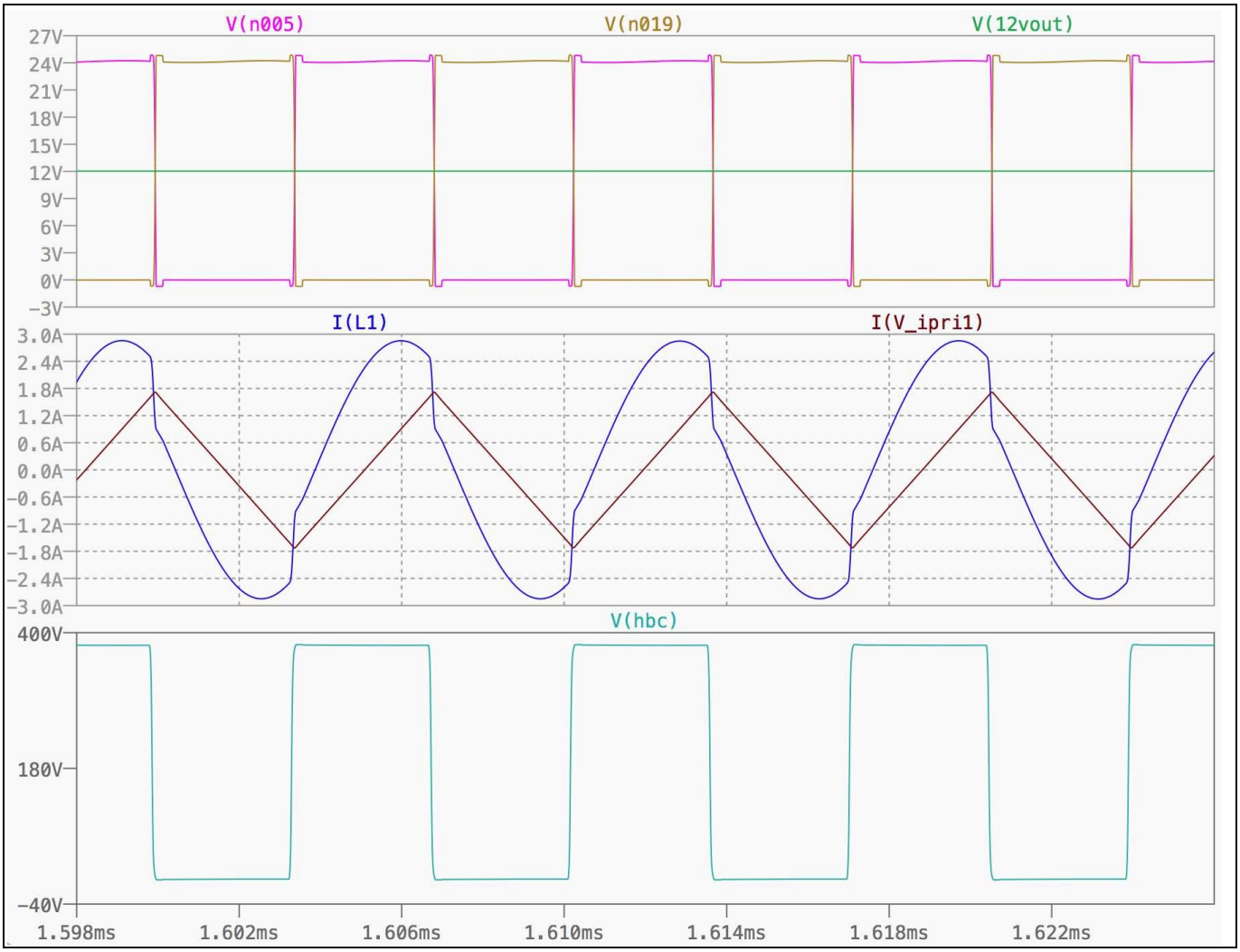

Figure 46 Showing operating waveforms for n = 15 with nominal V_{in} = 380 V

4.2.3.4 Simulation results for LLC with Fr(Hz) = 157 kHz, n = 16 at V_{in} = 380 V

The same group of traces is shown in the simulation result for the Design 2 circuit using n = 16 for the turns ratio. The converter is regulating to 12 V output, and the measured switching frequency is just under 157 kHz. Very little or no hard-switching is evident at turn-off. There is evidence of a very short DCM interval, so this is an optimum efficiency point for the converter for both switching losses and RMS current factor.

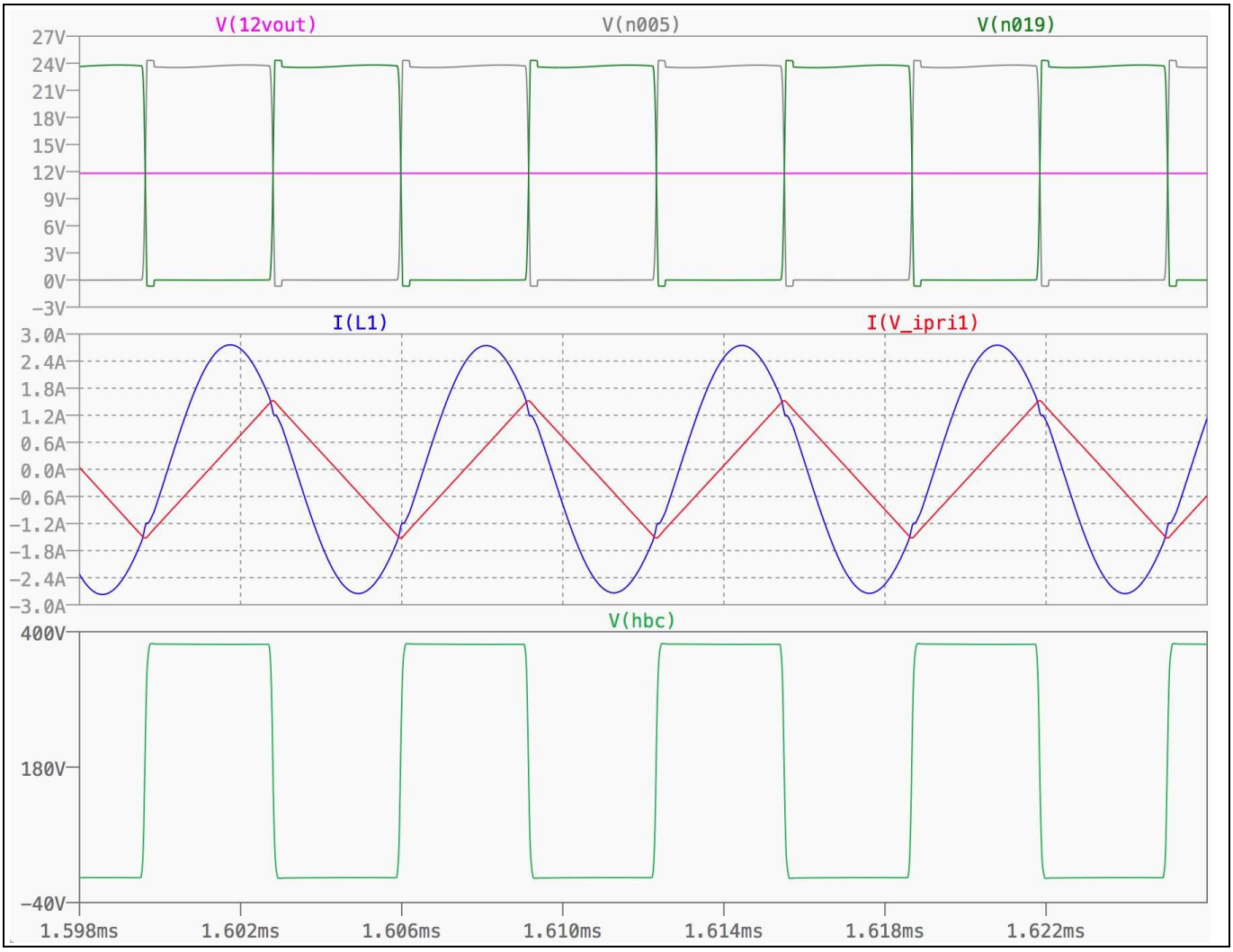

Figure 47 Showing operating waveforms for n = 16 with nominal V_{in} = 380 V

4.2.4 Setting up 12 V 600 W design for mainly boost/DCM operation at nominal Fr(Hz) for up to 395 V input by V_{in} and peak input ripple

The LLC converter can be used in many types of applications – both embedded and in AC off-line power supplies. In the latter case, a consideration to take into account is the two times line frequency ripple current which appears on the output of an active PFC front end. This will entail some variation in the DC input to the LLC converter, which is not present when testing an evaluation board with a laboratory power supply. This ripple will vary depending on the output loading of the complete power system – it's not unusual for it to be at a level of +/- 3 to 5 percent under heavy loading, and this should be taken into account when planning the input working voltage range. Furthermore, as an active PFC regulator will regulate the average output voltage, and typically with a loop cross-over frequency no higher than 10 Hz, the actual ripple voltage can be going both above and below the nominal regulation point.

To aid in dealing with this, an optional input peak ripple voltage may be entered in the data entry block at the top, and this will be factored into the nominal input voltage and minimum input voltage, and this will adjust the recommended transformer turns ratio appropriately.

A special challenge is presented in high-current LV outputs. In this case, it may be desirable to use single-turn outputs, which limits the increments of gain available from the transformer. For example, with this converter

requirement for 12 V output and 380 V input, one obvious possiblty is to use a two-turn secondary, and then the step-down ratios that are possible would include 15.5 to 1, 16 to 1, 16.5 to 1, and 17 to 1. However, a two-turn secondary doubles the number of turns on the secondary and the primary, which, for the same transformer winding window, quadruples the resistance. For efficiency reasons, this may be unacceptable.

A better optimization may result when using PFC by setting the transformer turns as necessary to adjust for covering the desired input voltage to an integer value, and adjusting the regulation of the input voltage to a slightly different value. This is why this example uses V_{innom} = 395 V, and ripple 3.2 percent.

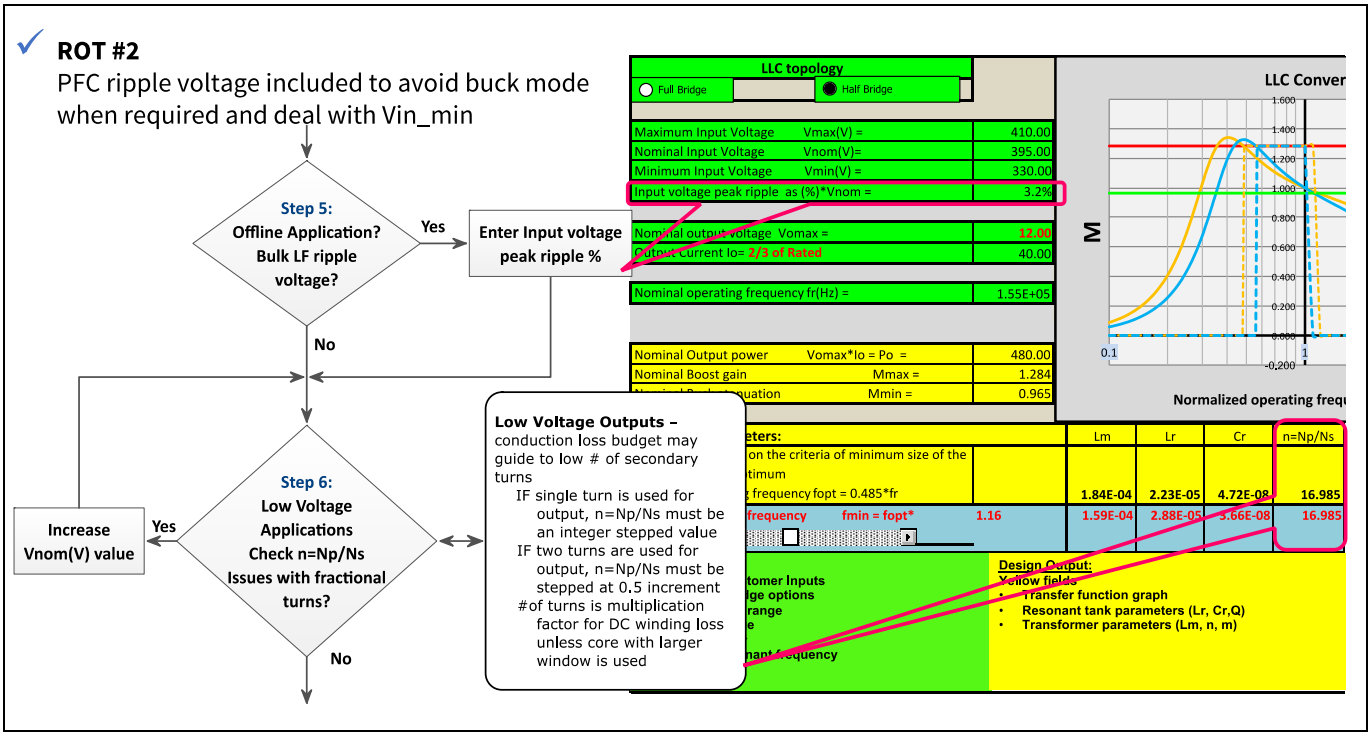

Figure 48 Setting turns ratio and V_{in} ripple percentage

4.2.5 ROT over-ride – m-ratio adjustment

At this point the data entry is complete, and the results in the **Operating Parameters** block should be reviewed in preparation for adjustment of the variable minimum frequency.

At this point the default design looks like this:

- Cr = 47 nF
- Lr = 22.3 µH
- Lm = 184 µH
- N = 17; m = 9.25
- F_{min} = 0.485 for 330 V input

From the RMS factor analysis in section 4.2 and the graph of Figure 40, we know that the RMS factor would be quite high (~57 percent) for a boost gain of 1.3 with F_{min} at or below 0.5. This suggests the need to reduce the m-ratio from 9.25 (which is a reasonable value for a converter with a working input range of 35 V to 40 V in DCM) to something in the range of 6 to 7 for this wide input range design. This is done with the variable minimum frequency slider, with one eye on the m-ratio, and a second on the resulting value of Cr. Once you are close to the desired m-ratio, then the final value should be selected by adjusting so that the value of Cr falls on commercially available component values. In general, the recommendation is to use two capacitors for Cr,

preferably in a half-bridge configuration, so the resulting Cr value in the LLC calculator should be equivalent to two standard values in parallel. For example, two 18 nF capacitors combine to a net value of 36 nF.

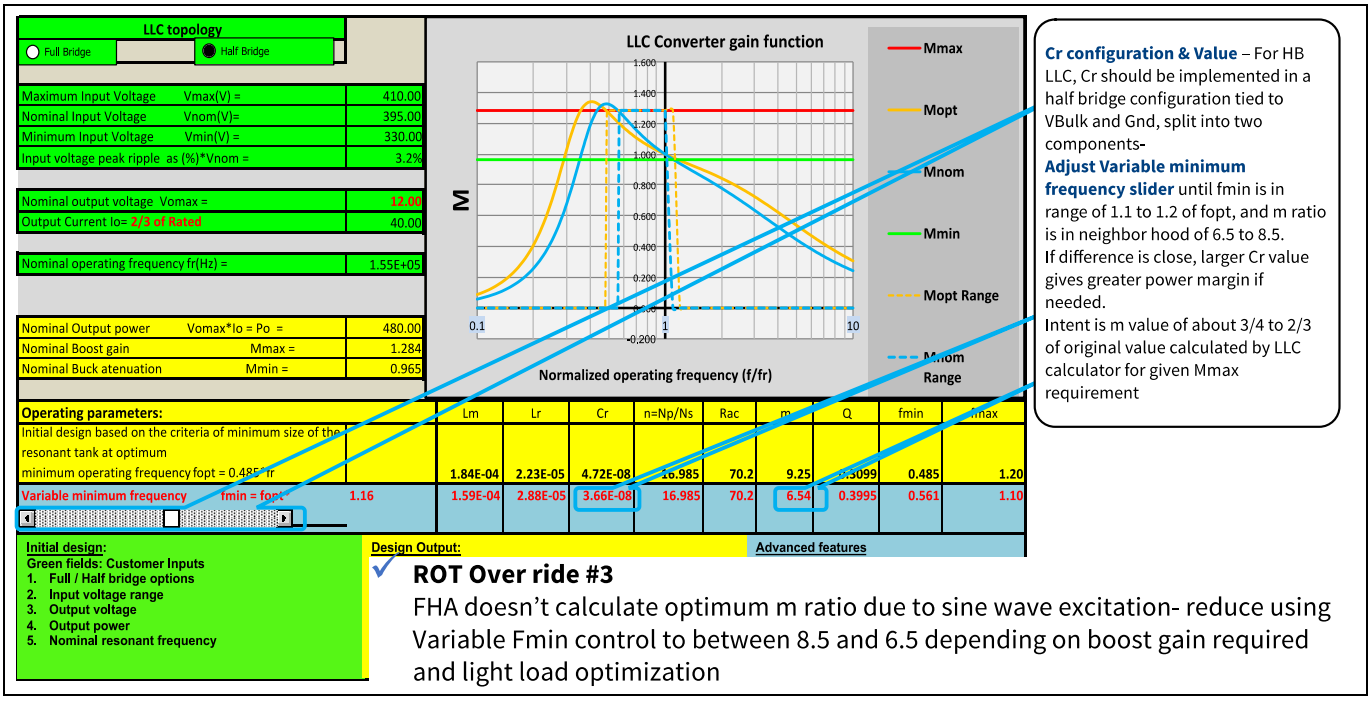

Figure 49 Final m-ratio adjustment and fit to available Cr capacitor values

4.2.6 Check calculated operating and control frequency span

From the LLC calculator tool the calculated F_{min} value can be read out, at 0.561. Due to the low m-ratio and the very small range in buck (from 395 V to 410 V), F_{max} is predicted at full load as 1.1 times the Fr(Hz).

From analysis of earlier examples, we have seen that the FHA calculated F_{min} for power regulation at low-line tends to be as much as 20 percent lower than exact analysis or simulation predicts. From the viewpoint of the ultimate RMS current factor and efficiency at low-line, this is a "good thing"; for programming a controller, more exact information is preferred.

Figure 50 shows a power margin analysis for this configuration described above calculated in MatLAB – here, the predicted operating point for F_{min} is a normalized switching frequency of 0.7, instead of the FHA value of 0.561. Numerically this translates to an actual minimum switching frequency of about 110 kHz.

This indicates a result for the RMS current factor of about 1.33, instead of about 1.47 if the F_{min} actually was 0.56. Before going to design, this and other parameters should be verified. The next section will discuss how to do this without the MatLAB-based software, using a specific simulation approach in LTspice which minimizes the simulation time and focuses just on the LLC tank behavior with a no-cost tool approach.

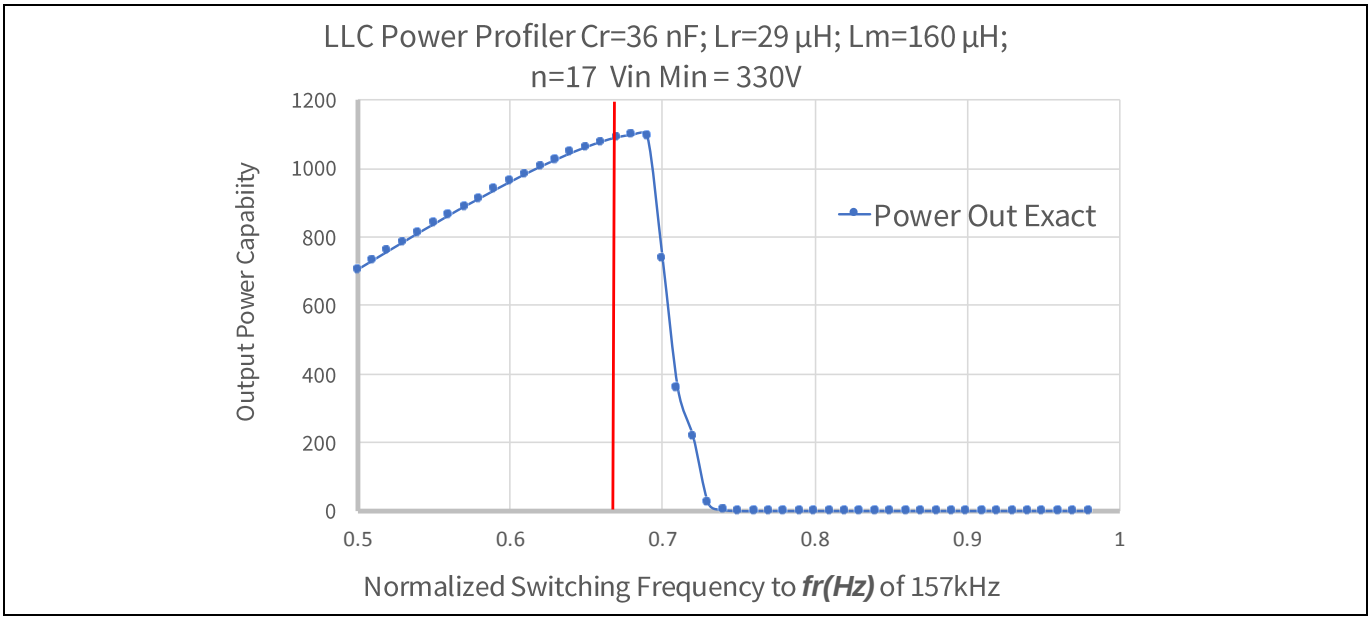

Figure 50 Power margin analysis for V_{in_min} = 330 V for Cr = 30 nF

4.2.7 Collect parameters for design verification

The final step in the process with the LLC calculator is to collect all of the parameters needed to use in the parameterized LTspice simulation, which will be discussed in the next section. These are found in the original input parameters and the blue row with the variable minimum frequency slider, but as described in Figure 51, one parameter, the R_{ac} effective primary-side reflected resistance, must be modified by the degree to which the output load current was modified in order to generate an alignment with the desired higher Q at full load. This is done by multiplying R_{ac} by the actual Io current value used divided by the target full-load current; in this case,

$R_{ac} = (40/50) \times 70.2 = 56.1$

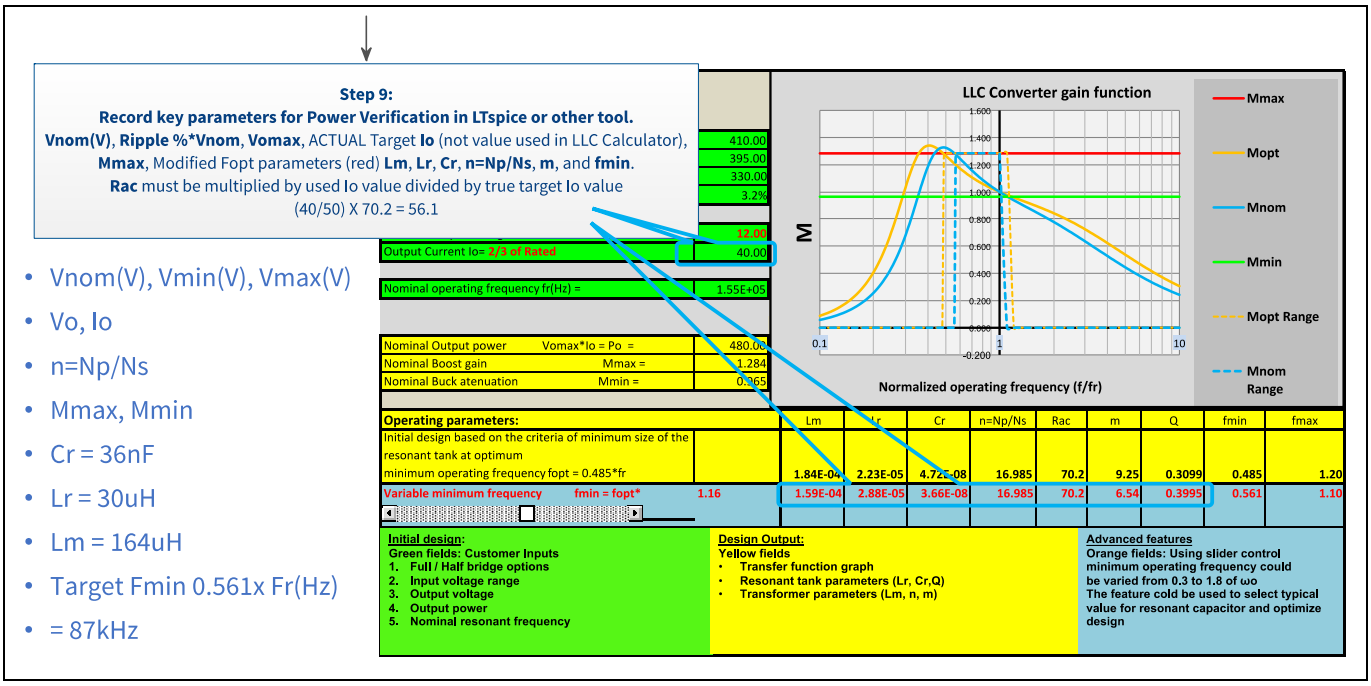

Figure 51 Parameter pass to verification mind map

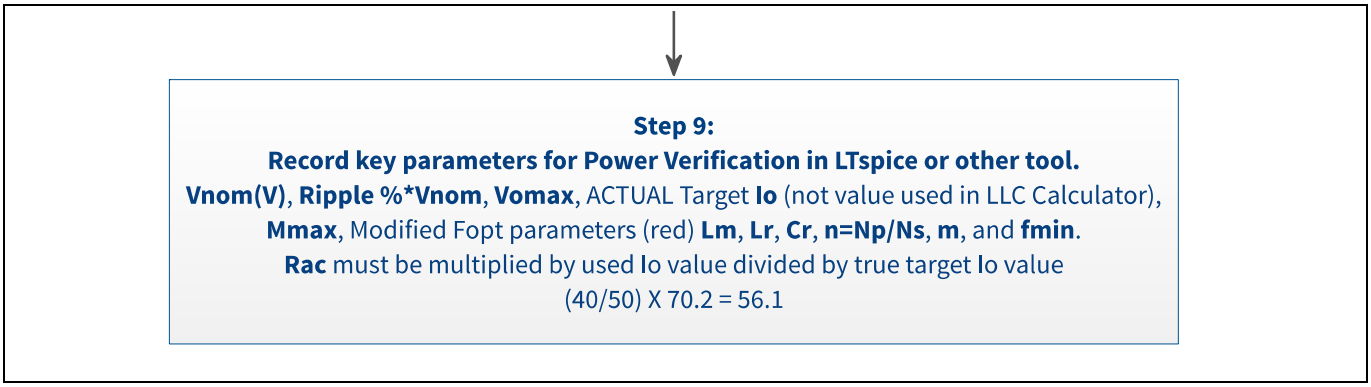

Figure 52 Parameters from the LLC calculator panel

5 Using LTspice as a fast LLC tank design verification tool

5.1 The benefits of a simple parameterized model that runs in tens of seconds, not tens of minutes

An easy-to-use parameterized simulation was developed for the free simulation program LTspice in order to verify the performance results from the key parameters of an LLC tank design, and generate additional data such as the power capability of the network, the RMS operating voltage for the resonant capacitor, etc. Additional analysis is performed interactively using the waveform viewer. The simulation format does not use proprietary or exclusive features and can be adapted to other simulation programs. It also does not use conventional switch models, MOSFETs or gate driver circuits, which is a key contribution to the speed.

Key functionality and features include:

- Use of a transient mode simulation with a unity gain transformer, with the LLC tank using a simplified swept frequency unipolar drive, but with with full modeling of the non-linear input and output stage configuration in DCM and buck mode (**Figure 53**).
- The minimum V_{in} is used as the primary-side test voltage, and the nominal bus voltage is used as the secondary-side test parameter to test tank gain, using a unity gain coupling transformer.
- Verification of key parameters, including Fr(Hz) unity gain frequency, M_{max} gain for low-line operation, nominal FSW for rated power, and power output margin.
- Fulfills the need to have exact calculation based on non-linear primary- and secondary-side circuits to verify V_{in_min} regulation and actual power margin capability, along with component stress such as maximum RMS voltage on resonant capacitor Cr.
- Only a parameter list in the SPICE directives needs to be updated for most different LLC configurations – parameterized model elements are used.
- Verification data is obtained via interactive measurement in the graph window and additional saved data in the .LOG file.

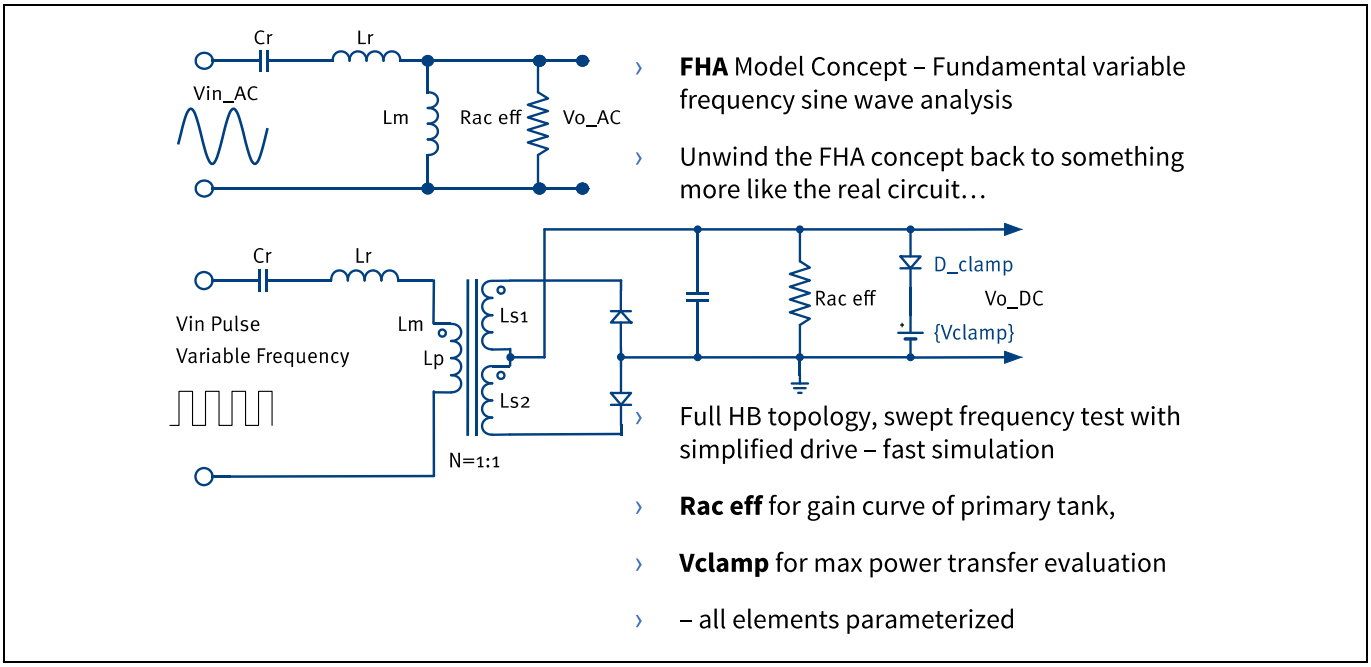

Figure 53 FHA vs simplified full non-linear primary and secondary verification schematics

5.2 LTspice circuit example for wide input range parameterized n = 17T design

The parameterized simulation circuit is shown in **Figure 54**. Key component parameters are set up by a separate section (see below) set-up for user entry of the converter parameters, and from this actual component parameters are caculated to set up the simulation. There are three main blocks to the circuit:

- The primary-side tank square-wave drive is generated by the combination of an LTC6990 VCO oscillator and the parameterized voltage gain block E1. This is an older version of the LTC6990 model, which doesn't have a delay in start-up time and is provided with the simulation circuit files.
- A ramped voltage source VC1 is used to sweep the input current on the "SET" pin of U1, thus sweeping the frequency range from high to low, similar to the classic start-up method for the LLC converter.
- The variable-frequency square wave at the output of E1 drives the primary-side LLC tank (consisting of parameterized components Lr, Cr and Lm) with an output voltage equivalent to the low-line input voltage.
- The coupled inductor/transformer structure is unity gain, with the half-bridge center-tapped output configuration, driving a conventional LLC half-bridge rectifier and filter.
- The clamping circuit for evaluating maximum power at minimum V_{in} with full M_{nom} boost-up gain is composed of the parameterized voltage source V1 and diode D3. It is set to clamp just above the nominal bulk operating voltage point for nominal input voltage.
- Operating points with voltage and current can be determined interactively using the definitions set-up in the plot file, and the maximum power capability is quickly determined from data saved in the .LOG file (average and RMS output current and output voltage).
- A filtered approximation of the current output power is provided at the PWR_Out net.
- Run-time is fast – typically under 15 seconds on a 2016 MacBook Pro with 64 bit LTspice. Run-time may be slower on other versions of LTspice and computer systems, but will rarely be over a minute.

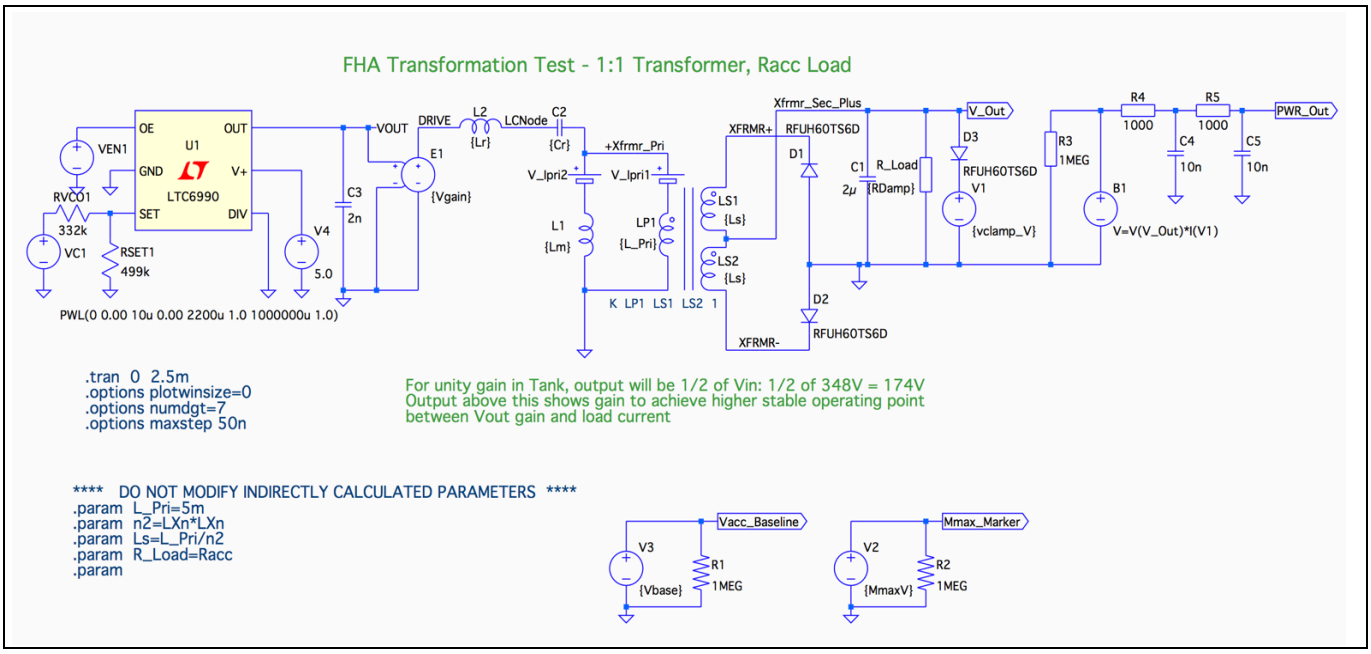

Figure 54 Parameterized LTspice verification simulation

5.2.1 Entering values for parameterized SPICE directives on the schematic sheet

Only a few parameters need to be entered by the user by editing the appropriate SPICE directive lines on the schematic, as shown in **Figure 55** with the complete simulation parameterization pane.

- Tank parameters Lm, Cr and Lr (using standard notation for scaling such as n, u, k, etc.).
- The net R_{acc} value for the effective primary-side full load reflected from the output back through the transformer to the primary-side LLC tank. This is calculated in the LLC calculator, but should be corrected to reflect the true full-load condition, not a ROT-modified lighter load.
- The input voltage test range is entered with two parameters:
  - V_{nom} for the nominal input voltage given to the LLC calculator, which sets the transformer turns ratio and the input voltage operating point at resonance; this is used as the test voltage to determine if the converter can deliver the necessary M_{nom} boost gain at low-line input.
  - V_{in}, which is the minimum line input voltage; this is actually used as the source voltage for the LLC tank configuration under test.
- This ends the user input area…
- Calculated parameters include:
  - the output test V_{clamp}, for maximum power check
  - the M_{max} marker, setting a marker line for verifying delivery of M_{max} gain
  - vacc_baseline, the output voltage check boundary indicating unity gain for the tank (cross-check with frequency to verify the LLC tank Fr(Hz)
  - parameters for the drive circuitry.
- .LOG commands, to set up saving AVG and RMS current and voltage measurements in the log file, primarily for power margin capability (multiply sum of AVG current in I(D1) and I(D2) times V_{out} RMS).

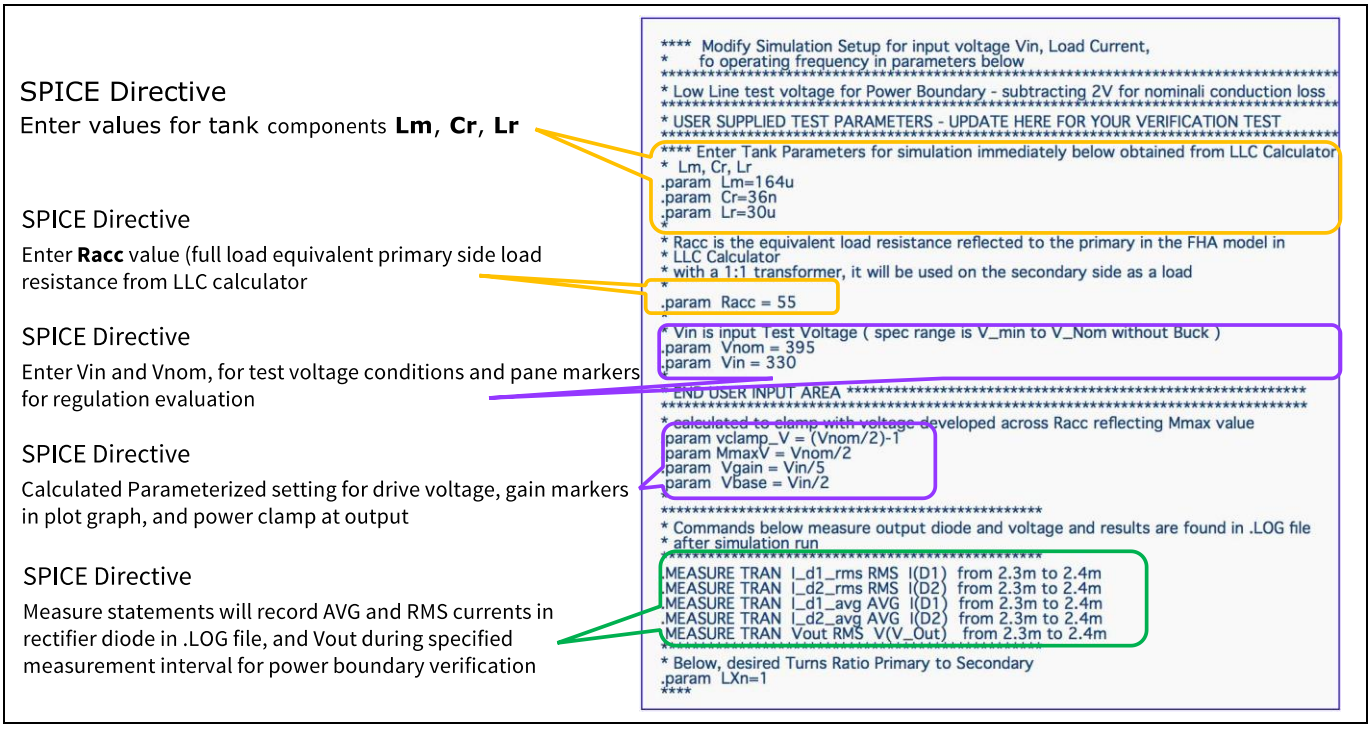

Figure 55 Using the SPICE directives list to enter tank and system parameters

5.2.2 Simulation results ready for evaluation

The full simulation time transient run of 2.5 ms is shown in **Figure 56**. The line markers for $V_{(vacc\_baseline)}$ and $V_{(mmax\_marker)}$ define the expected voltage levels for when the tank reaches unity gain at $V_{(vacc\_baseline)}$ and when the output gain reaches the required maximum boost value M_{max} at $V_{(mmax\_marker)}$. A detailed look at the DCM mode region (tank boost-up) with cursor read-outs at the onset of power delivery, rated power and approximately maximum power is shown in **Figure 57**.

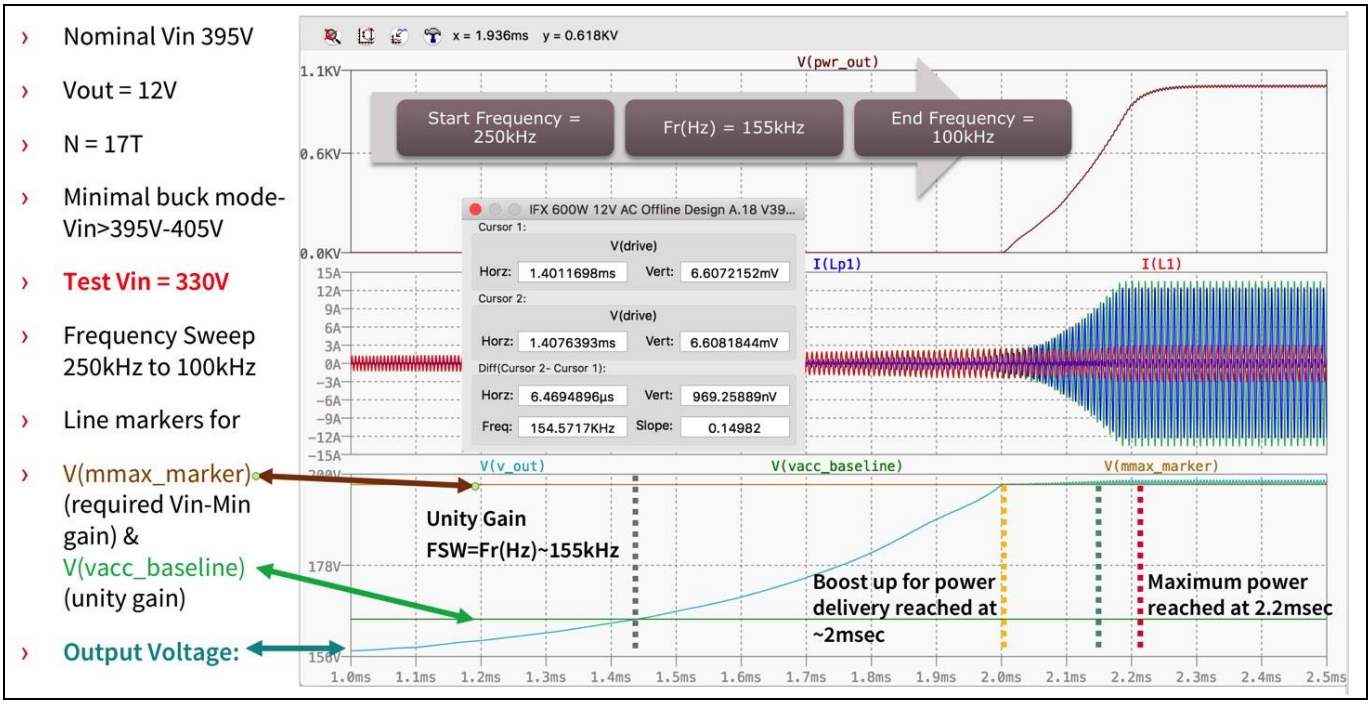

Figure 56 Annotated graph, simulation run completed, ready for interactive data analysis

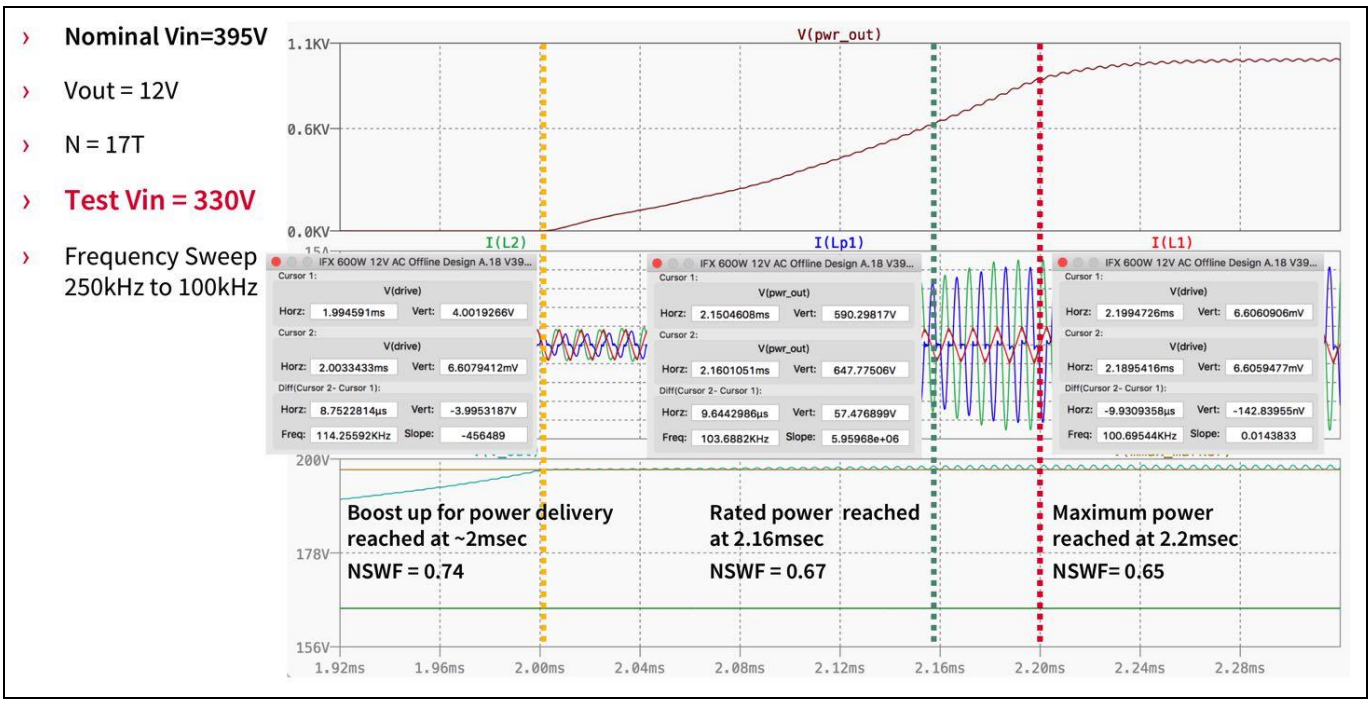

Figure 57 Detailed look at DCM region in boost-up mode

Key data points in Figure 57 are highlighted with the vertical dashed lines that have been added to the graph with notations added for NSFW. These include:

1. The switching frequency where the boost-up gain is sufficient to initiate power delivery into the clamped output; i.e. when the DCM boost at V_{min} input reaches the nominal bulk voltage as for normal operation (this is the orange-colored dashed vertical line).
2. The switching frequency where the boost-up gain is sufficient for power delivery to approximately reach the rated output power of 600 W (this is the teal-colored vertical dashed line).
3. The switching frequency where the boost-up power available is “maxing out” and the converter is near the borderline frequency between inductive and capacitive load (this is the red-colored dashed vertical line).

5.2.3 Interactive calculation of total current, power output, etc.

Interactive measurements are available which give details including both average and RMS currents through components such as the output rectifier diodes. This can be done at any point in the frequency and output voltage sweep, to evaluate operating conductions including possible thermal stress from high RMS factors related to the average current flow. Component currents of interest include the Lr RMS current, the Lm RMS and peak current, etc.

In the example of **Figure 58**, the averaged calculated total output power is shown at roughly the full power point (keeping in mind this is for minimum input voltage). These waveform data captures and calculations show a delivered output power of about 650 W. This point is before the swept frequency has reached its minimum value.

A critical factor in this frequency range is the RMS voltage across the resonant capacitor, as it will need to be sized for that capability – this usually means using a higher voltage-rated cap than may be expected, and often two smaller caps in parallel – which is facilitated by the preferred half-bridge center-tapped configuration.

From this detail of the differential mode measurement across the resonant capacitor Cr, the RMS voltage across the capacitor can be calculated for specific load point conditions. Note in **Figure 56** how rapidly the V-Cr peak-to-peak value rises after entering the delivered power measurement region at 2 ms into the simulation.

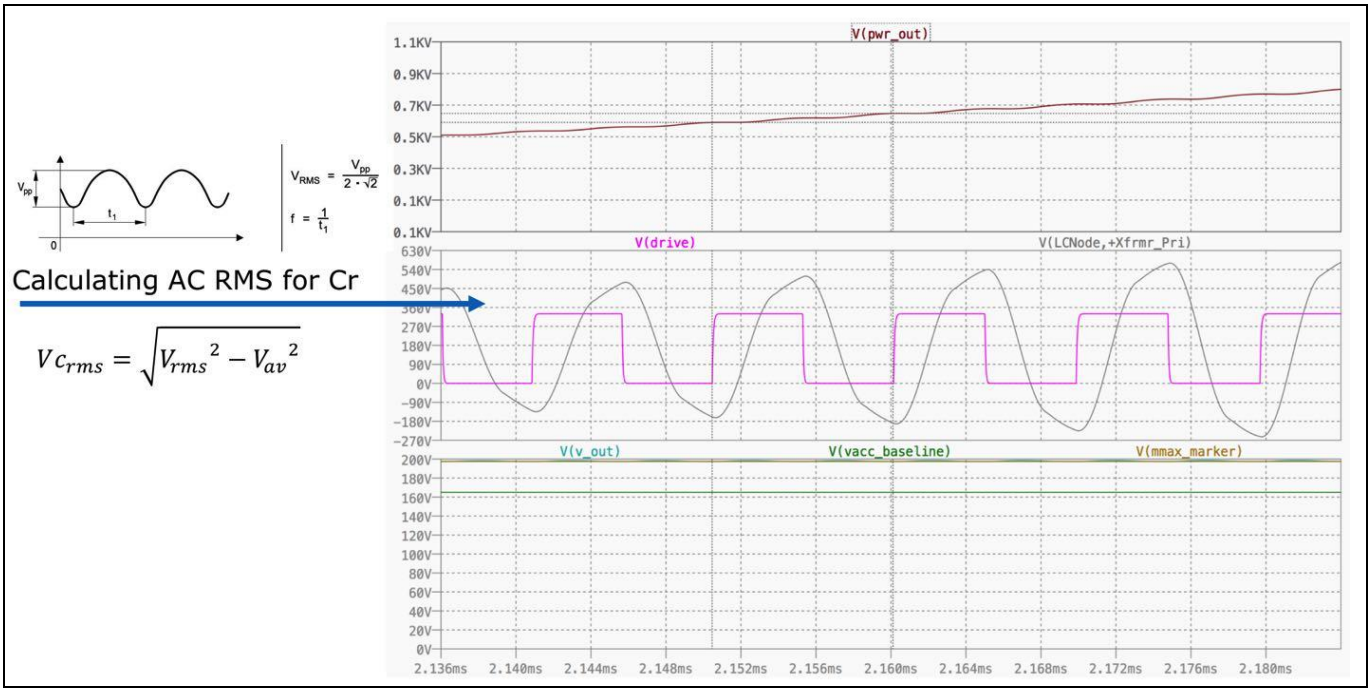

Figure 58 Simulation of interactive measurement in plot mode of LTspice

Opening the .LOG file and a summary of the simulation execution plus the requested data log can be read out, as in **Figure 59**. In this case, the data log is set up for recording average and RMS currents through the output diodes and the output voltage over the interval from 2.3 to 2.4 ms. Multiplying the sum of the diode currents and the output voltage:

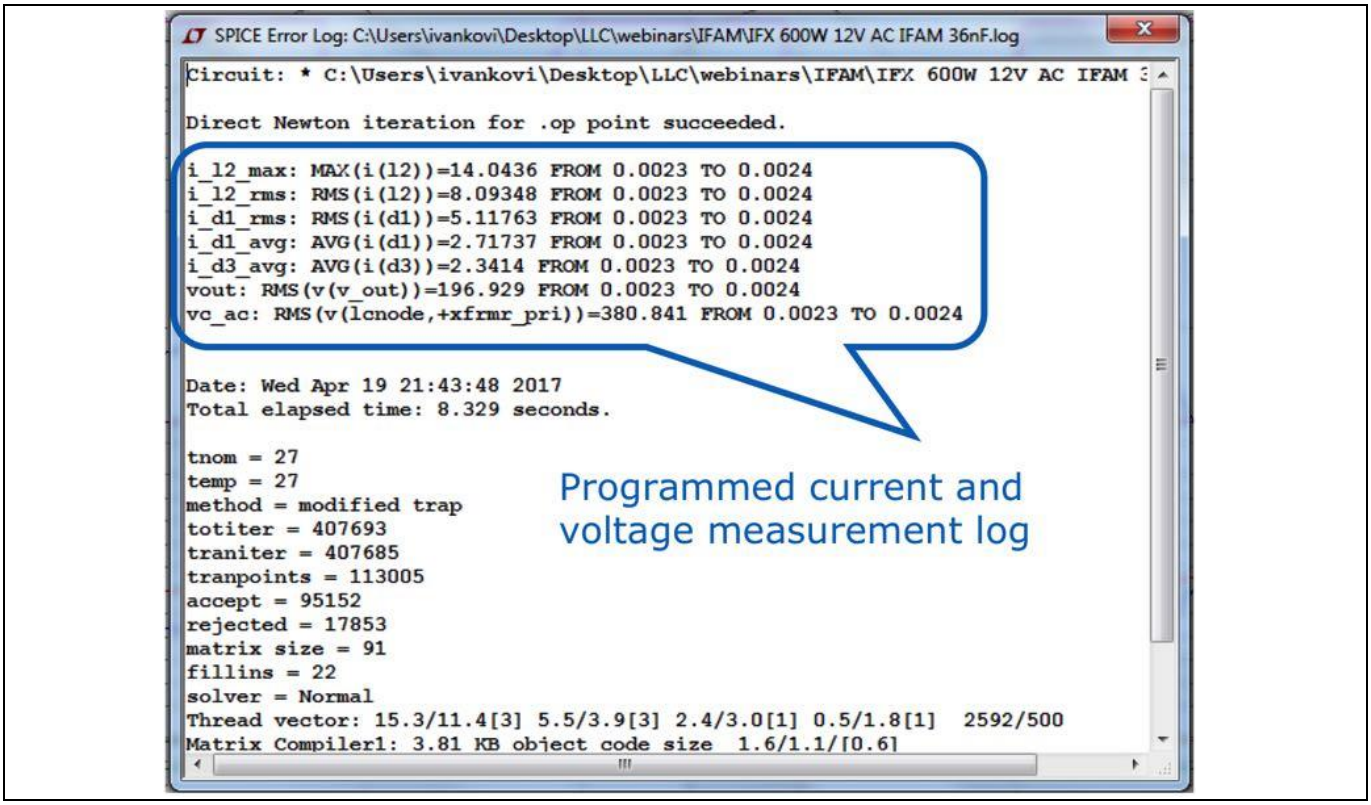

Figure 59 Data log file with programmed measurements in specified time intervals (set by SPICE directives on main schematic sheet – can be updated/added to by user)

This method with low-/no-cost simulation and interactive measurement is more time-consuming and somewhat less precise than the MatLAB program, but this is off-set by the far lower tool cost, and can provide satisfactory results in most cases.

6 Summary

A number of key points were driving the development of this technique, in consideration of the improvements in both the design process and the results:

- FHA misses important time-domain behavior at the heart of LLC functioning – the resonant mode charge pump formed with Cr.
- FHA under-predicts the output capability, and predicts a lower Q required, resulting in higher Cr, lower Lr and lower Lm, increasing primary-side losses.
- FHA models assume variable-frequency sine wave and miss the RMS factor increase in current on the secondary when using m-ratios with large values in order to “optimize” the primary-side current with FHA.
- Reverse FHA analysis does not accurately predict the gain capability and power margin of the LLC tank, and flags designs with more efficient tank designs in the real world – the bumble bee can fly well, and with lower losses overall with the correct tank configuration.
- With the use of some design ROT, the LLC calculator based on vector analysis calculations can be used to visualize and propose more optimum LLC tank designs than a conventional FHA approach, and runs well in an Excel environment.
- LTspice and other non-linear capable tools will tell the truth in verification and, using the right model format, do so quite quickly to confirm the main LLC converter parameters.
- Two high-performance alternative tank alignments have been presented for the Infineon/Finepower 12 V 600 W LLC converter using the existing transformer turns ratio n = 16:
  - one focused on improving light-load efficiency
  - one focused on minimizing secondary-side RMS current in the converter at low-line operation as well as any input voltage
  - both had lower RMS operating currents than the original design at any operating point, but with different end-point optimizations.
- A wide input range 12 V 600 W example has been proposed for WBG semiconducters using a transformer turns ratio of n = 17, illustrating how with wide input range capability, components might be reduced in size for the complete SMPS, with improved efficiency and power density, while demonstrating how ROT works with the LLC calculator gain results, and comparing these results to detailed exact mode calculations.
- The use of LTspice with a specifically designed simulation methodology is shown, which can verify tank behavior in under 30 seconds in typical cases with a high-performance notebook computer.

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Revision history

Major changes since the last revision

Page or reference	Description of change

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