Package Thermal Datasheet

PG-VQFN-48-31

About this document

This document aims at providing information about the thermal characteristics of the Infineon package PG-VQFN-48-31, used for Infineon Embedded Power ICs (Grade-1). The document contains details regarding dimensions, package outline, products involved, and a detailed overview of the thermal resistance characteristics of the package.

Intended audience

This document is intended for customers who would like to have information of the thermal characteristics of the package used, and the products making use of it.

Disclaimer

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1 Package Dimensions

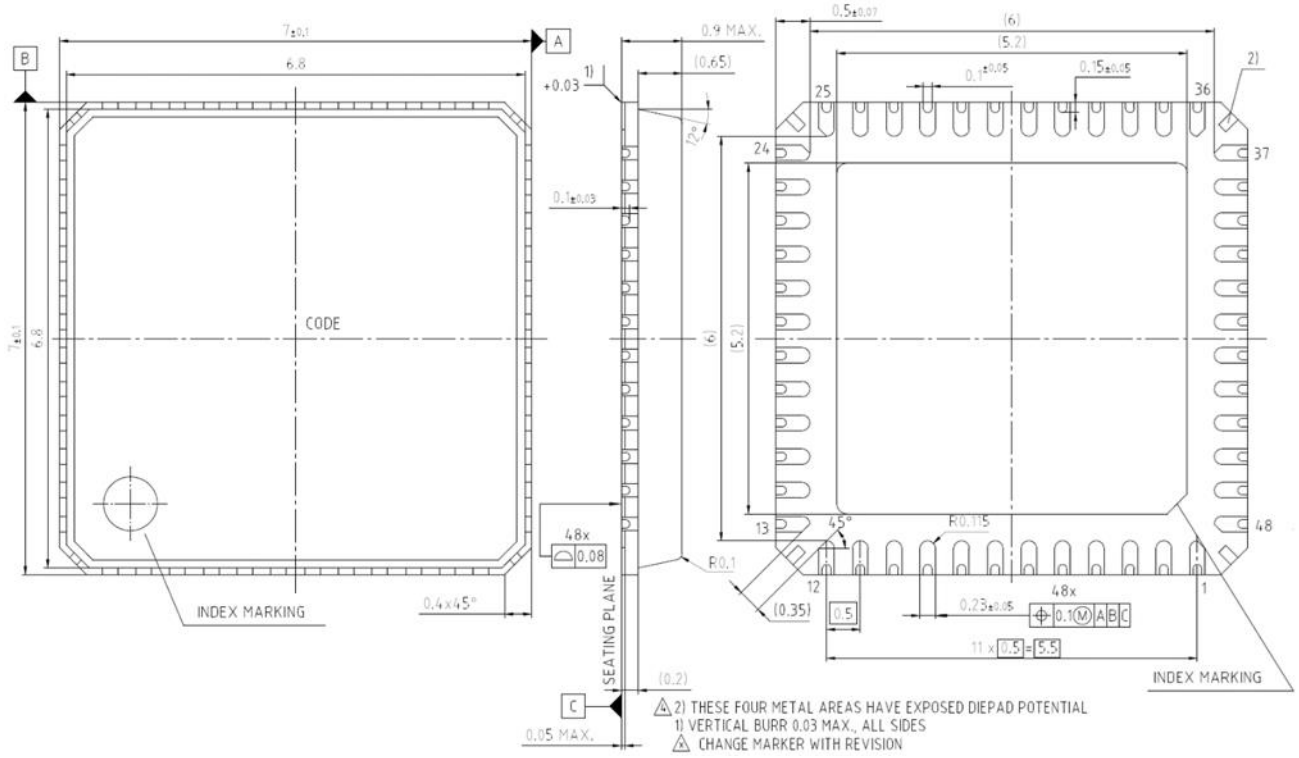
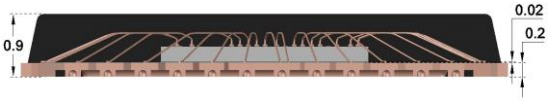
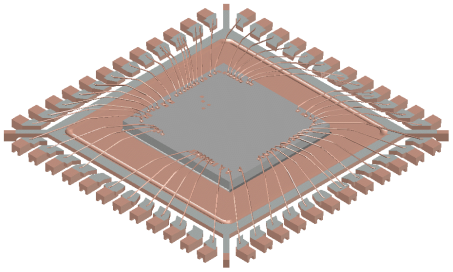


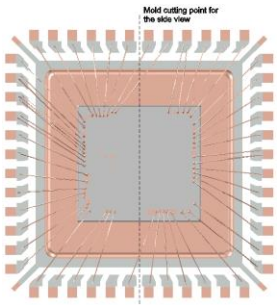
Figure 1: Package outline drawing for PG-VQFN-48-31 with dimensions



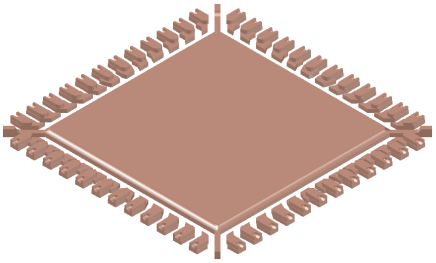
Side view



3D view (w/o mould compound)



Top view (w/o mould compound)



Bottom view (leadframe only)

Figure 2: 3D view of the package (TLE9861QXA20)

2 List of Embedded Power Products in PG-VQFN-48-31

Relay Driver IC with Integrated Arm® Cortex®-M0

Product name	Flash [KB]	Freq [MHz]	RAM [KB]	EEPROM in Flash incl. [KB]	High-side switch	High voltage monitor input	Interface
TLE9842QX	36	25	2	4	1	4	PWM + LIN
TLE9842-2QX	40	40	2	4	2	5	PWM + LIN
TLE9843QX	48	25	4	4	1	4	PWM + LIN
TLE9843-2QX	52	40	4	4	2	5	PWM + LIN
TLE9844QX	64	25	4	4	1	4	PWM + LIN
TLE9844-2QX	64	40	4	4	2	5	PWM + LIN

Half-Bridge Driver IC with Integrated Arm® Cortex®-M0

Product name	Flash [KB]	Freq [MHz]	RAM [KB]	EEPROM in Flash incl. [KB]	High-side switch	High voltage monitor input	PN MOS driver	Low-side MOSFET drivers	High-side MOSFET drivers	Interface
TLE9845QX	48	40	4	4	2	5	YES	-	-	PWM + LIN
TLE9850QX	48	40	4	4	1	4	NO	1	1	PWM + LIN

H-Bridge Driver IC with Integrated Arm® Cortex® M0

Product name	Flash [KB]	Freq [MHz]	RAM [KB]	EEPROM in Flash incl. [KB]	High-side switch	High voltage monitor input	Low-side MOSFET drivers	High-side MOSFET drivers	Interface
TLE9853QX	48	40	4	4	1	4	2	2	PWM + LIN
TLE9854QX	64	40	4	4	1	4	2	2	PWM + LIN
TLE9855QX	96	40	4	4	1	4	2	2	PWM + LIN
TLE9852QX	48	40	4	4	1	4	2	2	PWM + LIN

H-Bridge Driver with Integrated Arm® Cortex®-M3

Product name	Flash [KB]	Freq [MHz]	RAM [KB]	EEPROM in Flash incl. [KB]	OP-AMP	SD-ADC	Low-side MOSFET drivers	High-side MOSFET drivers	Interface
TLE9861QXA20	36	24	3	4	YES	-	2	2	PWM
TLE9862QXA40	256	40	8	4	YES	-	2	2	PWM + LIN
TLE9867QXA20	64	24	6	4	YES	-	2	2	PWM + LIN
TLE9867QXA40	64	40	6	4	YES	-	2	2	PWM + LIN
TLE9868QXB20	128	20	4	4	YES	YES	2	2	PWM + LIN
TLE9869QXA20	128	24	6	4	YES	-	2	2	PWM + LIN

3-Phase Bridge Driver with Integrated Arm® Cortex®-M3

Product name	Flash [KB]	Freq [MHz]	RAM [KB]	EEPROM in Flash incl. [KB]	OP-AMP	SD-ADC	Low-side MOSFET drivers	High-side MOSFET drivers	Interface
TLE9871QXA20	36	24	3	4	YES	-	3	3	PWM
TLE9872QXA40	256	40	8	4	YES	-	3	3	PWM + LIN
TLE9872-2QXA40	256	40	8	4	YES	YES	3	3	PWM + LIN
TLE9877QXA20	64	24	6	4	YES	-	3	3	PWM + LIN
TLE9877QXA40	64	40	6	4	YES	-	3	3	PWM + LIN
TLE9879QXA20	128	24	6	4	YES	-	3	3	PWM + LIN
TLE9879QXA40	128	40	6	4	YES	-	3	3	PWM + LIN
TLE9879-2QXA40	128	40	6	4	YES	YES	3	3	PWM + LIN

3 Thermal Resistance Definition

Package thermal resistance is the measure of a package's heat dissipation capability from a die's active surface (junction) to a specified reference point (case, pin, ambient, etc.). The value of thermal resistance depends on many factors, such as ambient temperature, PCB board used and much more. This chapter describes in details boundary conditions we use in the definition of various thermal resistances.

We divide thermal resistance into two groups: junction-to-case thermal resistance (package only) and junction-to-ambient thermal resistance (with PCB and housing). Below table shows the overview.

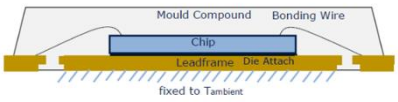
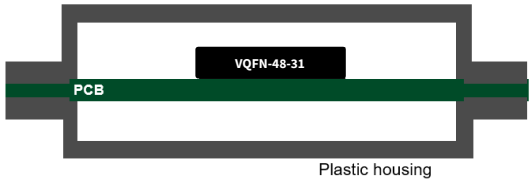
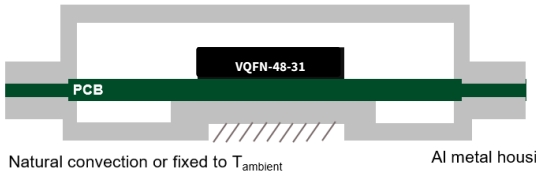
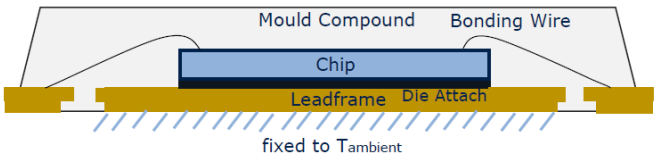
Package only	With PCB and housing
Junction to case thermal resistance: 	Junction to Ambient thermal resistance:  $R_{th\text{-}JA\ 2s2p}$ $R_{th\text{-}JA\ 1s0p}$ $R_{th\text{-}JA\ 1s0p}/1000mm^2$
	Junction to Housing thermal resistance:  $R_{th\text{-}JH1}$ $R_{th\text{-}JH2}$

Figure 3: Boundary conditions for thermal resistance definition
for package only (left column) and with PCB and housing (right column)

3.1 Package only

3.1.1 Junction-to-case thermal resistance ($R_{th\text{-}JC}$)



- The backside of the exposed pads is fixed to $T_{ambient}$
- The other side of the package has an adiabatic boundary condition

3.2 With PCB and housing

3.2.1 Junction-to-ambient thermal resistance ($R_{th\text{-}JA\ 2s2p}$)

- Only JEDEC (Joint Electron Device Engineering Council) board is used for thermal assessment. PCB construction is according to JEDEC standards 2s2p, with thermal vias placed under exposed pad as much as possible.
- PCB size – 74*116*1.5 mm
- Number of thermal vias – 16. Thermal vias are connected to only one Cu inner layer
- Natural Convection

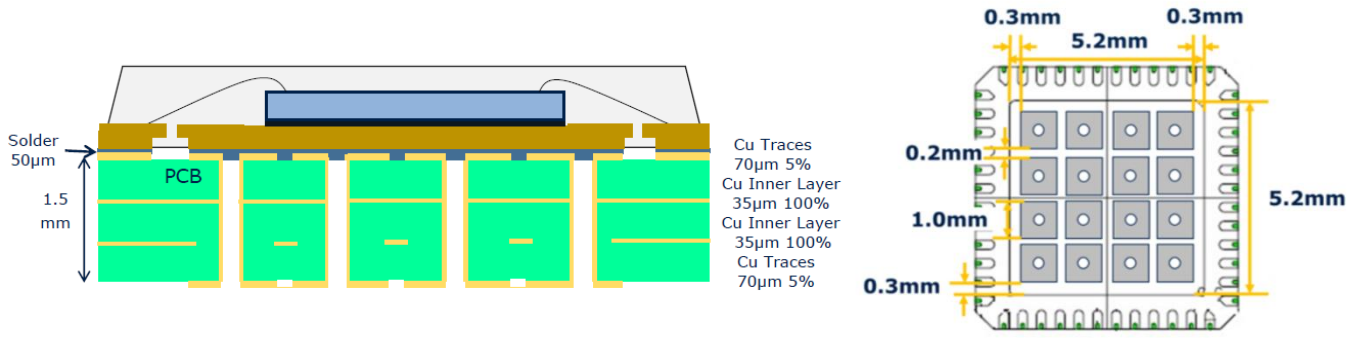
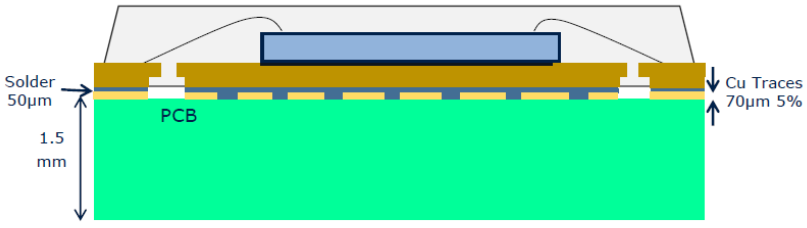


Figure 4: $R_{th\text{-}JA\ 2s2p}$ schematic and top view of JEDEC thermal vias.

3.2.2 Junction-to-ambient thermal resistance ($R_{th\text{-}JA\ 1s0p}$)/footprint only



- PCB construction is according to JEDEC standards 1s0p, without thermal vias
- Natural Convection

3.2.3 Junction-to-ambient thermal resistance ($R_{th\text{-}JA\ 1s0p}$)/1000mm² cooling area

- PCB construction is according to JEDEC 1s0p, without thermal vias
- standards 300mm² (or 600mm² or 1000mm²) cooling Cu is connected to the exposed pad on the first PCB layer
- Natural Convection

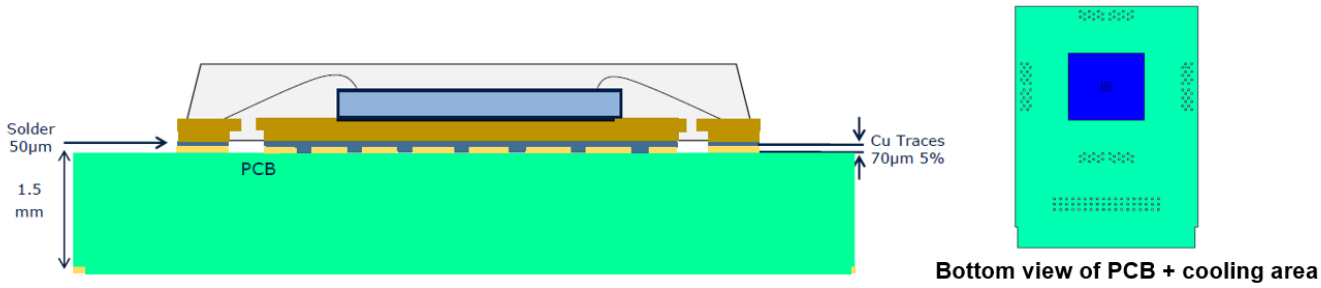
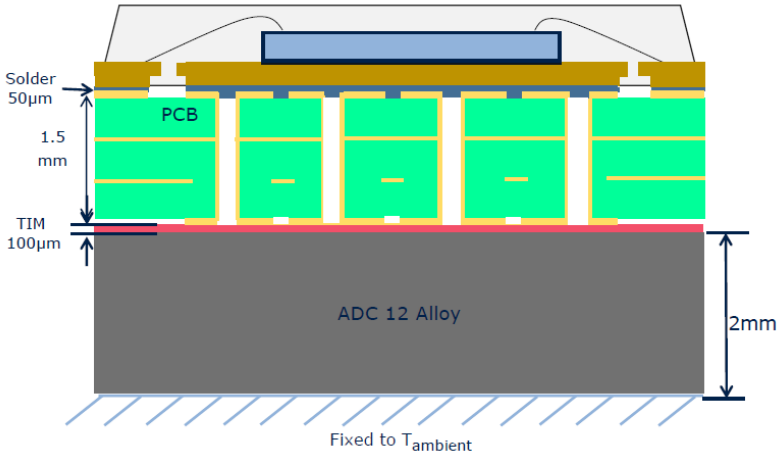


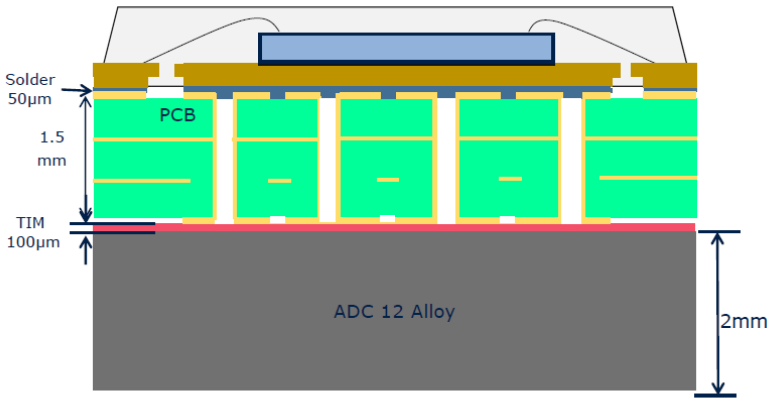
Figure 5: $R_{th\text{-}JA\ 1s0p}$ with 1000mm² Cu cooling area schematic and bottom view of PCB and cooling area.

3.2.4 Junction-to-housing thermal resistance ($R_{th\text{-}JH1}$)



- The backside of the housing is fixed to $T_{ambient}$
- PCB construction is according to JEDEC standards 2s2p, with thermal vias (same as $R_{th\text{-}JA\ 2s2p}$)
- TIM (100µm, 0,7W/mK, X and Y size is double of the package size)
- Housing: 2mm thick, X and Y the same as JEDEC 2s2p board, 92W/mK (alloy name: ADC12)

3.2.5 Junction-to-housing thermal resistance ($R_{th\text{-}JH2}$)



- The backside of the housing has natural convection
- PCB construction is according to JEDEC standards 2s2p, with thermal vias (same as $R_{th\text{-}JA\ 2s2p}$)
- TIM (100µm, 0,7W/mK, X and Y size is double of the package size)
- Housing: 2mm thick, X and Y the same as JEDEC 2s2p board, 92W/mK (alloy name: ADC12)

4 Thermal Characteristics

4.1 Thermal Impedance

To emphasis the impact of housing, Figure 6 shows the schematic once again. And in Figure 7, thermal impedance for TLE984x families (left) and for TLE986x/7x families (right) are presented. Please refer to chapter 3 to know the concrete boundary conditions in the definition of each thermal resistance.

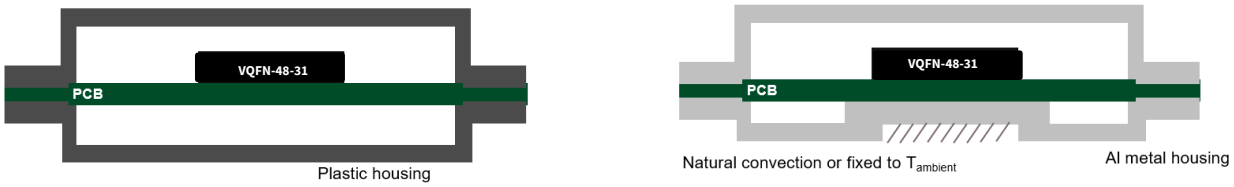


Figure 6: Plastic and metal housing schematics

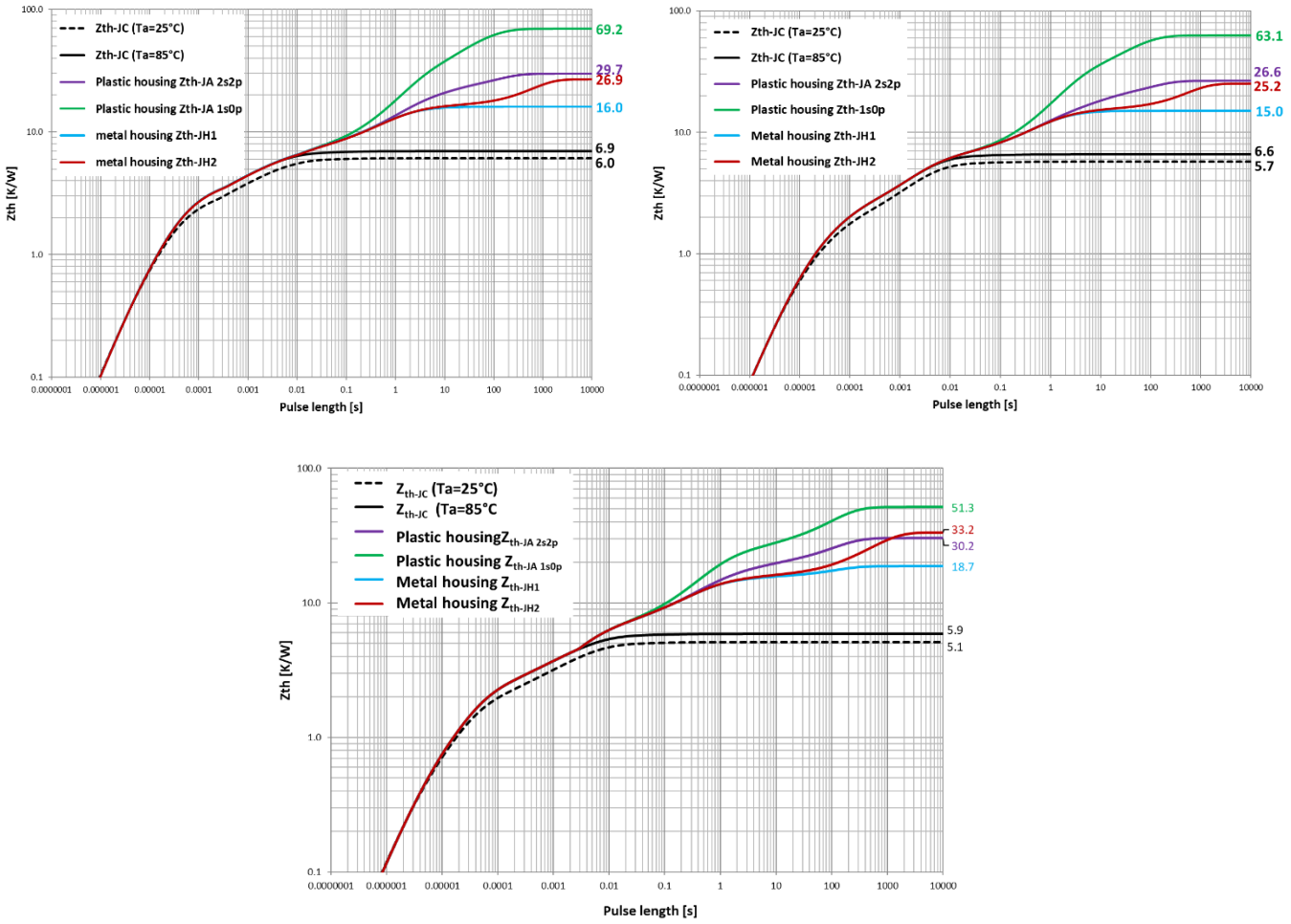


Figure 7: Thermal impedance for TLE984x (top left), for TLE986x/7x (top right) and for TLE985x families (lbottom)

4.2 Temperature Distributions

The temperature distribution in steady state for the setup with metal housing with natural convection at back side as defined in $R_{th\text{-}JH2}$ (see section 3.2.5), is shown below for TLE986x/7x families. All temperatures are in Kelvin. TLE984x families have the similar results.

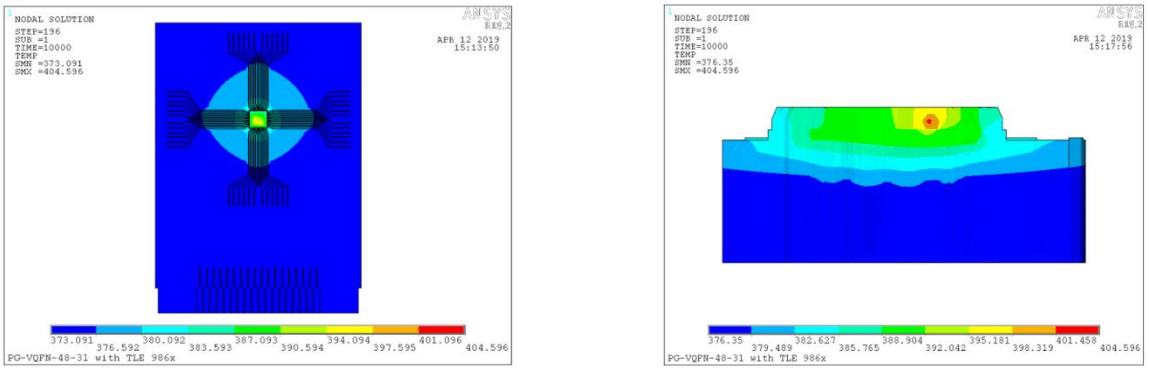
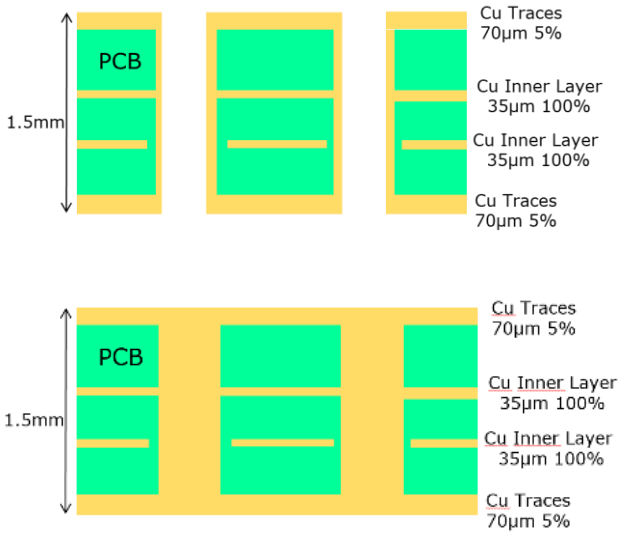


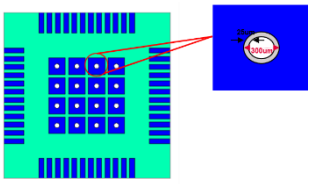
Figure 8: Temperature distribution at steady state for the setup with metal housing and natural convection at the back - top view (left) and side view (right).

4.3 Impact of thermal vias

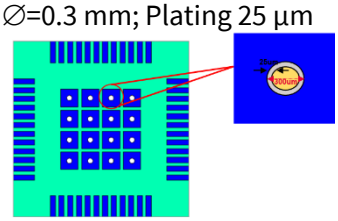
Thermal vias offer thermal short paths within PCB to imporve heat transfer from device to ambient. Besides JEDEC 2s2p board with air-filled and Cu-filled thermal vias, we extended our study on another 2 PCB, noted as PCB type 1 and PCB type 2. The cross section pictures in Figure 9 shows the differences in all set up. The size of PCBs are fixed at 74*116*1.5 mm as in JEDEC standard.



- JEDEC board-Air in vias
- ∅=0.3 mm; Plating 25 µm



- JEDEC board-Cu in vias
- ∅=0.3 mm; Plating 25 µm



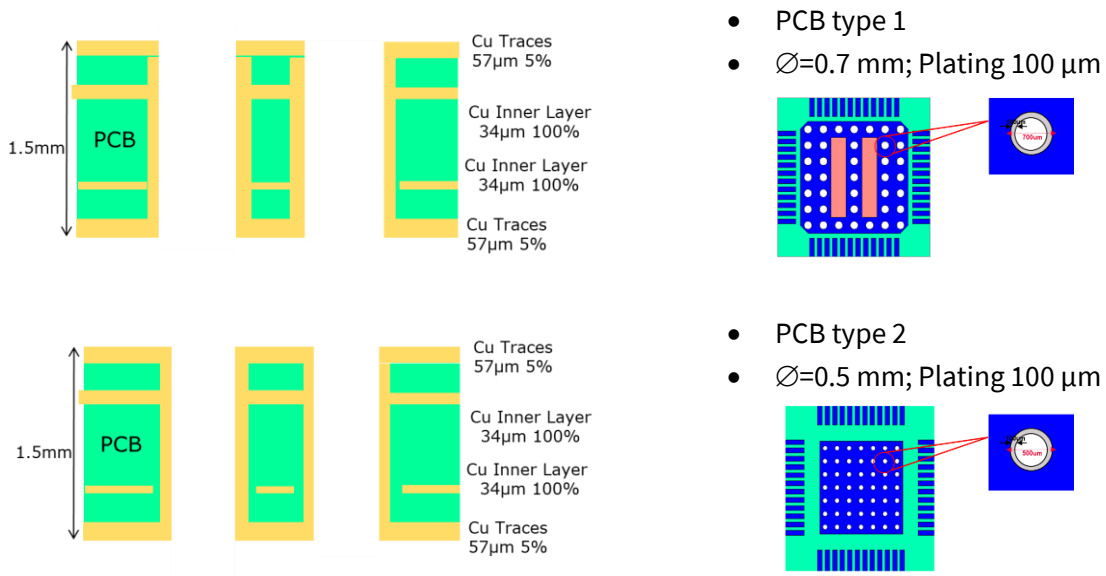


Figure 9: Cross section information of PCB investigated and their thermal vias

Figure 10 is the calculated results of junction to ambient thermal resistance ($R_{th\text{-}JA}$) for different PCB types. Obviously the more number of vias, the lower Rth-JA. Cu-filled vias are slightly better than air-filled vias for JEDEC board. When increasing thermal via diameters and thicker plating wall within the vias, Rth-JA is also improved. Therefore PCB type 1 gives the lowest Rth-JA.
In Chapter 4, all the thermal impedances of our products are calculated with the maximum number of vias in JEDEC board, where an arrow is pointing to on this chart.

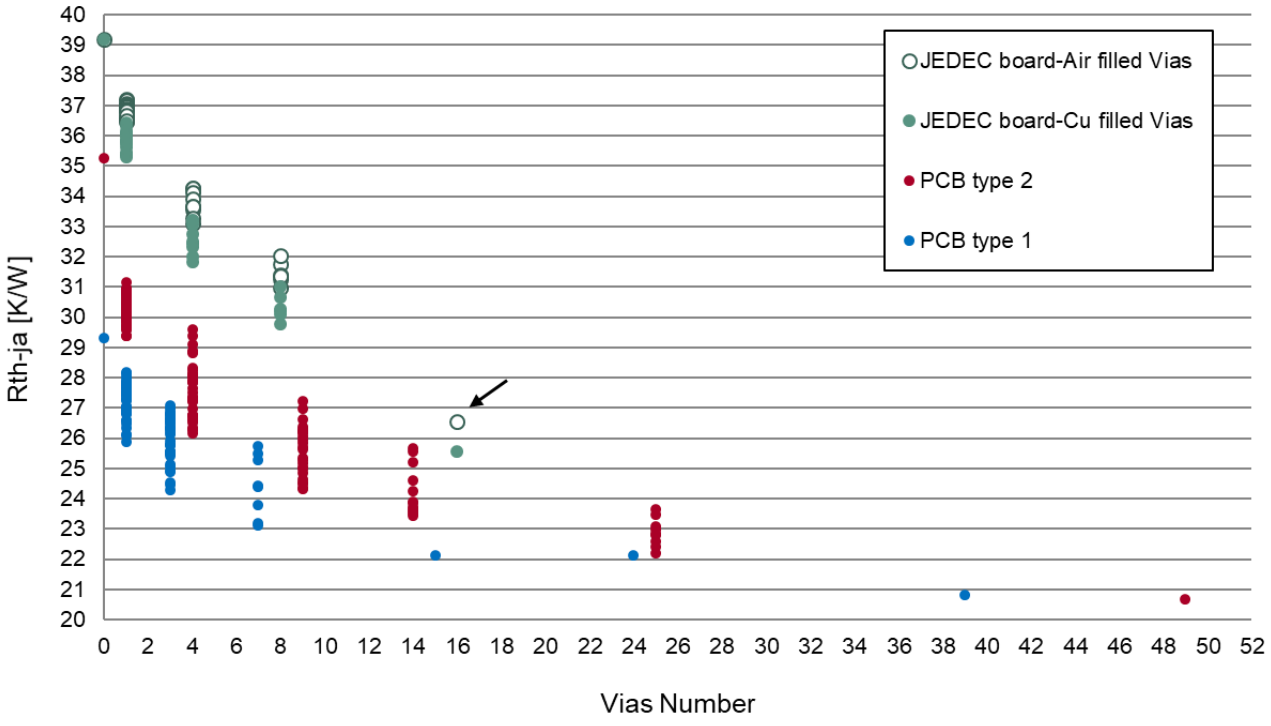


Figure 10: Impact of PCB types and number of thermal vias on Rth-JA

Glossary

R_{th}	Thermal Resistance
$T_{ambient}$	Ambient Temperature
JEDEC	Joint Electron Device Engineering Council
PCB	Printed Circuit Board
2s2p	JEDEC standard two internal copper planes embedded in the circuit board and the trace layer on the top surface of the PCB, ‘s’ refers to the signal layers on both outside surfaces of the board and ‘p’ refers to two power planes in the board (voltage and ground)
1s0p	JEDEC standard no internal copper planes embedded in the circuit board and the trace layer on the top surface of the PCB
ADC	Aluminium Alloy Die Casting
TIM	Thermal Interface Material

Revision History

Major changes since the last revision

Page or Reference	Description of change
Revision 3.0	2020-11-04 – Additonal products included (TLE985x)
Revision 2.0	2019-09-20 – Additional products included (TLE984x)
Revision 1.0	2019-05-16 – Initial Release

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