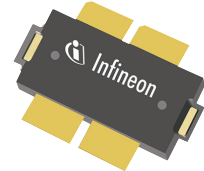


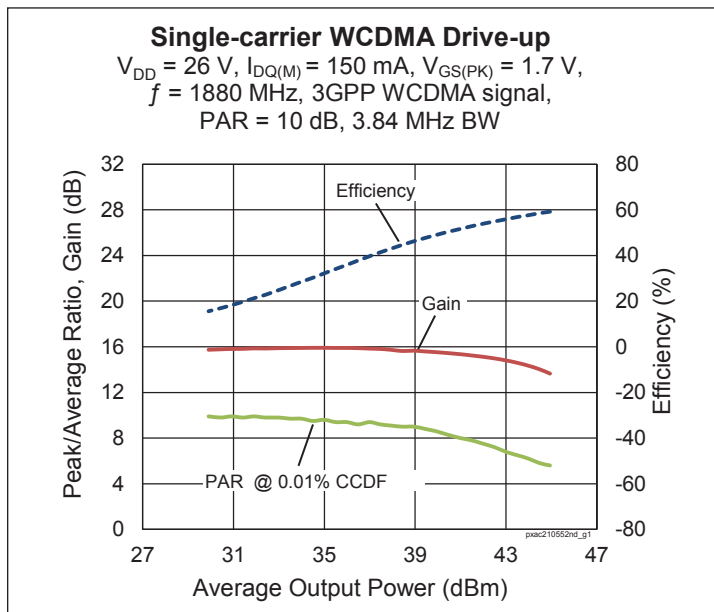
## Thermally-Enhanced High Power RF LDMOS FET 55 W, 28 V, 1805 – 2170 MHz

### Description

The PXAC210552ND is a 55-watt LDMOS FET with an asymmetrical design intended for use in multi-standard cellular power amplifier applications in the 1805 to 2170 MHz frequency band. Features include dual-path design, input matching, high gain and thermally-enhanced package with earless flanges. Manufactured with Infineon's advanced LDMOS process, this device provides excellent thermal performance and superior reliability.



PXAC210552ND  
Package PG-HB1SOF-4-1



### Features

- Broadband internal input and output matching
- Asymmetrical Doherty Design
  - Main:  $P_{1dB} = 20\text{ W Typ}$
  - Peak:  $P_{1dB} = 35\text{ W Typ}$
- Typical Pulsed CW performance, 1880 MHz, 26 V (Doherty Configuration)
  - Output power at  $P_{1dB} = 24.7\text{ W}$
  - Efficiency = 55.3%
  - Gain = 15.05 dB
- Capable of handling 10:1 VSWR @28 V, 55 W (CW) output power
- Integrated ESD protection
- Human Body Model class 1C (per ANSI/ESDA/ JEDEC JS-001)
- Low thermal resistance
- Pb-free and RoHS compliant

### Target RF Characteristics

#### Single-carrier WCDMA Specifications (tested in Infineon Doherty test fixture)

$V_{DD} = 26\text{ V}$ ,  $I_{DQ} = 150\text{ mA}$ ,  $P_{OUT} = 8.5\text{ W avg}$ ,  $V_{GS(PEAK)} = 1.7\text{ V}$ ,  $f = 1880\text{ MHz}$ , 3GPP signal, channel bandwidth = 3.84 MHz, peak/average = 10 dB @ 0.01% CCDF

Characteristic	Symbol	Min	Typ	Max	Unit
Linear Gain	$G_{ps}$	13	14.75	—	dB
Drain Efficiency	$\eta_D$	48	50.5	—	%
Adjacent Channel Power Ratio	ACPR	—	-29	-25	dBc

All published data at  $T_{CASE} = 25^\circ\text{C}$  unless otherwise indicated

ESD: Electrostatic discharge sensitive device—observe handling precautions!

**DC Characteristics** (each side)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}$ , $I_{DS} = 10\text{ mA}$	$V_{(BR)DSS}$	65	—	—	V
Drain Leakage Current	$V_{DS} = 28\text{ V}$ , $V_{GS} = 0\text{ V}$	$I_{DSS}$	—	—	0.1	$\mu\text{A}$
	$V_{DS} = 63\text{ V}$ , $V_{GS} = 0\text{ V}$	$I_{DSS}$	—	—	1.0	$\mu\text{A}$
Gate Leakage Current	$V_{GS} = 10\text{ V}$ , $V_{DS} = 0\text{ V}$	$I_{GSS}$	—	—	0.1	$\mu\text{A}$
On-State Resistance (main)	$V_{GS} = 10\text{ V}$ , $V_{DS} = 0.1\text{ V}$	$R_{DS(on)}$	—	0.38	—	$\Omega$
	(peak) $V_{GS} = 10\text{ V}$ , $V_{DS} = 0.1\text{ V}$	$R_{DS(on)}$	—	0.19	—	$\Omega$
Operating Gate Voltage (main)	$V_{DS} = 26\text{ V}$ , $I_{DQ} = 0.15\text{ A}$	$V_{GS}$	2.1	2.6	3.1	V
	(peak) $V_{DS} = 26\text{ V}$ , $I_{DQ} = 0\text{ A}$	$V_{GS}$	1.2	1.7	2.2	V

**Maximum Ratings**

Parameter	Symbol	Value	Unit
Drain-Source Voltage	$V_{DSS}$	65	V
Gate-Source Voltage	$V_{GS}$	-6 to +10	V
Junction Temperature	$T_J$	225	$^{\circ}\text{C}$
Storage Temperature Range	$T_{STG}$	-65 to +150	$^{\circ}\text{C}$

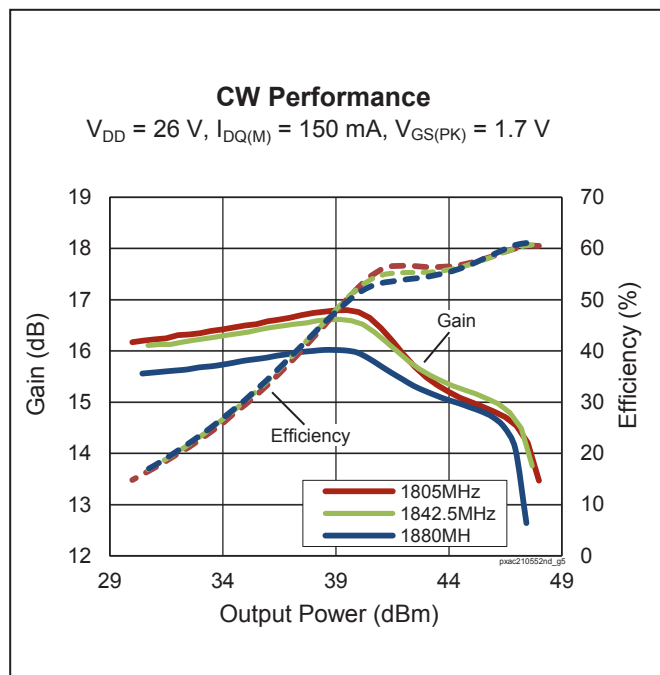
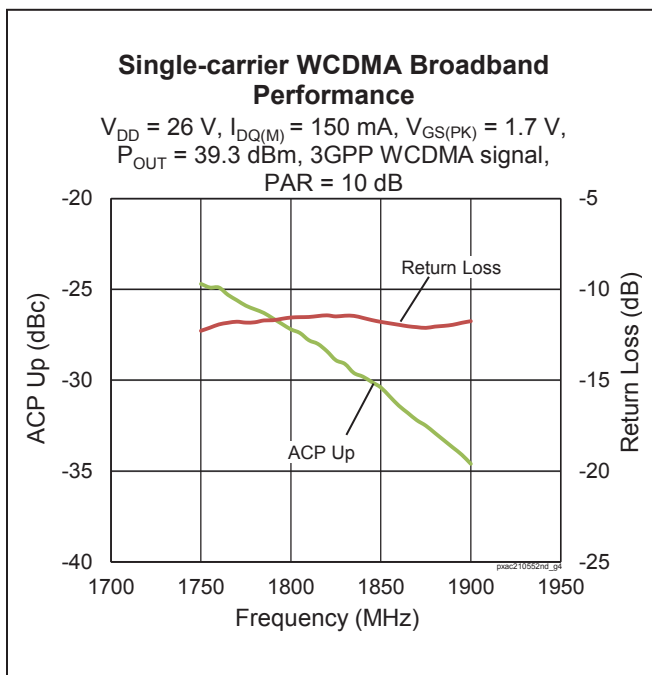
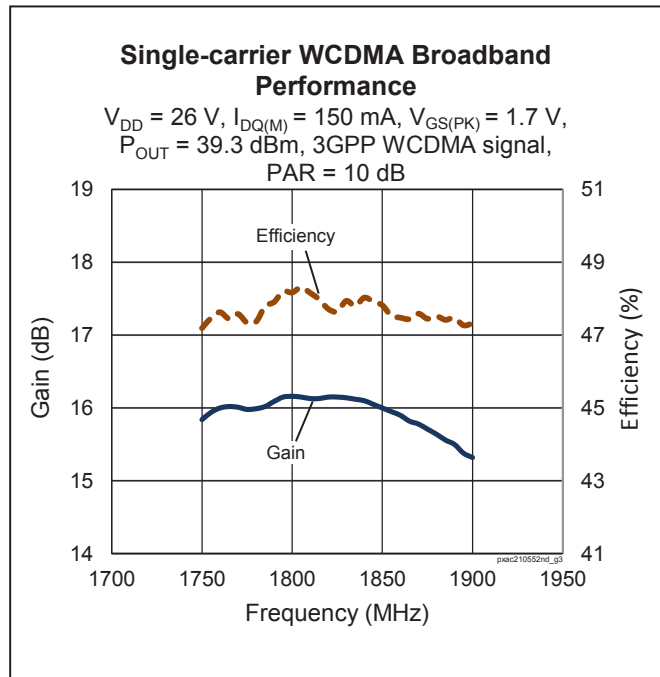
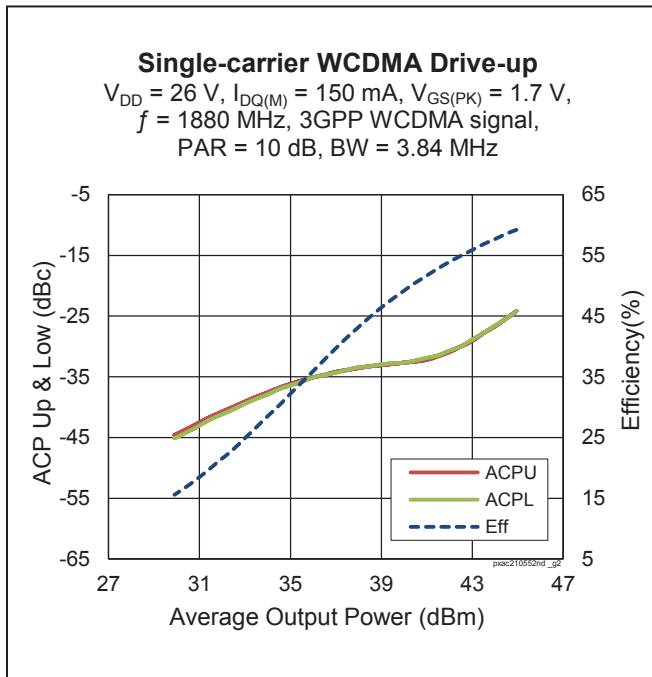
**Thermal Characteristics**

Parameter	Symbol	Value	Unit
Thermal Resistance ( $T_{CASE} = 85^{\circ}\text{C}$ , 8.5 W CW)	$R_{\theta JC}$	1.0	$^{\circ}\text{C}/\text{W}$

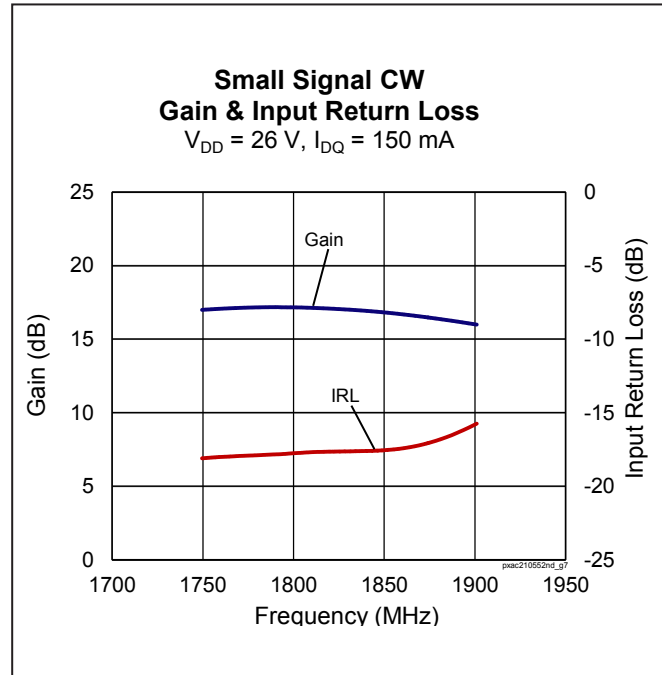
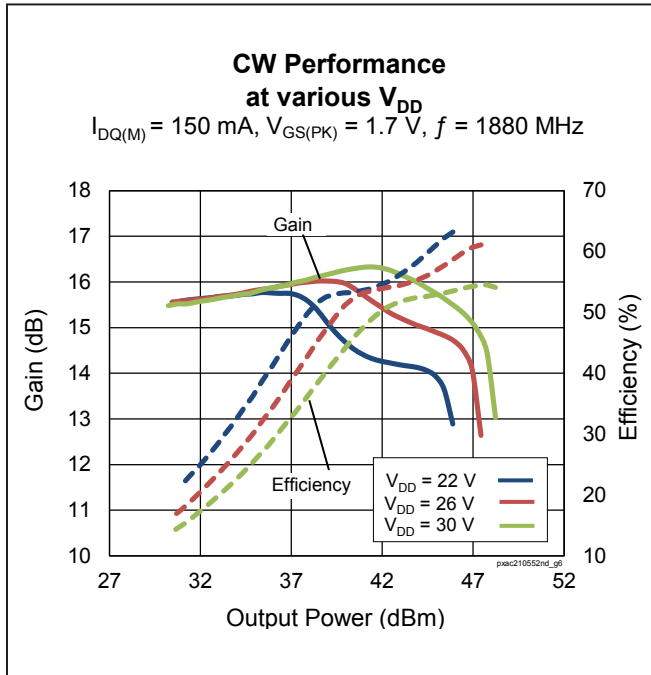
**Ordering Information**

Type and Version	Order Code	Package Description	Shipping
PXAC210552ND V1 R5	PXAC210552NDV1R5XUMA1	PG-HB1SOF-4-1	Tape & Reel, 500 pcs

**Typical RF Performance** (data taken in production test fixture)



Typical RF Performance (cont.)



Load Pull Performance

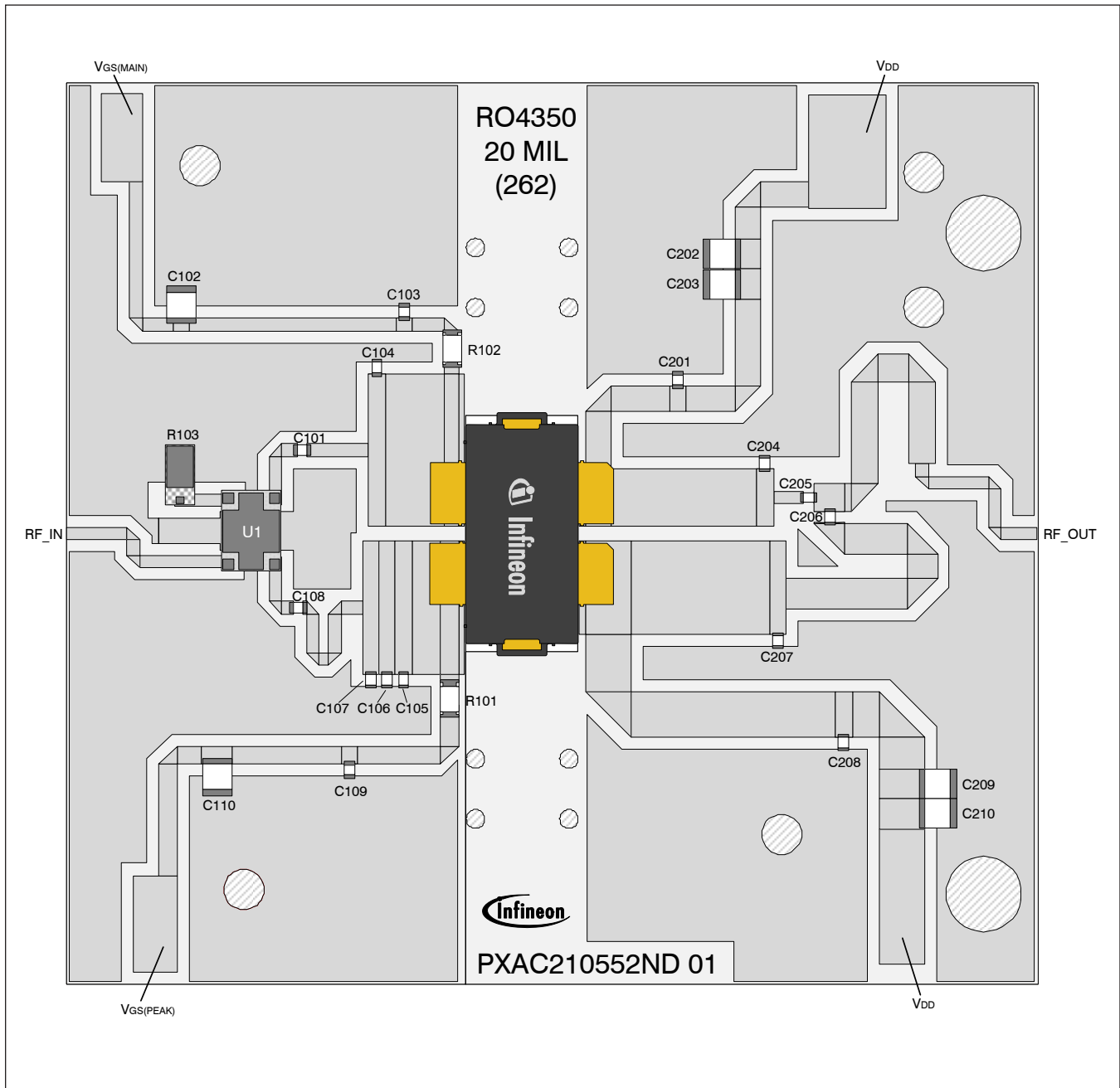
Main Side Load Pull Performance – Pulsed CW signal: 16  $\mu\text{s}$ , 10% duty cycle, 28 V,  $I_{DQ} = 150 \text{ mA}$

Freq [MHz]	$Z_s$ [ $\Omega$ ]	$P_{1dB}$									
		Max Output Power					Max PAE				
		$Z_l$ [ $\Omega$ ]	Gain [dB]	$P_{OUT}$ [dBm]	$P_{OUT}$ [W]	PAE [%]	$Z_l$ [ $\Omega$ ]	Gain [dB]	$P_{OUT}$ [dBm]	$P_{OUT}$ [W]	PAE [%]
1805	3.39-j11.75	19.9	57.2	43.89	24.5	10.73-j4.59	21.7	64.5	42.40	17.4	21.9-j2.52
1840	3.49-j12.55	19.8	56.5	43.88	24.4	10.06-j5.03	21.9	65.9	42.30	17.0	21.34+j0.21
1880	3.73-j13.55	20.02	58.6	43.90	24.5	10.59-j5.72	21.6	65.5	42.30	17.0	17.49+j2.36

Peak Side Load Pull Performance – Pulsed CW signal: 16  $\mu\text{s}$ , 10% duty cycle, 28 V,  $I_{DQ} = 250 \text{ mA}$

Freq [MHz]	$Z_s$ [ $\Omega$ ]	$P_{1dB}$									
		Max Output Power					Max PAE				
		$Z_l$ [ $\Omega$ ]	Gain [dB]	$P_{OUT}$ [dBm]	$P_{OUT}$ [W]	PAE [%]	$Z_l$ [ $\Omega$ ]	Gain [dB]	$P_{OUT}$ [dBm]	$P_{OUT}$ [W]	PAE [%]
1805	1.39-j5.07	19.3	54.8	47.4	55.2	3.64-j4.48	21.5	63.5	45.85	38.5	7.27-j2.64
1840	1.52-j5.1	19.5	53.4	47.3	53.2	3.49-j4.3	21.9	62.9	45.54	35.8	7.32-j2.2
1880	1.69-j5.34	19.7	53.6	47.2	52.8	3.44-j4.6	22.1	63.1	45.36	34.4	6.51-j1.49

Reference Circuit, 1805 – 1880 MHz



Reference circuit assembly diagram (not to scale)

## Reference Circuit (cont.)

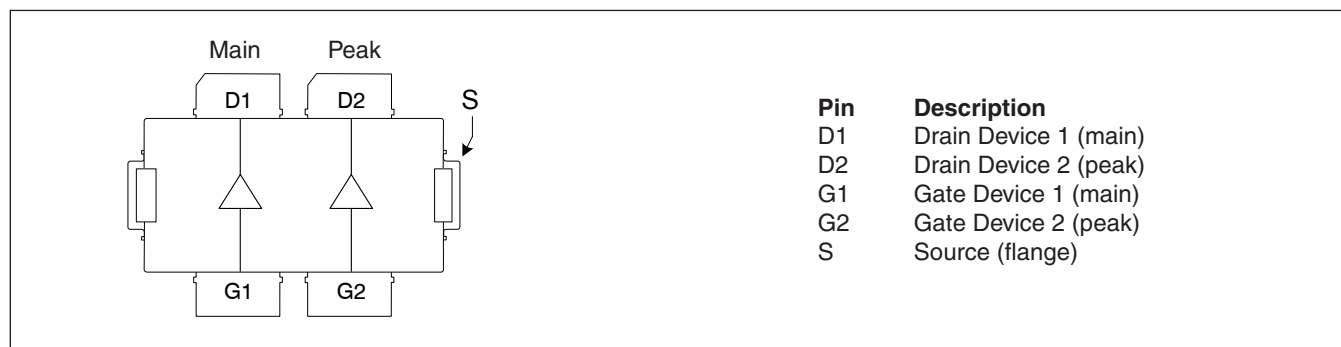
### Reference Circuit Assembly

DUT	PXAC210552ND V1
Test Fixture Part No.	LTA/PXAC210552ND V1
PCB	Rogers 4350, 0.508 mm [0.020"] thick, 2 oz. copper, $\epsilon_r = 3.66$ , $f = 1805 - 1880$ MHz
Find Gerber files for this test fixture on the Infineon Web site at <a href="http://www.infineon.com/rfpower">http://www.infineon.com/rfpower</a>	

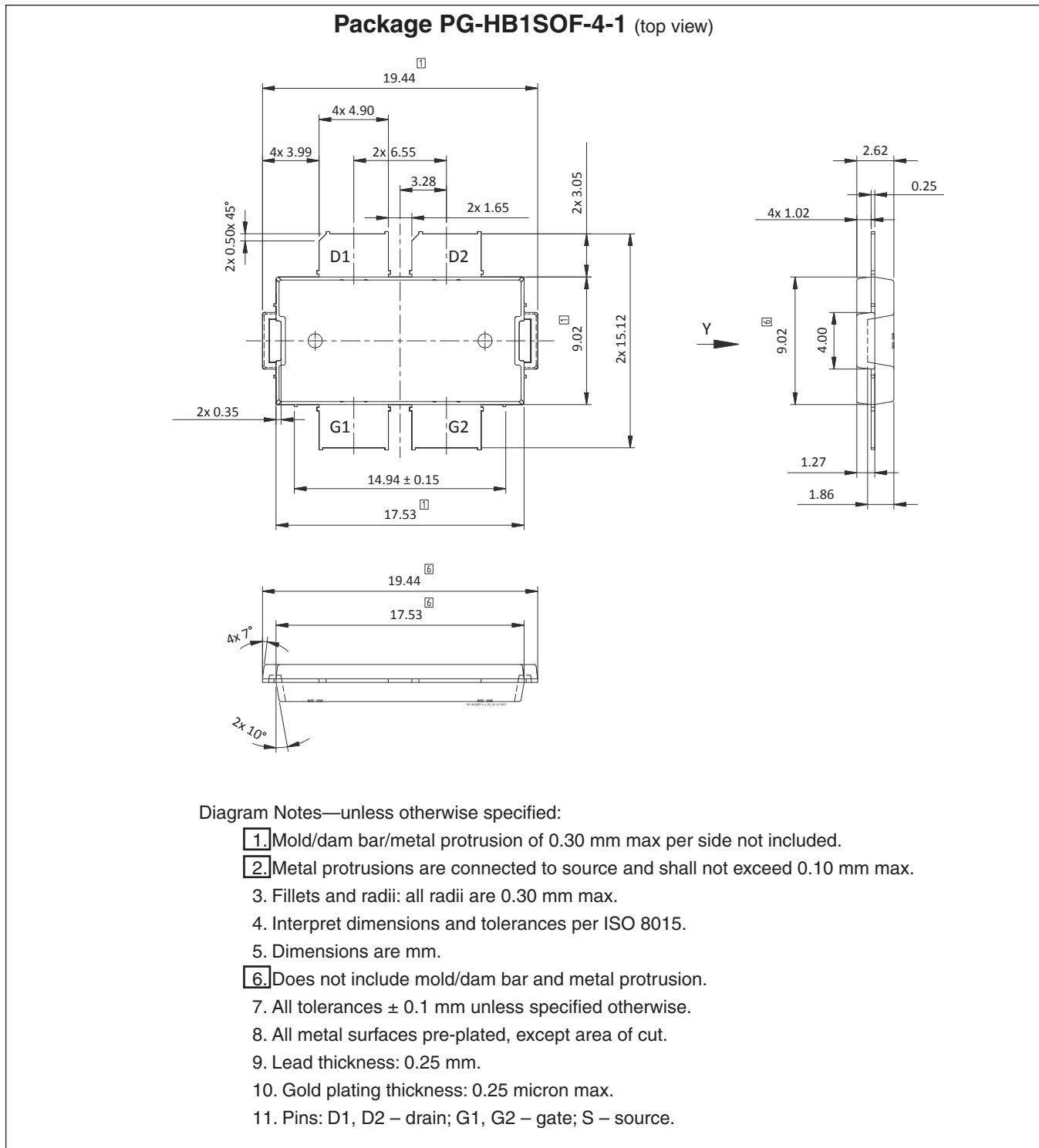
### Components Information

Component	Description	Manufacturer	P/N
<b>Input</b>			
C101	Capacitor, 12 pF	ATC	ATC600F120GW250T
C102, C110,	Capacitor, 10 $\mu$ F	Taiyo Yuden	UMK325C7106MM-T
C103, C108, C109,	Capacitor, 20 pF	ATC	ATC600F200JW250T
C104	Capacitor, 0.4 pF	ATC	ATC600F0R4CW250T
C105	Capacitor, 0.2 pF	ATC	ATC600F0R2CW250T
C106, C107	Capacitor, 1.2 pF	ATC	ATC600F1R2CW250T
R101, R102	Resistor, 10 ohms	Panasonic Electronic Components	ERJ-8GEYJ100V
R103	Resistor, 50 ohms	Richardson	C16A50Z4
U1	Hybrid Coupler	Anaren	X3C19P1-03S
<b>Output</b>			
C202, C203, C209, C210	Capacitor, 12 pF	ATC	ATC600F120GW250T
C201, C208	Capacitor, 20 pF	ATC	ATC600F200JW250T
C204, C207	Capacitor, 0.8 pF	ATC	ATC600F0R8CW250T
C205	Capacitor, 15 pF	ATC	ATC600F150JW250T
C206	Capacitor, 10 pF	ATC	ATC600F100JW250T

### Pinout Diagram (top view)



## Package Outline Specifications



Find the latest and most complete information about products and packaging at the Infineon Internet page  
<http://www.infineon.com/rfpower>





## Revision History

Revision	Date	Data Sheet Type	Page	Subjects (major changes since last revision)
01	2016-05-18	Advance	All	Data Sheet reflects advance specification for product development
02	2016-06-16	Advance	3, 4	Updated package outline diagram notes #6
03	2016-06-30	Production	All	Data Sheet reflects released product specification
04	2016-12-12	Production	7, 8	Updated package outline
04.1	2017-01-09	Production	7, 8	Revised typo in package outline

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