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PSoC[®] Creator[™] to ModusToolbox[®]

Porting Guide

Document Number: 002-25408 Rev *B

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1. Introduction



Overview

Porting a project from PSoC Creator to ModusToolbox is a moderately tedious task and this guide aims to make the process a bit easier. That being said the document *does not cover all the corner cases*. This document is a guide to the porting process and points you towards the right documentation based on your project's needs.

ModusToolbox provides a plethora of features that support our devices' capabilities. Connectivity is one such example. It is also highly customizable and configurable to suit your requirements. Your code can now be IDE independent and device agnostic! Porting your PSoC Creator project to ModusToolbox might open up a whole new world of opportunities and possibilities.

If you have any application specific queries or you run into a problem porting your application, ask a question in the <u>Cypress</u> <u>Developer Community</u>. We constantly strive to make ModusToolbox better to enhance the overall user experience. Your feedback is both welcome and appreciated.

Before You Begin

This guide expects that you have read the Eclipse IDE for ModusToolbox Quick Start Guide. If not, please do that first.

ModusToolbox is a different product than PSoC Creator. Cypress has taken great care to ensure that it is ready to develop production-quality products. However, ModusToolbox does not yet support all the Components and configuration options that are available in PSoC Creator. As a result, there are PSoC Creator-based designs that cannot be migrated to ModusToolbox 2.1. If you discover that your design cannot be reasonably ported to ModusToolbox, Cypress recommends that you continue to develop with PSoC Creator, which remains a fully supported development tool.

This guide covers only those Components that can be reasonably ported to ModusToolbox. If a Component is not listed in this guide, it likely means it is implemented differently in ModusToolbox. For example, ModusToolbox 2.1 either does **not** support the following, or uses a very different approach:

- UDB-based content. Here are some examples of PSoC Creator Components that do not have an alternative implementation in ModusToolbox:
 - Digital Logic Components
 - Digital Register Components
 - Digital Utility Components
- DSI routing. Digital signals cannot be routed through the DSI, which reduces the on-chip connectivity options available. This is generally presented as using a non-preferred connection (yellow) in PSoC Creator.
- Analog multiplexing. There is no analog MUX implementation in ModusToolbox, and all connectivity choices are set up in startup code but remain static thereafter. The only way to modify connectivity at run-time is through register writes to control AMXUXBUS switches.
- CapSense. CapSense in ModusToolbox is a middleware library. It is enabled by default for build support packages (BSPs) that support CapSense. This means that you cannot directly port a CapSense design from PSoC Creator. Instead, you re-implement your CapSense solution using the CapSense middleware APIs. The CapSense configuration settings however can be replicated. See <u>CapSense</u>.



Component APIs. In PSoC Creator, you could either use Component APIs or the PDL (and in some cases mix the two). ModusToolbox does not support any Component APIs, which means you must convert those calls to PDL APIs, or you will need to copy the PSoC Creator generated code.

If your PSoC Creator design makes use of these features, and a firmware-based alternative implementation is not available, then ModusToolbox may not be able to re-create the same functionality enabled by PSoC Creator. Please send your migration questions to the <u>Cypress Developer Community</u>. Cypress wants to hear about your issues, advise where possible, and prioritize features for future releases of ModusToolbox.

Terminology

PSoC Creator uses the term Components for the various peripherals in a design. ModusToolbox uses the terms peripherals and resources.

In PSoC Creator, you create projects in a workspace; oftentimes referred to as a design. In ModusToolbox, you create applications in a workspace. Applications consist of one of or more related projects.

The IDE that is bundled with the ModusToolbox installer is called the Eclipse IDE for ModusToolbox. ModusToolbox is an IDEindependent set of tools that you can use with the IDE that you prefer. It does not require the Eclipse IDE for ModusToolbox. However, this document assumes you are using the Eclipse IDE for ModusToolbox.

Expectations

It will likely take an advanced PSoC Creator user a day or two to port a moderately complex design that uses the PDL to the ModusToolbox environment. Moderate in this case is defined as a design that uses several Components, with about 500 lines of application code. This time requirement should include porting and debugging the application.

In general, PSoC Creator does many things automatically that you need to do manually in ModusToolbox. Some of these are common items and they are addressed in the common porting section. Other items are Component-specific, and they are addressed in the appropriate section for that Component.

Revision History

Document Title: PSoC® Creator™ to ModusToolbox [®] Porting Guide Document Number: 002-25408								
Revision	Revision Date Description of Change							
**	1/30/19	New document.						
*A 4/1/19 Updated for ModusToolbox 1.1								
*B 6/10/20 Updated for ModusToolbox 2.1								





Create New ModusToolbox Application

Open the Eclipse IDE for ModusToolbox, select your workspace, and create a new application using the Project Creator tool. Refer to the Eclipse IDE for ModusToolbox Quick Start Guide for details about the IDE, and refer to the ModusToolbox Project Creator Guide for details about the Project Creator tool.

When creating the new application:

- Select the BSP for your device. If you are using a custom board, select the BSP that is closest to your device. Refer to the "Creating a BSP for Your Board" section in the <u>ModusToolbox User Guide</u>.
- Select the application that you want to start with. If you want an empty project, you can select the Empty PSoC6 App. You can also rename your application. Once this is done, click Create.

A Quick Tour of a ModusToolbox Application

Once you create the application, it is imported into the IDE. Use the Project Explorer to view and open various application files and directories. The following image highlights several important files and directories:



- 1. This is the application directory that contains all the source code and other files required to successfully build your application. You can have more than one application in a workspace.
- 2. The **build** directory contains the build artifacts generated after the application is built. The build artifacts for each target are put into separate subdirectories.
- 3. The **deps** directory contains the *.lib* files for your application. The build system will use these files to include and update BSPs and libraries needed for your application.
- 4. The **libs** directory stores the imported BSPs and libraries. See <u>BSP Directory</u> later in this section.



- 5. Your main code is in the *main.c* file. This has some default calls already filled in, such as initializing the BSP which in turn configures the pins and clocks based on the generated code.
- 6. The project makefile consists of all the build configuration settings for your project. For more details, refer to the "ModusToolbox Build System" section in the <u>ModusToolbox User Guide</u>. You can also refer to the <u>Managing the Makefile for</u> <u>ModusToolbox v2.x</u> Knowledge Based Article.

BSP Directory

Inside the **libs** directory, there is at least one BSP subdirectory that begins with "TARGET_". This subdirectory contains all the necessary files to support the kit and devices. It also contains the *design.modus* file and the Generated Source files in *COMPONENT_BSP_DESIGN_MODUS*, as shown in the following image:



The design.modus file is where the Device Configurator stores all the device configuration information for the selected BSP.



Device Configurator

The following image shows the Device Configurator, where you enable and configure peripherals, pins, clocks, etc.

C:/Users/CKF/mtw2.1/1266/4-21-20/Hello_World/libs/TARGET_CY8CKIT-062-WIFI-BT/CC	OMPONENT_BSP_DESIGN_MODUS/d	esign.modus - Device Configurato	r 2.1 —		×
<u>File Edit View H</u> elp					
🛯 🗀 📇 🌇 🍋					
CY8C6247BZI-D54 CYW4343WKUBG	CSD (CapSense, etc.) 0 (CYBSP_CSI	D) - Parameters			o x
Peripherals Pins Analog-Routing System Peripheral-Clocks DMA	Enter filter text			20	⊟ Œ
Enter filter text 🖉 🖻 🖽 🛝	Name	Value			*
Resource Name(s) Personality	Peripheral Documentation Onfiguration Help	Open CSD Documentation			
Analog	 Inputs 				
Digital	? Clock	8 bit Divider 3 clk (CYBSP_C	SD_CLK_DIV) [USED]		-
▼ System	▼ CapSense				
✓ CSD (CapSense, etc.) 0 CYBSP_CSD CSD-2.0 ▼	(?) Enable CapSense	✓			
LCD Direct Drive 0 Icd_0_drive_0	(?) Target CPU core	Cortex M4			· ·
Multi-Counter Watchdog Timer (MCWDT) 0 srss_0_mcwdt_0	External Tools				
Multi-Counter Watchdog Timer (MCWDT) 1 srss_0_mcwdt_1	(?) CapSense Configurato	r Launch CapSense Configurator			
Real Time Clock (RTC) Srss 0 rtc 0	⑦ CapSense Tuner	Launch CapSense Tuner			
	▼ CSDADC				
	CSDIDAC				-
	CSD (CapSense, etc.) 0 (CYBSP_CSI	0) - Parameters Code Preview			
Notice List					രജ
0 Errors 1 0 Warnings 🗐 0 Tasks 👔 6 Infos					
Fix Description			Location		
1 The personality 'FLL-1.0', instantiated at 'FLL', can be updated.			CY8C6247BZI-D54: FL	L	
The personality 'PLL-1.0', instantiated at 'PLL', can be updated.			CY8C6247BZI-D54: PL	L	
The WCO is enabled. Chip startup will be slower because clock configuration car	not continue until the WCO is ready	. See the device datasheet for WCC			-
Ready					

You can access the Device Configurator in the Tools section of Quick Panel in the Eclipse IDE for ModusToolbox. Refer to the Device Configurator Guide for more details.

Migrate Pin Layout

Open the Design-Wide Resources (DWR) Pin Editor in PSoC Creator and click on the **Port** heading to sort your pins by port/pin. Then, open the ModusToolbox Device Configurator and select the **Pins** tab. Organize your windows so you can see both at the same time.





- 1. Use the PSoC Creator list as a guide for which pins to enable in the Device Configurator.
- 2. After enabling a pin, edit the alias to match the PSoC Creator name. The names are case sensitive. There are two translations needed while aliasing a pin based on the PSoC Creator name.
 - □ If you see a '\' in the PSoC Creator name, ignore the pin for the alias.
 - □ If you see a ':' in the PSoC Creator name, replace it with an underscore ('_') in the alias.
- 3. Once you have all the pins enabled and aliased correctly, it is time to start configuring the pins.

Pins that start with a '\' are embedded in a Component. This means you will not be able to find their settings in your schematic. Ignore those for now, once they are connected to their Components, the design rule checks will help you set up those pins.

- 4. In PSoC Creator, double-click on the name of the first pin. It will take you to the Configure Pins dialog. In this case, the pin is set to strong drive with an initial state of low and it is a digital out.
- 5. Change the settings in the Device Configurator as appropriate (in this case Strong Drive, input buffer off, with an initial drive state of 0).

PSoC Creator Configure Pins Dialog	Device Configurator Pins Parameters			
Configure 'LOAD_DIAG_EN' ? × Name: DAD_DIAG_EN Pins Builten Y 4 b Number of pins: 1 Display as bus 2 * * General Input Output Type Infield dive state: Display as bus 2 * * Max frequency: Infield dive state: Display divectoral One mode Display divectoral Infield dive state: Max frequency: Infield dive state: Infield dive state: Infield dive state: Display divectoral External terminal Display divectoral External terminal Datasheet OK	P6[4] - Parameters			

6. Go back to the PSoC Creator DWR Pin Editor and repeat the process with every pin.

3. System Configuration



There are various system settings in PSoC Creator that do not apply in ModusToolbox. For example, there is no UDB support in ModusToolbox. However, there are various ModusToolbox system settings available to configure your device.

System Clocks / Other Settings

Replicate your system clocks, debugging setup, and voltage from PSoC Creator in the Device Configurator **System** tab. This is straightforward and easy to do. The following image shows the **System** tab:



Analog Routing

PSoC Creator automatically routes and configures analog switches for all analog connections based on the schematic view and will auto assign resources like pins if not explicitly defined. ModusToolbox also automatically routes analog connections defined for each analog resource. There are two key areas to address when transitioning analog routing from PSoC Creator to ModusToolbox.

For static analog connections in ModusToolbox, choose the specific source or destination from each analog resource personality's Connection Parameters. When the design is built, the route will be configured all the way from the source to the destination. This includes source and destination analog resource switches, AMUXBUS switches, and connection to pins if required. The specific



register settings required to implement the routing can be seen in the *cycfg_connectivity.c/.h* files. If there is a routing resource conflict because two or more routes requires the same resource the user must deconflict the resource usage.

The analog routing can also be edited manually in ModusToolbox using the **Analog Route Editor** available in the Device Configurator. It also enables you to lock-down all or some of the resource routing. If in case any change that you make should encounter an error the routes are automatically rolled back to the previous state. You can refer to the Analog-Routing Tab section in the <u>Device Configurator Guide</u> for more information.

Dynamically changing analog connections in PSoC Creator are supported with Analog Mux Components. Analog Mux Components support multiple analog routes dynamically changeable at runtime with PSoC Creator generated function calls. ModusToolbox does not currently support analog multiplexers but user firmware can dynamically change analog routing switches to duplicate the functionality. Refer to the device TRM and analog driver documentation for detailed routing and switch control information. Analog resource switches are supported in their respective PDL drivers. AMUXBUS and GPIO analog switches are supported in the Cy_GPIO PDL driver.



Migrate Interrupts

There is no "interrupts" customizer available in ModusToolbox 2.1. All the interrupts used in your PSoC Creator application must be configured through code in ModusToolbox. Please follow these guidelines for porting interrupts.

Interrupts Internal to Component Code (BLE, CapSense, SCB, etc.)

Refer to the respective Component-specific migration section. Porting involves creating the interrupt structures, proxy interrupt handler, and initializing the interrupt as part of main code. The proxy interrupt handler should call the peripheral driver's interrupt handler as per the guidelines recommended in the Component specific migration section.

For example, an interrupt handler for I2C SCB calls the SCB driver's interrupt handler:

```
void I2C_Interrupt(void)
{
    Cy_SCB_I2C_Interrupt(I2C_HW, &I2C_context);
}
```

Interrupts External to Component Code (GPIO, MCWDT, etc.)

1. Create the interrupt structure in the source files where you initialize the interrupt.

Note The interrupt structure generated by the PSoC Creator code can be copied from the *Generated_Source/PSoC6/Pins* and *Interrupts/cyfitter_sysint_cfg.c* file as well.

- 2. Use this structure to initialize the interrupt along with the interrupt handler. See the following table for an example (MCWDT_STRUCT0 interrupt)
- 3. For the configuration of the interrupt source, refer to the Component migration section.



PSoC Creator	ModusToolbox 2.1
<pre>#include "cyfitter_sysint_cfg.h"</pre>	<pre>#include "cy_pdl.h"</pre>
<pre>#include "mcwdt/cy_mcwdt.h"</pre>	
<pre>#include "cy_device_headers.h"</pre>	/* MCWDT_isr */
woid MCWDT Interrupt Handler (woid)	<pre>const cy_stc_sysint_t MCWDT_isr_cfg = {</pre>
{	specific (cy8c6xxxxxx_xxxx.h) header file */
/* Clear the MCWDT peripheral interrupt */	.intrSrc = (IRQn_Type) srss_interrupt_mcwdt_0_IRQn,
<pre>/* Clear the CM4 NVIC pending interrupt for MCWDT */ NVIC_ClearPendingIRQ(MCWDT_isr_cfg.intrSrc);</pre>	<pre>.intrPriority = 7u };</pre>
/* Interrupt processing */	void MCWDT_Interrupt_Handler(void)
}	{ /* Clear the MCWDT peripheral interrupt */
void MCWDT Interrupt Init(void)	
{	/* Clear the CM4 NVIC pending interrupt for MCWDT
/* Configure ISR connected to MCWDT interrupt signal*/	<pre>*/ NVIC_ClearPendingIRQ(MCWDT_isr_cfg.intrSrc);</pre>
/* MCWDT_isr_cfg structure is defined by the SYSINT PDL component based on	/* Interrupt processing */
parameters entered in the customizer. */	}
Cv SvsInt Init(&MCWDT isr cfg,	
&MCWDT Interrupt Handler);	void MCWDT Interrupt Init(void)
/* Clear CM4 NVIC pending interrupt for MCWDT */	
<pre>NVIC_ClearPendingIRQ(MCWDT_isr_cfg.intrSrc);</pre>	Cy SysInt Init(&MCWDT isr cfg,
/* Enable CM4 NVIC MCWDT interrupt */	&MCWDT_Interrupt_Handler);
<pre>NVIC_EnableIRQ(MCWDT_isr_cfg.intrSrc);</pre>	/* Clear CM4 NVIC pending interrupt for MCWDT */
}	<pre>NVIC_ClearPendingIRQ(MCWDT_isr_cfg.intrSrc);</pre>
	/* Enable CM4 NVIC MCWDT interrupt */
	<pre>NVIC_EnableIRQ(MCWDT_isr_cfg.intrSrc);</pre>
	}

Deprecated Functions

Note that some of the functions used as part of sysint PDL driver (v1.10 or older) have been deprecated and replaced with new functions in the sysint v1.20 (or later). Code that uses the deprecated functions will still build and function. The deprecated functions have been supplied as macros that call their new counterparts. It is recommended that you update your code to use the new functions.

Deprecated functions (SysInt v1.10 or older)	New functions (SysInt v1.20 or later)			
Cy_SysInt_GetState	N/A - Invokes call to NVIC_GetEnableIRQ			
Cy_SysInt_SetIntSource	Cy_SysInt_SetInterruptSource			
Cy_SysInt_GetIntSource	Cy_SysInt_GetInterruptSource			
Cy_SysInt_SetIntSourceNMI	Cy_SysInt_SetNmiSource			
Cy_SysInt_GetIntSourceNMI	Cy_SysInt_GetNmiSource			

4. Porting Components



This chapter covers various PSoC Creator Components that can be ported to ModusToolbox, as well as common Component settings. If a Component is not contained in this chapter, your PSoC Creator design cannot be completely ported. This chapter covers the following:

- Common Component Settings
- Voltage DAC (12-bit)
- Scanning SAR ADC
- Low-Power Comparator
- Analog Reference (AREF)
- Programmable Analog
- I2S
- PDM-PCM
- <u>SCB</u>
- SMIF (QSPI)
- TCPWM
- MCWDT
- RTC
- <u>BLE</u>
- Emulated EEPROM
- DFU
- <u>USB</u>
- CapSense



Common Component Settings

Enable Component Clocks

Typically, just pick an unused clock in the Device Configurator. The correct clock rate should be set automatically the first time it is enabled. If you make changes to a peripheral, you may need to update the clock settings. In some cases, a warning will be generated if you use an 8-bit clock when you need a 32-bit clock to achieve the required bit rate. In those cases, change the clock used for the hardware block.

Assign Pins

The Device Configurator has parameters for various connections. In some cases, you'll have check boxes for both input and output connections on a pin. You only need to select one input. When you do, a new notice may be added telling you how you need to configure the pin. Resolve these errors as needed.

Resolve Configurator Errors, Warnings and Tasks

You can save the file, but code is not generated until you resolve all errors. You should also resolve any warnings/tasks in the notice list of the Device Configurator. The resulting code is generated automatically.

Aliases

Just like pins, set up the alias for your peripherals so that the names match your PSoC Creator Components.



Voltage DAC (12-bit)

Follow these steps to transition the PSoC Creator Voltage DAC (12-bit) to ModusToolbox:

1. Enable the 12-bit Continuous Time DAC in the ModusToolbox Device Configurator.



2. Transition the PSoC Creator Component parameters to the ModusToolbox 12-bit Continuous Time DAC parameters as follows:

C Creator			ModusToolbox Device Configurator					
	VDAC_1			12-bit Continuous Time DAC - Para	ameters	₽ ×		
	VDACTZ			Enter filter text				
Pin DAC Out			Name	Value				
				Peripheral Documentation				
Clock 1				⑦ Configuration Help	Open CTDAC Documentation			
1 M	AHz			▲ General				
Configure BIDAC 11		2 2		⑦ Vref Source	Vdda	•		
Configure VDAC_I				⑦ Output Buffer	Unbuffered to pin	•		
Basic Built-in		4 Þ		⑦ Format	12-bit unsigned	-		
Vref Source	Vdda 🔽 1	(x)		Initial Code	0			
Output Buffer	Unbuffered to pin 🔹 1	8		① Update Mode	Buffered write	-		
DAC Mode	12-bit two's-complement • f	×		Enable Deep Sleep Ope	ration			
Initial Code	0 1	<u>x</u>		Constanting				
Update Mode	Buffered write • 1	×		Connections				
Show Trigger Output Termin	al 🚺	×		E Clock	<unassigned></unassigned>	•		
Enable Deep Sleep Operation	n 🗌 /	×		⑦ Clock Frequency	🖰 0 kHz			
Number of Opamps Used	Vief = 3.3000 V	Range emression:		⑦ DAC Output	<unassigned></unassigned>			
Initial Code = 0, Vout = 1.6500 V		Code: Vout (V): -2048 0		? Trigger Output	<unassigned></unassigned>			
		0 1.6500		Advanced	1			
-2048	0 2047	2047 3.2882		Output Mode	Output the code value	-		
Datasheet	OK	Apply Cancel		③ Store Config in Flash				

a. The Vref Source value [Analog reference] requires two parameter changes in the 12-bit Continuous Time DAC as well as configuration of CTBm[0] OpAmp 1 to route and buffer the internal reference.

First set Vref Source to External and then select Reference Source as CTBm[0] OpAmp 1 out_1x. Enable CTBm[0] OpAMp 1 and set Personality to OpAmp-[version].

Let all parameters be default with the exception of the following changes:

- □ Set Vplus Input to AREF vref,
- □ Vminus Input to CTBm[0] OpAmp 1 out_1x,
- □ Output (internal only) to 12-bit Continuous Time DAC ctdrefdrive.
- b. The **Output Buffer** values [**Buffered to pin**, **Buffered internal**] convert to **Output Buffer**[**Buffered**]. The differences between **Buffered to pin** and **Buffered internal** are handled in the DAC output parameter based on where the output is routed.
- c. DAC Mode has been renamed to Format.



d. Sample and Hold (if visible)

- e. Initial Code
- f. The Update Mode values [Strobe edge sync, Strobe edge immediate, Strobe level] are not supported as they require DSI routing to connect to the strobe source. ModusToolbox does not currently support DSI routing. One workaround for a fixed frequency strobe is to set Update Mode to Buffered write and select a clock connection source configured for the required strobe rate.
- g. Show Trigger Output Terminal is not transferred because it only controls wire terminal visibility in PSoC Creators schematic view.
- h. Enable Deep Sleep Operation
- 3. PSoC Creator automatically routes the output using schematic entry. In ModusToolbox, the output is routed using **Connections** parameters. From the **DAC Output** drop down connection list, select the direct pin CTBm OpAmp input connections (green circles) or another connection routed through other resources (yellow circles).



If the **Output Buffer** parameter is set to **Buffered**, **CTBm[0] OpAmp 0 Vplus** must be selected as the output destination. The dedicated output pin is device specific and can be referenced in the device datasheet.

4. The trigger output in PSoC Creator is automatically routed using schematic entry. In ModusToolbox, all connections other than interrupts are selected from the Trigger Output parameter drop-down. Interrupt connections are fixed and already made to the CPU interrupt controller. See the <u>Interrupts section</u> for details on transitioning the interrupt, if present.



Scanning SAR ADC

Follow these steps to transition the PSoC Creator Scanning SAR ADC to ModusToolbox:

1. Enable the 12-bit SAR ADC in the ModusToolbox Device Configurator:



2. Transition the PSoC Creator **Config0** tab Component parameters to the ModusToolbox 12-bit SAR ADC parameters as follows:



- a. Vref Select
- b. Number of Channels
- c. Vref Bypass
- d. The Vneg for Single-Ended Channels (Vneg for S/E in PSoC Creator) parameter directly transfers values Vssa and Vref to ModusToolbox. The PSoC Creator External option for Vneg for S/E converts to External P1/P3/P5/P7 options for Vneg for Single-Ended Channels parameter in ModusToolbox depending on the specific pin chosen for your design.

PSoC Creator determines the specific pin automatically based on the schematic view. Refer to the Pin Editor in PSoC Creator to determine the I/O pin used.

- e. PSoC Creator **Free-run scan rate (SPS)** converts to ModusToolbox **Target Scan Rate (sps)**. PSoC Creator automatically selects and configures a clock source to generate the scan rate. In ModusToolbox you must select a Clock Connection and configure its source and divider to generate the frequency required for the scan rate. See the <u>SAR PDL</u> <u>documentation</u> for details on determining the correct clock frequency.
- f. The ModusToolbox parameter Hardware Trigger Mode, which is enabled once the SOC Enable parameter is checked, is derived from the PSoC Creator parameter Sample Mode located on the Common tab. If Sample Mode = Continuous then Hardware Trigger Mode = Level sensitive. If Sample Mode = Single Shot then Hardware Trigger Mode = Edge sensitive.
- g. Differential Result Format
- h. Single-Ended Result Format
- i. Samples Averaged
- j. Averaging Mode
- k. Compare Mode
- I. Low Threshold
- m. High Threshold
- 3. For each ADC input channel, the following parameters are transferred from PSoC Creator to ModusToolbox:
 - □ Input mode -> Input Mode
 - □ Avg -> Averaging
 - □ Limit Interrupt -> Range Interrupt Enable
 - □ Sat. interrupt -> Saturation Interrupt Enable
 - □ Minimum acq. Time (ns) -> Minimum Acquisition Time (ns)

The **En** check box in PSoC Creator is not supported in ModusToolbox as all channels are automatically enabled. Dynamic control of channel enables can be performed using PDL driver supplied APIs.

- 4. Transition the PSoC Creator **Common** tab Component parameters.
 - a. The **Show analog clock (aclk) terminal** check box does not transfer to ModusToolbox because the analog clock must always be manually configured.
 - b. The Parameter **Number of configs** is not supported in the ModusToolbox version of the SAR ADC. If more than one configuration is required, they must be configured in firmware. Multiple configurations are created by manually generating multiple PDL initialization structures as detailed in the PDL driver library documentation.
 - c. The Parameter **Sample Mode** is not in the ModusToolbox parameters list. This setting has been moved to an argument passed when calling the ADC start function provided in the PDL library.
 - d. The PSoC Creator **Use soc terminal** parameter converts to ModusToolbox **SOC Enable**. The **SOC Input** parameter can then select the source of the SOC signal.



 PSoC Creator automatically routes the output using schematic entry. In ModusToolbox the output is routed using Connections Parameters. The Ch[n] Vplus, and Ch[n] Vminus (if Input Mode is Differential) Parameters in ModusToolbox must select the desired analog pin connection for the channel. The dedicated input pins are device specific and can be referenced in the device datasheet.

	🔲 Ch0 Vplus	<unassigned></unassigned>				
•	Channel 1	O P10[0] analog				
	Input Mode	P10[1] analog				
	? Averaging	D10[2] applog				
	⑦ Range Interrupt Enable					
	③ Saturation Interrupt Enable	P10[3] analog				
	⑦ Minimum Acquisition Time (ns)	P10[4] analog				

- 6. The **eos** output in PSoC Creator is automatically routed using schematic entry. In ModusToolbox all connections other than interrupts are selected from the **EOS Trigger Output** parameter dropdown. Interrupt connections are fixed and already made to the CPU interrupt controller. Please see the Interrupts section for details on transitioning the interrupt if present.
- 7. The PSoC Creator **sdone** signal is not supported as it requires DSI routing to connect to the sdone source. ModusToolbox does not currently support DSI routing.



Low-Power Comparator

Follow these steps to transition the PSoC Creator Low Power Comparator to ModusToolbox:

1. Enable the Low-Power Comparator 0/1 in the ModusToolbox Device Configurator as follows:

Resource					
▼ An	alog				
	✓ Low-Power Comparator 0				
	Low-Power Comparator 1				
*	Programmable Analog				
	12-bit Continuous Time DAC 0				
	12-bit SAR ADC				
	AREF				
	CTBm[0] OpAmp 0				
	CTBm[0] OpAmp 1				

2. Transition the PSoC Creator Component parameters to the ModusToolbox Low-Power Comparator Parameters as follows:

PSoC Creator					ModusToolbox Device Configurator					
	LPComp) 1			Low-F	Power Comparator 0 - Parameters		8	×]
					Enter f	îlter text	<u> </u>	E	•	
Pin_LPCMP_P			-	SysInt_LPCMP	Name	2	Value			
					⊿ Pe	eripheral Documentation				
						⑦ Configuration Help	Open LPComp Documentation			
		-		9)	In a Ge	eneral				
Contigure 'LPComp_1'						? Hysteresis	\checkmark			
Name: LPComp_1 General Buit-in				4 Þ		⑦ Output Configuration	Direct		•	
Hysteresis	Enable	•	f(x)			Power/Speed	Low Power/Low		•	
Output Configuration	Direct	•	f(x)			Pulse/Interrupt Configuration	Rising Edge		•	1
Power/Speed	Low Power/Low	•	f(x)			Ocal VREF input		_		1
Local VREF input	Kising edge		f(x)		⊿ Co	onnections				
Vidda						? Positive Input (inp)	<unassigned></unassigned>			
V. Down						? Negative Input (inn)	<unassigned></unassigned>			
						⑦ Compare Output (dsi_comp)	<unassigned></unassigned>			
					⊿ Ac	dvanced				
Datasheet					Store Config in Flash	v				
OK Apply Cancel										

- a. Hysteresis
- b. Output Configuration
- c. Power/Speed
- d. Pulse/Interrupt Configuration
- e. Local VREF input



 PSoC Creator automatically routes the inputs using schematic entry. In ModusToolbox the Positive Input and Negative Inputs are routed using Connections Parameters. From the Positive or Negative Input drop-down connection list, select the direct pin connections (green circles) or another connection routed through AMUXBUSA or AMUXBUSB (yellow circles). Input pins are device specific and can be referenced in the device datasheet.

Select signal(s) - Device Configurator
Select any signal(s) to connect to 'Positive Input (inp)'.
P5[6] analog
🔲 🔾 12-bit Continuous Time DAC ctdrefdrive
🔲 🔾 12-bit Continuous Time DAC ctdvout
12-bit SAR ADC vminus
12-bit SAR ADC vplus
C AREF vbgr
CSD (CapSense, etc.) amuxbus_a
CSD (CapSense, etc.) amuxbus_b
OK Cancel

4. The comparator digital output in PSoC Creator is automatically routed using schematic entry. In ModusToolbox all connections other than interrupts are selected from the Compare Output (dsi_comp) parameter dropdown. Interrupt connections are fixed and already made to the CPU interrupt controller. Please see the Interrupts section for details on transitioning the interrupt if present.



Analog Reference (AREF)

Follow these steps to transition the PSoC Creator Programable Analog settings to ModusToolbox:

1. All designs that use any analog resource must enable the Analog Reference resource.



2. In a PSoC Creator design, the analog reference settings are in the Design-Wide Resources (DWR) **System** tab, in the **Analog Reference** section. The PSoC Creator **Bandgap Value** transitions to ModusToolbox **Voltage Reference Source**.

Current Reference Source, **Deep Sleep Mode**, and **Voltage Reference** ModusToolbox parameters are not provided in PSoC Creator designs as they default to the values shown in ModusToolbox. These settings should typically remain in their default state.

PSoC Creator		ModusToolbox Device Configu	rator
Design01.cydwr	- 4 Þ ×	AREF - Parameters	5 ×
Collapse Expand □ Collapse		Enter filter text	
Option	Value		
Analog Reference		Name	Value
- Bandgap Value	Local (1.20 V)	Peripheral Documentation	
- Opamp Reference Current	1 μA 💌 🚍	⑦ Configuration Help	Open SysAnalog Documentation
Available in DeepSleep		General	
Input value indicates the input voltage on VDDA pin.	A	⑦ Voltage Reference Source L	_ocal (1.2 V)
🕼 Pins 🛝 Analog 📴 DMA 🕒 Clocks 💉 Interrupt	s 😼 System 📱 Directives 4 🕨	⑦ Current Reference Source L	Local
		⑦ Deep Sleep Mode	Disable
		Connections	
		Voltage Reference	<unassigned></unassigned>
		Advanced	
		③ Store Config in Flash	
		1	



Programmable Analog

Follow these steps to transition the PSoC Creator Programable Analog settings to ModusToolbox:

1. All designs that use any analog resource under Programmable Analog section must enable the Programmable Analog resource.

Resource
 Analog
Low-Power Comparator 0
Low-Power Comparator 1
🔻 ✔ Programmable Analog
12-bit Continuous Time DAC 0
12-bit SAR ADC
AREF
CTBm[0] OpAmp 0
CTBm[0] OpAmp 1

2. In a PSoC Creator design, the analog reference settings are in the DWR **System** tab, in the **Analog References** section. The PSoC Creator **Opamp Reference Current** transitions to ModusToolbox **Opamp Reference Current**. **Available in Deep Sleep** parameter transitions to **Deep Sleep Enable** in ModusToolbox Toolbox.

Opamp Pump Clock Source ModusToolbox parameter is not provided in PSoC Creator designs as it defaults to the value shown in ModusToolbox. This setting should typically remain in its default state.

PSoC Creator		ModusToolbox Device Configurat	or
Design01.cydwr	★ 4 ▷ ★	Programmable Analog - Parameters	ā ×
⊃ Reset be Expand ⊡ Collapse		Enter filter text	
Analog Reference	Value	Name	Value
Bandgap Value	Local (1.20 V)	Peripheral Documentation	
Opamp Reference Current	1 μA	Configuration Help	Open CTB Documentation
Available in DeepSleep		Global Opamp Settings	
Input value indicates the input voltage on VDDA pin.	A 7	⑦ Opamp Reference Current	1 uA 🔹
🧳 Pins 🛝 Analog 📴 DMA 🕒 Clocks 💉 Interrupt	ts 🐶 System 🖺 Directives 4 🕨	Opamp Pump Clock Source	SRSS 👻
		⑦ Opamp Pump Clock Frequency	🖰 100 MHz
		▲ CTB0	
		⑦ Deep Sleep Enable	
		1	



I2S

Replicate the settings as appropriate.

PSo	oC Creator						1	Modu	IsToolbox Device (Configurator	
Cont	figure 'I2S_PDL_v2_0)'				?	×	Inter-IC	Sound Bus (I2S) 0 - Parameters		ØX
Mag	120						_	Enter filt	ter text		2 0 🗉 🕀
INGI								Name		Value	
	Basic Built-in					4		▼ Peri	pheral Documentation		
	Clock from terminal	Input clock free	quency (kH	z): Unknown					Configuration Help	Open I2S Documentation	
Cle	ock divider: 16 🖨							▼ Tim	ing		
6	∠ TX			RX					⑦ Clock	P CLK_HF1 root_clk [USED]	•
1	Mode:	Master	\sim	Mode:	Master	\sim			② External Interface Clock	<unassigned></unassigned>	*
6	Bit rate (kbps):	Unknown		Bit rate (kbps):	Unknown				Input Clock Frequency (kHz)	₾ 100000.000	
1	Nignment:	I2S mode	\sim	Alignment:	I2S mode				? Clock Divider	16	
0	Channels:	2	\sim	Channels:	2	\sim			⑦ Bit Rate (kbps)	一 781.250	
0	Channel length:	16	\sim	Channel length:	16	\sim		▼ TX			
١	Word length:	16	~	Word length:	16	\sim			? Enable	V	
F	Frame rate (ksps):	Unknown		Frame rate (ksps):	Unknown				? Mode	Master	•
(Overhead value:	0	\sim	Sign extension:	0	\sim			② Alignment	I2S mode	*
1	WS pulse width:	1 channel length	~	WS pulse width:	1 channel length	\sim			? Channels	2	
1	SDO latching time:	Normal	~	SDI latching time:	Normal	\sim			⑦ Channel Length	16	•
(Output clock polarity:	Normal	~	Output clock polarity:	Normal				Word Length	16	•
F	FIFO trigger level:	0	÷	FIFO trigger level:	0	A			Frame Rate (ksps)	<u></u> 24.414	
[DMA trigger			DMA trigger					Overhead Value	0	•
1	nterrupts:			Interrupts:					WS Pulse Width	1 channel length	*
	Trigger			Trigger					③ SDO Latching Time	Normal	•
	Not full			Not empty					Input Serial Clock Polarity	🖱 Normal	
	Empty			Full					⑦ Output Serial Clock Polarity	Normal	•
				Underflow					③ FIFO Trigger Level	0	
	Watebdoa	CECEECE	*	Watchdog	CCCCCCCC	A			⑦ DMA Trigger		
	Waterluog.	rrrrrr	Ŧ	Waterloog.	rrrrrr	T			Watchdog Enable		
								▼ RX			
									⑦ Enable		
	Datasheet			ОК	Apply	Cancel		Out	puts		
								Adv	anceu		



PDM-PCM

Replicate the settings as appropriate.

PSoC Creator			ModusToolbox Device Co	nfigurator	
Configure 'PDM_PCM'		? ×	PDM-PCM Converter 0 - Parameters		ØX
Name: PDM_PCM			Enter filter text	4	20 🖻 🕀
Basic Built-in		4 ۵	Name	Value	
E Channels			Peripheral Documentation		
Channel Recording Swap		a	⑦ Configuration Help	Open PDM PCM Documentation	
Left Channel Gain			Channels		
Binkt Channel Gain			Channel Recording Swap Left Channel Coin		
Right Channel Gain	00b · //		2 Left Channel Gain 3 Diabt Channel Cain	Udb	
Stereo / Mono Mode Select	Stereo V IC	0	Right Channel Gain Starrage Manda Calast	VaB	· · · ·
E Filter		-	() Stereo / Mono Mode Select	Stereo	•
Disable High Pass Filter		0	Disable High Pass Filter		
High Pass Filter Gain	8 f(0	Disable High Pass Filter Disable Filter Coin		
 Interrupts 			() High Pass Filter Gain	0	
RX FIFO is Not Empty Interrupt	_ f0	0	Not Empty		
RX FIFO Overflow Interrupts	□ f0	0	② Overflow		
RX FIFO Trigger Interrupts	_ f(0	③ Trigger		
RX FIFO Underflow Interrupts	D f0	0	② Underflow		
 Output Data 			▼ Output Data		
Output Data Sign Extension	D f(0	⑦ Output Data Sign Extension		
Output Data Word Length, in Bits	24 × f(0	⑦ Output Data Word Length, in Bits	16	•
Output FIFO			 Output FIFO 		
DMA Trigger Enable	M f0	0	⑦ DMA Trigger Enable		
Output FIFO Trigger Level	0 f0	0	Output FIFO Trigger Level	0	
Soft Mute	-		 Soft Mute 		
Enable Soft Mute	□ f(0	② Enable Soft Mute		
Select Soft Muta Eine Gain	0.2648		③ Select Soft Mute Fine Gain	0.26dB	-
Sefect Soft Muter me Gam	0.2000 1 //		③ Soft Mute Cycles	96	-
Soft Mute Cycles	90 × 10	0	▼ Timing		
	1/4		(?) Clock	d CLK_HF1 root_clk [USED]	•
Ist Clock Divisor	1/4 1/4	g	③ 1st Clock Divisor	1/1	-
2nd Clock Divisor	1/1 ~ #0		? 2nd Clock Divisor	1/1	-
3rd Clock Divisor	3 f(0	3rd Clock Divisor	3	
Number of PDM_CLK Periods	0 f(0	⑦ Number of PDM_CLK Periods	0	
Sinc Decimation Rate	32 f(:	0	⑦ Sinc Decimation Rate	32	
			 Inputs 		
			? PDM Data	<unassigned></unassigned>	•
			Outputs		
Datasheet	ОК	Apply Cancel	Advanced		
			1		



SCB

Personalities

For the SCB block, there are several personalities available in the Device Configurator: EZI2C, I2C, SPI, and UART. When you enable an SCB block, a dialog displays to select the appropriate personality:

Device Configurator 2.1	×
'Serial Communication Block (SCB) 0' supports mu personalities. Select the one that should be enab here.	ltiple bled
EZI2C-1.0 I2C-2.0	
SPI-1.0 UART-1.0	
OK Cancel	

Once enabled, you can change the personality from the drop-down next to the SCB name.

Resource	Name(s)	Personality
Analog		
 Communication 		EZI2C-1.0
Inter-IC Sound Bus (I2S) 0	audioss_0_i2s_0	I2C-2.0
Quad Serial Memory Interface (QSPI) 0	smif_0	I2C-1.0
✔ 📋 Serial Communication Block (SCB) 0	scb_0	SPI-1.0
Serial Communication Block (SCB) 1	scb_1	UART-1.0

How Do I Choose the Correct SCB?

SCBs have fixed connectivity to specific pins. In PSoC Creator, the tool selects the SCB automatically based on pin selection. In ModusToolbox, you must select the correct SCB manually, based on your pins. To determine the correct SCB, find the pin and click on the **Digital InOut** parameter under Internal Connection in the parameters window.

_			
▼	Internal Connection		
	? Analog	<unassigned></unassigned>	
	⑦ Digital Input	<unassigned></unassigned>	
	⑦ Digital Output	<unassigned></unassigned>	•
	② Digital InOut	<unassigned></unassigned>	
•	Advanced	Serial Communication Block (SCB) 1 I2C.scl [ENABLED]	
	Store Config in Flash	Serial Communication Block (SCB) 1 SPI.mosi [ENABLED]	
		Serial Communication Block (SCB) 1 UART.rx [ENABLED]	

This shows you which SCB block(s) connect to this pin. Look at all the pins you've assigned and start with the most constrained pin. If that pin connects to only one SCB, it is obvious which one you should enable. If that pin connects to more than one SCB, you must create a list of the SCBs to which it connects and go to the next most constrained pin. Doing so, you should be able to reduce your list to a definitive list of SCBs that work for your design.

In PSoC Creator, connecting and configuring clocks was automatic. In ModusToolbox, you specify clock and configuration manually. Refer to the <u>Device Configurator Guide</u> for more details regarding peripheral clock settings.



EZI2C

Replicate the settings as appropriate.

PSoC Creator					I	Modus	Toolbox Device Configu	rato	or	
Configure 'EZI2C_1'			?	×		Serial C	ommunication Block (SCB) 0 - Pa	rame	ters 🗗	×
Name: EZI2C_1						Enter filt	er text		<u>/</u>	(F
Basic Pins Built-in				۹ ۵		Name		Valu	e	
Clock Source						I ⊿ Peri	pheral Documentation			
Enable Clock from Terminal		f(x)					Configuration Help	Ope	n EZI2C (SCB) Documentation	
General	1					⊿ Gen	eral			
Data Rate (kbps)	100	f(x)					🕐 Data Rate (kbps)	100		-
Number of Addresses	1 ~	f(x)				-	? Number of Addresses	1		-
Primary Slave Address (7-bit)	0x08	f(x)	Actual data rate (kbps): 400				Primary Slave Address (7-bit)	8		
Sub-Address Size	8 bits ~	f(x)	SCB clock (kHz): 12500 👔				Sub-Address Size	e hit		-
Enable Wakeup from Deep Sleep Mode		f(x)				A Cor	nactions	0.01		
						- COF				
						· ·		< un	assigned >	
							?) Clock Frequency	Ö		
							? SCL	8	P0[2] digital_inout [USED]	-
						-	💎 SDA	P	P0[3] digital_inout [USED]	•
Datasheet	ОК		Apply Cance	4		⊿ Adv	anced			
			Curico Curico				? Store Config in Flash	1		

I2C

Set the mode as needed to match PSoC Creator and replicate the settings as appropriate.

PSoC Creator		ModusToolbox Device Configurator				
Configure 'I2Cm1'	? ×	Serial Communication Block (SCB) 2 - Parameters				
Name: 12Cm1		Enter filter text	2 🖻 🕀			
Basic Pins Bullt-in	4 Þ	Name	Value			
Clock Source		Peripheral Documentation Configuration Help	Open I2C (SCB) Documentation			
Enable Clock from Terminal		✓ General				
		⑦ Mode	Slave 💌			
Mode Master V f(x)		⑦ Data Rate (kbps)	100			
Data Data (Idea)		Use TX FIFO				
		Accept Matching Address in RX FIFO				
	ctual data rate (kbps): 97 🕕	Use RX FIFO	V			
Use RX FIFO	CB clock (kHz): 1562.5	 Slave 				
Master tL	Low (us): 5120	③ Slave Address (7-bit)	8			
Enable Manual SCL Control	High (us): 5120	③ Slave Address Mask (8-bit)	254			
		⑦ Accept General Call Address				
		Connections				
		Clock	<unassigned></unassigned>			
		🗐 SCL	<unassigned></unassigned>			
		🗐 SDA	<unassigned></unassigned>			
		③ SCL Output (scl_trig)	<unassigned></unassigned>			
Datasheet OK	Apply Cancel	 Actual Data Rate 				
		Actual Data Rate (kbps)	<u></u> 100			
		⑦ Clock Frequency	<u> </u>			
		 Advanced 				
		③ Store Config in Flash				



SPI

Replicate the settings as appropriate.

PSoC Creator			ModusToolbox Device Cor	nfigurator
Configure 'SPIm1'		? X	Serial Communication Block (SCB)	0 - Parameters 🛛 🗗 🗙
Name: SPIm1			Enter filter text	<u>/</u> E E
Basic Advanced Pins Dulter	n	4.1	Name	Value
E Clock Source			 Peripheral Documentation 	
Enable Clock from Terminal	D 60	1	⑦ Configuration Help	Open SPI SCB Documentation
E General		1	▲ General	[
Mode	Master Y RA	1	(?) Mode	Slave -
Sub Mode	Motorola Y f0	1	<u>③</u> Sub Mode	Motorola 🔻
SCLK Mode	CPHA = 0, CPOL = 0	1	(?) SCLK Mode	CPHA = 0, CPOL = 0
Data Rate (kbps)	125 fb	1	(?) Data Rate (kbps)	1000
Oversample	16 /0	1	(?) Enable Input Glitch Filte	r 📃
Enable Input Glitch Filter	[] [] []	1	Data Configuration	
Enable MISO Late Sampling	[] [] []	1	Bit Order	MISB FIRST
SCLK Free Running	[] [/a	1	RX Data Width	8
E Data Configuration		1	(7) IX Data Width	8
Bit Order	MSB First V f0x	1	Slave Select	A still and some
RX Data Width	8 //	1	SSU Polarity SSU Polarity	Active Low
TX Data Width	8 10	,	C SSI Polarity	Active Low •
Slave Select			Connections	Active Low 👻
Deassert SS Between Data Elements	· 🗆 //	1		
Number of SS	0 f0	1		Conta in the second second
		Advalidate rate line & UNIZH	<u> </u>	PU[4] digital_inout [USED] ▼
		Actual data race (cops): Onen	IZOM (§)	<pre><unassigned></unassigned></pre>
SOLK			(?) MISO	<unassigned> •</unassigned>
MOSI D7 D6			022 (?)	<unassigned></unassigned>
M80			? SS1	<unassigned></unassigned>
			? SS2	<unassigned></unassigned>
			? RX Trigger Output	<unassigned></unassigned>
			⑦ TX Trigger Output	<unassigned></unassigned>
			Data Rate	
			Actual Data Rate (kbps)	A
			Clock Frequency	A
Detector 1		-	 Trigger Level 	
Latasheet	OK .	/opy Cancel	(?) RX FIFO Level	63
			⑦ TX FIFO Level	63
			▲ API Mode	[
			(?) API Mode	High Level -
			Advanced	
			Store Config in Flash	



UART

Replicate the settings as appropriate.

PSoC Creator Configure 'UART_Debug' ? \times UART_Debug Name: ۹ ۵ Basic Advanced Pins Built-in Clock Source Enable Clock from Terminal f(x) General Com Mode Standard ~ f(x) ~ *f(x)* TX/RX Mode TX + RX Actual baud rate (bps): 115741 (i) Baud Rate (bps) 115200 f(x) Oversample 12 f(x) \sim LSB First Bit Order f(x) ~ 8 bits f(x) Data Width \sim Parity None f(x) ~ 1 f(x) Stop Bits Enable Digital Filter f(x) ОК Datasheet Apply Cancel

odusToolbox Device Co	nfigurator	
erial Communication Block (SCB) 0 - Param	eters É	×
nter filter text		Ŧ
lame	Value	-
Peripheral Documentation		
⑦ Configuration Help	Open UART (SCB) Documentation	
6 General		
⑦ Com Mode	Standard	•
⑦ Baud Rate (bps)	115200	
⑦ Oversample	8	-
③ Bit Order	LSB First	-
⑦ Data Width	8 bits	-
? Parity	None	Ţ
(?) Stop Bits	1 bit	Ţ
(?) Enable Digital Filter		_
Support RS-485		
⑦ TX-Enable		
Flow Control		
② Enable Flow Control		
⑦ CTS Polarity	Active Low	•
(?) RTS Polarity	Active Low	•
(?) RTS Activation Level	63	
Connections		
🗐 Clock	<unassigned></unassigned>	•
? RX	<unassigned></unassigned>	-
? TX	<unassigned></unassigned>	-
⑦ RX Trigger Output	<unassigned></unassigned>	
⑦ TX Trigger Output	<unassigned></unassigned>	
Actual Baud Rate	1	
? Actual Baud Rate (bps)	8	
(?) Baud Rate Accuracy (%)	<u> </u>	
⑦ Clock Frequency	8	
Trigger Level		
RX FIFO Level	63	
⑦ TX FIFO Level	63	
Multi Processor Mode		
② Enable Multi Processor Mode		
? Address	0	





SMIF (QSPI)

Replicate the settings as appropriate. Refer also to the ModusToolbox QSPI Configurator Guide, as needed.

PSoC Creator			ModusToolbox Device	ModusToolbox Device Configurator						
Configure 'SMIE ELASH'		? X	Quad Serial Memory Interface (QSPI) 0 - P	arameters 🗗 🗙	c					
			Enter filter text	2 🗉 🗉	à l					
Name: SMIF_FLASH			Name	Value						
Basic Built-in		٩ ۵	 Peripheral Documentation (?) Configuration Help 	Open SMIF Documentation						
 DMA Trigger Outputs 			Clocks							
RX FIFO DMA Trigger	f(x)	(?) HF Clock	CLK_HF0 root_clk [USED]	<u>.</u>					
TX FIEO DMA Trigger			⑦ Interface Clock	CLK_HF2 root_clk [USED]	<u>.</u>					
		<u> </u>	(?) SPI Clock	P11[7] digital_inout [USED]						
GPIO Configuration		_	External tools							
SMIF Datalines [0:1]	✓ f(.	N	(7) QSPI Configurator	Launch QSPI Configurator	·]					
SMIF Datalines [2:3]	✓ f(.	e la	SPI Data[0]	<unassigned></unassigned>	1					
SMIF Datalines [4:5]	[] f(.	0	③ SPI Data[1]	<up>signed ></up>	7					
SMIF Datalines [6:7]	f (× I	() SPI Data[2]	<unassigned></unassigned>	÷					
SMIE SPI Slave Select 0			() SPI Data[3]	<unassigned></unassigned>	Ť					
SMIL SPI Slave Select 0		v	SPI Data[4]	<unassigned></unassigned>	Ť					
SMIF SPI Slave Select 1				(unassigned)	1					
SMIF SPI Slave Select 2	□ f(.	×		<urassigneu></urassigneu>						
SMIF SPI Slave Select 3	□ f(.	()		<unassigned></unassigned>	-					
 Interrupt Cause 			(?) SPI Data[7]	<unassigned></unassigned>						
Memory Mode Alignment Error	□ f(.	8	SPI Slave Select 0	<unassigned></unassigned>						
RX Data FIFO Underflow	[] f(2	③ SPI Slave Select 1	<unassigned></unassigned>	Ť					
TX Command FIFO Overflow	f(I	③ SPI Slave Select 2	<ur><unassigned></unassigned></ur>	Ť.					
TV Data EIEO Overflow			(?) SPI Slave Select 3	<unassigned></unassigned>	Ť.					
		×	 Interrupt 							
IX and RX FIFO Trigger Levels			⑦ Memory Mode Alignment Erro	r 📃						
RX FIFO Trigger Level	0 × f(N	? RX Data FIFO Underflow		_					
TX FIFO Trigger Level	0 × f(×	(?) TX Command FIFO Overflow		_					
 Advanced user: Build configuration 			DMA Triggers							
Generate code from cv. smif.cvsmif file	f	× I	RX Trigger Output	<unassigned></unassigned>	1					
		×	RX FIFO Trigger Level	0						
			⑦ TX Trigger Output	<unassigned></unassigned>	.]					
Datasheet	OK	Apply Cancel	⑦ TX FIFO Trigger Level	0						
			Advanced							
			(?) Store Config in Flash		_					



TCPWM

Personalities

Like the SCB block, the TCPWM block includes several personalities in the Device Configurator: PWM, Quadrature Decoder, and Timer. When you enable a TCPWM block, a dialog displays to select the appropriate personality:

Vevice Configurator 2.1	×
'TCPWM[0] 32-bit Counter 1' supports multiple personalities. Select the one that should be enabled here.	I
PWM-1.0 Quadrature Decoder-1.0	
Timer - Counter-1.0	
OK Cancel	

Assign Inputs and Outputs

For the TCPWM block, the biggest change between PSoC Creator and ModusToolbox is routing into and out of the TCPWM. In PSoC Creator, you could connect wires between the TCPWM inputs and outputs and various other Components on the schematic. ModusToolbox does not have a schematic, so it requires a different mechanism.

1. To assign inputs and outputs in ModusToolbox, go to the Device Configurator Parameters pane for the TCPWM personality and scroll down to **Inputs** and **Outputs** sections, as shown:

▲ Inputs		
📋 Clock Signal	<unassigned></unassigned>	
⑦ Count Input	Disabled 🗸 🗸	
⑦ Kill Input	Disabled 🗸	
? Reload Input	Disabled 🗸	
? Start Input	Disabled 🗸	=
? Swap Input	Disabled 🗸	
PWM Output Polarity		
Invert PWM Output		
Invert PWM_n Output		
 Outputs 		
PWM (line)	<unassigned></unassigned>	
PWM_n (line_compl)	<unassigned></unassigned>	
Overflow	<unassigned></unassigned>	
⑦ Underflow	<unassigned></unassigned>	
⑦ Compare (cc_match)	<unassigned></unassigned>	

- 2. For **Inputs**, select the type of input required: **Rising Edge**, **Falling Edge**, **Either Edge**, Or **Level** (if available). A new row appears where you can choose the source of the input from a drop-down menu.
- 3. After choosing the input, click the link icon to jump to the Parameters pane for the peripheral connected to the TCPWM.
- 4. You also need to assign a clock input to the TCPWM from one of the many programmable clock dividers.
- 5. For the TCPWM Outputs, use the "..." to select multiple locations to route the TCPWM output.

Each TCPWM has specific outputs to which the **PWM** and **PWM_n** signals are connected. In PSoC Creator, if you connect a Pin Component to the **PWM** or **PWM_n** outputs and choose a pin, the appropriate TCPWM is selected automatically.



In ModusToolbox, you must select the correct TCPWM for your application. The easiest way to do this is:

- Go to the **Pins** tab in the Device Configurator.
- □ Enable the pin you want to use for a TCPWM output.
- □ Click on the digital output selection choose the TCPWM you want.

□ Then, use the end to open t

e the 🖾 to open the Parameters pane for that TCPWM.

For each TCPWM personality (PWM, Timer Counter, Quadrature Decoder), copy the configuration information from the PSoC Creator Component to the Device Configurator.

MCWDT

Replicate the settings as appropriate.

PSoC Creator				M	ModusToolbox Device Configurator						
Configure 'MCWDT_System	m'		? ×	N	Multi-Counter Watchdog Timer (MCWDT) 0 - Parameters - Modus C 🗴						
Name: MCWDT_Syste	m			E	ntar filtar tavt						
General Built-in			4 Þ			·= ··					
 Cascade 				N	lame	Value					
Cascade C0C1		f(x)		~	Counter0						
Cascade C1C2		f(x)			⑦ Clear on Match	Free running V					
Counter0					Match	32768					
Enable counter		f(x)				52100					
Match	60000	f(x)			() Mode	No action V					
Mode	Interrupt ~	f(x)		~	Counter1						
Clear on Match	Clear on match	f(x)			⑦ Clear on Match	Free running 🛛 🗸					
Counter1 Eachla counter		£()			⑦ Match	32768					
Match	22769	1(X) 5(v)			(?) Mode	No action Y					
Mater	No action	f(x)		- L	Counter?						
Clear on Match	Free running V	f(x)			2 Mode	No action					
Counter2											
Enable counter		f(x)			Period / Toggle Bit	16					
Period / Toggle Bit	Toggle bit 31 🗸	f(x)		~	Cascade						
Mode	Interrupt 🗸	f(x)			⑦ Cascade C0C1						
					? Cascade C1C2						
All counters are clock	(ed by either LFCLK (nominal 32 KHZ) or t	by a ca	scaded counter.	~	 Advanced 						
C2 (32-bit)	C1 (16-bit)		C0 (16-bit)		? Store Config in Flash						
Freq (Hz): 0.00 Period (hr): 18.64	Freq (Hz): 0.49 Period (s): 2.05		Freq (Hz): 0.53 Period (s): 1.88								
The interrupts are OF	?'d together to a single interrupt										
Datasheet	ОК		Apply Cancel								



RTC

Replicate the settings as appropriate.

PSoC Creator	ModusToolbox Device Configurator
Configure 'RTC' ? X	Real Time Clock (RTC) - Parameters - Modus Configurator
Name: RTC	Enter filter text
General Built-in 4 D	Name Value
General Settings	General Ormat MM/DD/YYYY
Date Format MM/DD/YYYY f(x) Enable Interrupts If (x) f(x)	Time and Date
Time Reset on Start	(?) Seconds 0 (?) Minutes 0
Daylight Saving (DST) Settings	? Hours Format 24H ~
Enable DST Functionality f(x)	? Hours 12 ? Day of the Week Sunday
Datasheet OK Apply Cancel	⑦ Month 1
	(?) Day of the Month January ~
	Advanced
	③ Store Config in Flash

BLE

Replicate all settings from the PSoC Creator Component customizer to the ModusToolbox Bluetooth Configurator. Refer also to the <u>ModusToolbox Bluetooth Configurator Guide</u>, as needed.

PSoC Creator	ModusToolbox Bluetooth Configurator
Configure 'BLE' ? × Name: Image: State in the state	Dr/ModusToolbox/CodeExamples/CE212736_mtw/CE212736_config/GeneratedSour File Help Save General GATT Settings GAP Settings Link Layer Settings General Maximum number of BLE connections: 1 * AP role Peripheral Broadcaster Central Over-The-Air bootboading with code sharing Disabled Stack and Profile Profile only BLE Controller only (HCI over UART)

For a detailed explanation regarding how to configure the correct BLE middleware appropriate for your project, refer to the <u>BLE</u> <u>Middleware API Reference Manual</u>.BLE



Emulated EEPROM

Unlike most ModusToolbox peripherals, the Emulated EEPROM is not configured by the Device Configurator. Use the Library Manager to enable the middleware. Refer to the Library Manager User Guide for more details.

PSoC Creator	ModusToolbox Library Manager
Configure 'Em_EEPROM_v2_0' ? X	Kanager 1.1
	Settings Help
Name: <u>Em_EEPROM</u>	Directory: /My App
Basic Built-in 4 D	Projection (1997)
EEDROM Size 256 f(4)	Project: //my_/vpp
	Active BSP: CY8CKIT-062-WIFI-BT
Redundant Copy Yes V f(x)	Enter filter text
Use Blocking Write Yes \checkmark $f(x)$	
Use Emulated EEPROM Yes Y f(x)	BSPs Libraries
Actual EEPROM size (bytes): 2048	Name Version
Vear Level Factor 2x Y (1/x)	Board Utils
	PSoC 6 Base Libraries
Datasheet OK Apply Cancel	V core-lib Latest 1X release
	✓ psoc6hal Latest 1X release
	✓ psoc6make Latest 1.X release
	✓ psoc6pdl Latest 1.X release
	 PSoC 6 Middleware
	✓ capsense Latest 2.X release
	clib-support Latest 1.X release
	csdadc Latest 2.X release
	csdidac Latest 2.X release
	dfu Latest 4.X release
	✓ *emeeprom Latest 2.X release
	emwin Latest 3.4 release
	freertos Latest 10.X release
	usbdev Latest 2.X release
	 WiFi Middleware libraries

The Emulated EEPROM does not have a configuration dialog in ModusToolbox. Refer to the <u>Em EEPROM Middleware API</u> <u>Reference Manual</u> to learn how to configure the Emulated EEPROM middleware. There is no a way to alias it, so all the PSoC Creator API calls must be renamed to use the middleware API directly.



DFU

The Bootloader was renamed to Device Firmware Update (DFU) tool. In PSoC Creator, the DFU SDK is enabled in the project Build Settings under Peripheral Driver Library. In ModusToolbox, use the Library Manager to enable the dfu middleware. Refer to the Library Manager User Guide for more details.

			ModusToolbox Library Manager			
			? ×	🔛 Library Manager 1.1		
~				Settings Help		
6-q2-update 🗸				Secondly Tich		
Default (Tools > Options): C:\f Default (Tools > Options): C:\f Decutom aftware package imports: Expand *` Collapse I Check All check All DFU DFU_SDK DFU_SDK Core Communication UART Communication BLE Communication SPI RTOS FreeRTOS DFFRERTOS OK	Program Files (x86)\Cypress Version 5.46 3.0.0 3.0.0 3.0.0 3.0.0 3.0.0 3.0.0 10.0.1 10.0.1	Descript * FlexColo DFU SDK Files spe UART co BLE com I2C com SPI com The simp The simp Cancel	Directory: Project: Active BSP: CY8CKIT-062-BLE Enter filter text BSPs Libraries Name Version Abstraction Layers Board Utils PSoC 6 Base Libraries PSoC 6 Middleware bless Latest 3X release capsense Latest 3X release cibi-support Latest 1X release csdidac Latest 2X release csdidac Latest 2X release csdidac Latest 2X release emeeprom Latest 2X release emeeprom Latest 2X release emeeprom Latest 5X release emwin Latest 5X release freertos Latest 10X release		
	iq2update ✓ Default (Tools > Options): C.V Custom ttware package imports: jExpand * Collapse ♥ Check Al ckage □ LCD Driver □ DFU □ DFU SDK □ DFU SDK □ Core □ App type □ Communication UART □ Communication BLE □ Communication SPI ■ Communication SPI ■ FreeRTOS □ FreeRTOS □ FreeRTOS □ Memory Management utilities	iq2update ✓ Default (Tools > Options): C:\Program Files (x88 Custom Files (x88 ftware package imports: Standard Sta	iq2update ✓ Default (Tools > Options): C:\Program Files (k86)\Cypress Custom Image: Construction of the system of the syste	? × iq2update ~ Default (Tools > Options): C:\Program Files (k86)\Cypress\PDL\3.1.2 Custom * thware package imports: * gExpand * Collapse for Check All Uncheck All ckage Variant Version Descript * - LCD Driver FlexColor S.4.6 - DFU_SDK		

Refer to the <u>Device Firmware Update Host User Guide</u> and the <u>DFU Middleware API Reference Manual</u> to learn how to configure the DFU middleware.



USB

A USB application can use the USB PDL driver directly or the USB middleware in ModusToolbox. Use the Library Manager to enable the middleware. Refer to the Library Manager User Guide for more details.

BSPs	Libraries			
Name			Version	
Abst	traction Layer	s		
Boar	rd Utils			
BT N	/liddleware lib	oraries		
PSo	C 6 Base Libra	ries		
 PSo 	C 6 Middlewa	ire		
	capsense		Latest 2.X release	
	clib-supp	ort	Latest 1.X release	
	csdadc		Latest 2.X release	
[csdidac		Latest 2.X release	
	dfu		Latest 4.X release	
	emeepror	n	Latest 2.X release	
	emwin		Latest 5.X release	
	freertos		Latest 10.X release	
	✓ *usbdev		Latest 2.X release	
▶ WiFi	Middleware	libraries		

The PSoC Creator USB Configurator settings can be replicated to the ModusToolbox USB Configurator. For USB Configurator details, refer to the <u>ModusToolbox USB Configurator Guide</u>.

PSoC Creator	ModusToolbox USB Configurator						
Configure 'USBFS_Dev_1' ? X	design.cyusbdev - USB Configurator 2.1 – 🗆 🗙						
Name: USBFS_Dev_1 Configuration Built-in 4 b	File Edit View Help						
□ Basic	Configuration Descriptor Interface DescriptorType Field Size Value Field Size Value Field Size Value bescriptorType 18 bx01 bcdUSB b2 bx02 bDeviceClass 18 bx00 bDeviceProtocol 18 0 bdeviceProtocol 18 dV0 bdeviceProtocol 18 dVendor z8 dv84 idProduct 18 iProduct iProduct						
Data Endpoint 2 Priority Interrupt Medium Y f(x) Data Endpoint 3 Priority Interrupt Medium Y f(x)	Notice List III III IIII IIII IIII IIII IIII III						
Datasheet OK Apply Cancel							

Refer to the <u>USB Middleware API Reference Manual</u> to learn how to configure the USB peripheral. The USB middleware in turn uses the USB PDL driver. If your PSoC Creator project uses the USB PDL driver, then you should be able to port the project following the guidelines mentioned in this document for a normal PDL driver.



CapSense

CapSense is delivered as a middleware library in ModusToolbox. Use the Library Manager to enable the middleware. Refer to the Library Manager User Guide for more details.

BSPs	Libraries		
Name			Version
Abst	traction Lay	ers	
Boar	rd Utils		
BT N	/liddleware l	ibraries	
PSo	C 6 Base Lib	raries	
👻 PSo	C 6 Middlew	/are	
	*capsen:	se	Latest 2.X release
	clib-sup	port	Latest 1.X release
	csdadc		Latest 2.X release
	csdidac		Latest 2.X release
	dfu		Latest 4.X release
	emeepro	om	Latest 2.X release
	emwin		Latest 5.X release
	freertos		Latest 10.X release
	usbdev		Latest 2.X release
▶ WiFi	Middlewar	e libraries	

CapSense middleware is enabled by default for BSPs that support CapSense. CapSense configuration settings can be replicated from the PSoC Creator Component customizer to the ModusToolbox CapSense Configurator.

SoC	Creator							Mo	dusToolbox CapS	ense Configur	ato	r				
Configure	'CapSense'						? ×	*							- 0	×
子 Load co	onfiguration 🛛 🛃 Sav	ve configuration 🖻 Expe	ort Regist	ter Map				Eile	Edit View Help							
Name:	CapSense								iiii 🖬 🖨 🚆 III) + (™	*						
Bas	ic Advanced Ge	estures ADC Built-In	1				4 Þ	Basic	Advanced Pins							_
1 Mo	ve up 🔸 Move do	own 💥 Delete	CSD tu	ning mode:	SmartS	ense (Full /	Auto-Tune) ~	T M	love up 🗣 Move down 🕱 Delete	Contra Mada		SD tuning mode	SmartSens	se (Full Au	ito-Tune)	•
Туре	Name	Sensing mode	Sen	sing element	nt(s)		Finger capacitance	Type	Rutton	CSX (Mutual-	Sensi	ng Element(s)	1 7		Finger Cap	acitance
0	Button0	CSX (Mutual-cap)	1	Rx	1	Tx	N/A		Button1	cap) CSX (Mutual-	1	Ry	1 T	iv.	N/A	
0	Button 1	CSX (Mutual-cap)	1	Rx	1	Tx	N/A	220	LinearSliderD	CSD (Self-cap)	5	Seaments		~	0.16 pF	
ΣD	LinearSlider0	CSD (Self-cap)	5	Segmen	nts		0.16 pF	+		Cob (Sen Cap)	5	Jegmenta			0.10 pi	
								Senso	NY FRANJEYAR							
								CSD) electrodes: 5	CSX electrodes:	4				Pins requ	ired: 12
Sensor	resources		10.10					Notice	List							0 8
CSD ele	ctrodes: 5 CSX	electrodes: 4 Pins re	equired:	12 Pi	ns availa	able: 36		▲ Fit	x Description						Lo	cation
Data	sheet			OK		Apply	Cancel									
Conto								Ready							Device:	PSoC 6

Instead of setting the clock frequency, you now set the clock frequency divider in the CapSense Configurator. The **Tx clock source** settings and the **Sense clock source** settings are now in the **Widget Details** subtab under **Advanced** tab. Gestures are also in the **Widget Details** tab for the Linear Sliders.

The CapSense ADC is a middleware library in ModusToolbox called CSDADC. Enable this middleware like any other middleware using the Library Manager Tool.

For information on designing your CapSense applications, refer to the <u>PSoC 4 and PSoC 6 MCU CapSense Design Guide</u>. For CapSense Configurator specific details you can refer to the <u>CapSense Configurator Guide</u>.





Importing Your Code

If you've used other files beyond the *main.c* file in PSoC Creator to build your application, you can simply drag and drop those files into the application directory and they will be included in your application. This also works for directories. Build your application and start working on the errors. (The following sections will help with resolving some of these errors.)

Building project.h File

The files you copy from a PSoC Creator project likely reference the *project.h* file to pull in the specific component settings. ModusToolbox doesn't have a *project.h* file. You should create this file as it is a convenient place to put headers, defines, and constants that you might need elsewhere in your project. To get started, put the following in your *project.h* file:

```
#include "cy_pdl.h"
#include "cybsp.h"
```

Rewriting main.c File

If you copy the *main.c* file from your PSoC Creator design, nothing will work. Pins and clocks are not initialized automatically in ModusToolbox software. Add the following calls to your *main.c* file so that everything is initialized correctly:

```
cy_rslt_t result;
/* Initialize the device and board peripherals */
result = cybsp_init() ;
if (result != CY_RSLT_SUCCESS)
{
    CY_ASSERT(0);
}
enable irq();
```

Rewriting Component-Specific APIs and Migrating ISRs

There are two approaches to this:

- Inspect your code, find all Component-specific APIs, and look up the correct PDL call to do the same thing.
- Alternatively, you can simply build the application and look at the errors to help find all the component API calls.

Additionally, if you go to the same code in PSoC Creator, you can right-click on the call and use the "Go to Definition" command to find the code. In most cases, you can copy the component-specific API code and replace the API call with it. Or you can copy the code into a file and prototype into a header file to quickly move the call over.

As for ISRs, follow the same techniques described above.