PSoC® Creator™ Release Notes

Version 2.1

Revision Date: June 28, 2012

PSoC Creator 2.1 is a new release of the Cypress PSoC 3 and PSoC 5 device configuration environment. This release adds rubber-banding support in the schematic editor, an analog routing editor, and a Document Manager.

This production-quality release does not replace existing installations of PSoC Creator; it installs alongside them. This enables you to move designs to the new version at your own pace. We guarantee that your existing designs can be opened in the new software. To ensure that you can always return to your previous setup, a backup of your project is automatically created when opening a project in a new version of the tool.

This document describes general software features and changes since the PSoC Creator 2.0 release.

If you have technical questions visit www.cypress.com/go/support or call 1-800-541-4736 and select 8.

Contents

New Features

New cy_boot and Bootloading Components

Bootloading has been redesigned in this release to improve ease-of-use and to reduce the flash footprint by approximately 20%. Previously, the bootloading APIs were included in the cy_boot component. Now, these are generated from a pair of new components: Bootloader and Bootloadable. The configuration of bootloading options, which used to occur in the design-wide resources System Editor, is now performed by editing the component parameter editors. This is more natural and intuitive.

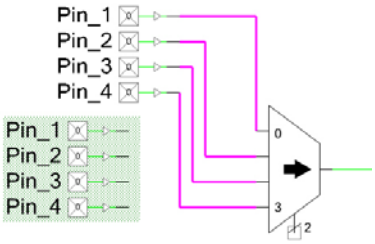
The existing Bootloader and Bootloadable project types are still used, and each is now required to incorporate its namesake component. New Bootloadable projects are backward compatible with Bootloaders that were built in PSoC Creator 1.0 and 2.0.

Note that the cy_boot component has revved a major version number to v3.10. As a result, the user APIs it provides are being changed. Existing application firmware should be modified to call the instance-named APIs, rather than the CyBtldr-prefixed APIs. Refer to the *PSoC Creator 2.1 Migration Guide* and the *System Reference Guide* for more information.

Note Custom bootloaders (that is, those that implement their own communication interface instead of using a Cypress-supplied component) are supported in this release.

Rubber-Banding Schematic Wires

Prior to this release, moving components or wires in the schematic editor caused connections to break. This required you to manually move, or re-draw, wires to retain the expected functionality. With rubber-banding, moves no longer break connections. Wires stretch and squeeze automatically to keep connections intact, and the process of creating clean, error-free designs is appreciably simplified.



Rubber-banding includes a preview, where you can see how the wires will be redrawn. You can make small adjustments to adjust the wiring. You can select one or many components and wires to find the perfect adjustment if the design is too congested.

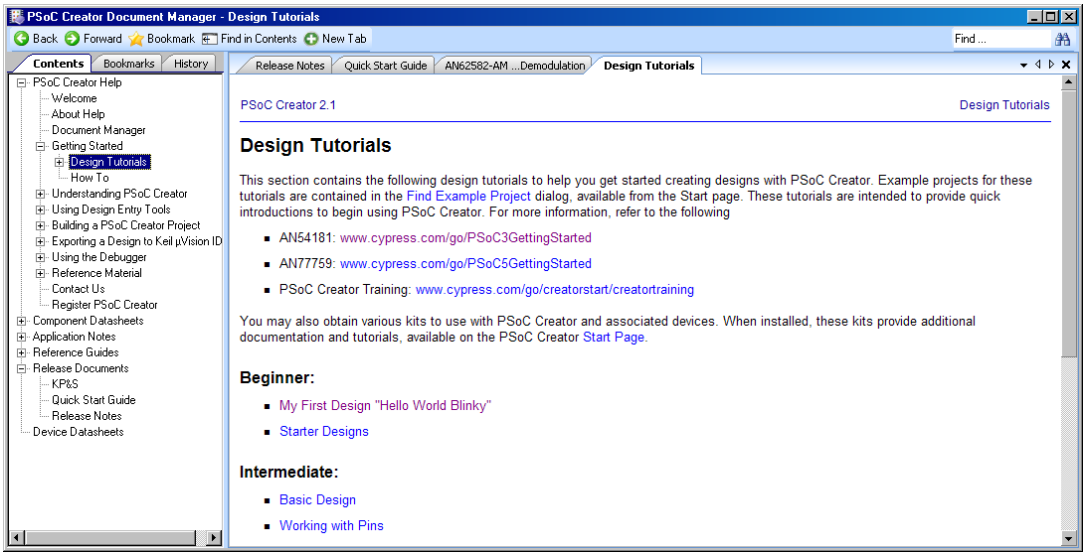
However, sometimes, you do want moves to break wires. To do this, press the [Ctrl] key while moving components.

If you prefer moves that break by default, there is an option called Schematic Moves “rubber-band” in the Tools > Options dialog, under Design Entry, in the Wire section. If you disable this option, normal moves will break wiring, but they will not break if you press the [Ctrl] key.

Document Manager

PSoC documentation is spread across many locations: on the web and in the PSoC Creator distribution. It also takes many forms, including datasheets, user and reference guides, application notes, and so on. This can make it hard to find the right information.

The new Document Manager tool helps you locate documentation, regardless of the location, and presents it in a convenient, simple-to-use tabbed viewer. The Document Manager is available from the Start menu and from the PSoC Creator Help menu.

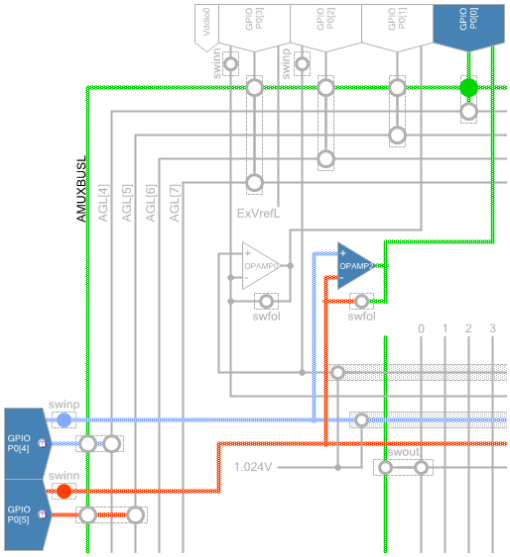


Datasheets Tab in Workspace Explorer

Another new documentation feature is the Datasheets tab in the Workspace Explorer. Under this tab, there are links to the datasheets for components that you use in your design. It is a convenient way to access the documentation for things you actually have in the design.

Analog Device Editor

Many users love the schematic capture interface and how it enables the rapid creation of analog circuits. However, sometimes you just need to know how those wires are realized in the device itself. The Analog Device Viewer/Editor, found in the new Analog tab of the Design-Wide Resource Editor, gives you that visibility.

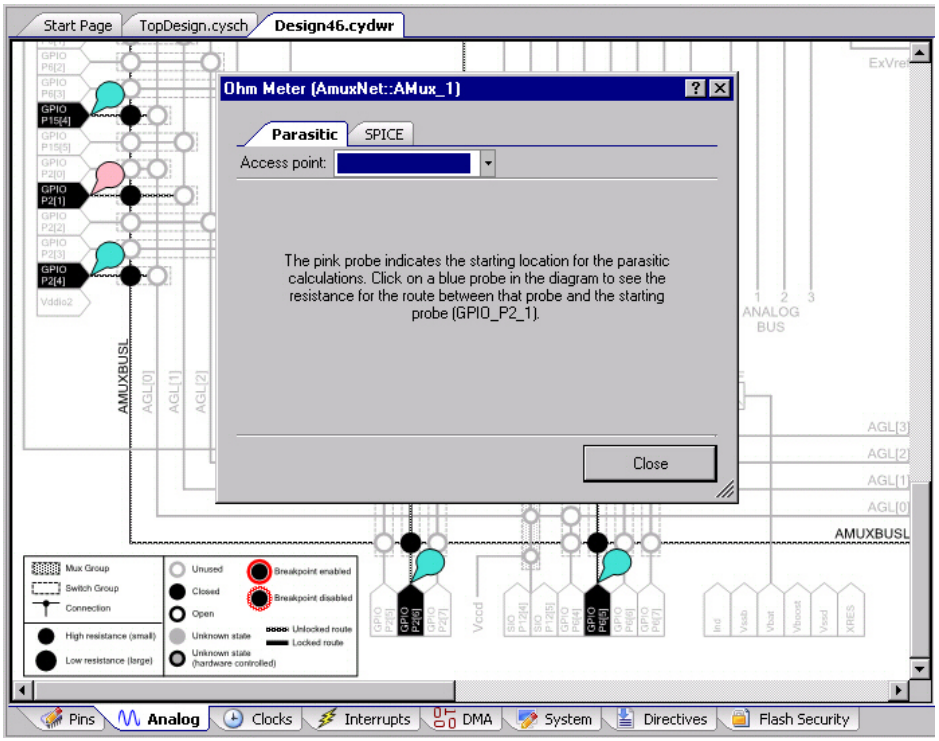


You can also lock routes so that perfected circuits will not be moved by adding new functionality to a design. To really optimize your analog performance, you can also rip-up and re-route signals to get the connectivity and parasitic properties that match your needs.

Ohm Meter

The Analog Device Editor also provides a unique “Ohm Meter” feature that shows the internal resistance associated with signal paths. Right-click on a pin or resource block and select “Start Ohm Meter.” On the pull-right menu, all the available terminals on that block are listed.

Select one and the editor automatically puts pins on all the possible connections that can be made from that point.



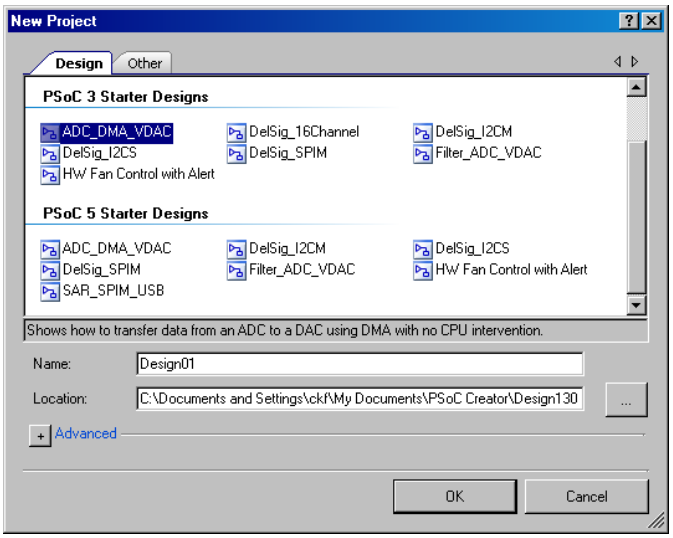
Click on one of these pins and the Ohm Meter indicates the resistance between the two points. It also provides a SPICE-compatible netlist for the passive elements of the selected route. Pick any other pin and the Ohm Meter will instantly update with the data for the new route.

Timing-Driven Placement

Timing-driven placement (TDP) is a back-end feature to reduce warnings from the static timing analyzer (STA). By examining both the clocking requirements of components and the presence of connections between them, TDP seeks to allocate components to UDB resources that are least likely to generate timing violations. It builds on the timing-driven routing (TDR) feature introduced in the PSoC Creator 2.0 release to recognize timing problems and adjust placement to avoid them.

Starter Design Templates

With the new Starter Design templates you don't need to create every new design from scratch. Instead of choosing an "Empty PSoC Design," you can pick from a list of pre-prepared designs that include popular functionality in the schematic and the C code to get it running.



New Power Supervision Components

There is a new category of components in the Component Catalog called "Power Supervision." This category contains the following components:

- The Voltage Sequencer component was a "Concept" component in a previous release of PSoC Creator. It has been updated to version 2.0 and validated as production-worthy. This component is used to turn on an array of voltage regulators in a specified sequence with specified timing.
- The Voltage Fault Detector component monitors up to 32 voltage inputs and detects/reports user-defined under-voltage (UV) or over-voltage (OV) thresholds.
- The Trim and Margin component provides a simple way to adjust the nominal output voltage of up to 24 power converters to meet user-specified nominal voltages, plus high and low margin settings.
- The Power Monitor component measures power converter output voltages and load currents, as well as monitors the health of the power converters generating warnings

New Fan Controller Component

There is another new category of components in the Component Catalog called "Thermal Management," which contains the Fan Controller component. This component was a "Concept" component in a previous release of PSoC Creator. It has been updated to version 2.0 and validated as production-worthy. This component is a system-level fan controller solution to help reduce development time and effort. The component encapsulates all necessary hardware blocks, including PWMs, tachometer input capture timer, control registers, status registers and a DMA controller.

Design Impact

Updated EEPROM Component

The EEPROM component now supports byte-write, and all APIs have been updated to improve performance. Note that, to achieve the optimization, the device temperature is no longer checked on every write operation. It is the application's responsibility to verify the temperature (and re-calibrate the EEPROM component) as needed.

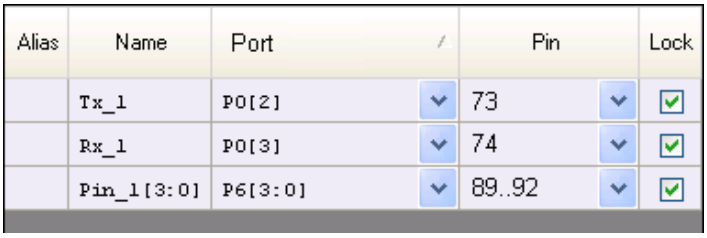
Debugging With Interrupts

Stepping through code in the debugger can be difficult when you have a lot of interrupts active in the system and they are being triggered from components in your schematic (which keep running even though you stopped the CPU). The ISRs get executed and trick the debugger into thinking a step or step-over command has completed. Sometimes you just want to validate your C code flow, so we added a button that toggles the global interrupt enable bit. With this button, you can turn interrupts off temporarily to check the code is working as expected. Then re-enable them with a single click to verify the whole system is working well.

Design-Wide Resource Editor Enhancements

The Design-Wide Resource Editors have been given a face-lift to make them easier to use.

The Pins Editor has added a "Pin" column, as shown, which allows you to choose by pin number rather than only by port address. Also, when you select a pin this table it automatically highlights the selection in the pin diagram so you can see exactly where your selections are on the package.



The Clocks Editor has an improved interface for the MHz ECO source (XTAL). It is now possible to set the accuracy based on PPM and to enable automatic gain control to support low drive level crystal oscillators.

New Clock Synchronization Check

PSoC Creator 2.1 adds a new timing design rule check (DRC) that ensures synchronized clocks are not running above half of BUS_CLK (unless BUS_CLK itself is the clock source). This is an important design consideration for high-speed digital designs.

This warning has been seen in CapSense designs when the scan rate is 24 MHz. Cypress recommends lowering the scan rate to address the warning in these situations. However, the condition does not cause applications to fail.

The Cypress knowledge base article "New clock synchronization check exposes aliased scan rate issue in CapSense" includes more details and solutions. The article is available online at: http://www.cypress.com/go/creatoronlinekps.

IMO Accuracy Change for Two PSoC 3 Families

The IMO clock accuracy for the CY8C32* and CY8C34* PSoC 3 device families was reduced from +/-1% to 2%. Other PSoC 3 devices remain at 1%.

PSoC Creator 2.1 correctly reports the accuracy for the IMO and, as a result, you may see design rule warnings for designs that rely on the prior value. If you encounter these warnings we recommend you review the clock requirements of your design closely and consider a new source if the new IMO spec is not sufficiently accurate.

Obsolete Components

A number of old versions of components have been re-classified as Obsolete for all devices. In all cases there are newer versions of the component that are of a higher quality. Using these components will cause a design-rule warning in the Notice List window. This message requests that you update the component version or, in a few cases, take alternative actions to get onto supported implementations.

The PSoC Creator 2.2 release will not include these components. The impacted components are as follows.

ADC_DelSig	v1.0	EEPROM	v0.0	SegLCD	v1.50
ADC_DelSig	v1.10	EEPROM	v1.10	SegLCD	v1.60
ADC_DelSig	v1.20	EZI2C	v1.0	SGPIO_Initiator	v1.20
ADC_DelSig	v1.21	EZI2C	v1.10	SGPIO_Target	v1.30
AMux	v1.0	FanController	v1.20	ShiftReg	v1.10
AMux	v1.10	Filter	v1.10	SleepTimer	v1.0
AMuxSeq	v1.10	I2C	v1.0	SleepTimer	v1.50
BoostConv	v1.0	I2C	v1.10	SPI_Master	v1.0
CAN	v0.5	IDAC8	v1.0	SPI_Master	v1.10
CAN	v1.10	IDAC8	v1.10	SPI_Slave	v1.0
CAN	v1.20	Mixer	v1.0	SPI_Slave	v1.10
CapSense	v0.5	PGA	v1.0	StaticSegLCD	v1.10
CapSense	v1.10	PGA	v1.10	StaticSegLCD	v1.20
CapSense	v1.20	PGA_Inv	v1.0	TIA	v0.5
CapSense	v1.30	PrISM	v1.10	Timer	v1.0
CharLCD	v0.2	PRS	v0.5	Timer	v1.10
CharLCD	v1.10	PRS	v1.10	UART	v1.0
CharLCD	v1.20	PRS	v1.20	UART	v1.10
Comp	v1.0	PWM	v1.0	UART	v1.20
Counter	v1.0	QuadDec	v1.10	USBFS	v0.2
Counter	v1.10	RTC	v0.5	USBFS	v1.10
CRC	v1.10	RTC	v1.10	USBFS	v1.20
cy_boot	v1.0	SegLCD	v1.0	USBFS	v1.30
cy_boot	v1.10	SegLCD	v1.10	VDAC8	v1.0
cy_boot	v1.20	SegLCD	v1.20	VDAC8	v1.10
DieTemp	v1.0	SegLCD	v1.30	VoltageSequencer	v1.50

Device Configuration Mode

For new designs, the default Device Configuration Mode setting in the Design-Wide Resources (DWR) System Editor has been changed from "DMA" to "Compressed." This will increase boot time, but free up more flash for application code. Existing projects are not impacted by the change.

PSoC 5LP Devices

You may notice references to PSoC 5LP devices in the component datasheets and other documentation. This device family is a future Cypress product that has not been released.

Several components were updated solely to include support for PSoC 5LP; check the change logs in the component datasheets to verify whether new component revisions contain changes that are relevant to your device.

Please contact your local Cypress Sales, Sales Rep or Distributor for more information about PSoC 5LP.

Exporting to µVision4 IDE

"Device not Found"

Sometimes when exporting a project to µVision4, a pop-up displays an error "Device not Found." Beginning with version 4.23 of the µVision IDE, a check was added to ensure that the device is present in µVision's device catalog. Some PSoC 5 devices were added to the catalog, but no PSoC 3 devices. The Keil compilers that Cypress officially supports are packaged with versions of µVision that do not have this issue. This issue will be addressed in the Public Release version of PSoC Creator 2.1.

Switching Compilers not Supported

The Export to µVision4 features supports for export to GCC, MDK, and RVDS. However, it does not support switching compilers after you have exported. You will have to create a new project with the different compiler. This issue will be addressed in the Public Release version of PSoC Creator 2.1.

Support for PSoC 3 ES2 Devices Closed

As announced in the 2.0 release notes, support for the pre-production (ES2-marked) PSoC 3 devices has been discontinued in the 2.1 release. If you open a project that targets any of those devices the tool directs you to the equivalent production device. It also creates a backup of the original project that you can continue to use in PSoC Creator 1.0 or 2.0.

If you are still using Cypress kits with ES-marked devices, please go to www.cypress.com/go/psockitupgrade to request a free replacement kit.

Supported Devices

The design flow and tools available in PSoC Creator 2.1 support the following PSoC 3 (CY8C3x) and PSoC 5 (CY8C5x) families of devices:

PSoC 3:	CY8C32*	CY8C34*	CY8C36*	CY8C38*
PSoC 5:	CY8C53*	CY8C54*	CY8C55*	CY8C56*

Supported Toolchains

Toolchains for PSoC 3 (8051)

DP8051 Keil™ 9.03

The Keil PK51 Professional Developers Kit for PSoC is installed with PSoC Creator. It supports optimization levels 0 through 5. If you would like to use the compiler optimization levels above level 5, you should purchase the standard PK51 product by contacting Keil.

- In North, Central, or South America... sales.us@keil.com
- In Europe, Asia, Africa, or Australia... sales.intl@keil.com

The free toolchain comes with a 30 day evaluation license. You can extend the license, without cost, by registering the product from within PSoC Creator (Help > Register > Keil…). Note that the extended license is for one year and that you will need to re-register it on expiry.

DP8051 Keil Generic

This option can be used to select a separately-installed version of the Keil toolchain. While any version can be selected, the only version officially supported versions are 8.16 and 9.03.

Toolchains for PSoC 5 (ARM)

ARM GCC 4.4.1

The CodeSourcery Sourcery G++ Lite for ARM is installed with PSoC Creator. It has no use restrictions and does not require license activation (it is distributed under the terms of the GNU Public License).

ARM GCC Generic

This option can be used to select a separately-installed version of the Sourcery G++ toolchain.

ARM RVDS Generic

This option can be used to select a separately-installed version of the ARM RealView Development System. The officially supported versions are 4.0 (build 529) and 4.1 (build 791).

ARM MDK Generic

This option can be used to select a separately-installed version of the ARM Microcontroller Development Kit. The officially supported versions are 4.0 (build 524) and 4.1 (build 713).

Installation

Minimum and Recommended System Requirements

The following are system requirements to install and use PSoC Creator 2.1. Each requirement specifies a minimum that your system must meet or exceed.

PSoC Creator will execute correctly in highly resource-constrained systems. However, performance (startup time, project creation and opening, build times, and so on) may be impacted when resources are scarce. The most directly impacted performance metric is build time. The following sections provide examples of the resource scarcity impact.

Note During initial startup, PSoC Creator builds and caches component DLL files used to display the component parameter editors. As a result, the tool will launch slowly the first time after installation or a Windows® reboot. This is not indicative of a problem or a long-term performance degradation.

Summary

Hardware/Operation System Requirements	Minimum
▪ Processor	1 GHz or faster 32-bit (x86) or Intel 64/AMD64 64-bit
▪ RAM	512 MB (1 GB preferred)
▪ Free Hard Drive Space	2 GB
▪ Screen Resolution	1024x768
▪ USB	2.0

Software Prerequisites *	Minimum Version
▪ Microsoft Internet Explorer (not IE8 beta)	7
▪ .NET Framework	2.0 SP2
▪ Adobe Reader (for viewing PDF Documentation)	9.2 **
▪ Windows Installer	3.1
▪ PSoC Programmer	3.15.1
▪ Keil Compiler	8.16 (9.03 provided)

* To install and run PSoC Creator, you may also need to install additional software. The Cypress Installer will guide you through the process if the additional programs are not already installed.

** For Windows 7, the minimum required version of Adobe Reader is version 9.2. You can download the latest version here: http://get.adobe.com/reader/. You can also use a non-Adobe PDF reader if you prefer; however, Cypress has no recommendations for any particular non-Adobe reader or version.

Processor

1 GHz or faster 32-bit (x86) or Intel 64/AMD64 64-bit processor is required.

PSoC Creator exhibits a predictable relationship between CPU speed and build time above 1 GHz. Doubling the CPU speed, e.g., from 1 GHz to 2 GHz or 1.5 GHz to 3 GHz, almost halves the build time.

On a fast (3 GHz) PC, simple designs can build in about one minute. At low speeds even designs that fill the device and generate complex routing solutions will build in under 5 minutes.

Operating System

One of the following Windows platforms is required:

- Windows XP SP2 or SP3 (32-bit supported)
- Windows Vista (32- and 64-bit supported) and SP1
- Windows 7 (32- and 64-bit supported) and SP1
- Mac OS X with Parallels Desktop v6 or v7 running Windows XP 32-bit SP3
- Mac OS X with Parallels Desktop v6 or v7 running Windows 7 64-bit SP1

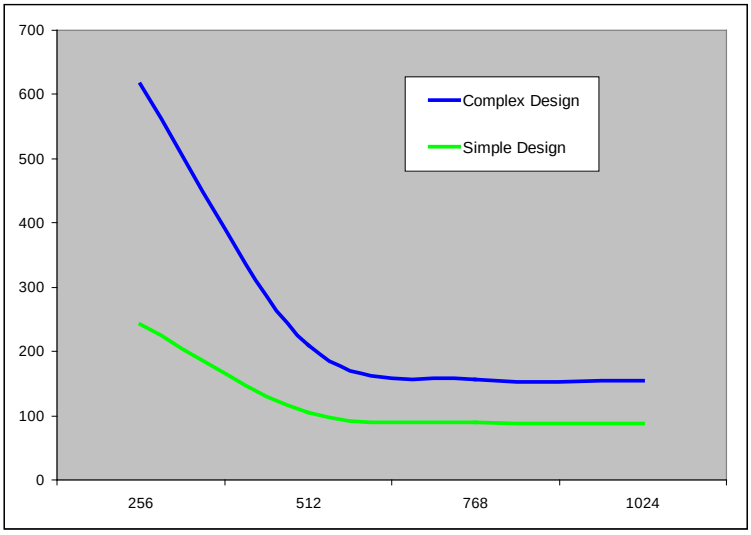
Memory

A minimum of 512 MB of RAM is required, but 1 GB is recommended.

Note Cypress does extensive performance testing on every PSoC Creator release. The minimum RAM configuration used in these tests is 1 GB. No guarantees of system performance are given below 1 GB.

With no other applications running, the minimum system configuration will ensure that the tool launches quickly, creates and opens projects in a few seconds, and responds to user input without feeling sluggish.

System RAM has the most direct impact on PSoC Creator build times. The following chart shows how insufficient RAM (i.e., below 512 MB) causes an excessive increase in build time, even for “empty” designs.



The graph shows that performance is heavily degraded below the threshold where memory paging is required but extra memory above that level does not generate a significant improvement.

Free Disk Space

PSoC Creator requires 2 GB of free disk space.

PSoC Creator will install and run with just 1 GB of free disk space. However, in order to allow Windows to do memory paging, we also require at least as much free disk space as you have RAM in your system, resulting in a minimum free disk space requirement of 2 GB.

If your disk is highly fragmented it will severely impact memory paging time and can result in very long build times. Disks that are nearly full are particularly prone to fragmentation. We recommend de-fragmenting your disk If you experience excessively long build times (10 minutes or more).

USB

PSoC Creator requires a USB 2.0-compliant host to program and debug.

Screen

A resolution of 1024x768 pixels or higher is required.

Note The build time examples given above were obtained with new product installations on minimally fragmented disks with no other applications running. If your build times exceed these expectations we recommend closing unnecessary applications, adding RAM to the system (to reduce paging) and ensuring that there is sufficient free and unfragmented disk space.

Software Update Instructions

As part of the installation process, the Cypress Update Manager utility will also be installed and located on the Start menu. You can use this utility to update all programs you have installed when updates for them become available.

Open Source

Portions of this software package are licensed under free and/or open source licenses such as the GNU General Public License. Such free and/or open source software is subject to the applicable license agreement and not the Cypress license agreement covering this software package. The applicable license terms will accompany each source code package. You may obtain the source code of such free and/or open source software at no charge from the following web site: www.cypress.com/go/opensource.

Installation Notes

The installation process is a set of wizards that walk you through installing various components. You can install PSoC Creator and various prerequisites from the web or from a CD. There are slight differences in the process, based on the medium used to install the software.

The CDs provide the necessary prerequisites and the wizards to guide you through installing the appropriate software. The following sections contain more specific installation details.

Note Do NOT plug in your Miniprog3 until all software installation is complete AND the PSoC Creator application has been opened.

PSoC Creator CD Installation

The PSoC Creator CD contains PSoC Creator and PSoC Programmer, as well as various prerequisites.

1. Load the CD. The main installer program should run automatically. If not, double-click the cyautorun.exe file to launch it.
2. On the main installer, click the **Install Software for PSoC…** button to launch the PSoC Creator InstallShield Wizard.
3. Follow the prompts on the wizard. The CyInstaller for PSoC Creator opens and displays steps to install PSoC Creator.
4. Click the hyperlink for any software that is not installed as indicated (such as, Acrobat Reader, etc.). Run the installer for that program as needed.
5. Continue following the prompts to install PSoC Creator.

Cypress PSoC Kit CD Installation

A kit CD contains PSoC Creator and PSoC Programmer, as well as projects, documentation, and prerequisites needed for the associated kit. Refer to kit instructions.

Web Installation

If you are downloading the software from the web (www.cypress.com/go/creator), run the PSoC Creator single package executable.

1. Double-click the PSoC Creator executable file to launch the installer.
2. If a non-Cypress prerequisite is missing (like .Net and Windows Installer, etc), a webpage with a download link will pop up. Download and install the prerequisites. Run the installer of those programs as needed.
3. Follow the prompts to install PSoC Creator. The CyInstaller for PSoC Creator opens and displays a series of steps to install PSoC Creator, and it will perform pre-requisite checks and install the prerequisites.
4. When complete, close the installer.

Further Reading

The primary documentation for PSoC Creator is provided in the Help, which you can open from the **Help** menu or by pressing [**F1**]. Other documents included with this release are also available from the **Help** menu, under **Documentation**. These documents include (but are not limited to):

- Quick Start Guide
- Known Problems and Solutions (KP&S)
- System Reference Guide
- Component Author Guide

The PSoC Creator KP&S document is a snapshot of the Knowledge Base issues available on online at the Cypress web site: http://www.cypress.com/go/creatoronlinekps.

Even more information is provided online at www.cypress.com/go/creator, including:

- PSoC 3, PSoC 5 Architecture Technical Reference Manual (TRM)
- PSoC 3 and PSoC 5 Registers TRM
- PSoC 3 and PSoC 5 Device Datasheets
- Migration Guides
- Application Notes
- Training

Contact your Cypress representative, as needed.

Defects Fixed

The following defects were fixed in this release. These defects are separated into different categories. The numbers with an asterisk (*) indicate fixes made since the Early Access release.

Bootloading

Cypress ID	Defect	Fix and Impact
109195	With PSoC Creator 1.0 created bootloader project, the PSoC Creator 2.0 bootloader host program downloads the bootloadable image only once.	In PSoC Creator 2.0, bootloader host program was enhanced to ensure support for future PSoC devices. This results in the bootloader host program taking slightly more than a second to initiate a transfer causing the bootloader to close the window for download. To correct this issue, open the bootloader project's .cydwr file. Go to System Tab and expand Bootloader settings. Change the "Wait For Command Time (10ms)" parameter value from “10” to "200". Rebuild the bootloader project. This is the default time out for new projects.
123109	Multi-App bootloaders fail to load when flash is protected.	Standard bootloaders use the last row of flash for metadata and design rule checks ensure the user has not protected that row. In the Multi-App case the bootloader needs two rows, which fails if the extra row is protected. A new DRC checks for two writable rows.
127046*	Compiler Warnings are generated for Bootloadable projects when building with either RVDS or MDK compilers.	RVDS and MDK compilers enforce stricter warnings on certain C constructs. This caused a warning to be generated for an internal C file. Offending C construct causing the warnings has been fixed.
126556*	Componet Update Tool does not warn users about changes when updating to the new cy_boot v3.00 component.	There are newer changes to bootloader with cy_boot v3.00 that will affect existing bootloader and bootloadable projects. Component Update Tool now warns users about changes to design when updating to cy_boot v3.00.

Build System

Cypress ID	Defect	Fix and Impact
100799	The report file occasionally lists seamingly impossible usage of status/control resources. When the design uses status registers and sync cells the usage numbers do not add up to the device maximum and it is difficult to understand the actual resources used.	Status cells can be used for status registers, statusi registers or sync cells (4 per status cell). Control cells can be control registers or count7 cells. In both cases the report file now clarifies usage by showing the total usage and an indented breakdown of how the cells are used.
119246	Attempts to assign a non-SIO pin component to an SIO-supporting physical pin results in a non-intuitive error: "apr.M0014: Location for SIO port "Pin_1" is invalid; SIO ports must align with the start of an SIO pair".	The root of the problem is that the non-SIO pin is locked to the SIO physical pin, which means another pin component, which does need the SIO, cannot be placed. This is an error condition but the appropriate message warns the user that there are no free SIO pins for the unplaceable component.

Cypress ID	Defect	Fix and Impact
124545	PSoC Creator installation triggers Windows Application Compatibility Assistant to pop up on Windows 7 and Vista.	Creator installer fixed to not issue pop ups during installations for Windows 7 and Vista.
126294	Missing library warnings for CapSense projects opened in uVision.	Export to IDE feature for CapSense projects did not include all dependent libraries. This issue is now fixed.
113155*	Export to IDE fails for projects with missing references.	When a project with missing references is exported, an unfriendly user error message is displayed. This is now fixed. If the referenced project is not essential, the export process proceeds without errors. If the referenced project is critical the missing reference will cause the export to stop.

Debugging/Programming

Cypress ID	Defect	Fix and Impact
59680	Unnecessary warnings issued about non-volatile latch (NVL) retention limits when editing System DWR parameters.	Warnings about changes to the following parameters have been disabled – a) Enable Error Correcting Code (ECC) b) Enable Fast IMO During Startup c) Use Optional XRES
114403	Debugging a PSoC 5 design with "On Run/Reset, run to" option set to "First Breakpoint" causes debugger to stop at reset vector.	A temporary breakpoint was unnecessarily added. This is now corrected.
113697	The "Select Debug Target" dialog was very confusing to users, with poorly-labeled buttons that offered overlapping functionality.	The dialog was updated with better error reporting, a single "Connect/Disconnect button", no "Apply Settings" button, and a "Port Settings" button for easy access to the MiniProg3 setup choices.
115226	Debugging PSoC designs on non-english language machines causes debugger to exit unexpectedly.	Creator, like other applications, stores user preferences in typical Windows assigned folders (Local Settings). Non-english language machines contain non-ascii characters in such Local Settings folders causing debugger to exit. This is now corrected and the debugger recognizes non-ascii character based folder locations.
118396	Program/Debug using uVision 4 does not work.	PSoC Programmer driver has been updated to work with any uVision IDE versions.
55149*	Debugger does not continue on request for designs that include interrupts.	When global interrupts are enabled, interrupts can trigger while debug session is ongoing. The interrupt triggered will cause execution to transfer to its corresponding ISR, finish ISR and returns to code where breakpoint is set causing breakpoint to be triggered again. This is fixed by providing new buttons in Debug menu to Enable/Disable Global interrupts. The new buttons allow for single stepping/running code in debugger while interrupts are enabled.
126869*	Read-only memory addresses can be edited in debug tool window during debugging.	When debugging, read-only memory addresses were allowed to be changed via memory window. This is now fixed.

Framework

Cypress ID	Defect	Fix and Impact
52158	Documentation for several important system level APIs was difficult to find.	The System Reference Guide is now available from the following: • Documentation tab in the Workspace Explorer • Schematic context menu (right click on schematic "white space")
58072	Device Selector incorrectly lists Delta Sigma ADC resources resulting in incorrect filtering.	Device Selector now handles multi-line entries in the table so that ADCs are correctly represented and filterable.
85928	Tool fails to launch the Parameter Editor for components imported from a Cypress library.	When importing a component that implements a custom Parameter Editor, the customizers must be rebuilt. This is now automatically performed at the end of the import operation.
108174	Unable to register PSoC Creator.	The cypress.com server that handles product registration was updated to correct a defect that prevented many users from registering the product. Please register manually from the Help menu if you were impacted.
112608	PSoC Creator 2.0 crashes while creating a project in the 'bin' directory.	Tool does not allow saves in PSoC Creator install directories.
112858	PSoC Creator archiver ignores user specified destination.	Destination selection made in the directory chooser dialog is now propagated to the archiver.
114442	Irrelevant search results in the Example Project finder.	When the device field is "All", the search returns all projects. Corrected search logic.
71538	Occasionally, text boxes do not get placed where the user clicks in the schematic. In some cases the text box is off-page and is not visible in the schematic editor without scrolling.	The schematic editor was unnecessarily updating the mouse location and moving the text box from where the user wanted to the current mouse location (the move was not visible, only the bad location). The update action has been removed and users should not experience unintentional moved or missing (off page) text box placement.
86824	Renaming files with case-only edits leads to build errors and reports of missing, or already-existing, files.	The tool now retains the file name internally and retains case. This means that users can change the case of files in safety.
105875	When re-targeting a design, from pre-production PSoC 3 silicon for example, the OBSOLETE / PROTOTYPE warning text in the schematic file remains, even though the component versions are approved for production.	Changing the device now forces a schematic refresh, updating the symbols and the OBSOLETE / PROTOTYPE messages.
105901	Save dialogs for workspaces are presented when closing them even though no changes have been made to the project.	Simple actions, like changing the open tab in the Component Catalog, would mark the project as edited. This information is now stored in user data, not the project file, and so unnecessary save dialog display is avoided.
107451	PSoC Creator bundles and archives do not extract properly on Mac OS X. The directory structure is not re-created.	The SharpZip option to clean file names (paths) was used to ensure the archives can be extracted or copied to any PC OS.

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111179	When there are multiple projects in a workspace the Project/Export to IDE menu option doesn't indicate which project will be exported.	The menu item now lists the project name in parentheses to avoid confusion and unwanted exports.
117848	Excessive disk access noticed when moving the mouse.	An unnecessary "IsValid" call was being made to verify the edited status of every file in the project, on every mouse move. This has been removed and the tool performance is no longer impacted.
118404	Generated Verilog code includes an extra comma after the last port definition, resulting in build errors.	The code generator was correctly omiting commas after input ports but not output or inout types. This caused the extra comma when there were no inputs to the Verilog module (which is the most common situation and the reason why "most" generated Verilog was valid). The generator now checks for extra comments for all three types.
121469	Datapath simulation does not match actual behavior.	The datapath Verilog simulation files were updated with fixes and re-worked implementations for the datapath commands: ADD, SUB, INC and DEC.
122244	Opening projects takes 15 minutes or longer.	Projects that use many bookmarks show the problem. The bookmarks are recorded as duplicates on every save of the project or workspace. Over time the project file grows exponentially and the time to open the increases accordingly. The bookmarks are now correctly updated to avoid the file bloat.
123903	Tool cannot create a workspace bundle (internal crash) on PCs configured to use Cyrillic characters for date, time and number format.	All calls were converted to be culture-invariant. Tool should be able to save bundles on Russian, Ukranian, etc. machines.
78183	Projects with inline assembly source files does not build correctly.	Creator maintains project level and file level toolchain settings. Features such as inline assembly require file level settings to be specified. The tool ignored file level settings. This is now corrected and the tool recognizes file level settings appropriately.
91597	Archiver feature in Creator does not work for workspaces listed in the same folder location as its containing projects.	Workspaces and its containing projects are now bundled appropriately irrespective of their folder locations. The bundled workspace can be reopened in Creator without any issues.
79804*	Adding component items such as PDF, HTML files for a component does not use the component name.	Tool uses an in-built naming scheme to automatically generate names for items added for a component. This naming scheme was improperly generating names when adding new component items for a Component. The naming scheme algorithm is now fixed.
53390*	Error message window does not stay on after confirming error messages while adding items for a component.	When an error is encountered during the Add Component Item menu, the error message window disappears on user accepting error message. This is now corrected such that the error message window stays open so the user can correct the error and try the command again.
123865*	Component Update will not launch for projects with unsaved changes.	When a project has unsaved changes, the component update dialog does not proceed. The component update tool message is fixed to proceed after user confirmation for project save operation.
78572*	Creator requires multiple clicks to restore from minimized state.	When PSoC Creator is in the background or has been minimized, it often takes multiple clicks on the icon in order to restore it. This defect is now fixed.

Cypress ID	Defect	Fix and Impact
51847*	Wire names are not recomputed when multiple instances of a macro are added to the Schematic.	When a macro component created with input and output wires is instantiated multiple times on the schematic, the input and output wire names of all the instances remain same causing errors to show up. This defect is now fixed.
74647*	A copy of a schmatic from Creator to Word or Powerpoint produces an unclear image.	The image resolution for the copy operation on schematics was set low resulting in an unclear image on paste operation. The graphics object copied is set to high quality to fix the issue.
94137*	The order of all open documents is not maintained when Creator is closed and reopened.	Tool did not save the ordering information of open documents. This resulted in Creator always using its default open documents ordering when relaunched after closing. This defect is now fixed.
127110*	Inconsistent information between Creator and Datasheet about USB availability in CY8C3665AXI-016 device .	Creator had incorrectly shown the absence of USB in device CY8C3665AXI-016. This is corrected.
125758*	Export to IDE command does not update the exported project information when Toolchain is changed.	If a project was exported for uVision, and then the selected toolchain is changed (eg: GCC->MDK) the changed settings does not get reflected in the subsequent exports. This is now fixed and the correct project settings is exported.

System

Cypress ID	Defect	Fix and Impact
67400	DMA register initialization is slower than the optimum.	Rearranged code in the ClockSetup() API to set the MASTER_CLK before initializing DMA.
115187	Cannot find a #define for EEPROM sector size.	Added new #define for EEPROM Sector size (CYDEV_EEPROM_SECTOR_SIZE) in cydevice_trm.h file.
117608	PSoC 5 designs build with a warning about an unused variable - timeout_p in cyfitter_cfg.c file.	The warning was generated under the following conditions – a) Using PSoC 5 b) Using the MHz XTAL c) Not using the PLL d) Not using the 32k XTAL The generated code no longer includes the variable when it is not needed.
87491	Performance of analog components is poor at low voltage (Vdda).	Internal charge pumps are used to power the analog blocks in low device voltage situations. These pumps were not enabled in the boot code, compromising performance. The tool now enables the clocks below 4.0V if analog routing, the analog mux bus, or CapSense is used in the design.
121348	Oscillations occur on the automatic gain control (AGC), causing resonant frequency changes when the MHz oscilator is enabled on the XTAL pins.	The default values for MHz ECO automatic gain control feedback and crystal error watchdog reference voltages were changed to improve ECO reliability.

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121665	The Vref component's IgnoreSleep parameter does not keep the reference active in sleep mode.	The IgnoreSleep parameter, which was supposed to enable the component to remain active while the device was in low power modes, was removed. The on-board voltage references on the devices do not, in fact, support that functionality. No change to component behavior is expected as a result. Using older versions is safe because the tool simply ignore the parameter.
121899	Tool does not allow the user to use a DSI clock to supply USB with the required 48MHz clock.	PSoC 5 devices cannot support USB clocking from the IMO source. As a result, in PSoC Creator 2.0, the user was required to enable a MHZ ECO on the XTAL pins in order to use USB on those devices. This did not account for a good quality DSI signal being used as the clock source. It is now posssible to configure a schematic signal as a closck source and use that to drive USB.
122640	An SIO pin pair with voltage levels based on VREF(1.024V) gives bad output voltage unless both pins are output.	The tool was assuming that SIO pairs would both be outputs and so could share the reference voltage. When the component is configured as one input and one output, the voltages are not as expected. The tool now detects the different pin directions and changes analog routing as needed.
122854	A Pin component with a width of two and threshold Vddio/2 cannot be placed in SIO pins.	The Pins DWR would allow the placement in P12 but this would generate a mapper error, saying that the selection is invalid. The rule checks were updated to allow the selection of all legal locations and prevention of bogus errors.
127156*	Voltage Follower does not work as expected with Vref set to 0.256V as input.	On PSoC5 devices, when the 0.256V Vref input is connected to the input of Opamp, the output measured is not 0.256V as expected. The problem is caused by incorrect treatment of 0.256V negative input on Opamp. This is now corrected to perform as expected.
127863*	Project does not work on board when using ECC to store configuration data information.	When a design has the "Store Configuraiton Data in ECC Memory" System setting enabled, the base ECC address was incorrectly calculated resulting in an incorrect data access. This issue found in 2.1 EA reelase is fixed.
128209*	Errors seen with designs using clocks running faster than half the frequency of the clock synchronizing it.	When a design uses a clock that runs faster than half the frequency of the clock synchronizing it, an error was issued in 2.1 EA tool. The error is now changed to a warning.

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