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PSoC 6 MCU: CY8C63x6, CY8C63x7 Registers Technical Reference Manual (TRM)

PSoC 63 MCU with Bluetooth LE

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Contents

Register Mapping

The Register Mapping section discusses the registers and lists all registers in mapping tables, in address order for PSoC® 6 MCU with Bluetooth LE. For Architecture details, see PSoC 6 MCU with Bluetooth LE: CY8C63x6, CY8C63x7 Architecture Technical Reference Manual (TRM).

Note that memory mapped I/O (MMIO) registers support only 32-bit access, unless otherwise specified in the register description.

Register General Conventions

The register conventions specific to this section and the Register Reference chapter are listed in this table.

Convention	Description	Explanation
RW	Read/Write	These bits can be both read and written.
R	Read only	These bits can only be read. Writing has no effect on the bit value.
W	Write only	These bits can only be written. Reading the bit returns the reset value.
RW1C	Read/Write ‘1’ to clear	These bits can be read as well as cleared by writing ‘1’. Writing ‘0’ has no effect on the bit value.
RW0C	Read/Write ‘0’ to clear	These bits can be read as well as cleared by writing ‘0’. Writing ‘1’ has no effect on the bit value.
RW1S	Read/Write ‘1’ to set	These bits can be read as well as set by writing ‘1’. Writing ‘0’ has no effect on the bit value.
A	Alias	This register is an additional alias for another register. This convention is used when a physical register is mapped to multiple addresses, typically for firmware debug purposes. See the corresponding register descriptions for more details.
None / Reserved	Reserved bits	Keep these bits at the default value
‘x’ in a register /bit field name	Multiple instances	Multiple instances/address ranges of the same register/bit field

Acronyms

This table lists the acronyms used in this document

Table 3-1. Acronyms

Symbol	Unit of Measure
ABUS	analog output bus
AC	alternating current
ADC	analog-to-digital converter
AHB	AMBA (advanced microcontroller bus architecture) high-performance bus, an ARM data transfer bus
API	application programming interface
APOR	analog power-on reset
BC	broadcast clock
BOM	bill of materials
BR	bit rate
BRA	bus request acknowledge
BRQ	bus request

Table 3-1. Acronyms

Symbol	Unit of Measure
CAN	controller area network
CI	carry in
CMP	compare
CO	carry out
CPU	central processing unit
CRC	cyclic redundancy check
CSD	CapSense® sigma delta
CT	continuous time
CTBm	continuous time block-mini
DAC	digital-to-analog converter
DC	direct current
DI	digital or data input
DMA	direct memory access
DNL	differential nonlinearity
DO	digital or data output
DSI	digital signal interface
DSM	deep-sleep mode
ECO	external crystal oscillator
EEPROM	electrically erasable programmable read only memory
EMIF	external memory interface
FB	feedback
FIFO	first in first out
FSR	full scale range
GPIO	general purpose I/O
HCI	host-controller interface
HFCLK	high-frequency clock
I^2C	inter-integrated circuit
IDE	integrated development environment
ILO	internal low-speed oscillator
IMO	internal main oscillator
INL	integral nonlinearity
I/O	input/output
IOR	I/O read
IOW	I/O write
IRES	initial power on reset
IRA	interrupt request acknowledge
IRQ	interrupt request
ISR	interrupt service routine
IVR	interrupt vector read
L2CAP	logical link control and adaptation protocol
LPCOMP	low-power comparator
LRb	last received bit
LRB	last received byte
LSb	least significant bit

Table 3-1. Acronyms

Symbol	Unit of Measure
LSB	least significant byte
LUT	lookup table
MISO	master-in-slave-out
MMIO	memory mapped input/output
MOSI	master-out-slave-in
MSb	most significant bit
MSB	most significant byte
PC	program counter
PCH	program counter high
PCL	program counter low
PD	power down
PGA	programmable gain amplifier
PM	power management
PMA	PSoC memory arbiter
POR	power-on reset
PPOR	precision power-on reset
PRS	pseudo random sequence
PSoC	Programmable System-on-Chip
PSRR	power supply rejection ratio
PSSDC	power system sleep duty cycle
PWM	pulse width modulator
RAM	random-access memory
RETI	return from interrupt
RF	radio frequency
ROM	read only memory
RW	read/write
SAR	successive approximation register
SC	switched capacitor
SCB	serial communication block
SIE	serial interface engine
SIO	special I/O
SE0	single-ended zero
SNR	signal-to-noise ratio
SOF	start of frame
SOI	start of instruction
SP	stack pointer
SPD	sequential phase detector
SPI	serial peripheral interconnect
SPIM	serial peripheral interconnect master
SPIS	serial peripheral interconnect slave
SRAM	static random-access memory
SRSS	system resources sub-system
SROM	supervisory read only memory
SSADC	single slope ADC

Table 3-1. Acronyms

Symbol	Unit of Measure
SSC	supervisory system call
SYSCLK	system clock
SWD	single wire debug
TC	terminal count
TD	transaction descriptors
UART	universal asynchronous receiver/transmitter
UDB	universal digital block
USB	universal serial bus
USBIO	USB I/O
WCO	watch crystal oscillator
WDT	watchdog timer
WDR	watchdog reset
XRES	external reset
XRES_N	external reset, active low

Section A: Supervisory Flash Registers

This section encompasses the following chapter:

1 Supervisory Flash (SFLASH) Registers

This section discusses the Supervisory Flash (SFLASH) registers. It lists all the registers in mapping tables, in address order.

1.1 Register Details

Register	Address	Description
SFLASH_SI_REVISION_ID	0x16000001	Indicates Silicon Revision ID of the device
SFLASH_SILICON_ID	0x16000002	Indicates Silicon ID of the device
SFLASH_FAMILY_ID	0x1600000C	Indicates Family ID of the device
SFLASH_SAR_TEMP_MULTIPLIER	0x16000648	SAR Temperature Sensor Multiplication Factor
SFLASH_SAR_TEMP_OFFSET	0x1600064A	SAR Temperature Sensor Offset

1.1.1 SFLASH_SI_REVISION_ID

Indicates Silicon Revision ID of the device

Address: 0x16000001

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	SI_REVISION_ID [7:0]							

Bits	Name	Description
7 : 0	SI_REVISION_ID	Silicon Revision ID Default Value: X

1.1.2 SFLASH_SILICON_ID

Indicates Silicon ID of the device

Address: 0x16000002

Retention: Retained

Bits	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SW Access	RW							
HW Access								
Name	ID [7:0]							

Bits	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SW Access	RW							
HW Access								
Name	ID [15:8]							

Bits	**Name**	**Description**
15 : 0	ID	Silicon ID Default Value: X

1.1.3 SFLASH_FAMILY_ID

Indicates Family ID of the device

Address: 0x1600000C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	FAMILY_ID [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	FAMILY_ID [15:8]							

Bits	Name	Description
15 : 0	FAMILY_ID	Family ID Default Value: X

1.1.4 SFLASH_SAR_TEMP_MULTIPLIER

SAR Temperature Sensor Multiplication Factor

Address: 0x16000648

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	TEMP_MULTIPLIER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	TEMP_MULTIPLIER [15:8]							

Bits	Name	Description
15 : 0	TEMP_MULTIPLIER	Multiplier value for SAR temperature sensor Default Value: X

1.1.5 SFLASH_SAR_TEMP_OFFSET

SAR Temperature Sensor Offset

Address: 0x1600064A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	TEMP_OFFSET [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	TEMP_OFFSET [15:8]							

Bits	Name	Description
15 : 0	TEMP_OFFSET	Offset value for SAR temperature sensor Default Value: X

Section B: Peripheral Group 0

This section encompasses the following chapters:

2 Peripheral Registers

This section discusses the Peripheral registers. It lists all the registers in mapping tables, in address order.

2.1 Register Details

Register	Address	Description
PERI_GR0_SL_CTL	0x40010020	Slave control
PERI_GR1_SL_CTL	0x40010060	Slave control
PERI_GR1_TIMEOUT_CTL	0x40010064	Timeout control
PERI_GR2_SL_CTL	0x400100A0	Slave control
PERI_GR2_TIMEOUT_CTL	0x400100A4	Timeout control. See PERI_GR1_TIMEOUT_CTL for the details of bit fields.
PERI_GR3_CLOCK_CTL	0x400100C0	Clock control
PERI_GR3_SL_CTL	0x400100E0	Slave control
PERI_GR3_TIMEOUT_CTL	0x400100E4	Timeout control. See PERI_GR1_TIMEOUT_CTL for the details of bit fields.
PERI_GR4_CLOCK_CTL	0x40010100	Clock control. See PERI_GR3_CLOCK_CTL for the details of bit fields.
PERI_GR4_SL_CTL	0x40010120	Slave control
PERI_GR4_TIMEOUT_CTL	0x40010124	Timeout control. See PERI_GR1_TIMEOUT_CTL for the details of bit fields.
PERI_GR6_CLOCK_CTL	0x40010180	Clock control. See PERI_GR3_CLOCK_CTL for the details of bit fields.
PERI_GR6_SL_CTL	0x400101A0	Slave control
PERI_GR6_TIMEOUT_CTL	0x400101A4	Timeout control. See PERI_GR1_TIMEOUT_CTL for the details of bit fields.
PERI_GR9_CLOCK_CTL	0x40010240	Clock control. See PERI_GR3_CLOCK_CTL for the details of bit fields.
PERI_GR9_SL_CTL	0x40010260	Slave control. See PERI_GR1_SL_CTL for the details of bit fields.
PERI_GR9_TIMEOUT_CTL	0x40010264	Timeout control. See PERI_GR1_TIMEOUT_CTL for the details of bit fields.
PERI_GR10_CLOCK_CTL	0x40010280	Clock control. See PERI_GR3_CLOCK_CTL for the details of bit fields.
PERI_GR10_SL_CTL	0x400102A0	Slave control
PERI_GR10_TIMEOUT_CTL	0x400102A4	Timeout control. See PERI_GR1_TIMEOUT_CTL for the details of bit fields.
PERI_DIV_CMD	0x40010400	Divider command register
PERI_DIV_8_CTL0	0x40010800	Divider control register (for 8.0 divider)
PERI_DIV_8_CTL1	0x40010804	Divider control register (for 8.0 divider). See PERI_DIV_8_CTL0 for the details of bit fields.
PERI_DIV_8_CTL2	0x40010808	Divider control register (for 8.0 divider). See PERI_DIV_8_CTL0 for the details of bit fields.
PERI_DIV_8_CTL3	0x4001080C	Divider control register (for 8.0 divider). See PERI_DIV_8_CTL0 for the details of bit fields.

Register	Address	Description
PERI_DIV_8_CTL4	0x40010810	Divider control register (for 8.0 divider). See PERI_DIV_8_CTL0 for the details of bit fields.
PERI_DIV_8_CTL5	0x40010814	Divider control register (for 8.0 divider). See PERI_DIV_8_CTL0 for the details of bit fields.
PERI_DIV_8_CTL6	0x40010818	Divider control register (for 8.0 divider). See PERI_DIV_8_CTL0 for the details of bit fields.
PERI_DIV_8_CTL7	0x4001081C	Divider control register (for 8.0 divider). See PERI_DIV_8_CTL0 for the details of bit fields.
PERI_DIV_16_CTL0	0x40010900	Divider control register (for 16.0 divider)
PERI_DIV_16_CTL1	0x40010904	Divider control register (for 16.0 divider). See PERI_DIV_16_CTL0 for the details of bit fields.
PERI_DIV_16_CTL2	0x40010908	Divider control register (for 16.0 divider). See PERI_DIV_16_CTL0 for the details of bit fields.
PERI_DIV_16_CTL3	0x4001090C	Divider control register (for 16.0 divider). See PERI_DIV_16_CTL0 for the details of bit fields.
PERI_DIV_16_CTL4	0x40010910	Divider control register (for 16.0 divider). See PERI_DIV_16_CTL0 for the details of bit fields.
PERI_DIV_16_CTL5	0x40010914	Divider control register (for 16.0 divider). See PERI_DIV_16_CTL0 for the details of bit fields.
PERI_DIV_16_CTL6	0x40010918	Divider control register (for 16.0 divider). See PERI_DIV_16_CTL0 for the details of bit fields.
PERI_DIV_16_CTL7	0x4001091C	Divider control register (for 16.0 divider). See PERI_DIV_16_CTL0 for the details of bit fields.
PERI_DIV_16_CTL8	0x40010920	Divider control register (for 16.0 divider). See PERI_DIV_16_CTL0 for the details of bit fields.
PERI_DIV_16_CTL9	0x40010924	Divider control register (for 16.0 divider). See PERI_DIV_16_CTL0 for the details of bit fields.
PERI_DIV_16_CTL10	0x40010928	Divider control register (for 16.0 divider). See PERI_DIV_16_CTL0 for the details of bit fields.
PERI_DIV_16_CTL11	0x4001092C	Divider control register (for 16.0 divider). See PERI_DIV_16_CTL0 for the details of bit fields.
PERI_DIV_16_CTL12	0x40010930	Divider control register (for 16.0 divider). See PERI_DIV_16_CTL0 for the details of bit fields.
PERI_DIV_16_CTL13	0x40010934	Divider control register (for 16.0 divider). See PERI_DIV_16_CTL0 for the details of bit fields.
PERI_DIV_16_CTL14	0x40010938	Divider control register (for 16.0 divider). See PERI_DIV_16_CTL0 for the details of bit fields.
PERI_DIV_16_CTL15	0x4001093C	Divider control register (for 16.0 divider). See PERI_DIV_16_CTL0 for the details of bit fields.
PERI_DIV_16_5_CTL0	0x40010A00	Divider control register (for 16.5 divider)
PERI_DIV_16_5_CTL1	0x40010A04	Divider control register (for 16.5 divider). See PERI_DIV_16_5_CTL0 for the details of bit fields.
PERI_DIV_16_5_CTL2	0x40010A08	Divider control register (for 16.5 divider). See PERI_DIV_16_5_CTL0 for the details of bit fields.
PERI_DIV_16_5_CTL3	0x40010A0C	Divider control register (for 16.5 divider). See PERI_DIV_16_5_CTL0 for the details of bit fields.
PERI_DIV_24_5_CTL0	0x40010B00	Divider control register (for 24.5 divider)
PERI_CLOCK_CTL0	0x40010C00	Clock control register
PERI_CLOCK_CTL1	0x40010C04	Clock control register. See PERI_CLOCK_CTL0 for the details of bit fields.
PERI_CLOCK_CTL2	0x40010C08	Clock control register. See PERI_CLOCK_CTL0 for the details of bit fields.
PERI_CLOCK_CTL3	0x40010C0C	Clock control register. See PERI_CLOCK_CTL0 for the details of bit fields.
PERI_CLOCK_CTL4	0x40010C10	Clock control register. See PERI_CLOCK_CTL0 for the details of bit fields.
PERI_CLOCK_CTL5	0x40010C14	Clock control register. See PERI_CLOCK_CTL0 for the details of bit fields.
PERI_CLOCK_CTL6	0x40010C18	Clock control register. See PERI_CLOCK_CTL0 for the details of bit fields.

Register	Address	Description
PERI_CLOCK_CTL7	0x40010C1C	Clock control register. See PERI_CLOCK_CTL0 for the details of bit fields.
PERI_CLOCK_CTL8	0x40010C20	Clock control register. See PERI_CLOCK_CTL0 for the details of bit fields.
PERI_CLOCK_CTL9	0x40010C24	Clock control register. See PERI_CLOCK_CTL0 for the details of bit fields.
PERI_CLOCK_CTL10	0x40010C28	Clock control register. See PERI_CLOCK_CTL0 for the details of bit fields.
PERI_CLOCK_CTL11	0x40010C2C	Clock control register. See PERI_CLOCK_CTL0 for the details of bit fields.
PERI_CLOCK_CTL12	0x40010C30	Clock control register. See PERI_CLOCK_CTL0 for the details of bit fields.
PERI_CLOCK_CTL13	0x40010C34	Clock control register. See PERI_CLOCK_CTL0 for the details of bit fields.
PERI_CLOCK_CTL14	0x40010C38	Clock control register. See PERI_CLOCK_CTL0 for the details of bit fields.
PERI_CLOCK_CTL15	0x40010C3C	Clock control register. See PERI_CLOCK_CTL0 for the details of bit fields.
PERI_CLOCK_CTL16	0x40010C40	Clock control register. See PERI_CLOCK_CTL0 for the details of bit fields.
PERI_CLOCK_CTL17	0x40010C44	Clock control register. See PERI_CLOCK_CTL0 for the details of bit fields.
PERI_CLOCK_CTL18	0x40010C48	Clock control register. See PERI_CLOCK_CTL0 for the details of bit fields.
PERI_CLOCK_CTL19	0x40010C4C	Clock control register. See PERI_CLOCK_CTL0 for the details of bit fields.
PERI_CLOCK_CTL20	0x40010C50	Clock control register. See PERI_CLOCK_CTL0 for the details of bit fields.
PERI_CLOCK_CTL21	0x40010C54	Clock control register. See PERI_CLOCK_CTL0 for the details of bit fields.
PERI_CLOCK_CTL22	0x40010C58	Clock control register. See PERI_CLOCK_CTL0 for the details of bit fields.
PERI_CLOCK_CTL23	0x40010C5C	Clock control register. See PERI_CLOCK_CTL0 for the details of bit fields.
PERI_CLOCK_CTL24	0x40010C60	Clock control register. See PERI_CLOCK_CTL0 for the details of bit fields.
PERI_CLOCK_CTL25	0x40010C64	Clock control register. See PERI_CLOCK_CTL0 for the details of bit fields.
PERI_CLOCK_CTL26	0x40010C68	Clock control register. See PERI_CLOCK_CTL0 for the details of bit fields.
PERI_CLOCK_CTL27	0x40010C6C	Clock control register. See PERI_CLOCK_CTL0 for the details of bit fields.
PERI_CLOCK_CTL28	0x40010C70	Clock control register. See PERI_CLOCK_CTL0 for the details of bit fields.
PERI_CLOCK_CTL29	0x40010C74	Clock control register. See PERI_CLOCK_CTL0 for the details of bit fields.
PERI_CLOCK_CTL30	0x40010C78	Clock control register. See PERI_CLOCK_CTL0 for the details of bit fields.
PERI_CLOCK_CTL31	0x40010C7C	Clock control register. See PERI_CLOCK_CTL0 for the details of bit fields.
PERI_CLOCK_CTL32	0x40010C80	Clock control register. See PERI_CLOCK_CTL0 for the details of bit fields.
PERI_CLOCK_CTL33	0x40010C84	Clock control register. See PERI_CLOCK_CTL0 for the details of bit fields.
PERI_CLOCK_CTL34	0x40010C88	Clock control register. See PERI_CLOCK_CTL0 for the details of bit fields.
PERI_CLOCK_CTL35	0x40010C8C	Clock control register. See PERI_CLOCK_CTL0 for the details of bit fields.
PERI_CLOCK_CTL36	0x40010C90	Clock control register. See PERI_CLOCK_CTL0 for the details of bit fields.
PERI_CLOCK_CTL37	0x40010C94	Clock control register. See PERI_CLOCK_CTL0 for the details of bit fields.
PERI_CLOCK_CTL38	0x40010C98	Clock control register. See PERI_CLOCK_CTL0 for the details of bit fields.
PERI_CLOCK_CTL39	0x40010C9C	Clock control register. See PERI_CLOCK_CTL0 for the details of bit fields.
PERI_CLOCK_CTL40	0x40010CA0	Clock control register. See PERI_CLOCK_CTL0 for the details of bit fields.
PERI_CLOCK_CTL41	0x40010CA4	Clock control register. See PERI_CLOCK_CTL0 for the details of bit fields.
PERI_CLOCK_CTL42	0x40010CA8	Clock control register. See PERI_CLOCK_CTL0 for the details of bit fields.
PERI_CLOCK_CTL43	0x40010CAC	Clock control register. See PERI_CLOCK_CTL0 for the details of bit fields.
PERI_CLOCK_CTL44	0x40010CB0	Clock control register. See PERI_CLOCK_CTL0 for the details of bit fields.
PERI_CLOCK_CTL45	0x40010CB4	Clock control register. See PERI_CLOCK_CTL0 for the details of bit fields.
PERI_CLOCK_CTL46	0x40010CB8	Clock control register. See PERI_CLOCK_CTL0 for the details of bit fields.
PERI_CLOCK_CTL47	0x40010CBC	Clock control register. See PERI_CLOCK_CTL0 for the details of bit fields.
PERI_CLOCK_CTL48	0x40010CC0	Clock control register. See PERI_CLOCK_CTL0 for the details of bit fields.

Register	Address	Description
PERI_CLOCK_CTL49	0x40010CC4	Clock control register. See PERI_CLOCK_CTL0 for the details of bit fields.
PERI_CLOCK_CTL50	0x40010CC8	Clock control register. See PERI_CLOCK_CTL0 for the details of bit fields.
PERI_CLOCK_CTL51	0x40010CCC	Clock control register. See PERI_CLOCK_CTL0 for the details of bit fields.
PERI_CLOCK_CTL52	0x40010CD0	Clock control register. See PERI_CLOCK_CTL0 for the details of bit fields.
PERI_CLOCK_CTL53	0x40010CD4	Clock control register. See PERI_CLOCK_CTL0 for the details of bit fields.
PERI_CLOCK_CTL54	0x40010CD8	Clock control register. See PERI_CLOCK_CTL0 for the details of bit fields.
PERI_CLOCK_CTL55	0x40010CDC	Clock control register. See PERI_CLOCK_CTL0 for the details of bit fields.
PERI_CLOCK_CTL56	0x40010CE0	Clock control register. See PERI_CLOCK_CTL0 for the details of bit fields.
PERI_CLOCK_CTL57	0x40010CE4	Clock control register. See PERI_CLOCK_CTL0 for the details of bit fields.
PERI_CLOCK_CTL58	0x40010CE8	Clock control register. See PERI_CLOCK_CTL0 for the details of bit fields.
PERI_TR_CMD	0x40011000	Trigger command register
PERI_TR_GR0_TR_OUT_CTL0	0x40012000	Trigger control register
PERI_TR_GR0_TR_OUT_CTL1	0x40012004	Trigger control register. See PERI_TR_GR0_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR0_TR_OUT_CTL2	0x40012008	Trigger control register. See PERI_TR_GR0_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR0_TR_OUT_CTL3	0x4001200C	Trigger control register. See PERI_TR_GR0_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR0_TR_OUT_CTL4	0x40012010	Trigger control register. See PERI_TR_GR0_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR0_TR_OUT_CTL5	0x40012014	Trigger control register. See PERI_TR_GR0_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR0_TR_OUT_CTL6	0x40012018	Trigger control register. See PERI_TR_GR0_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR0_TR_OUT_CTL7	0x4001201C	Trigger control register. See PERI_TR_GR0_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR0_TR_OUT_CTL8	0x40012020	Trigger control register. See PERI_TR_GR0_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR0_TR_OUT_CTL9	0x40012024	Trigger control register. See PERI_TR_GR0_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR0_TR_OUT_CTL10	0x40012028	Trigger control register. See PERI_TR_GR0_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR0_TR_OUT_CTL11	0x4001202C	Trigger control register. See PERI_TR_GR0_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR0_TR_OUT_CTL12	0x40012030	Trigger control register. See PERI_TR_GR0_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR0_TR_OUT_CTL13	0x40012034	Trigger control register. See PERI_TR_GR0_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR0_TR_OUT_CTL14	0x40012038	Trigger control register. See PERI_TR_GR0_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR0_TR_OUT_CTL15	0x4001203C	Trigger control register. See PERI_TR_GR0_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR1_TR_OUT_CTL0	0x40012200	Trigger control register. See PERI_TR_GR0_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR1_TR_OUT_CTL1	0x40012204	Trigger control register. See PERI_TR_GR0_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR1_TR_OUT_CTL2	0x40012208	Trigger control register. See PERI_TR_GR0_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR1_TR_OUT_CTL3	0x4001220C	Trigger control register. See PERI_TR_GR0_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR1_TR_OUT_CTL4	0x40012210	Trigger control register. See PERI_TR_GR0_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR1_TR_OUT_CTL5	0x40012214	Trigger control register. See PERI_TR_GR0_TR_OUT_CTL0 for the details of bit fields.

Register	Address	Description
PERI_TR_GR1_TR_OUT_CTL6	0x40012218	Trigger control register. See PERI_TR_GR0_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR1_TR_OUT_CTL7	0x4001221C	Trigger control register. See PERI_TR_GR0_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR1_TR_OUT_CTL8	0x40012220	Trigger control register. See PERI_TR_GR0_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR1_TR_OUT_CTL9	0x40012224	Trigger control register. See PERI_TR_GR0_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR1_TR_OUT_CTL10	0x40012228	Trigger control register. See PERI_TR_GR0_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR1_TR_OUT_CTL11	0x4001222C	Trigger control register. See PERI_TR_GR0_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR1_TR_OUT_CTL12	0x40012230	Trigger control register. See PERI_TR_GR0_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR1_TR_OUT_CTL13	0x40012234	Trigger control register. See PERI_TR_GR0_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR1_TR_OUT_CTL14	0x40012238	Trigger control register. See PERI_TR_GR0_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR1_TR_OUT_CTL15	0x4001223C	Trigger control register. See PERI_TR_GR0_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR2_TR_OUT_CTL0	0x40012400	Trigger control register
PERI_TR_GR2_TR_OUT_CTL1	0x40012404	Trigger control register. See PERI_TR_GR2_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR2_TR_OUT_CTL2	0x40012408	Trigger control register. See PERI_TR_GR2_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR2_TR_OUT_CTL3	0x4001240C	Trigger control register. See PERI_TR_GR2_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR2_TR_OUT_CTL4	0x40012410	Trigger control register. See PERI_TR_GR2_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR2_TR_OUT_CTL5	0x40012414	Trigger control register. See PERI_TR_GR2_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR2_TR_OUT_CTL6	0x40012418	Trigger control register. See PERI_TR_GR2_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR2_TR_OUT_CTL7	0x4001241C	Trigger control register. See PERI_TR_GR2_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR2_TR_OUT_CTL8	0x40012420	Trigger control register. See PERI_TR_GR2_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR2_TR_OUT_CTL9	0x40012424	Trigger control register. See PERI_TR_GR2_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR2_TR_OUT_CTL10	0x40012428	Trigger control register. See PERI_TR_GR2_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR2_TR_OUT_CTL11	0x4001242C	Trigger control register. See PERI_TR_GR2_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR2_TR_OUT_CTL12	0x40012430	Trigger control register. See PERI_TR_GR2_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR2_TR_OUT_CTL13	0x40012434	Trigger control register. See PERI_TR_GR2_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR3_TR_OUT_CTL0	0x40012600	Trigger control register. See PERI_TR_GR2_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR3_TR_OUT_CTL1	0x40012604	Trigger control register. See PERI_TR_GR2_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR3_TR_OUT_CTL2	0x40012608	Trigger control register. See PERI_TR_GR2_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR3_TR_OUT_CTL3	0x4001260C	Trigger control register. See PERI_TR_GR2_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR3_TR_OUT_CTL4	0x40012610	Trigger control register. See PERI_TR_GR2_TR_OUT_CTL0 for the details of bit fields.

Register	Address	Description
PERI_TR_GR3_TR_OUT_CTL5	0x40012614	Trigger control register. See PERI_TR_GR2_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR3_TR_OUT_CTL6	0x40012618	Trigger control register. See PERI_TR_GR2_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR3_TR_OUT_CTL7	0x4001261C	Trigger control register. See PERI_TR_GR2_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR3_TR_OUT_CTL8	0x40012620	Trigger control register. See PERI_TR_GR2_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR3_TR_OUT_CTL9	0x40012624	Trigger control register. See PERI_TR_GR2_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR3_TR_OUT_CTL10	0x40012628	Trigger control register. See PERI_TR_GR2_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR3_TR_OUT_CTL11	0x4001262C	Trigger control register. See PERI_TR_GR2_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR3_TR_OUT_CTL12	0x40012630	Trigger control register. See PERI_TR_GR2_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR3_TR_OUT_CTL13	0x40012634	Trigger control register. See PERI_TR_GR2_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR4_TR_OUT_CTL0	0x40012800	Trigger control register
PERI_TR_GR4_TR_OUT_CTL1	0x40012804	Trigger control register. See PERI_TR_GR4_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR5_TR_OUT_CTL0	0x40012A00	Trigger control register. See PERI_TR_GR4_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR5_TR_OUT_CTL1	0x40012A04	Trigger control register. See PERI_TR_GR4_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR6_TR_OUT_CTL0	0x40012C00	Trigger control register
PERI_TR_GR7_TR_OUT_CTL0	0x40012E00	Trigger control register. See PERI_TR_GR4_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR7_TR_OUT_CTL1	0x40012E04	Trigger control register. See PERI_TR_GR4_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR8_TR_OUT_CTL0	0x40013000	Trigger control register. See PERI_TR_GR4_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR8_TR_OUT_CTL1	0x40013004	Trigger control register. See PERI_TR_GR4_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR9_TR_OUT_CTL0	0x40013200	Trigger control register
PERI_TR_GR9_TR_OUT_CTL1	0x40013204	Trigger control register. See PERI_TR_GR9_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR9_TR_OUT_CTL2	0x40013208	Trigger control register. See PERI_TR_GR9_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR9_TR_OUT_CTL3	0x4001320C	Trigger control register. See PERI_TR_GR9_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR9_TR_OUT_CTL4	0x40013210	Trigger control register. See PERI_TR_GR9_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR9_TR_OUT_CTL5	0x40013214	Trigger control register. See PERI_TR_GR9_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR9_TR_OUT_CTL6	0x40013218	Trigger control register. See PERI_TR_GR9_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR9_TR_OUT_CTL7	0x4001321C	Trigger control register. See PERI_TR_GR9_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR10_TR_OUT_CTL0	0x40013400	Trigger control register. See PERI_TR_GR9_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR10_TR_OUT_CTL1	0x40013404	Trigger control register. See PERI_TR_GR9_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR10_TR_OUT_CTL2	0x40013408	Trigger control register. See PERI_TR_GR9_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR10_TR_OUT_CTL3	0x4001340C	Trigger control register. See PERI_TR_GR9_TR_OUT_CTL0 for the details of bit fields.

Register	Address	Description
PERI_TR_GR10_TR_OUT_CTL4	0x40013410	Trigger control register. See PERI_TR_GR9_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR10_TR_OUT_CTL5	0x40013414	Trigger control register. See PERI_TR_GR9_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR10_TR_OUT_CTL6	0x40013418	Trigger control register. See PERI_TR_GR9_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR10_TR_OUT_CTL7	0x4001341C	Trigger control register. See PERI_TR_GR9_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR11_TR_OUT_CTL0	0x40013600	Trigger control register
PERI_TR_GR11_TR_OUT_CTL1	0x40013604	Trigger control register. See PERI_TR_GR11_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR11_TR_OUT_CTL2	0x40013608	Trigger control register. See PERI_TR_GR11_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR11_TR_OUT_CTL3	0x4001360C	Trigger control register. See PERI_TR_GR11_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR11_TR_OUT_CTL4	0x40013610	Trigger control register. See PERI_TR_GR11_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR11_TR_OUT_CTL5	0x40013614	Trigger control register. See PERI_TR_GR11_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR11_TR_OUT_CTL6	0x40013618	Trigger control register. See PERI_TR_GR11_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR11_TR_OUT_CTL7	0x4001361C	Trigger control register. See PERI_TR_GR11_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR11_TR_OUT_CTL8	0x40013620	Trigger control register. See PERI_TR_GR11_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR11_TR_OUT_CTL9	0x40013624	Trigger control register. See PERI_TR_GR11_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR11_TR_OUT_CTL10	0x40013628	Trigger control register. See PERI_TR_GR11_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR11_TR_OUT_CTL11	0x4001362C	Trigger control register. See PERI_TR_GR11_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR11_TR_OUT_CTL12	0x40013630	Trigger control register. See PERI_TR_GR11_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR11_TR_OUT_CTL13	0x40013634	Trigger control register. See PERI_TR_GR11_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR11_TR_OUT_CTL14	0x40013638	Trigger control register. See PERI_TR_GR11_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR11_TR_OUT_CTL15	0x4001363C	Trigger control register. See PERI_TR_GR11_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR12_TR_OUT_CTL0	0x40013800	Trigger control register
PERI_TR_GR12_TR_OUT_CTL1	0x40013804	Trigger control register. See PERI_TR_GR12_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR12_TR_OUT_CTL2	0x40013808	Trigger control register. See PERI_TR_GR12_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR12_TR_OUT_CTL3	0x4001380C	Trigger control register. See PERI_TR_GR12_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR12_TR_OUT_CTL4	0x40013810	Trigger control register. See PERI_TR_GR12_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR12_TR_OUT_CTL5	0x40013814	Trigger control register. See PERI_TR_GR12_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR12_TR_OUT_CTL6	0x40013818	Trigger control register. See PERI_TR_GR12_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR12_TR_OUT_CTL7	0x4001381C	Trigger control register. See PERI_TR_GR12_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR12_TR_OUT_CTL8	0x40013820	Trigger control register. See PERI_TR_GR12_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR12_TR_OUT_CTL9	0x40013824	Trigger control register. See PERI_TR_GR12_TR_OUT_CTL0 for the details of bit fields.

Register	Address	Description
PERI_TR_GR13_TR_OUT_CTL0	0x40013A00	Trigger control register
PERI_TR_GR13_TR_OUT_CTL1	0x40013A04	Trigger control register. See PERI_TR_GR13_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR13_TR_OUT_CTL2	0x40013A08	Trigger control register. See PERI_TR_GR13_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR13_TR_OUT_CTL3	0x40013A0C	Trigger control register. See PERI_TR_GR13_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR13_TR_OUT_CTL4	0x40013A10	Trigger control register. See PERI_TR_GR13_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR13_TR_OUT_CTL5	0x40013A14	Trigger control register. See PERI_TR_GR13_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR13_TR_OUT_CTL6	0x40013A18	Trigger control register. See PERI_TR_GR13_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR13_TR_OUT_CTL7	0x40013A1C	Trigger control register. See PERI_TR_GR13_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR13_TR_OUT_CTL8	0x40013A20	Trigger control register. See PERI_TR_GR13_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR13_TR_OUT_CTL9	0x40013A24	Trigger control register. See PERI_TR_GR13_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR13_TR_OUT_CTL10	0x40013A28	Trigger control register. See PERI_TR_GR13_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR13_TR_OUT_CTL11	0x40013A2C	Trigger control register. See PERI_TR_GR13_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR13_TR_OUT_CTL12	0x40013A30	Trigger control register. See PERI_TR_GR13_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR13_TR_OUT_CTL13	0x40013A34	Trigger control register. See PERI_TR_GR13_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR13_TR_OUT_CTL14	0x40013A38	Trigger control register. See PERI_TR_GR13_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR13_TR_OUT_CTL15	0x40013A3C	Trigger control register. See PERI_TR_GR13_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR13_TR_OUT_CTL16	0x40013A40	Trigger control register. See PERI_TR_GR13_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR13_TR_OUT_CTL17	0x40013A44	Trigger control register. See PERI_TR_GR13_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR14_TR_OUT_CTL0	0x40013C00	Trigger control register
PERI_TR_GR14_TR_OUT_CTL1	0x40013C04	Trigger control register. See PERI_TR_GR14_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR14_TR_OUT_CTL2	0x40013C08	Trigger control register. See PERI_TR_GR14_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR14_TR_OUT_CTL3	0x40013C0C	Trigger control register. See PERI_TR_GR14_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR14_TR_OUT_CTL4	0x40013C10	Trigger control register. See PERI_TR_GR14_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR14_TR_OUT_CTL5	0x40013C14	Trigger control register. See PERI_TR_GR14_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR14_TR_OUT_CTL6	0x40013C18	Trigger control register. See PERI_TR_GR14_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR14_TR_OUT_CTL7	0x40013C1C	Trigger control register. See PERI_TR_GR14_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR14_TR_OUT_CTL8	0x40013C20	Trigger control register. See PERI_TR_GR14_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR14_TR_OUT_CTL9	0x40013C24	Trigger control register. See PERI_TR_GR14_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR14_TR_OUT_CTL10	0x40013C28	Trigger control register. See PERI_TR_GR14_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR14_TR_OUT_CTL11	0x40013C2C	Trigger control register. See PERI_TR_GR14_TR_OUT_CTL0 for the details of bit fields.

Register	Address	Description
PERI_TR_GR14_TR_OUT_CTL12	0x40013C30	Trigger control register. See PERI_TR_GR14_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR14_TR_OUT_CTL13	0x40013C34	Trigger control register. See PERI_TR_GR14_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR14_TR_OUT_CTL14	0x40013C38	Trigger control register. See PERI_TR_GR14_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GR14_TR_OUT_CTL15	0x40013C3C	Trigger control register. See PERI_TR_GR14_TR_OUT_CTL0 for the details of bit fields.
PERI_PPU_PR0_ADDR0	0x40014000	PPU region address 0 (slave structure)
PERI_PPU_PR0_ATT0	0x40014004	PPU region attributes 0 (slave structure)
PERI_PPU_PR0_ADDR1	0x40014020	PPU region address 1 (master structure)
PERI_PPU_PR0_ATT1	0x40014024	PPU region attributes 1 (master structure)
PERI_PPU_PR1_ADDR0	0x40014040	PPU region address 0 (slave structure). See PERI_PPU_PR0_ADDR0 for the details of bit fields.
PERI_PPU_PR1_ATT0	0x40014044	PPU region attributes 0 (slave structure). See PERI_PPU_PR0_ATT0 for the details of bit fields.
PERI_PPU_PR1_ADDR1	0x40014060	PPU region address 1 (master structure)
PERI_PPU_PR1_ATT1	0x40014064	PPU region attributes 1 (master structure). See PERI_PPU_PR0_ATT1 for the details of bit fields.
PERI_PPU_PR2_ADDR0	0x40014080	PPU region address 0 (slave structure). See PERI_PPU_PR0_ADDR0 for the details of bit fields.
PERI_PPU_PR2_ATT0	0x40014084	PPU region attributes 0 (slave structure). See PERI_PPU_PR0_ATT0 for the details of bit fields.
PERI_PPU_PR2_ADDR1	0x400140A0	PPU region address 1 (master structure)
PERI_PPU_PR2_ATT1	0x400140A4	PPU region attributes 1 (master structure). See PERI_PPU_PR0_ATT1 for the details of bit fields.
PERI_PPU_PR3_ADDR0	0x400140C0	PPU region address 0 (slave structure). See PERI_PPU_PR0_ADDR0 for the details of bit fields.
PERI_PPU_PR3_ATT0	0x400140C4	PPU region attributes 0 (slave structure). See PERI_PPU_PR0_ATT0 for the details of bit fields.
PERI_PPU_PR3_ADDR1	0x400140E0	PPU region address 1 (master structure)
PERI_PPU_PR3_ATT1	0x400140E4	PPU region attributes 1 (master structure). See PERI_PPU_PR0_ATT1 for the details of bit fields.
PERI_PPU_PR4_ADDR0	0x40014100	PPU region address 0 (slave structure). See PERI_PPU_PR0_ADDR0 for the details of bit fields.
PERI_PPU_PR4_ATT0	0x40014104	PPU region attributes 0 (slave structure). See PERI_PPU_PR0_ATT0 for the details of bit fields.
PERI_PPU_PR4_ADDR1	0x40014120	PPU region address 1 (master structure)
PERI_PPU_PR4_ATT1	0x40014124	PPU region attributes 1 (master structure). See PERI_PPU_PR0_ATT1 for the details of bit fields.
PERI_PPU_PR5_ADDR0	0x40014140	PPU region address 0 (slave structure). See PERI_PPU_PR0_ADDR0 for the details of bit fields.
PERI_PPU_PR5_ATT0	0x40014144	PPU region attributes 0 (slave structure). See PERI_PPU_PR0_ATT0 for the details of bit fields.
PERI_PPU_PR5_ADDR1	0x40014160	PPU region address 1 (master structure)
PERI_PPU_PR5_ATT1	0x40014164	PPU region attributes 1 (master structure). See PERI_PPU_PR0_ATT1 for the details of bit fields.
PERI_PPU_PR6_ADDR0	0x40014180	PPU region address 0 (slave structure). See PERI_PPU_PR0_ADDR0 for the details of bit fields.
PERI_PPU_PR6_ATT0	0x40014184	PPU region attributes 0 (slave structure). See PERI_PPU_PR0_ATT0 for the details of bit fields.
PERI_PPU_PR6_ADDR1	0x400141A0	PPU region address 1 (master structure)
PERI_PPU_PR6_ATT1	0x400141A4	PPU region attributes 1 (master structure). See PERI_PPU_PR0_ATT1 for the details of bit fields.

Register	Address	Description
PERI_PPU_PR7_ADDR0	0x400141C0	PPU region address 0 (slave structure). See PERI_PPU_PR0_ADDR0 for the details of bit fields.
PERI_PPU_PR7_ATT0	0x400141C4	PPU region attributes 0 (slave structure). See PERI_PPU_PR0_ATT0 for the details of bit fields.
PERI_PPU_PR7_ADDR1	0x400141E0	PPU region address 1 (master structure)
PERI_PPU_PR7_ATT1	0x400141E4	PPU region attributes 1 (master structure). See PERI_PPU_PR0_ATT1 for the details of bit fields.
PERI_PPU_PR8_ADDR0	0x40014200	PPU region address 0 (slave structure). See PERI_PPU_PR0_ADDR0 for the details of bit fields.
PERI_PPU_PR8_ATT0	0x40014204	PPU region attributes 0 (slave structure). See PERI_PPU_PR0_ATT0 for the details of bit fields.
PERI_PPU_PR8_ADDR1	0x40014220	PPU region address 1 (master structure)
PERI_PPU_PR8_ATT1	0x40014224	PPU region attributes 1 (master structure). See PERI_PPU_PR0_ATT1 for the details of bit fields.
PERI_PPU_PR9_ADDR0	0x40014240	PPU region address 0 (slave structure). See PERI_PPU_PR0_ADDR0 for the details of bit fields.
PERI_PPU_PR9_ATT0	0x40014244	PPU region attributes 0 (slave structure). See PERI_PPU_PR0_ATT0 for the details of bit fields.
PERI_PPU_PR9_ADDR1	0x40014260	PPU region address 1 (master structure)
PERI_PPU_PR9_ATT1	0x40014264	PPU region attributes 1 (master structure). See PERI_PPU_PR0_ATT1 for the details of bit fields.
PERI_PPU_PR10_ADDR0	0x40014280	PPU region address 0 (slave structure). See PERI_PPU_PR0_ADDR0 for the details of bit fields.
PERI_PPU_PR10_ATT0	0x40014284	PPU region attributes 0 (slave structure). See PERI_PPU_PR0_ATT0 for the details of bit fields.
PERI_PPU_PR10_ADDR1	0x400142A0	PPU region address 1 (master structure)
PERI_PPU_PR10_ATT1	0x400142A4	PPU region attributes 1 (master structure). See PERI_PPU_PR0_ATT1 for the details of bit fields.
PERI_PPU_PR11_ADDR0	0x400142C0	PPU region address 0 (slave structure). See PERI_PPU_PR0_ADDR0 for the details of bit fields.
PERI_PPU_PR11_ATT0	0x400142C4	PPU region attributes 0 (slave structure). See PERI_PPU_PR0_ATT0 for the details of bit fields.
PERI_PPU_PR11_ADDR1	0x400142E0	PPU region address 1 (master structure)
PERI_PPU_PR11_ATT1	0x400142E4	PPU region attributes 1 (master structure). See PERI_PPU_PR0_ATT1 for the details of bit fields.
PERI_PPU_PR12_ADDR0	0x40014300	PPU region address 0 (slave structure). See PERI_PPU_PR0_ADDR0 for the details of bit fields.
PERI_PPU_PR12_ATT0	0x40014304	PPU region attributes 0 (slave structure). See PERI_PPU_PR0_ATT0 for the details of bit fields.
PERI_PPU_PR12_ADDR1	0x40014320	PPU region address 1 (master structure)
PERI_PPU_PR12_ATT1	0x40014324	PPU region attributes 1 (master structure). See PERI_PPU_PR0_ATT1 for the details of bit fields.
PERI_PPU_PR13_ADDR0	0x40014340	PPU region address 0 (slave structure). See PERI_PPU_PR0_ADDR0 for the details of bit fields.
PERI_PPU_PR13_ATT0	0x40014344	PPU region attributes 0 (slave structure). See PERI_PPU_PR0_ATT0 for the details of bit fields.
PERI_PPU_PR13_ADDR1	0x40014360	PPU region address 1 (master structure)
PERI_PPU_PR13_ATT1	0x40014364	PPU region attributes 1 (master structure). See PERI_PPU_PR0_ATT1 for the details of bit fields.
PERI_PPU_PR14_ADDR0	0x40014380	PPU region address 0 (slave structure). See PERI_PPU_PR0_ADDR0 for the details of bit fields.
PERI_PPU_PR14_ATT0	0x40014384	PPU region attributes 0 (slave structure). See PERI_PPU_PR0_ATT0 for the details of bit fields.
PERI_PPU_PR14_ADDR1	0x400143A0	PPU region address 1 (master structure)

Register	Address	Description
PERI_PPU_PR14_ATT1	0x400143A4	PPU region attributes 1 (master structure). See PERI_PPU_PR0_ATT1 for the details of bit fields.
PERI_PPU_PR15_ADDR0	0x400143C0	PPU region address 0 (slave structure). See PERI_PPU_PR0_ADDR0 for the details of bit fields.
PERI_PPU_PR15_ATT0	0x400143C4	PPU region attributes 0 (slave structure). See PERI_PPU_PR0_ATT0 for the details of bit fields.
PERI_PPU_PR15_ADDR1	0x400143E0	PPU region address 1 (master structure)
PERI_PPU_PR15_ATT1	0x400143E4	PPU region attributes 1 (master structure). See PERI_PPU_PR0_ATT1 for the details of bit fields.
PERI_PPU_GR0_ADDR0	0x40015000	PPU region address 0 (slave structure)
PERI_PPU_GR0_ATT0	0x40015004	PPU region attributes 0 (slave structure)
PERI_PPU_GR0_ADDR1	0x40015020	PPU region address 1 (master structure)
PERI_PPU_GR0_ATT1	0x40015024	PPU region attributes 1 (master structure)
PERI_PPU_GR1_ADDR0	0x40015040	PPU region address 0 (slave structure)
PERI_PPU_GR1_ATT0	0x40015044	PPU region attributes 0 (slave structure). See PERI_PPU_GR0_ATT0 for the details of bit fields.
PERI_PPU_GR1_ADDR1	0x40015060	PPU region address 1 (master structure)
PERI_PPU_GR1_ATT1	0x40015064	PPU region attributes 1 (master structure). See PERI_PPU_GR0_ATT1 for the details of bit fields.
PERI_PPU_GR2_ADDR0	0x40015080	PPU region address 0 (slave structure)
PERI_PPU_GR2_ATT0	0x40015084	PPU region attributes 0 (slave structure). See PERI_PPU_GR0_ATT0 for the details of bit fields.
PERI_PPU_GR2_ADDR1	0x400150A0	PPU region address 1 (master structure)
PERI_PPU_GR2_ATT1	0x400150A4	PPU region attributes 1 (master structure). See PERI_PPU_GR0_ATT1 for the details of bit fields.
PERI_PPU_GR3_ADDR0	0x400150C0	PPU region address 0 (slave structure)
PERI_PPU_GR3_ATT0	0x400150C4	PPU region attributes 0 (slave structure). See PERI_PPU_GR0_ATT0 for the details of bit fields.
PERI_PPU_GR3_ADDR1	0x400150E0	PPU region address 1 (master structure)
PERI_PPU_GR3_ATT1	0x400150E4	PPU region attributes 1 (master structure). See PERI_PPU_GR0_ATT1 for the details of bit fields.
PERI_PPU_GR4_ADDR0	0x40015100	PPU region address 0 (slave structure)
PERI_PPU_GR4_ATT0	0x40015104	PPU region attributes 0 (slave structure). See PERI_PPU_GR0_ATT0 for the details of bit fields.
PERI_PPU_GR4_ADDR1	0x40015120	PPU region address 1 (master structure)
PERI_PPU_GR4_ATT1	0x40015124	PPU region attributes 1 (master structure). See PERI_PPU_GR0_ATT1 for the details of bit fields.
PERI_PPU_GR6_ADDR0	0x40015180	PPU region address 0 (slave structure)
PERI_PPU_GR6_ATT0	0x40015184	PPU region attributes 0 (slave structure). See PERI_PPU_GR0_ATT0 for the details of bit fields.
PERI_PPU_GR6_ADDR1	0x400151A0	PPU region address 1 (master structure)
PERI_PPU_GR6_ATT1	0x400151A4	PPU region attributes 1 (master structure). See PERI_PPU_GR0_ATT1 for the details of bit fields.
PERI_PPU_GR9_ADDR0	0x40015240	PPU region address 0 (slave structure)
PERI_PPU_GR9_ATT0	0x40015244	PPU region attributes 0 (slave structure)
PERI_PPU_GR9_ADDR1	0x40015260	PPU region address 1 (master structure)
PERI_PPU_GR9_ATT1	0x40015264	PPU region attributes 1 (master structure). See PERI_PPU_GR0_ATT1 for the details of bit fields.
PERI_PPU_GR10_ADDR0	0x40015280	PPU region address 0 (slave structure)
PERI_PPU_GR10_ATT0	0x40015284	PPU region attributes 0 (slave structure). See PERI_PPU_GR0_ATT0 for the details of bit fields.

Register	Address	Description
PERI_PPU_GR10_ADDR1	0x400152A0	PPU region address 1 (master structure)
PERI_PPU_GR10_ATT1	0x400152A4	PPU region attributes 1 (master structure). See PERI_PPU_GR0_ATT1 for the details of bit fields.
PERI_GR1_PPU_SL0_ADDR0	0x40100000	PPU region address 0 (slave structure)
PERI_GR1_PPU_SL0_ATT0	0x40100004	PPU region attributes 0 (slave structure)
PERI_GR1_PPU_SL0_ADDR1	0x40100020	PPU region address 1 (master structure)
PERI_GR1_PPU_SL0_ATT1	0x40100024	PPU region attributes 1 (master structure)
PERI_GR1_PPU_SL1_ADDR0	0x40100040	PPU region address 0 (slave structure)
PERI_GR1_PPU_SL1_ATT0	0x40100044	PPU region attributes 0 (slave structure). See PERI_GR1_PPU_SL0_ATT0 for the details of bit fields.
PERI_GR1_PPU_SL1_ADDR1	0x40100060	PPU region address 1 (master structure)
PERI_GR1_PPU_SL1_ATT1	0x40100064	PPU region attributes 1 (master structure). See PERI_GR1_PPU_SL0_ATT1 for the details of bit fields.
PERI_GR2_PPU_SL0_ADDR0	0x40200000	PPU region address 0 (slave structure)
PERI_GR2_PPU_SL0_ATT0	0x40200004	PPU region attributes 0 (slave structure). See PERI_GR1_PPU_SL0_ATT0 for the details of bit fields.
PERI_GR2_PPU_SL0_ADDR1	0x40200020	PPU region address 1 (master structure)
PERI_GR2_PPU_SL0_ATT1	0x40200024	PPU region attributes 1 (master structure). See PERI_GR1_PPU_SL0_ATT1 for the details of bit fields.
PERI_GR2_PPU_SL1_ADDR0	0x40200040	PPU region address 0 (slave structure)
PERI_GR2_PPU_SL1_ATT0	0x40200044	PPU region attributes 0 (slave structure). See PERI_GR1_PPU_SL0_ATT0 for the details of bit fields.
PERI_GR2_PPU_SL1_ADDR1	0x40200060	PPU region address 1 (master structure)
PERI_GR2_PPU_SL1_ATT1	0x40200064	PPU region attributes 1 (master structure). See PERI_GR1_PPU_SL0_ATT1 for the details of bit fields.
PERI_GR2_PPU_SL2_ADDR0	0x40200080	PPU region address 0 (slave structure)
PERI_GR2_PPU_SL2_ATT0	0x40200084	PPU region attributes 0 (slave structure). See PERI_GR1_PPU_SL0_ATT0 for the details of bit fields.
PERI_GR2_PPU_SL2_ADDR1	0x402000A0	PPU region address 1 (master structure)
PERI_GR2_PPU_SL2_ATT1	0x402000A4	PPU region attributes 1 (master structure). See PERI_GR1_PPU_SL0_ATT1 for the details of bit fields.
PERI_GR2_PPU_SL3_ADDR0	0x402000C0	PPU region address 0 (slave structure)
PERI_GR2_PPU_SL3_ATT0	0x402000C4	PPU region attributes 0 (slave structure). See PERI_GR1_PPU_SL0_ATT0 for the details of bit fields.
PERI_GR2_PPU_SL3_ADDR1	0x402000E0	PPU region address 1 (master structure)
PERI_GR2_PPU_SL3_ATT1	0x402000E4	PPU region attributes 1 (master structure). See PERI_GR1_PPU_SL0_ATT1 for the details of bit fields.
PERI_GR2_PPU_SL4_ADDR0	0x40200100	PPU region address 0 (slave structure)
PERI_GR2_PPU_SL4_ATT0	0x40200104	PPU region attributes 0 (slave structure). See PERI_GR1_PPU_SL0_ATT0 for the details of bit fields.
PERI_GR2_PPU_SL4_ADDR1	0x40200120	PPU region address 1 (master structure)
PERI_GR2_PPU_SL4_ATT1	0x40200124	PPU region attributes 1 (master structure). See PERI_GR1_PPU_SL0_ATT1 for the details of bit fields.
PERI_GR2_PPU_SL5_ADDR0	0x40200140	PPU region address 0 (slave structure)
PERI_GR2_PPU_SL5_ATT0	0x40200144	PPU region attributes 0 (slave structure). See PERI_GR1_PPU_SL0_ATT0 for the details of bit fields.
PERI_GR2_PPU_SL5_ADDR1	0x40200160	PPU region address 1 (master structure)
PERI_GR2_PPU_SL5_ATT1	0x40200164	PPU region attributes 1 (master structure). See PERI_GR1_PPU_SL0_ATT1 for the details of bit fields.
PERI_GR2_PPU_SL6_ADDR0	0x40200180	PPU region address 0 (slave structure)

Register	Address	Description
PERI_GR2_PPU_SL6_ATT0	0x40200184	PPU region attributes 0 (slave structure). See PERI_GR1_PPU_SL0_ATT0 for the details of bit fields.
PERI_GR2_PPU_SL6_ADDR1	0x402001A0	PPU region address 1 (master structure)
PERI_GR2_PPU_SL6_ATT1	0x402001A4	PPU region attributes 1 (master structure). See PERI_GR1_PPU_SL0_ATT1 for the details of bit fields.
PERI_GR2_PPU_SL7_ADDR0	0x402001C0	PPU region address 0 (slave structure)
PERI_GR2_PPU_SL7_ATT0	0x402001C4	PPU region attributes 0 (slave structure). See PERI_GR1_PPU_SL0_ATT0 for the details of bit fields.
PERI_GR2_PPU_SL7_ADDR1	0x402001E0	PPU region address 1 (master structure)
PERI_GR2_PPU_SL7_ATT1	0x402001E4	PPU region attributes 1 (master structure). See PERI_GR1_PPU_SL0_ATT1 for the details of bit fields.
PERI_GR2_PPU_SL8_ADDR0	0x40200200	PPU region address 0 (slave structure)
PERI_GR2_PPU_SL8_ATT0	0x40200204	PPU region attributes 0 (slave structure)
PERI_GR2_PPU_SL8_ADDR1	0x40200220	PPU region address 1 (master structure)
PERI_GR2_PPU_SL8_ATT1	0x40200224	PPU region attributes 1 (master structure). See PERI_GR1_PPU_SL0_ATT1 for the details of bit fields.
PERI_GR2_PPU_SL9_ADDR0	0x40200240	PPU region address 0 (slave structure). See PERI_GR2_PPU_SL8_ADDR0 for the details of bit fields.
PERI_GR2_PPU_SL9_ATT0	0x40200244	PPU region attributes 0 (slave structure). See PERI_GR2_PPU_SL8_ATT0 for the details of bit fields.
PERI_GR2_PPU_SL9_ADDR1	0x40200260	PPU region address 1 (master structure)
PERI_GR2_PPU_SL9_ATT1	0x40200264	PPU region attributes 1 (master structure). See PERI_GR1_PPU_SL0_ATT1 for the details of bit fields.
PERI_GR2_PPU_SL12_ADDR0	0x40200300	PPU region address 0 (slave structure)
PERI_GR2_PPU_SL12_ATT0	0x40200304	PPU region attributes 0 (slave structure). See PERI_GR2_PPU_SL8_ATT0 for the details of bit fields.
PERI_GR2_PPU_SL12_ADDR1	0x40200320	PPU region address 1 (master structure)
PERI_GR2_PPU_SL12_ATT1	0x40200324	PPU region attributes 1 (master structure). See PERI_GR1_PPU_SL0_ATT1 for the details of bit fields.
PERI_GR2_PPU_SL13_ADDR0	0x40200340	PPU region address 0 (slave structure)
PERI_GR2_PPU_SL13_ATT0	0x40200344	PPU region attributes 0 (slave structure). See PERI_GR1_PPU_SL0_ATT0 for the details of bit fields.
PERI_GR2_PPU_SL13_ADDR1	0x40200360	PPU region address 1 (master structure)
PERI_GR2_PPU_SL13_ATT1	0x40200364	PPU region attributes 1 (master structure). See PERI_GR1_PPU_SL0_ATT1 for the details of bit fields.
PERI_GR2_PPU_RG0_ADDR0	0x40201000	PPU region address 0 (slave structure)
PERI_GR2_PPU_RG0_ATT0	0x40201004	PPU region attributes 0 (slave structure)
PERI_GR2_PPU_RG0_ADDR1	0x40201020	PPU region address 1 (master structure)
PERI_GR2_PPU_RG0_ATT1	0x40201024	PPU region attributes 1 (master structure)
PERI_GR2_PPU_RG1_ADDR0	0x40201040	PPU region address 0 (slave structure)
PERI_GR2_PPU_RG1_ATT0	0x40201044	PPU region attributes 0 (slave structure). See PERI_GR2_PPU_RG0_ATT0 for the details of bit fields.
PERI_GR2_PPU_RG1_ADDR1	0x40201060	PPU region address 1 (master structure)
PERI_GR2_PPU_RG1_ATT1	0x40201064	PPU region attributes 1 (master structure). See PERI_GR2_PPU_RG0_ATT1 for the details of bit fields.
PERI_GR2_PPU_RG2_ADDR0	0x40201080	PPU region address 0 (slave structure)
PERI_GR2_PPU_RG2_ATT0	0x40201084	PPU region attributes 0 (slave structure). See PERI_GR2_PPU_RG0_ATT0 for the details of bit fields.
PERI_GR2_PPU_RG2_ADDR1	0x402010A0	PPU region address 1 (master structure)
PERI_GR2_PPU_RG2_ATT1	0x402010A4	PPU region attributes 1 (master structure). See PERI_GR2_PPU_RG0_ATT1 for the details of bit fields.

Register	Address	Description
PERI_GR2_PPU_RG3_ADDR0	0x402010C0	PPU region address 0 (slave structure)
PERI_GR2_PPU_RG3_ATT0	0x402010C4	PPU region attributes 0 (slave structure). See PERI_GR2_PPU_RG0_ATT0 for the details of bit fields.
PERI_GR2_PPU_RG3_ADDR1	0x402010E0	PPU region address 1 (master structure)
PERI_GR2_PPU_RG3_ATT1	0x402010E4	PPU region attributes 1 (master structure). See PERI_GR2_PPU_RG0_ATT1 for the details of bit fields.
PERI_GR2_PPU_RG4_ADDR0	0x40201100	PPU region address 0 (slave structure)
PERI_GR2_PPU_RG4_ATT0	0x40201104	PPU region attributes 0 (slave structure). See PERI_GR2_PPU_RG0_ATT0 for the details of bit fields.
PERI_GR2_PPU_RG4_ADDR1	0x40201120	PPU region address 1 (master structure)
PERI_GR2_PPU_RG4_ATT1	0x40201124	PPU region attributes 1 (master structure). See PERI_GR2_PPU_RG0_ATT1 for the details of bit fields.
PERI_GR2_PPU_RG5_ADDR0	0x40201140	PPU region address 0 (slave structure)
PERI_GR2_PPU_RG5_ATT0	0x40201144	PPU region attributes 0 (slave structure). See PERI_GR2_PPU_RG0_ATT0 for the details of bit fields.
PERI_GR2_PPU_RG5_ADDR1	0x40201160	PPU region address 1 (master structure)
PERI_GR2_PPU_RG5_ATT1	0x40201164	PPU region attributes 1 (master structure). See PERI_GR2_PPU_RG0_ATT1 for the details of bit fields.
PERI_GR2_PPU_RG6_ADDR0	0x40201180	PPU region address 0 (slave structure)
PERI_GR2_PPU_RG6_ATT0	0x40201184	PPU region attributes 0 (slave structure). See PERI_GR2_PPU_RG0_ATT0 for the details of bit fields.
PERI_GR2_PPU_RG6_ADDR1	0x402011A0	PPU region address 1 (master structure)
PERI_GR2_PPU_RG6_ATT1	0x402011A4	PPU region attributes 1 (master structure). See PERI_GR2_PPU_RG0_ATT1 for the details of bit fields.
PERI_GR2_PPU_RG7_ADDR0	0x402011C0	PPU region address 0 (slave structure)
PERI_GR2_PPU_RG7_ATT0	0x402011C4	PPU region attributes 0 (slave structure). See PERI_GR2_PPU_RG0_ATT0 for the details of bit fields.
PERI_GR2_PPU_RG7_ADDR1	0x402011E0	PPU region address 1 (master structure)
PERI_GR2_PPU_RG7_ATT1	0x402011E4	PPU region attributes 1 (master structure). See PERI_GR2_PPU_RG0_ATT1 for the details of bit fields.
PERI_GR2_PPU_RG8_ADDR0	0x40201200	PPU region address 0 (slave structure)
PERI_GR2_PPU_RG8_ATT0	0x40201204	PPU region attributes 0 (slave structure). See PERI_GR2_PPU_RG0_ATT0 for the details of bit fields.
PERI_GR2_PPU_RG8_ADDR1	0x40201220	PPU region address 1 (master structure)
PERI_GR2_PPU_RG8_ATT1	0x40201224	PPU region attributes 1 (master structure). See PERI_GR2_PPU_RG0_ATT1 for the details of bit fields.
PERI_GR2_PPU_RG9_ADDR0	0x40201240	PPU region address 0 (slave structure)
PERI_GR2_PPU_RG9_ATT0	0x40201244	PPU region attributes 0 (slave structure). See PERI_GR2_PPU_RG0_ATT0 for the details of bit fields.
PERI_GR2_PPU_RG9_ADDR1	0x40201260	PPU region address 1 (master structure)
PERI_GR2_PPU_RG9_ATT1	0x40201264	PPU region attributes 1 (master structure). See PERI_GR2_PPU_RG0_ATT1 for the details of bit fields.
PERI_GR2_PPU_RG10_ADDR0	0x40201280	PPU region address 0 (slave structure)
PERI_GR2_PPU_RG10_ATT0	0x40201284	PPU region attributes 0 (slave structure). See PERI_GR2_PPU_RG0_ATT0 for the details of bit fields.
PERI_GR2_PPU_RG10_ADDR1	0x402012A0	PPU region address 1 (master structure)
PERI_GR2_PPU_RG10_ATT1	0x402012A4	PPU region attributes 1 (master structure). See PERI_GR2_PPU_RG0_ATT1 for the details of bit fields.
PERI_GR2_PPU_RG11_ADDR0	0x402012C0	PPU region address 0 (slave structure)
PERI_GR2_PPU_RG11_ATT0	0x402012C4	PPU region attributes 0 (slave structure). See PERI_GR2_PPU_RG0_ATT0 for the details of bit fields.
PERI_GR2_PPU_RG11_ADDR1	0x402012E0	PPU region address 1 (master structure)

Register	Address	Description
PERI_GR2_PPU_RG11_ATT1	0x402012E4	PPU region attributes 1 (master structure). See PERI_GR2_PPU_RG0_ATT1 for the details of bit fields.
PERI_GR2_PPU_RG12_ADDR0	0x40201300	PPU region address 0 (slave structure)
PERI_GR2_PPU_RG12_ATT0	0x40201304	PPU region attributes 0 (slave structure). See PERI_GR2_PPU_RG0_ATT0 for the details of bit fields.
PERI_GR2_PPU_RG12_ADDR1	0x40201320	PPU region address 1 (master structure)
PERI_GR2_PPU_RG12_ATT1	0x40201324	PPU region attributes 1 (master structure). See PERI_GR2_PPU_RG0_ATT1 for the details of bit fields.
PERI_GR2_PPU_RG13_ADDR0	0x40201340	PPU region address 0 (slave structure)
PERI_GR2_PPU_RG13_ATT0	0x40201344	PPU region attributes 0 (slave structure). See PERI_GR2_PPU_RG0_ATT0 for the details of bit fields.
PERI_GR2_PPU_RG13_ADDR1	0x40201360	PPU region address 1 (master structure)
PERI_GR2_PPU_RG13_ATT1	0x40201364	PPU region attributes 1 (master structure). See PERI_GR2_PPU_RG0_ATT1 for the details of bit fields.
PERI_GR2_PPU_RG14_ADDR0	0x40201380	PPU region address 0 (slave structure)
PERI_GR2_PPU_RG14_ATT0	0x40201384	PPU region attributes 0 (slave structure). See PERI_GR2_PPU_RG0_ATT0 for the details of bit fields.
PERI_GR2_PPU_RG14_ADDR1	0x402013A0	PPU region address 1 (master structure)
PERI_GR2_PPU_RG14_ATT1	0x402013A4	PPU region attributes 1 (master structure). See PERI_GR2_PPU_RG0_ATT1 for the details of bit fields.
PERI_GR2_PPU_RG15_ADDR0	0x402013C0	PPU region address 0 (slave structure)
PERI_GR2_PPU_RG15_ATT0	0x402013C4	PPU region attributes 0 (slave structure). See PERI_GR2_PPU_RG0_ATT0 for the details of bit fields.
PERI_GR2_PPU_RG15_ADDR1	0x402013E0	PPU region address 1 (master structure)
PERI_GR2_PPU_RG15_ATT1	0x402013E4	PPU region attributes 1 (master structure). See PERI_GR2_PPU_RG0_ATT1 for the details of bit fields.
PERI_GR2_PPU_RG16_ADDR0	0x40201400	PPU region address 0 (slave structure)
PERI_GR2_PPU_RG16_ATT0	0x40201404	PPU region attributes 0 (slave structure). See PERI_GR2_PPU_RG0_ATT0 for the details of bit fields.
PERI_GR2_PPU_RG16_ADDR1	0x40201420	PPU region address 1 (master structure)
PERI_GR2_PPU_RG16_ATT1	0x40201424	PPU region attributes 1 (master structure). See PERI_GR2_PPU_RG0_ATT1 for the details of bit fields.
PERI_GR2_PPU_RG17_ADDR0	0x40201440	PPU region address 0 (slave structure)
PERI_GR2_PPU_RG17_ATT0	0x40201444	PPU region attributes 0 (slave structure). See PERI_GR2_PPU_RG0_ATT0 for the details of bit fields.
PERI_GR2_PPU_RG17_ADDR1	0x40201460	PPU region address 1 (master structure)
PERI_GR2_PPU_RG17_ATT1	0x40201464	PPU region attributes 1 (master structure). See PERI_GR2_PPU_RG0_ATT1 for the details of bit fields.
PERI_GR2_PPU_RG18_ADDR0	0x40201480	PPU region address 0 (slave structure)
PERI_GR2_PPU_RG18_ATT0	0x40201484	PPU region attributes 0 (slave structure). See PERI_GR2_PPU_RG0_ATT0 for the details of bit fields.
PERI_GR2_PPU_RG18_ADDR1	0x402014A0	PPU region address 1 (master structure)
PERI_GR2_PPU_RG18_ATT1	0x402014A4	PPU region attributes 1 (master structure). See PERI_GR2_PPU_RG0_ATT1 for the details of bit fields.
PERI_GR2_PPU_RG19_ADDR0	0x402014C0	PPU region address 0 (slave structure)
PERI_GR2_PPU_RG19_ATT0	0x402014C4	PPU region attributes 0 (slave structure). See PERI_GR2_PPU_RG0_ATT0 for the details of bit fields.
PERI_GR2_PPU_RG19_ADDR1	0x402014E0	PPU region address 1 (master structure)
PERI_GR2_PPU_RG19_ATT1	0x402014E4	PPU region attributes 1 (master structure). See PERI_GR2_PPU_RG0_ATT1 for the details of bit fields.
PERI_GR2_PPU_RG20_ADDR0	0x40201500	PPU region address 0 (slave structure)

Register	Address	Description
PERI_GR2_PPU_RG20_ATT0	0x40201504	PPU region attributes 0 (slave structure). See PERI_GR2_PPU_RG0_ATT0 for the details of bit fields.
PERI_GR2_PPU_RG20_ADDR1	0x40201520	PPU region address 1 (master structure)
PERI_GR2_PPU_RG20_ATT1	0x40201524	PPU region attributes 1 (master structure). See PERI_GR2_PPU_RG0_ATT1 for the details of bit fields.
PERI_GR2_PPU_RG21_ADDR0	0x40201540	PPU region address 0 (slave structure)
PERI_GR2_PPU_RG21_ATT0	0x40201544	PPU region attributes 0 (slave structure). See PERI_GR2_PPU_RG0_ATT0 for the details of bit fields.
PERI_GR2_PPU_RG21_ADDR1	0x40201560	PPU region address 1 (master structure)
PERI_GR2_PPU_RG21_ATT1	0x40201564	PPU region attributes 1 (master structure). See PERI_GR2_PPU_RG0_ATT1 for the details of bit fields.
PERI_GR2_PPU_RG22_ADDR0	0x40201580	PPU region address 0 (slave structure)
PERI_GR2_PPU_RG22_ATT0	0x40201584	PPU region attributes 0 (slave structure). See PERI_GR2_PPU_RG0_ATT0 for the details of bit fields.
PERI_GR2_PPU_RG22_ADDR1	0x402015A0	PPU region address 1 (master structure)
PERI_GR2_PPU_RG22_ATT1	0x402015A4	PPU region attributes 1 (master structure). See PERI_GR2_PPU_RG0_ATT1 for the details of bit fields.
PERI_GR2_PPU_RG23_ADDR0	0x402015C0	PPU region address 0 (slave structure)
PERI_GR2_PPU_RG23_ATT0	0x402015C4	PPU region attributes 0 (slave structure). See PERI_GR2_PPU_RG0_ATT0 for the details of bit fields.
PERI_GR2_PPU_RG23_ADDR1	0x402015E0	PPU region address 1 (master structure)
PERI_GR2_PPU_RG23_ATT1	0x402015E4	PPU region attributes 1 (master structure). See PERI_GR2_PPU_RG0_ATT1 for the details of bit fields.
PERI_GR2_PPU_RG24_ADDR0	0x40201600	PPU region address 0 (slave structure)
PERI_GR2_PPU_RG24_ATT0	0x40201604	PPU region attributes 0 (slave structure). See PERI_GR2_PPU_RG0_ATT0 for the details of bit fields.
PERI_GR2_PPU_RG24_ADDR1	0x40201620	PPU region address 1 (master structure)
PERI_GR2_PPU_RG24_ATT1	0x40201624	PPU region attributes 1 (master structure). See PERI_GR2_PPU_RG0_ATT1 for the details of bit fields.
PERI_GR2_PPU_RG25_ADDR0	0x40201640	PPU region address 0 (slave structure)
PERI_GR2_PPU_RG25_ATT0	0x40201644	PPU region attributes 0 (slave structure)
PERI_GR2_PPU_RG25_ADDR1	0x40201660	PPU region address 1 (master structure)
PERI_GR2_PPU_RG25_ATT1	0x40201664	PPU region attributes 1 (master structure). See PERI_GR2_PPU_RG0_ATT1 for the details of bit fields.
PERI_GR2_PPU_RG26_ADDR0	0x40201680	PPU region address 0 (slave structure)
PERI_GR2_PPU_RG26_ATT0	0x40201684	PPU region attributes 0 (slave structure). See PERI_GR2_PPU_RG25_ATT0 for the details of bit fields.
PERI_GR2_PPU_RG26_ADDR1	0x402016A0	PPU region address 1 (master structure)
PERI_GR2_PPU_RG26_ATT1	0x402016A4	PPU region attributes 1 (master structure). See PERI_GR2_PPU_RG0_ATT1 for the details of bit fields.
PERI_GR2_PPU_RG27_ADDR0	0x402016C0	PPU region address 0 (slave structure)
PERI_GR2_PPU_RG27_ATT0	0x402016C4	PPU region attributes 0 (slave structure). See PERI_GR2_PPU_RG25_ATT0 for the details of bit fields.
PERI_GR2_PPU_RG27_ADDR1	0x402016E0	PPU region address 1 (master structure)
PERI_GR2_PPU_RG27_ATT1	0x402016E4	PPU region attributes 1 (master structure). See PERI_GR2_PPU_RG0_ATT1 for the details of bit fields.
PERI_GR2_PPU_RG28_ADDR0	0x40201700	PPU region address 0 (slave structure)
PERI_GR2_PPU_RG28_ATT0	0x40201704	PPU region attributes 0 (slave structure). See PERI_GR2_PPU_RG25_ATT0 for the details of bit fields.
PERI_GR2_PPU_RG28_ADDR1	0x40201720	PPU region address 1 (master structure)
PERI_GR2_PPU_RG28_ATT1	0x40201724	PPU region attributes 1 (master structure). See PERI_GR2_PPU_RG0_ATT1 for the details of bit fields.

Register	Address	Description
PERI_GR3_PPU_SL0_ADDR0	0x40300000	PPU region address 0 (slave structure)
PERI_GR3_PPU_SL0_ATT0	0x40300004	PPU region attributes 0 (slave structure). See PERI_GR1_PPU_SL0_ATT0 for the details of bit fields.
PERI_GR3_PPU_SL0_ADDR1	0x40300020	PPU region address 1 (master structure)
PERI_GR3_PPU_SL0_ATT1	0x40300024	PPU region attributes 1 (master structure). See PERI_GR1_PPU_SL0_ATT1 for the details of bit fields.
PERI_GR3_PPU_SL1_ADDR0	0x40300040	PPU region address 0 (slave structure)
PERI_GR3_PPU_SL1_ATT0	0x40300044	PPU region attributes 0 (slave structure)
PERI_GR3_PPU_SL1_ADDR1	0x40300060	PPU region address 1 (master structure)
PERI_GR3_PPU_SL1_ATT1	0x40300064	PPU region attributes 1 (master structure). See PERI_GR1_PPU_SL0_ATT1 for the details of bit fields.
PERI_GR3_PPU_SL2_ADDR0	0x40300080	PPU region address 0 (slave structure)
PERI_GR3_PPU_SL2_ATT0	0x40300084	PPU region attributes 0 (slave structure). See PERI_GR1_PPU_SL0_ATT0 for the details of bit fields.
PERI_GR3_PPU_SL2_ADDR1	0x403000A0	PPU region address 1 (master structure)
PERI_GR3_PPU_SL2_ATT1	0x403000A4	PPU region attributes 1 (master structure). See PERI_GR1_PPU_SL0_ATT1 for the details of bit fields.
PERI_GR3_PPU_SL3_ADDR0	0x403000C0	PPU region address 0 (slave structure)
PERI_GR3_PPU_SL3_ATT0	0x403000C4	PPU region attributes 0 (slave structure). See PERI_GR1_PPU_SL0_ATT0 for the details of bit fields.
PERI_GR3_PPU_SL3_ADDR1	0x403000E0	PPU region address 1 (master structure)
PERI_GR3_PPU_SL3_ATT1	0x403000E4	PPU region attributes 1 (master structure). See PERI_GR1_PPU_SL0_ATT1 for the details of bit fields.
PERI_GR3_PPU_SL4_ADDR0	0x40300100	PPU region address 0 (slave structure)
PERI_GR3_PPU_SL4_ATT0	0x40300104	PPU region attributes 0 (slave structure). See PERI_GR1_PPU_SL0_ATT0 for the details of bit fields.
PERI_GR3_PPU_SL4_ADDR1	0x40300120	PPU region address 1 (master structure)
PERI_GR3_PPU_SL4_ATT1	0x40300124	PPU region attributes 1 (master structure). See PERI_GR1_PPU_SL0_ATT1 for the details of bit fields.
PERI_GR3_PPU_SL5_ADDR0	0x40300140	PPU region address 0 (slave structure)
PERI_GR3_PPU_SL5_ATT0	0x40300144	PPU region attributes 0 (slave structure). See PERI_GR1_PPU_SL0_ATT0 for the details of bit fields.
PERI_GR3_PPU_SL5_ADDR1	0x40300160	PPU region address 1 (master structure)
PERI_GR3_PPU_SL5_ATT1	0x40300164	PPU region attributes 1 (master structure). See PERI_GR1_PPU_SL0_ATT1 for the details of bit fields.
PERI_GR3_PPU_SL6_ADDR0	0x40300180	PPU region address 0 (slave structure)
PERI_GR3_PPU_SL6_ATT0	0x40300184	PPU region attributes 0 (slave structure). See PERI_GR2_PPU_SL8_ATT0 for the details of bit fields.
PERI_GR3_PPU_SL6_ADDR1	0x403001A0	PPU region address 1 (master structure)
PERI_GR3_PPU_SL6_ATT1	0x403001A4	PPU region attributes 1 (master structure). See PERI_GR1_PPU_SL0_ATT1 for the details of bit fields.
PERI_GR3_PPU_SL8_ADDR0	0x40300200	PPU region address 0 (slave structure)
PERI_GR3_PPU_SL8_ATT0	0x40300204	PPU region attributes 0 (slave structure). See PERI_GR1_PPU_SL0_ATT0 for the details of bit fields.
PERI_GR3_PPU_SL8_ADDR1	0x40300220	PPU region address 1 (master structure)
PERI_GR3_PPU_SL8_ATT1	0x40300224	PPU region attributes 1 (master structure). See PERI_GR1_PPU_SL0_ATT1 for the details of bit fields.
PERI_GR3_PPU_SL9_ADDR0	0x40300240	PPU region address 0 (slave structure). See PERI_GR3_PPU_SL8_ADDR0 for the details of bit fields.
PERI_GR3_PPU_SL9_ATT0	0x40300244	PPU region attributes 0 (slave structure). See PERI_GR1_PPU_SL0_ATT0 for the details of bit fields.
PERI_GR3_PPU_SL9_ADDR1	0x40300260	PPU region address 1 (master structure)

Register	Address	Description
PERI_GR3_PPU_SL9_ATT1	0x40300264	PPU region attributes 1 (master structure). See PERI_GR1_PPU_SL0_ATT1 for the details of bit fields.
PERI_GR3_PPU_SL10_ADDR0	0x40300280	PPU region address 0 (slave structure)
PERI_GR3_PPU_SL10_ATT0	0x40300284	PPU region attributes 0 (slave structure). See PERI_GR1_PPU_SL0_ATT0 for the details of bit fields.
PERI_GR3_PPU_SL10_ADDR1	0x403002A0	PPU region address 1 (master structure)
PERI_GR3_PPU_SL10_ATT1	0x403002A4	PPU region attributes 1 (master structure). See PERI_GR1_PPU_SL0_ATT1 for the details of bit fields.
PERI_GR3_PPU_SL11_ADDR0	0x403002C0	PPU region address 0 (slave structure)
PERI_GR3_PPU_SL11_ATT0	0x403002C4	PPU region attributes 0 (slave structure)
PERI_GR3_PPU_SL11_ADDR1	0x403002E0	PPU region address 1 (master structure)
PERI_GR3_PPU_SL11_ATT1	0x403002E4	PPU region attributes 1 (master structure). See PERI_GR1_PPU_SL0_ATT1 for the details of bit fields.
PERI_GR3_PPU_SL12_ADDR0	0x40300300	PPU region address 0 (slave structure)
PERI_GR3_PPU_SL12_ATT0	0x40300304	PPU region attributes 0 (slave structure). See PERI_GR1_PPU_SL0_ATT0 for the details of bit fields.
PERI_GR3_PPU_SL12_ADDR1	0x40300320	PPU region address 1 (master structure)
PERI_GR3_PPU_SL12_ATT1	0x40300324	PPU region attributes 1 (master structure). See PERI_GR1_PPU_SL0_ATT1 for the details of bit fields.
PERI_GR4_PPU_SL0_ADDR0	0x40400000	PPU region address 0 (slave structure)
PERI_GR4_PPU_SL0_ATT0	0x40400004	PPU region attributes 0 (slave structure). See PERI_GR1_PPU_SL0_ATT0 for the details of bit fields.
PERI_GR4_PPU_SL0_ADDR1	0x40400020	PPU region address 1 (master structure)
PERI_GR4_PPU_SL0_ATT1	0x40400024	PPU region attributes 1 (master structure). See PERI_GR1_PPU_SL0_ATT1 for the details of bit fields.
PERI_GR4_PPU_SL2_ADDR0	0x40400080	PPU region address 0 (slave structure)
PERI_GR4_PPU_SL2_ATT0	0x40400084	PPU region attributes 0 (slave structure). See PERI_GR1_PPU_SL0_ATT0 for the details of bit fields.
PERI_GR4_PPU_SL2_ADDR1	0x404000A0	PPU region address 1 (master structure)
PERI_GR4_PPU_SL2_ATT1	0x404000A4	PPU region attributes 1 (master structure). See PERI_GR1_PPU_SL0_ATT1 for the details of bit fields.
PERI_GR6_PPU_SL0_ADDR0	0x40600000	PPU region address 0 (slave structure)
PERI_GR6_PPU_SL0_ATT0	0x40600004	PPU region attributes 0 (slave structure). See PERI_GR1_PPU_SL0_ATT0 for the details of bit fields.
PERI_GR6_PPU_SL0_ADDR1	0x40600020	PPU region address 1 (master structure)
PERI_GR6_PPU_SL0_ATT1	0x40600024	PPU region attributes 1 (master structure). See PERI_GR1_PPU_SL0_ATT1 for the details of bit fields.
PERI_GR6_PPU_SL1_ADDR0	0x40600040	PPU region address 0 (slave structure)
PERI_GR6_PPU_SL1_ATT0	0x40600044	PPU region attributes 0 (slave structure). See PERI_GR1_PPU_SL0_ATT0 for the details of bit fields.
PERI_GR6_PPU_SL1_ADDR1	0x40600060	PPU region address 1 (master structure)
PERI_GR6_PPU_SL1_ATT1	0x40600064	PPU region attributes 1 (master structure). See PERI_GR1_PPU_SL0_ATT1 for the details of bit fields.
PERI_GR6_PPU_SL2_ADDR0	0x40600080	PPU region address 0 (slave structure). See PERI_GR6_PPU_SL1_ADDR0 for the details of bit fields.
PERI_GR6_PPU_SL2_ATT0	0x40600084	PPU region attributes 0 (slave structure). See PERI_GR1_PPU_SL0_ATT0 for the details of bit fields.
PERI_GR6_PPU_SL2_ADDR1	0x406000A0	PPU region address 1 (master structure)
PERI_GR6_PPU_SL2_ATT1	0x406000A4	PPU region attributes 1 (master structure). See PERI_GR1_PPU_SL0_ATT1 for the details of bit fields.
PERI_GR6_PPU_SL3_ADDR0	0x406000C0	PPU region address 0 (slave structure). See PERI_GR6_PPU_SL1_ADDR0 for the details of bit fields.

Register	Address	Description
PERI_GR6_PPU_SL3_ATT0	0x406000C4	PPU region attributes 0 (slave structure). See PERI_GR1_PPU_SL0_ATT0 for the details of bit fields.
PERI_GR6_PPU_SL3_ADDR1	0x406000E0	PPU region address 1 (master structure)
PERI_GR6_PPU_SL3_ATT1	0x406000E4	PPU region attributes 1 (master structure). See PERI_GR1_PPU_SL0_ATT1 for the details of bit fields.
PERI_GR6_PPU_SL4_ADDR0	0x40600100	PPU region address 0 (slave structure). See PERI_GR6_PPU_SL1_ADDR0 for the details of bit fields.
PERI_GR6_PPU_SL4_ATT0	0x40600104	PPU region attributes 0 (slave structure). See PERI_GR1_PPU_SL0_ATT0 for the details of bit fields.
PERI_GR6_PPU_SL4_ADDR1	0x40600120	PPU region address 1 (master structure)
PERI_GR6_PPU_SL4_ATT1	0x40600124	PPU region attributes 1 (master structure). See PERI_GR1_PPU_SL0_ATT1 for the details of bit fields.
PERI_GR6_PPU_SL5_ADDR0	0x40600140	PPU region address 0 (slave structure). See PERI_GR6_PPU_SL1_ADDR0 for the details of bit fields.
PERI_GR6_PPU_SL5_ATT0	0x40600144	PPU region attributes 0 (slave structure). See PERI_GR1_PPU_SL0_ATT0 for the details of bit fields.
PERI_GR6_PPU_SL5_ADDR1	0x40600160	PPU region address 1 (master structure)
PERI_GR6_PPU_SL5_ATT1	0x40600164	PPU region attributes 1 (master structure). See PERI_GR1_PPU_SL0_ATT1 for the details of bit fields.
PERI_GR6_PPU_SL6_ADDR0	0x40600180	PPU region address 0 (slave structure). See PERI_GR6_PPU_SL1_ADDR0 for the details of bit fields.
PERI_GR6_PPU_SL6_ATT0	0x40600184	PPU region attributes 0 (slave structure). See PERI_GR1_PPU_SL0_ATT0 for the details of bit fields.
PERI_GR6_PPU_SL6_ADDR1	0x406001A0	PPU region address 1 (master structure)
PERI_GR6_PPU_SL6_ATT1	0x406001A4	PPU region attributes 1 (master structure). See PERI_GR1_PPU_SL0_ATT1 for the details of bit fields.
PERI_GR6_PPU_SL7_ADDR0	0x406001C0	PPU region address 0 (slave structure). See PERI_GR6_PPU_SL1_ADDR0 for the details of bit fields.
PERI_GR6_PPU_SL7_ATT0	0x406001C4	PPU region attributes 0 (slave structure). See PERI_GR1_PPU_SL0_ATT0 for the details of bit fields.
PERI_GR6_PPU_SL7_ADDR1	0x406001E0	PPU region address 1 (master structure)
PERI_GR6_PPU_SL7_ATT1	0x406001E4	PPU region attributes 1 (master structure). See PERI_GR1_PPU_SL0_ATT1 for the details of bit fields.
PERI_GR6_PPU_SL8_ADDR0	0x40600200	PPU region address 0 (slave structure). See PERI_GR6_PPU_SL1_ADDR0 for the details of bit fields.
PERI_GR6_PPU_SL8_ATT0	0x40600204	PPU region attributes 0 (slave structure). See PERI_GR1_PPU_SL0_ATT0 for the details of bit fields.
PERI_GR6_PPU_SL8_ADDR1	0x40600220	PPU region address 1 (master structure)
PERI_GR6_PPU_SL8_ATT1	0x40600224	PPU region attributes 1 (master structure). See PERI_GR1_PPU_SL0_ATT1 for the details of bit fields.
PERI_GR6_PPU_SL9_ADDR0	0x40600240	PPU region address 0 (slave structure). See PERI_GR6_PPU_SL1_ADDR0 for the details of bit fields.
PERI_GR6_PPU_SL9_ATT0	0x40600244	PPU region attributes 0 (slave structure). See PERI_GR1_PPU_SL0_ATT0 for the details of bit fields.
PERI_GR6_PPU_SL9_ADDR1	0x40600260	PPU region address 1 (master structure)
PERI_GR6_PPU_SL9_ATT1	0x40600264	PPU region attributes 1 (master structure). See PERI_GR1_PPU_SL0_ATT1 for the details of bit fields.
PERI_GR9_PPU_SL0_ADDR0	0x41000000	PPU region address 0 (slave structure)
PERI_GR9_PPU_SL0_ATT0	0x41000004	PPU region attributes 0 (slave structure). See PERI_GR1_PPU_SL0_ATT0 for the details of bit fields.
PERI_GR9_PPU_SL0_ADDR1	0x41000020	PPU region address 1 (master structure)
PERI_GR9_PPU_SL0_ATT1	0x41000024	PPU region attributes 1 (master structure). See PERI_GR1_PPU_SL0_ATT1 for the details of bit fields.
PERI_GR9_PPU_SL1_ADDR0	0x41000040	PPU region address 0 (slave structure)

Register	Address	Description
PERI_GR9_PPU_SL1_ATT0	0x41000044	PPU region attributes 0 (slave structure)
PERI_GR9_PPU_SL1_ADDR1	0x41000060	PPU region address 1 (master structure)
PERI_GR9_PPU_SL1_ATT1	0x41000064	PPU region attributes 1 (master structure). See PERI_GR1_PPU_SL0_ATT1 for the details of bit fields.
PERI_GR10_PPU_SL0_ADDR0	0x42A00000	PPU region address 0 (slave structure)
PERI_GR10_PPU_SL0_ATT0	0x42A00004	PPU region attributes 0 (slave structure). See PERI_GR1_PPU_SL0_ATT0 for the details of bit fields.
PERI_GR10_PPU_SL0_ADDR1	0x42A00020	PPU region address 1 (master structure)
PERI_GR10_PPU_SL0_ATT1	0x42A00024	PPU region attributes 1 (master structure). See PERI_GR1_PPU_SL0_ATT1 for the details of bit fields.
PERI_GR10_PPU_SL1_ADDR0	0x42A00040	PPU region address 0 (slave structure)
PERI_GR10_PPU_SL1_ATT0	0x42A00044	PPU region attributes 0 (slave structure). See PERI_GR2_PPU_SL8_ATT0 for the details of bit fields.
PERI_GR10_PPU_SL1_ADDR1	0x42A00060	PPU region address 1 (master structure)
PERI_GR10_PPU_SL1_ATT1	0x42A00064	PPU region attributes 1 (master structure). See PERI_GR1_PPU_SL0_ATT1 for the details of bit fields.
PERI_GR10_PPU_SL2_ADDR0	0x42A00080	PPU region address 0 (slave structure)
PERI_GR10_PPU_SL2_ATT0	0x42A00084	PPU region attributes 0 (slave structure). See PERI_GR2_PPU_SL8_ATT0 for the details of bit fields.
PERI_GR10_PPU_SL2_ADDR1	0x42A000A0	PPU region address 1 (master structure)
PERI_GR10_PPU_SL2_ATT1	0x42A000A4	PPU region attributes 1 (master structure). See PERI_GR1_PPU_SL0_ATT1 for the details of bit fields.

2.1.1 PERI_GR0_SL_CTL

Slave control

Address: 0x40010020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	None
HW Access	None						R	None
Name	None [7:2]						EN-ABLED_1	None

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	ENABLED_1	Peripheral group, slave 1 enable. If the slave is disabled, its clock is gated off (constant "0") and its resets are activated. Note: For peripheral group 0 (the peripheral interconnect MMIO registers), this field is a constant '1' (SW: R): the slave can NOT be disabled. Default Value: 1

2.1.1 PERI_GR1_SL_CTL

Slave control

Address: 0x40010060

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	R
HW Access	None						R	R
Name	None [7:2]						EN-ABLED_1	EN-ABLED_0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	ENABLED_1	Peripheral group, slave 1 enable. If the slave is disabled, its clock is gated off (constant "0") and its resets are activated. Note: For peripheral group 0 (the peripheral interconnect MMIO registers), this field is a constant '1' (SW: R): the slave can NOT be disabled. Default Value: 1
0	ENABLED_0	Peripheral group, slave 0 enable. This field is for the peripheral group internal MMIO register slave (PPU structures) and is a constant '1'. This slave can NOT be disabled. Default Value: 1

2.1.2 PERI_GR1_TIMEOUT_CTL

Timeout control

Address: 0x40010064

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	TIMEOUT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	TIMEOUT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	TIMEOUT	This field specifies a number of peripheral group (clk_group) clock cycles. If an AHB-Lite bus transfer takes more than the specified number of cycles (timeout detection), the bus transfer is terminated with an AHB-Lite bus error and a fault is generated (and possibly recorded in the fault report structure(s)). "0x0000"-"0xfffe": Number of peripheral group clock cycles. "0xffff": This value is the default/reset value and specifies that no timeout detection is performed: a bus transfer will never be terminated and a fault will never be generated. Default Value: 65535

2.1.3 PERI_GR2_SL_CTL

Slave control

Address: 0x400100A0

Retention: Retained

Bits	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SW Access	RW	RW	RW	RW	RW	RW	RW	R
HW Access	R	R	R	R	R	R	R	R
Name	EN-ABLED_7	EN-ABLED_6	EN-ABLED_5	EN-ABLED_4	EN-ABLED_3	EN-ABLED_2	EN-ABLED_1	EN-ABLED_0

Bits	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SW Access	None		RW	RW	None		RW	RW
HW Access	None		R	R	None		R	R
Name	None [15:14]		EN-ABLED_13	EN-ABLED_12	None [11:10]		EN-ABLED_9	EN-ABLED_8

Bits	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	**Name**	**Description**
13	ENABLED_13	Default Value: 1
12	ENABLED_12	Default Value: 1
9	ENABLED_9	Default Value: 1
8	ENABLED_8	Default Value: 1
7	ENABLED_7	Default Value: 1
6	ENABLED_6	Default Value: 1
5	ENABLED_5	Default Value: 1
4	ENABLED_4	Default Value: 1
3	ENABLED_3	Default Value: 1

2.1.3 PERI_GR2_SL_CTL (continued)

2	ENABLED_2	Peripheral group, slave 2 enable. If the slave is disabled, its clock is gated off (constant "0") and its resets are activated. Note: For peripheral group 0 (the peripheral interconnect, master interface MMIO registers), this field is a constant '1' (SW: R): the slave can NOT be disabled. Default Value: 1
1	ENABLED_1	Peripheral group, slave 1 enable. If the slave is disabled, its clock is gated off (constant "0") and its resets are activated. Note: For peripheral group 0 (the peripheral interconnect MMIO registers), this field is a constant '1' (SW: R): the slave can NOT be disabled. Default Value: 1
0	ENABLED_0	Peripheral group, slave 0 enable. This field is for the peripheral group internal MMIO register slave (PPU structures) and is a constant '1'. This slave can NOT be disabled. Default Value: 1

2.1.4 PERI_GR3_CLOCK_CTL

Clock control

Address: 0x400100C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INT8_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 8	INT8_DIV	Specifies a group clock divider (from the peripheral clock "clk_peri" to the group clock "clk_group[3/4/5/...15]"). Integer division by (1+INT8_DIV). Allows for integer divisions in the range [1, 256]. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0

2.1.5 PERI_GR3_SL_CTL

Slave control

Address: 0x400100E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	RW	RW	RW	RW	RW	R
HW Access	None	R	R	R	R	R	R	R
Name	None	EN-ABLED_6	EN-ABLED_5	EN-ABLED_4	EN-ABLED_3	EN-ABLED_2	EN-ABLED_1	EN-ABLED_0

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [15:13]			EN-ABLED_12	EN-ABLED_11	EN-ABLED_10	EN-ABLED_9	EN-ABLED_8

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
12	ENABLED_12	Default Value: 1
11	ENABLED_11	Default Value: 1
10	ENABLED_10	Default Value: 1
9	ENABLED_9	Default Value: 1
8	ENABLED_8	Default Value: 1
6	ENABLED_6	Default Value: 1
5	ENABLED_5	Default Value: 1
4	ENABLED_4	Default Value: 1
3	ENABLED_3	Default Value: 1

2.1.5 PERI_GR3_SL_CTL (continued)

2	ENABLED_2	Peripheral group, slave 2 enable. If the slave is disabled, its clock is gated off (constant "0") and its resets are activated. Note: For peripheral group 0 (the peripheral interconnect, master interface MMIO registers), this field is a constant '1' (SW: R): the slave can NOT be disabled. Default Value: 1
1	ENABLED_1	Peripheral group, slave 1 enable. If the slave is disabled, its clock is gated off (constant "0") and its resets are activated. Note: For peripheral group 0 (the peripheral interconnect MMIO registers), this field is a constant '1' (SW: R): the slave can NOT be disabled. Default Value: 1
0	ENABLED_0	Peripheral group, slave 0 enable. This field is for the peripheral group internal MMIO register slave (PPU structures) and is a constant '1'. This slave can NOT be disabled. Default Value: 1

2.1.6 PERI_GR4_SL_CTL

Slave control

Address: 0x40010120

Retention: Retained

Bits	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SW Access	None					RW	None	R
HW Access	None					R	None	R
Name	None [7:3]					EN-ABLED_2	None	EN-ABLED_0

Bits	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	**Name**	**Description**
2	ENABLED_2	Peripheral group, slave 2 enable. If the slave is disabled, its clock is gated off (constant "0") and its resets are activated. Note: For peripheral group 0 (the peripheral interconnect, master interface MMIO registers), this field is a constant '1' (SW: R): the slave can NOT be disabled. Default Value: 1
0	ENABLED_0	Peripheral group, slave 0 enable. This field is for the peripheral group internal MMIO register slave (PPU structures) and is a constant '1'. This slave can NOT be disabled. Default Value: 1

2.1.7 PERI_GR6_SL_CTL

Slave control

Address: 0x400101A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	R
HW Access	R	R	R	R	R	R	R	R
Name	EN-ABLED_7	EN-ABLED_6	EN-ABLED_5	EN-ABLED_4	EN-ABLED_3	EN-ABLED_2	EN-ABLED_1	EN-ABLED_0

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [15:10]						EN-ABLED_9	EN-ABLED_8

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	ENABLED_9	Default Value: 1
8	ENABLED_8	Default Value: 1
7	ENABLED_7	Default Value: 1
6	ENABLED_6	Default Value: 1
5	ENABLED_5	Default Value: 1
4	ENABLED_4	Default Value: 1
3	ENABLED_3	Default Value: 1
2	ENABLED_2	Peripheral group, slave 2 enable. If the slave is disabled, its clock is gated off (constant "0") and its resets are activated. Note: For peripheral group 0 (the peripheral interconnect, master interface MMIO registers), this field is a constant '1' (SW: R): the slave can NOT be disabled. Default Value: 1

2.1.7 PERI_GR6_SL_CTL (continued)

1	ENABLED_1	Peripheral group, slave 1 enable. If the slave is disabled, its clock is gated off (constant "0") and its resets are activated. Note: For peripheral group 0 (the peripheral interconnect MMIO registers), this field is a constant '1' (SW: R): the slave can NOT be disabled. Default Value: 1
0	ENABLED_0	Peripheral group, slave 0 enable. This field is for the peripheral group internal MMIO register slave (PPU structures) and is a constant '1'. This slave can NOT be disabled. Default Value: 1

2.1.8 PERI_GR10_SL_CTL

Slave control

Address: 0x400102A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW	RW	R
HW Access	None					R	R	R
Name	None [7:3]					EN-ABLED_2	EN-ABLED_1	EN-ABLED_0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	ENABLED_2	Peripheral group, slave 2 enable. If the slave is disabled, its clock is gated off (constant "0") and its resets are activated. Note: For peripheral group 0 (the peripheral interconnect, master interface MMIO registers), this field is a constant '1' (SW: R): the slave can NOT be disabled. Default Value: 1
1	ENABLED_1	Peripheral group, slave 1 enable. If the slave is disabled, its clock is gated off (constant "0") and its resets are activated. Note: For peripheral group 0 (the peripheral interconnect MMIO registers), this field is a constant '1' (SW: R): the slave can NOT be disabled. Default Value: 1
0	ENABLED_0	Peripheral group, slave 0 enable. This field is for the peripheral group internal MMIO register slave (PPU structures) and is a constant '1'. This slave can NOT be disabled. Default Value: 1

2.1.9 PERI_DIV_CMD

Divider command register

Address: 0x40010400

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW					
HW Access	R		R					
Name	TYPE_SEL [7:6]		DIV_SEL [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW					
HW Access	R		R					
Name	PA_TYPE_SEL [15:14]		PA_DIV_SEL [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None					
HW Access	RW1C	RW1C	None					
Name	ENABLE	DISABLE	None [29:24]					

Bits	Name	Description
31	ENABLE	Clock divider enable command (mutually exclusive with DISABLE). Typically, SW sets this field to '1' to enable a divider and HW sets this field to '0' to indicate that divider enabling has completed. When a divider is enabled, its integer and fractional (if present) counters are initialized to "0". If a divider is to be re-enabled using different integer and fractional divider values, the SW should follow these steps: 0: Disable the divider using the DIV_CMD.DISABLE field. 1: Configure the divider's DIV_XXX_CTL register. 2: Enable the divider using the DIV_CMD_ENABLE field. The DIV_SEL and TYPE_SEL fields specify which divider is to be enabled. The enabled divider may be phase aligned to either "clk_peri" (typical usage) or to ANY enabled divider. The PA_DIV_SEL and PA_TYPE_SEL fields specify the reference divider. The HW sets the ENABLE field to '0' when the enabling is performed and the HW set the DIV_XXX_CTL.EN field of the divider to '1' when the enabling is performed. Note that enabling with phase alignment to a low frequency divider takes time. E.g. To align to a divider that generates a clock of "clk_peri"/n (with n being the integer divider value INT_DIV+1), up to n cycles may be required to perform alignment. Phase alignment to "clk_peri" takes affect immediately. SW can set this field to '0' during phase alignment to abort the enabling process. Default Value: 0

2.1.9 PERI_DIV_CMD (continued)

30	DISABLE	Clock divider disable command (mutually exclusive with ENABLE). SW sets this field to '1' and HW sets this field to '0'. The DIV_SEL and TYPE_SEL fields specify which divider is to be disabled. The HW sets the DISABLE field to '0' immediately and the HW sets the DIV_XXX_CTL.EN field of the divider to '0' immediately. Default Value: 0
15 : 14	PA_TYPE_SEL	Specifies the divider type of the divider to which phase alignment is performed for the clock enable command: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
13 : 8	PA_DIV_SEL	(PA_TYPE_SEL, PA_DIV_SEL) specifies the divider to which phase alignment is performed for the clock enable command. Any enabled divider can be used as reference. This allows all dividers to be aligned with each other, even when they are enabled at different times. If PA_DIV_SEL is "63" and PA_TYPE_SEL is "3", "clk_peri" is used as reference. Default Value: 63
7 : 6	TYPE_SEL	Specifies the divider type of the divider on which the command is performed: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
5 : 0	DIV_SEL	(TYPE_SEL, DIV_SEL) specifies the divider on which the command (DISABLE/ENABLE) is performed. If DIV_SEL is "63" and TYPE_SEL is "3" (default/reset value), no divider is specified and no clock signal(s) are generated. Default Value: 63

2.1.10 PERI_DIV_8_CTL0

Divider control register (for 8.0 divider)

Address: 0x40010800

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INT8_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 8	INT8_DIV	Integer division by (1+INT8_DIV). Allows for integer divisions in the range [1, 256]. Note: this type of divider does NOT allow for a fractional division. For the generation of a divided clock, the integer division range is restricted to [2, 256]. For the generation of a 50/50% duty cycle digital divided clock, the integer division range is resticited to even numbers in the range [2, 256]. The generation of a 50/50 % duty cycle analog divided clock has no restrictions. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0
0	EN	Divider enabled. HW sets this field to '1' as a result of an ENABLE command. HW sets this field to '0' as a result on a DISABLE command. Note that this field is retained. As a result, the divider does NOT have to be re-enabled after transitioning from DeepSleep to Active power mode. Default Value: 0

2.1.11 PERI_DIV_16_CTL0

Divider control register (for 16.0 divider)

Address: 0x40010900

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INT16_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INT16_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 8	INT16_DIV	Integer division by (1+INT16_DIV). Allows for integer divisions in the range [1, 65,536]. Note: this type of divider does NOT allow for a fractional division. For the generation of a divided clock, the integer division range is restricted to [2, 65,536]. For the generation of a 50/50% duty cycle digital divided clock, the integer division range is restricted to even numbers in the range [2, 65,536]. The generation of a 50/50 % duty cycle analog divided clock has no restrictions. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0
0	EN	Divider enabled. HW sets this field to '1' as a result of an ENABLE command. HW sets this field to '0' as a result on a DISABLE command. Note that this field is retained. As a result, the divider does NOT have to be re-enabled after transitioning from DeepSleep to Active power mode. Default Value: 0

2.1.12 PERI_DIV_16_5_CTL0

Divider control register (for 16.5 divider)

Address: 0x40010A00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		R
HW Access	R					None		RW
Name	FRAC5_DIV [7:3]					None [2:1]		EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INT16_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INT16_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 8	INT16_DIV	Integer division by (1+INT16_DIV). Allows for integer divisions in the range [1, 65,536]. Note: combined with fractional division, this divider type allows for a division in the range [1, 65,536 31/32] in 1/32 increments. For the generation of a divided clock, the division range is restricted to [2, 65,536 31/32]. For the generation of a 50/50% duty cycle divided clock, the division range is restricted to [2, 65,536]. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0
7 : 3	FRAC5_DIV	Fractional division by (FRAC5_DIV/32). Allows for fractional divisions in the range [0, 31/32]. Note that fractional division results in clock jitter as some clock periods may be 1 "clk_peri" cycle longer than other clock periods. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0

2.1.12 PERI_DIV_16_5_CTL0 (continued)

0	EN	Divider enabled. HW sets this field to '1' as a result of an ENABLE command. HW sets this field to '0' as a result on a DISABLE command. Note that this field is retained. As a result, the divider does NOT have to be re-enabled after transitioning from DeepSleep to Active power mode. Default Value: 0

2.1.13 PERI_DIV_24_5_CTL0

Divider control register (for 24.5 divider)

Address: 0x40010B00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		R
HW Access	R					None		RW
Name	FRAC5_DIV [7:3]					None [2:1]		EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INT24_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INT24_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	INT24_DIV [31:24]							

Bits	Name	Description
31 : 8	INT24_DIV	Integer division by (1+INT24_DIV). Allows for integer divisions in the range [1, 16,777,216]. Note: combined with fractional division, this divider type allows for a division in the range [1, 16,777,216 31/32] in 1/32 increments. For the generation of a divided clock, the integer division range is restricted to [2, 16,777,216 31/32]. For the generation of a 50/50% duty cycle divided clock, the division range is restricted to [2, 16,777,216]. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0
7 : 3	FRAC5_DIV	Fractional division by (FRAC5_DIV/32). Allows for fractional divisions in the range [0, 31/32]. Note that fractional division results in clock jitter as some clock periods may be 1 "clk_peri" cycle longer than other clock periods. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0

2.1.13 PERI_DIV_24_5_CTL0 (continued)

0	EN	Divider enabled. HW sets this field to '1' as a result of an ENABLE command. HW sets this field to '0' as a result on a DISABLE command. Note that this field is retained. As a result, the divider does NOT have to be re-enabled after transitioning from DeepSleep to Active power mode. Default Value: 0

2.1.14 PERI_CLOCK_CTL0

Clock control register

Address: 0x40010C00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None		RW			
HW Access	R		None		R			
Name	TYPE_SEL [7:6]		None [5:4]		DIV_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	TYPE_SEL	Specifies divider type: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
3 : 0	DIV_SEL	Specifies one of the dividers of the divider type specified by TYPE_SEL. If DIV_SEL is "63" and TYPE_SEL is "3" (default/reset value), no divider is specified and no clock control signal(s) are generated. When transitioning a clock between two out-of-phase dividers, spurious clock control signals may be generated for one "clk_peri" cycle during this transition. These clock control signals may cause a single clock period that is smaller than any of the two divider periods. To prevent these spurious clock signals, the clock multiplexer can be disconnected (DIV_SEL is "63" and TYPE_-SEL is "3") for a transition time that is larger than the smaller of the two divider periods. Default Value: 15

2.1.15 PERI_TR_CMD

Trigger command register

Address: 0x40011000

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	TR_SEL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				GROUP_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	COUNT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None					
HW Access	RW1C	R	None					
Name	ACTIVATE	OUT_SEL	None [29:24]					

Bits	Name	Description
31	ACTIVATE	SW sets this field to '1' by to activate (set to '1') a trigger as identified by TR_SEL and OUT_SEL for COUNT cycles. HW sets this field to '0' when the cycle counter is decremented to "0". Note: a COUNT value of 255 is a special case and trigger activation is under direct control of the ACTIVATE field (the counter is not decremented). Default Value: 0
30	OUT_SEL	Specifies whether trigger activation is for a specific input or output trigger of the trigger multiplexer. Activation of a specific input trigger, will result in activation of all output triggers that have the specific input trigger selected through their TR_OUT_CTL.TR_SEL field. Activation of a specific output trigger, will result in activation of the specified TR_SEL output trigger only. '0': TR_SEL selection and trigger activation is for an input trigger to the trigger multiplexer. '1': TR_SEL selection and trigger activation is for an output trigger from the trigger multiplexer. Default Value: 0
23 : 16	COUNT	Amount of "clk_peri" cycles a specific trigger is activated. During activation (ACTIVATE is '1'), HW decrements this field to "0" using a cycle counter. During activation, SW should not modify this register field. A value of 255 is a special case: HW does NOT decrement this field to "0" and trigger activation is under direct control of ACTIVATE when ACTIVATE is '1' the trigger is activated and when ACTIVATE is '0' the trigger is deactivated. Default Value: 0

2.1.15 PERI_TR_CMD (continued)

11 : 8	GROUP_SEL	Specifies the trigger group. Default Value: 0
7 : 0	TR_SEL	Specifies the activated trigger when ACTIVATE is '1'. OUT_SEL specifies whether the activated trigger is an input trigger or output trigger to the trigger multiplexer. During activation (ACTIVATE is '1'), SW should not modify this register field. If the specified trigger is not present, the trigger activation has no effect. Default Value: 0

2.1.16 PERI_TR_GR0_TR_OUT_CTL0

Trigger control register

Address: 0x40012000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		TR_SEL [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [15:10]						TR_EDGE	TR_INV

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	TR_EDGE	Specifies if the (inverted) output trigger is treated as a level sensitive or edge sensitive trigger. '0': level sensitive. '1': edge sensitive trigger. The (inverted) output trigger duration needs to be at least 2 cycles on the consumer clock. the(inverted) output trigger is synchronized to the consumer clock and a two cycle pulse is generated on the consumer clock. Default Value: 0
8	TR_INV	Specifies if the output trigger is inverted. Default Value: 0
5 : 0	TR_SEL	Specifies input trigger. This field is typically set during the setup of a chip use case scenario. Changing this field while activated triggers are present on the input triggers may result in unpredictable behavior. Note that input trigger 0 (default value) is typically connected to a constant signal level of '0', and as a result will not cause HW activation of the output trigger. Default Value: 0

2.1.17 PERI_TR_GR2_TR_OUT_CTL0

Trigger control register

Address: 0x40012400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		TR_SEL [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [15:10]						TR_EDGE	TR_INV

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	TR_EDGE	Specifies if the (inverted) output trigger is treated as a level sensitive or edge sensitive trigger. '0': level sensitive. '1': edge sensitive trigger. The (inverted) output trigger duration needs to be at least 2 cycles on the consumer clock. the(inverted) output trigger is synchronized to the consumer clock and a two cycle pulse is generated on the consumer clock. Default Value: 0
8	TR_INV	Specifies if the output trigger is inverted. Default Value: 0
5 : 0	TR_SEL	Specifies input trigger. This field is typically set during the setup of a chip use case scenario. Changing this field while activated triggers are present on the input triggers may result in unpredictable behavior. Note that input trigger 0 (default value) is typically connected to a constant signal level of '0', and as a result will not cause HW activation of the output trigger. Default Value: 0

2.1.18 PERI_TR_GR4_TR_OUT_CTL0

Trigger control register

Address: 0x40012800

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		TR_SEL [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [15:10]						TR_EDGE	TR_INV

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	TR_EDGE	Specifies if the (inverted) output trigger is treated as a level sensitive or edge sensitive trigger. '0': level sensitive. '1': edge sensitive trigger. The (inverted) output trigger duration needs to be at least 2 cycles on the consumer clock. the(inverted) output trigger is synchronized to the consumer clock and a two cycle pulse is generated on the consumer clock. Default Value: 0
8	TR_INV	Specifies if the output trigger is inverted. Default Value: 0
5 : 0	TR_SEL	Specifies input trigger. This field is typically set during the setup of a chip use case scenario. Changing this field while activated triggers are present on the input triggers may result in unpredictable behavior. Note that input trigger 0 (default value) is typically connected to a constant signal level of '0', and as a result will not cause HW activation of the output trigger. Default Value: 0

2.1.19 PERI_TR_GR6_TR_OUT_CTL0

Trigger control register

Address: 0x40012C00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		TR_SEL [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [15:10]						TR_EDGE	TR_INV

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	TR_EDGE	Specifies if the (inverted) output trigger is treated as a level sensitive or edge sensitive trigger. '0': level sensitive. '1': edge sensitive trigger. The (inverted) output trigger duration needs to be at least 2 cycles on the consumer clock. the(inverted) output trigger is synchronized to the consumer clock and a two cycle pulse is generated on the consumer clock. Default Value: 0
8	TR_INV	Specifies if the output trigger is inverted. Default Value: 0
5 : 0	TR_SEL	Specifies input trigger. This field is typically set during the setup of a chip use case scenario. Changing this field while activated triggers are present on the input triggers may result in unpredictable behavior. Note that input trigger 0 (default value) is typically connected to a constant signal level of '0', and as a result will not cause HW activation of the output trigger. Default Value: 0

2.1.20 PERI_TR_GR9_TR_OUT_CTL0

Trigger control register

Address: 0x40013200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		TR_SEL [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [15:10]						TR_EDGE	TR_INV

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	TR_EDGE	Specifies if the (inverted) output trigger is treated as a level sensitive or edge sensitive trigger. '0': level sensitive. '1': edge sensitive trigger. The (inverted) output trigger duration needs to be at least 2 cycles on the consumer clock. the(inverted) output trigger is synchronized to the consumer clock and a two cycle pulse is generated on the consumer clock. Default Value: 0
8	TR_INV	Specifies if the output trigger is inverted. Default Value: 0
5 : 0	TR_SEL	Specifies input trigger. This field is typically set during the setup of a chip use case scenario. Changing this field while activated triggers are present on the input triggers may result in unpredictable behavior. Note that input trigger 0 (default value) is typically connected to a constant signal level of '0', and as a result will not cause HW activation of the output trigger. Default Value: 0

2.1.21 PERI_TR_GR11_TR_OUT_CTL0

Trigger control register

Address: 0x40013600

Retention: Retained

Bits	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SW Access	None	RW						
HW Access	None	R						
Name	None	TR_SEL [6:0]						

Bits	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	**Name**	**Description**
6 : 0	TR_SEL	Specifies input trigger. This field is typically set during the setup of a chip use case scenario. Changing this field while activated triggers are present on the input triggers may result in unpredictable behavior. Note that input trigger 0 (default value) is typically connected to a constant signal level of '0', and as a result will not cause HW activation of the output trigger. Default Value: 0

2.1.22 PERI_TR_GR12_TR_OUT_CTL0

Trigger control register

Address: 0x40013800

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			R				
Name	None [7:5]			TR_SEL [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4 : 0	TR_SEL	Specifies input trigger. This field is typically set during the setup of a chip use case scenario. Changing this field while activated triggers are present on the input triggers may result in unpredictable behavior. Note that input trigger 0 (default value) is typically connected to a constant signal level of '0', and as a result will not cause HW activation of the output trigger. Default Value: 0

2.1.23 PERI_TR_GR13_TR_OUT_CTL0

Trigger control register

Address: 0x40013A00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		TR_SEL [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	TR_SEL	Specifies input trigger. This field is typically set during the setup of a chip use case scenario. Changing this field while activated triggers are present on the input triggers may result in unpredictable behavior. Note that input trigger 0 (default value) is typically connected to a constant signal level of '0', and as a result will not cause HW activation of the output trigger. Default Value: 0

2.1.24 PERI_TR_GR14_TR_OUT_CTL0

Trigger control register

Address: 0x40013C00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		TR_SEL [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	TR_SEL	Specifies input trigger. This field is typically set during the setup of a chip use case scenario. Changing this field while activated triggers are present on the input triggers may result in unpredictable behavior. Note that input trigger 0 (default value) is typically connected to a constant signal level of '0', and as a result will not cause HW activation of the output trigger. Default Value: 0

2.1.25 PERI_PPU_PR0_ADDR0

PPU region address 0 (slave structure)

Address: 0x40014000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	This field specifies the most significant bits of the 32-bit address of an address region. The region size is defined by PPU_REGION_ATT.REGION_SIZE. A region of n Byte is always n Byte aligned. As a result, some of the lesser significant address bits of ADDR24 may be ignored in determining whether a bus transfer address is within an address region. E.g., a 64 KByte address region (REGION_SIZE is "15") is 64 KByte aligned, and ADDR24[7:0] are ignored. Default Value: Undefined

2.1.25 PERI_PPU_PR0_ADDR0 (continued)

7 : 0	SUBREGION_DISABLE	This field is used to individually disabled the eight equally sized subregions in which a region is partitioned. Subregion disable: Bit 0: subregion 0 disable. Bit 1: subregion 1 disable. Bit 2: subregion 2 disable. Bit 3: subregion 3 disable. Bit 4: subregion 4 disable. Bit 5: subregion 5 disable. Bit 6: subregion 6 disable. Bit 7: subregion 7 disable. E.g., a 64 KByte address region (REGION_SIZE is "15") has eight 8 KByte subregions. The access control as defined by PPU_REGION_ATT applies if the bus transfer address is within the address region AND the addressed subregion is NOT disabled. Note that the smallest region size is 256 B and the smallest subregion size is 32 B. Default Value: Undefined

2.1.26 PERI_PPU_PR0_ATT0

PPU region attributes 0 (slave structure)

Address: 0x40014004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	R	RW	RW	R	RW	RW
HW Access	None	R	R	R	R	R	R	R
Name	None	NS	PX	PW	PR	UX	UW	UR

Bits	15	14	13	12	11	10	9	8
SW Access	RW							R
HW Access	R							R
Name	PC_MASK_15_TO_1 [15:9]							PC_MASK_0

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None	RW				
HW Access	R	R	None	R				
Name	ENABLED	PC_MATCH	None	REGION_SIZE [28:24]				

Bits	Name	Description
31	ENABLED	Region enable: '0': Disabled. A disabled region will never result in a match on the bus transfer address. '1': Enabled. Note: a disabled address region performs logic gating to reduce dynamic power consumption. Default Value: 0
30	PC_MATCH	This field specifies if the PC field participates in the "matching" process or the "access evaluation" process: '0': PC field participates in "access evaluation". '1': PC field participates in "matching". Note that it is possible to define different access control for multiple protection contexts by using multiple protection structures with the same address region and PC_MATCH set to '1'. Default Value: Undefined

2.1.26 PERI_PPU_PR0_ATT0 (continued)

28 : 24	REGION_SIZE	This field specifies the region size: "0"-"6": Undefined. "7": 256 B region "8": 512 B region "9": 1 KB region "10": 2 KB region "11": 4 KB region "12": 8 KB region "13": 16 KB region "14": 32 KB region "15": 64 KB region "16": 128 KB region "17": 256 KB region "18": 512 KB region "19": 1 MB region "20": 2 MB region "21": 4 MB region "22": 8 MB region "23": 16 MB region "24": 32 MB region "25": 64 MB region "26": 128 MB region "27": 256 MB region "28": 512 MB region "29": 1 GB region "30": 2 GB region "31": 4 GB region Default Value: Undefined
15 : 9	PC_MASK_15_TO_1	This field specifies protection context identifier based access control. Bit i: protection context i+1 enable. If '0', protection context i+1 access is disabled; i.e. not allowed. If '1', protection context i+1 access is enabled; i.e. allowed. Default Value: Undefined
8	PC_MASK_0	This field specifies protection context identifier based access control for protection context "0". Default Value: 1
6	NS	Non-secure: '0': Secure (secure accesses allowed, non-secure access NOT allowed). '1': Non-secure (both secure and non-secure accesses allowed). Default Value: Undefined
5	PX	Privileged execute enable: '0': Disabled (privileged, execute accesses are NOT allowed). '1': Enabled (privileged, execute accesses are allowed). Default Value: 1
4	PW	Privileged write enable: '0': Disabled (privileged, write accesses are NOT allowed). '1': Enabled (privileged, write accesses are allowed). Default Value: Undefined
3	PR	Privileged read enable: '0': Disabled (privileged, read accesses are NOT allowed). '1': Enabled (privileged, read accesses are allowed). Default Value: Undefined
2	UX	User execute enable: '0': Disabled (user, execute accesses are NOT allowed). '1': Enabled (user, execute accesses are allowed). Default Value: 1

2.1.26 PERI_PPU_PR0_ATT0 (continued)

1	UW	User write enable: '0': Disabled (user, write accesses are NOT allowed). '1': Enabled (user, write accesses are allowed). Default Value: Undefined
0	UR	User read enable: '0': Disabled (user, read accesses are NOT allowed). '1': Enabled (user, read accesses are allowed). Default Value: Undefined

2.1.27 PERI_PPU_PR0_ADDR1

PPU region address 1 (master structure)

Address: 0x40014020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4194624
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 252

2.1.28 PERI_PPU_PR0_ATT1

PPU region attributes 1 (master structure)

Address: 0x40014024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	R	RW	R	R	RW	R
HW Access	None	R	R	R	R	R	R	R
Name	None	NS	PX	PW	PR	UX	UW	UR

Bits	15	14	13	12	11	10	9	8
SW Access	RW							R
HW Access	R							R
Name	PC_MASK_15_TO_1 [15:9]							PC_MASK_0

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None	R				
HW Access	R	R	None	R				
Name	ENABLED	PC_MATCH	None	REGION_SIZE [28:24]				

Bits	Name	Description
31	ENABLED	See corresponding field for PPU structure with programmable address. Default Value: 0
30	PC_MATCH	See corresponding field for PPU structure with programmable address. Default Value: Undefined
28 : 24	REGION_SIZE	See corresponding field for PPU structure with programmable address. "7": 256 B region Default Value: 7
15 : 9	PC_MASK_15_TO_1	See corresponding field for PPU structure with programmable address. Default Value: Undefined
8	PC_MASK_0	See corresponding field for PPU structure with programmable address. Default Value: 1
6	NS	See corresponding field for PPU structure with programmable address. Default Value: Undefined

2.1.28 PERI_PPU_PR0_ATT1 (continued)

5	PX	See corresponding field for PPU structure with programmable address. Note that this register is constant '0'; i.e. privileged execute accesses are NEVER allowed. Default Value: 0
4	PW	See corresponding field for PPU structure with programmable address. Default Value: Undefined
3	PR	See corresponding field for PPU structure with programmable address. Note that this register is constant '1'; i.e. privileged read accesses are ALWAYS allowed. Default Value: 1
2	UX	See corresponding field for PPU structure with programmable address. Note that this register is constant '0'; i.e. user execute accesses are NEVER allowed. Default Value: 0
1	UW	See corresponding field for PPU structure with programmable address. Default Value: Undefined
0	UR	See corresponding field for PPU structure with programmable address. Note that this register is constant '1'; i.e. user read accesses are ALWAYS allowed. Default Value: 1

2.1.29 PERI_PPU_PR1_ADDR1

PPU region address 1 (master structure)

Address: 0x40014060

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4194624
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 243

2.1.30 PERI_PPU_PR2_ADDR1

PPU region address 1 (master structure)

Address: 0x400140A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4194624
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 207

2.1.31 PERI_PPU_PR3_ADDR1

PPU region address 1 (master structure)

Address: 0x400140E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4194624
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 63

2.1.32 PERI_PPU_PR4_ADDR1

PPU region address 1 (master structure)

Address: 0x40014120

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4194625
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 252

2.1.33 PERI_PPU_PR5_ADDR1

PPU region address 1 (master structure)

Address: 0x40014160

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4194625
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 243

2.1.34 PERI_PPU_PR6_ADDR1

PPU region address 1 (master structure)

Address: 0x400141A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4194625
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 207

2.1.35 PERI_PPU_PR7_ADDR1

PPU region address 1 (master structure)

Address: 0x400141E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4194625
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 63

2.1.36 PERI_PPU_PR8_ADDR1

PPU region address 1 (master structure)

Address: 0x40014220

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4194626
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 252

2.1.37 PERI_PPU_PR9_ADDR1

PPU region address 1 (master structure)

Address: 0x40014260

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4194626
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 243

2.1.38 PERI_PPU_PR10_ADDR1

PPU region address 1 (master structure)

Address: 0x400142A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4194626
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 207

2.1.39 PERI_PPU_PR11_ADDR1

PPU region address 1 (master structure)

Address: 0x400142E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4194626
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 63

2.1.40 PERI_PPU_PR12_ADDR1

PPU region address 1 (master structure)

Address: 0x40014320

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4194627
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 252

2.1.41 PERI_PPU_PR13_ADDR1

PPU region address 1 (master structure)

Address: 0x40014360

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4194627
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 243

2.1.42 PERI_PPU_PR14_ADDR1

PPU region address 1 (master structure)

Address: 0x400143A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4194627
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 207

2.1.43 PERI_PPU_PR15_ADDR1

PPU region address 1 (master structure)

Address: 0x400143E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4194627
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 63

2.1.44 PERI_PPU_GR0_ADDR0

PPU region address 0 (slave structure)

Address: 0x40015000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": address of protected region. Note: this field is read-only. Its value is chip specific. Default Value: 4194304
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Note: this field is read-only. Its value is chip specific. Default Value: 0

2.1.45 PERI_PPU_GR0_ATT0

PPU region attributes 0 (slave structure)

Address: 0x40015004

Retention: Retained

Bits	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SW Access	None	RW	R	RW	RW	R	RW	RW
HW Access	None	R	R	R	R	R	R	R
Name	None	NS	PX	PW	PR	UX	UW	UR

Bits	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SW Access	RW							R
HW Access	R							R
Name	PC_MASK_15_TO_1 [15:9]							PC_MASK_0

Bits	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**
SW Access	RW	RW	None	R				
HW Access	R	R	None	R				
Name	ENABLED	PC_MATCH	None	REGION_SIZE [28:24]				

Bits	**Name**	**Description**
31	ENABLED	See corresponding field for PPU structure with programmable address. Default Value: 0
30	PC_MATCH	See corresponding field for PPU structure with programmable address. Default Value: Undefined
28 : 24	REGION_SIZE	See corresponding field for PPU structure with programmable address. Note: this field is read-only. Its value is chip specific. Default Value: 19
15 : 9	PC_MASK_15_TO_1	See corresponding field for PPU structure with programmable address. Default Value: Undefined
8	PC_MASK_0	See corresponding field for PPU structure with programmable address. Default Value: 1
6	NS	See corresponding field for PPU structure with programmable address. Default Value: Undefined

2.1.45 PERI_PPU_GR0_ATT0 (continued)

5	PX	See corresponding field for PPU structure with programmable address. Note that this register is constant '1'; i.e. user execute accesses are ALWAYS allowed. Default Value: 1
4	PW	See corresponding field for PPU structure with programmable address. Default Value: Undefined
3	PR	See corresponding field for PPU structure with programmable address. Default Value: Undefined
2	UX	See corresponding field for PPU structure with programmable address. Note that this register is constant '1'; i.e. user execute accesses are ALWAYS allowed. Default Value: 1
1	UW	See corresponding field for PPU structure with programmable address. Default Value: Undefined
0	UR	See corresponding field for PPU structure with programmable address. Default Value: Undefined

2.1.46 PERI_PPU_GR0_ADDR1

PPU region address 1 (master structure)

Address: 0x40015020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4194640
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 252

2.1.47 PERI_PPU_GR0_ATT1

PPU region attributes 1 (master structure)

Address: 0x40015024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	R	RW	R	R	RW	R
HW Access	None	R	R	R	R	R	R	R
Name	None	NS	PX	PW	PR	UX	UW	UR

Bits	15	14	13	12	11	10	9	8
SW Access	RW							R
HW Access	R							R
Name	PC_MASK_15_TO_1 [15:9]							PC_MASK_0

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None	R				
HW Access	R	R	None	R				
Name	ENABLED	PC_MATCH	None	REGION_SIZE [28:24]				

Bits	Name	Description
31	ENABLED	See corresponding field for PPU structure with programmable address. Default Value: 0
30	PC_MATCH	See corresponding field for PPU structure with programmable address. Default Value: Undefined
28 : 24	REGION_SIZE	See corresponding field for PPU structure with programmable address. "7": 256 B region Default Value: 7
15 : 9	PC_MASK_15_TO_1	See corresponding field for PPU structure with programmable address. Default Value: Undefined
8	PC_MASK_0	See corresponding field for PPU structure with programmable address. Default Value: 1
6	NS	See corresponding field for PPU structure with programmable address. Default Value: Undefined

2.1.47 PERI_PPU_GR0_ATT1 (continued)

5	PX	See corresponding field for PPU structure with programmable address. Note that this register is constant '0'; i.e. privileged execute accesses are NEVER allowed. Default Value: 0
4	PW	See corresponding field for PPU structure with programmable address. Default Value: Undefined
3	PR	See corresponding field for PPU structure with programmable address. Note that this register is constant '1'; i.e. privileged read accesses are ALWAYS allowed. Default Value: 1
2	UX	See corresponding field for PPU structure with programmable address. Note that this register is constant '0'; i.e. user execute accesses are NEVER allowed. Default Value: 0
1	UW	See corresponding field for PPU structure with programmable address. Default Value: Undefined
0	UR	See corresponding field for PPU structure with programmable address. Note that this register is constant '1'; i.e. user read accesses are ALWAYS allowed. Default Value: 1

2.1.48 PERI_PPU_GR1_ADDR0

PPU region address 0 (slave structure)

Address: 0x40015040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": address of protected region. Note: this field is read-only. Its value is chip specific. Default Value: 4198400
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Note: this field is read-only. Its value is chip specific. Default Value: 0

2.1.49 PERI_PPU_GR1_ADDR1

PPU region address 1 (master structure)

Address: 0x40015060

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4194640
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 243

2.1.50 PERI_PPU_GR2_ADDR0

PPU region address 0 (slave structure)

Address: 0x40015080

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": address of protected region. Note: this field is read-only. Its value is chip specific. Default Value: 4202496
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Note: this field is read-only. Its value is chip specific. Default Value: 0

2.1.51 PERI_PPU_GR2_ADDR1

PPU region address 1 (master structure)

Address: 0x400150A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4194640
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 207

2.1.52 PERI_PPU_GR3_ADDR0

PPU region address 0 (slave structure)

Address: 0x400150C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": address of protected region. Note: this field is read-only. Its value is chip specific. Default Value: 4206592
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Note: this field is read-only. Its value is chip specific. Default Value: 0

2.1.53 PERI_PPU_GR3_ADDR1

PPU region address 1 (master structure)

Address: 0x400150E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4194640
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 63

2.1.54 PERI_PPU_GR4_ADDR0

PPU region address 0 (slave structure)

Address: 0x40015100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": address of protected region. Note: this field is read-only. Its value is chip specific. Default Value: 4210688
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Note: this field is read-only. Its value is chip specific. Default Value: 0

2.1.55 PERI_PPU_GR4_ADDR1

PPU region address 1 (master structure)

Address: 0x40015120

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4194641
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 252

2.1.56 PERI_PPU_GR6_ADDR0

PPU region address 0 (slave structure)

Address: 0x40015180

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": address of protected region. Note: this field is read-only. Its value is chip specific. Default Value: 4218880
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Note: this field is read-only. Its value is chip specific. Default Value: 0

2.1.57 PERI_PPU_GR6_ADDR1

PPU region address 1 (master structure)

Address: 0x400151A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4194641
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 207

2.1.58 PERI_PPU_GR9_ADDR0

PPU region address 0 (slave structure)

Address: 0x40015240

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": address of protected region. Note: this field is read-only. Its value is chip specific. Default Value: 4259840
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Note: this field is read-only. Its value is chip specific. Default Value: 0

2.1.59 PERI_PPU_GR9_ATT0

PPU region attributes 0 (slave structure)

Address: 0x40015244

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	R	RW	RW	R	RW	RW
HW Access	None	R	R	R	R	R	R	R
Name	None	NS	PX	PW	PR	UX	UW	UR

Bits	15	14	13	12	11	10	9	8
SW Access	RW							R
HW Access	R							R
Name	PC_MASK_15_TO_1 [15:9]							PC_MASK_0

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None	R				
HW Access	R	R	None	R				
Name	ENABLED	PC_MATCH	None	REGION_SIZE [28:24]				

Bits	Name	Description
31	ENABLED	See corresponding field for PPU structure with programmable address. Default Value: 0
30	PC_MATCH	See corresponding field for PPU structure with programmable address. Default Value: Undefined
28 : 24	REGION_SIZE	See corresponding field for PPU structure with programmable address. Note: this field is read-only. Its value is chip specific. Default Value: 23
15 : 9	PC_MASK_15_TO_1	See corresponding field for PPU structure with programmable address. Default Value: Undefined
8	PC_MASK_0	See corresponding field for PPU structure with programmable address. Default Value: 1
6	NS	See corresponding field for PPU structure with programmable address. Default Value: Undefined

2.1.59 PERI_PPU_GR9_ATT0 (continued)

5	PX	See corresponding field for PPU structure with programmable address. Note that this register is constant '1'; i.e. user execute accesses are ALWAYS allowed. Default Value: 1
4	PW	See corresponding field for PPU structure with programmable address. Default Value: Undefined
3	PR	See corresponding field for PPU structure with programmable address. Default Value: Undefined
2	UX	See corresponding field for PPU structure with programmable address. Note that this register is constant '1'; i.e. user execute accesses are ALWAYS allowed. Default Value: 1
1	UW	See corresponding field for PPU structure with programmable address. Default Value: Undefined
0	UR	See corresponding field for PPU structure with programmable address. Default Value: Undefined

2.1.60 PERI_PPU_GR9_ADDR1

PPU region address 1 (master structure)

Address: 0x40015260

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4194642
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 243

2.1.61 PERI_PPU_GR10_ADDR0

PPU region address 0 (slave structure)

Address: 0x40015280

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": address of protected region. Note: this field is read-only. Its value is chip specific. Default Value: 4366336
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Note: this field is read-only. Its value is chip specific. Default Value: 0

2.1.62 PERI_PPU_GR10_ADDR1

PPU region address 1 (master structure)

Address: 0x400152A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4194642
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 207

2.1.63 PERI_GR1_PPU_SL0_ADDR0

PPU region address 0 (slave structure)

Address: 0x40100000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": address of protected region. Note: this field is read-only. Its value is chip specific. Default Value: 4198400
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Note: this field is read-only. Its value is chip specific. Default Value: 0

2.1.64 PERI_GR1_PPU_SL0_ATT0

PPU region attributes 0 (slave structure)

Address: 0x40100004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	R	RW	RW	R	RW	RW
HW Access	None	R	R	R	R	R	R	R
Name	None	NS	PX	PW	PR	UX	UW	UR

Bits	15	14	13	12	11	10	9	8
SW Access	RW							R
HW Access	R							R
Name	PC_MASK_15_TO_1 [15:9]							PC_MASK_0

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None	R				
HW Access	R	R	None	R				
Name	ENABLED	PC_MATCH	None	REGION_SIZE [28:24]				

Bits	Name	Description
31	ENABLED	See corresponding field for PPU structure with programmable address. Default Value: 0
30	PC_MATCH	See corresponding field for PPU structure with programmable address. Default Value: Undefined
28 : 24	REGION_SIZE	See corresponding field for PPU structure with programmable address. Note: this field is read-only. Its value is chip specific. Default Value: 15
15 : 9	PC_MASK_15_TO_1	See corresponding field for PPU structure with programmable address. Default Value: Undefined
8	PC_MASK_0	See corresponding field for PPU structure with programmable address. Default Value: 1
6	NS	See corresponding field for PPU structure with programmable address. Default Value: Undefined

2.1.64 PERI_GR1_PPU_SL0_ATT0 (continued)

5	PX	See corresponding field for PPU structure with programmable address. Note that this register is constant '1'; i.e. user execute accesses are ALWAYS allowed. Default Value: 1
4	PW	See corresponding field for PPU structure with programmable address. Default Value: Undefined
3	PR	See corresponding field for PPU structure with programmable address. Default Value: Undefined
2	UX	See corresponding field for PPU structure with programmable address. Note that this register is constant '1'; i.e. user execute accesses are ALWAYS allowed. Default Value: 1
1	UW	See corresponding field for PPU structure with programmable address. Default Value: Undefined
0	UR	See corresponding field for PPU structure with programmable address. Default Value: Undefined

2.1.65 PERI_GR1_PPU_SL0_ADDR1

PPU region address 1 (master structure)

Address: 0x40100020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4198400
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 252

2.1.66 PERI_GR1_PPU_SL0_ATT1

PPU region attributes 1 (master structure)

Address: 0x40100024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	R	RW	R	R	RW	R
HW Access	None	R	R	R	R	R	R	R
Name	None	NS	PX	PW	PR	UX	UW	UR

Bits	15	14	13	12	11	10	9	8
SW Access	RW							R
HW Access	R							R
Name	PC_MASK_15_TO_1 [15:9]							PC_MASK_0

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None	R				
HW Access	R	R	None	R				
Name	ENABLED	PC_MATCH	None	REGION_SIZE [28:24]				

Bits	Name	Description
31	ENABLED	See corresponding field for PPU structure with programmable address. Default Value: 0
30	PC_MATCH	See corresponding field for PPU structure with programmable address. Default Value: Undefined
28 : 24	REGION_SIZE	See corresponding field for PPU structure with programmable address. "7": 256 B region Default Value: 7
15 : 9	PC_MASK_15_TO_1	See corresponding field for PPU structure with programmable address. Default Value: Undefined
8	PC_MASK_0	See corresponding field for PPU structure with programmable address. Default Value: 1
6	NS	See corresponding field for PPU structure with programmable address. Default Value: Undefined

2.1.66 PERI_GR1_PPU_SL0_ATT1 (continued)

5	PX	See corresponding field for PPU structure with programmable address. Note that this register is constant '0'; i.e. privileged execute accesses are NEVER allowed. Default Value: 0
4	PW	See corresponding field for PPU structure with programmable address. Default Value: Undefined
3	PR	See corresponding field for PPU structure with programmable address. Note that this register is constant '1'; i.e. privileged read accesses are ALWAYS allowed. Default Value: 1
2	UX	See corresponding field for PPU structure with programmable address. Note that this register is constant '0'; i.e. user execute accesses are NEVER allowed. Default Value: 0
1	UW	See corresponding field for PPU structure with programmable address. Default Value: Undefined
0	UR	See corresponding field for PPU structure with programmable address. Note that this register is constant '1'; i.e. user read accesses are ALWAYS allowed. Default Value: 1

2.1.67 PERI_GR1_PPU_SL1_ADDR0

PPU region address 0 (slave structure)

Address: 0x40100040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": address of protected region. Note: this field is read-only. Its value is chip specific. Default Value: 4198656
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Note: this field is read-only. Its value is chip specific. Default Value: 0

2.1.68 PERI_GR1_PPU_SL1_ADDR1

PPU region address 1 (master structure)

Address: 0x40100060

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4198400
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 243

2.1.69 PERI_GR2_PPU_SL0_ADDR0

PPU region address 0 (slave structure)

Address: 0x40200000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": address of protected region. Note: this field is read-only. Its value is chip specific. Default Value: 4202496
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Note: this field is read-only. Its value is chip specific. Default Value: 0

2.1.70 PERI_GR2_PPU_SL1_ADDR0

PPU region address 0 (slave structure)

Address: 0x40200040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": address of protected region. Note: this field is read-only. Its value is chip specific. Default Value: 4202752
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Note: this field is read-only. Its value is chip specific. Default Value: 0

2.1.71 PERI_GR2_PPU_SL1_ADDR1

PPU region address 1 (master structure)

Address: 0x40200060

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4202496
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 243

2.1.72 PERI_GR2_PPU_SL2_ADDR0

PPU region address 0 (slave structure)

Address: 0x40200080

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": address of protected region. Note: this field is read-only. Its value is chip specific. Default Value: 4203008
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Note: this field is read-only. Its value is chip specific. Default Value: 0

2.1.73 PERI_GR2_PPU_SL2_ADDR1

PPU region address 1 (master structure)

Address: 0x402000A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4202496
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 207

2.1.74 PERI_GR2_PPU_SL3_ADDR0

PPU region address 0 (slave structure)

Address: 0x402000C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": address of protected region. Note: this field is read-only. Its value is chip specific. Default Value: 4203264
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Note: this field is read-only. Its value is chip specific. Default Value: 0

2.1.75 PERI_GR2_PPU_SL3_ADDR1

PPU region address 1 (master structure)

Address: 0x402000E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4202496
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 63

2.1.76 PERI_GR2_PPU_SL4_ADDR0

PPU region address 0 (slave structure)

Address: 0x40200100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": address of protected region. Note: this field is read-only. Its value is chip specific. Default Value: 4203520
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Note: this field is read-only. Its value is chip specific. Default Value: 0

2.1.77 PERI_GR2_PPU_SL4_ADDR1

PPU region address 1 (master structure)

Address: 0x40200120

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4202497
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 252

2.1.78 PERI_GR2_PPU_SL5_ADDR0

PPU region address 0 (slave structure)

Address: 0x40200140

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": address of protected region. Note: this field is read-only. Its value is chip specific. Default Value: 4203776
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Note: this field is read-only. Its value is chip specific. Default Value: 0

2.1.79 PERI_GR2_PPU_SL5_ADDR1

PPU region address 1 (master structure)

Address: 0x40200160

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4202497
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 243

2.1.80 PERI_GR2_PPU_SL6_ADDR0

PPU region address 0 (slave structure)

Address: 0x40200180

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": address of protected region. Note: this field is read-only. Its value is chip specific. Default Value: 4204032
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Note: this field is read-only. Its value is chip specific. Default Value: 0

2.1.81 PERI_GR2_PPU_SL6_ADDR1

PPU region address 1 (master structure)

Address: 0x402001A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4202497
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 207

2.1.82 PERI_GR2_PPU_SL7_ADDR0

PPU region address 0 (slave structure)

Address: 0x402001C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": address of protected region. Note: this field is read-only. Its value is chip specific. Default Value: 4204288
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Note: this field is read-only. Its value is chip specific. Default Value: 0

2.1.83 PERI_GR2_PPU_SL7_ADDR1

PPU region address 1 (master structure)

Address: 0x402001E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4202497
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 63

2.1.84 PERI_GR2_PPU_SL8_ADDR0

PPU region address 0 (slave structure)

Address: 0x40200200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": address of protected region. Note: this field is read-only. Its value is chip specific. Default Value: 4204544
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Note: this field is read-only. Its value is chip specific. Default Value: 0

2.1.85 PERI_GR2_PPU_SL8_ATT0

PPU region attributes 0 (slave structure)

Address: 0x40200204

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	R	RW	RW	R	RW	RW
HW Access	None	R	R	R	R	R	R	R
Name	None	NS	PX	PW	PR	UX	UW	UR

Bits	15	14	13	12	11	10	9	8
SW Access	RW							R
HW Access	R							R
Name	PC_MASK_15_TO_1 [15:9]							PC_MASK_0

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None	R				
HW Access	R	R	None	R				
Name	ENABLED	PC_MATCH	None	REGION_SIZE [28:24]				

Bits	Name	Description
31	ENABLED	See corresponding field for PPU structure with programmable address. Default Value: 0
30	PC_MATCH	See corresponding field for PPU structure with programmable address. Default Value: Undefined
28 : 24	REGION_SIZE	See corresponding field for PPU structure with programmable address. Note: this field is read-only. Its value is chip specific. Default Value: 11
15 : 9	PC_MASK_15_TO_1	See corresponding field for PPU structure with programmable address. Default Value: Undefined
8	PC_MASK_0	See corresponding field for PPU structure with programmable address. Default Value: 1
6	NS	See corresponding field for PPU structure with programmable address. Default Value: Undefined

2.1.85 PERI_GR2_PPU_SL8_ATT0 (continued)

5	PX	See corresponding field for PPU structure with programmable address. Note that this register is constant '1'; i.e. user execute accesses are ALWAYS allowed. Default Value: 1
4	PW	See corresponding field for PPU structure with programmable address. Default Value: Undefined
3	PR	See corresponding field for PPU structure with programmable address. Default Value: Undefined
2	UX	See corresponding field for PPU structure with programmable address. Note that this register is constant '1'; i.e. user execute accesses are ALWAYS allowed. Default Value: 1
1	UW	See corresponding field for PPU structure with programmable address. Default Value: Undefined
0	UR	See corresponding field for PPU structure with programmable address. Default Value: Undefined

2.1.86 PERI_GR2_PPU_SL8_ADDR1

PPU region address 1 (master structure)

Address: 0x40200220

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4202498
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 252

2.1.87 PERI_GR2_PPU_SL9_ADDR1

PPU region address 1 (master structure)

Address: 0x40200260

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4202498
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 243

2.1.88 PERI_GR2_PPU_SL12_ADDR0

PPU region address 0 (slave structure)

Address: 0x40200300

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": address of protected region. Note: this field is read-only. Its value is chip specific. Default Value: 4205568
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Note: this field is read-only. Its value is chip specific. Default Value: 0

2.1.89 PERI_GR2_PPU_SL12_ADDR1

PPU region address 1 (master structure)

Address: 0x40200320

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4202499
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 252

2.1.90 PERI_GR2_PPU_SL13_ADDR0

PPU region address 0 (slave structure)

Address: 0x40200340

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": address of protected region. Note: this field is read-only. Its value is chip specific. Default Value: 4205824
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Note: this field is read-only. Its value is chip specific. Default Value: 0

2.1.91 PERI_GR2_PPU_SL13_ADDR1

PPU region address 1 (master structure)

Address: 0x40200360

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4202499
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 243

2.1.92 PERI_GR2_PPU_RG0_ADDR0

PPU region address 0 (slave structure)

Address: 0x40201000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": address of protected region. Note: this field is read-only. Its value is chip specific. Default Value: 4203264
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Note: this field is read-only. Its value is chip specific. Default Value: 254

2.1.93 PERI_GR2_PPU_RG0_ATT0

PPU region attributes 0 (slave structure)

Address: 0x40201004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	R	RW	RW	R	RW	RW
HW Access	None	R	R	R	R	R	R	R
Name	None	NS	PX	PW	PR	UX	UW	UR

Bits	15	14	13	12	11	10	9	8
SW Access	RW							R
HW Access	R							R
Name	PC_MASK_15_TO_1 [15:9]							PC_MASK_0

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None	R				
HW Access	R	R	None	R				
Name	ENABLED	PC_MATCH	None	REGION_SIZE [28:24]				

Bits	Name	Description
31	ENABLED	See corresponding field for PPU structure with programmable address. Default Value: 0
30	PC_MATCH	See corresponding field for PPU structure with programmable address. Default Value: Undefined
28 : 24	REGION_SIZE	See corresponding field for PPU structure with programmable address. Note: this field is read-only. Its value is chip specific. Default Value: 7
15 : 9	PC_MASK_15_TO_1	See corresponding field for PPU structure with programmable address. Default Value: Undefined
8	PC_MASK_0	See corresponding field for PPU structure with programmable address. Default Value: 1
6	NS	See corresponding field for PPU structure with programmable address. Default Value: Undefined

2.1.93 PERI_GR2_PPU_RG0_ATT0 (continued)

5	PX	See corresponding field for PPU structure with programmable address. Note that this register is constant '1'; i.e. user execute accesses are ALWAYS allowed. Default Value: 1
4	PW	See corresponding field for PPU structure with programmable address. Default Value: Undefined
3	PR	See corresponding field for PPU structure with programmable address. Default Value: Undefined
2	UX	See corresponding field for PPU structure with programmable address. Note that this register is constant '1'; i.e. user execute accesses are ALWAYS allowed. Default Value: 1
1	UW	See corresponding field for PPU structure with programmable address. Default Value: Undefined
0	UR	See corresponding field for PPU structure with programmable address. Default Value: Undefined

2.1.94 PERI_GR2_PPU_RG0_ADDR1

PPU region address 1 (master structure)

Address: 0x40201020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4202512
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 252

2.1.95 PERI_GR2_PPU_RG0_ATT1

PPU region attributes 1 (master structure)

Address: 0x40201024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	R	RW	R	R	RW	R
HW Access	None	R	R	R	R	R	R	R
Name	None	NS	PX	PW	PR	UX	UW	UR

Bits	15	14	13	12	11	10	9	8
SW Access	RW							R
HW Access	R							R
Name	PC_MASK_15_TO_1 [15:9]							PC_MASK_0

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None	R				
HW Access	R	R	None	R				
Name	ENABLED	PC_MATCH	None	REGION_SIZE [28:24]				

Bits	Name	Description
31	ENABLED	See corresponding field for PPU structure with programmable address. Default Value: 0
30	PC_MATCH	See corresponding field for PPU structure with programmable address. Default Value: Undefined
28 : 24	REGION_SIZE	See corresponding field for PPU structure with programmable address. "7": 256 B region Default Value: 7
15 : 9	PC_MASK_15_TO_1	See corresponding field for PPU structure with programmable address. Default Value: Undefined
8	PC_MASK_0	See corresponding field for PPU structure with programmable address. Default Value: 1
6	NS	See corresponding field for PPU structure with programmable address. Default Value: Undefined

2.1.95 PERI_GR2_PPU_RG0_ATT1 (continued)

5	PX	See corresponding field for PPU structure with programmable address. Note that this register is constant '0'; i.e. privileged execute accesses are NEVER allowed. Default Value: 0
4	PW	See corresponding field for PPU structure with programmable address. Default Value: Undefined
3	PR	See corresponding field for PPU structure with programmable address. Note that this register is constant '1'; i.e. privileged read accesses are ALWAYS allowed. Default Value: 1
2	UX	See corresponding field for PPU structure with programmable address. Note that this register is constant '0'; i.e. user execute accesses are NEVER allowed. Default Value: 0
1	UW	See corresponding field for PPU structure with programmable address. Default Value: Undefined
0	UR	See corresponding field for PPU structure with programmable address. Note that this register is constant '1'; i.e. user read accesses are ALWAYS allowed. Default Value: 1

2.1.96 PERI_GR2_PPU_RG1_ADDR0

PPU region address 0 (slave structure)

Address: 0x40201040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": address of protected region. Note: this field is read-only. Its value is chip specific. Default Value: 4203264
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Note: this field is read-only. Its value is chip specific. Default Value: 253

2.1.97 PERI_GR2_PPU_RG1_ADDR1

PPU region address 1 (master structure)

Address: 0x40201060

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4202512
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 243

2.1.98 PERI_GR2_PPU_RG2_ADDR0

PPU region address 0 (slave structure)

Address: 0x40201080

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": address of protected region. Note: this field is read-only. Its value is chip specific. Default Value: 4203264
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Note: this field is read-only. Its value is chip specific. Default Value: 251

2.1.99 PERI_GR2_PPU_RG2_ADDR1

PPU region address 1 (master structure)

Address: 0x402010A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4202512
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 207

2.1.100 PERI_GR2_PPU_RG3_ADDR0

PPU region address 0 (slave structure)

Address: 0x402010C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": address of protected region. Note: this field is read-only. Its value is chip specific. Default Value: 4203264
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Note: this field is read-only. Its value is chip specific. Default Value: 247

2.1.101 PERI_GR2_PPU_RG3_ADDR1

PPU region address 1 (master structure)

Address: 0x402010E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4202512
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 63

2.1.102 PERI_GR2_PPU_RG4_ADDR0

PPU region address 0 (slave structure)

Address: 0x40201100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": address of protected region. Note: this field is read-only. Its value is chip specific. Default Value: 4203264
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Note: this field is read-only. Its value is chip specific. Default Value: 239

2.1.103 PERI_GR2_PPU_RG4_ADDR1

PPU region address 1 (master structure)

Address: 0x40201120

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4202513
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 252

2.1.104 PERI_GR2_PPU_RG5_ADDR0

PPU region address 0 (slave structure)

Address: 0x40201140

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": address of protected region. Note: this field is read-only. Its value is chip specific. Default Value: 4203264
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Note: this field is read-only. Its value is chip specific. Default Value: 223

2.1.105 PERI_GR2_PPU_RG5_ADDR1

PPU region address 1 (master structure)

Address: 0x40201160

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4202513
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 243

2.1.106 PERI_GR2_PPU_RG6_ADDR0

PPU region address 0 (slave structure)

Address: 0x40201180

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": address of protected region. Note: this field is read-only. Its value is chip specific. Default Value: 4203264
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Note: this field is read-only. Its value is chip specific. Default Value: 191

2.1.107 PERI_GR2_PPU_RG6_ADDR1

PPU region address 1 (master structure)

Address: 0x402011A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4202513
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 207

2.1.108 PERI_GR2_PPU_RG7_ADDR0

PPU region address 0 (slave structure)

Address: 0x402011C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": address of protected region. Note: this field is read-only. Its value is chip specific. Default Value: 4203264
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Note: this field is read-only. Its value is chip specific. Default Value: 127

2.1.109 PERI_GR2_PPU_RG7_ADDR1

PPU region address 1 (master structure)

Address: 0x402011E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4202513
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 63

2.1.110 PERI_GR2_PPU_RG8_ADDR0

PPU region address 0 (slave structure)

Address: 0x40201200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": address of protected region. Note: this field is read-only. Its value is chip specific. Default Value: 4203281
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Note: this field is read-only. Its value is chip specific. Default Value: 254

2.1.111 PERI_GR2_PPU_RG8_ADDR1

PPU region address 1 (master structure)

Address: 0x40201220

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4202514
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 252

2.1.112 PERI_GR2_PPU_RG9_ADDR0

PPU region address 0 (slave structure)

Address: 0x40201240

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": address of protected region. Note: this field is read-only. Its value is chip specific. Default Value: 4203281
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Note: this field is read-only. Its value is chip specific. Default Value: 253

2.1.113 PERI_GR2_PPU_RG9_ADDR1

PPU region address 1 (master structure)

Address: 0x40201260

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4202514
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 243

2.1.114 PERI_GR2_PPU_RG10_ADDR0

PPU region address 0 (slave structure)

Address: 0x40201280

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": address of protected region. Note: this field is read-only. Its value is chip specific. Default Value: 4203281
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Note: this field is read-only. Its value is chip specific. Default Value: 251

2.1.115 PERI_GR2_PPU_RG10_ADDR1

PPU region address 1 (master structure)

Address: 0x402012A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4202514
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 207

2.1.116 PERI_GR2_PPU_RG11_ADDR0

PPU region address 0 (slave structure)

Address: 0x402012C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": address of protected region. Note: this field is read-only. Its value is chip specific. Default Value: 4203281
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Note: this field is read-only. Its value is chip specific. Default Value: 247

2.1.117 PERI_GR2_PPU_RG11_ADDR1

PPU region address 1 (master structure)

Address: 0x402012E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4202514
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 63

2.1.118 PERI_GR2_PPU_RG12_ADDR0

PPU region address 0 (slave structure)

Address: 0x40201300

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": address of protected region. Note: this field is read-only. Its value is chip specific. Default Value: 4203281
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Note: this field is read-only. Its value is chip specific. Default Value: 239

2.1.119 PERI_GR2_PPU_RG12_ADDR1

PPU region address 1 (master structure)

Address: 0x40201320

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4202515
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 252

2.1.120 PERI_GR2_PPU_RG13_ADDR0

PPU region address 0 (slave structure)

Address: 0x40201340

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": address of protected region. Note: this field is read-only. Its value is chip specific. Default Value: 4203281
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Note: this field is read-only. Its value is chip specific. Default Value: 223

2.1.121 PERI_GR2_PPU_RG13_ADDR1

PPU region address 1 (master structure)

Address: 0x40201360

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4202515
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 243

2.1.122 PERI_GR2_PPU_RG14_ADDR0

PPU region address 0 (slave structure)

Address: 0x40201380

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": address of protected region. Note: this field is read-only. Its value is chip specific. Default Value: 4203281
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Note: this field is read-only. Its value is chip specific. Default Value: 191

2.1.123 PERI_GR2_PPU_RG14_ADDR1

PPU region address 1 (master structure)

Address: 0x402013A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4202515
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 207

2.1.124 PERI_GR2_PPU_RG15_ADDR0

PPU region address 0 (slave structure)

Address: 0x402013C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": address of protected region. Note: this field is read-only. Its value is chip specific. Default Value: 4203281
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Note: this field is read-only. Its value is chip specific. Default Value: 127

2.1.125 PERI_GR2_PPU_RG15_ADDR1

PPU region address 1 (master structure)

Address: 0x402013E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4202515
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 63

2.1.126 PERI_GR2_PPU_RG16_ADDR0

PPU region address 0 (slave structure)

Address: 0x40201400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": address of protected region. Note: this field is read-only. Its value is chip specific. Default Value: 4204554
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Note: this field is read-only. Its value is chip specific. Default Value: 254

2.1.127 PERI_GR2_PPU_RG16_ADDR1

PPU region address 1 (master structure)

Address: 0x40201420

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4202516
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 252

2.1.128 PERI_GR2_PPU_RG17_ADDR0

PPU region address 0 (slave structure)

Address: 0x40201440

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": address of protected region. Note: this field is read-only. Its value is chip specific. Default Value: 4204554
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Note: this field is read-only. Its value is chip specific. Default Value: 253

2.1.129 PERI_GR2_PPU_RG17_ADDR1

PPU region address 1 (master structure)

Address: 0x40201460

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4202516
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 243

2.1.130 PERI_GR2_PPU_RG18_ADDR0

PPU region address 0 (slave structure)

Address: 0x40201480

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": address of protected region. Note: this field is read-only. Its value is chip specific. Default Value: 4204554
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Note: this field is read-only. Its value is chip specific. Default Value: 251

2.1.131 PERI_GR2_PPU_RG18_ADDR1

PPU region address 1 (master structure)

Address: 0x402014A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4202516
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 207

2.1.132 PERI_GR2_PPU_RG19_ADDR0

PPU region address 0 (slave structure)

Address: 0x402014C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": address of protected region. Note: this field is read-only. Its value is chip specific. Default Value: 4204554
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Note: this field is read-only. Its value is chip specific. Default Value: 247

2.1.133 PERI_GR2_PPU_RG19_ADDR1

PPU region address 1 (master structure)

Address: 0x402014E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4202516
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 63

2.1.134 PERI_GR2_PPU_RG20_ADDR0

PPU region address 0 (slave structure)

Address: 0x40201500

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": address of protected region. Note: this field is read-only. Its value is chip specific. Default Value: 4204570
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Note: this field is read-only. Its value is chip specific. Default Value: 239

2.1.135 PERI_GR2_PPU_RG20_ADDR1

PPU region address 1 (master structure)

Address: 0x40201520

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4202517
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 252

2.1.136 PERI_GR2_PPU_RG21_ADDR0

PPU region address 0 (slave structure)

Address: 0x40201540

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": address of protected region. Note: this field is read-only. Its value is chip specific. Default Value: 4204570
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Note: this field is read-only. Its value is chip specific. Default Value: 223

2.1.137 PERI_GR2_PPU_RG21_ADDR1

PPU region address 1 (master structure)

Address: 0x40201560

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4202517
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 243

2.1.138 PERI_GR2_PPU_RG22_ADDR0

PPU region address 0 (slave structure)

Address: 0x40201580

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": address of protected region. Note: this field is read-only. Its value is chip specific. Default Value: 4204570
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Note: this field is read-only. Its value is chip specific. Default Value: 191

2.1.139 PERI_GR2_PPU_RG22_ADDR1

PPU region address 1 (master structure)

Address: 0x402015A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4202517
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 207

2.1.140 PERI_GR2_PPU_RG23_ADDR0

PPU region address 0 (slave structure)

Address: 0x402015C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": address of protected region. Note: this field is read-only. Its value is chip specific. Default Value: 4204570
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Note: this field is read-only. Its value is chip specific. Default Value: 127

2.1.141 PERI_GR2_PPU_RG23_ADDR1

PPU region address 1 (master structure)

Address: 0x402015E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4202517
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 63

2.1.142 PERI_GR2_PPU_RG24_ADDR0

PPU region address 0 (slave structure)

Address: 0x40201600

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": address of protected region. Note: this field is read-only. Its value is chip specific. Default Value: 4203520
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Note: this field is read-only. Its value is chip specific. Default Value: 252

2.1.143 PERI_GR2_PPU_RG24_ADDR1

PPU region address 1 (master structure)

Address: 0x40201620

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4202518
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 252

2.1.144 PERI_GR2_PPU_RG25_ADDR0

PPU region address 0 (slave structure)

Address: 0x40201640

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": address of protected region. Note: this field is read-only. Its value is chip specific. Default Value: 4203584
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Note: this field is read-only. Its value is chip specific. Default Value: 0

2.1.145 PERI_GR2_PPU_RG25_ATT0

PPU region attributes 0 (slave structure)

Address: 0x40201644

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	R	RW	RW	R	RW	RW
HW Access	None	R	R	R	R	R	R	R
Name	None	NS	PX	PW	PR	UX	UW	UR

Bits	15	14	13	12	11	10	9	8
SW Access	RW							R
HW Access	R							R
Name	PC_MASK_15_TO_1 [15:9]							PC_MASK_0

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None	R				
HW Access	R	R	None	R				
Name	ENABLED	PC_MATCH	None	REGION_SIZE [28:24]				

Bits	Name	Description
31	ENABLED	See corresponding field for PPU structure with programmable address. Default Value: 0
30	PC_MATCH	See corresponding field for PPU structure with programmable address. Default Value: Undefined
28 : 24	REGION_SIZE	See corresponding field for PPU structure with programmable address. Note: this field is read-only. Its value is chip specific. Default Value: 9
15 : 9	PC_MASK_15_TO_1	See corresponding field for PPU structure with programmable address. Default Value: Undefined
8	PC_MASK_0	See corresponding field for PPU structure with programmable address. Default Value: 1
6	NS	See corresponding field for PPU structure with programmable address. Default Value: Undefined

2.1.145 PERI_GR2_PPU_RG25_ATT0 (continued)

5	PX	See corresponding field for PPU structure with programmable address. Note that this register is constant '1'; i.e. user execute accesses are ALWAYS allowed. Default Value: 1
4	PW	See corresponding field for PPU structure with programmable address. Default Value: Undefined
3	PR	See corresponding field for PPU structure with programmable address. Default Value: Undefined
2	UX	See corresponding field for PPU structure with programmable address. Note that this register is constant '1'; i.e. user execute accesses are ALWAYS allowed. Default Value: 1
1	UW	See corresponding field for PPU structure with programmable address. Default Value: Undefined
0	UR	See corresponding field for PPU structure with programmable address. Default Value: Undefined

2.1.146 PERI_GR2_PPU_RG25_ADDR1

PPU region address 1 (master structure)

Address: 0x40201660

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4202518
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 243

2.1.147 PERI_GR2_PPU_RG26_ADDR0

PPU region address 0 (slave structure)

Address: 0x40201680

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": address of protected region. Note: this field is read-only. Its value is chip specific. Default Value: 4203588
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Note: this field is read-only. Its value is chip specific. Default Value: 0

2.1.148 PERI_GR2_PPU_RG26_ADDR1

PPU region address 1 (master structure)

Address: 0x402016A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4202518
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 207

2.1.149 PERI_GR2_PPU_RG27_ADDR0

PPU region address 0 (slave structure)

Address: 0x402016C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": address of protected region. Note: this field is read-only. Its value is chip specific. Default Value: 4203640
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Note: this field is read-only. Its value is chip specific. Default Value: 0

2.1.150 PERI_GR2_PPU_RG27_ADDR1

PPU region address 1 (master structure)

Address: 0x402016E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4202518
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 63

2.1.151 PERI_GR2_PPU_RG28_ADDR0

PPU region address 0 (slave structure)

Address: 0x40201700

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": address of protected region. Note: this field is read-only. Its value is chip specific. Default Value: 4203644
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Note: this field is read-only. Its value is chip specific. Default Value: 0

2.1.152 PERI_GR2_PPU_RG28_ADDR1

PPU region address 1 (master structure)

Address: 0x40201720

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4202519
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 252

2.1.153 PERI_GR3_PPU_SL0_ADDR0

PPU region address 0 (slave structure)

Address: 0x40300000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": address of protected region. Note: this field is read-only. Its value is chip specific. Default Value: 4206592
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Note: this field is read-only. Its value is chip specific. Default Value: 0

2.1.154 PERI_GR3_PPU_SL0_ADDR1

PPU region address 1 (master structure)

Address: 0x40300020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4206592
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 252

2.1.155 PERI_GR3_PPU_SL1_ADDR0

PPU region address 0 (slave structure)

Address: 0x40300040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": address of protected region. Note: this field is read-only. Its value is chip specific. Default Value: 4206848
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Note: this field is read-only. Its value is chip specific. Default Value: 0

2.1.156 PERI_GR3_PPU_SL1_ATT0

PPU region attributes 0 (slave structure)

Address: 0x40300044

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	R	RW	RW	R	RW	RW
HW Access	None	R	R	R	R	R	R	R
Name	None	NS	PX	PW	PR	UX	UW	UR

Bits	15	14	13	12	11	10	9	8
SW Access	RW							R
HW Access	R							R
Name	PC_MASK_15_TO_1 [15:9]							PC_MASK_0

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None	R				
HW Access	R	R	None	R				
Name	ENABLED	PC_MATCH	None	REGION_SIZE [28:24]				

Bits	Name	Description
31	ENABLED	See corresponding field for PPU structure with programmable address. Default Value: 0
30	PC_MATCH	See corresponding field for PPU structure with programmable address. Default Value: Undefined
28 : 24	REGION_SIZE	See corresponding field for PPU structure with programmable address. Note: this field is read-only. Its value is chip specific. Default Value: 13
15 : 9	PC_MASK_15_TO_1	See corresponding field for PPU structure with programmable address. Default Value: Undefined
8	PC_MASK_0	See corresponding field for PPU structure with programmable address. Default Value: 1
6	NS	See corresponding field for PPU structure with programmable address. Default Value: Undefined

2.1.156 PERI_GR3_PPU_SL1_ATT0 (continued)

5	PX	See corresponding field for PPU structure with programmable address. Note that this register is constant '1'; i.e. user execute accesses are ALWAYS allowed. Default Value: 1
4	PW	See corresponding field for PPU structure with programmable address. Default Value: Undefined
3	PR	See corresponding field for PPU structure with programmable address. Default Value: Undefined
2	UX	See corresponding field for PPU structure with programmable address. Note that this register is constant '1'; i.e. user execute accesses are ALWAYS allowed. Default Value: 1
1	UW	See corresponding field for PPU structure with programmable address. Default Value: Undefined
0	UR	See corresponding field for PPU structure with programmable address. Default Value: Undefined

2.1.157 PERI_GR3_PPU_SL1_ADDR1

PPU region address 1 (master structure)

Address: 0x40300060

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4206592
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 243

2.1.158 PERI_GR3_PPU_SL2_ADDR0

PPU region address 0 (slave structure)

Address: 0x40300080

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": address of protected region. Note: this field is read-only. Its value is chip specific. Default Value: 4207104
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Note: this field is read-only. Its value is chip specific. Default Value: 0

2.1.159 PERI_GR3_PPU_SL2_ADDR1

PPU region address 1 (master structure)

Address: 0x403000A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4206592
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 207

2.1.160 PERI_GR3_PPU_SL3_ADDR0

PPU region address 0 (slave structure)

Address: 0x403000C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": address of protected region. Note: this field is read-only. Its value is chip specific. Default Value: 4207360
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Note: this field is read-only. Its value is chip specific. Default Value: 0

2.1.161 PERI_GR3_PPU_SL3_ADDR1

PPU region address 1 (master structure)

Address: 0x403000E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4206592
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 63

2.1.162 PERI_GR3_PPU_SL4_ADDR0

PPU region address 0 (slave structure)

Address: 0x40300100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": address of protected region. Note: this field is read-only. Its value is chip specific. Default Value: 4207616
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Note: this field is read-only. Its value is chip specific. Default Value: 0

2.1.163 PERI_GR3_PPU_SL4_ADDR1

PPU region address 1 (master structure)

Address: 0x40300120

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4206593
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 252

2.1.164 PERI_GR3_PPU_SL5_ADDR0

PPU region address 0 (slave structure)

Address: 0x40300140

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": address of protected region. Note: this field is read-only. Its value is chip specific. Default Value: 4207872
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Note: this field is read-only. Its value is chip specific. Default Value: 0

2.1.165 PERI_GR3_PPU_SL5_ADDR1

PPU region address 1 (master structure)

Address: 0x40300160

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4206593
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 243

2.1.166 PERI_GR3_PPU_SL6_ADDR0

PPU region address 0 (slave structure)

Address: 0x40300180

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": address of protected region. Note: this field is read-only. Its value is chip specific. Default Value: 4208128
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Note: this field is read-only. Its value is chip specific. Default Value: 0

2.1.167 PERI_GR3_PPU_SL6_ADDR1

PPU region address 1 (master structure)

Address: 0x403001A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4206593
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 207

2.1.168 PERI_GR3_PPU_SL8_ADDR0

PPU region address 0 (slave structure)

Address: 0x40300200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": address of protected region. Note: this field is read-only. Its value is chip specific. Default Value: 4208640
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Note: this field is read-only. Its value is chip specific. Default Value: 0

2.1.169 PERI_GR3_PPU_SL8_ADDR1

PPU region address 1 (master structure)

Address: 0x40300220

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4206594
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 252

2.1.170 PERI_GR3_PPU_SL9_ADDR1

PPU region address 1 (master structure)

Address: 0x40300260

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4206594
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 243

2.1.171 PERI_GR3_PPU_SL10_ADDR0

PPU region address 0 (slave structure)

Address: 0x40300280

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": address of protected region. Note: this field is read-only. Its value is chip specific. Default Value: 4209408
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Note: this field is read-only. Its value is chip specific. Default Value: 0

2.1.172 PERI_GR3_PPU_SL10_ADDR1

PPU region address 1 (master structure)

Address: 0x403002A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4206594
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 207

2.1.173 PERI_GR3_PPU_SL11_ADDR0

PPU region address 0 (slave structure)

Address: 0x403002C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": address of protected region. Note: this field is read-only. Its value is chip specific. Default Value: 4209664
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Note: this field is read-only. Its value is chip specific. Default Value: 0

2.1.174 PERI_GR3_PPU_SL11_ATT0

PPU region attributes 0 (slave structure)

Address: 0x403002C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	R	RW	RW	R	RW	RW
HW Access	None	R	R	R	R	R	R	R
Name	None	NS	PX	PW	PR	UX	UW	UR

Bits	15	14	13	12	11	10	9	8
SW Access	RW							R
HW Access	R							R
Name	PC_MASK_15_TO_1 [15:9]							PC_MASK_0

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None	R				
HW Access	R	R	None	R				
Name	ENABLED	PC_MATCH	None	REGION_SIZE [28:24]				

Bits	Name	Description
31	ENABLED	See corresponding field for PPU structure with programmable address. Default Value: 0
30	PC_MATCH	See corresponding field for PPU structure with programmable address. Default Value: Undefined
28 : 24	REGION_SIZE	See corresponding field for PPU structure with programmable address. Note: this field is read-only. Its value is chip specific. Default Value: 16
15 : 9	PC_MASK_15_TO_1	See corresponding field for PPU structure with programmable address. Default Value: Undefined
8	PC_MASK_0	See corresponding field for PPU structure with programmable address. Default Value: 1
6	NS	See corresponding field for PPU structure with programmable address. Default Value: Undefined

2.1.174 PERI_GR3_PPU_SL11_ATT0 (continued)

5	PX	See corresponding field for PPU structure with programmable address. Note that this register is constant '1'; i.e. user execute accesses are ALWAYS allowed. Default Value: 1
4	PW	See corresponding field for PPU structure with programmable address. Default Value: Undefined
3	PR	See corresponding field for PPU structure with programmable address. Default Value: Undefined
2	UX	See corresponding field for PPU structure with programmable address. Note that this register is constant '1'; i.e. user execute accesses are ALWAYS allowed. Default Value: 1
1	UW	See corresponding field for PPU structure with programmable address. Default Value: Undefined
0	UR	See corresponding field for PPU structure with programmable address. Default Value: Undefined

2.1.175 PERI_GR3_PPU_SL11_ADDR1

PPU region address 1 (master structure)

Address: 0x403002E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4206594
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 63

2.1.176 PERI_GR3_PPU_SL12_ADDR0

PPU region address 0 (slave structure)

Address: 0x40300300

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": address of protected region. Note: this field is read-only. Its value is chip specific. Default Value: 4210432
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Note: this field is read-only. Its value is chip specific. Default Value: 0

2.1.177 PERI_GR3_PPU_SL12_ADDR1

PPU region address 1 (master structure)

Address: 0x40300320

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4206595
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 252

2.1.178 PERI_GR4_PPU_SL0_ADDR0

PPU region address 0 (slave structure)

Address: 0x40400000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": address of protected region. Note: this field is read-only. Its value is chip specific. Default Value: 4210688
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Note: this field is read-only. Its value is chip specific. Default Value: 0

2.1.179 PERI_GR4_PPU_SL0_ADDR1

PPU region address 1 (master structure)

Address: 0x40400020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4210688
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 252

2.1.180 PERI_GR4_PPU_SL2_ADDR0

PPU region address 0 (slave structure)

Address: 0x40400080

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": address of protected region. Note: this field is read-only. Its value is chip specific. Default Value: 4211200
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Note: this field is read-only. Its value is chip specific. Default Value: 0

2.1.181 PERI_GR4_PPU_SL2_ADDR1

PPU region address 1 (master structure)

Address: 0x404000A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4210688
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 207

2.1.182 PERI_GR6_PPU_SL0_ADDR0

PPU region address 0 (slave structure)

Address: 0x40600000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": address of protected region. Note: this field is read-only. Its value is chip specific. Default Value: 4218880
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Note: this field is read-only. Its value is chip specific. Default Value: 0

2.1.183 PERI_GR6_PPU_SL0_ADDR1

PPU region address 1 (master structure)

Address: 0x40600020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4218880
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 252

2.1.184 PERI_GR6_PPU_SL1_ADDR0

PPU region address 0 (slave structure)

Address: 0x40600040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": address of protected region. Note: this field is read-only. Its value is chip specific. Default Value: 4219136
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Note: this field is read-only. Its value is chip specific. Default Value: 0

2.1.185 PERI_GR6_PPU_SL1_ADDR1

PPU region address 1 (master structure)

Address: 0x40600060

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4218880
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 243

2.1.186 PERI_GR6_PPU_SL2_ADDR1

PPU region address 1 (master structure)

Address: 0x406000A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4218880
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 207

2.1.187 PERI_GR6_PPU_SL3_ADDR1

PPU region address 1 (master structure)

Address: 0x406000E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4218880
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 63

2.1.188 PERI_GR6_PPU_SL4_ADDR1

PPU region address 1 (master structure)

Address: 0x40600120

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4218881
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 252

2.1.189 PERI_GR6_PPU_SL5_ADDR1

PPU region address 1 (master structure)

Address: 0x40600160

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4218881
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 243

2.1.190 PERI_GR6_PPU_SL6_ADDR1

PPU region address 1 (master structure)

Address: 0x406001A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4218881
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 207

2.1.191 PERI_GR6_PPU_SL7_ADDR1

PPU region address 1 (master structure)

Address: 0x406001E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4218881
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 63

2.1.192 PERI_GR6_PPU_SL8_ADDR1

PPU region address 1 (master structure)

Address: 0x40600220

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4218882
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 252

2.1.193 PERI_GR6_PPU_SL9_ADDR1

PPU region address 1 (master structure)

Address: 0x40600260

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4218882
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 243

2.1.194 PERI_GR9_PPU_SL0_ADDR0

PPU region address 0 (slave structure)

Address: 0x41000000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": address of protected region. Note: this field is read-only. Its value is chip specific. Default Value: 4259840
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Note: this field is read-only. Its value is chip specific. Default Value: 0

2.1.195 PERI_GR9_PPU_SL0_ADDR1

PPU region address 1 (master structure)

Address: 0x41000020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4259840
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 252

2.1.196 PERI_GR9_PPU_SL1_ADDR0

PPU region address 0 (slave structure)

Address: 0x41000040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": address of protected region. Note: this field is read-only. Its value is chip specific. Default Value: 4263936
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Note: this field is read-only. Its value is chip specific. Default Value: 0

2.1.197 PERI_GR9_PPU_SL1_ATT0

PPU region attributes 0 (slave structure)

Address: 0x41000044

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	R	RW	RW	R	RW	RW
HW Access	None	R	R	R	R	R	R	R
Name	None	NS	PX	PW	PR	UX	UW	UR

Bits	15	14	13	12	11	10	9	8
SW Access	RW							R
HW Access	R							R
Name	PC_MASK_15_TO_1 [15:9]							PC_MASK_0

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None	R				
HW Access	R	R	None	R				
Name	ENABLED	PC_MATCH	None	REGION_SIZE [28:24]				

Bits	Name	Description
31	ENABLED	See corresponding field for PPU structure with programmable address. Default Value: 0
30	PC_MATCH	See corresponding field for PPU structure with programmable address. Default Value: Undefined
28 : 24	REGION_SIZE	See corresponding field for PPU structure with programmable address. Note: this field is read-only. Its value is chip specific. Default Value: 19
15 : 9	PC_MASK_15_TO_1	See corresponding field for PPU structure with programmable address. Default Value: Undefined
8	PC_MASK_0	See corresponding field for PPU structure with programmable address. Default Value: 1
6	NS	See corresponding field for PPU structure with programmable address. Default Value: Undefined

2.1.197 PERI_GR9_PPU_SL1_ATT0 (continued)

5	PX	See corresponding field for PPU structure with programmable address. Note that this register is constant '1'; i.e. user execute accesses are ALWAYS allowed. Default Value: 1
4	PW	See corresponding field for PPU structure with programmable address. Default Value: Undefined
3	PR	See corresponding field for PPU structure with programmable address. Default Value: Undefined
2	UX	See corresponding field for PPU structure with programmable address. Note that this register is constant '1'; i.e. user execute accesses are ALWAYS allowed. Default Value: 1
1	UW	See corresponding field for PPU structure with programmable address. Default Value: Undefined
0	UR	See corresponding field for PPU structure with programmable address. Default Value: Undefined

2.1.198 PERI_GR9_PPU_SL1_ADDR1

PPU region address 1 (master structure)

Address: 0x41000060

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4259840
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 243

2.1.199 PERI_GR10_PPU_SL0_ADDR0

PPU region address 0 (slave structure)

Address: 0x42A00000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": address of protected region. Note: this field is read-only. Its value is chip specific. Default Value: 4366336
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Note: this field is read-only. Its value is chip specific. Default Value: 0

2.1.200 PERI_GR10_PPU_SL0_ADDR1

PPU region address 1 (master structure)

Address: 0x42A00020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4366336
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 252

2.1.201 PERI_GR10_PPU_SL1_ADDR0

PPU region address 0 (slave structure)

Address: 0x42A00040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": address of protected region. Note: this field is read-only. Its value is chip specific. Default Value: 4366592
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Note: this field is read-only. Its value is chip specific. Default Value: 0

2.1.202 PERI_GR10_PPU_SL1_ADDR1

PPU region address 1 (master structure)

Address: 0x42A00060

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4366336
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 243

2.1.203 PERI_GR10_PPU_SL2_ADDR0

PPU region address 0 (slave structure)

Address: 0x42A00080

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": address of protected region. Note: this field is read-only. Its value is chip specific. Default Value: 4366848
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Note: this field is read-only. Its value is chip specific. Default Value: 0

2.1.204 PERI_GR10_PPU_SL2_ADDR1

PPU region address 1 (master structure)

Address: 0x42A000A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	See corresponding field for PPU structure with programmable address. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4366336
7 : 0	SUBREGION_DISABLE	See corresponding field for PPU structure with programmable address. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 207

Section C: Peripheral Group 1

This section encompasses the following chapters:

3 Cryptography Registers

This section discusses the Cryptography Registers (CRYPTO) registers. It lists all the registers in mapping tables, in address order.

3.1 Register Details

Register	Address	Description
CRYPTO_CTL	0x40110000	Control
CRYPTO_STATUS	0x40110004	Status
CRYPTO_RAM_PWRUP_DELAY	0x40110008	Power up delay used for SRAM power domain
CRYPTO_ERROR_STATUS0	0x40110020	Error status 0
CRYPTO_ERROR_STATUS1	0x40110024	Error status 1
CRYPTO_INSTR_FF_CTL	0x40110040	Instruction FIFO control
CRYPTO_INSTR_FF_STATUS	0x40110044	Instruction FIFO status
CRYPTO_INSTR_FF_WR	0x40110048	Instruction FIFO write
CRYPTO_RF_DATA0	0x40110080	Register-file
CRYPTO_RF_DATA1	0x40110084	Register-file. See CRYPTO_RF_DATA0 for the details of bit fields.
CRYPTO_RF_DATA2	0x40110088	Register-file. See CRYPTO_RF_DATA0 for the details of bit fields.
CRYPTO_RF_DATA3	0x4011008C	Register-file. See CRYPTO_RF_DATA0 for the details of bit fields.
CRYPTO_RF_DATA4	0x40110090	Register-file. See CRYPTO_RF_DATA0 for the details of bit fields.
CRYPTO_RF_DATA5	0x40110094	Register-file. See CRYPTO_RF_DATA0 for the details of bit fields.
CRYPTO_RF_DATA6	0x40110098	Register-file. See CRYPTO_RF_DATA0 for the details of bit fields.
CRYPTO_RF_DATA7	0x4011009C	Register-file. See CRYPTO_RF_DATA0 for the details of bit fields.
CRYPTO_RF_DATA8	0x401100A0	Register-file. See CRYPTO_RF_DATA0 for the details of bit fields.
CRYPTO_RF_DATA9	0x401100A4	Register-file. See CRYPTO_RF_DATA0 for the details of bit fields.
CRYPTO_RF_DATA10	0x401100A8	Register-file. See CRYPTO_RF_DATA0 for the details of bit fields.
CRYPTO_RF_DATA11	0x401100AC	Register-file. See CRYPTO_RF_DATA0 for the details of bit fields.
CRYPTO_RF_DATA12	0x401100B0	Register-file. See CRYPTO_RF_DATA0 for the details of bit fields.
CRYPTO_RF_DATA13	0x401100B4	Register-file. See CRYPTO_RF_DATA0 for the details of bit fields.
CRYPTO_RF_DATA14	0x401100B8	Register-file. See CRYPTO_RF_DATA0 for the details of bit fields.
CRYPTO_RF_DATA15	0x401100BC	Register-file. See CRYPTO_RF_DATA0 for the details of bit fields.
CRYPTO_AES_CTL	0x40110100	AES control
CRYPTO_STR_RESULT	0x40110180	String result

Register	Address	Description
CRYPTO_PR_LFSR_CTL0	0x40110200	Pseudo random LFSR control 0
CRYPTO_PR_LFSR_CTL1	0x40110204	Pseudo random LFSR control 1
CRYPTO_PR_LFSR_CTL2	0x40110208	Pseudo random LFSR control 2
CRYPTO_PR_RESULT	0x40110210	Pseudo random result
CRYPTO_TR_CTL0	0x40110280	True random control 0
CRYPTO_TR_CTL1	0x40110284	True random control 1
CRYPTO_TR_RESULT	0x40110288	True random result
CRYPTO_TR_GARO_CTL	0x401102A0	True random GARO control
CRYPTO_TR_FIRO_CTL	0x401102A4	True random FIRO control
CRYPTO_TR_MON_CTL	0x401102C0	True random monitor control
CRYPTO_TR_MON_CMD	0x401102C8	True random monitor command
CRYPTO_TR_MON_RC_CTL	0x401102D0	True random monitor RC control
CRYPTO_TR_MON_RC_STATUS0	0x401102D8	True random monitor RC status 0
CRYPTO_TR_MON_RC_STATUS1	0x401102DC	True random monitor RC status 1
CRYPTO_TR_MON_AP_CTL	0x401102E0	True random monitor AP control
CRYPTO_TR_MON_AP_STATUS0	0x401102E8	True random monitor AP status 0
CRYPTO_TR_MON_AP_STATUS1	0x401102EC	True random monitor AP status 1
CRYPTO_SHA_CTL	0x40110300	SHA control
CRYPTO_CRC_CTL	0x40110400	CRC control
CRYPTO_CRC_DATA_CTL	0x40110410	CRC data control
CRYPTO_CRC_POL_CTL	0x40110420	CRC polynomial control
CRYPTO_CRC_LFSR_CTL	0x40110430	CRC LFSR control
CRYPTO_CRC_REM_CTL	0x40110440	CRC remainder control
CRYPTO_CRC_REM_RESULT	0x40110448	CRC remainder result
CRYPTO_VU_CTL0	0x40110480	Vector unit control 0
CRYPTO_VU_CTL1	0x40110484	Vector unit control 1
CRYPTO_VU_STATUS	0x40110490	Vector unit status
CRYPTO_INTR	0x401107C0	Interrupt register
CRYPTO_INTR_SET	0x401107C4	Interrupt set register
CRYPTO_INTR_MASK	0x401107C8	Interrupt mask register
CRYPTO_INTR_MASKED	0x401107CC	Interrupt masked register
CRYPTO_MEM_BUFF0	0x40114000	Memory buffer. This is the starting address of a register bank containing 1024 registers (CRYPTO_MEM_BUFF0 to CRYPTO_MEM_BUFF1023)

3.1.1 CRYPTO_CTL

Control

Address: 0x40110000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	
HW Access	None						R	
Name	None [7:2]						PWR_MODE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	ENABLED	None [30:24]						

Bits	Name	Description
31	ENABLED	IP enable: '0': Disabled. All non-retention registers (command and status registers) are reset to their default value when the IP is disabled. All retention registers retain their value when the IP is disabled. '1': Enabled. Default Value: 0 **0x0: DISABLED** **0x1: ENABLED**
1 : 0	PWR_MODE	Set power mode for memory buffer SRAM. Default Value: 3 **0x0: OFF :** See CM4_PWR_CTL **0x1: RESERVED :** undefined **0x2: RETAINED :** See CM4_PWR_CTL **0x3: ENABLED :** See CM4_PWR_CTL

3.1.2 CRYPTO_STATUS

Status

Address: 0x40110004

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	VU_BUSY	TR_BUSY	PR_BUSY	STR_BUSY	CRC_BUSY	SHA_BUSY	DES_BUSY	AES_BUSY

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	CM-D_FF_BUSY	None [30:24]						

Bits	Name	Description
31	CMD_FF_BUSY	Reflects the state of the command FIFO (copy of CMD_FF_STATUS.BUSY): '0': No instruction pending. '1': Instruction pending. Default Value: 0
7	VU_BUSY	Reflects the state of the vector unit component. Default Value: 0
6	TR_BUSY	Reflects the state of the TR component. Default Value: 0
5	PR_BUSY	Reflects the state of the PR component. Default Value: 0
4	STR_BUSY	Reflects the state of the CRC component. Default Value: 0
3	CRC_BUSY	Reflects the state of the CRC component. Default Value: 0

3.1.2 CRYPTO_STATUS (continued)

2	SHA_BUSY	Reflects the state of the SHA component. Default Value: 0
1	DES_BUSY	Reflects the state of the DES component. Default Value: 0
0	AES_BUSY	Reflects the state of the AES component: '0': Component is not busy. '1': Component is busy performing an instruction. When the component is busy, it is NOT possible to start another operation. However, it is possible to access the instruction FIFO or memory buffer (to prepare for another operation). Default Value: 0

3.1.3 CRYPTO_RAM_PWRUP_DELAY

Power up delay used for SRAM power domain

Address: 0x40110008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	PWRUP_DELAY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						PWRUP_DELAY [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 0	PWRUP_DELAY	Number clock cycles delay needed after power domain power up Default Value: 150

3.1.4 CRYPTO_ERROR_STATUS0

Error status 0

Address: 0x40110020

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Captures error description information. For INSTR_OPC_ERROR: - Violating instruction. For INSTR_CC_ERROR: - Violating instruction. For BUS_ERROR: - Violating transfer address. Default Value: Undefined

3.1.5 CRYPTO_ERROR_STATUS1

Error status 1

Address: 0x40110024

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA23 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA23 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	DATA23 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None				RW		
HW Access	RW1S	None				RW		
Name	VALID	None [30:27]				IDX [26:24]		

Bits	Name	Description
31	VALID	Specifies if ERROR_STATUS0 and ERROR_STATUS1 capture valid error information. Default Value: 0
26 : 24	IDX	Error source: "0": INSTR_OPC_ERROR, instruction decoder error. "1": INSTR_CC_ERROR, instruction condition code error. "2": BUS_ERROR, Bus master interface AHB-Lite bus error. "3": TR_AP_DETECT_ERROR. "4": TR_RC_DETECT_ERROR. "5"-"7": Undefined. Default Value: 0
23 : 0	DATA23	Captures error description information. For BUS_ERROR: - Violating transfer, read attribute (DATA23[0]). - Violating transfer, size attribute (DATA23[5:4]). "0": 8-bit transfer, "1": 16 bits transfer, "2": 32-bit transfer. For INSTR_CC_ERROR: Default Value: Undefined

3.1.6 CRYPTO_INSTR_FF_CTL

Instruction FIFO control

Address: 0x40110040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW		
HW Access	None					R		
Name	None [7:3]					EVENT_LEVEL [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	RW
HW Access	None						R	RW1S
Name	None [23:18]						BLOCK	CLEAR

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
17	BLOCK	This field specifies the behavior when an instruction is written to a full FIFO (INSTR_FIFO_WR MMIO register): '0': The write is ignored/dropped and the INTR.INSTR_FF_OVERFLOW interrupt cause is set to '1'. '1': The write is blocked, resulting in AHB-Lite wait states and the INTR.INSTR_FF_OVERFLOW interrupt cause is set to '1' (this cause may be masked out). The instruction is written to the FIFO as soon as a FIFO entry becomes available. The maximum time is roughly the time of the execution of the slowest/longest instruction. Note that this setting may "lock up" the CPU. When the CPU is "locked up" it can not respond to interrupts. As a result, the interrupt latency is increased. Default Value: 1
16	CLEAR	When '1', the instruction FIFO is cleared/invalidated. Invalidation will last for as long as this field is '1'. If a quick clear/invalidation is required, the field should be set to '1' and be followed by a set to '0'. If a clear/invalidation is required for an extended time period, the field should be set to '1' during the complete time period. HW sets this field to '1' on when an error INTR cause is activated. Default Value: 0

3.1.6 CRYPTO_INSTR_FF_CTL (continued)

2 : 0	EVENT_LEVEL	Event level. When the number of entries in the instruction FIFO is less than the amount of this field, an event is generated: - "event" = INSTR_FF_STATUS.USED < EVENT_LEVEL. Default Value: 0

3.1.7 CRYPTO_INSTR_FF_STATUS

Instruction FIFO status

Address: 0x40110044

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R			
HW Access	None				W			
Name	None [7:4]				USED [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							R
HW Access	None							W
Name	None [23:17]							EVENT

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	BUSY	None [30:24]						

Bits	Name	Description
31	BUSY	Reflects the state of the instruction FIFO: '0': No instruction pending (USED is "0"). '1': Instruction pending. Default Value: 0
16	EVENT	Instruction FIFO event. Default Value: 0
3 : 0	USED	Number of instructions in the instruction FIFO. The value of this field ranges from 0 to 8. Default Value: 0

3.1.8 CRYPTO_INSTR_FF_WR

Instruction FIFO write

Address: 0x40110048

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	W							
HW Access	R							
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	W							
HW Access	R							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Instruction or instruction operand data that is written to the instruction FIFO. Default Value: 0

3.1.9 CRYPTO_RF_DATA0

Register-file

Address: 0x40110080

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Register-file data. For the vector unit component, a register-file register has the following layout: DATA[29:16]: data DATA[11:0]: bit size (minus 1) Default Value: 0

3.1.10 CRYPTO_AES_CTL

AES control

Address: 0x40110100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	
HW Access	None						R	
Name	None [7:2]						KEY_SIZE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1 : 0	KEY_SIZE	AES key size: "0": 128-bit key, 10 rounds AES (inverse) cipher operation. SRC_CTL0 specifies the location of a 16 Byte key. "1": 192-bit key, 12 rounds AES (inverse) cipher operation. SRC_CTL0 specifies the location of a 24 Byte key. "2": 256-bit key, 14 rounds AES (inverse) cipher operation. SRC_CTL0 specifies the location of a 32 Byte key. "3": Undefined Default Value: 0 **0x0: AES128 :** **0x1: AES192 :** **0x2: AES256 :**

3.1.11 CRYPTO_STR_RESULT

String result

Address: 0x40110180

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							W
Name	None [7:1]							MEMCMP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	MEMCMP	Result of a STR_MEMCMP operation: '0': source 0 equals source 1. '1': source 0 does NOT equal source 1. Default Value: Undefined

3.1.12 CRYPTO_PR_LFSR_CTL0

Pseudo random LFSR control 0

Address: 0x40110200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	LFSR32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	LFSR32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	LFSR32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	LFSR32 [31:24]							

Bits	Name	Description
31 : 0	LFSR32	State of a 32-bit Linear Feedback Shift Registers (LFSR) that is used to generate a pseudo random bit sequence. This register needs to be initialized by SW. The initialization value should be different from "0". The three PR_LFSR_CTL registers represents the state of a 32-bit, 31-bit and 29-bit LFSR. Individually, these LFSRs generate a pseudo random bit sequence that repeats itself after (2^32)-1, (2^31)-1 and (2^29)-1 bits. The numbers (2^32)-1, (2^31)-1 and (2^29)-1 are relatively prime (their greatest common denominator is "1"). The three bit sequence are combined (XOR'd) into a single bitstream to create a pseudo random bit sequence that repeats itself after ((2^32)-1) * ((2^31)-1) * ((2*29)-1) bits. The following polynomials are used: - 32-bit irreducible polynomial: x^32+x^30+x^26+x^25+1. - 31-bit irreducible polynomial: x^31+x^28+1. - 29-bit irreducible polynomial: x^29+x^27+1. Default Value: 3633683401

3.1.13 CRYPTO_PR_LFSR_CTL1

Pseudo random LFSR control 1

Address: 0x40110204

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	LFSR31 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	LFSR31 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	LFSR31 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None	RW						
HW Access	None	RW						
Name	None	LFSR31 [30:24]						

Bits	Name	Description
30 : 0	LFSR31	State of a 31-bit Linear Feedback Shift Registers (LFSR) that is used to generate a pseudo random bit sequence. See PR_LFSR_CTL0. Default Value: 733549048

3.1.14 CRYPTO_PR_LFSR_CTL2

Pseudo random LFSR control 2

Address: 0x40110208

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	LFSR29 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	LFSR29 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	LFSR29 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None			RW				
HW Access	None			RW				
Name	None [31:29]			LFSR29 [28:24]				

Bits	Name	Description
28 : 0	LFSR29	State of a 29-bit Linear Feedback Shift Registers (LFSR) that is used to generate a pseudo random bit sequence. See PR_LFSR_CTL0. Default Value: 101462455

3.1.15 CRYPTO_PR_RESULT

Pseudo random result

Address: 0x40110210

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	A							
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	A							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Result of a pseudo random number generation operation. The resulting value DATA is in the range [0, MAX], with MAX specified by rsrc0. HW generates the number in this field. Note that SW can write this field. This functionality can be used prevent information leakage. Default Value: 0

3.1.16 CRYPTO_TR_CTL0

True random control 0

Address: 0x40110280

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SAMPLE_CLOCK_DIV [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	RED_CLOCK_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INIT_DELAY [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None		RW	RW	None			RW
HW Access	None		R	R	None			R
Name	None [31:30]		STOP_ON_RC_DETECT	STOP_ON_AP_DETECT	None [27:25]			VON_NEUMANN_CORR

Bits	Name	Description
29	STOP_ON_RC_DETECT	Specifies if TRNG functionality is stopped on a repetition count test detection (when HW sets INTR.TR_RC_DETECT to '1'): '0': Functionality is NOT stopped. '1': Functionality is stopped (TR_CTL1 fields are set to '0' by HW). Default Value: 0
28	STOP_ON_AP_DETECT	Specifies if TRNG functionality is stopped on an adaptive proportion test detection (when HW sets INTR.TR_AP_DETECT to '1'): '0': Functionality is NOT stopped. '1': Functionality is stopped (TR_CTL1 fields are set to '0' by HW). Default Value: 0

3.1.16 CRYPTO_TR_CTL0 (continued)

24	VON_NEUMANN_CORR	Specifies if the "von Neumann corrector" is disabled or enabled: '0': disabled. '1': enabled. The "von Neumann corrector" post-processes the reduced bits to remove a '0' or '1' bias. The corrector operates on reduced bit pairs ("oldest bit, newest bit"): "00": no bit is produced. "01": '0' bit is produced (oldest bit). "10": '1' bit is produced (oldest bit). "11": no bit is produced. Note that the corrector produces bits at a random pace and at a frequency that is 1/4 of the reduced bit frequency (reduced bits are processed in pairs, and half of the pairs do NOT produce a bit). Default Value: 0
23 : 16	INIT_DELAY	Specifies an initialization delay: number of removed/dropped samples before reduced bits are generated. This field should be programmed in the range [1, 255]. After starting the oscillators, at least the first 2 samples should be removed/dropped to clear the state of internal synchronizers. In addition, it is advised to drop at least the second 2 samples from the oscillators (to circumvent the semi-predictable oscillator startup behavior). This result in the default field value of "3". Field encoding is as follows: "0": 1 sample is dropped. "1": 2 samples are dropped. ... "255": 256 samples are dropped. The TR_INITIALIZED interrupt cause is set to '1', when the initialization delay is passed. Default Value: 3
15 : 8	RED_CLOCK_DIV	Specifies the clock divider that is used to produce reduced bits. "0": 1 reduced bit is produced for each sample. "1": 1 reduced bit is produced for each 2 samples. ... "255": 1 reduced bit is produced for each 256 samples. The reduced bits are considered random bits and shifted into TR_RESULT0.DATA32. Default Value: 0
7 : 0	SAMPLE_CLOCK_DIV	Specifies the clock divider that is used to sample oscillator data. This clock divider is wrt. "clk_sys". "0": sample clock is "clk_sys". "1": sample clock is "clk_sys"/2. ... "255": sample clock is "clk_sys"/256. Default Value: 0

3.1.17 CRYPTO_TR_CTL1

True random control 1

Address: 0x40110284

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
Name	None [7:6]		FIRO31_EN	FIRO15_EN	GA-RO31_EN	GA-RO15_EN	RO15_EN	RO11_EN

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	FIRO31_EN	FW sets this field to '1' to enable the programmable Fibonacci ring oscillator with up to 31 inverters. The TR_FIRO_CTL register specifies the programmable polynomial. Default Value: 0
4	FIRO15_EN	FW sets this field to '1' to enable the fixed Fibonacci ring oscillator with 15 inverters. Default Value: 0
3	GARO31_EN	FW sets this field to '1' to enable the programmable Galois ring oscillator with up to 31 inverters. The TR_GARO_CTL register specifies the programmable polynomial. Default Value: 0
2	GARO15_EN	FW sets this field to '1' to enable the fixed Galois ring oscillator with 15 inverters. Default Value: 0
1	RO15_EN	FW sets this field to '1' to enable the ring oscillator with 15 inverters. Default Value: 0
0	RO11_EN	FW sets this field to '1' to enable the ring oscillator with 11 inverters. Default Value: 0

3.1.18 CRYPTO_TR_RESULT

True random result

Address: 0x40110288

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	A							
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	A							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Generated true random number. HW generates the number in the least significant bit positions of this field. The TR_DATA_AVAILABLE interrupt cause is activated when the number is generated. Note that SW can write this field. This functionality can be used prevent information leakage. Default Value: 0

3.1.19 CRYPTO_TR_GARO_CTL

True random GARO control

Address: 0x401102A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	POLYNOMIAL31 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	POLYNOMIAL31 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	POLYNOMIAL31 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None	RW						
HW Access	None	R						
Name	None	POLYNOMIAL31 [30:24]						

Bits	Name	Description
30 : 0	POLYNOMIAL31	Polynomial for programmable Galois ring oscillator. The polynomial is represented WITHOUT the high order bit (this bit is always assumed '1'). The polynomial should be aligned such that the more significant bits (bit 30 and down) contain the polynomial and the less significant bits (bit 0 and up) contain padding '0's. Default Value: 0

3.1.20 CRYPTO_TR_FIRO_CTL

True random FIRO control

Address: 0x401102A4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	POLYNOMIAL31 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	POLYNOMIAL31 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	POLYNOMIAL31 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None	RW						
HW Access	None	R						
Name	None	POLYNOMIAL31 [30:24]						

Bits	Name	Description
30 : 0	POLYNOMIAL31	Polynomial for programmable Fibonacci ring oscillator. The polynomial is represented WITHOUT the high order bit (this bit is always assumed '1'). The polynomial should be aligned such that the more significant bits (bit 30 and down) contain the polynomial and the less significant bits (bit 0 and up) contain padding '0's. Default Value: 0

3.1.21 CRYPTO_TR_MON_CTL

True random monitor control

Address: 0x401102C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	
HW Access	None						R	
Name	None [7:2]						BITSTREAM_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1 : 0	BITSTREAM_SEL	Selection of the bitstream: "0": DAS bitstream. "1": RED bitstream. "2": TR bitstream. "3": Undefined. Default Value: 2

3.1.22 CRYPTO_TR_MON_CMD

True random monitor command

Address: 0x401102C8

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						RW1C	RW1C
Name	None [7:2]						START_RC	START_AP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	START_RC	Repetition count (RC) test enable: '0': Disabled. '1': Enabled. On a RC detection, HW sets this field to '0' and sets INTR.TR_RC_DETECT to '1. Default Value: 0
0	START_AP	Adaptive proportion (AP) test enable: '0': Stopped. '1': Started. On a AP detection, HW sets this field to '0' and sets INTR.TR_AP_DETECT to '1. Default Value: 0

3.1.23 CRYPTO_TR_MON_RC_CTL

True random monitor RC control

Address: 0x401102D0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CUTOFF_COUNT8 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	CUTOFF_COUNT8	Cutoff count (legal range is [1, 255]): "0": Illegal. "1": 1 repetition. ... "255": 255 repetitions. Default Value: 255

3.1.24 CRYPTO_TR_MON_RC_STATUS0

True random monitor RC status 0

Address: 0x401102D8

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							BIT

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	BIT	Current active bit value: '0': '0'. '1': '1'. This field is only valid when TR_MON_RC_STATUS1.REP_COUNT is NOT equal to "0". Default Value: 0

3.1.25 CRYPTO_TR_MON_RC_STATUS1

True random monitor RC status 1

Address: 0x401102DC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	REP_COUNT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	REP_COUNT	Number of repetitions of the current active bit counter: "0": 0 repetitions. ... "255": 255 repetitions. Default Value: 0

3.1.26 CRYPTO_TR_MON_AP_CTL

True random monitor AP control

Address: 0x401102E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CUTOFF_COUNT16 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CUTOFF_COUNT16 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	WINDOW_SIZE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	WINDOW_SIZE [31:24]							

Bits	Name	Description
31 : 16	WINDOW_SIZE	Window size (minus 1) : "0": 1 bit. ... "65535": 65536 bits. Default Value: 65535
15 : 0	CUTOFF_COUNT16	Cutoff count (legal range is [1, 65535]). "0": Illegal. "1": 1 occurrence. ... "65535": 65535 occurrences. Default Value: 65535

3.1.27 CRYPTO_TR_MON_AP_STATUS0

True random monitor AP status 0

Address: 0x401102E8

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							BIT

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	BIT	Current active bit value: '0': '0'. '1': '1'. This field is only valid when TR_MON_AP_STATUS1.OCC_COUNT is NOT equal to "0". Default Value: 0

3.1.28 CRYPTO_TR_MON_AP_STATUS1

True random monitor AP status 1

Address: 0x401102EC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	OCC_COUNT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	OCC_COUNT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	WINDOW_INDEX [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	WINDOW_INDEX [31:24]							

Bits	Name	Description
31 : 16	WINDOW_INDEX	Counter to keep track of the current index in the window (counts from "0" to TR_MON_AP_CTL.WINDOW_SIZE). Default Value: 0
15 : 0	OCC_COUNT	Number of occurrences of the current active bit counter: "0": 0 occurrences ... "65535": 65535 occurrences Default Value: 0

3.1.29 CRYPTO_SHA_CTL

SHA control

Address: 0x40110300

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW		
HW Access	None					R		
Name	None [7:3]					MODE [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2 : 0	MODE	SHA mode: "0": SHA1. The message is 16 32 bits words: 64 Bytes. The hash is 5 32-bit words: 20 Bytes. There are 80 32-bit message schedule round constants: 320 Bytes. "1": SHA224, SHA256. The message is 16 32-bit words: 64 Bytes. The hash is 8 32-bit words: 32 Bytes. There are 64 32-bit message schedule round constants: 256 Bytes. The difference between SHA224 and SHA256 is entirely in software (differences in initialization hash and message digest size). "2": SHA512/224, SHA512/256, SHA384, SHA512. The message is 8 64-bit words: 64 Bytes. The hash is 8 64-bit words: 64 Bytes. There are 80 64-bit message schedule round constants: 640 Bytes. The difference between SHA512/224, SHA512/256, SHA384 and SHA512 is entirely in software (differences in initialization hash and message digest size). "3"-"7": Undefined. Default Value: 0 **0x0: SHA1 :** **0x1: SHA256 :** **0x2: SHA512 :**

3.1.30 CRYPTO_CRC_CTL

CRC control

Address: 0x40110400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							DATA_RE-VERSE

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							REM_RE-VERSE

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	REM_REVERSE	Specifies whether the remainder is bit reversed (reversal is performed after XORing): '0': No. '1': Yes. Default Value: 0
0	DATA_REVERSE	Specifies the bit order in which a data Byte is processed (reversal is performed after XORing): '0': Most significant bit (bit 1) first. '1': Least significant bit (bit 0) first. Default Value: 0

3.1.31 CRYPTO_CRC_DATA_CTL

CRC data control

Address: 0x40110410

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA_XOR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA_XOR	Specifies a byte mask with which each data byte is XOR'd. The XOR is performed before data reversal. Default Value: 0

3.1.32 CRYPTO_CRC_POL_CTL

CRC polynomial control

Address: 0x40110420

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	POLYNOMIAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	POLYNOMIAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	POLYNOMIAL [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	POLYNOMIAL [31:24]							

Bits	Name	Description
31 : 0	POLYNOMIAL	CRC polynomial. The polynomial is represented WITHOUT the high order bit (this bit is always assumed '1'). The polynomial should be aligned/shifted such that the more significant bits (bit 31 and down) contain the polynomial and the less significant bits (bit 0 and up) contain padding '0's. Some frequently used polynomials: - CRC32: POLYNOMIAL is 0x04c11db7 (x^32 + x^26 + x^23 + x^22 + x^16 + x^12 + x^11 + x^10 + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1). - CRC16: POLYNOMIAL is 0x80050000 (x^16 + x^15 + x^2 + 1, shifted by 16 bit positions). - CRC16 CCITT: POLYNOMIAL is 0x10210000 (x^16 + x^12 + x^5 + 1, shifted by 16 bit positions). Default Value: 0

3.1.33 CRYPTO_CRC_LFSR_CTL

CRC LFSR control

Address: 0x40110430

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	LFSR32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	LFSR32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	LFSR32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	LFSR32 [31:24]							

Bits	Name	Description
31 : 0	LFSR32	State of a 32-bit Linear Feedback Shift Registers (LFSR) that is used to implement CRC. This register needs to be initialized by SW to provide the CRC seed value. The seed value should be aligned such that the more significant bits (bit 31 and down) contain the seed value and the less significant bits (bit 0 and up) contain padding '0's. Note that SW can write this field. This functionality can be used prevent information leakage (through either CRC_LFSR_CTL or CRC_REM_RESULT) from the privileged domain to the user domain. Default Value: 0

3.1.34 CRYPTO_CRC_REM_CTL

CRC remainder control

Address: 0x40110440

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	REM_XOR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	REM_XOR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	REM_XOR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	REM_XOR [31:24]							

Bits	Name	Description
31 : 0	REM_XOR	Specifies a mask with which the CRC_LFSR_CTL.LFSR32 register is XOR'd to produce a remainder. The XOR is performed before remainder reversal. Default Value: 0

3.1.35 CRYPTO_CRC_REM_RESULT

CRC remainder result

Address: 0x40110448

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	REM [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	REM [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	REM [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	REM [31:24]							

Bits	Name	Description
31 : 0	REM	Remainder value. The alignment of the remainder depends on CRC_REM_CTL0.REM_REVERSE: '0': the more significant bits (bit 31 and down) contain the remainder. '1': the less significant bits (bit 0 and up) contain the remainder. Note: This field is combinatorially derived from CRC_LFSR_CTL.LFSR32, CRC_REM_CTL0.REM_REVERSE and CRC_REM_CTL1.REM_XOR. Default Value: 0

3.1.36 CRYPTO_VU_CTL0

Vector unit control 0

Address: 0x40110480

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							ALWAYS_EXECUTE

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	ALWAYS_EXECUTE	Specifies if a conditional instruction is executed or not, when its condition code evaluates to false/'0'. '0': The instruction is NOT executed. As a result, the instruction may be handled faster than when it is executed. '1': The instruction is executed, but the execution result (including status field information) is not reflected in the IP. The instruction is handled just as fast as when it is executed. Note: a conditional instruction with a condition code that evaluates to false/'0' does not affect the architectural state: VU_STATUS fields, memory or register-file data. Note: Always execution is useful to prevent/complicate differential timing and differential power attacks. Default Value: 0

3.1.37 CRYPTO_VU_CTL1

Vector unit control 1

Address: 0x40110484

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW		None					
HW Access	R		None					
Name	ADDR [15:14]		None [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 14	ADDR	Specifies base address of vector unit operands in memory. The register-file registers provide offsets wrt. this base address. The base address is a multiple of 16 KB. The register-file registers provide 12-bit word address offsets in this 16 KB. Together, they provide access to a 16 KB memory region for vector unit instructions: ADDR[31:14] = VU_CTL1.ADDR[31:14] ADDR[13:2] = register-file register offset The base address is either the IP's internal memory buffer (memory capacity is the internal memory buffer capacity) or a location in system memory (memory capacity is 16 KB). For best performance, the IP's memory buffer should be used and VU_CTL1.ADDR should be programmed to MEM_BUFF. If VU_CTL1.ADDR is set to MEM_BUFF and the memory buffer capacity is less than 16 KB, memory accesses beyond the memory buffer capacity access a memory hole (reads return "0" and writes are ignored). E.g., if the memory buffer is 8 KB, accesses with ADDR[13] set to '1', access a memory hole. If the IP's memory buffer capacity is not large enough to support the vector unit operands, VU_CTL1.ADDR can be set to a 16 KB aligned location in system memory. Default Value: 0

3.1.38 CRYPTO_VU_STATUS

Vector unit status

Address: 0x40110490

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R	R	R	R
HW Access	None				W	W	W	W
Name	None [7:4]				ONE	ZERO	EVEN	CARRY

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	ONE	STATUS ONE field. Default Value: 0
2	ZERO	STATUS ZERO field. Default Value: 0
1	EVEN	STATUS EVEN field. Default Value: 0
0	CARRY	STATUS CARRY field. Default Value: 0

3.1.39 CRYPTO_INTR

Interrupt register

Address: 0x401107C0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	None			RW1S	RW1S	RW1S	RW1S	RW1S
Name	None [7:5]			PR_-DATA_AVAILABLE	TR_-DATA_AVAILABLE	TR_INI-TIALIZED	IN-STR_FF_OVERFLOW	IN-STR_FF_LEVEL

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	None			RW1S	RW1S	RW1S	RW1S	RW1S
Name	None [23:21]			TR_RC_-DE-TECT_ERROR	TR_AP_DE-TECT_ER-ROR	BUS_ER-ROR	INSTR_C-C_ERROR	INSTR_OP-C_ERROR

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
20	TR_RC_DETECT_ER-ROR	This interrupt cause is activated (HW sets the field to '1') when the true random number generator monitor adaptive proportion test detects a disproportionate occurrence of a specific bit value. Default Value: 0
19	TR_AP_DETECT_ER-ROR	This interrupt cause is activated (HW sets the field to '1') when the true random number generator monitor adaptive proportion test detects a repetition of a specific bit value. Default Value: 0
18	BUS_ERROR	This interrupt cause is activated (HW sets the field to '1') when a AHB-Lite bus error is observed on the AHB-Lite master interface. Default Value: 0
17	INSTR_CC_ERROR	This interrupt cause is activated (HW sets the field to '1') when the instruction decoder encounters an instruction with a non-defined condition code. This error is only generated for VU instructions. Default Value: 0

3.1.39 CRYPTO_INTR (continued)

16	INSTR_OPC_ERROR	This interrupt cause is activated (HW sets the field to '1') when the instruction decoder encounters an instruction with a non-defined operation code (opcode). Default Value: 0
4	PR_DATA_AVAILABLE	This interrupt cause is activated (HW sets the field to '1') when the pseudo random number generator has generated a data value. Default Value: 0
3	TR_DATA_AVAILABLE	This interrupt cause is activated (HW sets the field to '1') when the true random number generator has generated a data value of the specified bit size. Default Value: 0
2	TR_INITIALIZED	This interrupt cause is activated (HW sets the field to '1') when the true random number generator is initialized. Default Value: 0
1	INSTR_FF_OVERFLOW	This interrupt cause is activated (HW sets the field to '1') when the instruction FIFO overflows (an attempt is made to write to a full FIFO). Default Value: 0
0	INSTR_FF_LEVEL	This interrupt cause is activated (HW sets the field to '1') when the instruction FIFO event is activated. Default Value: 0

3.1.40 CRYPTO_INTR_SET

Interrupt set register

Address: 0x401107C4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	None			A	A	A	A	A
Name	None [7:5]			PR_-DATA_AVAILABLE	TR_-DATA_AVAILABLE	TR_INI-TIALIZED	IN-STR_FF_OVERFLOW	IN-STR_FF_LEVEL

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	None			A	A	A	A	A
Name	None [23:21]			TR_RC_-DE-TECT_ERROR	TR_AP_DE-TECT_ER-ROR	BUS_ER-ROR	INSTR_C-C_ERROR	INSTR_OP-C_ERROR

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
20	TR_RC_DETECT_ER-ROR	SW writes a '1' to this field to set the corresponding field in interrupt request register. Default Value: 0
19	TR_AP_DETECT_ER-ROR	SW writes a '1' to this field to set the corresponding field in interrupt request register. Default Value: 0
18	BUS_ERROR	SW writes a '1' to this field to set the corresponding field in interrupt request register. Default Value: 0
17	INSTR_CC_ERROR	SW writes a '1' to this field to set the corresponding field in interrupt request register. Default Value: 0
16	INSTR_OPC_ERROR	SW writes a '1' to this field to set the corresponding field in interrupt request register. Default Value: 0
4	PR_DATA_AVAILABLE	SW writes a '1' to this field to set the corresponding field in interrupt request register. Default Value: 0

3.1.40 CRYPTO_INTR_SET (continued)

3	TR_DATA_AVAILABLE	SW writes a '1' to this field to set the corresponding field in interrupt request register. Default Value: 0
2	TR_INITIALIZED	SW writes a '1' to this field to set the corresponding field in interrupt request register. Default Value: 0
1	INSTR_FF_OVERFLOW	SW writes a '1' to this field to set the corresponding field in interrupt request register. Default Value: 0
0	INSTR_FF_LEVEL	SW writes a '1' to this field to set the corresponding field in interrupt request register. Default Value: 0

3.1.41 CRYPTO_INTR_MASK

Interrupt mask register

Address: 0x401107C8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [7:5]			PR_-DATA_AVAILABLE	TR_-DATA_AVAILABLE	TR_INI-TIALIZED	IN-STR_FF_OVERFLOW	IN-STR_FF_LEVEL

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [23:21]			TR_RC_-DE-TECT_ERROR	TR_AP_DE-TECT_ER-ROR	BUS_ER-ROR	INSTR_C-C_ERROR	INSTR_OP-C_ERROR

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
20	TR_RC_DETECT_ER-ROR	Mask bit for corresponding field in interrupt request register. Default Value: 0
19	TR_AP_DETECT_ER-ROR	Mask bit for corresponding field in interrupt request register. Default Value: 0
18	BUS_ERROR	Mask bit for corresponding field in interrupt request register. Default Value: 0
17	INSTR_CC_ERROR	Mask bit for corresponding field in interrupt request register. Default Value: 0
16	INSTR_OPC_ERROR	Mask bit for corresponding field in interrupt request register. Default Value: 0
4	PR_DATA_AVAILABLE	Mask bit for corresponding field in interrupt request register. Default Value: 0

3.1.41 CRYPTO_INTR_MASK (continued)

3	TR_DATA_AVAILABLE	Mask bit for corresponding field in interrupt request register. Default Value: 0
2	TR_INITIALIZED	Mask bit for corresponding field in interrupt request register. Default Value: 0
1	INSTR_FF_OVERFLOW	Mask bit for corresponding field in interrupt request register. Default Value: 0
0	INSTR_FF_LEVEL	Mask bit for corresponding field in interrupt request register. Default Value: 0

3.1.42 CRYPTO_INTR_MASKED

Interrupt masked register

Address: 0x401107CC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			R	R	R	R	R
HW Access	None			W	W	W	W	W
Name	None [7:5]			PR_-DATA_AVAILABLE	TR_-DATA_AVAILABLE	TR_INI-TIALIZED	IN-STR_FF_OVERFLOW	IN-STR_FF_LEVEL

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None			R	R	R	R	R
HW Access	None			W	W	W	W	W
Name	None [23:21]			TR_RC_-DE-TECT_ERROR	TR_AP_DE-TECT_ER-ROR	BUS_ER-ROR	INSTR_C-C_ERROR	INSTR_OP-C_ERROR

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
20	TR_RC_DETECT_ER-ROR	Logical and of corresponding request and mask bits. Default Value: 0
19	TR_AP_DETECT_ER-ROR	Logical and of corresponding request and mask bits. Default Value: 0
18	BUS_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
17	INSTR_CC_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
16	INSTR_OPC_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
4	PR_DATA_AVAILABLE	Logical and of corresponding request and mask bits. Default Value: 0

3.1.42 CRYPTO_INTR_MASKED (continued)

3	TR_DATA_AVAILABLE	Logical and of corresponding request and mask bits. Default Value: 0
2	TR_INITIALIZED	Logical and of corresponding request and mask bits. Default Value: 0
1	INSTR_FF_OVERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
0	INSTR_FF_LEVEL	Logical and of corresponding request and mask bits. Default Value: 0

3.1.43 CRYPTO_MEM_BUFF0

Memory buffer

Address: 0x40114000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Default Value: Undefined

Section D: Peripheral Group 2

This section encompasses the following chapters:

4 CPU Sub System (CPUSS) Registers

This section discusses the CPU Sub System (CPUSS) registers. It lists all the registers in mapping tables, in address order.

4.1 Register Details

Register	Address	Description
CPUSS_CM0_CTL	0x40210000	CM0+ control
CPUSS_CM0_STATUS	0x40210008	CM0+ status
CPUSS_CM0_CLOCK_CTL	0x40210010	CM0+ clock control
CPUSS_CM0_INT_CTL0	0x40210020	CM0+ interrupt control 0
CPUSS_CM0_INT_CTL1	0x40210024	CM0+ interrupt control 1
CPUSS_CM0_INT_CTL2	0x40210028	CM0+ interrupt control 2
CPUSS_CM0_INT_CTL3	0x4021002C	CM0+ interrupt control 3
CPUSS_CM0_INT_CTL4	0x40210030	CM0+ interrupt control 4
CPUSS_CM0_INT_CTL5	0x40210034	CM0+ interrupt control 5
CPUSS_CM0_INT_CTL6	0x40210038	CM0+ interrupt control 6
CPUSS_CM0_INT_CTL7	0x4021003C	CM0+ interrupt control 7
CPUSS_CM4_PWR_CTL	0x40210080	CM4 power control
CPUSS_CM4_PWR_DELAY_CTL	0x40210084	CM4 power control
CPUSS_CM4_STATUS	0x40210088	CM4 status
CPUSS_CM4_CLOCK_CTL	0x40210090	CM4 clock control
CPUSS_CM4_NMI_CTL	0x402100A0	CM4 NMI control
CPUSS_RAM0_CTL0	0x40210100	RAM 0 control 0
CPUSS_RAM0_PWR_MACRO_CTL0	0x40210140	RAM 0 power control
CPUSS_RAM0_PWR_MACRO_CTL1	0x40210144	RAM 0 power control. See CPUSS_RAM0_PWR_MACRO_CTL0 for the details of bit fields.
CPUSS_RAM0_PWR_MACRO_CTL2	0x40210148	RAM 0 power control. See CPUSS_RAM0_PWR_MACRO_CTL0 for the details of bit fields.
CPUSS_RAM0_PWR_MACRO_CTL3	0x4021014C	RAM 0 power control. See CPUSS_RAM0_PWR_MACRO_CTL0 for the details of bit fields.
CPUSS_RAM0_PWR_MACRO_CTL4	0x40210150	RAM 0 power control. See CPUSS_RAM0_PWR_MACRO_CTL0 for the details of bit fields.
CPUSS_RAM0_PWR_MACRO_CTL5	0x40210154	RAM 0 power control. See CPUSS_RAM0_PWR_MACRO_CTL0 for the details of bit fields.
CPUSS_RAM0_PWR_MACRO_CTL6	0x40210158	RAM 0 power control. See CPUSS_RAM0_PWR_MACRO_CTL0 for the details of bit fields.
CPUSS_RAM0_PWR_MACRO_CTL7	0x4021015C	RAM 0 power control. See CPUSS_RAM0_PWR_MACRO_CTL0 for the details of bit fields.
CPUSS_RAM0_PWR_MACRO_CTL8	0x40210160	RAM 0 power control. See CPUSS_RAM0_PWR_MACRO_CTL0 for the details of bit fields.
CPUSS_RAM_PWR_DELAY_CTL	0x402101C0	Power up delay used for all SRAM power domains

Register	Address	Description
CPUSS_ROM_CTL	0x402101D0	ROM control
CPUSS_UDB_PWR_CTL	0x402101F0	UDB power control
CPUSS_UDB_PWR_DELAY_CTL	0x402101F4	UDB power control
CPUSS_DP_STATUS	0x40210208	Debug port status
CPUSS_BUFF_CTL	0x40210220	Buffer control
CPUSS_SYSTICK_CTL	0x40210240	SysTick timer control
CPUSS_CM0_VECTOR_TABLE_BASE	0x402102B0	CM0+ vector table base
CPUSS_CM4_VECTOR_TABLE_BASE	0x402102C0	CM4 vector table base
CPUSS_CM0_PC0_HANDLER	0x40210320	CM0+ protection context 0 handler
CPUSS_IDENTITY	0x40210400	Identity
CPUSS_PROTECTION	0x40210500	Protection status
CPUSS_CM0_NMI_CTL	0x40210520	CM0+ NMI control
CPUSS_MBIST_STAT	0x402105A0	Memory BIST status
CPUSS_TRIM_ROM_CTL	0x4021F000	ROM trim control
CPUSS_TRIM_RAM_CTL	0x4021F004	RAM trim control

4.1.1 CPUSS_CM0_CTL

CM0+ control

Address: 0x40210000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						RW1S	R
Name	None [7:2]						ENABLED	SLV_STALL

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VECTKEYSTAT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VECTKEYSTAT [31:24]							

Bits	Name	Description
31 : 16	VECTKEYSTAT	Register key (to prevent accidental writes). - Should be written with a 0x05fa key value for the write to take effect. - Always reads as 0xfa05. Default Value: 64005
1	ENABLED	Processor enable: '0': Disabled. Processor clock is turned off and reset is activated. After SW clears this field to '0', HW automatically sets this field to '1'. This effectively results in a CM0+ reset, followed by a CM0+ warm boot. '1': Enabled. Note: The intent is that this bit is modified only through an external probe or by the CM4 while the CM0+ is in Sleep or DeepSleep power mode. If this field is cleared to '0' by the CM0+ itself, it should be done under controlled conditions (such that undesirable side effects can be prevented). Note: The CM0+ CPU has a AIRCR.SYSRESETREQ register field that allows the CM0+ to reset the complete device (ENABLED only disables/enables the CM0+), resulting in a warm boot. This CPU register field has similar "built-in protection" as this CM0_CTL register to prevent accidental system writes (the upper 16-bits of the register need to be written with a 0x05fa key value; see CPU user manual for more details). Default Value: 1

0	SLV_STALL	Processor debug access control: '0': Access. '1': Stall access. This field is used to stall/delay debug accesses. This is useful to protect execution of code that needs to be protected from debug accesses. Default Value: 0

4.1.2 CPUSS_CM0_STATUS

CM0+ status

Address: 0x40210008

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						W	W
Name	None [7:2]						SLEEP-DEEP	SLEEPING

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	SLEEPDEEP	Specifies if the CPU is in Sleep or DeepSleep power mode. See SLEEPING field. Default Value: 0
0	SLEEPING	Specifies if the CPU is in Active, Sleep or DeepSleep power mode: - Active power mode: SLEEPING is '0'. - Sleep power mode: SLEEPING is '1' and SLEEPDEEP is '0'. - DeepSleep power mode: SLEEPING is '1' and SLEEPDEEP is '1'. Default Value: 0

4.1.3 CPUSS_CM0_CLOCK_CTL

CM0+ clock control

Address: 0x40210010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	SLOW_INT_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	PERI_INT_DIV [31:24]							

Bits	Name	Description
31 : 24	PERI_INT_DIV	Specifies the peripheral clock divider (from the high frequency clock "clk_hf" to the peripheral clock "clk_peri"). Integer division by (1+PERI_INT_DIV). Allows for integer divisions in the range [1, 256] (PERI_INT_DIV is in the range [0, 255]). Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Note that Fperi <= Fperi_max. Fperi_max is likely to be smaller than Fhf_max. In other words, if Fhf = Fhf_max, PERI_INT_DIV should not be set to "0". Default Value: 1
15 : 8	SLOW_INT_DIV	Specifies the slow clock divider (from the peripheral clock "clk_peri" to the slow clock "clk_slow"). Integer division by (1+SLOW_INT_DIV). Allows for integer divisions in the range [1, 256] (SLOW_INT_DIV is in the range [0, 255]). Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0

4.1.4 CPUSS_CM0_INT_CTL0

CM0+ interrupt control 0

Address: 0x40210020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	MUX0_SEL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	MUX1_SEL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	MUX2_SEL [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	MUX3_SEL [31:24]							

Bits	Name	Description
31 : 24	MUX3_SEL	System interrupt select for CPU interrupt source 3. Default Value: 240
23 : 16	MUX2_SEL	System interrupt select for CPU interrupt source 2. Default Value: 240
15 : 8	MUX1_SEL	System interrupt select for CPU interrupt source 1. Default Value: 240
7 : 0	MUX0_SEL	System interrupt select for CPU interrupt source 0. If the field value is 240, no system interrupt is connected and the CPU interrupt source is always '0'/de-activated. Default Value: 240

4.1.5 CPUSS_CM0_INT_CTL1

CM0+ interrupt control 1

Address: 0x40210024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	MUX0_SEL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	MUX1_SEL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	MUX2_SEL [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	MUX3_SEL [31:24]							

Bits	Name	Description
31 : 24	MUX3_SEL	System interrupt select for CPU interrupt source 7. Default Value: 240
23 : 16	MUX2_SEL	System interrupt select for CPU interrupt source 6. Default Value: 240
15 : 8	MUX1_SEL	System interrupt select for CPU interrupt source 5. Default Value: 240
7 : 0	MUX0_SEL	System interrupt select for CPU interrupt source 4. Default Value: 240

4.1.6 CPUSS_CM0_INT_CTL2

CM0+ interrupt control 2

Address: 0x40210028

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	MUX0_SEL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	MUX1_SEL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	MUX2_SEL [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	MUX3_SEL [31:24]							

Bits	Name	Description
31 : 24	MUX3_SEL	System interrupt select for CPU interrupt source 11. Default Value: 240
23 : 16	MUX2_SEL	System interrupt select for CPU interrupt source 10. Default Value: 240
15 : 8	MUX1_SEL	System interrupt select for CPU interrupt source 9. Default Value: 240
7 : 0	MUX0_SEL	System interrupt select for CPU interrupt source 8. Default Value: 240

4.1.7 CPUSS_CM0_INT_CTL3

CM0+ interrupt control 3

Address: 0x4021002C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	MUX0_SEL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	MUX1_SEL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	MUX2_SEL [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	MUX3_SEL [31:24]							

Bits	Name	Description
31 : 24	MUX3_SEL	System interrupt select for CPU interrupt source 15. Default Value: 240
23 : 16	MUX2_SEL	System interrupt select for CPU interrupt source 14. Default Value: 240
15 : 8	MUX1_SEL	System interrupt select for CPU interrupt source 13. Default Value: 240
7 : 0	MUX0_SEL	System interrupt select for CPU interrupt source 12. Default Value: 240

4.1.8 CPUSS_CM0_INT_CTL4

CM0+ interrupt control 4

Address: 0x40210030

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	MUX0_SEL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	MUX1_SEL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	MUX2_SEL [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	MUX3_SEL [31:24]							

Bits	Name	Description
31 : 24	MUX3_SEL	System interrupt select for CPU interrupt source 19. Default Value: 240
23 : 16	MUX2_SEL	System interrupt select for CPU interrupt source 18. Default Value: 240
15 : 8	MUX1_SEL	System interrupt select for CPU interrupt source 17. Default Value: 240
7 : 0	MUX0_SEL	System interrupt select for CPU interrupt source 16. Default Value: 240

4.1.9 CPUSS_CM0_INT_CTL5

CM0+ interrupt control 5

Address: 0x40210034

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	MUX0_SEL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	MUX1_SEL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	MUX2_SEL [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	MUX3_SEL [31:24]							

Bits	Name	Description
31 : 24	MUX3_SEL	System interrupt select for CPU interrupt source 23. Default Value: 240
23 : 16	MUX2_SEL	System interrupt select for CPU interrupt source 22. Default Value: 240
15 : 8	MUX1_SEL	System interrupt select for CPU interrupt source 21. Default Value: 240
7 : 0	MUX0_SEL	System interrupt select for CPU interrupt source 20. Default Value: 240

4.1.10 CPUSS_CM0_INT_CTL6

CM0+ interrupt control 6

Address: 0x40210038

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	MUX0_SEL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	MUX1_SEL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	MUX2_SEL [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	MUX3_SEL [31:24]							

Bits	Name	Description
31 : 24	MUX3_SEL	System interrupt select for CPU interrupt source 27. Default Value: 240
23 : 16	MUX2_SEL	System interrupt select for CPU interrupt source 26. Default Value: 240
15 : 8	MUX1_SEL	System interrupt select for CPU interrupt source 25. Default Value: 240
7 : 0	MUX0_SEL	System interrupt select for CPU interrupt source 24. Default Value: 240

4.1.11 CPUSS_CM0_INT_CTL7

CM0+ interrupt control 7

Address: 0x4021003C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	MUX0_SEL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	MUX1_SEL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	MUX2_SEL [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	MUX3_SEL [31:24]							

Bits	Name	Description
31 : 24	MUX3_SEL	System interrupt select for CPU interrupt source 31. Default Value: 240
23 : 16	MUX2_SEL	System interrupt select for CPU interrupt source 30. Default Value: 240
15 : 8	MUX1_SEL	System interrupt select for CPU interrupt source 29. Default Value: 240
7 : 0	MUX0_SEL	System interrupt select for CPU interrupt source 28. Default Value: 240

4.1.12 CPUSS_CM4_PWR_CTL

CM4 power control

Address: 0x40210080

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	
HW Access	None						R	
Name	None [7:2]						PWR_MODE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VECTKEYSTAT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VECTKEYSTAT [31:24]							

Bits	Name	Description
31 : 16	VECTKEYSTAT	Register key (to prevent accidental writes). - Should be written with a 0x05fa key value for the write to take effect. - Always reads as 0xfa05. Default Value: 64005
1 : 0	PWR_MODE	Set Power mode for CM4 Default Value: 1 **0x0: OFF :** Switch CM4 offPower off, clock off, isolate, reset and no retain. **0x1: RESET :** Reset CM4 Clock off, no isolated, no retain and reset. Note: The CM4 CPU has a AIRCR.SYSRESETREQ register field that allows the CM4 to reset the complete device (RESET only resets the CM4), resulting in a warm boot.

4.1.12 CPUSS_CM4_PWR_CTL (continued)

0x2: RETAINED :
Put CM4 in Retained mode
This can only become effective if CM4 is in SleepDeep mode. Check PWR_DONE flag to see if CM4 RETAINED state has been reached.
Power off, clock off, isolate, no reset and retain.

0x3: ENABLED :
Switch CM4 on.
Power on, clock on, no isolate, no reset and no retain.

4.1.13 CPUSS_CM4_PWR_DELAY_CTL

CM4 power control

Address: 0x40210084

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	UP [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						UP [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 0	UP	Number clock cycles delay needed after power domain power up Default Value: 300

4.1.14 CPUSS_CM4_STATUS

CM4 status

Address: 0x40210088

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			R	None		R	R
HW Access	None			W	None		W	W
Name	None [7:5]			PWR_-DONE	None [3:2]		SLEEP-DEEP	SLEEPING

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4	PWR_DONE	After a PWR_MODE change this flag indicates if the new power mode has taken effect or not. Note: this flag can also change as a result of a change in debug power up req Default Value: 1
1	SLEEPDEEP	Specifies if the CPU is in Sleep or DeepSleep power mode. See SLEEPING field. Default Value: 1
0	SLEEPING	Specifies if the CPU is in Active, Sleep or DeepSleep power mode: - Active power mode: SLEEPING is '0'. - Sleep power mode: SLEEPING is '1' and SLEEPDEEP is '0'. - DeepSleep power mode: SLEEPING is '1' and SLEEPDEEP is '1'. Default Value: 1

4.1.15 CPUSS_CM4_CLOCK_CTL

CM4 clock control

Address: 0x40210090

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	FAST_INT_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 8	FAST_INT_DIV	Specifies the fast clock divider (from the high frequency clock "clk_hf" to the peripheral clock "clk_fast"). Integer division by (1+FAST_INT_DIV). Allows for integer divisions in the range [1, 256] (FAST_INT_DIV is in the range [0, 255]). Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0

4.1.16 CPUSS_CM4_NMI_CTL

CM4 NMI control

Address: 0x402100A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	MUX0_SEL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	MUX0_SEL	System interrupt select for CPU NMI. The reset value ensure that the CPU NMI is NOT connect-ed to any system interrupt after DeepSleep reset. Default Value: 240

4.1.17 CPUSS_RAM0_CTL0

RAM 0 control 0

Address: 0x40210100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	
HW Access	None						R	
Name	None [7:2]						SLOW_WS [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						FAST_WS [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 8	FAST_WS	Memory wait states for the fast clock domain ("clk_fast"). The number of wait states is expressed in "clk_hf" clock domain cycles. Default Value: 0
1 : 0	SLOW_WS	Memory wait states for the slow clock domain ("clk_slow"). The number of wait states is expressed in "clk_hf" clock domain cycles. Default Value: 1

4.1.18 CPUSS_RAM0_PWR_MACRO_CTL0

RAM 0 power control

Address: 0x40210140

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	
HW Access	None						R	
Name	None [7:2]						PWR_MODE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VECTKEYSTAT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VECTKEYSTAT [31:24]							

Bits	Name	Description
31 : 16	VECTKEYSTAT	Register key (to prevent accidental writes). - Should be written with a 0x05fa key value for the write to take effect. - Always reads as 0xfa05. Default Value: 64005
1 : 0	PWR_MODE	Set Power mode for 1 SRAM0 Macro Default Value: 3 **0x0: OFF :** See CM4_PWR_CTL **0x1: RESERVED :** undefined **0x2: RETAINED :** See CM4_PWR_CTL **0x3: ENABLED :** See CM4_PWR_CTL

4.1.19 CPUSS_RAM_PWR_DELAY_CTL

Power up delay used for all SRAM power domains

Address: 0x402101C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	UP [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						UP [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 0	UP	Number clock cycles delay needed after power domain power up Default Value: 150

4.1.20 CPUSS_ROM_CTL

ROM control

Address: 0x402101D0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	
HW Access	None						R	
Name	None [7:2]						SLOW_WS [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						FAST_WS [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 8	FAST_WS	Memory wait states for the fast clock domain ("clk_fast"). The number of wait states is expressed in "clk_hf" clock domain cycles. Default Value: 0
1 : 0	SLOW_WS	Memory wait states for the slow clock domain ("clk_slow"). The number of wait states is expressed in "clk_hf" clock domain cycles. Timing paths to and from the memory have a (fixed) minimum duration that always needs to be considered/met. The "clk_hf" clock domain frequency determines this field's value such that the timing paths minimum duration is met. A table/formula will be provided for this field's values for different "clk_hf" frequencies. Default Value: 1

4.1.21 CPUSS_UDB_PWR_CTL

UDB power control

Address: 0x402101F0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	
HW Access	None						R	
Name	None [7:2]						PWR_MODE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VECTKEYSTAT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VECTKEYSTAT [31:24]							

Bits	Name	Description
31 : 16	VECTKEYSTAT	Register key (to prevent accidental writes). - Should be written with a 0x05fa key value for the write to take effect. - Always reads as 0xfa05. Default Value: 64005
1 : 0	PWR_MODE	Set Power mode for UDBs Default Value: 1 **0x0: OFF :** See CM4_PWR_CTL **0x1: RESET :** See CM4_PWR_CTL **0x2: RETAINED :** See CM4_PWR_CTL **0x3: ENABLED :** See CM4_PWR_CTL

4.1.22 CPUSS_UDB_PWR_DELAY_CTL

UDB power control

Address: 0x402101F4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	UP [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						UP [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 0	UP	Number clock cycles delay needed after power domain power up Default Value: 300

4.1.23 CPUSS_DP_STATUS

Debug port status

Address: 0x40210208

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					R	R	R
HW Access	None					W	W	W
Name	None [7:3]					SWJ_-JTAG_SEL	SWJ_DE-BUG_EN	SWJ_CON-NECTED

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	SWJ_JTAG_SEL	Specifies if the JTAG or SWD interface is selected. This signal is valid when DP_CTL.PTM_SEL is '0' (SWJ mode selected) and SWJ_CONNECTED is '1' (SWJ is connected). '0': SWD selected. '1': JTAG selected. Default Value: 1
1	SWJ_DEBUG_EN	Specifies if SWJ debug is enabled, i.e. CDBGPWRUPACK is '1' and thus debug clocks are on: '0': Disabled. '1': Enabled. Default Value: 0
0	SWJ_CONNECTED	Specifies if the SWJ debug port is connected; i.e. debug host interface is active: '0': Not connected/not active. '1': Connected/active. Default Value: 0

4.1.24 CPUSS_BUFF_CTL

Buffer control

Address: 0x40210220

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							WRITE_BUFF

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	WRITE_BUFF	Specifies if write transfer can be buffered in the bus infrastructure bridges: '0': Write transfers are not buffered, independent of the transfer's bufferable attribute. '1': Write transfers can be buffered, if the transfer's bufferable attribute indicates that the transfer is a bufferable/posted write. Default Value: 1

4.1.25 CPUSS_SYSTICK_CTL

SysTick timer control

Address: 0x40210240

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	TENMS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	TENMS [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	TENMS [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None				RW	
HW Access	R	R	None				R	
Name	NOREF	SKEW	None [29:26]				CLOCK_SOURCE [25:24]	

Bits	Name	Description
31	NOREF	Specifies if an external clock source is provided: '0': An external clock source is provided. '1': An external clock source is NOT provided and only the CPU internal clock can be used as SysTick timer clock source. Default Value: 0
30	SKEW	Specifies the precision of the clock source and if the TENMS field represents exactly 10 ms (clock source frequency is a multiple of 100 Hz). This affects the suitability of the SysTick timer as a SW real-time clock: 0: Precise. 1: Imprecise. Default Value: 1

25 : 24	CLOCK_SOURCE	Specifies an external clock source: 0: The low frequency clock clk_lf is selected. The precision of this clock depends on whether the low frequency clock source is a SRSS internal RC oscillator (imprecise) or a device external crystal oscillator (precise). 1: The internal main oscillator (IMO) clock clk_imo is selected. o 2: The external crystal oscillator (ECO) clock clk_eco is selected. 3: The SRSS "clk_timer" is selected ("clk_timer" is a divided/gated version of "clk_hf" or "clk_imo"). Note: If NOREF is 1, the CLOCK_SOURCE value is NOT used. Note: It is SWs responsibility to provide the correct NOREF, SKEW and TENMS field values for the selected clock source. Default Value: 0
23 : 0	TENMS	Specifies the number of clock source cycles (minus 1) that make up 10 ms. E.g., for a 32,768 Hz reference clock, TENMS is 328 1 = 327. Default Value: 327

4.1.26 CPUSS_CM0_VECTOR_TABLE_BASE

CM0+ vector table base

Address: 0x402102B0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	Address of CM0+ vector table. Note: the CM0+ vector table is at an address that is a 256 B multiple. Default Value: 0

4.1.27 CPUSS_CM4_VECTOR_TABLE_BASE

CM4 vector table base

Address: 0x402102C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW						None	
HW Access							None	
Name	ADDR22 [15:10]						None [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	ADDR22 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	ADDR22 [31:24]							

Bits	Name	Description
31 : 10	ADDR22	Address of CM4 vector table. Note: the CM4 vector table is at an address that is a 1024 B multiple. Default Value: 0

4.1.28 CPUSS_CM0_PC0_HANDLER

CM0+ protection context 0 handler

Address: 0x40210320

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Address of the protection context 0 handler. This field is used to detect entry to Cypress "trusted" code through an exception/interrupt. Default Value: 0

4.1.29 CPUSS_IDENTITY

Identity

Address: 0x40210400

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				None		R	R
HW Access	W				None		W	W
Name	PC [7:4]				None [3:2]		NS	P

Bits	15	14	13	12	11	10	9	8
SW Access	None				R			
HW Access	None				W			
Name	None [15:12]				MS [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11 : 8	MS	This field specifies the bus master identifier of the transfer that reads the register. Default Value: Undefined
7 : 4	PC	This field specifies the protection context of the transfer that reads the register. Default Value: Undefined
1	NS	This field specifies the security setting ('0': secure mode; '1': non-secure mode) of the transfer that reads the register. Default Value: Undefined
0	P	This field specifies the privileged setting ('0': user mode; '1': privileged mode) of the transfer that reads the register. Default Value: Undefined

4.1.30 CPUSS_PROTECTION

Protection status

Address: 0x40210500

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW		
HW Access	None					R		
Name	None [7:3]					STATE [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2 : 0	STATE	Protection state: "0": UNKNOWN. "1": VIRGIN. "2": NORMAL. "3": SECURE. "4": DEAD. The following state transitions are allowed (and enforced by HW): - UNKNOWN => VIRGIN/NORMAL/SECURE/DEAD - NORMAL => DEAD - SECURE => DEAD An attempt to make a NOT allowed state transition will NOT affect this register field. Default Value: 0

4.1.31 CPUSS_CM0_NMI_CTL

CM0+ NMI control

Address: 0x40210520

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	MUX0_SEL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	MUX0_SEL	System interrupt select for CPU NMI. The reset value ensures that the CPU NMI is NOT connected to any system interrupt after DeepSleep reset. Default Value: 240

4.1.32 CPUSS_MBIST_STAT

Memory BIST status

Address: 0x402105A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						RW	RW
Name	None [7:2]						SFP_FAIL	SF-P_READY

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	SFP_FAIL	Report status of the BIST run, only valid if SFP_READY=1 Default Value: 0
0	SFP_READY	Flag indicating the BIST run is done. Note that after starting a BIST run this flag must be set be-fore a new run can be started. For the first BIST run this will be 0. Default Value: 0

4.1.33 CPUSS_TRIM_ROM_CTL

ROM trim control

Address: 0x4021F000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW			
HW Access	None			R	R			
Name	None [7:5]			RME	RM [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4	RME	Read-Write margin enable control. This selects between the default Read-Write margin setting, and the external pin Read-Write margin setting. Default Value: 0
3 : 0	RM	Read-Write margin control. This is used for setting the Read-Write margin. It programs the sense amplifier differential setting and allows the trade off between speed and robustness. - RM[1:0] values control access time and cycle time of the memory. RM[1:0] = "0" is the slowest possible mode of operation for the memory. This setting is required for VDDMIN operation. - RM[3:2] are factory pins reserved for debug mode and should be set to "0". Default Value: 2

4.1.34 CPUSS_TRIM_RAM_CTL

RAM trim control

Address: 0x4021F004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW			RW	RW			
HW Access	R			R	R			
Name	WPULSE [7:5]			RME	RM [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW			None		RW	
HW Access	None	R			None		R	
Name	None	WA [14:12]			None [11:10]		RA [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
14 : 12	WA	Write assist enable control (Active High). - WA[1:0] Write Assist pins to control negative voltage on SRAM bitline. Default Value: 6
9 : 8	RA	Read Assist control for WL under-drive. Default Value: 0
7 : 5	WPULSE	Write Assist Pulse to control pulse width of negative voltage on SRAM bitline. Default Value: 0
4	RME	Read-Write margin enable control. This selects between the default Read-Write margin setting, and the external RM[3:0] Read-Write margin setting. Default Value: 0
3 : 0	RM	Read-Write margin control. This is used for setting the Read-Write margin. It programs the sense amplifier differential setting and allows the trade off between speed and robustness. - RM[1:0] values control access time and cycle time of the memory. RM[1:0] = "0" is the slowest possible mode of operation for the memory. This setting is required for VDDMIN operation. - RM[3:2] are factory pins reserved for debug mode and should be set to "0". Default Value: 2

5 Fault Registers

This section discusses the Fault registers. It lists all the registers in mapping tables, in address order.

5.1 Register Details

Register	Address	Description
FAULT_STRUCT0_CTL	0x40220000	Fault control
FAULT_STRUCT0_STATUS	0x4022000C	Fault status
FAULT_STRUCT0_DATA0	0x40220010	Fault data
FAULT_STRUCT0_DATA1	0x40220014	Fault data. See FAULT_STRUCT0_DATA0 for the details of bit fields.
FAULT_STRUCT0_DATA2	0x40220018	Fault data. See FAULT_STRUCT0_DATA0 for the details of bit fields.
FAULT_STRUCT0_DATA3	0x4022001C	Fault data. See FAULT_STRUCT0_DATA0 for the details of bit fields.
FAULT_STRUCT0_PENDING0	0x40220040	Fault pending 0
FAULT_STRUCT0_PENDING1	0x40220044	Fault pending 1
FAULT_STRUCT0_PENDING2	0x40220048	Fault pending 2
FAULT_STRUCT0_MASK0	0x40220050	Fault mask 0
FAULT_STRUCT0_MASK1	0x40220054	Fault mask 1
FAULT_STRUCT0_MASK2	0x40220058	Fault mask 2
FAULT_STRUCT0_INTR	0x402200C0	Interrupt
FAULT_STRUCT0_INTR_SET	0x402200C4	Interrupt set
FAULT_STRUCT0_INTR_MASK	0x402200C8	Interrupt mask
FAULT_STRUCT0_INTR_MASKED	0x402200CC	Interrupt masked
FAULT_STRUCT1_CTL	0x40220100	Fault control. See FAULT_STRUCT0_CTL for the details of bit fields.
FAULT_STRUCT1_STATUS	0x4022010C	Fault status. See FAULT_STRUCT0_STATUS for the details of bit fields.
FAULT_STRUCT1_DATA0	0x40220110	Fault data. See FAULT_STRUCT0_DATA0 for the details of bit fields.
FAULT_STRUCT1_DATA1	0x40220114	Fault data. See FAULT_STRUCT0_DATA0 for the details of bit fields.
FAULT_STRUCT1_DATA2	0x40220118	Fault data. See FAULT_STRUCT0_DATA0 for the details of bit fields.
FAULT_STRUCT1_DATA3	0x4022011C	Fault data. See FAULT_STRUCT0_DATA0 for the details of bit fields.
FAULT_STRUCT1_PENDING0	0x40220140	Fault pending 0. See FAULT_STRUCT0_PENDING0 for the details of bit fields.
FAULT_STRUCT1_PENDING1	0x40220144	Fault pending 1. See FAULT_STRUCT0_PENDING1 for the details of bit fields.
FAULT_STRUCT1_PENDING2	0x40220148	Fault pending 2. See FAULT_STRUCT0_PENDING2 for the details of bit fields.
FAULT_STRUCT1_MASK0	0x40220150	Fault mask 0. See FAULT_STRUCT0_MASK0 for the details of bit fields.
FAULT_STRUCT1_MASK1	0x40220154	Fault mask 1. See FAULT_STRUCT0_MASK1 for the details of bit fields.

Register	Address	Description
FAULT_STRUCT1_MASK2	0x40220158	Fault mask 2. See FAULT_STRUCT0_MASK2 for the details of bit fields.
FAULT_STRUCT1_INTR	0x402201C0	Interrupt. See FAULT_STRUCT0_INTR for the details of bit fields.
FAULT_STRUCT1_INTR_SET	0x402201C4	Interrupt set. See FAULT_STRUCT0_INTR_SET for the details of bit fields.
FAULT_STRUCT1_INTR_MASK	0x402201C8	Interrupt mask. See FAULT_STRUCT0_INTR_MASK for the details of bit fields.
FAULT_STRUCT1_INTR_MASKED	0x402201CC	Interrupt masked. See FAULT_STRUCT0_INTR_MASKED for the details of bit fields.

5.1.1 FAULT_STRUCT0_CTL

Fault control

Address: 0x40220000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [7:3]					RESET_REQ_EN	OUT_EN	TR_EN

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	RESET_REQ_EN	Reset request enable: '0': Disabled. '1': Enabled. The output reset request signal "fault_reset_req" reflects STATUS.VALID. This reset causes a warm/soft/core reset. This warm/soft/core reset does not affect the fault logic STATUS, DATA0, ..., DATA3 registers (allowing for post soft reset failure analysis). The "fault_reset_req" signals of the individual fault report structures are combined (logically OR'd) into a single SRSS "fault_reset_req" signal. Default Value: 0
1	OUT_EN	IO output signal enable: '0': Disabled. The IO output signal "fault_out" is '0'. The IO output enable signal "fault_out_en" is '0'. '1': Enabled. The IO output signal "fault_out" reflects STATUS.VALID. The IO output enable signal "fault_out_en" is '1'. Default Value: 0

5.1.1 FAULT_STRUCT0_CTL (continued)

0	TR_EN	Trigger output enable: '0': Disabled. The trigger output "tr_fault" is '0'. '1': Enabled. The trigger output "tr_fault" reflects STATUS.VALID. The trigger can be used to initiate a Datawire transfer of the FAULT data (FAULT_DATA0 through FAULT_DATA3). Default Value: 0

5.1.2 FAULT_STRUCT0_STATUS

Fault status

Address: 0x4022000C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	R						
HW Access	None	W						
Name	None	IDX [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW0C	None						
HW Access	RW1S	None						
Name	VALID	None [30:24]						

Bits	Name	Description
31	VALID	Valid indication: '0': Invalid. '1': Valid. HW sets this field to '1' when new fault source data is captured. New fault source data is ONLY captured when VALID is '0'. SW can clear this field to '0' when the fault is handled (by SW). Default Value: 0
6 : 0	IDX	The fault source index for which fault information is captured in DATA0 through DATA3. The fault information is fault source specific and described below. Note: this register field (and associated fault source data in DATA0 through DATA3) should only be considered valid, when VALID is '1'. Default Value: Undefined

5.1.2 FAULT_STRUCT0_STATUS (continued)

0x0: MPU_0 :
Bus master 0 MPU/SMPU.
DATA0[31:0]: Violating address.
DATA1[0]: User read.
DATA1[1]: User write.
DATA1[2]: User execute.
DATA1[3]: Privileged read.
DATA1[4]: Privileged write.
DATA1[5]: Privileged execute.
DATA1[6]: Non-secure.
DATA1[11:8]: Master identifier.
DATA1[15:12]: Protection context identifier.
DATA1[31]: '0' MPU violation; '1': SMPU violation.

0x1: MPU_1 :
Bus master 1 MPU. See MPU_0 description.

0x2: MPU_2 :
Bus master 2 MPU. See MPU_0 description.

0x3: MPU_3 :
Bus master 3 MPU. See MPU_0 description.

0x4: MPU_4 :
Bus master 4 MPU. See MPU_0 description.

0x5: MPU_5 :
Bus master 5 MPU. See MPU_0 description.

0x6: MPU_6 :
Bus master 6 MPU. See MPU_0 description.

0x7: MPU_7 :
Bus master 7 MPU. See MPU_0 description.

0x8: MPU_8 :
Bus master 8 MPU. See MPU_0 description.

0x9: MPU_9 :
Bus master 9 MPU. See MPU_0 description.

0xa: MPU_10 :
Bus master 10 MPU. See MPU_0 description.

0xb: MPU_11 :
Bus master 11 MPU. See MPU_0 description.

0xc: MPU_12 :
Bus master 12 MPU. See MPU_0 description.

0xd: MPU_13 :
Bus master 13 MPU. See MPU_0 description.

0xe: MPU_14 :
Bus master 14 MPU. See MPU_0 description.

0xf: MPU_15 :
Bus master 15 MPU. See MPU_0 description.

0x10: CM4_SYS_MPU :
CM4 system bus AHB-Lite interface MPU. See MPU_0 description.

5.1.2 FAULT_STRUCT0_STATUS (continued)

0x1c: MS_PPU_0 :
Peripheral master interface 0 PPU.
DATA0[31:0]: Violating address.
DATA1[0]: User read.
DATA1[1]: User write.
DATA1[2]: User execute.
DATA1[3]: Privileged read.
DATA1[4]: Privileged write.
DATA1[5]: Privileged execute.
DATA1[6]: Non-secure.
DATA1[11:8]: Master identifier.
DATA1[15:12]: Protection context identifier.
DATA1[31]: '0': PPU violation, '1': peripheral bus error.

0x1d: MS_PPU_1 :
Peripheral master interface 0 PPU. See MS_PPU_0 description.

0x1e: MS_PPU_2 :
Peripheral master interface 1 PPU. See MS_PPU_0 description.

0x1f: MS_PPU_3 :
Peripheral master interface 2 PPU. See MS_PPU_0 description.

0x20: GROUP_PPU_0 :
Peripheral group 0 PPU.
DATA0[31:0]: Violating address.
DATA1[0]: User read.
DATA1[1]: User write.
DATA1[2]: User execute.
DATA1[3]: Privileged read.
DATA1[4]: Privileged write.
DATA1[5]: Privileged execute.
DATA1[6]: Non-secure.
DATA1[11:8]: Master identifier.
DATA1[15:12]: Protection context identifier.
DATA1[31:30]: "0": PPU violation, "1": timeout detected, "2": peripheral bus error.

0x21: GROUP_PPU_1 :
Peripheral group 1 PPU. See GROUP_PPU_0 description.

0x22: GROUP_PPU_2 :
Peripheral group 2 PPU. See GROUP_PPU_0 description.

0x23: GROUP_PPU_3 :
Peripheral group 3 PPU. See GROUP_PPU_0 description.

0x24: GROUP_PPU_4 :
Peripheral group 4 PPU. See GROUP_PPU_0 description.

0x25: GROUP_PPU_5 :
Peripheral group 5 PPU. See GROUP_PPU_0 description.

0x26: GROUP_PPU_6 :
Peripheral group 6 PPU. See GROUP_PPU_0 description.

0x27: GROUP_PPU_7 :
Peripheral group 7 PPU. See GROUP_PPU_0 description.

0x28: GROUP_PPU_8 :
Peripheral group 8 PPU. See GROUP_PPU_0 description.

0x29: GROUP_PPU_9 :
Peripheral group 9 PPU. See GROUP_PPU_0 description.

5.1.2 FAULT_STRUCT0_STATUS (continued)

0x2a: GROUP_PPU_10 :
Peripheral group 10 PPU. See GROUP_PPU_0 description.

0x2b: GROUP_PPU_11 :
Peripheral group 11 PPU. See GROUP_PPU_0 description.

0x2c: GROUP_PPU_12 :
Peripheral group 12 PPU. See GROUP_PPU_0 description.

0x2d: GROUP_PPU_13 :
Peripheral group 13 PPU. See GROUP_PPU_0 description.

0x2e: GROUP_PPU_14 :
Peripheral group 14 PPU. See GROUP_PPU_0 description.

0x2f: GROUP_PPU_15 :
Peripheral group 15 PPU. See GROUP_PPU_0 description.

0x32: FLASHC_MAIN_BUS_ERROR :
Flash controller, main interface, bus error:
FAULT_DATA0[31:0]: Violating address.
FAULT_DATA1[31]: '0': FLASH macro interface bus error; '1': memory hole.
FAULT_DATA1[15:12]: Protection context identifier.
FAULT_DATA1[11:8]: Master identifier.

5.1.3 FAULT_STRUCT0_DATA0

Fault data

Address: 0x40220010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Captured fault source data. Note: the fault source index STATUS.IDX specifies the format of the DATA registers. Default Value: Undefined

5.1.4 FAULT_STRUCT0_PENDING0

Fault pending 0

Address: 0x40220040

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	SOURCE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	SOURCE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	SOURCE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	SOURCE [31:24]							

Bits	Name	Description
31 : 0	SOURCE	This field specifies the following sources: Bit 0: CM0 MPU. Bit 1: CRYPTO MPU. Bit 2: DW 0 MPU. Bit 3: DW 1 MPU. ... Bit 14: CM4 code bus MPU. Bit 15: DAP MPU. Bit 16: CM4 s+G92ystem bus MPU. Bit 28: Peripheral master interface 0 PPU. Bit 29: Peripheral master interface 1 PPU. Bit 30: Peripheral master interface 2 PPU. Bit 31: Peripheral master interface 3 PPU. Default Value: Undefined

5.1.5 FAULT_STRUCT0_PENDING1

Fault pending 1

Address: 0x40220044

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	SOURCE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	SOURCE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	SOURCE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	SOURCE [31:24]							

Bits	Name	Description
31 : 0	SOURCE	This field specifies the following sources: Bit 0: Peripheral group 0 PPU. Bit 1: Peripheral group 1 PPU. Bit 2: Peripheral group 2 PPU. Bit 3: Peripheral group 3 PPU. Bit 4: Peripheral group 4 PPU. Bit 5: Peripheral group 5 PPU. Bit 6: Peripheral group 6 PPU. Bit 7: Peripheral group 7 PPU. ... Bit 15: Peripheral group 15 PPU. Bit 18: Flash controller, main interface, bus error. Default Value: Undefined

5.1.6 FAULT_STRUCT0_PENDING2

Fault pending 2

Address: 0x40220048

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	SOURCE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	SOURCE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	SOURCE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	SOURCE [31:24]							

Bits	Name	Description
31 : 0	SOURCE	Reserved. Default Value: Undefined

5.1.7 FAULT_STRUCT0_MASK0

Fault mask 0

Address: 0x40220050

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SOURCE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	SOURCE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	SOURCE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	SOURCE [31:24]							

Bits	Name	Description
31 : 0	SOURCE	Fault source enables: Bits 31-0: Fault sources 31 to 0. Default Value: 0

5.1.8 FAULT_STRUCT0_MASK1

Fault mask 1

Address: 0x40220054

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SOURCE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	SOURCE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	SOURCE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	SOURCE [31:24]							

Bits	Name	Description
31 : 0	SOURCE	Fault source enables: Bits 31-0: Fault sources 63 to 32. Default Value: 0

5.1.9 FAULT_STRUCT0_MASK2

Fault mask 2

Address: 0x40220058

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SOURCE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	SOURCE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	SOURCE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	SOURCE [31:24]							

Bits	Name	Description
31 : 0	SOURCE	Fault source enables: Bits 31-0: Fault sources 95 to 64. Default Value: 0

5.1.10 FAULT_STRUCT0_INTR

Interrupt

Address: 0x402200C0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1C
HW Access	None							RW1S
Name	None [7:1]							FAULT

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	FAULT	This interrupt cause field is activated (HW sets the field to '1') when an enabled (MASK0/MASK1/MASK2) pending fault source is captured: - STATUS.VALID is set to '1'. - STATUS.IDX specifies the fault source index. - DATA0 through DATA3 captures the fault source data. SW writes a '1' to these field to clear the interrupt cause to '0'. Default Value: 0

5.1.11 FAULT_STRUCT0_INTR_SET

Interrupt set

Address: 0x402200C4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1S
HW Access	None							A
Name	None [7:1]							FAULT

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	FAULT	SW writes a '1' to this field to set the corresponding field in the INTR register. Default Value: 0

5.1.12 FAULT_STRUCT0_INTR_MASK

Interrupt mask

Address: 0x402200C8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							FAULT

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	FAULT	Mask bit for corresponding field in the INTR register. Default Value: 0

5.1.13 FAULT_STRUCT0_INTR_MASKED

Interrupt masked

Address: 0x402200CC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							W
Name	None [7:1]							FAULT

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	FAULT	Logical and of corresponding INTR and INTR_MASK fields. Default Value: 0

6 Inter-Processor Communication Registers

This section discusses the Inter-Processor Communication (IPC) registers. It lists all the registers in mapping tables, in address order.

6.1 Register Details

Register	Address	Description
IPC_STRUCT0_ACQUIRE	0x40230000	IPC acquire
IPC_STRUCT0_RELEASE	0x40230004	IPC release
IPC_STRUCT0_NOTIFY	0x40230008	IPC notification
IPC_STRUCT0_DATA	0x4023000C	IPC data
IPC_STRUCT0_LOCK_STATUS	0x40230010	IPC lock status
IPC_STRUCT1_ACQUIRE	0x40230020	IPC acquire. See IPC_STRUCT0_ACQUIRE for the details of bit fields.
IPC_STRUCT1_RELEASE	0x40230024	IPC release. See IPC_STRUCT0_RELEASE for the details of bit fields.
IPC_STRUCT1_NOTIFY	0x40230028	IPC notification. See IPC_STRUCT0_NOTIFY for the details of bit fields.
IPC_STRUCT1_DATA	0x4023002C	IPC data. See IPC_STRUCT0_DATA for the details of bit fields.
IPC_STRUCT1_LOCK_STATUS	0x40230030	IPC lock status. See IPC_STRUCT0_LOCK_STATUS for the details of bit fields.
IPC_STRUCT2_ACQUIRE	0x40230040	IPC acquire. See IPC_STRUCT0_ACQUIRE for the details of bit fields.
IPC_STRUCT2_RELEASE	0x40230044	IPC release. See IPC_STRUCT0_RELEASE for the details of bit fields.
IPC_STRUCT2_NOTIFY	0x40230048	IPC notification. See IPC_STRUCT0_NOTIFY for the details of bit fields.
IPC_STRUCT2_DATA	0x4023004C	IPC data. See IPC_STRUCT0_DATA for the details of bit fields.
IPC_STRUCT2_LOCK_STATUS	0x40230050	IPC lock status. See IPC_STRUCT0_LOCK_STATUS for the details of bit fields.
IPC_STRUCT3_ACQUIRE	0x40230060	IPC acquire. See IPC_STRUCT0_ACQUIRE for the details of bit fields.
IPC_STRUCT3_RELEASE	0x40230064	IPC release. See IPC_STRUCT0_RELEASE for the details of bit fields.
IPC_STRUCT3_NOTIFY	0x40230068	IPC notification. See IPC_STRUCT0_NOTIFY for the details of bit fields.
IPC_STRUCT3_DATA	0x4023006C	IPC data. See IPC_STRUCT0_DATA for the details of bit fields.
IPC_STRUCT3_LOCK_STATUS	0x40230070	IPC lock status. See IPC_STRUCT0_LOCK_STATUS for the details of bit fields.
IPC_STRUCT4_ACQUIRE	0x40230080	IPC acquire. See IPC_STRUCT0_ACQUIRE for the details of bit fields.
IPC_STRUCT4_RELEASE	0x40230084	IPC release. See IPC_STRUCT0_RELEASE for the details of bit fields.
IPC_STRUCT4_NOTIFY	0x40230088	IPC notification. See IPC_STRUCT0_NOTIFY for the details of bit fields.
IPC_STRUCT4_DATA	0x4023008C	IPC data. See IPC_STRUCT0_DATA for the details of bit fields.
IPC_STRUCT4_LOCK_STATUS	0x40230090	IPC lock status. See IPC_STRUCT0_LOCK_STATUS for the details of bit fields.
IPC_STRUCT5_ACQUIRE	0x402300A0	IPC acquire. See IPC_STRUCT0_ACQUIRE for the details of bit fields.

Register	Address	Description
IPC_STRUCT5_RELEASE	0x402300A4	IPC release. See IPC_STRUCT0_RELEASE for the details of bit fields.
IPC_STRUCT5_NOTIFY	0x402300A8	IPC notification. See IPC_STRUCT0_NOTIFY for the details of bit fields.
IPC_STRUCT5_DATA	0x402300AC	IPC data. See IPC_STRUCT0_DATA for the details of bit fields.
IPC_STRUCT5_LOCK_STATUS	0x402300B0	IPC lock status. See IPC_STRUCT0_LOCK_STATUS for the details of bit fields.
IPC_STRUCT6_ACQUIRE	0x402300C0	IPC acquire. See IPC_STRUCT0_ACQUIRE for the details of bit fields.
IPC_STRUCT6_RELEASE	0x402300C4	IPC release. See IPC_STRUCT0_RELEASE for the details of bit fields.
IPC_STRUCT6_NOTIFY	0x402300C8	IPC notification. See IPC_STRUCT0_NOTIFY for the details of bit fields.
IPC_STRUCT6_DATA	0x402300CC	IPC data. See IPC_STRUCT0_DATA for the details of bit fields.
IPC_STRUCT6_LOCK_STATUS	0x402300D0	IPC lock status. See IPC_STRUCT0_LOCK_STATUS for the details of bit fields.
IPC_STRUCT7_ACQUIRE	0x402300E0	IPC acquire. See IPC_STRUCT0_ACQUIRE for the details of bit fields.
IPC_STRUCT7_RELEASE	0x402300E4	IPC release. See IPC_STRUCT0_RELEASE for the details of bit fields.
IPC_STRUCT7_NOTIFY	0x402300E8	IPC notification. See IPC_STRUCT0_NOTIFY for the details of bit fields.
IPC_STRUCT7_DATA	0x402300EC	IPC data. See IPC_STRUCT0_DATA for the details of bit fields.
IPC_STRUCT7_LOCK_STATUS	0x402300F0	IPC lock status. See IPC_STRUCT0_LOCK_STATUS for the details of bit fields.
IPC_STRUCT8_ACQUIRE	0x40230100	IPC acquire. See IPC_STRUCT0_ACQUIRE for the details of bit fields.
IPC_STRUCT8_RELEASE	0x40230104	IPC release. See IPC_STRUCT0_RELEASE for the details of bit fields.
IPC_STRUCT8_NOTIFY	0x40230108	IPC notification. See IPC_STRUCT0_NOTIFY for the details of bit fields.
IPC_STRUCT8_DATA	0x4023010C	IPC data. See IPC_STRUCT0_DATA for the details of bit fields.
IPC_STRUCT8_LOCK_STATUS	0x40230110	IPC lock status. See IPC_STRUCT0_LOCK_STATUS for the details of bit fields.
IPC_STRUCT9_ACQUIRE	0x40230120	IPC acquire. See IPC_STRUCT0_ACQUIRE for the details of bit fields.
IPC_STRUCT9_RELEASE	0x40230124	IPC release. See IPC_STRUCT0_RELEASE for the details of bit fields.
IPC_STRUCT9_NOTIFY	0x40230128	IPC notification. See IPC_STRUCT0_NOTIFY for the details of bit fields.
IPC_STRUCT9_DATA	0x4023012C	IPC data. See IPC_STRUCT0_DATA for the details of bit fields.
IPC_STRUCT9_LOCK_STATUS	0x40230130	IPC lock status. See IPC_STRUCT0_LOCK_STATUS for the details of bit fields.
IPC_STRUCT10_ACQUIRE	0x40230140	IPC acquire. See IPC_STRUCT0_ACQUIRE for the details of bit fields.
IPC_STRUCT10_RELEASE	0x40230144	IPC release. See IPC_STRUCT0_RELEASE for the details of bit fields.
IPC_STRUCT10_NOTIFY	0x40230148	IPC notification. See IPC_STRUCT0_NOTIFY for the details of bit fields.
IPC_STRUCT10_DATA	0x4023014C	IPC data. See IPC_STRUCT0_DATA for the details of bit fields.
IPC_STRUCT10_LOCK_STATUS	0x40230150	IPC lock status. See IPC_STRUCT0_LOCK_STATUS for the details of bit fields.
IPC_STRUCT11_ACQUIRE	0x40230160	IPC acquire. See IPC_STRUCT0_ACQUIRE for the details of bit fields.
IPC_STRUCT11_RELEASE	0x40230164	IPC release. See IPC_STRUCT0_RELEASE for the details of bit fields.
IPC_STRUCT11_NOTIFY	0x40230168	IPC notification. See IPC_STRUCT0_NOTIFY for the details of bit fields.
IPC_STRUCT11_DATA	0x4023016C	IPC data. See IPC_STRUCT0_DATA for the details of bit fields.
IPC_STRUCT11_LOCK_STATUS	0x40230170	IPC lock status. See IPC_STRUCT0_LOCK_STATUS for the details of bit fields.
IPC_STRUCT12_ACQUIRE	0x40230180	IPC acquire. See IPC_STRUCT0_ACQUIRE for the details of bit fields.
IPC_STRUCT12_RELEASE	0x40230184	IPC release. See IPC_STRUCT0_RELEASE for the details of bit fields.
IPC_STRUCT12_NOTIFY	0x40230188	IPC notification. See IPC_STRUCT0_NOTIFY for the details of bit fields.
IPC_STRUCT12_DATA	0x4023018C	IPC data. See IPC_STRUCT0_DATA for the details of bit fields.
IPC_STRUCT12_LOCK_STATUS	0x40230190	IPC lock status. See IPC_STRUCT0_LOCK_STATUS for the details of bit fields.
IPC_STRUCT13_ACQUIRE	0x402301A0	IPC acquire. See IPC_STRUCT0_ACQUIRE for the details of bit fields.
IPC_STRUCT13_RELEASE	0x402301A4	IPC release. See IPC_STRUCT0_RELEASE for the details of bit fields.
IPC_STRUCT13_NOTIFY	0x402301A8	IPC notification. See IPC_STRUCT0_NOTIFY for the details of bit fields.

Register	Address	Description
IPC_STRUCT13_DATA	0x402301AC	IPC data. See IPC_STRUCT0_DATA for the details of bit fields.
IPC_STRUCT13_LOCK_STATUS	0x402301B0	IPC lock status. See IPC_STRUCT0_LOCK_STATUS for the details of bit fields.
IPC_STRUCT14_ACQUIRE	0x402301C0	IPC acquire. See IPC_STRUCT0_ACQUIRE for the details of bit fields.
IPC_STRUCT14_RELEASE	0x402301C4	IPC release. See IPC_STRUCT0_RELEASE for the details of bit fields.
IPC_STRUCT14_NOTIFY	0x402301C8	IPC notification. See IPC_STRUCT0_NOTIFY for the details of bit fields.
IPC_STRUCT14_DATA	0x402301CC	IPC data. See IPC_STRUCT0_DATA for the details of bit fields.
IPC_STRUCT14_LOCK_STATUS	0x402301D0	IPC lock status. See IPC_STRUCT0_LOCK_STATUS for the details of bit fields.
IPC_STRUCT15_ACQUIRE	0x402301E0	IPC acquire. See IPC_STRUCT0_ACQUIRE for the details of bit fields.
IPC_STRUCT15_RELEASE	0x402301E4	IPC release. See IPC_STRUCT0_RELEASE for the details of bit fields.
IPC_STRUCT15_NOTIFY	0x402301E8	IPC notification. See IPC_STRUCT0_NOTIFY for the details of bit fields.
IPC_STRUCT15_DATA	0x402301EC	IPC data. See IPC_STRUCT0_DATA for the details of bit fields.
IPC_STRUCT15_LOCK_STATUS	0x402301F0	IPC lock status. See IPC_STRUCT0_LOCK_STATUS for the details of bit fields.
IPC_INTR_STRUCT0_INTR	0x40231000	Interrupt
IPC_INTR_STRUCT0_INTR_SET	0x40231004	Interrupt set
IPC_INTR_STRUCT0_INTR_MASK	0x40231008	Interrupt mask
IPC_INTR_STRUCT0_INTR_MASKED	0x4023100C	Interrupt masked
IPC_INTR_STRUCT1_INTR	0x40231020	Interrupt. See IPC_INTR_STRUCT0_INTR for the details of bit fields.
IPC_INTR_STRUCT1_INTR_SET	0x40231024	Interrupt set. See IPC_INTR_STRUCT0_INTR_SET for the details of bit fields.
IPC_INTR_STRUCT1_INTR_MASK	0x40231028	Interrupt mask. See IPC_INTR_STRUCT0_INTR_MASK for the details of bit fields.
IPC_INTR_STRUCT1_INTR_MASKED	0x4023102C	Interrupt masked. See IPC_INTR_STRUCT0_INTR_MASKED for the details of bit fields.
IPC_INTR_STRUCT2_INTR	0x40231040	Interrupt. See IPC_INTR_STRUCT0_INTR for the details of bit fields.
IPC_INTR_STRUCT2_INTR_SET	0x40231044	Interrupt set. See IPC_INTR_STRUCT0_INTR_SET for the details of bit fields.
IPC_INTR_STRUCT2_INTR_MASK	0x40231048	Interrupt mask. See IPC_INTR_STRUCT0_INTR_MASK for the details of bit fields.
IPC_INTR_STRUCT2_INTR_MASKED	0x4023104C	Interrupt masked. See IPC_INTR_STRUCT0_INTR_MASKED for the details of bit fields.
IPC_INTR_STRUCT3_INTR	0x40231060	Interrupt. See IPC_INTR_STRUCT0_INTR for the details of bit fields.
IPC_INTR_STRUCT3_INTR_SET	0x40231064	Interrupt set. See IPC_INTR_STRUCT0_INTR_SET for the details of bit fields.
IPC_INTR_STRUCT3_INTR_MASK	0x40231068	Interrupt mask. See IPC_INTR_STRUCT0_INTR_MASK for the details of bit fields.
IPC_INTR_STRUCT3_INTR_MASKED	0x4023106C	Interrupt masked. See IPC_INTR_STRUCT0_INTR_MASKED for the details of bit fields.
IPC_INTR_STRUCT4_INTR	0x40231080	Interrupt. See IPC_INTR_STRUCT0_INTR for the details of bit fields.
IPC_INTR_STRUCT4_INTR_SET	0x40231084	Interrupt set. See IPC_INTR_STRUCT0_INTR_SET for the details of bit fields.
IPC_INTR_STRUCT4_INTR_MASK	0x40231088	Interrupt mask. See IPC_INTR_STRUCT0_INTR_MASK for the details of bit fields.
IPC_INTR_STRUCT4_INTR_MASKED	0x4023108C	Interrupt masked. See IPC_INTR_STRUCT0_INTR_MASKED for the details of bit fields.
IPC_INTR_STRUCT5_INTR	0x402310A0	Interrupt. See IPC_INTR_STRUCT0_INTR for the details of bit fields.
IPC_INTR_STRUCT5_INTR_SET	0x402310A4	Interrupt set. See IPC_INTR_STRUCT0_INTR_SET for the details of bit fields.
IPC_INTR_STRUCT5_INTR_MASK	0x402310A8	Interrupt mask. See IPC_INTR_STRUCT0_INTR_MASK for the details of bit fields.
IPC_INTR_STRUCT5_INTR_MASKED	0x402310AC	Interrupt masked. See IPC_INTR_STRUCT0_INTR_MASKED for the details of bit fields.
IPC_INTR_STRUCT6_INTR	0x402310C0	Interrupt. See IPC_INTR_STRUCT0_INTR for the details of bit fields.
IPC_INTR_STRUCT6_INTR_SET	0x402310C4	Interrupt set. See IPC_INTR_STRUCT0_INTR_SET for the details of bit fields.
IPC_INTR_STRUCT6_INTR_MASK	0x402310C8	Interrupt mask. See IPC_INTR_STRUCT0_INTR_MASK for the details of bit fields.
IPC_INTR_STRUCT6_INTR_MASKED	0x402310CC	Interrupt masked. See IPC_INTR_STRUCT0_INTR_MASKED for the details of bit fields.
IPC_INTR_STRUCT7_INTR	0x402310E0	Interrupt. See IPC_INTR_STRUCT0_INTR for the details of bit fields.
IPC_INTR_STRUCT7_INTR_SET	0x402310E4	Interrupt set. See IPC_INTR_STRUCT0_INTR_SET for the details of bit fields.

Register	Address	Description
IPC_INTR_STRUCT7_INTR_MASK	0x402310E8	Interrupt mask. See IPC_INTR_STRUCT0_INTR_MASK for the details of bit fields.
IPC_INTR_STRUCT7_INTR_MASKED	0x402310EC	Interrupt masked. See IPC_INTR_STRUCT0_INTR_MASKED for the details of bit fields.
IPC_INTR_STRUCT8_INTR	0x40231100	Interrupt. See IPC_INTR_STRUCT0_INTR for the details of bit fields.
IPC_INTR_STRUCT8_INTR_SET	0x40231104	Interrupt set. See IPC_INTR_STRUCT0_INTR_SET for the details of bit fields.
IPC_INTR_STRUCT8_INTR_MASK	0x40231108	Interrupt mask. See IPC_INTR_STRUCT0_INTR_MASK for the details of bit fields.
IPC_INTR_STRUCT8_INTR_MASKED	0x4023110C	Interrupt masked. See IPC_INTR_STRUCT0_INTR_MASKED for the details of bit fields.
IPC_INTR_STRUCT9_INTR	0x40231120	Interrupt. See IPC_INTR_STRUCT0_INTR for the details of bit fields.
IPC_INTR_STRUCT9_INTR_SET	0x40231124	Interrupt set. See IPC_INTR_STRUCT0_INTR_SET for the details of bit fields.
IPC_INTR_STRUCT9_INTR_MASK	0x40231128	Interrupt mask. See IPC_INTR_STRUCT0_INTR_MASK for the details of bit fields.
IPC_INTR_STRUCT9_INTR_MASKED	0x4023112C	Interrupt masked. See IPC_INTR_STRUCT0_INTR_MASKED for the details of bit fields.
IPC_INTR_STRUCT10_INTR	0x40231140	Interrupt. See IPC_INTR_STRUCT0_INTR for the details of bit fields.
IPC_INTR_STRUCT10_INTR_SET	0x40231144	Interrupt set. See IPC_INTR_STRUCT0_INTR_SET for the details of bit fields.
IPC_INTR_STRUCT10_INTR_MASK	0x40231148	Interrupt mask. See IPC_INTR_STRUCT0_INTR_MASK for the details of bit fields.
IPC_INTR_STRUCT10_INTR_MASKED	0x4023114C	Interrupt masked. See IPC_INTR_STRUCT0_INTR_MASKED for the details of bit fields.
IPC_INTR_STRUCT11_INTR	0x40231160	Interrupt. See IPC_INTR_STRUCT0_INTR for the details of bit fields.
IPC_INTR_STRUCT11_INTR_SET	0x40231164	Interrupt set. See IPC_INTR_STRUCT0_INTR_SET for the details of bit fields.
IPC_INTR_STRUCT11_INTR_MASK	0x40231168	Interrupt mask. See IPC_INTR_STRUCT0_INTR_MASK for the details of bit fields.
IPC_INTR_STRUCT11_INTR_MASKED	0x4023116C	Interrupt masked. See IPC_INTR_STRUCT0_INTR_MASKED for the details of bit fields.
IPC_INTR_STRUCT12_INTR	0x40231180	Interrupt. See IPC_INTR_STRUCT0_INTR for the details of bit fields.
IPC_INTR_STRUCT12_INTR_SET	0x40231184	Interrupt set. See IPC_INTR_STRUCT0_INTR_SET for the details of bit fields.
IPC_INTR_STRUCT12_INTR_MASK	0x40231188	Interrupt mask. See IPC_INTR_STRUCT0_INTR_MASK for the details of bit fields.
IPC_INTR_STRUCT12_INTR_MASKED	0x4023118C	Interrupt masked. See IPC_INTR_STRUCT0_INTR_MASKED for the details of bit fields.
IPC_INTR_STRUCT13_INTR	0x402311A0	Interrupt. See IPC_INTR_STRUCT0_INTR for the details of bit fields.
IPC_INTR_STRUCT13_INTR_SET	0x402311A4	Interrupt set. See IPC_INTR_STRUCT0_INTR_SET for the details of bit fields.
IPC_INTR_STRUCT13_INTR_MASK	0x402311A8	Interrupt mask. See IPC_INTR_STRUCT0_INTR_MASK for the details of bit fields.
IPC_INTR_STRUCT13_INTR_MASKED	0x402311AC	Interrupt masked. See IPC_INTR_STRUCT0_INTR_MASKED for the details of bit fields.
IPC_INTR_STRUCT14_INTR	0x402311C0	Interrupt. See IPC_INTR_STRUCT0_INTR for the details of bit fields.
IPC_INTR_STRUCT14_INTR_SET	0x402311C4	Interrupt set. See IPC_INTR_STRUCT0_INTR_SET for the details of bit fields.
IPC_INTR_STRUCT14_INTR_MASK	0x402311C8	Interrupt mask. See IPC_INTR_STRUCT0_INTR_MASK for the details of bit fields.
IPC_INTR_STRUCT14_INTR_MASKED	0x402311CC	Interrupt masked. See IPC_INTR_STRUCT0_INTR_MASKED for the details of bit fields.
IPC_INTR_STRUCT15_INTR	0x402311E0	Interrupt. See IPC_INTR_STRUCT0_INTR for the details of bit fields.
IPC_INTR_STRUCT15_INTR_SET	0x402311E4	Interrupt set. See IPC_INTR_STRUCT0_INTR_SET for the details of bit fields.
IPC_INTR_STRUCT15_INTR_MASK	0x402311E8	Interrupt mask. See IPC_INTR_STRUCT0_INTR_MASK for the details of bit fields.
IPC_INTR_STRUCT15_INTR_MASKED	0x402311EC	Interrupt masked. See IPC_INTR_STRUCT0_INTR_MASKED for the details of bit fields.

6.1.1 IPC_STRUCT0_ACQUIRE

IPC acquire

Address: 0x40230000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				None		R	R
HW Access	W				None		W	W
Name	PC [7:4]				None [3:2]		NS	P

Bits	15	14	13	12	11	10	9	8
SW Access	None				R			
HW Access	None				W			
Name	None [15:12]				MS [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	RW	None						
Name	SUCCESS	None [30:24]						

Bits	Name	Description
31	SUCCESS	Specifies if the lock is successfully acquired or not (reading the ACQUIRE register can have affect on SUCCESS and LOCK_STATUS.ACQUIRED): '0': Not successfully acquired; i.e. the lock was already acquired by another read transaction and not released. The P, NS, PC and MS fields reflect the access attributes of the transaction that previously successfully acuired the lock; the fields are NOT affected by the current access. '1': Successfully acquired. The P, NS, PC and MS fields reflect the access attributes of the current access. Note that this field is NOT SW writable. A lock is released by writing to the associated RELEASE register (irrespective of the write value). Default Value: 0
11 : 8	MS	This field specifies the bus master identifier that successfully acquired the lock. Default Value: Undefined
7 : 4	PC	This field specifies the protection context that successfully acquired the lock. Default Value: Undefined

6.1.1 IPC_STRUCT0_ACQUIRE (continued)

1	NS	Secure/on-secure access control: '0': secure. '1': non-secure. This field is set with the secure/non-secure access control of the access that successfully acquired the lock. Default Value: Undefined
0	P	User/privileged access control: '0': user mode. '1': privileged mode. This field is set with the user/privileged access control of the access that successfully acquired the lock. Default Value: Undefined

6.1.2 IPC_STRUCT0_RELEASE

IPC release

Address: 0x40230004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access								
Name	INTR_RELEASE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access								
Name	INTR_RELEASE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	INTR_RELEASE	This field allows for the generation of release events to the IPC interrupt structures, but only when the lock is acquired (LOCK_STATUS.ACQUIRED is '1'). The IPC release cause fields associated with this IPC structure are set to '1', but only for those IPC interrupt structures for which the corresponding bit field in INTR_RELEASE[] is set to '1'. SW writes a '1' to the bit fields to generate a release event. Due to the transient nature of this event, SW always reads a '0' from this field. As a side effect, a write to this register will always set LOCK_STATUS.ACQUIRED to '0' (even when no release event is generated; i.e. the written data is "0"). Default Value: 0

6.1.3 IPC_STRUCT0_NOTIFY

IPC notification

Address: 0x40230008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access								
Name	INTR_NOTIFY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access								
Name	INTR_NOTIFY [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	INTR_NOTIFY	This field allows for the generation of notification events to the IPC interrupt structures. The IPC notification cause fields associated with this IPC structure are set to '1', but only for those IPC interrupt structures for which the corresponding bit field in INTR_NOTIFY[] is set to '1'. SW writes a '1' to the bit fields to generate a notify event. Due to the transient nature of this event, SW always reads a '0' from this field. Default Value: 0

6.1.4 IPC_STRUCT0_DATA

IPC data

Address: 0x4023000C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	This field holds a 32-bit data element that is associated with the IPC structure. Default Value: Undefined

6.1.5 IPC_STRUCT0_LOCK_STATUS

IPC lock status

Address: 0x40230010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				None		R	R
HW Access	W				None		W	W
Name	PC [7:4]				None [3:2]		NS	P

Bits	15	14	13	12	11	10	9	8
SW Access	None				R			
HW Access	None				W			
Name	None [15:12]				MS [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	R	None						
Name	ACQUIRED	None [30:24]						

Bits	Name	Description
31	ACQUIRED	Specifies if the lock is acquired. This field is set to '1', if a ACQUIRE read transfer successfully acquires the lock (the ACQUIRE read transfer returns ACQUIRE.SUCCESS as '1'). Default Value: 0
11 : 8	MS	This field specifies the bus master identifier that successfully acquired the lock. Default Value: Undefined
7 : 4	PC	This field specifies the protection context that successfully acquired the lock. Default Value: Undefined
1	NS	This field specifies the cecure/on-secure access control: '0': secure. '1': non-secure. Default Value: Undefined
0	P	This field specifies the user/privileged access control: '0': user mode. '1': privileged mode. Default Value: Undefined

6.1.6 IPC_INTR_STRUCT0_INTR

Interrupt

Address: 0x40231000

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C							
HW Access	RW1S							
Name	RELEASE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1C							
HW Access	RW1S							
Name	RELEASE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW1C							
HW Access	RW1S							
Name	NOTIFY [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1C							
HW Access	RW1S							
Name	NOTIFY [31:24]							

Bits	Name	Description
31 : 16	NOTIFY	These interrupt cause fields are activated (HW sets the field to '1') when a IPC notification event is detected. One bit field for each master. SW writes a '1' to these field to clear the interrupt cause. Default Value: 0
15 : 0	RELEASE	These interrupt cause fields are activated (HW sets the field to '1') when a IPC release event is detected. One bit field for each master. SW writes a '1' to these field to clear the interrupt cause. Default Value: 0

6.1.7 IPC_INTR_STRUCT0_INTR_SET

Interrupt set

Address: 0x40231004

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S							
HW Access	A							
Name	RELEASE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1S							
HW Access	A							
Name	RELEASE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW1S							
HW Access	A							
Name	NOTIFY [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1S							
HW Access	A							
Name	NOTIFY [31:24]							

Bits	Name	Description
31 : 16	NOTIFY	SW writes a '1' to this field to set the corresponding field in the INTR register. Default Value: 0
15 : 0	RELEASE	SW writes a '1' to this field to set the corresponding field in the INTR register. Default Value: 0

6.1.8 IPC_INTR_STRUCT0_INTR_MASK

Interrupt mask

Address: 0x40231008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	RELEASE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	RELEASE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	NOTIFY [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	NOTIFY [31:24]							

Bits	Name	Description
31 : 16	NOTIFY	Mask bit for corresponding field in the INTR register. Default Value: 0
15 : 0	RELEASE	Mask bit for corresponding field in the INTR register. Default Value: 0

6.1.9 IPC_INTR_STRUCT0_INTR_MASKED

Interrupt masked

Address: 0x4023100C

Retention: Not Retained

Bits	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SW Access	R							
HW Access	W							
Name	RELEASE [7:0]							

Bits	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SW Access	R							
HW Access	W							
Name	RELEASE [15:8]							

Bits	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SW Access	R							
HW Access	W							
Name	NOTIFY [23:16]							

Bits	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**
SW Access	R							
HW Access	W							
Name	NOTIFY [31:24]							

Bits	**Name**	**Description**
31 : 16	NOTIFY	Logical and of corresponding INTR and INTR_MASK fields. Default Value: 0
15 : 0	RELEASE	Logical and of corresponding request and mask bits. Default Value: 0

7 Protection Unit Registers

This section discusses the Protection Unit registers. It lists all the registers in mapping tables, in address order.

7.1 Register Details

Register	Address	Description
PROT_SMPU_MS0_CTL	0x40240000	Master 0 protection context control
PROT_SMPU_MS1_CTL	0x40240004	Master 1 protection context control
PROT_SMPU_MS2_CTL	0x40240008	Master 2 protection context control
PROT_SMPU_MS3_CTL	0x4024000C	Master 3 protection context control
PROT_SMPU_MS14_CTL	0x40240038	Master 14 protection context control
PROT_SMPU_MS15_CTL	0x4024003C	Master 15 protection context control
PROT_SMPU_SMPU_STRUCT0_ADDR0	0x40242000	SMPU region address 0 (slave structure)
PROT_SMPU_SMPU_STRUCT0_ATT0	0x40242004	SMPU region attributes 0 (slave structure)
PROT_SMPU_SMPU_STRUCT0_ADDR1	0x40242020	SMPU region address 1 (master structure)
PROT_SMPU_SMPU_STRUCT0_ATT1	0x40242024	SMPU region attributes 1 (master structure)
PROT_SMPU_SMPU_STRUCT1_ADDR0	0x40242040	SMPU region address 0 (slave structure). See PROT_SMPU_SMPU_STRUCT0_ADDR0 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT1_ATT0	0x40242044	SMPU region attributes 0 (slave structure). See PROT_SMPU_SMPU_STRUCT0_ATT0 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT1_ADDR1	0x40242060	SMPU region address 1 (master structure)
PROT_SMPU_SMPU_STRUCT1_ATT1	0x40242064	SMPU region attributes 1 (master structure). See PROT_SMPU_SMPU_STRUCT0_ATT1 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT2_ADDR0	0x40242080	SMPU region address 0 (slave structure). See PROT_SMPU_SMPU_STRUCT0_ADDR0 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT2_ATT0	0x40242084	SMPU region attributes 0 (slave structure). See PROT_SMPU_SMPU_STRUCT0_ATT0 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT2_ADDR1	0x402420A0	SMPU region address 1 (master structure)
PROT_SMPU_SMPU_STRUCT2_ATT1	0x402420A4	SMPU region attributes 1 (master structure). See PROT_SMPU_SMPU_STRUCT0_ATT1 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT3_ADDR0	0x402420C0	SMPU region address 0 (slave structure). See PROT_SMPU_SMPU_STRUCT0_ADDR0 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT3_ATT0	0x402420C4	SMPU region attributes 0 (slave structure). See PROT_SMPU_SMPU_STRUCT0_ATT0 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT3_ADDR1	0x402420E0	SMPU region address 1 (master structure)
PROT_SMPU_SMPU_STRUCT3_ATT1	0x402420E4	SMPU region attributes 1 (master structure). See PROT_SMPU_SMPU_STRUCT0_ATT1 for the details of bit fields.

Register	Address	Description
PROT_SMPU_SMPU_STRUCT4_ADDR0	0x40242100	SMPU region address 0 (slave structure). See PROT_SMPU_SMPU_STRUCT0_ADDR0 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT4_ATT0	0x40242104	SMPU region attributes 0 (slave structure). See PROT_SMPU_SMPU_STRUCT0_ATT0 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT4_ADDR1	0x40242120	SMPU region address 1 (master structure)
PROT_SMPU_SMPU_STRUCT4_ATT1	0x40242124	SMPU region attributes 1 (master structure). See PROT_SMPU_SMPU_STRUCT0_ATT1 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT5_ADDR0	0x40242140	SMPU region address 0 (slave structure). See PROT_SMPU_SMPU_STRUCT0_ADDR0 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT5_ATT0	0x40242144	SMPU region attributes 0 (slave structure). See PROT_SMPU_SMPU_STRUCT0_ATT0 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT5_ADDR1	0x40242160	SMPU region address 1 (master structure)
PROT_SMPU_SMPU_STRUCT5_ATT1	0x40242164	SMPU region attributes 1 (master structure). See PROT_SMPU_SMPU_STRUCT0_ATT1 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT6_ADDR0	0x40242180	SMPU region address 0 (slave structure). See PROT_SMPU_SMPU_STRUCT0_ADDR0 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT6_ATT0	0x40242184	SMPU region attributes 0 (slave structure). See PROT_SMPU_SMPU_STRUCT0_ATT0 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT6_ADDR1	0x402421A0	SMPU region address 1 (master structure)
PROT_SMPU_SMPU_STRUCT6_ATT1	0x402421A4	SMPU region attributes 1 (master structure). See PROT_SMPU_SMPU_STRUCT0_ATT1 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT7_ADDR0	0x402421C0	SMPU region address 0 (slave structure). See PROT_SMPU_SMPU_STRUCT0_ADDR0 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT7_ATT0	0x402421C4	SMPU region attributes 0 (slave structure). See PROT_SMPU_SMPU_STRUCT0_ATT0 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT7_ADDR1	0x402421E0	SMPU region address 1 (master structure)
PROT_SMPU_SMPU_STRUCT7_ATT1	0x402421E4	SMPU region attributes 1 (master structure). See PROT_SMPU_SMPU_STRUCT0_ATT1 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT8_ADDR0	0x40242200	SMPU region address 0 (slave structure). See PROT_SMPU_SMPU_STRUCT0_ADDR0 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT8_ATT0	0x40242204	SMPU region attributes 0 (slave structure). See PROT_SMPU_SMPU_STRUCT0_ATT0 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT8_ADDR1	0x40242220	SMPU region address 1 (master structure)
PROT_SMPU_SMPU_STRUCT8_ATT1	0x40242224	SMPU region attributes 1 (master structure). See PROT_SMPU_SMPU_STRUCT0_ATT1 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT9_ADDR0	0x40242240	SMPU region address 0 (slave structure). See PROT_SMPU_SMPU_STRUCT0_ADDR0 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT9_ATT0	0x40242244	SMPU region attributes 0 (slave structure). See PROT_SMPU_SMPU_STRUCT0_ATT0 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT9_ADDR1	0x40242260	SMPU region address 1 (master structure)
PROT_SMPU_SMPU_STRUCT9_ATT1	0x40242264	SMPU region attributes 1 (master structure). See PROT_SMPU_SMPU_STRUCT0_ATT1 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT10_ADDR0	0x40242280	SMPU region address 0 (slave structure). See PROT_SMPU_SMPU_STRUCT0_ADDR0 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT10_ATT0	0x40242284	SMPU region attributes 0 (slave structure). See PROT_SMPU_SMPU_STRUCT0_ATT0 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT10_ADDR1	0x402422A0	SMPU region address 1 (master structure)
PROT_SMPU_SMPU_STRUCT10_ATT1	0x402422A4	SMPU region attributes 1 (master structure). See PROT_SMPU_SMPU_STRUCT0_ATT1 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT11_ADDR0	0x402422C0	SMPU region address 0 (slave structure). See PROT_SMPU_SMPU_STRUCT0_ADDR0 for the details of bit fields.

Register	Address	Description
PROT_SMPU_SMPU_STRUCT11_ATT0	0x402422C4	SMPU region attributes 0 (slave structure). See PROT_SMPU_SMPU_STRUCT0_ATT0 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT11_ADDR1	0x402422E0	SMPU region address 1 (master structure)
PROT_SMPU_SMPU_STRUCT11_ATT1	0x402422E4	SMPU region attributes 1 (master structure). See PROT_SMPU_SMPU_STRUCT0_ATT1 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT12_ADDR0	0x40242300	SMPU region address 0 (slave structure). See PROT_SMPU_SMPU_STRUCT0_ADDR0 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT12_ATT0	0x40242304	SMPU region attributes 0 (slave structure). See PROT_SMPU_SMPU_STRUCT0_ATT0 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT12_ADDR1	0x40242320	SMPU region address 1 (master structure)
PROT_SMPU_SMPU_STRUCT12_ATT1	0x40242324	SMPU region attributes 1 (master structure). See PROT_SMPU_SMPU_STRUCT0_ATT1 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT13_ADDR0	0x40242340	SMPU region address 0 (slave structure). See PROT_SMPU_SMPU_STRUCT0_ADDR0 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT13_ATT0	0x40242344	SMPU region attributes 0 (slave structure). See PROT_SMPU_SMPU_STRUCT0_ATT0 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT13_ADDR1	0x40242360	SMPU region address 1 (master structure)
PROT_SMPU_SMPU_STRUCT13_ATT1	0x40242364	SMPU region attributes 1 (master structure). See PROT_SMPU_SMPU_STRUCT0_ATT1 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT14_ADDR0	0x40242380	SMPU region address 0 (slave structure). See PROT_SMPU_SMPU_STRUCT0_ADDR0 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT14_ATT0	0x40242384	SMPU region attributes 0 (slave structure). See PROT_SMPU_SMPU_STRUCT0_ATT0 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT14_ADDR1	0x402423A0	SMPU region address 1 (master structure)
PROT_SMPU_SMPU_STRUCT14_ATT1	0x402423A4	SMPU region attributes 1 (master structure). See PROT_SMPU_SMPU_STRUCT0_ATT1 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT15_ADDR0	0x402423C0	SMPU region address 0 (slave structure). See PROT_SMPU_SMPU_STRUCT0_ADDR0 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT15_ATT0	0x402423C4	SMPU region attributes 0 (slave structure). See PROT_SMPU_SMPU_STRUCT0_ATT0 for the details of bit fields.
PROT_SMPU_SMPU_STRUCT15_ADDR1	0x402423E0	SMPU region address 1 (master structure)
PROT_SMPU_SMPU_STRUCT15_ATT1	0x402423E4	SMPU region attributes 1 (master structure). See PROT_SMPU_SMPU_STRUCT0_ATT1 for the details of bit fields.
PROT_MPU0_MS_CTL	0x40244000	Master control
PROT_MPU1_MS_CTL	0x40244400	Master control
PROT_MPU1_MPU_STRUCT0_ADDR	0x40244600	MPU region address
PROT_MPU1_MPU_STRUCT0_ATT	0x40244604	MPU region attributes
PROT_MPU1_MPU_STRUCT1_ADDR	0x40244620	MPU region address. See PROT_MPU1_MPU_STRUCT0_ADDR for the details of bit fields.
PROT_MPU1_MPU_STRUCT1_ATT	0x40244624	MPU region attributes. See PROT_MPU1_MPU_STRUCT0_ATT for the details of bit fields.
PROT_MPU1_MPU_STRUCT2_ADDR	0x40244640	MPU region address. See PROT_MPU1_MPU_STRUCT0_ADDR for the details of bit fields.
PROT_MPU1_MPU_STRUCT2_ATT	0x40244644	MPU region attributes. See PROT_MPU1_MPU_STRUCT0_ATT for the details of bit fields.
PROT_MPU1_MPU_STRUCT3_ADDR	0x40244660	MPU region address. See PROT_MPU1_MPU_STRUCT0_ADDR for the details of bit fields.
PROT_MPU1_MPU_STRUCT3_ATT	0x40244664	MPU region attributes. See PROT_MPU1_MPU_STRUCT0_ATT for the details of bit fields.
PROT_MPU1_MPU_STRUCT4_ADDR	0x40244680	MPU region address. See PROT_MPU1_MPU_STRUCT0_ADDR for the details of bit fields.
PROT_MPU1_MPU_STRUCT4_ATT	0x40244684	MPU region attributes. See PROT_MPU1_MPU_STRUCT0_ATT for the details of bit fields.
PROT_MPU1_MPU_STRUCT5_ADDR	0x402446A0	MPU region address. See PROT_MPU1_MPU_STRUCT0_ADDR for the details of bit fields.
PROT_MPU1_MPU_STRUCT5_ATT	0x402446A4	MPU region attributes. See PROT_MPU1_MPU_STRUCT0_ATT for the details of bit fields.
PROT_MPU1_MPU_STRUCT6_ADDR	0x402446C0	MPU region address. See PROT_MPU1_MPU_STRUCT0_ADDR for the details of bit fields.

Register	Address	Description
PROT_MPU1_MPU_STRUCT6_ATT	0x402446C4	MPU region attributes. See PROT_MPU1_MPU_STRUCT0_ATT for the details of bit fields.
PROT_MPU1_MPU_STRUCT7_ADDR	0x402446E0	MPU region address. See PROT_MPU1_MPU_STRUCT0_ADDR for the details of bit fields.
PROT_MPU1_MPU_STRUCT7_ATT	0x402446E4	MPU region attributes. See PROT_MPU1_MPU_STRUCT0_ATT for the details of bit fields.
PROT_MPU14_MS_CTL	0x40247800	Master control. See PROT_MPU1_MS_CTL for the details of bit fields.
PROT_MPU15_MS_CTL	0x40247C00	Master control. See PROT_MPU1_MS_CTL for the details of bit fields.
PROT_MPU15_MPU_STRUCT0_ADDR	0x40247E00	MPU region address. See PROT_MPU1_MPU_STRUCT0_ADDR for the details of bit fields.
PROT_MPU15_MPU_STRUCT0_ATT	0x40247E04	MPU region attributes. See PROT_MPU1_MPU_STRUCT0_ATT for the details of bit fields.
PROT_MPU15_MPU_STRUCT1_ADDR	0x40247E20	MPU region address. See PROT_MPU1_MPU_STRUCT0_ADDR for the details of bit fields.
PROT_MPU15_MPU_STRUCT1_ATT	0x40247E24	MPU region attributes. See PROT_MPU1_MPU_STRUCT0_ATT for the details of bit fields.
PROT_MPU15_MPU_STRUCT2_ADDR	0x40247E40	MPU region address. See PROT_MPU1_MPU_STRUCT0_ADDR for the details of bit fields.
PROT_MPU15_MPU_STRUCT2_ATT	0x40247E44	MPU region attributes. See PROT_MPU1_MPU_STRUCT0_ATT for the details of bit fields.
PROT_MPU15_MPU_STRUCT3_ADDR	0x40247E60	MPU region address. See PROT_MPU1_MPU_STRUCT0_ADDR for the details of bit fields.
PROT_MPU15_MPU_STRUCT3_ATT	0x40247E64	MPU region attributes. See PROT_MPU1_MPU_STRUCT0_ATT for the details of bit fields.
PROT_MPU15_MPU_STRUCT4_ADDR	0x40247E80	MPU region address. See PROT_MPU1_MPU_STRUCT0_ADDR for the details of bit fields.
PROT_MPU15_MPU_STRUCT4_ATT	0x40247E84	MPU region attributes. See PROT_MPU1_MPU_STRUCT0_ATT for the details of bit fields.
PROT_MPU15_MPU_STRUCT5_ADDR	0x40247EA0	MPU region address. See PROT_MPU1_MPU_STRUCT0_ADDR for the details of bit fields.
PROT_MPU15_MPU_STRUCT5_ATT	0x40247EA4	MPU region attributes. See PROT_MPU1_MPU_STRUCT0_ATT for the details of bit fields.
PROT_MPU15_MPU_STRUCT6_ADDR	0x40247EC0	MPU region address. See PROT_MPU1_MPU_STRUCT0_ADDR for the details of bit fields.
PROT_MPU15_MPU_STRUCT6_ATT	0x40247EC4	MPU region attributes. See PROT_MPU1_MPU_STRUCT0_ATT for the details of bit fields.
PROT_MPU15_MPU_STRUCT7_ADDR	0x40247EE0	MPU region address. See PROT_MPU1_MPU_STRUCT0_ADDR for the details of bit fields.
PROT_MPU15_MPU_STRUCT7_ATT	0x40247EE4	MPU region attributes. See PROT_MPU1_MPU_STRUCT0_ATT for the details of bit fields.

7.1.1 PROT_SMPU_MS0_CTL

Master 0 protection context control

Address: 0x40240000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						NS	P

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						PRIO [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	RW							R
HW Access	R							R
Name	PC_MASK_15_TO_1 [23:17]							PC_MASK_0

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 17	PC_MASK_15_TO_1	Protection context mask for protection contexts "15" down to "1". Bit PC_MASK_15_TO_1[i] indicates if the MPU MS_CTL.PC[3:0] protection context field can be set to the value "i+1": - PC_MASK_15_TO_1[i] is '0': MPU MS_CTL.PC[3:0] can NOT be set to "i+1"; and PC[3:0] is not changed. If the protection context of the write transfer is "0", protection is not applied and PC[3:0] can be changed. - PC_MASK_15_TO_1[i] is '1': MPU MS_CTL.PC[3:0] can be set to "i+1". Note: When CPUSS_CM0_PC_CTL.VALID[i] is '1' (the associated protection context handler is valid), write transfers to PC_MASK_15_TO_1[i-1] always write '0', regardless of data written. This ensures that when valid protection context handlers are used to enter protection contexts 1, 2 or 3 through (HW modifies MPU MS_CTL.PC[3:0] on entry of the handler), it is NOT possible for SW to enter those protection contexts (SW modifies MPU MS_CTL.PC[3:0]). Default Value: 0
16	PC_MASK_0	Protection context mask for protection context "0". This field is a constant '0': - PC_MASK_0 is '0': MPU MS_CTL.PC[3:0] can NOT be set to "0" and PC[3:0] is not changed. If the protection context of the write transfer is "0", protection is not applied and PC[3:0] can be changed. Default Value: 0

7.1.1 PROT_SMPU_MS0_CTL (continued)

9 : 8	PRIO	Device wide bus arbitration priority setting ("0": highest priority, "3": lowest priority). Notes: The AHB-Lite interconnect performs arbitration on the individual beats/transfers of a burst (this optimizes latency over locality/bandwidth). The AXI-Lite interconnects performs a single arbitration for the complete burst (this optimizes locality/bandwidth over latency). Masters with the same priority setting form a "priority group". Within a "priority group", round robin arbitration is performed. Default Value: 3
1	NS	Security setting ('0': secure mode; '1': non-secure mode). Notes: This field is ONLY used for masters that do NOT provide their own secure/non-secure access control attribute. Note that the default/reset field value provides non-secure mode access capabilities to all masters. Default Value: 1
0	P	Privileged setting ('0': user mode; '1': privileged mode). Notes: This field is ONLY used for masters that do NOT provide their own user/privileged access control attribute. The default/reset field value provides privileged mode access capabilities. Default Value: 1

7.1.2 PROT_SMPU_MS1_CTL

Master 1 protection context control

Address: 0x40240004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						NS	P

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						PRIO [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	RW							R
HW Access	R							R
Name	PC_MASK_15_TO_1 [23:17]							PC_MASK_0

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 17	PC_MASK_15_TO_1	See MS0_CTL.PC_MASK_15_TO_1. Default Value: 0
16	PC_MASK_0	See MS0_CTL.PC_MASK_0. Default Value: 0
9 : 8	PRIO	See MS0_CTL.PRIO Default Value: 3
1	NS	See MS0_CTL.NS. Default Value: 1
0	P	See MS0_CTL.P. Default Value: 1

7.1.3 PROT_SMPU_MS2_CTL

Master 2 protection context control

Address: 0x40240008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						PRIO [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							R
HW Access	None							R
Name	None [23:17]							PC_MASK_0

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
16	PC_MASK_0	See MS0_CTL.PC_MASK_0. Default Value: 0
9 : 8	PRIO	See MS0_CTL.PRIO Default Value: 3

7.1.4 PROT_SMPU_MS3_CTL

Master 3 protection context control

Address: 0x4024000C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						PRIO [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							R
HW Access	None							R
Name	None [23:17]							PC_MASK_0

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
16	PC_MASK_0	See MS0_CTL.PC_MASK_0. Default Value: 0
9 : 8	PRIO	See MS0_CTL.PRIO Default Value: 3

7.1.5 PROT_SMPU_MS14_CTL

Master 14 protection context control

Address: 0x40240038

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						NS	P

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						PRIO [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	RW							R
HW Access	R							R
Name	PC_MASK_15_TO_1 [23:17]							PC_MASK_0

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 17	PC_MASK_15_TO_1	See MS0_CTL.PC_MASK_15_TO_1. Default Value: 0
16	PC_MASK_0	See MS0_CTL.PC_MASK_0. Default Value: 0
9 : 8	PRIO	See MS0_CTL.PRIO Default Value: 3
1	NS	See MS0_CTL.NS. Default Value: 1
0	P	See MS0_CTL.P. Default Value: 1

7.1.6 PROT_SMPU_MS15_CTL

Master 15 protection context control

Address: 0x4024003C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						NS	P

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						PRIO [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	RW							R
HW Access	R							R
Name	PC_MASK_15_TO_1 [23:17]							PC_MASK_0

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 17	PC_MASK_15_TO_1	See MS0_CTL.PC_MASK_15_TO_1. Default Value: 0
16	PC_MASK_0	See MS0_CTL.PC_MASK_0. Default Value: 0
9 : 8	PRIO	See MS0_CTL.PRIO Default Value: 3
1	NS	See MS0_CTL.NS. Default Value: 1
0	P	See MS0_CTL.P. Default Value: 1

7.1.7 PROT_SMPU_SMPU_STRUCT0_ADDR0

SMPU region address 0 (slave structure)

Address: 0x40242000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	This field specifies the most significant bits of the 32-bit address of an address region. The region size is defined by ATT0.REGION_SIZE. A region of n Byte is always n Byte aligned. As a result, some of the lesser significant address bits of ADDR24 may be ignored in determining whether a bus transfer address is within an address region. E.g., a 64 KByte address region (REGION_-SIZE is "15") is 64 KByte aligned, and ADDR24[7:0] are ignored. Default Value: Undefined

7.1.7 PROT_SMPU_SMPU_STRUCT0_ADDR0 (continued)

7 : 0	SUBREGION_DISABLE	This field is used to individually disabled the eight equally sized subregions in which a region is partitioned. Subregion disable: Bit 0: subregion 0 disable. Bit 1: subregion 1 disable. Bit 2: subregion 2 disable. Bit 3: subregion 3 disable. Bit 4: subregion 4 disable. Bit 5: subregion 5 disable. Bit 6: subregion 6 disable. Bit 7: subregion 7 disable. E.g., a 64 KByte address region (ATT0.REGION_SIZE is "15") has eight 8 KByte subregions. The access control as defined by ATT0 applies if the bus transfer address is within the address region AND the addressed subregion is NOT disabled. Note that the smallest region size is 256 B and the smallest subregion size is 32 B. Default Value: Undefined

7.1.8 PROT_SMPU_SMPU_STRUCT0_ATT0

SMPU region attributes 0 (slave structure)

Address: 0x40242004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	RW	RW	RW	RW	RW	RW
HW Access	None	R	R	R	R	R	R	R
Name	None	NS	PX	PW	PR	UX	UW	UR

Bits	15	14	13	12	11	10	9	8
SW Access	RW							R
HW Access	R							R
Name	PC_MASK_15_TO_1 [15:9]							PC_MASK_0

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None	RW				
HW Access	R	R	None	R				
Name	ENABLED	PC_MATCH	None	REGION_SIZE [28:24]				

Bits	Name	Description
31	ENABLED	Region enable: '0': Disabled. A disabled region will never result in a match on the bus transfer address. '1': Enabled. Note: a disabled address region performs logic gating to reduce dynamic power consumption. Default Value: 0
30	PC_MATCH	This field specifies if the PC field participates in the "matching" process or the "access evaluation" process: '0': PC field participates in "access evaluation". '1': PC field participates in "matching". Note that it is possible to define different access control for multiple protection contexts by using multiple protection structures with the same address region and PC_MATCH set to '1'. Default Value: Undefined

7.1.8 PROT_SMPU_SMPU_STRUCT0_ATT0 (continued)

28 : 24	REGION_SIZE	This field specifies the region size: "0"-"6": Undefined. "7": 256 B region "8": 512 B region "9": 1 KB region "10": 2 KB region "11": 4 KB region "12": 8 KB region "13": 16 KB region "14": 32 KB region "15": 64 KB region "16": 128 KB region "17": 256 KB region "18": 512 KB region "19": 1 MB region "20": 2 MB region "21": 4 MB region "22": 8 MB region "23": 16 MB region "24": 32 MB region "25": 64 MB region "26": 128 MB region "27": 256 MB region "28": 512 MB region "39": 1 GB region "30": 2 GB region "31": 4 GB region Default Value: Undefined
15 : 9	PC_MASK_15_TO_1	This field specifies protection context identifier based access control. Bit i: protection context i+1 enable. If '0', protection context i+1 access is disabled; i.e. not allowed. If '1', protection context i+1 access is enabled; i.e. allowed. Default Value: Undefined
8	PC_MASK_0	This field specifies protection context identifier based access control for protection context "0". Default Value: 1
6	NS	Non-secure: '0': Secure (secure accesses allowed, non-secure access NOT allowed). '1': Non-secure (both secure and non-secure accesses allowed). Default Value: Undefined
5	PX	Privileged execute enable: '0': Disabled (privileged, execute accesses are NOT allowed). '1': Enabled (privileged, execute accesses are allowed). Default Value: Undefined
4	PW	Privileged write enable: '0': Disabled (privileged, write accesses are NOT allowed). '1': Enabled (privileged, write accesses are allowed). Default Value: Undefined
3	PR	Privileged read enable: '0': Disabled (privileged, read accesses are NOT allowed). '1': Enabled (privileged, read accesses are allowed). Default Value: Undefined
2	UX	User execute enable: '0': Disabled (user, execute accesses are NOT allowed). '1': Enabled (user, execute accesses are allowed). Default Value: Undefined

7.1.8 PROT_SMPU_SMPU_STRUCT0_ATT0 (continued)

1	UW	User write enable: '0': Disabled (user, write accesses are NOT allowed). '1': Enabled (user, write accesses are allowed). Default Value: Undefined
0	UR	User read enable: '0': Disabled (user, read accesses are NOT allowed). '1': Enabled (user, read accesses are allowed). Default Value: Undefined

7.1.9 PROT_SMPU_SMPU_STRUCT0_ADDR1

SMPU region address 1 (master structure)

Address: 0x40242020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	This field specifies the most significant bits of the 32-bit address of an address region. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4203552
7 : 0	SUBREGION_DISABLE	This field is used to individually disabled the eight equally sized subregions in which a region is partitioned. Subregion disable: Bit 0: subregion 0 disable. Bit 1: subregion 1 disable. Bit 2: subregion 2 disable. Bit 3: subregion 3 disable. Bit 4: subregion 4 disable. Bit 5: subregion 5 disable. Bit 6: subregion 6 disable. Bit 7: subregion 7 disable. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 252

7.1.10 PROT_SMPU_SMPU_STRUCT0_ATT1

SMPU region attributes 1 (master structure)

Address: 0x40242024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	R	RW	R	R	RW	R
HW Access	None	R	R	R	R	R	R	R
Name	None	NS	PX	PW	PR	UX	UW	UR

Bits	15	14	13	12	11	10	9	8
SW Access	RW							R
HW Access	R							R
Name	PC_MASK_15_TO_1 [15:9]							PC_MASK_0

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None	R				
HW Access	R	R	None	R				
Name	ENABLED	PC_MATCH	None	REGION_SIZE [28:24]				

Bits	Name	Description
31	ENABLED	Region enable: '0': Disabled. A disabled region will never result in a match on the bus transfer address. '1': Enabled. Default Value: 0
30	PC_MATCH	This field specifies if the PC field participates in the "matching" process or the "access evaluation" process: '0': PC field participates in "access evaluation". '1': PC field participates in "matching". Note that it is possible to define different access control for multiple protection contexts by using multiple protection structures with the same address region and PC_MATCH set to '1'. Default Value: Undefined
28 : 24	REGION_SIZE	This field specifies the region size: "7": 256 B region (8 32 B subregions) Note: this field is read-only. Default Value: 7

7.1.10 PROT_SMPU_SMPU_STRUCT0_ATT1 (continued)

15 : 9	PC_MASK_15_TO_1	This field specifies protection context identifier based access control. Bit i: protection context i+1 enable. If '0', protection context i+1 access is disabled; i.e. not allowed. If '1', protection context i+1 access is enabled; i.e. allowed. Default Value: Undefined
8	PC_MASK_0	This field specifies protection context identifier based access control for protection context "0". Default Value: 1
6	NS	Non-secure: '0': Secure (secure accesses allowed, non-secure access NOT allowed). '1': Non-secure (both secure and non-secure accesses allowed). Default Value: Undefined
5	PX	Privileged execute enable: '0': Disabled (privileged, execute accesses are NOT allowed). '1': Enabled (privileged, execute accesses are allowed). Note that this register is constant '0'; i.e. privileged execute accesses are NEVER allowed. Default Value: 0
4	PW	Privileged write enable: '0': Disabled (privileged, write accesses are NOT allowed). '1': Enabled (privileged, write accesses are allowed). Default Value: Undefined
3	PR	Privileged read enable: '0': Disabled (privileged, read accesses are NOT allowed). '1': Enabled (privileged, read accesses are allowed). Note that this register is constant '1'; i.e. privileged read accesses are ALWAYS allowed. Default Value: 1
2	UX	User execute enable: '0': Disabled (user, execute accesses are NOT allowed). '1': Enabled (user, execute accesses are allowed). Note that this register is constant '0'; i.e. user execute accesses are NEVER allowed. Default Value: 0
1	UW	User write enable: '0': Disabled (user, write accesses are NOT allowed). '1': Enabled (user, write accesses are allowed). Default Value: Undefined
0	UR	User read enable: '0': Disabled (user, read accesses are NOT allowed). '1': Enabled (user, read accesses are allowed). Note that this register is constant '1'; i.e. user read accesses are ALWAYS allowed. Default Value: 1

7.1.11 PROT_SMPU_SMPU_STRUCT1_ADDR1

SMPU region address 1 (master structure)

Address: 0x40242060

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	This field specifies the most significant bits of the 32-bit address of an address region. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4203552
7 : 0	SUBREGION_DISABLE	This field is used to individually disabled the eight equally sized subregions in which a region is partitioned. Subregion disable: Bit 0: subregion 0 disable. Bit 1: subregion 1 disable. Bit 2: subregion 2 disable. Bit 3: subregion 3 disable. Bit 4: subregion 4 disable. Bit 5: subregion 5 disable. Bit 6: subregion 6 disable. Bit 7: subregion 7 disable. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 243

7.1.12 PROT_SMPU_SMPU_STRUCT2_ADDR1

SMPU region address 1 (master structure)

Address: 0x402420A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	This field specifies the most significant bits of the 32-bit address of an address region. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4203552
7 : 0	SUBREGION_DISABLE	This field is used to individually disabled the eight equally sized subregions in which a region is partitioned. Subregion disable: Bit 0: subregion 0 disable. Bit 1: subregion 1 disable. Bit 2: subregion 2 disable. Bit 3: subregion 3 disable. Bit 4: subregion 4 disable. Bit 5: subregion 5 disable. Bit 6: subregion 6 disable. Bit 7: subregion 7 disable. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 207

7.1.13 PROT_SMPU_SMPU_STRUCT3_ADDR1

SMPU region address 1 (master structure)

Address: 0x402420E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	This field specifies the most significant bits of the 32-bit address of an address region. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4203552
7 : 0	SUBREGION_DISABLE	This field is used to individually disabled the eight equally sized subregions in which a region is partitioned. Subregion disable: Bit 0: subregion 0 disable. Bit 1: subregion 1 disable. Bit 2: subregion 2 disable. Bit 3: subregion 3 disable. Bit 4: subregion 4 disable. Bit 5: subregion 5 disable. Bit 6: subregion 6 disable. Bit 7: subregion 7 disable. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 63

7.1.14 PROT_SMPU_SMPU_STRUCT4_ADDR1

SMPU region address 1 (master structure)

Address: 0x40242120

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	This field specifies the most significant bits of the 32-bit address of an address region. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4203553
7 : 0	SUBREGION_DISABLE	This field is used to individually disabled the eight equally sized subregions in which a region is partitioned. Subregion disable: Bit 0: subregion 0 disable. Bit 1: subregion 1 disable. Bit 2: subregion 2 disable. Bit 3: subregion 3 disable. Bit 4: subregion 4 disable. Bit 5: subregion 5 disable. Bit 6: subregion 6 disable. Bit 7: subregion 7 disable. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 252

7.1.15 PROT_SMPU_SMPU_STRUCT5_ADDR1

SMPU region address 1 (master structure)

Address: 0x40242160

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	This field specifies the most significant bits of the 32-bit address of an address region. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4203553
7 : 0	SUBREGION_DISABLE	This field is used to individually disabled the eight equally sized subregions in which a region is partitioned. Subregion disable: Bit 0: subregion 0 disable. Bit 1: subregion 1 disable. Bit 2: subregion 2 disable. Bit 3: subregion 3 disable. Bit 4: subregion 4 disable. Bit 5: subregion 5 disable. Bit 6: subregion 6 disable. Bit 7: subregion 7 disable. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 243

7.1.16 PROT_SMPU_SMPU_STRUCT6_ADDR1

SMPU region address 1 (master structure)

Address: 0x402421A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	This field specifies the most significant bits of the 32-bit address of an address region. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4203553
7 : 0	SUBREGION_DISABLE	This field is used to individually disabled the eight equally sized subregions in which a region is partitioned. Subregion disable: Bit 0: subregion 0 disable. Bit 1: subregion 1 disable. Bit 2: subregion 2 disable. Bit 3: subregion 3 disable. Bit 4: subregion 4 disable. Bit 5: subregion 5 disable. Bit 6: subregion 6 disable. Bit 7: subregion 7 disable. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 207

7.1.17 PROT_SMPU_SMPU_STRUCT7_ADDR1

SMPU region address 1 (master structure)

Address: 0x402421E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	This field specifies the most significant bits of the 32-bit address of an address region. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4203553
7 : 0	SUBREGION_DISABLE	This field is used to individually disabled the eight equally sized subregions in which a region is partitioned. Subregion disable: Bit 0: subregion 0 disable. Bit 1: subregion 1 disable. Bit 2: subregion 2 disable. Bit 3: subregion 3 disable. Bit 4: subregion 4 disable. Bit 5: subregion 5 disable. Bit 6: subregion 6 disable. Bit 7: subregion 7 disable. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 63

7.1.18 PROT_SMPU_SMPU_STRUCT8_ADDR1

SMPU region address 1 (master structure)

Address: 0x40242220

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	This field specifies the most significant bits of the 32-bit address of an address region. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4203554
7 : 0	SUBREGION_DISABLE	This field is used to individually disabled the eight equally sized subregions in which a region is partitioned. Subregion disable: Bit 0: subregion 0 disable. Bit 1: subregion 1 disable. Bit 2: subregion 2 disable. Bit 3: subregion 3 disable. Bit 4: subregion 4 disable. Bit 5: subregion 5 disable. Bit 6: subregion 6 disable. Bit 7: subregion 7 disable. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 252

7.1.19 PROT_SMPU_SMPU_STRUCT9_ADDR1

SMPU region address 1 (master structure)

Address: 0x40242260

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	This field specifies the most significant bits of the 32-bit address of an address region. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4203554
7 : 0	SUBREGION_DISABLE	This field is used to individually disabled the eight equally sized subregions in which a region is partitioned. Subregion disable: Bit 0: subregion 0 disable. Bit 1: subregion 1 disable. Bit 2: subregion 2 disable. Bit 3: subregion 3 disable. Bit 4: subregion 4 disable. Bit 5: subregion 5 disable. Bit 6: subregion 6 disable. Bit 7: subregion 7 disable. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 243

7.1.20 PROT_SMPU_SMPU_STRUCT10_ADDR1

SMPU region address 1 (master structure)

Address: 0x402422A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	This field specifies the most significant bits of the 32-bit address of an address region. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4203554
7 : 0	SUBREGION_DISABLE	This field is used to individually disabled the eight equally sized subregions in which a region is partitioned. Subregion disable: Bit 0: subregion 0 disable. Bit 1: subregion 1 disable. Bit 2: subregion 2 disable. Bit 3: subregion 3 disable. Bit 4: subregion 4 disable. Bit 5: subregion 5 disable. Bit 6: subregion 6 disable. Bit 7: subregion 7 disable. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 207

7.1.21 PROT_SMPU_SMPU_STRUCT11_ADDR1

SMPU region address 1 (master structure)

Address: 0x402422E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	This field specifies the most significant bits of the 32-bit address of an address region. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4203554
7 : 0	SUBREGION_DISABLE	This field is used to individually disabled the eight equally sized subregions in which a region is partitioned. Subregion disable: Bit 0: subregion 0 disable. Bit 1: subregion 1 disable. Bit 2: subregion 2 disable. Bit 3: subregion 3 disable. Bit 4: subregion 4 disable. Bit 5: subregion 5 disable. Bit 6: subregion 6 disable. Bit 7: subregion 7 disable. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 63

7.1.22 PROT_SMPU_SMPU_STRUCT12_ADDR1

SMPU region address 1 (master structure)

Address: 0x40242320

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	This field specifies the most significant bits of the 32-bit address of an address region. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4203555
7 : 0	SUBREGION_DISABLE	This field is used to individually disabled the eight equally sized subregions in which a region is partitioned. Subregion disable: Bit 0: subregion 0 disable. Bit 1: subregion 1 disable. Bit 2: subregion 2 disable. Bit 3: subregion 3 disable. Bit 4: subregion 4 disable. Bit 5: subregion 5 disable. Bit 6: subregion 6 disable. Bit 7: subregion 7 disable. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 252

7.1.23 PROT_SMPU_SMPU_STRUCT13_ADDR1

SMPU region address 1 (master structure)

Address: 0x40242360

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	This field specifies the most significant bits of the 32-bit address of an address region. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4203555
7 : 0	SUBREGION_DISABLE	This field is used to individually disabled the eight equally sized subregions in which a region is partitioned. Subregion disable: Bit 0: subregion 0 disable. Bit 1: subregion 1 disable. Bit 2: subregion 2 disable. Bit 3: subregion 3 disable. Bit 4: subregion 4 disable. Bit 5: subregion 5 disable. Bit 6: subregion 6 disable. Bit 7: subregion 7 disable. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 243

7.1.24 PROT_SMPU_SMPU_STRUCT14_ADDR1

SMPU region address 1 (master structure)

Address: 0x402423A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	This field specifies the most significant bits of the 32-bit address of an address region. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4203555
7 : 0	SUBREGION_DISABLE	This field is used to individually disabled the eight equally sized subregions in which a region is partitioned. Subregion disable: Bit 0: subregion 0 disable. Bit 1: subregion 1 disable. Bit 2: subregion 2 disable. Bit 3: subregion 3 disable. Bit 4: subregion 4 disable. Bit 5: subregion 5 disable. Bit 6: subregion 6 disable. Bit 7: subregion 7 disable. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 207

7.1.25 PROT_SMPU_SMPU_STRUCT15_ADDR1

SMPU region address 1 (master structure)

Address: 0x402423E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	This field specifies the most significant bits of the 32-bit address of an address region. "ADDR_DEF1": base address of structure. Note: this field is read-only. Default Value: 4203555
7 : 0	SUBREGION_DISABLE	This field is used to individually disabled the eight equally sized subregions in which a region is partitioned. Subregion disable: Bit 0: subregion 0 disable. Bit 1: subregion 1 disable. Bit 2: subregion 2 disable. Bit 3: subregion 3 disable. Bit 4: subregion 4 disable. Bit 5: subregion 5 disable. Bit 6: subregion 6 disable. Bit 7: subregion 7 disable. Two out of a total of eight 32 B subregions are enabled. These subregions includes region structures 0 and 1. Note: this field is read-only. Default Value: 63

7.1.26 PROT_MPU0_MS_CTL

Master control

Address: 0x40244000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				RW			
Name	None [7:4]				PC [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				RW			
Name	None [23:20]				PC_SAVED [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	PC_SAVED	Saved protection context. Modifications to this field are constrained by the associated MS_CTL.PC_MASK_0 and MS_CTL.PC_MASK_15_TO_1[] fields. Default Value: 0
3 : 0	PC	Active protection context. Modifications to this field are constrained by the associated MS_CTL.PC_MASK_0 and MS_CTL.PC_MASK_15_TO_1[] fields. In addition, a write transfer with protection context "0" can change this field. The CM0+ CPU PC field is writable by HW and SW (all other PC fields are only writable by SW). On entry of a Cypress "trusted" exception/interrupt handler (the handler start address equals CPUSS CM0_PC0_HANDLER.ADDR): - PC_SAVED is not changed if PC is "0". PC_SAVED is set to PC if PC is not "0". - PC is set to "0". On entry of any other exception/interrupt handler (the handler start address does not equal CPUSS CM0_PC0_HANDLER.ADDR): - PC_SAVED is not changed. - PC is set to PC_SAVED. Protection context "0" is considered a special protection context in trusted systems and should be reserved for Cypress "trusted" code execution. In addition, a write transfer with protection context "0" can change this field. Default Value: 0

7.1.27 PROT_MPU1_MS_CTL

Master control

Address: 0x40244400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				RW			
Name	None [7:4]				PC [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	PC	Active protection context. Modifications to this field are constrained by the associated MS_CTL.PC_MASK_0 and MS_CTL.PC_MASK_15_TO_1[] fields. In addition, a write transfer with protection context "0" can change this field. The CM0+ CPU PC field is writable by HW and SW (all other PC fields are only writable by SW). On entry of a Cypress "trusted" exception/interrupt handler (the handler start address equals CPUSS CM0_PC0_HANDLER.ADDR): - PC_SAVED is not changed if PC is "0". PC_SAVED is set to PC if PC is not "0". - PC is set to "0". On entry of any other exception/interrupt handler (the handler start address does not equal CPUSS CM0_PC0_HANDLER.ADDR): - PC_SAVED is not changed. - PC is set to PC_SAVED. Protection context "0" is considered a special protection context in trusted systems and should be reserved for Cypress "trusted" code execution. In addition, a write transfer with protection context "0" can change this field. Default Value: 0

7.1.28 PROT_MPU1_MPU_STRUCT0_ADDR

MPU region address

Address: 0x40244600

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SUBREGION_DISABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	ADDR24 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	ADDR24 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	ADDR24 [31:24]							

Bits	Name	Description
31 : 8	ADDR24	This field specifies the most significant bits of the 32-bit address of an address region. The region size is defined by ATT.REGION_SIZE. A region of n Byte is always n Byte aligned. As a result, some of the lesser significant address bits of ADDR24 may be ignored in determining whether a bus transfer address is within an address region. E.g., a 64 KByte address region (REGION_-SIZE is "15") is 64 KByte aligned, and ADDR24[7:0] are ignored. Default Value: Undefined

7.1.28 PROT_MPU1_MPU_STRUCT0_ADDR (continued)

7 : 0	SUBREGION_DISABLE	This field is used to individually disabled the eight equally sized subregions in which a region is partitioned. Subregion disable: Bit 0: subregion 0 disable. Bit 1: subregion 1 disable. Bit 2: subregion 2 disable. Bit 3: subregion 3 disable. Bit 4: subregion 4 disable. Bit 5: subregion 5 disable. Bit 6: subregion 6 disable. Bit 7: subregion 7 disable. E.g., a 64 KByte address region (REGION_SIZE is "15") has eight 8 KByte subregions. The access control as defined by MPU_REGION_ATT applies if the bus transfer address is within the address region AND the addressed subregion is NOT disabled. Note that the smallest region size is 256 B and the smallest subregion size is 32 B. Default Value: Undefined

7.1.29 PROT_MPU1_MPU_STRUCT0_ATT

MPU region attrributes

Address: 0x40244604

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	RW	RW	RW	RW	RW	RW
HW Access	None	R	R	R	R	R	R	R
Name	None	NS	PX	PW	PR	UX	UW	UR

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None		RW				
HW Access	R	None		R				
Name	ENABLED	None [30:29]		REGION_SIZE [28:24]				

Bits	Name	Description
31	ENABLED	Region enable: '0': Disabled. A disabled region will never result in a match on the bus transfer address. '1': Enabled. Note: a disabled address region performs logic gating to reduce dynamic power consumption. Default Value: 0

7.1.29 PROT_MPU1_MPU_STRUCT0_ATT (continued)

28 : 24	REGION_SIZE	This field specifies the region size: "0"-"6": Undefined. "7": 256 B region "8": 512 B region "9": 1 KB region "10": 2 KB region "11": 4 KB region "12": 8 KB region "13": 16 KB region "14": 32 KB region "15": 64 KB region "16": 128 KB region "17": 256 KB region "18": 512 KB region "19": 1 MB region "20": 2 MB region "21": 4 MB region "22": 8 MB region "23": 16 MB region "24": 32 MB region "25": 64 MB region "26": 128 MB region "27": 256 MB region "28": 512 MB region "39": 1 GB region "30": 2 GB region "31": 4 GB region Default Value: Undefined
6	NS	Non-secure: '0': Secure (secure accesses allowed, non-secure access NOT allowed). '1': Non-secure (both secure and non-secure accesses allowed). Default Value: Undefined
5	PX	Privileged execute enable: '0': Disabled (privileged, execute accesses are NOT allowed). '1': Enabled (privileged, execute accesses are allowed). Default Value: Undefined
4	PW	Privileged write enable: '0': Disabled (privileged, write accesses are NOT allowed). '1': Enabled (privileged, write accesses are allowed). Default Value: Undefined
3	PR	Privileged read enable: '0': Disabled (privileged, read accesses are NOT allowed). '1': Enabled (privileged, read accesses are allowed). Default Value: Undefined
2	UX	User execute enable: '0': Disabled (user, execute accesses are NOT allowed). '1': Enabled (user, execute accesses are allowed). Default Value: Undefined
1	UW	User write enable: '0': Disabled (user, write accesses are NOT allowed). '1': Enabled (user, write accesses are allowed). Default Value: Undefined

7.1.29 PROT_MPU1_MPU_STRUCT0_ATT (continued)

0	UR	User read enable: '0': Disabled (user, read accesses are NOT allowed). '1': Enabled (user, read accesses are allowed). Default Value: Undefined

8 Flash Controller Registers

This section discusses the Flash Controller registers. It lists all the registers in mapping tables, in address order.

8.1 Register Details

Register	Address	Description
FLASHC_FLASH_CTL	0x40250000	Control
FLASHC_FLASH_PWR_CTL	0x40250004	Flash power control
FLASHC_FLASH_CMD	0x40250008	Command
FLASHC_BIST_CTL	0x40250100	BIST control
FLASHC_BIST_CMD	0x40250104	BIST command
FLASHC_BIST_ADDR_START	0x40250108	BIST address start register
FLASHC_BIST_DATA0	0x4025010C	BIST data register(s)
FLASHC_BIST_DATA1	0x40250110	BIST data register(s). See FLASHC_BIST_DATA0 for the details of bit fields.
FLASHC_BIST_DATA2	0x40250114	BIST data register(s). See FLASHC_BIST_DATA0 for the details of bit fields.
FLASHC_BIST_DATA3	0x40250118	BIST data register(s). See FLASHC_BIST_DATA0 for the details of bit fields.
FLASHC_BIST_DATA_ACT0	0x4025012C	BIST data actual register(s)
FLASHC_BIST_DATA_ACT1	0x40250130	BIST data actual register(s). See FLASHC_BIST_DATA_ACT0 for the details of bit fields.
FLASHC_BIST_DATA_ACT2	0x40250134	BIST data actual register(s). See FLASHC_BIST_DATA_ACT0 for the details of bit fields.
FLASHC_BIST_DATA_ACT3	0x40250138	BIST data actual register(s). See FLASHC_BIST_DATA_ACT0 for the details of bit fields.
FLASHC_BIST_DATA_EXP0	0x4025014C	BIST data expected register(s)
FLASHC_BIST_DATA_EXP1	0x40250150	BIST data expected register(s). See FLASHC_BIST_DATA_EXP0 for the details of bit fields.
FLASHC_BIST_DATA_EXP2	0x40250154	BIST data expected register(s). See FLASHC_BIST_DATA_EXP0 for the details of bit fields.
FLASHC_BIST_DATA_EXP3	0x40250158	BIST data expected register(s). See FLASHC_BIST_DATA_EXP0 for the details of bit fields.
FLASHC_BIST_ADDR	0x4025016C	BIST address register
FLASHC_BIST_STATUS	0x40250170	BIST status register
FLASHC_CM0_CA_CTL0	0x40250400	CM0+ cache control
FLASHC_CM0_CA_CTL1	0x40250404	CM0+ cache control
FLASHC_CM0_CA_CTL2	0x40250408	CM0+ cache control
FLASHC_CM0_CA_CMD	0x4025040C	CM0+ cache command
FLASHC_CM0_CA_STATUS0	0x40250440	CM0+ cache status 0
FLASHC_CM0_CA_STATUS1	0x40250444	CM0+ cache status 1
FLASHC_CM0_CA_STATUS2	0x40250448	CM0+ cache status 2

Register	Address	Description
FLASHC_CM4_CA_CTL0	0x40250480	CM4 cache control
FLASHC_CM4_CA_CTL1	0x40250484	CM4 cache control
FLASHC_CM4_CA_CTL2	0x40250488	CM4 cache control
FLASHC_CM4_CA_CMD	0x4025048C	CM4 cache command
FLASHC_CM4_CA_STATUS0	0x402504C0	CM4 cache status 0
FLASHC_CM4_CA_STATUS1	0x402504C4	CM4 cache status 1
FLASHC_CM4_CA_STATUS2	0x402504C8	CM4 cache status 2
FLASHC_CRYPTO_BUFF_CTL	0x40250500	Cryptography buffer control
FLASHC_CRYPTO_BUFF_CMD	0x40250508	Cryptography buffer command
FLASHC_DW0_BUFF_CTL	0x40250580	Datawire 0 buffer control
FLASHC_DW0_BUFF_CMD	0x40250588	Datawire 0 buffer command
FLASHC_DW1_BUFF_CTL	0x40250600	Datawire 1 buffer control
FLASHC_DW1_BUFF_CMD	0x40250608	Datawire 1 buffer command
FLASHC_DAP_BUFF_CTL	0x40250680	Debug access port buffer control
FLASHC_DAP_BUFF_CMD	0x40250688	Debug access port buffer command
FLASHC_EXT_MS0_BUFF_CTL	0x40250700	External master 0 buffer control
FLASHC_EXT_MS0_BUFF_CMD	0x40250708	External master 0 buffer command
FLASHC_EXT_MS1_BUFF_CTL	0x40250780	External master 1 buffer control
FLASHC_EXT_MS1_BUFF_CMD	0x40250788	External master 1 buffer command
FLASHC_FM_CTL	0x4025F000	Flash macro control
FLASHC_STATUS	0x4025F004	Status
FLASHC_FM_ADDR	0x4025F008	Flash macro address
FLASHC_GEOMETRY	0x4025F00C	Regular flash geometry
FLASHC_GEOMETRY_SUPERVISORY	0x4025F010	Supervisory flash geometry
FLASHC_TIMER_CTL	0x4025F014	Timer control
FLASHC_ANA_CTL0	0x4025F018	Analog control 0
FLASHC_ANA_CTL1	0x4025F01C	Analog control 1
FLASHC_GEOMETRY_GEN	0x4025F020	N/A, DNU
FLASHC_TEST_CTL	0x4025F024	Test mode control
FLASHC_WAIT_CTL	0x4025F028	Wiat State control
FLASHC_MONITOR_STATUS	0x4025F02C	Monitor Status
FLASHC_SCRATCH_CTL	0x4025F030	Scratch Control
FLASHC_HV_CTL	0x4025F034	High voltage control
FLASHC_ACLK_CTL	0x4025F038	Aclk control
FLASHC_INTR	0x4025F03C	Interrupt
FLASHC_INTR_SET	0x4025F040	Interrupt set
FLASHC_INTR_MASK	0x4025F044	Interrupt mask
FLASHC_INTR_MASKED	0x4025F048	Interrupt masked
FLASHC_FM_HV_DATA_ALL	0x4025F04C	Flash macro high Voltage page latches data (for all page latches)
FLASHC_CAL_CTL0	0x4025F050	Cal control BG LO trim bits
FLASHC_CAL_CTL1	0x4025F054	Cal control BG HI trim bits
FLASHC_CAL_CTL2	0x4025F058	Cal control BG LO&HI ipref trim, ref sel, fm_active, turbo_ext

Register	Address	Description
FLASHC_CAL_CTL3	0x4025F05C	Cal control osc trim bits, idac, sdac, itim, bdac.
FLASHC_BOOKMARK	0x4025F060	Bookmark register - keeps the current FW HV seq
FLASHC_RED_CTL01	0x4025F080	Redundancy Control normal sectors 0,1
FLASHC_RED_CTL23	0x4025F084	Redundancy Controll normal sectors 2,3
FLASHC_RED_CTL45	0x4025F088	Redundancy Controll normal sectors 4,5
FLASHC_RED_CTL67	0x4025F08C	Redundancy Controll normal sectors 6,7
FLASHC_RED_CTL_SM01	0x4025F090	Redundancy Controll special sectors 0,1
FLASHC_TM_CMPR0	0x4025F100	Do Not Use. This is the starting address of a register bank containing 32 registers (FLASHC_TM_CMPR0 to FLASHC_TM_CMPR31).
FLASHC_FM_HV_DATA0	0x4025F800	Flash macro high Voltage page latches data. This is the starting address of a register bank containing 128 registers (FLASHC_FM_HV_DATA0 to FLASHC_FM_HV_DATA127).
FLASHC_FM_MEM_DATA0	0x4025FC00	Flash macro memory sense amplifier and column decoder data. This is the starting address of a register bank containing 128 registers (FLASHC_FM_MEM_DATA0 to FLASHC_FM_MEM_DATA127).

8.1.1 FLASHC_FLASH_CTL

Control

Address: 0x40250000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				MAIN_WS [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							REMAP

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description

8.1.1 FLASHC_FLASH_CTL (continued)

8	REMAP	Specifies remapping of FLASH macro main region. 0: No remapping. 1: Remapping. The highest address bit of the FLASH main region is inverted. This effectively re-maps the location of FLASH main region physical sectors in the logical address space. In other words, the higher half physical sectors are swapped with the lower half physical sectors. Note: remapping only affects reading of the FLASH main region (over the R interface). It does NOT affect programming/erasing of the FLASH memory region (over the C interface). E.g., for a 512 KB / 4 Mb main region, the logical address space ranges from [0x1000:0000, 0x1007:ffff] (the highest bit if the FLASH main region is bit 18). The memory has four physical sectors: sectors 0, 1, 2 and 3. If REMAP is '0', the physical regions logical addresses are as follows: - The physical region 0: [0x1000:0000, 0x1001:ffff]. - The physical region 1: [0x1002:0000, 0x1003:ffff]. - The physical region 2: [0x1004:0000, 0x1005:ffff]. - The physical region 3: [0x1006:0000, 0x1007:ffff]. If REMAP is '1', the physical regions logical addresses are as follows: - The physical region 0: [0x1004:0000, 0x1005:ffff]. - The physical region 1: [0x1006:0000, 0x1007:ffff]. - The physical region 2: [0x1000:0000, 0x1001:ffff]. - The physical region 3: [0x1002:0000, 0x1003:ffff]. Note: when the REMAP is changed, SW should invalidate the caches and buffers. Default Value: 0
3 : 0	MAIN_WS	FLASH macro main interface wait states: 0: 0 wait states. ... 15: 15 wait states Default Value: 0

8.1.2 FLASHC_FLASH_PWR_CTL

Flash power control

Address: 0x40250004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						EN-ABLE_HV	ENABLE

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	ENABLE_HV	Controls "enable_hv" pin of the Flash memory. Default Value: 1
0	ENABLE	Controls "enable" pin of the Flash memory. Default Value: 1

8.1.3 FLASHC_FLASH_CMD

Command

Address: 0x40250008

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1S
HW Access	None							RW1C
Name	None [7:1]							INV

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	INV	FLASH cache and buffer invalidation for ALL cache and buffers. SW writes a '1' to clear the cache and buffers. HW sets this field to '0' when the operation is completed. The operation takes a maximum of three clock cycles on the slowest of the clk_slow and clk_fast clocks. The caches' LRU structures are also reset to their default state. Default Value: 0

8.1.4 FLASHC_BIST_CTL

BIST control

Address: 0x40250100

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	
HW Access	R	R	R	R	R	R	R	
Name	STOP_ON_ERROR	INCR_DECR_BOTH	ADDR_COMPLIMENT_ENABLED	ADDR_START_ENABLED	ROW_FIRST	UP	OPCODE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	STOP_ON_ERROR	Specifies the BIST to continue indefinitely, regardless of occurrence of errors or not. 0: BIST controller doesn't stop on the data failures, it continues regardless of the errors. 1: BIST controller stops on when the first data failure is encountered. Default Value: 0

8.1.4 FLASHC_BIST_CTL (continued)

6	INCR_DECR_BOTH	Specifies to generate patterns where both column address and row address are incremented/ decremented simultaneously. 0: Generate normal increment/decrement patterns. 1: Generate address patterns with both row and column address changing. Example: With UP = 1 and ROW_FIRST = 0 00_00 01_01 10_10 11_11 00_01 01_10 10_11 11_00 00_10 ... Default Value: 0
5	ADDR_COMPLI-MENT_ENABLED	Specifies to generate address compliment patterns. 0: Generate normal increment/decrement patterns. 1: Generate address patterns which interleaves compliment of previous address in between. Example: The following is an example pattern, With UP=1 and ROW_FIRST =0 00_00 11_11 00_01 11_10 00_10 11_01 ... Default Value: 0
4	ADDR_START_ENABLED	Specifies Flash BIST start addresses: '0': Row and column addresses start with their maximum/minimum values. '1': Row and column addresses start with their values as specified by BIST_ADDR_START. This feature is supported only for simple increment/decrement patterns. It is not supported with address compliment pattern (BIST_CTL.ADDR_COMPLIMENT_ENABLED) or address pattern which increments/decrements both row address and column address (BIST_CTL.INCR_DE-CR_BOTH) for every read. Default Value: 0
3	ROW_FIRST	Specifies how the Flash BIST addresses are generated: '0': Column address is incremented/decremented till it reaches its maximum/minimum value. Once it reach its maximum/minimum value, it is set to its minimum/maximum value and only then is the row address incremented/decremented. '1': Row address is incremented/decremented till it reaches its maximum/minimum value. Once it reach its maximum/minimum value, it is set to its minimum/maximum value and only then is the column address incremented/decremented. Default Value: 0
2	UP	Specifies direction in which Flash BIST steps through addresses: 0: BIST steps through the Flash from the maximum row and column addresses (as specified by a design time configuration parameter when ADDR_START_ENABLED is "0" and as specified by BIST_ADDR_START when ADDR_START_ENABLED is "1") to the minimum row and col-umn addresses. 1: BIST steps through the Flash from the minimum row and column addresses ("0" when AD-DR_START_ENABLED is "0" and as specified by BIST_ADDR_START when AD-DR_START_ENABLED is "1"' to the maximum row and column addresses. Default Value: 0

8.1.4 FLASHC_BIST_CTL (continued)

1 : 0	OPCODE	This field specifies how the data check should be performed after reading the data from Flash memory. 0: Read the Flash and compare the output to BIST_DATA (R0). 1: Read the Flash and compare the output to the binary complement of BIST_DATA (R1). 3: Read the Flash and compare with BIST_DATA[] and compliment of BIST_DATA alternately (R01). The expected data of the first read is BIST_DATA, expected data of the second read is binary compliment of BIST_DATA, third read expected data is BIST_DATA, fourth read expected data is binary compliment of BIST_DATA and so on. Default Value: 0

8.1.5 FLASHC_BIST_CMD

BIST command

Address: 0x40250104

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							RW1C
Name	None [7:1]							START

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	START	1: Start FLASH BIST. Hardware set this field to '0' when BIST is completed. Default Value: 0

8.1.6 FLASHC_BIST_ADDR_START

BIST address start register

Address: 0x40250108

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	COL_ADDR_START [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	COL_ADDR_START [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	ROW_ADDR_START [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	ROW_ADDR_START [31:24]							

Bits	Name	Description
31 : 16	ROW_ADDR_START	Row start address. Useful to apply BIST to a part of an Flash. The value of this field should be in a legal range (a value outside of the legal range has an undefined result, and may lock up the BIST state machine). This legal range is dependent on the number of rows of the SRAM the BIST is applied to (as specified by BIST_CTL.SRAMS_ENABLED). E.g. for a Flash with m columns, the legal range is [0, m-1]. Default Value: 0
15 : 0	COL_ADDR_START	Column start address. Useful to apply BIST to a part of an Flash. The value of this field should be in a legal range (a value outside of the legal range has an undefined result, and may lock up the BIST state machine). This legal range is dependent on the number of columns of the SRAM the BIST is applied to (as specified by BIST_CTL.SRAMS_ENABLED). E.g. for a Flash with n columns, the legal range is [0, n-1]. Default Value: 0

8.1.7 FLASHC_BIST_DATA0

BIST data register(s)

Address: 0x4025010C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	BIST data register to store the expected value for data comparison. For a 128-bit Flash memory, there will be 4 BIST_DATA registers to store 128-bit value. Default Value: 0

8.1.8 FLASHC_BIST_DATA_ACT0

BIST data actual register(s)

Address: 0x4025012C

Retention: Not Retained

Bits	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SW Access	R							
HW Access	W							
Name	DATA [7:0]							

Bits	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SW Access	R							
HW Access	W							
Name	DATA [15:8]							

Bits	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SW Access	R							
HW Access	W							
Name	DATA [23:16]							

Bits	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**
SW Access	R							
HW Access	W							
Name	DATA [31:24]							

Bits	**Name**	**Description**
31 : 0	DATA	This field specified the actual Flash data output that caused the BIST failure. Default Value: Undefined

8.1.9 FLASHC_BIST_DATA_EXP0

BIST data expected register(s)

Address: 0x4025014C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	This field specified the expected Flash data output. Default Value: Undefined

8.1.10 FLASHC_BIST_ADDR

BIST address register

Address: 0x4025016C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	COL_ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	COL_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	ROW_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	ROW_ADDR [31:24]							

Bits	Name	Description
31 : 16	ROW_ADDR	Current row address. Default Value: Undefined
15 : 0	COL_ADDR	Current column address. Default Value: Undefined

8.1.11 FLASHC_BIST_STATUS

BIST status register

Address: 0x40250170

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							W1S
Name	None [7:1]							FAIL

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	FAIL	0: BIST passed. 1: BIST failed. Default Value: 0

8.1.12 FLASHC_CM0_CA_CTL0

CM0+ cache control

Address: 0x40250400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	
HW Access	None						R	
Name	None [23:18]						WAY [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None			RW		
HW Access	R	R	None			R		
Name	ENABLED	PREF_EN	None [29:27]			SET_ADDR [26:24]		

Bits	Name	Description
31	ENABLED	Cache enable: 0: Disabled. The cache tag valid bits are reset to '0's and the cache LRU information is set to '1's (making way 0 the LRU way and way 3 the MRU way). 1: Enabled. Default Value: 1
30	PREF_EN	Prefetch enable: 0: Disabled. 1: Enabled. Prefetching requires the cache to be enabled; i.e. ENABLED is '1'. Default Value: 1
26 : 24	SET_ADDR	Specifies the cache set for which cache information is provided in CM0_CA_STATUS0/1/2. Default Value: 0
17 : 16	WAY	Specifies the cache way for which cache information is provided in CM0_CA_STATUS0/1/2. Default Value: 0

8.1.13 FLASHC_CM0_CA_CTL1

CM0+ cache control

Address: 0x40250404

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	
HW Access	None						R	
Name	None [7:2]						PWR_MODE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VECTKEYSTAT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VECTKEYSTAT [31:24]							

Bits	Name	Description
31 : 16	VECTKEYSTAT	Register key (to prevent accidental writes). - Should be written with a 0x05fa key value for the write to take effect. - Always reads as 0xfa05. Default Value: 64005
1 : 0	PWR_MODE	Set Power mode for CM0 cache Default Value: 3 **0x0: OFF :** See CM4_PWR_CTL **0x1: RESERVED :** undefined **0x2: RETAINED :** See CM4_PWR_CTL

8.1.13 FLASHC_CM0_CA_CTL1 (continued)

0x3: ENABLED :

See CM4_PWR_CTL

8.1.14 FLASHC_CM0_CA_CTL2

CM0+ cache control

Address: 0x40250408

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	PWRUP_DELAY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						PWRUP_DELAY [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 0	PWRUP_DELAY	Number clock cycles delay needed after power domain power up Default Value: 300

8.1.15 FLASHC_CM0_CA_CMD

CM0+ cache command

Address: 0x4025040C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1S
HW Access	None							RW1C
Name	None [7:1]							INV

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	INV	FLASH cache invalidation. SW writes a "1" to clear the cache. W sets this field to "0" when the operation is completed. The operation takes a maximum of three clock cycles on the slowest of the clk_slow and clk_fast clocks. The cache's LRU structure is also reset to its default state. Default Value: 0

8.1.16 FLASHC_CM0_CA_STATUS0

CM0+ cache status 0

Address: 0x40250440

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	VALID16 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	VALID16 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	VALID16	Sixteen valid bits of the cache line specified by CM0_CA_CTL.WAY and CM0_-CA_CTL.SET_ADDR. Default Value: 0

8.1.17 FLASHC_CM0_CA_STATUS1

CM0+ cache status 1

Address: 0x40250444

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	TAG [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	TAG [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	TAG [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	TAG [31:24]							

Bits	Name	Description
31 : 0	TAG	Cache line address of the cache line specified by CM0_CA_CTL.WAY and CM0_-CA_CTL.SET_ADDR. Default Value: Undefined

8.1.18 FLASHC_CM0_CA_STATUS2

CM0+ cache status 2

Address: 0x40250448

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R					
HW Access	None		W					
Name	None [7:6]		LRU [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	LRU	Six bit LRU representation of the cache set specified by CM0_CA_CTL.SET_ADDR. The encoding of the field is as follows ("X_LRU_Y" indicates that way X is Less Recently Used than way Y): Bit 5: 0_LRU_1: way 0 less recently used than way 1. Bit 4: 0_LRU_2. Bit 3: 0_LRU_3. Bit 2: 1_LRU_2. Bit 1: 1_LRU_3. Bit 0: 2_LRU_3. Default Value: Undefined

8.1.19 FLASHC_CM4_CA_CTL0

CM4 cache control

Address: 0x40250480

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	
HW Access	None						R	
Name	None [23:18]						WAY [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None			RW		
HW Access	R	R	None			R		
Name	ENABLED	PREF_EN	None [29:27]			SET_ADDR [26:24]		

Bits	Name	Description
31	ENABLED	See CM0_CA_CTL. Default Value: 1
30	PREF_EN	See CM0_CA_CTL. Default Value: 1
26 : 24	SET_ADDR	See CM0_CA_CTL. Default Value: 0
17 : 16	WAY	See CM0_CA_CTL. Default Value: 0

8.1.20 FLASHC_CM4_CA_CTL1

CM4 cache control

Address: 0x40250484

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	
HW Access	None						R	
Name	None [7:2]						PWR_MODE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VECTKEYSTAT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VECTKEYSTAT [31:24]							

Bits	Name	Description
31 : 16	VECTKEYSTAT	Register key (to prevent accidental writes). - Should be written with a 0x05fa key value for the write to take effect. - Always reads as 0xfa05. Default Value: 64005
1 : 0	PWR_MODE	Set Power mode for CM4 cache Default Value: 3 **0x0: OFF :** See CM4_PWR_CTL **0x1: RESERVED :** undefined **0x2: RETAINED :** See CM4_PWR_CTL

8.1.20 FLASHC_CM4_CA_CTL1 (continued)

0x3: ENABLED :

See CM4_PWR_CTL

8.1.21 FLASHC_CM4_CA_CTL2

CM4 cache control

Address: 0x40250488

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	PWRUP_DELAY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						PWRUP_DELAY [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 0	PWRUP_DELAY	Number clock cycles delay needed after power domain power up Default Value: 300

8.1.22 FLASHC_CM4_CA_CMD

CM4 cache command

Address: 0x4025048C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1S
HW Access	None							RW1C
Name	None [7:1]							INV

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	INV	See CM0_CA_CMD. Default Value: 0

8.1.23 FLASHC_CM4_CA_STATUS0

CM4 cache status 0

Address: 0x402504C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	VALID16 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	VALID16 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	VALID16	See CM0_CA_STATUS0. Default Value: 0

8.1.24 FLASHC_CM4_CA_STATUS1

CM4 cache status 1

Address: 0x402504C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	TAG [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	TAG [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	TAG [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	TAG [31:24]							

Bits	Name	Description
31 : 0	TAG	See CM0_CA_STATUS1. Default Value: Undefined

8.1.25 FLASHC_CM4_CA_STATUS2

CM4 cache status 2

Address: 0x402504C8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R					
HW Access	None		W					
Name	None [7:6]		LRU [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	LRU	See CM0_CA_STATUS2. Default Value: Undefined

8.1.26 FLASHC_CRYPTO_BUFF_CTL

Cryptography buffer control

Address: 0x40250500

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None					
HW Access	R	R	None					
Name	ENABLED	PREF_EN	None					

Bits	Name	Description
31	ENABLED	Cache enable: 0: Disabled. 1: Enabled. Default Value: 1
30	PREF_EN	Prefetch enable: 0: Disabled. 1: Enabled. Prefetching requires the buffer to be enabled; i.e. ENABLED is '1'. Default Value: 1

8.1.27 FLASHC_CRYPTO_BUFF_CMD

Cryptography buffer command

Address: 0x40250508

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1S
HW Access	None							RW1C
Name	None [7:1]							INV

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	INV	FLASH buffer invalidation. SW writes a "1" to clear the buffer. HW sets this field to '0' when the operation is completed. Default Value: 0

8.1.28 FLASHC_DW0_BUFF_CTL

Datawire 0 buffer control

Address: 0x40250580

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None					
HW Access	R	R	None					
Name	ENABLED	PREF_EN	None					

Bits	Name	Description
31	ENABLED	See CRYPTO_BUFF_CTL. Default Value: 1
30	PREF_EN	See CRYPTO_BUFF_CTL. Default Value: 1

8.1.29 FLASHC_DW0_BUFF_CMD

Datawire 0 buffer command

Address: 0x40250588

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1S
HW Access	None							RW1C
Name	None [7:1]							INV

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	INV	See CRYPTO_BUFF_CMD. Default Value: 0

8.1.30 FLASHC_DW1_BUFF_CTL

Datawire 1 buffer control

Address: 0x40250600

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None					
HW Access	R	R	None					
Name	ENABLED	PREF_EN	None					

Bits	Name	Description
31	ENABLED	See CRYPTO_BUFF_CTL. Default Value: 1
30	PREF_EN	See CRYPTO_BUFF_CTL. Default Value: 1

8.1.31 FLASHC_DW1_BUFF_CMD

Datawire 1 buffer command

Address: 0x40250608

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1S
HW Access	None							RW1C
Name	None [7:1]							INV

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	INV	See CRYPTO_BUFF_CMD. Default Value: 0

8.1.32 FLASHC_DAP_BUFF_CTL

Debug access port buffer control

Address: 0x40250680

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None					
HW Access	R	R	None					
Name	ENABLED	PREF_EN	None					

Bits	Name	Description
31	ENABLED	See CRYPTO_BUFF_CTL. Default Value: 1
30	PREF_EN	See CRYPTO_BUFF_CTL. Default Value: 1

8.1.33 FLASHC_DAP_BUFF_CMD

Debug access port buffer command

Address: 0x40250688

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1S
HW Access	None							RW1C
Name	None [7:1]							INV

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	INV	See CRYPTO_BUFF_CMD. Default Value: 0

8.1.34 FLASHC_EXT_MS0_BUFF_CTL

External master 0 buffer control

Address: 0x40250700

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None					
HW Access	R	R	None					
Name	ENABLED	PREF_EN	None					

Bits	Name	Description
31	ENABLED	See CRYPTO_BUFF_CTL. Default Value: 1
30	PREF_EN	See CRYPTO_BUFF_CTL. Default Value: 1

8.1.35 FLASHC_EXT_MS0_BUFF_CMD

External master 0 buffer command

Address: 0x40250708

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1S
HW Access	None							RW1C
Name	None [7:1]							INV

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	INV	See CRYPTO_BUFF_CMD. Default Value: 0

8.1.36 FLASHC_EXT_MS1_BUFF_CTL

External master 1 buffer control

Address: 0x40250780

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None					
HW Access	R	R	None					
Name	ENABLED	PREF_EN	None					

Bits	Name	Description
31	ENABLED	See CRYPTO_BUFF_CTL. Default Value: 1
30	PREF_EN	See CRYPTO_BUFF_CTL. Default Value: 1

8.1.37 FLASHC_EXT_MS1_BUFF_CMD

External master 1 buffer command

Address: 0x40250788

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1S
HW Access	None							RW1C
Name	None [7:1]							INV

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	INV	See CRYPTO_BUFF_CMD. Default Value: 0

8.1.38 FLASHC_FM_CTL

Flash macro control

Address: 0x4025F000

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				FM_MODE [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						FM_SEQ [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None	RW						
HW Access	None	R						
Name	None	DAA_MUX_SEL [22:16]						

Bits	31	30	29	28	27	26	25	24
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [31:26]						WR_EN	IF_SEL

Bits	Name	Description
25	WR_EN	"0": normal mode "1": Fm Write Enable Default Value: 0
24	IF_SEL	Interface selection. Specifies the interface that is used for flash memory read operations: '0': R interface is used (default value). In this case, the flash memory address is provided as part of the R signal interface. '1': C interface is used. In this case, the flash memory address is provided by FM_MEM_ADDR (the page address) and by the C interface access offset in the FM_MEM_DATA structure. Default Value: 0
22 : 16	DAA_MUX_SEL	Direct memory cell access address. Default Value: 0
9 : 8	FM_SEQ	Flash macro sequence select: "0": TBD "1": TBD "2": TBD "3": TBD Default Value: 0

8.1.38 FLASHC_FM_CTL (continued)

3 : 0	FM_MODE	Flash macro mode selection: "0": Normal functional mode. "1": Sets "pre-program control bit" for soft pre-program operation of all selected SONOS cells. the control bit is cleared by the HW after any program operation. "2": Sets ... "15": TBD Default Value: 0

8.1.39 FLASHC_STATUS

Status

Address: 0x4025F004

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R	R	R	R	R	R
HW Access	None		W	W	W	W	W	W
Name	None [7:6]		IF-_SEL_MON	WR_EN_MON	TURBO_N	ILLE-GAL_HVOP	HV_REGS_ISOLATED	HV_TIM-ER_RUN-NING

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	IF_SEL_MON	FM_CTL.IF_SEL bit after being synchronized in clk_r domain Default Value: 0
4	WR_EN_MON	FM_CTL.WR_EN bit after being synchronized in clk_r domain Default Value: 0
3	TURBO_N	After FM power up indicates the analog blocks currents are boosted to faster reach their functional state.. Used in the testchip boot only as an "FM READY" flag. '0' - turbo mode '1' - normal mode Default Value: 0
2	ILLEGAL_HVOP	Indicates a bulk, sector erase, program has been requested when axa=1 '0' - no error '1' - illegal HV operation error Default Value: 0

8.1.39 FLASHC_STATUS (continued)

1	HV_REGS_ISOLATED	Indicates the isolation status at HV trim and redundancy registers inputs '0' - Not isolated, writing permitted '1' - isolated writing disabled Default Value: 0
0	HV_TIMER_RUNNING	Indicates if the high voltage timer is running: '0': not running '1': running Default Value: 0

8.1.40 FLASHC_FM_ADDR

Flash macro address

Address: 0x4025F008

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	RA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	RA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	BA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							RW
HW Access	None							R
Name	None [31:25]							AXA

Bits	Name	Description
24	AXA	Auxiliary address field: '0': regular flash memory. '1': supervisory flash memory. Default Value: 0
23 : 16	BA	Bank address. Default Value: 0
15 : 0	RA	Row address. Default Value: 0

8.1.41 FLASHC_GEOMETRY

Regular flash geometry

Address: 0x4025F00C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	W				W			
Name	PAGE_SIZE_LOG2 [7:4]				WORD_SIZE_LOG2 [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	ROW_COUNT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	ROW_COUNT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	BANK_COUNT [31:24]							

Bits	Name	Description
31 : 24	BANK_COUNT	Number of banks (minus 1): "0": 1 bank "1": 2 banks ... "255": 256 banks Default Value: 0
23 : 8	ROW_COUNT	Number of rows (minus 1): "0": 1 row "1": 2 rows "2": 3 rows ... "65535": 65536 rows Default Value: 0

8.1.41 FLASHC_GEOMETRY (continued)

7 : 4	PAGE_SIZE_LOG2	Number of Bytes per page (log 2): "0": 1 Byte "1": 2 Bytes "2": 4 Bytes ... "15": 32768 Bytes The currently planned flash macros have a page size of either 256 Byte or 512 Byte, resulting in PAGE_SIZE_LOG2 settings of 8 and 9 respectively. Default Value: 0
3 : 0	WORD_SIZE_LOG2	Number of Bytes per word (log 2). A word is defined as the data that is read from the flash macro over the R interface with a single read access: "0": 1 Byte "1": 2 Bytes "2": 4 Bytes ... "7": 128 Bytes The currently planned flash macros have a word size of either 32-bit, 64-bit or 128-bit, resulting in WORD_SIZE_LOG2 settings of 2, 3 and 4 respectively. Default Value: 0

8.1.42 FLASHC_GEOMETRY_SUPERVISORY

Supervisory flash geometry

Address: 0x4025F010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	W				W			
Name	PAGE_SIZE_LOG2 [7:4]				WORD_SIZE_LOG2 [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	ROW_COUNT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	ROW_COUNT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	BANK_COUNT [31:24]							

Bits	Name	Description
31 : 24	BANK_COUNT	Number of banks (minus 1). BANK_COUNT is less or equal to GEOMETRY.BANK_COUNT. Default Value: 0
23 : 8	ROW_COUNT	Number of rows (minus 1). ROW_COUNT is typically less than GEOMETRY.ROW_COUNT Default Value: 0
7 : 4	PAGE_SIZE_LOG2	Number of Bytes per page (log 2). See GEOMETRY.PAGE_SIZE_LOG2. Typically, PAGE_-SIZE_LOG2 equals GEOMETRY.PAGE_SIZE_LOG2. Default Value: 0
3 : 0	WORD_SIZE_LOG2	Number of Bytes per word (log 2). See GEOMETRY.WORD_SIZE_LOG2. Typically, WORD_-SIZE_LOG2 equals GEOMETRY.WORD_SIZE_LOG2. Default Value: 0

8.1.43 FLASHC_TIMER_CTL

Timer control

Address: 0x4025F014

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							SCALE

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	None		RW	RW	RW
HW Access	RW0C	RW0C	RW0C	None		R	R	R
Name	TIMER_EN	ACLK_EN	PUMP_EN	None [28:27]		PRE_PROG_CSL	PRE_PROG	PUMP_CLOCK_SEL

Bits	Name	Description
31	TIMER_EN	Timer enable: '0': disabled '1': enabled. SW sets this field to '1' to start the timer. HW sets this field to '0' when the timer is expired. Default Value: 0
30	ACLK_EN	ACLK enable (generates a single cycle pulse for the FM): '0': disabled '1': enabled. SW set this field to '1' to generate a single cycle pulse. HW sets this field to '0' when the pulse is generated. Default Value: 0
29	PUMP_EN	Pump enable: '0': disabled '1': enabled (also requires FM_CTL.IF_SEL to be '1', this additional restriction is required to prevent non intentional clearing of the FM). SW sets this field to '1' to generate a single PE pulse. HW clears this field when timer is expired. Default Value: 0

8.1.43 FLASHC_TIMER_CTL (continued)

26	PRE_PROG_CSL	'0' CSL lines driven by CSL_DAC '1' CSL lines driven by VNEG_G Default Value: 1
25	PRE_PROG	'1' during pre-program operation Default Value: 0
24	PUMP_CLOCK_SEL	Pump clock select: '0': internal clock. '1': external clock. Default Value: 0
16	SCALE	Timer tick scale: '0': 1 microsecond. '1': 100 microseconds. Default Value: 0
15 : 0	PERIOD	Timer period in either microseconds (SCALE is '0') or 100's of microseconds (SCALE is '1') multiples. Default Value: 0

8.1.44 FLASHC_ANA_CTL0

Analog control 0

Address: 0x4025F018

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW		
HW Access	None					R		
Name	None [15:11]					CSLDAC [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None				RW	None		RW
HW Access	None				R	None		R
Name	None [31:28]				FLIP_AMUXBUS_AB	None [26:25]		VCC_SEL

Bits	Name	Description
27	FLIP_AMUXBUS_AB	Flips amuxbusa and amuxbusb '0': amuxbusa, amuxbusb '1': amuxbusb, amuxbusb Default Value: 0
24	VCC_SEL	Vcc select: '0': 1.2 V : LP reset value '1': 0.95 V: ULP reset value Note: the flash macro compiler has a configuration option that specifies the default/reset value of this field. Default Value: 0
10 : 8	CSLDAC	Trimming of common source line DAC. Default Value: 4

8.1.45 FLASHC_ANA_CTL1

Analog control 1

Address: 0x4025F01C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	MDAC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				PDAC [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None	RW	RW	RW	RW			
HW Access	None	R	R	R	R			
Name	None	RST_S-FT_HVPL	R_GRANT_CTL	VPROT_OVERRIDE	NDAC [27:24]			

Bits	Name	Description
30	RST_SFT_HVPL	'1': Page Latches Soft Reset Default Value: 0
29	R_GRANT_CTL	r_grant control: "0": r_grant normal functionality "1": forces r_grant LO synchronized on clk_r Default Value: 0
28	VPROT_OVERRIDE	'0': vprot = BG.vprot. '1': vprot = vcc Default Value: 0
27 : 24	NDAC	Trimming of negative pump output Voltage: Default Value: 6
19 : 16	PDAC	Trimming of positive pump output Voltage: Default Value: 6
7 : 0	MDAC	Trimming of the output margin Voltage as a function of Vpos and Vneg. Default Value: 0

8.1.46 FLASHC_GEOMETRY_GEN

N/A, DNU

Address: 0x4025F020

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R	R	R	None
HW Access	None				W	W	W	None
Name	None [7:4]				DNU_0x20_3	DNU_0x20_2	DNU_0x20_1	None

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	DNU_0x20_3	N/A Default Value: 0
2	DNU_0x20_2	N/A Default Value: 0
1	DNU_0x20_1	N/A Default Value: 0

8.1.47 FLASHC_TEST_CTL

Test mode control

Address: 0x4025F024

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			R				
Name	None [7:5]			TEST_MODE [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [15:12]				TM_DIS-NEG	TM_DIS-POS	TM_PE	PN_CTL

Bits	23	22	21	20	19	18	17	16
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [23:19]					EN-ABLE_OSC	CSL_DE-BUG	EN_-CLK_MON

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	UNSCRAM-BLE_WA	None [30:24]						

Bits	Name	Description
31	UNSCRAMBLE_WA	See BSN-242 memo '0': normal '1': disables the Word Address scrambling Default Value: 0
18	ENABLE_OSC	0': the oscillator enable logic has control over the internal oscillator '1': forces oscillator enable HI Default Value: 0
17	CSL_DEBUG	Engineering Debug Register Default Value: 0
16	EN_CLK_MON	1: enables the oscillator output monitor Default Value: 0
11	TM_DISNEG	Test mode negative pump disable Default Value: 0
10	TM_DISPOS	Test mode positive pump disable Default Value: 0

8.1.47 FLASHC_TEST_CTL (continued)

9	TM_PE	PUMP_EN override: Pump Enable =PUMP_EN | PE_TM Default Value: 0
8	PN_CTL	Positive/negative margin mode control: '0': negative margin control '1': positive margin control Default Value: 0
4 : 0	TEST_MODE	Test mode control: "0"-"31": TBD Default Value: 0

8.1.48 FLASHC_WAIT_CTL

Wiat State control

Address: 0x4025F028

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				WAIT_FM_MEM_RD [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				WAIT_FM_HV_RD [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None					RW		
HW Access	None					R		
Name	None [23:19]					WAIT_FM_HV_WR [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
18 : 16	WAIT_FM_HV_WR	Number of C interface wait cycles (on "clk_c") for a write to the high Voltage page latches. Default Value: 3
11 : 8	WAIT_FM_HV_RD	Number of C interface wait cycles (on "clk_c") for a read from the high Voltage page latches. Common for reading HV Page Latches and the DATA_COMP_RESULT bit Default Value: 11
3 : 0	WAIT_FM_MEM_RD	Number of C interface wait cycles (on "clk_c") for a read from the memory Default Value: 9

8.1.49 FLASHC_MONITOR_STATUS

Monitor Status

Address: 0x4025F02C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					R	R	None
HW Access	None					W	W	None
Name	None [7:3]					NEG_PUMP_VHI	POS_PUMP_VLO	None

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	NEG_PUMP_VHI	NEG pump VHI Default Value: 1
1	POS_PUMP_VLO	POS pump VLO Default Value: 0

8.1.50 FLASHC_SCRATCH_CTL

Scratch Control

Address: 0x4025F030

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DUMMY32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DUMMY32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DUMMY32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	DUMMY32 [31:24]							

Bits	Name	Description
31 : 0	DUMMY32	Scratchpad register fields. Provided for test purposes. Default Value: 0

8.1.51 FLASHC_HV_CTL

High voltage control

Address: 0x4025F034

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	TIMER_CLOCK_FREQ [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	TIMER_CLOCK_FREQ	Specifies the frequency in MHz of the timer clock "clk_t" as provide to the flash macro. E.g., if "4", the timer clock "clk_t" has a frequency of 4 MHz. Default Value: 50

8.1.52 FLASHC_ACLK_CTL

Aclk control

Address: 0x4025F038

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							W
HW Access	None							R
Name	None [7:1]							ACLK_GEN

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	ACLK_GEN	A write to this register generates a ACLK pulse for the flash macro (also requires FM_CTL.IF_-SEL to be '1'). Default Value: 0

8.1.53 FLASHC_INTR

Interrupt

Address: 0x4025F03C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1C
HW Access	None							RW1S
Name	None [7:1]							TIMER_EXPIRED

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	TIMER_EXPIRED	Set to '1', when event is detected. Write INTR field with '1', to clear bit. Write INTR_SET field with '1', to set bit. Default Value: 0

8.1.54 FLASHC_INTR_SET

Interrupt set

Address: 0x4025F040

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1S
HW Access	None							A
Name	None [7:1]							TIMER_EXPIRED

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	TIMER_EXPIRED	Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect). Default Value: 0

8.1.55 FLASHC_INTR_MASK

Interrupt mask

Address: 0x4025F044

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							TIMER_EXPIRED

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	TIMER_EXPIRED	Mask for corresponding field in INTR register. Default Value: 0

8.1.56 FLASHC_INTR_MASKED

Interrupt masked

Address: 0x4025F048

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							W
Name	None [7:1]							TIMER_EX-PIRED

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	TIMER_EXPIRED	Logical and of corresponding request and mask fields. Default Value: 0

8.1.57 FLASHC_FM_HV_DATA_ALL

Flash macro high Voltage page latches data (for all page latches)

Address: 0x4025F04C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	W							
HW Access	R							
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	W							
HW Access	R							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Write all high Voltage page latches with the same 32-bit data in a single write cycle Default Value: 0

8.1.58 FLASHC_CAL_CTL0

Cal control BG LO trim bits

Address: 0x4025F050

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW			RW				
HW Access	R			R				
Name	CDAC_LO_HV [7:5]			VCT_TRIM_LO_HV [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW				
HW Access	R			R				
Name	VBG_TC_TRIM_LO_HV [15:13]			VBG_TRIM_LO_HV [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				IPREF_TRIM_LO_HV [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	IPREF_TRIM_LO_HV	LO Bandgap IPTAT trim control. Default Value: 8
15 : 13	VBG_TC_TRIM_LO_HV	LO Bandgap Voltage Temperature Compensation trim control Default Value: 4
12 : 8	VBG_TRIM_LO_HV	LO Bandgap Voltage trim control. Default Value: 15
7 : 5	CDAC_LO_HV	LO Temperature compensated trim DAC. To control Vcstat slope for Vpos. Default Value: 4
4 : 0	VCT_TRIM_LO_HV	LO Bandgap Voltage Temperature Compensation trim control. Default Value: 15

8.1.59 FLASHC_CAL_CTL1

Cal control BG HI trim bits

Address: 0x4025F054

Retention: Retained

<table>
<tr><th>Bits</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td>SW Access</td><td colspan="3">RW</td><td colspan="5">RW</td></tr>
<tr><td>HW Access</td><td colspan="3">R</td><td colspan="5">R</td></tr>
<tr><td>Name</td><td colspan="3">CDAC_HI_HV [7:5]</td><td colspan="5">VCT_TRIM_HI_HV [4:0]</td></tr>
</table>

<table>
<tr><th>Bits</th><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th></tr>
<tr><td>SW Access</td><td colspan="3">RW</td><td colspan="5">RW</td></tr>
<tr><td>HW Access</td><td colspan="3">R</td><td colspan="5">R</td></tr>
<tr><td>Name</td><td colspan="3">VBG_TC_TRIM_HI_HV [15:13]</td><td colspan="5">VBG_TRIM_HI_HV [12:8]</td></tr>
</table>

<table>
<tr><th>Bits</th><th>23</th><th>22</th><th>21</th><th>20</th><th>19</th><th>18</th><th>17</th><th>16</th></tr>
<tr><td>SW Access</td><td colspan="4">None</td><td colspan="4">RW</td></tr>
<tr><td>HW Access</td><td colspan="4">None</td><td colspan="4">R</td></tr>
<tr><td>Name</td><td colspan="4">None [23:20]</td><td colspan="4">IPREF_TRIM_HI_HV [19:16]</td></tr>
</table>

<table>
<tr><th>Bits</th><th>31</th><th>30</th><th>29</th><th>28</th><th>27</th><th>26</th><th>25</th><th>24</th></tr>
<tr><td>SW Access</td><td colspan="8">None</td></tr>
<tr><td>HW Access</td><td colspan="8">None</td></tr>
<tr><td>Name</td><td colspan="8">None [31:24]</td></tr>
</table>

Bits	Name	Description
19 : 16	IPREF_TRIM_HI_HV	HI Bandgap IPTAT trim control. Default Value: 8
15 : 13	VBG_TC_TRIM_HI_HV	HI Bandgap Voltage Temperature Compensation trim control. Default Value: 4
12 : 8	VBG_TRIM_HI_HV	HI Bandgap Voltage trim control. Default Value: 15
7 : 5	CDAC_HI_HV	HI Temperature compensated trim DAC. To control Vcstat slope for Vpos. Default Value: 4
4 : 0	VCT_TRIM_HI_HV	HI Bandgap Voltage Temperature Compensation trim control. Default Value: 15

8.1.60 FLASHC_CAL_CTL2

Cal control BG LO ipref trim, ref sel, fm_active, turbo_ext

Address: 0x4025F058

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW			RW				
HW Access	R			R				
Name	ICREF_TC_TRIM_LO_HV [7:5]			ICREF_TRIM_LO_HV [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW				
HW Access	R			R				
Name	ICREF_TC_TRIM_HI_HV [15:13]			ICREF_TRIM_HI_HV [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [23:20]				TUR-BO_EX-T_HV	FM_AC-TIVE_HV	IREF_SEL_HV	VREF_SEL_HV

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19	TURBO_EXT_HV	0: turbo signal generated internally 1: turbo cleared by clk_pump_ext HI Default Value: 0
18	FM_ACTIVE_HV	0: No Action 1: Forces FM SYS in active mode Default Value: 0
17	IREF_SEL_HV	Current reference: '0': internal current reference '1': external current reference Default Value: 0
16	VREF_SEL_HV	Voltage reference: '0': internal bandgap reference '1': external voltage reference Default Value: 0
15 : 13	ICREF_TC_TRIM_HI_HV	HI Bandgap Current Temperature Compensation trim control. Default Value: 3

8.1.60 FLASHC_CAL_CTL2 (continued)

12 : 8	ICREF_TRIM_HI_HV	HI Bandgap Current trim control. Default Value: 16
7 : 5	ICREF_TC_TRIM_LO_HV	LO Bandgap Current Temperature Compensation trim control Default Value: 3
4 : 0	ICREF_TRIM_LO_HV	LO Bandgap Current trim control. Default Value: 16

8.1.61 FLASHC_CAL_CTL3

Cal control osc trim bits, idac, sdac, itim, bdac.

Address: 0x4025F05C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW			RW	RW			
HW Access	R			R	R			
Name	IDAC_HV [7:5]			OS-C_RANGE_TRIM_HV	OSC_TRIM_HV [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW				RW		RW
HW Access	R	R				R		R
Name	VDDHI_HV	ITIM_HV [14:11]				SDAC_HV [10:9]		IDAC_HV

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW	RW	RW	
HW Access	None				R	R	R	
Name	None [23:20]				BGHI_EN_HV	BGLO_EN_HV	TURBO_PULSEW_HV [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19	BGHI_EN_HV	HI Bandgap Enable Default Value: 0
18	BGLO_EN_HV	LO Bandgap Enable Default Value: 0
17 : 16	TURBO_PULSEW_HV	Turbo pulse width trim Default Value: 0
15	VDDHI_HV	0': vdd<2.3V '1': vdd>=2.3V Default Value: 1
14 : 11	ITIM_HV	Trimming of timing current Default Value: 4
10 : 9	SDAC_HV	Default Value: 2
8 : 5	IDAC_HV	Default Value: 8

4	OSC_RANGE_TRIM_HV	0: Oscillator High Frequency Range 1: Oscillator Low Frequency range Default Value: 0
3 : 0	OSC_TRIM_HV	Flash macro pump clock trim control. Default Value: 4

8.1.62 FLASHC_BOOKMARK

Bookmark register - keeps the current FW HV seq

Address: 0x4025F060

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	BOOKMARK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	BOOKMARK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	W							
HW Access	R							
Name	BOOKMARK [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	W							
HW Access	R							
Name	BOOKMARK [31:24]							

Bits	Name	Description
31 : 0	BOOKMARK	Used by FW. Keeps the Current HV cycle sequence Default Value: 0

8.1.63 FLASHC_RED_CTL01

Redundancy Control normal sectors 0,1

Address: 0x4025F080

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	RED_ADDR_0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							RED_EN_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	RED_ADDR_1 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							RW
HW Access	None							R
Name	None [31:25]							RED_EN_1

Bits	Name	Description
24	RED_EN_1	'1': Redundancy Enable for Sector 1 Default Value: 0
23 : 16	RED_ADDR_1	Bad Row Pair Address for Sector 1 Default Value: 0
8	RED_EN_0	'1': Redundancy Enable for Sector 0 Default Value: 0
7 : 0	RED_ADDR_0	Bad Row Pair Address for Sector 0 Default Value: 0

8.1.64 FLASHC_RED_CTL23

Redundancy Controll normal sectors 2,3

Address: 0x4025F084

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	RED_ADDR_2 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							RED_EN_2

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	RED_ADDR_3 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							RW
HW Access	None							R
Name	None [31:25]							RED_EN_3

Bits	Name	Description
24	RED_EN_3	1': Redundancy Enable for Sector 3 Default Value: 0
23 : 16	RED_ADDR_3	Bad Row Pair Address for Sector 3 Default Value: 0
8	RED_EN_2	1': Redundancy Enable for Sector 2 Default Value: 0
7 : 0	RED_ADDR_2	Bad Row Pair Address for Sector 2 Default Value: 0

8.1.65 FLASHC_RED_CTL45

Redundancy Controll normal sectors 4,5

Address: 0x4025F088

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	VLIM_TRIM_HV_0	DNU_45_6	FDIV_TRIM_HV_1	DNU_45_5	FDIV_TRIM_HV_0	DNU_45_3	REG_ACT_HV	DNU_45_1

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							DNU_45_8

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DNU_45_23_16 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	DNU_45_23_16	Not Used Default Value: 0
8	DNU_45_8	Not Used Default Value: 0
7	VLIM_TRIM_HV_0	'2b00' V2 = 650mV see vlim_trim_hv<1> value as well '2b01' V2 = 600mV '2b10' V2 = 750mV '2b11' V2 = 700mV Default Value: 0
6	DNU_45_6	Not Used Default Value: 0
5	FDIV_TRIM_HV_1	'2b00' F = 1MHz see fdiv_trim_hv<0> value as well '2b01' F = 0.5MHz '2b10' F = 2MHz '2b11' F = 4Mhz Default Value: 0

8.1.65 FLASHC_RED_CTL45 (continued)

4	DNU_45_5	Not Used Default Value: 0
3	FDIV_TRIM_HV_0	'2b00' F = 1MHz see fdiv_trim_hv<1> value as well '2b01' F = 0.5MHz '2b10' F = 2MHz '2b11' F = 4Mhz Default Value: 0
2	DNU_45_3	Not Used Default Value: 0
1	REG_ACT_HV	Forces the VBST regulator in active mode all the time Default Value: 0
0	DNU_45_1	Not Used Default Value: 0

8.1.66 FLASHC_RED_CTL67

Redundancy Controll normal sectors 6,7

Address: 0x4025F08C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	DNU_67_7	IPREF_TRI-MA_HI_HV	DNU_67_5	IP-REF_TC_HV	DNU_67_3	VPROT_ACT_HV	DNU_67_1	VLIM_TRIM_HV_1

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							IPREF_TRI-MA_LO_HV

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DNU_67_23_16 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	DNU_67_23_16	Not Used Default Value: 0
8	IPREF_TRIMA_LO_HV	Adds 200-300nA boost on IPREF_LO Default Value: 0
7	DNU_67_7	Not Used Default Value: 0
6	IPREF_TRIMA_HI_HV	Adds 200-300nA boost on IPREF_HI Default Value: 0
5	DNU_67_5	Not Used Default Value: 0
4	IPREF_TC_HV	Reduces the IPREF Tempco by not subtracting ICREF form IPREF - IPREF will be 1uA Default Value: 0
3	DNU_67_3	Not Used Default Value: 0

8.1.66 FLASHC_RED_CTL67 (continued)

2	VPROT_ACT_HV	Forces VPROT in active mode all the time Default Value: 0
1	DNU_67_1	Not Used Default Value: 0
0	VLIM_TRIM_HV_1	'2b00' V2 = 650mV see vlim_trim_hv<0> value as well '2b01' V2 = 600mV '2b10' V2 = 750mV '2b11' V2 = 700mV Default Value: 0

8.1.67 FLASHC_RED_CTL_SM01

Redundancy Controll special sectors 0,1

Address: 0x4025F090

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	RED_ADDR_SM0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							RED_EN_SM0

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	RED_ADDR_SM1 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None					RW
HW Access	R	R	None					R
Name	R_GRANT_EN	TRKD	None [29:25]					RED_EN_SM1

Bits	Name	Description
31	R_GRANT_EN	'0': r_grant handshake disabled, r_grant always 1. '1': r_grand handshake enabled Default Value: 0
30	TRKD	Sense Amp Control tracking delay Default Value: 0
24	RED_EN_SM1	Redundancy Enable for Special Sector 1 Default Value: 0
23 : 16	RED_ADDR_SM1	Bad Row Pair Address for Special Sector 1 Default Value: 0
8	RED_EN_SM0	Redundancy Enable for Special Sector 0 Default Value: 0
7 : 0	RED_ADDR_SM0	Bad Row Pair Address for Special Sector 0 Default Value: 0

8.1.68 FLASHC_TM_CMPR0

Do Not Use

Address: 0x4025F100

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							W
Name	None [7:1]							DATA_-COMP_RE-SULT

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	DATA_COMP_RESULT	The result of a comparison between the flash macro data output and the content of the high voltage page latches. The comparison result for a given column "Column_Number" is updated in this register field on a read to address: 0x100+4*Column_Number. The number of wait states is given by WAIT_CTL.WAIT_FM_HV_RD. '0': FALSE (not equal) '1': TRUE (equal) Default Value: 0

8.1.69 FLASHC_FM_HV_DATA0

Flash macro high Voltage page latches data

Address: 0x4025F800

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Four page latch Bytes (when writing to the page latches, it also requires FM_CTL.IF_SEL to be '1'). Note: the high Voltage page latches are readable for test mode functionality. Default Value: 0

8.1.70 FLASHC_FM_MEM_DATA0

Flash macro memory sense amplifier and column decoder data

Address: 0x4025FC00

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Sense amplifier and column multiplexer structure Bytes. The read data is dependent on FM_CTL.IF_SEL: - IF_SEL is "0": data as specified by the R interface address - IF_SEL is "1": data as specified by FM_MEM_ADDR and the offset of the accessed FM_MEM_-DATA register. Default Value: 0

9 System Resources Subsystem Registers

This section discusses the System Resources Subsystem (SRSS) registers. It lists all the registers in mapping tables, in address order.

9.1 Register Details

Register	Address	Description
PWR_CTL	0x40260000	Power Mode Control
PWR_HIBERNATE	0x40260004	HIBERNATE Mode Register
PWR_LVD_CTL	0x40260008	Low Voltage Detector (LVD) Configuration Register
PWR_BUCK_CTL	0x40260014	Buck Control Register
PWR_BUCK_CTL2	0x40260018	Buck Control Register 2
PWR_LVD_STATUS	0x4026001C	Low Voltage Detector (LVD) Status Register
PWR_HIB_DATA0	0x40260080	HIBERNATE Data Register
WDT_CTL	0x40260180	Watchdog Counter Control Register
WDT_CNT	0x40260184	Watchdog Counter Count Register
WDT_MATCH	0x40260188	Watchdog Counter Match Register
CLK_DSI_SELECT0	0x40260300	Clock DSI Select Register
CLK_DSI_SELECT1	0x40260304	Clock DSI Select Register. See CLK_DSI_SELECT0 for the details of bit fields.
CLK_DSI_SELECT2	0x40260308	Clock DSI Select Register. See CLK_DSI_SELECT0 for the details of bit fields.
CLK_DSI_SELECT3	0x4026030C	Clock DSI Select Register. See CLK_DSI_SELECT0 for the details of bit fields.
CLK_DSI_SELECT4	0x40260310	Clock DSI Select Register. See CLK_DSI_SELECT0 for the details of bit fields.
CLK_PATH_SELECT0	0x40260340	Clock Path Select Register
CLK_PATH_SELECT1	0x40260344	Clock Path Select Register. See CLK_PATH_SELECT0 for the details of bit fields.
CLK_PATH_SELECT2	0x40260348	Clock Path Select Register. See CLK_PATH_SELECT0 for the details of bit fields.
CLK_PATH_SELECT3	0x4026034C	Clock Path Select Register. See CLK_PATH_SELECT0 for the details of bit fields.
CLK_PATH_SELECT4	0x40260350	Clock Path Select Register. See CLK_PATH_SELECT0 for the details of bit fields.
CLK_ROOT_SELECT0	0x40260380	Clock Root Select Register
CLK_ROOT_SELECT1	0x40260384	Clock Root Select Register. See CLK_ROOT_SELECT0 for the details of bit fields.
CLK_ROOT_SELECT2	0x40260388	Clock Root Select Register. See CLK_ROOT_SELECT0 for the details of bit fields.
CLK_ROOT_SELECT3	0x4026038C	Clock Root Select Register. See CLK_ROOT_SELECT0 for the details of bit fields.
CLK_ROOT_SELECT4	0x40260390	Clock Root Select Register. See CLK_ROOT_SELECT0 for the details of bit fields.
CLK_SELECT	0x40260500	Clock selection register

Register	Address	Description
CLK_TIMER_CTL	0x40260504	Timer Clock Control Register
CLK_ILO_CONFIG	0x4026050C	ILO Configuration
CLK_IMO_CONFIG	0x40260510	IMO Configuration
CLK_OUTPUT_FAST	0x40260514	Fast Clock Output Select Register
CLK_OUTPUT_SLOW	0x40260518	Slow Clock Output Select Register
CLK_CAL_CNT1	0x4026051C	Clock Calibration Counter 1
CLK_CAL_CNT2	0x40260520	Clock Calibration Counter 2
CLK_ECO_CONFIG	0x4026052C	ECO Configuration Register
CLK_ECO_STATUS	0x40260530	ECO Status Register
CLK_PILO_CONFIG	0x4026053C	Precision ILO Configuration Register
CLK_FLL_CONFIG	0x40260580	FLL Configuration Register
CLK_FLL_CONFIG2	0x40260584	FLL Configuration Register 2
CLK_FLL_CONFIG3	0x40260588	FLL Configuration Register 3
CLK_FLL_CONFIG4	0x4026058C	FLL Configuration Register 4
CLK_FLL_STATUS	0x40260590	FLL Status Register
CLK_PLL_CONFIG0	0x40260600	PLL Configuration Register
CLK_PLL_STATUS0	0x40260640	PLL Status Register
SRSS_INTR	0x40260700	SRSS Interrupt Register
SRSS_INTR_SET	0x40260704	SRSS Interrupt Set Register
SRSS_INTR_MASK	0x40260708	SRSS Interrupt Mask Register
SRSS_INTR_MASKED	0x4026070C	SRSS Interrupt Masked Register
SRSS_INTR_CFG	0x40260710	SRSS Interrupt Configuration Register
RES_CAUSE	0x40260800	Reset Cause Observation Register
RES_CAUSE2	0x40260804	Reset Cause Observation Register 2
PWR_TRIM_REF_CTL	0x40267F00	Reference Trim Register
PWR_TRIM_BODOVP_CTL	0x40267F04	BOD/OVP Trim Register
CLK_TRIM_CCO_CTL	0x40267F08	CCO Trim Register
CLK_TRIM_CCO_CTL2	0x40267F0C	CCO Trim Register 2
PWR_TRIM_WAKE_CTL	0x40267F30	Wakeup Trim Register
PWR_TRIM_LVD_CTL	0x4026FF10	LVD Trim Register
CLK_TRIM_ILO_CTL	0x4026FF18	ILO Trim Register
PWR_TRIM_PWRSYS_CTL	0x4026FF1C	Power System Trim Register
CLK_TRIM_ECO_CTL	0x4026FF20	ECO Trim Register
CLK_TRIM_PILO_CTL	0x4026FF24	PILO Trim Register
CLK_TRIM_PILO_CTL2	0x4026FF28	PILO Trim Register 2
CLK_TRIM_PILO_CTL3	0x4026FF2C	PILO Trim Register 3

9.1.1 PWR_CTL

Power Mode Control

Address: 0x40260000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R	R	None		R	
HW Access	None		RW	RW	None		RW	
Name	None [7:6]		LP-M_READY	DEBUG_-SESSION	None [3:2]		POWER_MODE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	R	RW	None	
HW Access	A	A	A	A	RW	A	None	
Name	LIN-REG_DIS	NWELL_REG_DIS	RET_REG_DIS	DPS-LP_REG_DIS	VREF-BUF_OK	IREF_LP-MODE	None [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	R	RW	RW	RW	RW	RW	RW	RW
HW Access	RW	A	A	A	R	A	A	A
Name	ACT_REF_OK	ACT_REF_DIS	VREF-BUF_DIS	VREF-BUF_LP-MODE	PLL_LS_BYPASS	BGREF_LP MODE	POR-BOD_LP-MODE	LIN-REG_LP-MODE

Bits	Name	Description
31	ACT_REF_OK	Indicates that the normal mode of the Active Reference is ready. Default Value: 0
30	ACT_REF_DIS	Disables the Active Reference. Firmware must ensure that LPM_READY==1 and BGREF_LP-MODE==1 for at least 1us before disabling the Active Reference. When enabling the Active Reference, use ACT_REF_OK indicator to know when it is ready. This register is only reset by XRES/POR/BOD/HIBERNATE. 0: Active Reference is enabled 1: Active Reference is disabled Default Value: 0
29	VREFBUF_DIS	Disable the 800mV voltage reference buffer. Firmware should only disable the buffer when there is no connected circuit that is using it. SRSS circuits that require it are the PLL and ECO. A particular product may have circuits outside the SRSS that use the buffer. This register is only reset by XRES/POR/BOD/HIBERNATE. Default Value: 0

9.1.1 PWR_CTL (continued)

28	VREFBUF_LPMODE	Control the power mode of the 800mV voltage reference buffer. The value in this register is ignored and normal mode is used until LPM_READY==1. 0: Voltage Reference Buffer operates in normal mode. They work for vddd ramp rates of 100mV/us or less. This register is only reset by XRES/POR/BOD/HIBERNATE. 1: Voltage Reference Buffer operates in low power mode. Power supply rejection is reduced to save current, and they work for vddd ramp rates of 10mV/us or less. Default Value: 0
27	PLL_LS_BYPASS	Bypass level shifter inside the PLL. 0: Do not bypass the level shifter. This setting is ok for all operational modes and vccd target voltage. 1: Bypass the level shifter. This may reduce jitter on the PLL output clock, but can only be used when vccd is targeted to 1.1V nominal. Otherwise, it can result in clock degradation and static current. Default Value: 0
26	BGREF_LPMODE	Control the power mode of the Bandgap Voltage and Current References. This applies to voltage and current generation and is different than the reference voltage buffer. The value in this register is ignored and normal mode is used until LPM_READY==1. When lower power mode is used, the Active Reference circuit can be disabled to reduce current. Firmware is responsible to ensure ACT_REF_OK==1 before changing back to normal mode. This register is only reset by XRES/POR/BOD/HIBERNATE. 0: Active Bandgap Voltage and Current Reference operates in normal mode. They work for vddd ramp rates of 100mV/us or less. 1: Active Bandgap Voltage and Current Reference operates in low power mode. Power supply rejection is reduced to save current, and they work for vddd ramp rates of 10mV/us or less. The Active Reference may be disabled using ACT_REF_DIS=0. Default Value: 0
25	PORBOD_LPMODE	Control the power mode of the POR/BOD circuits. The value in this register is ignored and normal mode is used until LPM_READY==1. This register is only reset by XRES/POR/BOD/HIBERNATE. 0: POR/BOD circuits operate in normal mode. They work for vddd ramp rates of 100mV/us or less. 1: POR/BOD circuits operate in low power mode. Response time is reduced to save current, and they work for vddd ramp rates of 10mV/us or less. Default Value: 0
24	LINREG_LPMODE	Control the power mode of the Linear Regulator. The value in this register is ignored and normal mode is used until LPM_READY==1. This register is only reset by XRES/POR/BOD/HIBERNATE. 0: Linear Regulator operates in normal mode. Internal current consumption is 50uA and load current capability is 50mA to 300mA, depending on the number of regulator modules present in the product. 1: Linear Regulator operates in low power mode. Internal current consumption is 5uA and load current capability is 25mA. Firmware must ensure the current is kept within the limit. Default Value: 0
23	LINREG_DIS	Disable the linear Core Regulator. This is only legal when the on-chip buck regulator supplies vccd, but there is no hardware protection for this case. This register is only reset by XRES/POR/BOD/HIBERNATE. 0: Linear regulator is on. 1: Linear regulator is off. Default Value: 0

9.1.1 PWR_CTL (continued)

22	NWELL_REG_DIS	Disable the Nwell regulator. This is only legal when the on-chip buck regulator supplies vccd, but there is no hardware protection for this case. This register is only reset by XRES/POR/BOD/HIBERNATE. 0: Nwell Regulator is on. 1: Nwell Regulator is off. Default Value: 0
21	RET_REG_DIS	Disable the Retention regulator. This is only legal when the on-chip buck regulator supplies vccd, but there is no hardware protection for this case. This register is only reset by XRES/POR/BOD/HIBERNATE. 0: Retention Regulator is on. 1: Retention Regulator is off. Default Value: 0
20	DPSLP_REG_DIS	Disable the DeepSleep regulator. This is only legal when the on-chip buck regulator supplies vccd, but there is no hardware protection for this case. This register is only reset by XRES/POR/BOD/HIBERNATE. 0: DeepSleep Regulator is on. 1: DeepSleep Regulator is off. Default Value: 0
19	VREFBUF_OK	Indicates that the voltage reference buffer is ready. Due to synchronization delays, it may take two IMO clock cycles for hardware to clear this bit after asserting VREFBUF_DIS=1. Default Value: 0
18	IREF_LPMODE	Control the power mode of the reference current generator. The value in this register is ignored and normal mode is used until LPM_READY==1. This register is only reset by XRES/POR/BOD/HIBERNATE. 0: Current reference generator operates in normal mode. It works for vddd ramp rates of 100mV/us or less. 1: Current reference generator operates in low power mode. Response time is reduced to save current, and it works for vddd ramp rates of 10mV/us or less. Default Value: 0
5	LPM_READY	Indicates whether certain low power functions are ready. The low current circuits take longer to startup after XRES/POR/BOD/HIBERNATE wakeup than the normal mode circuits. HIBERNATE mode may be entered regardless of this bit. This register is only reset by XRES/POR/BOD/HIBERNATE. 0: If a low power circuit operation is requested, it will stay in its normal operating mode until it is ready. If DEEPSLEEP is requested by all processors WFI/WFE, the device will instead enter SLEEP. When low power circuits are ready, device will automatically enter the originally requested mode. 1: Normal operation. DEEPSLEEP and low power circuits operate as requested in other registers. Default Value: 0
4	DEBUG_SESSION	Indicates whether a debug session is active (CDBGPWRUPREQ signal is 1) Default Value: 0 **0x0: NO_SESSION :** No debug session active **0x1: SESSION_ACTIVE :** Debug session is active. Power modes behave differently to keep the debug session active.
1 : 0	POWER_MODE	Current power mode of the device. Note that this field cannot be read in all power modes on actual silicon. Default Value: 0

9.1.1 PWR_CTL (continued)

0x0: RESET :

System is resetting.

0x1: ACTIVE :

At least one CPU is running.

0x2: SLEEP :

No CPUs are running. Peripherals may be running.

0x3: DEEPSLEEP :

Main high-frequency clock is off; low speed clocks are available. Communication interface clocks may be present.

9.1.2 PWR_HIBERNATE

HIBERNATE Mode Register

Address: 0x40260004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	TOKEN [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	UNLOCK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW	RW	RW	None
HW Access	A				A	A	A	None
Name	POLARITY_HIBPIN [23:20]				MASK_HIB-WDT	MASK_HI-BALARM	FREEZE	None

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW1S	None		RW			
HW Access	A	R	None		A			
Name	HIBER-NATE	HIBER-NATE_DIS-ABLE	None [29:28]		MASK_HIBPIN [27:24]			

Bits	Name	Description
31	HIBERNATE	Firmware sets this bit to enter HIBERNATE mode. The system will enter HIBERNATE mode immediately after writing to this bit and will wakeup only in response to XRES or WAKEUP event. Both UNLOCK and FREEZE must have been set correctly in a previous write operations. Otherwise, it will not enter HIBERNATE. External supplies must have been stable for 250us before entering HIBERNATE mode. Default Value: 0
30	HIBERNATE_DISABLE	Hibernate disable bit. 0: Normal operation, HIBERNATE works as described 1: Further writes to this register are ignored Note: This bit is a write-once bit until the next reset. Avoid changing any other bits in this register while disabling HIBERNATE mode. Also, it is recommended to clear the UNLOCK code, if it was previously written.. Default Value: 0
27 : 24	MASK_HIBPIN	When set, HIBERNATE will wakeup if the corresponding pin input matches the POLARITY_HIBPIN setting. Each bit corresponds to one of the wakeup pins. Default Value: 0

9.1.2 PWR_HIBERNATE (continued)

23 : 20	POLARITY_HIBPIN	Each bit sets the active polarity of the corresponding wakeup pin. 0: Pin input of 0 will wakeup the part from HIBERNATE 1: Pin input of 1 will wakeup the part from HIBERNATE Default Value: 0
19	MASK_HIBWDT	When set, HIBERNATE will wakeup if WDT matches Default Value: 0
18	MASK_HIBALARM	When set, HIBERNATE will wakeup for a RTC interrupt Default Value: 0
17	FREEZE	Firmware sets this bit to freeze the configuration, mode and state of all GPIOs and SIOs in the system. When entering HIBERNATE mode, the first write instructs DEEPSLEEP peripherals that they cannot ignore the upcoming freeze command. This occurs even in the illegal condition where UNLOCK is not set. If UNLOCK and HIBERNATE are properly set, the IOs actually freeze on the second write. Default Value: 0
15 : 8	UNLOCK	This byte must be set to 0x3A for FREEZE or HIBERNATE fields to operate. Any other value in this register will cause FREEZE/HIBERNATE to have no effect, except as noted in the FREEZE description. Default Value: 0
7 : 0	TOKEN	Contains a 8-bit token that is retained through a HIBERNATE/WAKEUP sequence that can be used by firmware to differentiate WAKEUP from a general RESET event. Note that waking up from HIBERNATE using XRES will reset this register. Default Value: 0

9.1.3 PWR_LVD_CTL

Low Voltage Detector (LVD) Configuration Register

Address: 0x40260008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW			RW			
HW Access	A	R			R			
Name	HVL-VD1_EN	HVLVD1_SRCSEL [6:4]			HVLVD1_TRIPSEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	HVLVD1_EN	Enable HVLVD1 voltage monitor. When the LVD is enabled, it takes 20us for it to settle. There is no hardware stabilization counter, and it may falsely trigger during settling. It is recommended that firmware keep the interrupt masked for at least 8us, write a 1'b1 to the corresponding SRSS_INTR field to any falsely pended interrupt, and then optionally unmask the interrupt. After enabling, it is further recommended to read the related PWR_LVD_STATUS field, since the interrupt only triggers on edges. This bit is cleared (LVD is disabled) when entering DEEPSLEEP to prevent false interrupts during wakeup. Default Value: 0
6 : 4	HVLVD1_SRCSEL	Source selection for HVLVD1 Default Value: 0 **0x0: VDDD :** Select VDDD **0x1: AMUXBUSA :** Select AMUXBUSA (VDDD branch)

9.1.3 PWR_LVD_CTL (continued)

		0x2: RESERVED : Reserved. Connected AMUXBUSA (VDDD branch) **0x3: VDDIO :** Reserved. Selects VDDD. **0x4: AMUXBUSB :** Select AMUXBUSB (VDDD branch)
3 : 0	HVLVD1_TRIPSEL	Threshold selection for HVLVD1. Disable the LVD (HVLVD1_EN=0) before changing the threshold. 0: rise=1.225V (nom), fall=1.2V (nom) 1: rise=1.425V (nom), fall=1.4V (nom) 2: rise=1.625V (nom), fall=1.6V (nom) 3: rise=1.825V (nom), fall=1.8V (nom) 4: rise=2.025V (nom), fall=2V (nom) 5: rise=2.125V (nom), fall=2.1V (nom) 6: rise=2.225V (nom), fall=2.2V (nom) 7: rise=2.325V (nom), fall=2.3V (nom) 8: rise=2.425V (nom), fall=2.4V (nom) 9: rise=2.525V (nom), fall=2.5V (nom) 10: rise=2.625V (nom), fall=2.6V (nom) 11: rise=2.725V (nom), fall=2.7V (nom) 12: rise=2.825V (nom), fall=2.8V (nom) 13: rise=2.925V (nom), fall=2.9V (nom) 14: rise=3.025V (nom), fall=3.0V (nom) 15: rise=3.125V (nom), fall=3.1V (nom) Default Value: 0

9.1.4 PWR_BUCK_CTL

Buck Control Register

Address: 0x40260014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW		
HW Access	None					A		
Name	None [7:3]					BUCK_OUT1_SEL [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None					
HW Access	A	A	None					
Name	BUCK_OUT1_EN	BUCK_EN	None [29:24]					

Bits	Name	Description
31	BUCK_OUT1_EN	Enable for vccbuck1 output. The value in this register is ignored unless PWR_-BUCK_CTL.BUCK_EN==1. This register is only reset by XRES/POR/BOD/HIBERNATE. The regulator takes up to 600us to charge the external capacitor. If there is additional load current while charging, this will increase the startup time. The TRM specifies the required sequence when transitioning vccd from the LDO to SIMO Buck output #1. Default Value: 0
30	BUCK_EN	Master enable for buck converter. This register is only reset by XRES/POR/BOD/HIBERNATE. Default Value: 0

9.1.4 PWR_BUCK_CTL (continued)

2 : 0	BUCK_OUT1_SEL	Voltage output selection for vccbuck1 output. This register is only reset by XRES/POR/BOD/HIBERNATE. When increasing the voltage, it can take up to 200us for the output voltage to settle. When decreasing the voltage, the settling time depends on the load current. 0: 0.85V 1: 0.875V 2: 0.90V 3: 0.95V 4: 1.05V 5: 1.10V 6: 1.15V 7: 1.20V Default Value: 5

9.1.5 PWR_BUCK_CTL2

Buck Control Register 2

Address: 0x40260018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW		
HW Access	None					R		
Name	None [7:3]					BUCK_OUT2_SEL [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None					
HW Access	R	R	None					
Name	BUCK_OUT2_EN	BUCK_OUT2_HW_SEL	None [29:24]					

Bits	Name	Description
31	BUCK_OUT2_EN	Enable for vccbuck2 output. The value in this register is ignored unless PWR_-BUCK_CTL.BUCK_EN==1. The regulator takes up to 600us to charge the external capacitor. If there is additional load current while charging, this will increase the startup time. Default Value: 0
30	BUCK_OUT2_HW_SEL	Hardware control for vccbuck2 output. When this bit is set, the value in BUCK_OUT2_EN is ignored and a hardware signal is used instead. If the product has supporting hardware, it can directly control the enable signal for vccbuck2. The same charging time in BUCK_OUT2_EN applies. Default Value: 0

9.1.5 PWR_BUCK_CTL2 (continued)

2 : 0	BUCK_OUT2_SEL	Voltage output selection for vccbuck2 output. When increasing the voltage, it can take up to 200us for the output voltage to settle. When decreasing the voltage, the settling time depends on the load current. 0: 1.15V 1: 1.20V 2: 1.25V 3: 1.30V 4: 1.35V 5: 1.40V 6: 1.45V 7: 1.50V Default Value: 0

9.1.6 PWR_LVD_STATUS

Low Voltage Detector (LVD) Status Register

Address: 0x4026001C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							HVL-VD1_OK

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	HVLVD1_OK	HVLVD1 output. 0: below voltage threshold 1: above voltage threshold Default Value: 0

9.1.7 PWR_HIB_DATA0

HIBERNATE Data Register

Address: 0x40260080

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	HIB_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	HIB_DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	A							
Name	HIB_DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	A							
Name	HIB_DATA [31:24]							

Bits	Name	Description
31 : 0	HIB_DATA	Additional data that is retained through a HIBERNATE/WAKEUP sequence that can be used by firmware for any application-specific purpose. Note that waking up from HIBERNATE using XRES will reset this register. Default Value: 0

9.1.8 WDT_CTL

Watchdog Counter Control Register

Address: 0x40260180

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							A
Name	None [7:1]							WDT_EN

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None					
HW Access	A		None					
Name	WDT_LOCK [31:30]		None [29:24]					

Bits	Name	Description
31 : 30	WDT_LOCK	Prohibits writing to WDT_*, CLK_ILO_CONFIG, CLK_SELECT.LFCLK_SEL, and CLK_TRIM_ILO_CTL registers when not equal 0. Requires at least two different writes to unlock. A change in WDT_LOCK takes effect beginning with the next write cycle. Note that this field is 2 bits to force multiple writes only. It represents only a single write protect signal protecting all those registers at the same time. WDT will lock on any reset. This field is not retained during Deep Sleep or Hibernate mode, so the WDT will be locked after wakeup from these modes. Default Value: 3 **0x0: NO_CHG :** No effect **0x1: CLR0 :** Clears bit 0

9.1.8 WDT_CTL (continued)

		0x2: CLR1 : Clears bit 1 **0x3: SET01 :** Sets both bits 0 and 1
0	WDT_EN	Enable this watchdog timer. This field is retained during Deep Sleep and Hibernate modes. Even though the default value is 1, in most cases the Cortex-M0+ executing the SROM code will change the value of this bit to 0. So effectively the user code starts with the WDT disabled. Default Value: 1

9.1.9 WDT_CNT

Watchdog Counter Count Register

Address: 0x40260184

Retention: Retained

Bits	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SW Access	RW							
HW Access	A							
Name	COUNTER [7:0]							

Bits	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SW Access	RW							
HW Access	A							
Name	COUNTER [15:8]							

Bits	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	**Name**	**Description**
15 : 0	COUNTER	Current value of WDT Counter. The write feature of this register is for verification purposes, has no synchronization, and can only be applied when the WDT is off. When writing, the value is updated immediately in the WDT counter, but it will read back as the old value until this register resynchronizes just after the negative edge of ILO. Writes will be ignored if they occur when the WDT is enabled. Default Value: 0

9.1.10 WDT_MATCH

Watchdog Counter Match Register

Address: 0x40260188

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	MATCH [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	MATCH [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				A			
Name	None [23:20]				IGNORE_BITS [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	IGNORE_BITS	The number of MSB bits of the watchdog timer that are NOT checked against MATCH. This value provides control over the time-to-reset of the watchdog (which happens after 3 successive matches). Up to 12 MSB can be ignored. Settings >12 behave like a setting of 12. Default Value: 0
15 : 0	MATCH	Match value for Watchdog counter. Every time WDT_COUNTER reaches MATCH an interrupt is generated. Two unserviced interrupts will lead to a system reset (i.e. at the third match). Default Value: 4096

9.1.11 CLK_DSI_SELECT0

Clock DSI Select Register

Address: 0x40260300

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			R				
Name	None [7:5]			DSI_MUX [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4 : 0	DSI_MUX	Selects a DSI source or low frequency clock for use in a clock path. The output of this mux can be selected for clock PATH *using CLK_SELECT_PATH register. Using the output of this mux as HFCLK source will result in undefined behavior. It can be used to clocks to DSI or to the reference inputs of FLL/PLL, subject to the frequency limits of those circuits. This mux is not glitch free, so do not change the selection while it is an actively selected clock. Default Value: 0* **0x0: DSI_OUT0 :** DSI0 - dsi_out[0] **0x1: DSI_OUT1 :** DSI1 - dsi_out[1] **0x2: DSI_OUT2 :** DSI2 - dsi_out[2]

9.1.11 CLK_DSI_SELECT0 (continued)

0x3: DSI_OUT3 :

DSI3 - dsi_out[3]

0x4: DSI_OUT4 :

DSI4 - dsi_out[4]

0x5: DSI_OUT5 :

DSI5 - dsi_out[5]

0x6: DSI_OUT6 :

DSI6 - dsi_out[6]

0x7: DSI_OUT7 :

DSI7 - dsi_out[7]

0x8: DSI_OUT8 :

DSI8 - dsi_out[8]

0x9: DSI_OUT9 :

DSI9 - dsi_out[9]

0xa: DSI_OUT10 :

DSI10 - dsi_out[10]

0xb: DSI_OUT11 :

DSI11 - dsi_out[11]

0xc: DSI_OUT12 :

DSI12 - dsi_out[12]

0xd: DSI_OUT13 :

DSI13 - dsi_out[13]

0xe: DSI_OUT14 :

DSI14 - dsi_out[14]

9.1.11 CLK_DSI_SELECT0 (continued)

0xf: DSI_OUT15 :

DSI15 - dsi_out[15]

0x10: ILO :

ILO - Internal Low-speed Oscillator

0x11: WCO :

WCO - Watch-Crystal Oscillator

0x12: ALTLF :

ALTLF - Alternate Low-Frequency Clock

0x13: PILO :

PILO - Precision Internal Low-speed Oscillator

9.1.12 CLK_PATH_SELECT0

Clock Path Select Register

Address: 0x40260340

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW		
HW Access	None					R		
Name	None [7:3]					PATH_MUX [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2 : 0	PATH_MUX	Selects a source for clock PATH. *Note that not all products support all clock sources. Selecting a clock source that is not supported will result in undefined behavior. Default Value: 0* **0x0: IMO :** IMO - Internal R/C Oscillator **0x1: EXTCLK :** EXTCLK - External Clock Pin **0x2: ECO :** ECO - External-Crystal Oscillator **0x3: ALTHF :** ALTHF - Alternate High-Frequency clock input (product-specific clock)

9.1.12 CLK_PATH_SELECT0 (continued)

0x4: DSI_MUX :

DSI_MUX - Output of DSI mux for this path. Using a DSI source directly as root of HFCLK will result in undefined behavior.

9.1.13 CLK_ROOT_SELECT0

Clock Root Select Register

Address: 0x40260380

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW		RW			
HW Access	None		R		R			
Name	None [7:6]		ROOT_DIV [5:4]		ROOT_MUX [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	A	None						
Name	ENABLE	None [30:24]						

Bits	Name	Description
31	ENABLE	Enable for this clock root. All clock roots default to disabled (ENABLE==0) except HFCLK0, which cannot be disabled. Default Value: 0
5 : 4	ROOT_DIV	Selects predivider value for this clock root and DSI input. Default Value: 0 **0x0: NO_DIV :** Transparent mode, feed through selected clock source w/o dividing. **0x1: DIV_BY_2 :** Divide selected clock source by 2 **0x2: DIV_BY_4 :** Divide selected clock source by 4

9.1.13 CLK_ROOT_SELECT0 (continued)

		0x3: DIV_BY_8 : Divide selected clock source by 8
3 : 0	ROOT_MUX	Selects a clock path as the root of HFCLK and for SRSS DSI input . Use CLK_SELECT_PATH[i] to configure the desired path. Some paths may have FLL or PLL available (product-specific), and the control and bypass mux selections of these are in other registers. Configure the FLL using CLK_FLL_CONFIG register. Configure a PLL using the related CLK_PLL_CONFIG[k] register. Note that not all products support all clock sources. Selecting a clock source that is not supported will result in undefined behavior. Default Value: 0 **0x0: PATH0 :** Select PATH0 (can be configured for FLL) **0x1: PATH1 :** Select PATH1 (can be configured for PLL0, if available in the product) **0x2: PATH2 :** Select PATH2 (can be configured for PLL1, if available in the product) **0x3: PATH3 :** Select PATH3 (can be configured for PLL2, if available in the product) **0x4: PATH4 :** Select PATH4 (can be configured for PLL3, if available in the product) **0x5: PATH5 :** Select PATH5 (can be configured for PLL4, if available in the product) **0x6: PATH6 :** Select PATH6 (can be configured for PLL5, if available in the product) **0x7: PATH7 :** Select PATH7 (can be configured for PLL6, if available in the product) **0x8: PATH8 :** Select PATH8 (can be configured for PLL7, if available in the product) **0x9: PATH9 :** Select PATH9 (can be configured for PLL8, if available in the product)

9.1.13 CLK_ROOT_SELECT0 (continued)

0xa: PATH10 :

Select PATH10 (can be configured for PLL9, if available in the product)

0xb: PATH11 :

Select PATH11 (can be configured for PLL10, if available in the product)

0xc: PATH12 :

Select PATH12 (can be configured for PLL11, if available in the product)

0xd: PATH13 :

Select PATH13 (can be configured for PLL12, if available in the product)

0xe: PATH14 :

Select PATH14 (can be configured for PLL13, if available in the product)

0xf: PATH15 :

Select PATH15 (can be configured for PLL14, if available in the product)

9.1.14 CLK_SELECT

Clock selection register

Address: 0x40260500

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	
HW Access	None						A	
Name	None [7:2]						LFCLK_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW			RW			
HW Access	R	R			R			
Name	PUMP_EN-ABLE	PUMP_DIV [14:12]			PUMP_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15	PUMP_ENABLE	Enable the pump clock. PUMP_ENABLE and the PUMP_SEL mux are not glitch-free to minimize side-effects, avoid changing the PUMP_SEL and PUMP_DIV while changing PUMP_ENABLE. To change the settings, do the following: 1) If the pump clock is enabled, write PUMP_ENABLE=0 without changing PUMP_SEL and PUMP_DIV. 2) Change PUMP_SEL and PUMP_DIV to desired settings with PUMP_ENABLE=0. 3) Write PUMP_ENABLE=1 without changing PUMP_SEL and PUMP_DIV. Default Value: 0
14 : 12	PUMP_DIV	Division ratio for PUMPCLK. Uses selected PUMP_SEL clock as the source. Default Value: 0 **0x0: NO_DIV :** Transparent mode, feed through selected clock source w/o dividing. **0x1: DIV_BY_2 :** Divide selected clock source by 2

9.1.14 CLK_SELECT (continued)

		0x2: DIV_BY_4 : Divide selected clock source by 4 **0x3: DIV_BY_8 :** Divide selected clock source by 8 **0x4: DIV_BY_16 :** Divide selected clock source by 16
11 : 8	PUMP_SEL	Selects clock PATH, where k=PUMP_SEL. The output of this mux goes to the PUMP_DIV to make PUMPCLK Each product has a specific number of available clock paths. Selecting a path that is not implemented on a product will result in undefined behavior. Note that this is not a glitch free mux. Default Value: 0
1 : 0	LFCLK_SEL	Select source for LFCLK. Note that not all products support all clock sources. Selecting a clock source that is not supported will result in undefined behavior. Writes to this field are ignored unless the WDT is unlocked using WDT_LOCK register. Default Value: 0 **0x0: ILO :** ILO - Internal Low-speed Oscillator **0x1: WCO :** WCO - Watch-Crystal Oscillator. Requires Backup domain to be present and properly configured (including external watch crystal, if used). **0x2: ALTLF :** ALTLF - Alternate Low-Frequency Clock. Capability is product-specific **0x3: PILO :** PILO - Precision ILO. If present, it works in DEEPSLEEP and higher modes. Does not work in HIBERNATE mode.

9.1.15 CLK_TIMER_CTL

Timer Clock Control Register

Address: 0x40260504

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							TIMER_-SEL

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						TIMER_HF0_DIV [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	TIMER_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	ENABLE	None [30:24]						

Bits	Name	Description
31	ENABLE	Enable for TIMERCLK. 0: TIMERCLK is off 1: TIMERCLK is enabled Default Value: 0
23 : 16	TIMER_DIV	Divide selected timer clock source by (1+TIMER_DIV). The output of this divider is TIMERCLK Allows for integer divisions in the range [1, 256]. Do not change this setting while the timer is enabled. Default Value: 7
9 : 8	TIMER_HF0_DIV	Predivider used when HF0_DIV is selected in TIMER_SEL. If HFCLK0 frequency is less than 100MHz and has approximately 50% duty cycle, then no division is required (NO_DIV). Otherwise, select a divide ratio of 2, 4, or 8 before selected HF0_DIV as the timer clock. Default Value: 0 **0x0: NO_DIV :** Transparent mode, feed through selected clock source w/o dividing or correcting duty cycle.

9.1.15 CLK_TIMER_CTL (continued)

		0x1: DIV_BY_2 : Divide HFCLK0 by 2. **0x2: DIV_BY_4 :** Divide HFCLK0 by 4. **0x3: DIV_BY_8 :** Divide HFCLK0 by 8.
0	TIMER_SEL	Select source for TIMERCLK. The output of this mux can be further divided using TIMER_DIV. Default Value: 0 **0x0: IMO :** IMO - Internal Main Oscillator **0x1: HF0_DIV :** Select the output of the predivider configured by TIMER_HF0_DIV.

9.1.16 CLK_ILO_CONFIG

ILO Configuration

Address: 0x4026050C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							A
Name	None [7:1]							ILO_BACK-UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	A	None						
Name	ENABLE	None [30:24]						

Bits	Name	Description
31	ENABLE	Master enable for ILO. Writes to this field are ignored unless the WDT is unlocked using WDT_LOCK register. After enabling, it takes at most two cycles to reach the accuracy spec. Default Value: 1
0	ILO_BACKUP	If backup domain is present on this product, this register indicates that ILO should stay enabled for use by backup domain during XRES, HIBERNATE mode, and through power-related resets like BOD on VDDD/VCCD. Writes to this field are ignored unless the WDT is unlocked using WDT_LOCK register. 0: ILO turns off at XRES/BOD event or HIBERNATE entry. 1: ILO remains on if backup domain is present and powered even for XRES/BOD or HIBERNATE entry. Default Value: 0

9.1.17 CLK_IMO_CONFIG

IMO Configuration

Address: 0x40260510

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	ENABLE	None						

Bits	Name	Description
31	ENABLE	Master enable for IMO oscillator. This bit must be high at all times for all functions to work properly. Hardware will automatically disable the IMO during HIBERNATE and XRES. It will automatically disable during DEEPSLEEP if DPSLP_ENABLE==0. Default Value: 1

9.1.18 CLK_OUTPUT_FAST

Fast Clock Output Select Register

Address: 0x40260514

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PATH_SEL0 [7:4]				FAST_SEL0 [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				HFCLK_SEL0 [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW			
HW Access	R				R			
Name	PATH_SEL1 [23:20]				FAST_SEL1 [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None				RW			
HW Access	None				R			
Name	None [31:28]				HFCLK_SEL1 [27:24]			

Bits	Name	Description
27 : 24	HFCLK_SEL1	Selects a HFCLK tree for use in fast clock output #1 logic Default Value: 0
23 : 20	PATH_SEL1	Selects a clock path to use in fast clock output #1 logic. 0: FLL output 1-15: PLL output on path1-path15 (if available) Default Value: 0
19 : 16	FAST_SEL1	Select signal for fast clock output #1 Default Value: 0 **0x0: NC :** Disabled - output is 0. For power savings, clocks are blocked before entering any muxes, including PATH_SEL1 and HFCLK_SEL1. **0x1: ECO :** External Crystal Oscillator (ECO)

9.1.18 CLK_OUTPUT_FAST (continued)

		0x2: EXTCLK : External clock input (EXTCLK) **0x3: ALTHF :** Alternate High-Frequency (ALTHF) clock input to SRSS **0x4: TIMERCLK :** Timer clock. It is grouped with the fast clocks because it may be a gated version of a fast clock, and therefore may have a short high pulse. **0x5: PATH_SEL1 :** Selects the clock path chosen by PATH_SEL1 field **0x6: HFCLK_SEL1 :** Selects the output of the HFCLK_SEL1 mux **0x7: SLOW_SEL1 :** Selects the output of CLK_OUTPUT_SLOW.SLOW_SEL1
11 : 8	HFCLK_SEL0	Selects a HFCLK tree for use in fast clock output #0 Default Value: 0
7 : 4	PATH_SEL0	Selects a clock path to use in fast clock output #0 logic. 0: FLL output 1-15: PLL output on path1-path15 (if available) Default Value: 0
3 : 0	FAST_SEL0	Select signal for fast clock output #0 Default Value: 0 **0x0: NC :** Disabled - output is 0. For power savings, clocks are blocked before entering any muxes, including PATH_SEL0 and HFCLK_SEL0. **0x1: ECO :** External Crystal Oscillator (ECO) **0x2: EXTCLK :** External clock input (EXTCLK) **0x3: ALTHF :** Alternate High-Frequency (ALTHF) clock input to SRSS

9.1.18 CLK_OUTPUT_FAST (continued)

0x4: TIMERCLK :

Timer clock. It is grouped with the fast clocks because it may be a gated version of a fast clock, and therefore may have a short high pulse.

0x5: PATH_SEL0 :

Selects the clock path chosen by PATH_SEL0 field

0x6: HFCLK_SEL0 :

Selects the output of the HFCLK_SEL0 mux

0x7: SLOW_SEL0 :

Selects the output of CLK_OUTPUT_SLOW.SLOW_SEL0

9.1.19 CLK_OUTPUT_SLOW

Slow Clock Output Select Register

Address: 0x40260518

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	SLOW_SEL1 [7:4]				SLOW_SEL0 [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	SLOW_SEL1	Select signal for slow clock output #1 Default Value: 0 **0x0: NC :** Disabled - output is 0. For power savings, clocks are blocked before entering any muxes. **0x1: ILO :** Internal Low Speed Oscillator (ILO) **0x2: WCO :** Watch-Crystal Oscillator (WCO) **0x3: BAK :** Root of the Backup domain clock tree (BAK)

9.1.19 CLK_OUTPUT_SLOW (continued)

		0x4: ALTLF : Alternate low-frequency clock input to SRSS (ALTLF) **0x5: LFCLK :** Root of the low-speed clock tree (LFCLK) **0x6: IMO :** Internal Main Oscillator (IMO). This is grouped with the slow clocks so it can be observed during DEEPSLEEP entry/exit. **0x7: SLPCTRL :** Sleep Controller clock (SLPCTRL). This is grouped with the slow clocks so it can be observed during DEEPSLEEP entry/exit. **0x8: PILO :** Precision Internal Low Speed Oscillator (PILO)
3 : 0	SLOW_SEL0	Select signal for slow clock output #0 Default Value: 0 **0x0: NC :** Disabled - output is 0. For power savings, clocks are blocked before entering any muxes. **0x1: ILO :** Internal Low Speed Oscillator (ILO) **0x2: WCO :** Watch-Crystal Oscillator (WCO) **0x3: BAK :** Root of the Backup domain clock tree (BAK) **0x4: ALTLF :** Alternate low-frequency clock input to SRSS (ALTLF) **0x5: LFCLK :** Root of the low-speed clock tree (LFCLK)

9.1.19 CLK_OUTPUT_SLOW (continued)

0x6: IMO :

Internal Main Oscillator (IMO). This is grouped with the slow clocks so it can be observed during DEEPSLEEP entry/exit.

0x7: SLPCTRL :

Sleep Controller clock (SLPCTRL). This is grouped with the slow clocks so it can be observed during DEEPSLEEP entry/exit.

0x8: PILO :

Precision Internal Low Speed Oscillator (PILO)

9.1.20 CLK_CAL_CNT1

Clock Calibration Counter 1

Address: 0x4026051C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	CAL_COUNTER1 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	CAL_COUNTER1 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	A							
Name	CAL_COUNTER1 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	CAL_COUNTER_DONE	None [30:24]						

Bits	Name	Description
31	CAL_COUNTER_DONE	Status bit indicating that the internal counter #1 is finished counting and CLK_-CAL_CNT2.COUNTER stopped counting up Default Value: 1
23 : 0	CAL_COUNTER1	Down-counter clocked on fast clock output #0 (see CLK_OUTPUT_FAST). This register always reads as zero. Counting starts internally when this register is written with a nonzero value. CAL_COUNTER_DONE goes immediately low to indicate that the counter has started and will be asserted when the counters are done. Do not write this field unless CAL_COUNTER_-DONE==1. Both clocks must be running or the measurement will not complete. A stalled counter can be recovered by selecting valid clocks, waiting until the measurement completes, and dis-carding the first result. Default Value: 0

9.1.21 CLK_CAL_CNT2

Clock Calibration Counter 2

Address: 0x40260520

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	CAL_COUNTER2 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	CAL_COUNTER2 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	CAL_COUNTER2 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 0	CAL_COUNTER2	Up-counter clocked on fast clock output #1 (see CLK_OUTPUT_FAST). When CLK_-CAL_CNT1.CAL_COUNTER_DONE==1, the counter is stopped and can be read by SW. Do not read this value unless CAL_COUNTER_DONE==1. The expected final value is related to the ratio of clock frequencies used for the two counters and the value loaded into counter 1: CLK_-CAL_CNT2.COUNTER=(F_cnt2/F_cnt1)*(CLK_CAL_CNT1.COUNTER) Default Value: 0

9.1.22 CLK_ECO_CONFIG

ECO Configuration Register

Address: 0x4026052C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	None
HW Access	None						R	None
Name	None [7:2]						AGC_EN	None

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	ECO_EN	None [30:24]						

Bits	Name	Description
31	ECO_EN	Master enable for ECO oscillator. Default Value: 0
1	AGC_EN	Automatic Gain Control (AGC) enable. When set, the oscillation amplitude is controlled to the level selected by ECO_TRIM0.ATRIM. When low, the amplitude is not explicitly controlled and can be as high as the vddd supply. WARNING: use care when disabling AGC because driving a crystal beyond its rated limit can permanently damage the crystal. Default Value: 1

9.1.23 CLK_ECO_STATUS

ECO Status Register

Address: 0x40260530

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						W	W
Name	None [7:2]						ECO_READY	ECO_OK

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	ECO_READY	Indicates the ECO internal oscillator circuit has had enough time to fully stabilize. This is the output of a counter since ECO was enabled, and it does not check the ECO output. It is recommended to also confirm ECO_OK==1. Default Value: 0
0	ECO_OK	Indicates the ECO internal oscillator circuit has sufficient amplitude. It may not meet the PPM accuracy or duty cycle spec. Default Value: 0

9.1.24 CLK_PILO_CONFIG

Precision ILO Configuration Register

Address: 0x4026053C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	PILO_FFREQ [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						PILO_FFREQ [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	None				
HW Access	R	R	R	None				
Name	PILO_EN	PILO_RE-SET_N	PILO_-CLK_EN	None [28:24]				

Bits	Name	Description
31	PILO_EN	Enable PILO. When enabling PILO, set PILO_EN=1, wait 1ms, then PILO_RESET_N=1 and PI-LO_CLK_EN=1. When disabling PILO, clear PILO_EN=0, PILO_RESET_N=0, and PLO_-CLK_EN=0 in the same write cycle. Default Value: 0
30	PILO_RESET_N	Reset the PILO. See PILO_EN field for required sequencing. Default Value: 0
29	PILO_CLK_EN	Enable the PILO clock output. See PILO_EN field for required sequencing. Default Value: 0
9 : 0	PILO_FFREQ	Fine frequency trim allowing +/-250ppm accuracy with periodic calibration. The nominal step size of the LSB is 8Hz. Default Value: 128

9.1.25 CLK_FLL_CONFIG

FLL Configuration Register

Address: 0x40260580

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	FLL_MULT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	FLL_MULT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	
HW Access	None						R	
Name	None [23:18]						FLL_MULT [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						RW
HW Access	R	None						R
Name	FLL_EN-ABLE	None [30:25]						FLL_OUT-PUT_DIV

Bits	Name	Description
31	FLL_ENABLE	Master enable for FLL. The FLL requires firmware sequencing when enabling, disabling, and entering/exiting DEEPSLEEP. To enable the FLL, first enable the CCO by writing CLK_FLL_CONFIG4.CCO_ENABLE=1 and wait until CLK_FLL_STATUS.CCO_READY==1. Next, ensure the reference clock has stabilized and CLK_FLL_CONFIG3.BYPASS_SEL=FLL_REF. Next, write FLL_ENABLE=1 and wait until CLK_FLL_STATUS.LOCKED==1. Finally, write CLK_FLL_CONFIG3.BYPASS_SEL=FLL_OUT to switch to the FLL output. It takes seven reference clock cycles plus four FLL output cycles to switch to the FLL output. Do not disable the FLL before this time completes. To disable the FLL, write CLK_FLL_CONFIG3.BYPASS_SEL=FLL_REF and (optionally) read the same register to ensure the write completes. Then, wait at least seven FLL reference clock cycles before disabling it with FLL_ENABLE=0. Lastly, disable the CCO by writing CLK_FLL_CONFIG4.CCO_ENABLE=0. Before entering DEEPSLEEP, either disable the FLL using above sequence or use the following procedure to deselect/select it before/after DEEPSLEEP. Before entering DEEPSLEEP, write CLK_FLL_CONFIG3.BYPASS_SEL=FLL_REF to change the FLL to use its reference clock. After DEEPSLEEP wakeup, wait until CLK_FLL_STATUS.LOCKED==1 and then write CLK_FLL_CONFIG3.BYPASS_SEL=FLL_OUT to switch to the FLL output. 0: Block is powered off 1: Block is powered on Default Value: 0

9.1.25 CLK_FLL_CONFIG (continued)

24	FLL_OUTPUT_DIV	Control bits for Output divider. Set the divide value before enabling the FLL, and do not change it while FLL is enabled. 0: no division 1: divide by 2 Default Value: 1
17 : 0	FLL_MULT	Multiplier to determine CCO frequency in multiples of the frequency of the selected reference clock (Fref). Ffll = (FLL_MULT) * (Fref / REFERENCE_DIV) / (OUTPUT_DIV+1) Default Value: 0

9.1.26 CLK_FLL_CONFIG2

FLL Configuration Register 2

Address: 0x40260584

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	FLL_REF_DIV [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW				
HW Access	None			R				
Name	None [15:13]			FLL_REF_DIV [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	LOCK_TOL [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							RW
HW Access	None							R
Name	None [31:25]							LOCK_TOL

Bits	Name	Description
24 : 16	LOCK_TOL	Lock tolerance sets the error threshold for when the FLL output is considered locked to the reference input. A high tolerance can be used to lock more quickly or to track a less accurate source. The tolerance should be set so that the FLL does not unlock under normal conditions. The tolerance is the allowed difference between the count value for the ideal formula and the measured value. 0: tolerate error of 1 count value 1: tolerate error of 2 count values ... 511: tolerate error of 512 count values Default Value: 2
12 : 0	FLL_REF_DIV	Control bits for reference divider. Set the divide value before enabling the FLL, and do not change it while FLL is enabled. 0: illegal (undefined behavior) 1: divide by 1 ... 8191: divide by 8191 Default Value: 1

9.1.27 CLK_FLL_CONFIG3

FLL Configuration Register 3

Address: 0x40260588

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	FLL_LF_PGAIN [7:4]				FLL_LF_IGAIN [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	SETTLING_COUNT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW				
HW Access	None			R				
Name	None [23:21]			SETTLING_COUNT [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	None		RW		None			
HW Access	None		R		None			
Name	None [31:30]		BYPASS_SEL [29:28]		None [27:24]			

Bits	Name	Description
29 : 28	BYPASS_SEL	Bypass mux located just after FLL output. See FLL_ENABLE description for instructions on how to use this field when enabling/disabling the FLL. Default Value: 0 **0x0: AUTO :** Reserved **0x1: AUTO1 :** Reserved **0x2: FLL_REF :** Select FLL reference input (bypass mode). Ignores lock indicator

9.1.27 CLK_FLL_CONFIG3 (continued)

		0x3: FLL_OUT : Select FLL output. Ignores lock indicator.
20 : 8	SETTLING_COUNT	Number of undivided reference clock cycles to wait after changing the CCO trim until the loop measurement restarts. A delay allows the CCO output to settle and gives a more accurate measurement. The default is tuned to an 8MHz reference clock since the IMO is expected to be the most common use case. 0: no settling time 1: wait one reference clock cycle ... 8191: wait 8191 reference clock cycles Default Value: 40
7 : 4	FLL_LF_PGAIN	FLL Loop Filter Gain Setting #2. The proportional gain is the sum of FLL_LF_IGAIN and FLL_LF_PGAIN. 0: 1/256 1: 1/128 2: 1/64 3: 1/32 4: 1/16 5: 1/8 6: 1/4 7: 1/2 8: 1.0 9: 2.0 10: 4.0 11: 8.0 >=12: illegal Default Value: 0
3 : 0	FLL_LF_IGAIN	FLL Loop Filter Gain Setting #1. The proportional gain is the sum of FLL_LF_IGAIN and FLL_LF_PGAIN. 0: 1/256 1: 1/128 2: 1/64 3: 1/32 4: 1/16 5: 1/8 6: 1/4 7: 1/2 8: 1.0 9: 2.0 10: 4.0 11: 8.0 >=12: illegal Default Value: 0

9.1.28 CLK_FLL_CONFIG4

FLL Configuration Register 4

Address: 0x4026058C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CCO_LIMIT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW		
HW Access	None					R		
Name	None [15:11]					CCO_RANGE [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	CCO_FREQ [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None					RW
HW Access	R	R	None					RW
Name	CCO_EN-ABLE	CCO_HW_UP-DATE_DIS	None [29:25]					CCO_-FREQ

Bits	Name	Description
31	CCO_ENABLE	Enable the CCO. It is required to enable the CCO before using the FLL. 0: Block is powered off 1: Block is powered on Default Value: 0
30	CCO_HW_UPDATE_DIS	Disable CCO frequency update by FLL hardware 0: Hardware update of CCO settings is allowed. Use this setting for normal FLL operation. 1: Hardware update of CCO settings is disabled. Use this setting for open-loop FLL operation. Default Value: 0
24 : 16	CCO_FREQ	CCO frequency code. This is updated by HW when the FLL is enabled. It can be manually updated to use the CCO in an open loop configuration. The meaning of each frequency code depends on the range. Default Value: 0
10 : 8	CCO_RANGE	Frequency range of CCO Default Value: 0

9.1.28 CLK_FLL_CONFIG4 (continued)

		0x0: RANGE0 : Target frequency is in range [48, 64) MHz **0x1: RANGE1 :** Target frequency is in range [64, 85) MHz **0x2: RANGE2 :** Target frequency is in range [85, 113) MHz **0x3: RANGE3 :** Target frequency is in range [113, 150) MHz **0x4: RANGE4 :** Target frequency is in range [150, 200] MHz
7 : 0	CCO_LIMIT	Maximum CCO offset allowed (used to prevent FLL dynamics from selecting an CCO frequency that the logic cannot support) Default Value: 255

9.1.29 CLK_FLL_STATUS

FLL Status Register

Address: 0x40260590

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					R	RW1C	R
HW Access	None					RW	A	W
Name	None [7:3]					CCO_READY	UNLOCK_OCCURRED	LOCKED

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	CCO_READY	This indicates that the CCO is internally settled and ready to use. Default Value: 0
1	UNLOCK_OCCURRED	Reserved. Do not use. Default Value: 0
0	LOCKED	FLL Lock Indicator. LOCKED is high when FLL is within CLK_FLL_CONFIG2.LOCK_TOL. If FLL is outside LOCK_TOL, LOCKED goes low. Note that this can happen during normal operation, if FLL needs to recalculate due to a change in the reference clock, change in voltage, or change in temperature. Default Value: 0

9.1.30 CLK_PLL_CONFIG0

PLL Configuration Register

Address: 0x40260600

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW						
HW Access	None	R						
Name	None	FEEDBACK_DIV [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW				
HW Access	None			R				
Name	None [15:13]			REFERENCE_DIV [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW				
HW Access	None			R				
Name	None [23:21]			OUTPUT_DIV [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None	RW		RW	None		
HW Access	R	None	R		R	None		
Name	ENABLE	None	BYPASS_SEL [29:28]		PLL_LF_-MODE	None [26:24]		

Bits	Name	Description
31	ENABLE	Master enable for PLL. Setup FEEDBACK_DIV, REFERENCE_DIV, and OUTPUT_DIV at least one cycle before setting ENABLE=1. To disable the PLL, first deselect it using .BYPASS_-SEL=PLL_REF, wait at least six PLL clock cycles, and then disable it with .ENABLE=0. Fpll = (FEEDBACK_DIV) * (Fref / REFERENCE_DIV) / (OUTPUT_DIV) 0: Block is disabled 1: Block is enabled Default Value: 0
29 : 28	BYPASS_SEL	Bypass mux located just after PLL output. This selection is glitch-free and can be changed while the PLL is running. Default Value: 0 **0x0: AUTO :** Automatic using lock indicator. When unlocked, automatically selects PLL reference input (bypass mode). When locked, automatically selects PLL output.

9.1.30 CLK_PLL_CONFIG0 (continued)

		0x1: AUTO1 : Same as AUTO **0x2: PLL_REF :** Select PLL reference input (bypass mode). Ignores lock indicator **0x3: PLL_OUT :** Select PLL output. Ignores lock indicator.
27	PLL_LF_MODE	VCO frequency range selection. Configure this bit according to the targeted VCO frequency. Do not change this setting while the PLL is enabled. 0: VCO frequency is [200MHz, 400MHz] 1: VCO frequency is [170MHz, 200MHz) Default Value: 0
20 : 16	OUTPUT_DIV	Control bits for Output divider. Set the divide value before enabling the PLL, and do not change it while PLL is enabled. 0: illegal (undefined behavior) 1: illegal (undefined behavior) 2: divide by 2. Suitable for direct usage as HFCLK source. ... 16: divide by 16. Suitable for direct usage as HFCLK source. >16: illegal (undefined behavior) Default Value: 2
12 : 8	REFERENCE_DIV	Control bits for reference divider. Set the divide value before enabling the PLL, and do not change it while PLL is enabled. 0: illegal (undefined behavior) 1: divide by 1 ... 20: divide by 20 others: illegal (undefined behavior) Default Value: 1
6 : 0	FEEDBACK_DIV	Control bits for feedback divider. Set the divide value before enabling the PLL, and do not change it while PLL is enabled. 0-21: illegal (undefined behavior) 22: divide by 22 ... 112: divide by 112 >112: illegal (undefined behavior) Default Value: 22

9.1.31 CLK_PLL_STATUS0

PLL Status Register

Address: 0x40260640

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1C	R
HW Access	None						A	W
Name	None [7:2]						UN-LOCK_OC-CURRED	LOCKED

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	UNLOCK_OCCURRED	This bit sets whenever the PLL Lock bit goes low, and stays set until cleared by firmware. Default Value: 0
0	LOCKED	PLL Lock Indicator Default Value: 0

9.1.32 SRSS_INTR

SRSS Interrupt Register

Address: 0x40260700

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW1C	None			RW1C	RW1C
HW Access	None		A	None			A	A
Name	None [7:6]		CLK_CAL	None [4:2]			HVLVD1	WDT_-MATCH

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	CLK_CAL	Clock calibration counter is done. This field is reset during DEEPSLEEP mode. Default Value: 0
1	HVLVD1	Interrupt for low voltage detector HVLVD1 Default Value: 0
0	WDT_MATCH	WDT Interrupt Request. This bit is set each time WDT_COUNTR==WDT_MATCH. W1C also feeds the watch dog. Missing 2 interrupts in a row will generate a reset. Due to internal synchronization, it takes 2 SYSCLK cycles to update after a W1C. Default Value: 0

9.1.33 SRSS_INTR_SET

SRSS Interrupt Set Register

Address: 0x40260704

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW1S	None			RW1S	RW1S
HW Access	None		A	None			A	A
Name	None [7:6]		CLK_CAL	None [4:2]			HVLVD1	WDT_-MATCH

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	CLK_CAL	Set interrupt for clock calibration counter done. This field is reset during DEEPSLEEP mode. Default Value: 0
1	HVLVD1	Set interrupt for low voltage detector HVLVD1 Default Value: 0
0	WDT_MATCH	Set interrupt for low voltage detector WDT_MATCH Default Value: 0

9.1.34 SRSS_INTR_MASK

SRSS Interrupt Mask Register

Address: 0x40260708

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	None			RW	RW
HW Access	None		R	None			R	R
Name	None [7:6]		CLK_CAL	None [4:2]			HVLVD1	WDT_-MATCH

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	CLK_CAL	Mask for clock calibration done Default Value: 0
1	HVLVD1	Mask for low voltage detector HVLVD1 Default Value: 0
0	WDT_MATCH	Mask for watchdog timer. Clearing this bit will not forward the interrupt to the CPU. It will not, however, disable the WDT reset generation on 2 missed interrupts. When WDT resets the chip, it also internally pends an interrupt that survives the reset. To prevent unintended ISR execution, clear SRSS_INTR.WDT_MATCH before setting this bit. Default Value: 0

9.1.35 SRSS_INTR_MASKED

SRSS Interrupt Masked Register

Address: 0x4026070C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R	None			R	R
HW Access	None		RW	None			RW	RW
Name	None [7:6]		CLK_CAL	None [4:2]			HVLVD1	WDT_-MATCH

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	CLK_CAL	Logical and of corresponding request and mask bits. Default Value: 0
1	HVLVD1	Logical and of corresponding request and mask bits. Default Value: 0
0	WDT_MATCH	Logical and of corresponding request and mask bits. Default Value: 0

9.1.36 SRSS_INTR_CFG

SRSS Interrupt Configuration Register

Address: 0x40260710

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	
HW Access	None						R	
Name	None [7:2]						HVLVD1_EDGE_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1 : 0	HVLVD1_EDGE_SEL	Sets which edge(s) will trigger an IRQ for HVLVD1 Default Value: 0 **0x0: DISABLE :** Disabled **0x1: RISING :** Rising edge **0x2: FALLING :** Falling edge **0x3: BOTH :** Both rising and falling edges

9.1.37 RES_CAUSE

Reset Cause Observation Register

Address: 0x40260800

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	A	A	A	A	A	A	A	A
Name	RE-SET_MCWDT2	RE-SET_MCWDT1	RE-SET_MCWDT0	RESET_-SOFT	RE-SET_CSV_WCO_LOSS	RESET_D-PSLP_-FAULT	RE-SET_ACT_-FAULT	RE-SET_WDT

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1C
HW Access	None							A
Name	None [15:9]							RE-SET_MCWDT3

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	RESET_MCWDT3	Multi-Counter Watchdog timer reset #3 has occurred since last power cycle. This hardware is not present in PSoC6 devices. Default Value: 0
7	RESET_MCWDT2	Multi-Counter Watchdog timer reset #2 has occurred since last power cycle. This hardware is not present in PSoC6 devices. Default Value: 0
6	RESET_MCWDT1	Multi-Counter Watchdog timer reset #1 has occurred since last power cycle. Default Value: 0
5	RESET_MCWDT0	Multi-Counter Watchdog timer reset #0 has occurred since last power cycle. Default Value: 0
4	RESET_SOFT	A CPU requested a system reset through it's SYSRESETREQ. This can be done via a debugger probe or in firmware. Default Value: 0

9.1.37 RES_CAUSE (continued)

3	RESET_CSV_W-CO_LOSS	Clock supervision logic requested a reset due to loss of a watch-crystal clock. Default Value: 0
2	RESET_DPSLP_FAULT	Fault logging system requested a reset from its DeepSleep logic. Default Value: 0
1	RESET_ACT_FAULT	Fault logging system requested a reset from its Active logic. Default Value: 0
0	RESET_WDT	A basic WatchDog Timer (WDT) reset has occurred since last power cycle. Default Value: 0

9.1.38 RES_CAUSE2

Reset Cause Observation Register 2

Address: 0x40260804

Retention: Retained

Bits	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SW Access	RW1C							
HW Access	A							
Name	RESET_CSV_HF_LOSS [7:0]							

Bits	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SW Access	RW1C							
HW Access	A							
Name	RESET_CSV_HF_LOSS [15:8]							

Bits	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SW Access	RW1C							
HW Access	A							
Name	RESET_CSV_HF_FREQ [23:16]							

Bits	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**
SW Access	RW1C							
HW Access	A							
Name	RESET_CSV_HF_FREQ [31:24]							

Bits	**Name**	**Description**
31 : 16	RESET_CSV_HF_FREQ	Clock supervision logic requested a reset due to frequency error of high-frequency clock. Each bit index K corresponds to a HFCLK. Unimplemented clock bits return zero. Default Value: 0
15 : 0	RESET_CSV_HF_LOSS	Clock supervision logic requested a reset due to loss of a high-frequency clock. Each bit index K corresponds to a HFCLK. Unimplemented clock bits return zero. Default Value: 0

9.1.39 PWR_TRIM_REF_CTL

Reference Trim Register

Address: 0x40267F00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	A				A			
Name	ACT_REF_ITRIM [7:4]				ACT_REF_TCTRIM [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW	None	RW				
HW Access	None	A	None	A				
Name	None	ACT_REF_I BOOST	None	ACT_REF_ABSTRIM [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW			
HW Access	A				A			
Name	DPSLP_REF_ABSTRIM [23:20]				DPSLP_REF_TCTRIM [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW				None			RW
HW Access	A				None			A
Name	DPSLP_REF_ITRIM [31:28]				None [27:25]			DPS-LP_REF_A BSTRIM

Bits	Name	Description
31 : 28	DPSLP_REF_ITRIM	DeepSleep current reference trim. This register is only reset by XRES/POR/BOD/HIBERNATE. Default Value: 7
24 : 20	DPSLP_REF_ABSTRIM	DeepSleep-Reference absolute voltage trim. This register is only reset by XRES/POR/BOD/HI-BERNATE. Default Value: 15
19 : 16	DPSLP_REF_TCTRIM	DeepSleep-Reference temperature trim. This register is only reset by XRES/POR/BOD/HIBER-NATE. 0 -> default setting at POR; not for trimming use others -> normal trim range Default Value: 0
14	ACT_REF_IBOOST	Active-Reference current boost. This register is only reset by XRES/POR/BOD/HIBERNATE. 0: normal operation others: risk mitigation Default Value: 0

9.1.39 PWR_TRIM_REF_CTL (continued)

12 : 8	ACT_REF_ABSTRIM	Active-Reference absolute voltage trim. This register is only reset by XRES/POR/BOD/HIBER-NATE. 0 -> default setting at POR; not for trimming use others -> normal trim range Default Value: 0
7 : 4	ACT_REF_ITRIM	Active-Reference current trim. This register is only reset by XRES/POR/BOD/HIBERNATE. 0 -> default setting at POR; not for trimming use others -> normal trim range Default Value: 0
3 : 0	ACT_REF_TCTRIM	Active-Reference temperature trim. This register is only reset by XRES/POR/BOD/HIBERNATE. 0 -> default setting at POR; not for trimming use others -> normal trim range Default Value: 0

9.1.40 PWR_TRIM_BODOVP_CTL

BOD/OVP Trim Register

Address: 0x40267F04

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW			None	RW		
HW Access	A	A			None	A		
Name	HVPORBOD_ITRIM	HVPORBOD_OFSTRIM [6:4]			None	HVPORBOD_TRIPSEL [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW		None	RW			RW	
HW Access	A		None	A			A	
Name	LVPORBOD_OFSTRIM [15:14]		None	LVPORBOD_TRIPSEL [12:10]			HVPORBOD_ITRIM [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			RW
HW Access	None				A			A
Name	None [23:20]				LVPORBOD_ITRIM [19:17]			LVPORBOD_OFSTRIM

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 17	LVPORBOD_ITRIM	LVPORBOD current trim. This register is only reset by XRES/POR/BOD/HIBERNATE. Default Value: 2
16 : 14	LVPORBOD_OFSTRIM	LVPORBOD offset trim. This register is only reset by XRES/POR/BOD/HIBERNATE. Default Value: 0
12 : 10	LVPORBOD_TRIPSEL	LVPORBOD trip point selection. Monitors vccd. This register is only reset by XRES/POR/BOD/HIBERNATE. Default Value: 3
9 : 7	HVPORBOD_ITRIM	HVPORBOD current trim. This register is only reset by XRES/POR/BOD/HIBERNATE. Default Value: 2
6 : 4	HVPORBOD_OFSTRIM	HVPORBOD offset trim. This register is only reset by XRES/POR/BOD/HIBERNATE. Default Value: 0
2 : 0	HVPORBOD_TRIPSEL	HVPORBOD trip point selection. Monitors vddd. This register is only reset by XRES/POR/BOD/HIBERNATE. Default Value: 4

9.1.41 CLK_TRIM_CCO_CTL

CCO Trim Register

Address: 0x40267F08

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		CCO_RCSTRIM [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None	RW					
HW Access	R	None	R					
Name	EN-ABLE_CNT	None	CCO_STABLE_CNT [29:24]					

Bits	Name	Description
31	ENABLE_CNT	Enables the automatic stabilization counter. Default Value: 1
29 : 24	CCO_STABLE_CNT	Terminal count for the stabilization counter from CCO_ENABLE until stable. Default Value: 39
5 : 0	CCO_RCSTRIM	CCO reference current source trim. Default Value: 32

9.1.42 CLK_TRIM_CCO_CTL2

CCO Trim Register 2

Address: 0x40267F0C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW			RW				
HW Access	R			R				
Name	CCO_FCTRIM2 [7:5]			CCO_FCTRIM1 [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW					RW	
HW Access	R	R					R	
Name	CCO_FC-TRIM4	CCO_FCTRIM3 [14:10]					CCO_FCTRIM2 [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW			
HW Access	R				R			
Name	CCO_FCTRIM5 [23:20]				CCO_FCTRIM4 [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							RW
HW Access	None							R
Name	None [31:25]							CCO_FC-TRIM5

Bits	Name	Description
24 : 20	CCO_FCTRIM5	CCO frequency 5th range calibration Default Value: 8
19 : 15	CCO_FCTRIM4	CCO frequency 4th range calibration Default Value: 16
14 : 10	CCO_FCTRIM3	CCO frequency 3rd range calibration Default Value: 16
9 : 5	CCO_FCTRIM2	CCO frequency 2nd range calibration Default Value: 8
4 : 0	CCO_FCTRIM1	CCO frequency 1st range calibration Default Value: 16

9.1.43 PWR_TRIM_WAKE_CTL

Wakeup Trim Register

Address: 0x40267F30

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	WAKE_DELAY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	WAKE_DELAY	Wakeup holdoff. Spec (fastest) wake time is achieved with a setting of 0. Additional delay can be added for debugging or workaround. The delay is counted by the IMO. Default Value: 0

9.1.44 PWR_TRIM_LVD_CTL

LVD Trim Register

Address: 0x4026FF10

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	HVLVD1_ITRIM [6:4]			None	HVLVD1_OFSTRIM [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
6 : 4	HVLVD1_ITRIM	HVLVD1 current trim Default Value: 2
2 : 0	HVLVD1_OFSTRIM	HVLVD1 offset trim Default Value: 0

9.1.45 CLK_TRIM_ILO_CTL

ILO Trim Register

Address: 0x4026FF18

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		A					
Name	None [7:6]		ILO_FTRIM [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	ILO_FTRIM	ILO frequency trims. LSB step size is 1.5% (typical) of the frequency. Default Value: 44

9.1.46 PWR_TRIM_PWRSYS_CTL

Power System Trim Register

Address: 0x4026FF1C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			A				
Name	None [7:5]			ACT_REG_TRIM [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None					
HW Access	A		None					
Name	ACT_REG_BOOST [31:30]		None [29:24]					

Bits	Name	Description
31 : 30	ACT_REG_BOOST	Controls the tradeoff between output current and internal operating current for the Active Regulator. The maximum output current depends on the silicon implementation, but an application may limit its maximum current to less than that. This may allow a reduction in the internal operating current of the regulator. The regulator internal operating current depends on the boost setting: 2'b00: 50uA 2'b01: 100uA 2'b10: 150uA 2'b11: 200uA The allowed setting is a lookup table based on the chip-specific maximum (set in factory) and an application-specific maximum (set by customer). The defaults are set assuming the application consumes the maximum allowed by the chip. 50mA chip: 2'b00 (default); 100mA chip: 2'b00 (default); 150mA chip: 50..100mA app => 2'b00, 150mA app => 2'b01 (default); 200mA chip: 50mA app => 2'b00, 100..150mA app => 2'b01, 200mA app => 2'b10 (default); 250mA chip: 50mA app => 2'b00, 100..150mA app => 2'b01, 200..250mA app => 2'b10 (default); 300mA chip: 50mA app => 2'b00, 100..150mA app => 2'b01, 200..250mA app => 2'b10, 300mA app => 2'b11 (default); This register is only reset by XRES/POR/BOD/HIBERNATE. Default Value: X

9.1.46 PWR_TRIM_PWRSYS_CTL (continued)

4 : 0	ACT_REG_TRIM	Trim for the Active-Regulator. This sets the output voltage level. This register is only reset by XRES/POR/BOD/HIBERNATE. Two voltages are supported: 0.9V and 1.1V. The codes for these are stored in SFLASH_LDO_0P9V_TRIM and SFLASH_LDO_1P1V_TRIM, respectively. Default Value: 23

9.1.47 CLK_TRIM_ECO_CTL

ECO Trim Register

Address: 0x4026FF20

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				None	RW		
HW Access	R				None	R		
Name	ATRIM [7:4]				None	WDTRIM [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW		RW		RW	
HW Access	None		R		R		R	
Name	None [15:14]		GTRIM [13:12]		RTRIM [11:10]		FTRIM [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW					
HW Access	None		R					
Name	None [23:22]		ITRIM [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
21 : 16	ITRIM	Current Trim Default Value: 31
13 : 12	GTRIM	Gain Trim - Startup time Default Value: 0
11 : 10	RTRIM	Feedback resistor Trim Default Value: 0
9 : 8	FTRIM	Filter Trim - 3rd harmonic oscillation Default Value: 0

9.1.47 CLK_TRIM_ECO_CTL (continued)

7 : 4	ATRIM	Amplitude trim to set the crystal drive level when ECO_CONFIG.AGC_EN=1. WARNING: use care when setting this field because driving a crystal beyond its rated limit can permanently damage the crystal. 0x0 - 150mV 0x1 - 175mV 0x2 - 200mV 0x3 - 225mV 0x4 - 250mV 0x5 - 275mV 0x6 - 300mV 0x7 - 325mV 0x8 - 350mV 0x9 - 375mV 0xA - 400mV 0xB - 425mV 0xC - 450mV 0xD - 475mV 0xE - 500mV 0xF - 525mV Default Value: 0
2 : 0	WDTRIM	Watch Dog Trim - Delta voltage below steady state level 0x0 - 50mV 0x1 - 75mV 0x2 - 100mV 0x3 - 125mV 0x4 - 150mV 0x5 - 175mV 0x6 - 200mV 0x7 - 225mV Default Value: 3

9.1.48 CLK_TRIM_PILO_CTL

PILO Trim Register

Address: 0x4026FF24

Retention: Retained

<table>
<tr><th>Bits</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td>SW Access</td><td colspan="2">None</td><td colspan="6">RW</td></tr>
<tr><td>HW Access</td><td colspan="2">None</td><td colspan="6">R</td></tr>
<tr><td>Name</td><td colspan="2">None [7:6]</td><td colspan="6">PILO_CFREQ [5:0]</td></tr>
</table>

<table>
<tr><th>Bits</th><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th></tr>
<tr><td>SW Access</td><td>None</td><td colspan="3">RW</td><td colspan="4">None</td></tr>
<tr><td>HW Access</td><td>None</td><td colspan="3">R</td><td colspan="4">None</td></tr>
<tr><td>Name</td><td>None</td><td colspan="3">PILO_OSC_TRIM [14:12]</td><td colspan="4">None [11:8]</td></tr>
</table>

<table>
<tr><th>Bits</th><th>23</th><th>22</th><th>21</th><th>20</th><th>19</th><th>18</th><th>17</th><th>16</th></tr>
<tr><td>SW Access</td><td colspan="4">RW</td><td colspan="2">RW</td><td colspan="2">RW</td></tr>
<tr><td>HW Access</td><td colspan="4">R</td><td colspan="2">R</td><td colspan="2">R</td></tr>
<tr><td>Name</td><td colspan="4">PILO_RES_TRIM [23:20]</td><td colspan="2">PILO_NBIAS_TRIM [19:18]</td><td colspan="2">PILO_COMP_TRIM [17:16]</td></tr>
</table>

<table>
<tr><th>Bits</th><th>31</th><th>30</th><th>29</th><th>28</th><th>27</th><th>26</th><th>25</th><th>24</th></tr>
<tr><td>SW Access</td><td>None</td><td colspan="3">RW</td><td colspan="2">RW</td><td>None</td><td>RW</td></tr>
<tr><td>HW Access</td><td>None</td><td colspan="3">R</td><td colspan="2">R</td><td>None</td><td>R</td></tr>
<tr><td>Name</td><td>None</td><td colspan="3">PILO_VTDIFF_TRIM [30:28]</td><td colspan="2">PILO_ISLOPE_TRIM [27:26]</td><td>None</td><td>PI-LO_RES_TRIM</td></tr>
</table>

Bits	Name	Description
30 : 28	PILO_VTDIFF_TRIM	Trim for VT-DIFF output (internal power supply) Default Value: 0
27 : 26	PILO_ISLOPE_TRIM	Trim for beta-multiplier current slope Default Value: 0
24 : 20	PILO_RES_TRIM	Trim for beta-multiplier branch current Default Value: 16
19 : 18	PILO_NBIAS_TRIM	Trim for biasn by trimming sub-Vth NMOS width in beta-multiplier Default Value: 2
17 : 16	PILO_COMP_TRIM	Trim for comparator bias current. Default Value: 0
14 : 12	PILO_OSC_TRIM	Trim for current in oscillator block. Default Value: 5

9.1.48 CLK_TRIM_PILO_CTL (continued)

5 : 0	PILO_CFREQ	Coarse frequency trim to meet 32.768kHz +/-2% across PVT without calibration. The nominal step size of the LSB is 1kHz. Default Value: 15

9.1.49 CLK_TRIM_PILO_CTL2

PILO Trim Register 2

Address: 0x4026FF28

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	PILO_VREF_TRIM [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW				
HW Access	None			R				
Name	None [15:13]			PILO_IREFBM_TRIM [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	PILO_IREF_TRIM [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	PILO_IREF_TRIM	Trim for current reference Default Value: 218
12 : 8	PILO_IREFBM_TRIM	Trim for beta-multiplier current reference Default Value: 16
7 : 0	PILO_VREF_TRIM	Trim for voltage reference Default Value: 224

9.1.50 CLK_TRIM_PILO_CTL3

PILO Trim Register 3

Address: 0x4026FF2C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	PILO_ENGOPT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	PILO_ENGOPT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	PILO_ENGOPT	Engineering options for PILO circuits 0: Short vdda to vpwr 1: Beta:mult current change 2: Iref generation Ptat current addition 3: Disable current path in secondary Beta:mult startup circuit 4: Double oscillator current 5: Switch between deep:sub:threshold and sub:threshold stacks in Vref generation block 6: Spare 7: Ptat component increase in Iref 8: vpwr_rc and vpwr_dig_rc shorting testmode 9: Switch b/w psub connection for cascode nfet for vref generation 10: Switch between sub:threshold and deep:sub:threshold stacks in comparator. 15-11: Frequency fine trim. See AKK-444 for an overview of the trim strategy. Default Value: 18432

10 Multi-Counter WDT (MCWDT) Registers

This section discusses the Multi-Counter WDT (MCWDT) registers. It lists all the registers in mapping tables, in address order.

10.1 Register Details

Register	Address	Description
MCWDT_CNTLOW0	0x40260204	Multi-Counter Watchdog Sub-counters 0/1
MCWDT_CNTHIGH0	0x40260208	Multi-Counter Watchdog Sub-counter 2
MCWDT_MATCH0	0x4026020C	Multi-Counter Watchdog Counter Match Register
MCWDT_CONFIG0	0x40260210	Multi-Counter Watchdog Counter Configuration
MCWDT_CTL0	0x40260214	Multi-Counter Watchdog Counter Control
MCWDT_INTR0	0x40260218	Multi-Counter Watchdog Counter Interrupt Register
MCWDT_INTR_SET0	0x4026021C	Multi-Counter Watchdog Counter Interrupt Set Register
MCWDT_INTR_MASK0	0x40260220	Multi-Counter Watchdog Counter Interrupt Mask Register
MCWDT_INTR_MASKED0	0x40260224	Multi-Counter Watchdog Counter Interrupt Masked Register
MCWDT_LOCK0	0x40260228	Multi-Counter Watchdog Counter Lock Register
MCWDT_CNTLOW1	0x40260244	Multi-Counter Watchdog Sub-counters 0/1. See MCWDT_CNTLOW0 for the details of bit fields.
MCWDT_CNTHIGH1	0x40260248	Multi-Counter Watchdog Sub-counter 2. See MCWDT_CNTHIGH0 for the details of bit fields.
MCWDT_MATCH1	0x4026024C	Multi-Counter Watchdog Counter Match Register. See MCWDT_MATCH0 for the details of bit fields.
MCWDT_CONFIG1	0x40260250	Multi-Counter Watchdog Counter Configuration. See MCWDT_CONFIG0 for the details of bit fields.
MCWDT_CTL1	0x40260254	Multi-Counter Watchdog Counter Control. See MCWDT_CTL0 for the details of bit fields.
MCWDT_INTR1	0x40260258	Multi-Counter Watchdog Counter Interrupt Register. See MCWDT_INTR0 for the details of bit fields.
MCWDT_INTR_SET1	0x4026025C	Multi-Counter Watchdog Counter Interrupt Set Register. See MCWDT_INTR_SET0 for the details of bit fields.
MCWDT_INTR_MASK1	0x40260260	Multi-Counter Watchdog Counter Interrupt Mask Register. See MCWDT_INTR_MASK0 for the details of bit fields.
MCWDT_INTR_MASKED1	0x40260264	Multi-Counter Watchdog Counter Interrupt Masked Register. See MCWDT_INTR_MASKED0 for the details of bit fields.
MCWDT_LOCK1	0x40260268	Multi-Counter Watchdog Counter Lock Register. See MCWDT_LOCK0 for the details of bit fields.

10.1.1 MCWDT_CNTLOW0

Multi-Counter Watchdog Sub-counters 0/1

Address: 0x40260204

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	WDT_CTR0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	WDT_CTR0 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	A							
Name	WDT_CTR1 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	A							
Name	WDT_CTR1 [31:24]							

Bits	Name	Description
31 : 16	WDT_CTR1	Current value of sub-counter 1 for this MCWDT. Software writes are ignored when the sub-counter is enabled Default Value: 0
15 : 0	WDT_CTR0	Current value of sub-counter 0 for this MCWDT. Software writes are ignored when the sub-counter is enabled. Default Value: 0

10.1.2 MCWDT_CNTHIGH0

Multi-Counter Watchdog Sub-counter 2

Address: 0x40260208

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	WDT_CTR2 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	WDT_CTR2 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	A							
Name	WDT_CTR2 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	A							
Name	WDT_CTR2 [31:24]							

Bits	Name	Description
31 : 0	WDT_CTR2	Current value of sub-counter 2 for this MCWDT. Software writes are ignored when the sub-counter is enabled Default Value: 0

10.1.3 MCWDT_MATCH0

Multi-Counter Watchdog Counter Match Register

Address: 0x4026020C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	WDT_MATCH0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	WDT_MATCH0 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	WDT_MATCH1 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	WDT_MATCH1 [31:24]							

Bits	Name	Description
31 : 16	WDT_MATCH1	Match value for sub-counter 1 of this MCWDT Default Value: 0
15 : 0	WDT_MATCH0	Match value for sub-counter 0 of this MCWDT Default Value: 0

10.1.4 MCWDT_CONFIG0

Multi-Counter Watchdog Counter Configuration

Address: 0x40260210

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	
HW Access	None				R	R	R	
Name	None [7:4]				WDT_CAS-CADE0_1	WDT_-CLEAR0	WDT_MODE0 [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	RW	RW	
HW Access	None				R	R	R	
Name	None [15:12]				WDT_CAS-CADE1_2	WDT_-CLEAR1	WDT_MODE1 [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							WDT_-MODE2

Bits	31	30	29	28	27	26	25	24
SW Access	None			RW				
HW Access	None			R				
Name	None [31:29]			WDT_BITS2 [28:24]				

Bits	Name	Description
28 : 24	WDT_BITS2	Bit to observe for WDT_INT2: 0: Assert after bit0 of WDT_CTR2 toggles (one int every tick) ... 31: Assert after bit31 of WDT_CTR2 toggles (one int every 2^31 ticks) Default Value: 0
16	WDT_MODE2	Watchdog Counter 2 Mode. Default Value: 0 **0x0: NOTHING :** Free running counter with no interrupt requests **0x1: INT :** Free running counter with interrupt request that occurs one LFCLK cycle after the specified bit in CTR2 toggles (see WDT_BITS2).

10.1.4 MCWDT_CONFIG0 (continued)

11	WDT_CASCADE1_2	Cascade Watchdog Counters 1,2. Counter 2 increments the cycle after WDT_CTR1=WDT_-MATCH1. It is allowed to cascade all three WDT counters. 0: Independent counters 1: Cascaded counters. When cascading all three counters, WDT_CLEAR1 must be 1. Default Value: 0
10	WDT_CLEAR1	Clear Watchdog Counter when WDT_CTR1==WDT_MATCH1. In other words WDT_CTR1 di-vides LFCLK by (WDT_MATCH1+1). 0: Free running counter 1: Clear on match. In this mode, the minimum legal setting of WDT_MATCH1 is 1. Default Value: 0
9 : 8	WDT_MODE1	Watchdog Counter Action on Match. Action is taken on the next increment after the values match (WDT_CTR1=WDT_MATCH1). Default Value: 0 **0x0: NOTHING :** Do nothing **0x1: INT :** Assert WDT_INTx **0x2: RESET :** Assert WDT Reset **0x3: INT_THEN_RESET :** Assert WDT_INTx, assert WDT Reset after 3rd unhandled interrupt
3	WDT_CASCADE0_1	Cascade Watchdog Counters 0,1. Counter 1 increments the cycle after WDT_CTR0=WDT_-MATCH0. 0: Independent counters 1: Cascaded counters Default Value: 0
2	WDT_CLEAR0	Clear Watchdog Counter when WDT_CTR0=WDT_MATCH0. In other words WDT_CTR0 di-vides LFCLK by (WDT_MATCH0+1). 0: Free running counter 1: Clear on match. In this mode, the minimum legal setting of WDT_MATCH0 is 1. Default Value: 0
1 : 0	WDT_MODE0	Watchdog Counter Action on Match. Action is taken on the next increment after the values match (WDT_CTR0=WDT_MATCH0). Default Value: 0 **0x0: NOTHING :** Do nothing **0x1: INT :** Assert WDT_INTx

10.1.4 MCWDT_CONFIG0 (continued)

0x2: RESET :

Assert WDT Reset

0x3: INT_THEN_RESET :

Assert WDT_INTx, assert WDT Reset after 3rd unhandled interrupt

10.1.5 MCWDT_CTL0

Multi-Counter Watchdog Counter Control

Address: 0x40260214

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1S	None	R	RW
HW Access	None				RW0C	None	RW	R
Name	None [7:4]				WDT_RE-SET0	None	WDT_EN-ABLED0	WDT_EN-ABLE0

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW1S	None	R	RW
HW Access	None				RW0C	None	RW	R
Name	None [15:12]				WDT_RE-SET1	None	WDT_EN-ABLED1	WDT_EN-ABLE1

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW1S	None	R	RW
HW Access	None				RW0C	None	RW	R
Name	None [23:20]				WDT_RE-SET2	None	WDT_EN-ABLED2	WDT_EN-ABLE2

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19	WDT_RESET2	Resets counter 2 back to 0000. Hardware will reset this bit after counter was reset. This will take up to one LFCLK cycle to take effect. Default Value: 0
17	WDT_ENABLED2	Indicates actual state of counter. May lag WDT_ENABLE2 by up to two LFCLK cycles. Default Value: 0
16	WDT_ENABLE2	Enable subcounter 2. May take up to 2 LFCLK cycles to take effect. 0: Counter is disabled (not clocked) 1: Counter is enabled (counting up) Default Value: 0
11	WDT_RESET1	Resets counter 1 back to 0000. Hardware will reset this bit after counter was reset. This will take up to one LFCLK cycle to take effect. Default Value: 0
9	WDT_ENABLED1	Indicates actual state of counter. May lag WDT_ENABLE1 by up to two LFCLK cycles. Default Value: 0

10.1.5 MCWDT_CTL0 (continued)

8	WDT_ENABLE1	Enable subcounter 1. May take up to 2 LFCLK cycles to take effect. 0: Counter is disabled (not clocked) 1: Counter is enabled (counting up) Default Value: 0
3	WDT_RESET0	Resets counter 0 back to 0000. Hardware will reset this bit after counter was reset. This will take up to one LFCLK cycle to take effect. Default Value: 0
1	WDT_ENABLED0	Indicates actual state of counter. May lag WDT_ENABLE0 by up to two LFCLK cycles. Default Value: 0
0	WDT_ENABLE0	Enable subcounter 0. May take up to 2 LFCLK cycles to take effect. 0: Counter is disabled (not clocked) 1: Counter is enabled (counting up) Default Value: 0

10.1.6 MCWDT_INTR0

Multi-Counter Watchdog Counter Interrupt Register

Address: 0x40260218

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW1C	RW1C	RW1C
HW Access	None					A	A	A
Name	None [7:3]					MCWDT_INT2	MCWDT_INT1	MCWDT_INT0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	MCWDT_INT2	MCWDT Interrupt Request for sub-counter 2. This bit is set by hardware as configured by this registers. This bit must be cleared by firmware. Clearing this bit also prevents Reset from happening when WDT_MODE2=3. Default Value: 0
1	MCWDT_INT1	MCWDT Interrupt Request for sub-counter 1. This bit is set by hardware as configured by this registers. This bit must be cleared by firmware. Clearing this bit also prevents Reset from happening when WDT_MODE1=3. Default Value: 0
0	MCWDT_INT0	MCWDT Interrupt Request for sub-counter 0. This bit is set by hardware as configured by this registers. This bit must be cleared by firmware. Clearing this bit also prevents Reset from happening when WDT_MODE0=3. Default Value: 0

10.1.7 MCWDT_INTR_SET0

Multi-Counter Watchdog Counter Interrupt Set Register

Address: 0x4026021C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW1S	RW1S	RW1S
HW Access	None					A	A	A
Name	None [7:3]					MCWDT_INT2	MCWDT_INT1	MCWDT_INT0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	MCWDT_INT2	Set interrupt for MCWDT_INT2 Default Value: 0
1	MCWDT_INT1	Set interrupt for MCWDT_INT1 Default Value: 0
0	MCWDT_INT0	Set interrupt for MCWDT_INT0 Default Value: 0

10.1.8 MCWDT_INTR_MASK0

Multi-Counter Watchdog Counter Interrupt Mask Register

Address: 0x40260220

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [7:3]					MCWDT_INT2	MCWDT_INT1	MCWDT_INT0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	MCWDT_INT2	Interrupt Mask for sub-counter 2. The bit controls if the interrupt is forwarded to the CPU. The interrupt is blocked when the value of the bit is 0. The interrupt is forwarded if the value of the bit is 1. Default Value: 0
1	MCWDT_INT1	Interrupt Mask for sub-counter 1. The bit controls if the interrupt is forwarded to the CPU. The interrupt is blocked when the value of the bit is 0. The interrupt is forwarded if the value of the bit is 1. Default Value: 0
0	MCWDT_INT0	Interrupt Mask for sub-counter 0. The bit controls if the interrupt is forwarded to the CPU. The interrupt is blocked when the value of the bit is 0. The interrupt is forwarded if the value of the bit is 1. Default Value: 0

10.1.9 MCWDT_INTR_MASKED0

Multi-Counter Watchdog Counter Interrupt Masked Register

Address: 0x40260224

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					R	R	R
HW Access	None					RW	RW	RW
Name	None [7:3]					MCWDT_INT2	MCWDT_INT1	MCWDT_INT0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	MCWDT_INT2	Logical and of corresponding request and mask bits. Default Value: 0
1	MCWDT_INT1	Logical and of corresponding request and mask bits. Default Value: 0
0	MCWDT_INT0	Logical and of corresponding request and mask bits. Default Value: 0

10.1.10 MCWDT_LOCK0

Multi-Counter Watchdog Counter Lock Register

Address: 0x40260228

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None					
HW Access	A		None					
Name	MCWDT_LOCK [31:30]		None [29:24]					

Bits	Name	Description
31 : 30	MCWDT_LOCK	Prohibits writing control and configuration registers related to this MCWDT when not equal 0 (as specified in the other register descriptions). Requires at least two different writes to unlock. Note that this field is 2 bits to force multiple writes only. Each MCWDT has a separate local lock. LFCLK settings are locked by the global WDT_LOCK register, and this register has no effect on that. Default Value: 0 **0x0: NO_CHG :** No effect **0x1: CLR0 :** Clears bit 0 **0x2: CLR1 :** Clears bit 1

10.1.10 MCWDT_LOCK0 (continued)

0x3: SET01 :

Sets both bits 0 and 1

11 Backup System Registers

This section discusses the Backup System registers. It lists all the registers in mapping tables, in address order.

11.1 Register Details

Register	Address	Description
BACKUP_CTL	0x40270000	Control
BACKUP_RTC_RW	0x40270008	RTC Read Write register
BACKUP_CAL_CTL	0x4027000C	Oscillator calibration for absolute frequency
BACKUP_STATUS	0x40270010	Status
BACKUP_RTC_TIME	0x40270014	Calendar Seconds, Minutes, Hours, Day of Week
BACKUP_RTC_DATE	0x40270018	Calendar Day of Month, Month, Year
BACKUP_ALM1_TIME	0x4027001C	Alarm 1 Seconds, Minute, Hours, Day of Week
BACKUP_ALM1_DATE	0x40270020	Alarm 1 Day of Month, Month
BACKUP_ALM2_TIME	0x40270024	Alarm 2 Seconds, Minute, Hours, Day of Week
BACKUP_ALM2_DATE	0x40270028	Alarm 2 Day of Month, Month
BACKUP_INTR	0x4027002C	Interrupt request register
BACKUP_INTR_SET	0x40270030	Interrupt set request register
BACKUP_INTR_MASK	0x40270034	Interrupt mask register
BACKUP_INTR_MASKED	0x40270038	Interrupt masked request register
BACKUP_OSCCNT	0x4027003C	32kHz oscillator counter
BACKUP_TICKS	0x40270040	128Hz tick counter
BACKUP_PMIC_CTL	0x40270044	PMIC control register
BACKUP_RESET	0x40270048	Backup reset register
BACKUP_BREG0	0x40271000	Backup register region
BACKUP_BREG1	0x40271004	Backup register region. See BACKUP_BREG0 for the details of bit fields.
BACKUP_BREG2	0x40271008	Backup register region. See BACKUP_BREG0 for the details of bit fields.
BACKUP_BREG3	0x4027100C	Backup register region. See BACKUP_BREG0 for the details of bit fields.
BACKUP_BREG4	0x40271010	Backup register region. See BACKUP_BREG0 for the details of bit fields.
BACKUP_BREG5	0x40271014	Backup register region. See BACKUP_BREG0 for the details of bit fields.
BACKUP_BREG6	0x40271018	Backup register region. See BACKUP_BREG0 for the details of bit fields.
BACKUP_BREG7	0x4027101C	Backup register region. See BACKUP_BREG0 for the details of bit fields.
BACKUP_BREG8	0x40271020	Backup register region. See BACKUP_BREG0 for the details of bit fields.

Register	Address	Description
BACKUP_BREG9	0x40271024	Backup register region. See BACKUP_BREG0 for the details of bit fields.
BACKUP_BREG10	0x40271028	Backup register region. See BACKUP_BREG0 for the details of bit fields.
BACKUP_BREG11	0x4027102C	Backup register region. See BACKUP_BREG0 for the details of bit fields.
BACKUP_BREG12	0x40271030	Backup register region. See BACKUP_BREG0 for the details of bit fields.
BACKUP_BREG13	0x40271034	Backup register region. See BACKUP_BREG0 for the details of bit fields.
BACKUP_BREG14	0x40271038	Backup register region. See BACKUP_BREG0 for the details of bit fields.
BACKUP_BREG15	0x4027103C	Backup register region. See BACKUP_BREG0 for the details of bit fields.
BACKUP_TRIM	0x4027FF00	Trim Register

11.1.1 BACKUP_CTL

Control

Address: 0x40270000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	None		
HW Access	None				A	None		
Name	None [7:4]				WCO_EN	None		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW		None		RW	
HW Access	None		A		None		A	
Name	None [15:14]		PRESCALER [13:12]		None [11:10]		CLK_SEL [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW	RW		RW
HW Access	None				A	A		A
Name	None [23:20]				VBACK-UP_MEAS	VDDBAK_CTL [18:17]		WCO_BY-PASS

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	A							
Name	EN_CHARGE_KEY [31:24]							

Bits	Name	Description
31 : 24	EN_CHARGE_KEY	When set to 3C, the supercap charger circuit is enabled. Any other code disables the supercap charger. THIS CHARGING CIRCUIT IS FOR A SUPERCAP ONLY AND CANNOT SAFELY CHARGE A BATTERY. DO NOT WRITE THIS KEY WHEN VBACKUP IS CONNECTED TO A BATTERY. Default Value: 0
19	VBACKUP_MEAS	Connect vbackup supply to the vbackup_meas output for measurement by an ADC attached to amuxbusa_adft_vddd. The vbackup_meas signal is scaled by 40% so it is within the supply range of the ADC. Default Value: 0
18 : 17	VDDBAK_CTL	Controls the behavior of the switch that generates vddbak from vbackup or vddd. 0: automatically select vddd if its brownout detector says it is valid. If the brownout says its not valid, then use vmax which is the highest of vddd or vbackup. 1,2,3: force vddbak and vmax to select vbackup, regardless of its voltage. Default Value: 0

11.1.1 BACKUP_CTL (continued)

16	WCO_BYPASS	Configures the WCO for different board-level connections to the WCO pins. For example, this can be used to connect an external watch crystal oscillator instead of a watch crystal. In all cases, the two related GPIO pins (WCO input and output pins) must be configured as analog connections using GPIO registers, and they must be hooked at the board level as described below. Configure this field before enabling the WCO, and do not change this setting when WCO_EN=1. 0: Watch crystal. Connect a 32.768 kHz watch crystal between WCO input and output pins. 1: Clock signal, either a square wave or sine wave. See PRESCALER field for connection information. Default Value: 0
13 : 12	PRESCALER	Prescaler for real time clock used when WCO_BYPASS=1. Configure this field before enabling the WCO, and do not change this setting when WCO_EN=1. 0: 32768 Hz square wave. Connect a 32768 Hz square wave to WCO output pin. Do not connect WCO input pin. 1: 60 Hz sine wave. Connect an AC-coupled sine wave to WCO input pin. Do not connect the WCO output pin at the board level. 2: 50 Hz sine wave. Connect an AC-couple sine wave to WCO input pin. Do not connect the WCO output pin at the board level. 3: reserved (32768 Hz) Default Value: 0
9 : 8	CLK_SEL	Clock select for BAK clock Default Value: 0 **0x0: WCO :** Watch-crystal oscillator input. **0x1: ALTBAK :** This allows to use the LFCLK selection as an alternate backup domain clock. Note that LFCLK is not available in all power modes, and clock glitches can propagate into the backup logic when the clock is stopped. For this reason, if the WCO is intended as the clock source then choose it directly instead of routing through LFCLK.
3	WCO_EN	Watch-crystal oscillator (WCO) enable. If there is a write in progress when this bit is cleared, the WCO will be internally kept on until the write completes. After enabling the WCO software must wait until STATUS.WCO_OK=1 before configuring any component that depends on clk_lf/clk_bak, like for example RTC or WDTs. Default Value: 0

11.1.2 BACKUP_RTC_RW

RTC Read Write register

Address: 0x40270008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						A	A
Name	None [7:2]						WRITE	READ

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	WRITE	Write bit Only when this bit is set can the RTC registers be written to (otherwise writes are ignored). This bit cannot be set if the RTC is still busy with a previous update (see RTC_BUSY bit) or if the Read bit is set or getting set. The user writes to the RTC user registers, when the Write bit is cleared by the user then the user registers content is copied to the actual RTC registers. Only user RTC registers that were written to will get copied, others will not be affected. When the SECONDS field is updated then TICKS will also be reset (WDT is not affected). When the Write bit is cleared by a reset (brown out/DeepSleep) then the RTC update will be ignored/lost. Do not set the Write bit if the RTC if the RTC is still busy with a previous update (see RTC_BUSY). Do not set the Write bit at the same time that the Read bit is cleared. Default Value: 0
0	READ	Read bit When this bit is set the RTC registers will be copied to user registers and frozen so that a coherent RTC value can safely be read. The RTC will keep on running. Do not set the read bit if the RTC is still busy with a previous update (see RTC_BUSY bit) or if the Write bit is set. Do not set the Read bit at the same time that the Write bit is cleared. Default Value: 0

11.1.3 BACKUP_CAL_CTL

Oscillator calibration for absolute frequency

Address: 0x4027000C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	RW					
HW Access	None	A	A					
Name	None	CALIB_-SIGN	CALIB_VAL [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	A	None						
Name	CAL_OUT	None [30:24]						

Bits	Name	Description
31	CAL_OUT	Output enable for 512Hz signal for calibration and allow CALIB_VAL to be written. Note that calibration does not affect the 512Hz output signal. Default Value: 0
6	CALIB_SIGN	Calibration sign: 0= Negative sign: remove pulses (it takes more clock ticks to count one second) 1= Positive sign: add pulses (it takes less clock ticks to count one second) Default Value: 0
5 : 0	CALIB_VAL	Calibration value for absolute frequency (at a fixed temperature). Each step causes 128 ticks to be added or removed each hour. Effectively that means that each step is 1.085ppm (= 128/(60*60*32,768)). Positive values 0x01-0x3c (1..60) add pulses, negative values remove pulses, thus giving a range of +/-65.1 ppm (limited by 60 minutes per hour, not the range of this field) Calibration is performed hourly, starting at 59 minutes and 59 seconds, and applied as 64 ticks every 30 seconds until there have been 2*CALIB_VAL adjustments. Default Value: 0

11.1.4 BACKUP_STATUS

Status

Address: 0x40270010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					R	None	R
HW Access	None					W	None	W
Name	None [7:3]					WCO_OK	None	RTC_BUSY

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	WCO_OK	Indicates that output has transitioned. Default Value: 0
0	RTC_BUSY	pending RTC write Default Value: 0

11.1.5 BACKUP_RTC_TIME

Calendar Seconds, Minutes, Hours, Day of Week

Address: 0x40270014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW						
HW Access	None	A						
Name	None	RTC_SEC [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW						
HW Access	None	A						
Name	None	RTC_MIN [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	None	RW	RW					
HW Access	None	A	A					
Name	None	CTRL_12HR	RTC_HOUR [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	None					RW		
HW Access	None					A		
Name	None [31:27]					RTC_DAY [26:24]		

Bits	Name	Description
26 : 24	RTC_DAY	Calendar Day of the week in BCD, 1-7 It is up to the user to define the meaning of the values, but 1=Monday is recommended Default Value: 0
22	CTRL_12HR	Select 12/24HR mode: 1=12HR, 0=24HR Default Value: 0
21 : 16	RTC_HOUR	Calendar hours in BCD, value depending on 12/24HR mode 0=24HR: [21:16]=0-23 1=12HR: [21]:0=AM, 1=PM, [20:16]=1-12 Default Value: 0
14 : 8	RTC_MIN	Calendar minutes in BCD, 0-59 Default Value: 0
6 : 0	RTC_SEC	Calendar seconds in BCD, 0-59 Default Value: 0

11.1.6 BACKUP_RTC_DATE

Calendar Day of Month, Month, Year

Address: 0x40270018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		A					
Name	None [7:6]		RTC_DATE [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW				
HW Access	None			A				
Name	None [15:13]			RTC_MON [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	A							
Name	RTC_YEAR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	RTC_YEAR	Calendar year in BCD, 0-99 Default Value: 0
12 : 8	RTC_MON	Calendar Month in BCD, 1-12 Default Value: 0
5 : 0	RTC_DATE	Calendar Day of the Month in BCD, 1-31 Automatic Leap Year Correction Default Value: 0

11.1.7 BACKUP_ALM1_TIME

Alarm 1 Seconds, Minute, Hours, Day of Week

Address: 0x4027001C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW						
HW Access	A	A						
Name	ALM_SEC_EN	ALM_SEC [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW						
HW Access	A	A						
Name	ALM_MIN_EN	ALM_MIN [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	RW	None	RW					
HW Access	A	None	A					
Name	ALM_HOUR_EN	None	ALM_HOUR [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None				RW		
HW Access	A	None				A		
Name	ALM_-DAY_EN	None [30:27]				ALM_DAY [26:24]		

Bits	Name	Description
31	ALM_DAY_EN	Alarm Day of the Week enable: 0=ignore, 1=match Default Value: 0
26 : 24	ALM_DAY	Alarm Day of the week in BCD, 1-7 It is up to the user to define the meaning of the values, but 1=Monday is recommended Default Value: 1
23	ALM_HOUR_EN	Alarm hour enable: 0=ignore, 1=match Default Value: 0
21 : 16	ALM_HOUR	Alarm hours in BCD, value depending on 12/24HR mode 12HR: [5]:0=AM, 1=PM, [4:0]=1-12 24HR: [5:0]=0-23 Default Value: 0
15	ALM_MIN_EN	Alarm minutes enable: 0=ignore, 1=match Default Value: 0

11.1.7 BACKUP_ALM1_TIME (continued)

14 : 8	ALM_MIN	Alarm minutes in BCD, 0-59 Default Value: 0
7	ALM_SEC_EN	Alarm second enable: 0=ignore, 1=match Default Value: 0
6 : 0	ALM_SEC	Alarm seconds in BCD, 0-59 Default Value: 0

11.1.8 BACKUP_ALM1_DATE

Alarm 1 Day of Month, Month

Address: 0x40270020

Retention: Retained

<table>
<tr><th>Bits</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td>SW Access</td><td>RW</td><td>None</td><td colspan="6">RW</td></tr>
<tr><td>HW Access</td><td>A</td><td>None</td><td colspan="6">A</td></tr>
<tr><td>Name</td><td>ALM_-
DATE_EN</td><td>None</td><td colspan="6">ALM_DATE [5:0]</td></tr>
</table>

<table>
<tr><th>Bits</th><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th></tr>
<tr><td>SW Access</td><td>RW</td><td colspan="2">None</td><td colspan="5">RW</td></tr>
<tr><td>HW Access</td><td>A</td><td colspan="2">None</td><td colspan="5">A</td></tr>
<tr><td>Name</td><td>ALM_MON_
EN</td><td colspan="2">None [14:13]</td><td colspan="5">ALM_MON [12:8]</td></tr>
</table>

<table>
<tr><th>Bits</th><th>23</th><th>22</th><th>21</th><th>20</th><th>19</th><th>18</th><th>17</th><th>16</th></tr>
<tr><td>SW Access</td><td colspan="8">None</td></tr>
<tr><td>HW Access</td><td colspan="8">None</td></tr>
<tr><td>Name</td><td colspan="8">None [23:16]</td></tr>
</table>

<table>
<tr><th>Bits</th><th>31</th><th>30</th><th>29</th><th>28</th><th>27</th><th>26</th><th>25</th><th>24</th></tr>
<tr><td>SW Access</td><td>RW</td><td colspan="7">None</td></tr>
<tr><td>HW Access</td><td>A</td><td colspan="7">None</td></tr>
<tr><td>Name</td><td>ALM_EN</td><td colspan="7">None [30:24]</td></tr>
</table>

Bits	Name	Description
31	ALM_EN	Master enable for alarm 1. 0: Alarm 1 is disabled. Fields for date and time are ignored. 1: Alarm 1 is enabled. If none of the date and time fields are enabled, then this alarm triggers once every second. Default Value: 0
15	ALM_MON_EN	Alarm Month enable: 0=ignore, 1=match Default Value: 0
12 : 8	ALM_MON	Alarm Month in BCD, 1-12 Default Value: 1
7	ALM_DATE_EN	Alarm Day of the Month enable: 0=ignore, 1=match Default Value: 0
5 : 0	ALM_DATE	Alarm Day of the Month in BCD, 1-31 Leap Year corrected Default Value: 1

11.1.9 BACKUP_ALM2_TIME

Alarm 2 Seconds, Minute, Hours, Day of Week

Address: 0x40270024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW						
HW Access	A	A						
Name	ALM_SEC_EN	ALM_SEC [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW						
HW Access	A	A						
Name	ALM_MIN_EN	ALM_MIN [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	RW	None	RW					
HW Access	A	None	A					
Name	ALM_HOUR_EN	None	ALM_HOUR [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None				RW		
HW Access	A	None				A		
Name	ALM_-DAY_EN	None [30:27]				ALM_DAY [26:24]		

Bits	Name	Description
31	ALM_DAY_EN	Alarm Day of the Week enable: 0=ignore, 1=match Default Value: 0
26 : 24	ALM_DAY	Alarm Day of the week in BCD, 1-7 It is up to the user to define the meaning of the values, but 1=Monday is recommended Default Value: 1
23	ALM_HOUR_EN	Alarm hour enable: 0=ignore, 1=match Default Value: 0
21 : 16	ALM_HOUR	Alarm hours in BCD, value depending on 12/24HR mode 12HR: [5]:0=AM, 1=PM, [4:0]=1-12 24HR: [5:0]=0-23 Default Value: 0
15	ALM_MIN_EN	Alarm minutes enable: 0=ignore, 1=match Default Value: 0

11.1.9 BACKUP_ALM2_TIME (continued)

14 : 8	ALM_MIN	Alarm minutes in BCD, 0-59 Default Value: 0
7	ALM_SEC_EN	Alarm second enable: 0=ignore, 1=match Default Value: 0
6 : 0	ALM_SEC	Alarm seconds in BCD, 0-59 Default Value: 0

11.1.10 BACKUP_ALM2_DATE

Alarm 2 Day of Month, Month

Address: 0x40270028

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	None	RW					
HW Access	A	None	A					
Name	ALM_-DATE_EN	None	ALM_DATE [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	RW	None		RW				
HW Access	A	None		A				
Name	ALM_MON_EN	None [14:13]		ALM_MON [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	A	None						
Name	ALM_EN	None [30:24]						

Bits	Name	Description
31	ALM_EN	Master enable for alarm 2. 0: Alarm 2 is disabled. Fields for date and time are ignored. 1: Alarm 2 is enabled. If none of the date and time fields are enabled, then this alarm triggers once every second. Default Value: 0
15	ALM_MON_EN	Alarm Month enable: 0=ignore, 1=match Default Value: 0
12 : 8	ALM_MON	Alarm Month in BCD, 1-12 Default Value: 1
7	ALM_DATE_EN	Alarm Day of the Month enable: 0=ignore, 1=match Default Value: 0
5 : 0	ALM_DATE	Alarm Day of the Month in BCD, 1-31 Leap Year corrected Default Value: 1

11.1.11 BACKUP_INTR

Interrupt request register

Address: 0x4027002C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW1C	RW1C	RW1C
HW Access	None					RW1S	RW1S	RW1S
Name	None [7:3]					CENTURY	ALARM2	ALARM1

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	CENTURY	Century overflow interrupt Default Value: 0
1	ALARM2	Alarm 2 Interrupt Default Value: 0
0	ALARM1	Alarm 1 Interrupt Default Value: 0

11.1.12 BACKUP_INTR_SET

Interrupt set request register

Address: 0x40270030

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW1S	RW1S	RW1S
HW Access	None					A	A	A
Name	None [7:3]					CENTURY	ALARM2	ALARM1

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	CENTURY	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
1	ALARM2	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	ALARM1	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

11.1.13 BACKUP_INTR_MASK

Interrupt mask register

Address: 0x40270034

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [7:3]					CENTURY	ALARM2	ALARM1

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	CENTURY	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	ALARM2	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	ALARM1	Mask bit for corresponding bit in interrupt request register. Default Value: 0

11.1.14 BACKUP_INTR_MASKED

Interrupt masked request register

Address: 0x40270038

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					R	R	R
HW Access	None					RW	RW	RW
Name	None [7:3]					CENTURY	ALARM2	ALARM1

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	CENTURY	Logical and of corresponding request and mask bits. Default Value: 0
1	ALARM2	Logical and of corresponding request and mask bits. Default Value: 0
0	ALARM1	Logical and of corresponding request and mask bits. Default Value: 0

11.1.15 BACKUP_OSCCNT

32kHz oscillator counter

Address: 0x4027003C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	A							
Name	CNT32KHZ [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	CNT32KHZ	32kHz oscillator count (msb=128Hz), calibration can cause bit 6 to skip. Reset when RTC_-TIME.RTC_SEC fields is written. Default Value: 0

11.1.16 BACKUP_TICKS

128Hz tick counter

Address: 0x40270040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R					
HW Access	None		A					
Name	None [7:6]		CNT128HZ [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	CNT128HZ	128Hz counter (msb=2Hz) When SECONDS is written this field will be reset. Default Value: 0

11.1.17 BACKUP_PMIC_CTL

PMIC control register

Address: 0x40270044

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	UNLOCK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							A
Name	None [23:17]							POLARITY

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW1S	RW	None				
HW Access	A	R	A	None				
Name	PMIC_EN	PMIC_AL-WAYSEN	PMIC_EN_OUTEN	None [28:24]				

Bits	Name	Description
31	PMIC_EN	Enable for external PMIC that supplies vddd (if present). This bit will only clear if UNLOCK was written correctly in a previous write operation and PMIC_ALWAYSEN=0. When PMIC_EN=0, the system functions normally until vddd is no longer present (OFF w/Backup mode). Firmware can set this bit, if it does so before vddd is actually removed. This bit is also set by any RTC alarm or PMIC pin wakeup event regardless of UNLOCK setting. Default Value: 1
30	PMIC_ALWAYSEN	Override normal PMIC controls to prevent accidentally turning off the PMIC by errant firmware. 0: Normal operation, PMIC_EN and PMIC_OUTEN work as described 1: PMIC_EN and PMIC_OUTEN are ignored and the output pad is forced enabled. Note: This bit is a write-once bit until the next backup reset. Default Value: 0
29	PMIC_EN_OUTEN	Output enable for the output driver in the PMIC_EN pad. 0: Output pad is tristate for PMIC_EN pin. This can allow this pin to be used for another purpose. Tristate condition is kept only if the UNLOCK key (0x3A) is present 1: Output pad is enabled for PMIC_EN pin. Default Value: 1

11.1.17 BACKUP_PMIC_CTL (continued)

16	POLARITY	Set polarity of wakeup signal used to enable the PMIC. Always write this bit "1". 0: reserved for future use, 1: PMIC enables when wakeup signal is high. Default Value: 0
15 : 8	UNLOCK	This byte must be set to 0x3A for PMIC to be disabled. When the UNLOCK code is not present: writes to PMIC_EN field are ignored and the hardware ignores the value in PMIC_EN. Do not change PMIC_EN in the same write cycle as setting/clearing the UNLOCK code; do these in separate write cycles. Default Value: 0

11.1.18 BACKUP_RESET

Backup reset register

Address: 0x40270048

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1S	None						
HW Access	A	None						
Name	RESET	None						

Bits	Name	Description
31	RESET	Writing 1 to this register resets the backup logic. Hardware clears it when the reset is complete. After setting this register, firmware should confirm it reads as 0 before attempting to write other backup registers. Default Value: 0

11.1.19 BACKUP_BREG0

Backup register region

Address: 0x40271000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	BREG [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	BREG [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	A							
Name	BREG [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	A							
Name	BREG [31:24]							

Bits	Name	Description
31 : 0	BREG	Backup memory that contains application-specific data. Memory is retained on vbackup supply. Default Value: 0

11.1.20 BACKUP_TRIM

Trim Register

Address: 0x4027FF00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		TRIM [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	TRIM	WCO trim Default Value: 0

12 Direct Memory Access (DMA) Registers

This section discusses the Direct Memory Access (DMA) registers. It lists all the registers in mapping tables, in address order.

12.1 Register Details

Register	Address	Description
DW0_CTL0	0x40280000	Control
DW0_STATUS0	0x40280004	Status
DW0_PENDING0	0x40280008	Pending channels
DW0_STATUS_INTR0	0x40280010	System interrupt control
DW0_STATUS_INTR_MASKED0	0x40280014	Status of interrupts masked
DW0_ACT_DESCR_CTL0	0x40280020	Active descriptor control
DW0_ACT_DESCR_SRC0	0x40280024	Active descriptor source
DW0_ACT_DESCR_DST0	0x40280028	Active descriptor destination
DW0_ACT_DESCR_X_CTL0	0x40280030	Active descriptor X loop control
DW0_ACT_DESCR_Y_CTL0	0x40280034	Active descriptor Y loop control
DW0_ACT_DESCR_NEXT_PTR0	0x40280038	Active descriptor next pointer
DW0_ACT_SRC0	0x40280040	Active source
DW0_ACT_DST0	0x40280044	Active destination
DW0_CH_STRUCT0_CH_CTL	0x40280800	Channel control
DW0_CH_STRUCT0_CH_STATUS	0x40280804	Channel status
DW0_CH_STRUCT0_CH_IDX	0x40280808	Channel current indices
DW0_CH_STRUCT0_CH_CURR_PTR	0x4028080C	Channel current descriptor pointer
DW0_CH_STRUCT0_INTR	0x40280810	Interrupt
DW0_CH_STRUCT0_INTR_SET	0x40280814	Interrupt set
DW0_CH_STRUCT0_INTR_MASK	0x40280818	Interrupt mask
DW0_CH_STRUCT0_INTR_MASKED	0x4028081C	Interrupt masked
DW0_CH_STRUCT1_CH_CTL	0x40280820	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT1_CH_STATUS	0x40280824	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT1_CH_IDX	0x40280828	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT1_CH_CURR_PTR	0x4028082C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT1_INTR	0x40280830	Interrupt. See DW0_CH_STRUCT0_INTRfor the details of bit fields.

Register	Address	Description
DW0_CH_STRUCT1_INTR_SET	0x40280834	Interrupt set. See DW0_CH_STRUCT0_INTR_SETfor the details of bit fields.
DW0_CH_STRUCT1_INTR_MASK	0x40280838	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT1_INTR_MASKED	0x4028083C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT2_CH_CTL	0x40280840	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT2_CH_STATUS	0x40280844	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT2_CH_IDX	0x40280848	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT2_CH_CURR_PTR	0x4028084C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT2_INTR	0x40280850	Interrupt. See DW0_CH_STRUCT0_INTRfor the details of bit fields.
DW0_CH_STRUCT2_INTR_SET	0x40280854	Interrupt set. See DW0_CH_STRUCT0_INTR_SETfor the details of bit fields.
DW0_CH_STRUCT2_INTR_MASK	0x40280858	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT2_INTR_MASKED	0x4028085C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT3_CH_CTL	0x40280860	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT3_CH_STATUS	0x40280864	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT3_CH_IDX	0x40280868	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT3_CH_CURR_PTR	0x4028086C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT3_INTR	0x40280870	Interrupt. See DW0_CH_STRUCT0_INTRfor the details of bit fields.
DW0_CH_STRUCT3_INTR_SET	0x40280874	Interrupt set. See DW0_CH_STRUCT0_INTR_SETfor the details of bit fields.
DW0_CH_STRUCT3_INTR_MASK	0x40280878	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT3_INTR_MASKED	0x4028087C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT4_CH_CTL	0x40280880	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT4_CH_STATUS	0x40280884	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT4_CH_IDX	0x40280888	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT4_CH_CURR_PTR	0x4028088C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT4_INTR	0x40280890	Interrupt. See DW0_CH_STRUCT0_INTRfor the details of bit fields.
DW0_CH_STRUCT4_INTR_SET	0x40280894	Interrupt set. See DW0_CH_STRUCT0_INTR_SETfor the details of bit fields.
DW0_CH_STRUCT4_INTR_MASK	0x40280898	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT4_INTR_MASKED	0x4028089C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT5_CH_CTL	0x402808A0	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT5_CH_STATUS	0x402808A4	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT5_CH_IDX	0x402808A8	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT5_CH_CURR_PTR	0x402808AC	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.

Register	Address	Description
DW0_CH_STRUCT5_INTR	0x402808B0	Interrupt. See DW0_CH_STRUCT0_INTRfor the details of bit fields.
DW0_CH_STRUCT5_INTR_SET	0x402808B4	Interrupt set. See DW0_CH_STRUCT0_INTR_SETfor the details of bit fields.
DW0_CH_STRUCT5_INTR_MASK	0x402808B8	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT5_INTR_MASKED	0x402808BC	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT6_CH_CTL	0x402808C0	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT6_CH_STATUS	0x402808C4	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT6_CH_IDX	0x402808C8	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT6_CH_CURR_PTR	0x402808CC	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT6_INTR	0x402808D0	Interrupt. See DW0_CH_STRUCT0_INTRfor the details of bit fields.
DW0_CH_STRUCT6_INTR_SET	0x402808D4	Interrupt set. See DW0_CH_STRUCT0_INTR_SETfor the details of bit fields.
DW0_CH_STRUCT6_INTR_MASK	0x402808D8	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT6_INTR_MASKED	0x402808DC	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT7_CH_CTL	0x402808E0	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT7_CH_STATUS	0x402808E4	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT7_CH_IDX	0x402808E8	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT7_CH_CURR_PTR	0x402808EC	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT7_INTR	0x402808F0	Interrupt. See DW0_CH_STRUCT0_INTRfor the details of bit fields.
DW0_CH_STRUCT7_INTR_SET	0x402808F4	Interrupt set. See DW0_CH_STRUCT0_INTR_SETfor the details of bit fields.
DW0_CH_STRUCT7_INTR_MASK	0x402808F8	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT7_INTR_MASKED	0x402808FC	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT8_CH_CTL	0x40280900	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT8_CH_STATUS	0x40280904	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT8_CH_IDX	0x40280908	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT8_CH_CURR_PTR	0x4028090C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT8_INTR	0x40280910	Interrupt. See DW0_CH_STRUCT0_INTRfor the details of bit fields.
DW0_CH_STRUCT8_INTR_SET	0x40280914	Interrupt set. See DW0_CH_STRUCT0_INTR_SETfor the details of bit fields.
DW0_CH_STRUCT8_INTR_MASK	0x40280918	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT8_INTR_MASKED	0x4028091C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT9_CH_CTL	0x40280920	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT9_CH_STATUS	0x40280924	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT9_CH_IDX	0x40280928	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.

Register	Address	Description
DW0_CH_STRUCT9_CH_CURR_PTR	0x4028092C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT9_INTR	0x40280930	Interrupt. See DW0_CH_STRUCT0_INTRfor the details of bit fields.
DW0_CH_STRUCT9_INTR_SET	0x40280934	Interrupt set. See DW0_CH_STRUCT0_INTR_SETfor the details of bit fields.
DW0_CH_STRUCT9_INTR_MASK	0x40280938	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT9_INTR_MASKED	0x4028093C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT10_CH_CTL	0x40280940	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT10_CH_STATUS	0x40280944	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT10_CH_IDX	0x40280948	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT10_CH_CURR_PTR	0x4028094C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT10_INTR	0x40280950	Interrupt. See DW0_CH_STRUCT0_INTRfor the details of bit fields.
DW0_CH_STRUCT10_INTR_SET	0x40280954	Interrupt set. See DW0_CH_STRUCT0_INTR_SETfor the details of bit fields.
DW0_CH_STRUCT10_INTR_MASK	0x40280958	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT10_INTR_MASKED	0x4028095C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT11_CH_CTL	0x40280960	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT11_CH_STATUS	0x40280964	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT11_CH_IDX	0x40280968	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT11_CH_CURR_PTR	0x4028096C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT11_INTR	0x40280970	Interrupt. See DW0_CH_STRUCT0_INTRfor the details of bit fields.
DW0_CH_STRUCT11_INTR_SET	0x40280974	Interrupt set. See DW0_CH_STRUCT0_INTR_SETfor the details of bit fields.
DW0_CH_STRUCT11_INTR_MASK	0x40280978	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT11_INTR_MASKED	0x4028097C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT12_CH_CTL	0x40280980	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT12_CH_STATUS	0x40280984	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT12_CH_IDX	0x40280988	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT12_CH_CURR_PTR	0x4028098C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT12_INTR	0x40280990	Interrupt. See DW0_CH_STRUCT0_INTRfor the details of bit fields.
DW0_CH_STRUCT12_INTR_SET	0x40280994	Interrupt set. See DW0_CH_STRUCT0_INTR_SETfor the details of bit fields.
DW0_CH_STRUCT12_INTR_MASK	0x40280998	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT12_INTR_MASKED	0x4028099C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT13_CH_CTL	0x402809A0	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT13_CH_STATUS	0x402809A4	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.

Register	Address	Description
DW0_CH_STRUCT13_CH_IDX	0x402809A8	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT13_CH_CURR_PTR	0x402809AC	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT13_INTR	0x402809B0	Interrupt. See DW0_CH_STRUCT0_INTRfor the details of bit fields.
DW0_CH_STRUCT13_INTR_SET	0x402809B4	Interrupt set. See DW0_CH_STRUCT0_INTR_SETfor the details of bit fields.
DW0_CH_STRUCT13_INTR_MASK	0x402809B8	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT13_INTR_MASKED	0x402809BC	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT14_CH_CTL	0x402809C0	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT14_CH_STATUS	0x402809C4	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT14_CH_IDX	0x402809C8	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT14_CH_CURR_PTR	0x402809CC	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT14_INTR	0x402809D0	Interrupt. See DW0_CH_STRUCT0_INTRfor the details of bit fields.
DW0_CH_STRUCT14_INTR_SET	0x402809D4	Interrupt set. See DW0_CH_STRUCT0_INTR_SETfor the details of bit fields.
DW0_CH_STRUCT14_INTR_MASK	0x402809D8	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT14_INTR_MASKED	0x402809DC	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW0_CH_STRUCT15_CH_CTL	0x402809E0	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW0_CH_STRUCT15_CH_STATUS	0x402809E4	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW0_CH_STRUCT15_CH_IDX	0x402809E8	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW0_CH_STRUCT15_CH_CURR_PTR	0x402809EC	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW0_CH_STRUCT15_INTR	0x402809F0	Interrupt. See DW0_CH_STRUCT0_INTRfor the details of bit fields.
DW0_CH_STRUCT15_INTR_SET	0x402809F4	Interrupt set. See DW0_CH_STRUCT0_INTR_SETfor the details of bit fields.
DW0_CH_STRUCT15_INTR_MASK	0x402809F8	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW0_CH_STRUCT15_INTR_MASKED	0x402809FC	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW1_CTL0	0x40281000	Control. See DW0_CTL0 for the details of bit fields.
DW1_STATUS0	0x40281004	Status. See DW0_STATUS0 for the details of bit fields.
DW1_PENDING0	0x40281008	Pending channels. See DW0_PENDING0 for the details of bit fields.
DW1_STATUS_INTR0	0x40281010	System interrupt control. See DW0_STATUS_INTR0 for the details of bit fields.
DW1_STATUS_INTR_MASKED0	0x40281014	Status of interrupts masked. See DW0_STATUS_INTR_MASKED0 for the details of bit fields.
DW1_ACT_DESCR_CTL0	0x40281020	Active descriptor control. See DW0_ACT_DESCR_CTL0 for the details of bit fields.
DW1_ACT_DESCR_SRC0	0x40281024	Active descriptor source. See DW0_ACT_DESCR_SRC0 for the details of bit fields.
DW1_ACT_DESCR_DST0	0x40281028	Active descriptor destination. See DW0_ACT_DESCR_DST0 for the details of bit fields.
DW1_ACT_DESCR_X_CTL0	0x40281030	Active descriptor X loop control. See DW0_ACT_DESCR_X_CTL0 for the details of bit fields.

Register	Address	Description
DW1_ACT_DESCR_Y_CTL0	0x40281034	Active descriptor Y loop control. See DW0_ACT_DESCR_Y_CTL0 for the details of bit fields.
DW1_ACT_DESCR_NEXT_PTR0	0x40281038	Active descriptor next pointer. See DW0_ACT_DESCR_NEXT_PTR0 for the details of bit fields.
DW1_ACT_SRC0	0x40281040	Active source. See DW0_ACT_SRC0 for the details of bit fields.
DW1_ACT_DST0	0x40281044	Active destination. See DW0_ACT_DST0 for the details of bit fields.
DW1_CH_STRUCT0_CH_CTL	0x40281800	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW1_CH_STRUCT0_CH_STATUS	0x40281804	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW1_CH_STRUCT0_CH_IDX	0x40281808	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW1_CH_STRUCT0_CH_CURR_PTR	0x4028180C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW1_CH_STRUCT0_INTR	0x40281810	Interrupt. See DW0_CH_STRUCT0_INTRfor the details of bit fields.
DW1_CH_STRUCT0_INTR_SET	0x40281814	Interrupt set. See DW0_CH_STRUCT0_INTR_SETfor the details of bit fields.
DW1_CH_STRUCT0_INTR_MASK	0x40281818	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASKfor the details of bit fields.
DW1_CH_STRUCT0_INTR_MASKED	0x4028181C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKEDfor the details of bit fields.
DW1_CH_STRUCT1_CH_CTL	0x40281820	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW1_CH_STRUCT1_CH_STATUS	0x40281824	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW1_CH_STRUCT1_CH_IDX	0x40281828	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW1_CH_STRUCT1_CH_CURR_PTR	0x4028182C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW1_CH_STRUCT1_INTR	0x40281830	Interrupt. See DW0_CH_STRUCT0_INTRfor the details of bit fields.
DW1_CH_STRUCT1_INTR_SET	0x40281834	Interrupt set. See DW0_CH_STRUCT0_INTR_SETfor the details of bit fields.
DW1_CH_STRUCT1_INTR_MASK	0x40281838	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW1_CH_STRUCT1_INTR_MASKED	0x4028183C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW1_CH_STRUCT2_CH_CTL	0x40281840	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW1_CH_STRUCT2_CH_STATUS	0x40281844	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW1_CH_STRUCT2_CH_IDX	0x40281848	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW1_CH_STRUCT2_CH_CURR_PTR	0x4028184C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW1_CH_STRUCT2_INTR	0x40281850	Interrupt. See DW0_CH_STRUCT0_INTRfor the details of bit fields.
DW1_CH_STRUCT2_INTR_SET	0x40281854	Interrupt set. See DW0_CH_STRUCT0_INTR_SETfor the details of bit fields.
DW1_CH_STRUCT2_INTR_MASK	0x40281858	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW1_CH_STRUCT2_INTR_MASKED	0x4028185C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW1_CH_STRUCT3_CH_CTL	0x40281860	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW1_CH_STRUCT3_CH_STATUS	0x40281864	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW1_CH_STRUCT3_CH_IDX	0x40281868	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.

Register	Address	Description
DW1_CH_STRUCT3_CH_CURR_PTR	0x4028186C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW1_CH_STRUCT3_INTR	0x40281870	Interrupt. See DW0_CH_STRUCT0_INTRfor the details of bit fields.
DW1_CH_STRUCT3_INTR_SET	0x40281874	Interrupt set. See DW0_CH_STRUCT0_INTR_SETfor the details of bit fields.
DW1_CH_STRUCT3_INTR_MASK	0x40281878	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW1_CH_STRUCT3_INTR_MASKED	0x4028187C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW1_CH_STRUCT4_CH_CTL	0x40281880	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW1_CH_STRUCT4_CH_STATUS	0x40281884	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW1_CH_STRUCT4_CH_IDX	0x40281888	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW1_CH_STRUCT4_CH_CURR_PTR	0x4028188C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW1_CH_STRUCT4_INTR	0x40281890	Interrupt. See DW0_CH_STRUCT0_INTRfor the details of bit fields.
DW1_CH_STRUCT4_INTR_SET	0x40281894	Interrupt set. See DW0_CH_STRUCT0_INTR_SETfor the details of bit fields.
DW1_CH_STRUCT4_INTR_MASK	0x40281898	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW1_CH_STRUCT4_INTR_MASKED	0x4028189C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW1_CH_STRUCT5_CH_CTL	0x402818A0	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW1_CH_STRUCT5_CH_STATUS	0x402818A4	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW1_CH_STRUCT5_CH_IDX	0x402818A8	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW1_CH_STRUCT5_CH_CURR_PTR	0x402818AC	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW1_CH_STRUCT5_INTR	0x402818B0	Interrupt. See DW0_CH_STRUCT0_INTRfor the details of bit fields.
DW1_CH_STRUCT5_INTR_SET	0x402818B4	Interrupt set. See DW0_CH_STRUCT0_INTR_SETfor the details of bit fields.
DW1_CH_STRUCT5_INTR_MASK	0x402818B8	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW1_CH_STRUCT5_INTR_MASKED	0x402818BC	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW1_CH_STRUCT6_CH_CTL	0x402818C0	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW1_CH_STRUCT6_CH_STATUS	0x402818C4	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW1_CH_STRUCT6_CH_IDX	0x402818C8	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW1_CH_STRUCT6_CH_CURR_PTR	0x402818CC	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW1_CH_STRUCT6_INTR	0x402818D0	Interrupt. See DW0_CH_STRUCT0_INTRfor the details of bit fields.
DW1_CH_STRUCT6_INTR_SET	0x402818D4	Interrupt set. See DW0_CH_STRUCT0_INTR_SETfor the details of bit fields.
DW1_CH_STRUCT6_INTR_MASK	0x402818D8	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW1_CH_STRUCT6_INTR_MASKED	0x402818DC	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW1_CH_STRUCT7_CH_CTL	0x402818E0	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW1_CH_STRUCT7_CH_STATUS	0x402818E4	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.

Register	Address	Description
DW1_CH_STRUCT7_CH_IDX	0x402818E8	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW1_CH_STRUCT7_CH_CURR_PTR	0x402818EC	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW1_CH_STRUCT7_INTR	0x402818F0	Interrupt. See DW0_CH_STRUCT0_INTRfor the details of bit fields.
DW1_CH_STRUCT7_INTR_SET	0x402818F4	Interrupt set. See DW0_CH_STRUCT0_INTR_SETfor the details of bit fields.
DW1_CH_STRUCT7_INTR_MASK	0x402818F8	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW1_CH_STRUCT7_INTR_MASKED	0x402818FC	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW1_CH_STRUCT8_CH_CTL	0x40281900	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW1_CH_STRUCT8_CH_STATUS	0x40281904	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW1_CH_STRUCT8_CH_IDX	0x40281908	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW1_CH_STRUCT8_CH_CURR_PTR	0x4028190C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW1_CH_STRUCT8_INTR	0x40281910	Interrupt. See DW0_CH_STRUCT0_INTRfor the details of bit fields.
DW1_CH_STRUCT8_INTR_SET	0x40281914	Interrupt set. See DW0_CH_STRUCT0_INTR_SETfor the details of bit fields.
DW1_CH_STRUCT8_INTR_MASK	0x40281918	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW1_CH_STRUCT8_INTR_MASKED	0x4028191C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW1_CH_STRUCT9_CH_CTL	0x40281920	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW1_CH_STRUCT9_CH_STATUS	0x40281924	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW1_CH_STRUCT9_CH_IDX	0x40281928	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW1_CH_STRUCT9_CH_CURR_PTR	0x4028192C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW1_CH_STRUCT9_INTR	0x40281930	Interrupt. See DW0_CH_STRUCT0_INTRfor the details of bit fields.
DW1_CH_STRUCT9_INTR_SET	0x40281934	Interrupt set. See DW0_CH_STRUCT0_INTR_SETfor the details of bit fields.
DW1_CH_STRUCT9_INTR_MASK	0x40281938	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW1_CH_STRUCT9_INTR_MASKED	0x4028193C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW1_CH_STRUCT10_CH_CTL	0x40281940	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW1_CH_STRUCT10_CH_STATUS	0x40281944	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW1_CH_STRUCT10_CH_IDX	0x40281948	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW1_CH_STRUCT10_CH_CURR_PTR	0x4028194C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW1_CH_STRUCT10_INTR	0x40281950	Interrupt. See DW0_CH_STRUCT0_INTRfor the details of bit fields.
DW1_CH_STRUCT10_INTR_SET	0x40281954	Interrupt set. See DW0_CH_STRUCT0_INTR_SETfor the details of bit fields.
DW1_CH_STRUCT10_INTR_MASK	0x40281958	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW1_CH_STRUCT10_INTR_MASKED	0x4028195C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW1_CH_STRUCT11_CH_CTL	0x40281960	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.

Register	Address	Description
DW1_CH_STRUCT11_CH_STATUS	0x40281964	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW1_CH_STRUCT11_CH_IDX	0x40281968	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW1_CH_STRUCT11_CH_CURR_PTR	0x4028196C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW1_CH_STRUCT11_INTR	0x40281970	Interrupt. See DW0_CH_STRUCT0_INTRfor the details of bit fields.
DW1_CH_STRUCT11_INTR_SET	0x40281974	Interrupt set. See DW0_CH_STRUCT0_INTR_SETfor the details of bit fields.
DW1_CH_STRUCT11_INTR_MASK	0x40281978	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW1_CH_STRUCT11_INTR_MASKED	0x4028197C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW1_CH_STRUCT12_CH_CTL	0x40281980	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW1_CH_STRUCT12_CH_STATUS	0x40281984	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW1_CH_STRUCT12_CH_IDX	0x40281988	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW1_CH_STRUCT12_CH_CURR_PTR	0x4028198C	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW1_CH_STRUCT12_INTR	0x40281990	Interrupt. See DW0_CH_STRUCT0_INTRfor the details of bit fields.
DW1_CH_STRUCT12_INTR_SET	0x40281994	Interrupt set. See DW0_CH_STRUCT0_INTR_SETfor the details of bit fields.
DW1_CH_STRUCT12_INTR_MASK	0x40281998	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW1_CH_STRUCT12_INTR_MASKED	0x4028199C	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW1_CH_STRUCT13_CH_CTL	0x402819A0	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW1_CH_STRUCT13_CH_STATUS	0x402819A4	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW1_CH_STRUCT13_CH_IDX	0x402819A8	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW1_CH_STRUCT13_CH_CURR_PTR	0x402819AC	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW1_CH_STRUCT13_INTR	0x402819B0	Interrupt. See DW0_CH_STRUCT0_INTRfor the details of bit fields.
DW1_CH_STRUCT13_INTR_SET	0x402819B4	Interrupt set. See DW0_CH_STRUCT0_INTR_SETfor the details of bit fields.
DW1_CH_STRUCT13_INTR_MASK	0x402819B8	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW1_CH_STRUCT13_INTR_MASKED	0x402819BC	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.
DW1_CH_STRUCT14_CH_CTL	0x402819C0	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW1_CH_STRUCT14_CH_STATUS	0x402819C4	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW1_CH_STRUCT14_CH_IDX	0x402819C8	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW1_CH_STRUCT14_CH_CURR_PTR	0x402819CC	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW1_CH_STRUCT14_INTR	0x402819D0	Interrupt. See DW0_CH_STRUCT0_INTRfor the details of bit fields.
DW1_CH_STRUCT14_INTR_SET	0x402819D4	Interrupt set. See DW0_CH_STRUCT0_INTR_SETfor the details of bit fields.
DW1_CH_STRUCT14_INTR_MASK	0x402819D8	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW1_CH_STRUCT14_INTR_MASKED	0x402819DC	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.

Register	Address	Description
DW1_CH_STRUCT15_CH_CTL	0x402819E0	Channel control. See DW0_CH_STRUCT0_CH_CTL for the details of bit fields.
DW1_CH_STRUCT15_CH_STATUS	0x402819E4	Channel status. See DW0_CH_STRUCT0_CH_STATUS for the details of bit fields.
DW1_CH_STRUCT15_CH_IDX	0x402819E8	Channel current indices. See DW0_CH_STRUCT0_CH_IDX for the details of bit fields.
DW1_CH_STRUCT15_CH_CURR_PTR	0x402819EC	Channel current descriptor pointer. See DW0_CH_STRUCT0_CH_CURR_PTR for the details of bit fields.
DW1_CH_STRUCT15_INTR	0x402819F0	Interrupt. See DW0_CH_STRUCT0_INTRfor the details of bit fields.
DW1_CH_STRUCT15_INTR_SET	0x402819F4	Interrupt set. See DW0_CH_STRUCT0_INTR_SETfor the details of bit fields.
DW1_CH_STRUCT15_INTR_MASK	0x402819F8	Interrupt mask. See DW0_CH_STRUCT0_INTR_MASK for the details of bit fields.
DW1_CH_STRUCT15_INTR_MASKED	0x402819FC	Interrupt masked. See DW0_CH_STRUCT0_INTR_MASKED for the details of bit fields.

12.1.1 DW0_CTL0

Control

Address: 0x40280000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	ENABLED	None						

Bits	**Name**	**Description**
31	ENABLED	IP enable: '0': Disabled. Disabling the IP activates the IP's Active logic reset: Active logic and non-retention MMIO registers are reset (retention MMIO registers are not affected). '1': Enabled. Default Value: 0

12.1.2 DW0_STATUS0

Status

Address: 0x40280004

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				None	R	R	R
HW Access	RW				None	RW	RW	RW
Name	PC [7:4]				None	B	NS	P

Bits	15	14	13	12	11	10	9	8
SW Access	None			R				
HW Access	None			W				
Name	None [15:13]			CH_IDX [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	None	R			None	R	R	
HW Access	None	W			None	W	W	
Name	None	STATE [22:20]			None	PREEMPT-ABLE	PRIO [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	ACTIVE	None [30:24]						

Bits	Name	Description
31	ACTIVE	Active channel present: 0: No. 1: Yes. Default Value: 0
22 : 20	STATE	State of the DW controller. 0: Default/inactive state. 1: Loading descriptor. 2: Loading data element from source location. 3: Storing data element to destination location. 4: Update of active control information (e.g. source and destination addresses). 5: Wait for trigger de-activation. Default Value: 0
18	PREEMPTABLE	Active channel preemptable. Default Value: Undefined
17 : 16	PRIO	Active channel priority. Default Value: Undefined

12.1.2 DW0_STATUS0 (continued)

12 : 8	CH_IDX	Active channel index. Default Value: Undefined
7 : 4	PC	Active channel protection context. Default Value: Undefined
2	B	Active channel, non-bufferable/bufferable access control: '0': non-bufferable '1': bufferable. Default Value: Undefined
1	NS	Active channel, secure/non-secure access control: '0': secure. '1': non-secure. Default Value: Undefined
0	P	Active channel, user/privileged access control: '0': user mode. '1': privileged mode. Default Value: Undefined

12.1.3 DW0_PENDING0

Pending channels

Address: 0x40280008

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	CH_PENDING [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	CH_PENDING [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CH_PENDING	Specifies pending DW channels; i.e. enabled channels whose trigger got activated. This field includes all channels that are in the pending state (not scheduled) or active state (scheduled and performing data transfer(s)). Default Value: 0

12.1.4 DW0_STATUS_INTR0

System interrupt control

Address: 0x40280010

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	CH [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	CH [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CH	Reflects the INTR.CH bit fields of all channels. Default Value: 0

12.1.5 DW0_STATUS_INTR_MASKED0

Status of interrupts masked

Address: 0x40280014

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	CH [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	CH [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CH	Reflects the INTR_MASKED.CH bit fields of all channels. Default Value: 0

12.1.6 DW0_ACT_DESCR_CTL0

Active descriptor control

Address: 0x40280020

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Copy of DESCR_CTL of the currently active descriptor. Default Value: Undefined

12.1.7 DW0_ACT_DESCR_SRC0

Active descriptor source

Address: 0x40280024

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Copy of DESCR_SRC of the currently active descriptor. Default Value: Undefined

12.1.8 DW0_ACT_DESCR_DST0

Active descriptor destination

Address: 0x40280028

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Copy of DESCR_DST of the currently active descriptor. Default Value: Undefined

12.1.9 DW0_ACT_DESCR_X_CTL0

Active descriptor X loop control

Address: 0x40280030

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Copy of DESCR_X_CTL of the currently active descriptor. Default Value: Undefined

12.1.10 DW0_ACT_DESCR_Y_CTL0

Active descriptor Y loop control

Address: 0x40280034

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Copy of DESCR_Y_CTL of the currently active descriptor. Default Value: Undefined

12.1.11 DW0_ACT_DESCR_NEXT_PTR0

Active descriptor next pointer

Address: 0x40280038

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R						None	
HW Access	W						None	
Name	ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 2	ADDR	Copy of DESCR_NEXT_PTR of the currently active descriptor. Default Value: Undefined

12.1.12 DW0_ACT_SRC0

Active source

Address: 0x40280040

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	SRC_ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	SRC_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	SRC_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	SRC_ADDR [31:24]							

Bits	Name	Description
31 : 0	SRC_ADDR	Current address of source location. Default Value: Undefined

12.1.13 DW0_ACT_DST0

Active destination

Address: 0x40280044

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DST_ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DST_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	DST_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	DST_ADDR [31:24]							

Bits	Name	Description
31 : 0	DST_ADDR	Current address of destination location. Default Value: Undefined

12.1.14 DW0_CH_STRUCT0_CH_CTL

Channel control

Address: 0x40280800

Retention: Retained

Bits	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SW Access	RW				None	RW	RW	RW
HW Access	R				None	R	R	R
Name	PC [7:4]				None	B	NS	P

Bits	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SW Access	None					RW	RW	
HW Access	None					R	R	
Name	None [23:19]					PREEMPT-ABLE	PRIO [17:16]	

Bits	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**
SW Access	RW	None						
HW Access	RW1C	None						
Name	ENABLED	None [30:24]						

Bits	**Name**	**Description**
31	ENABLED	Channel enable: 0: Disabled. The channels trigger is ignored and the channel cannot be made pending and therefore cannot be made active. If a pending channel is disabled, the channel is made non pending. If the activate channel is disabled, the channel is de-activated (bus transactions are completed). 1: Enabled. SW sets this field to 1 to enable a specific channel. HW sets this field to 0 on an error interrupt cause (the specific error is specified by CH_STATUS.INTR_CAUSE). Default Value: 0
18	PREEMPTABLE	Specifies if the channel is preemptable. '0': Not preemptable. 1: Preemptable. This field allows higher priority pending channels (from a higher priority group; i.e. an active channel can NOT be preempted by a pending channel in the same priority group) to preempt the active channel in between "single transfers" (a 1D transfer consists out of X_COUNT single transfers; a 2D transfer consists out of X_COUNT*Y_COUNT single transfers). Preemption will NOT affect the pending status of channel. As a result, after completion of a higher priority activated channel, the current channel may be reactivated. Default Value: 0

12.1.14 DW0_CH_STRUCT0_CH_CTL (continued)

17 : 16	PRIO	Channel priority: 0: highest priority. "1" "2" 3: lowest priority. Channels with the same priority constitute a priority group. Priority decoding determines the highest priority pending channel. This channel is determined as follows. First, the highest priority group with pending channels is identified. Second, within this priority group, round robin arbitration is applied. Round robin arbitration (within a priority group) gives the highest priority to the lower channel indices (within the priority group). Default Value: 0
7 : 4	PC	Protection context. This field is set with the protection context of the transaction that writes this register; i.e. the 'write data' is ignored and instead the context is inherited from the write transaction (note the field attributes should be HW:RW, SW:R). All transactions for this channel uses the PC field for the protection context. Default Value: 0
2	B	Non-bufferable/bufferable access control: '0': non-bufferable. '1': bufferable. This field is used to indicate to an AMBA bridge that a write transaction can complete without waiting for the destination to accept the write transaction data. All transactions for this channel uses the B field for the non-bufferable/bufferable access control ("hprot[2]"). Default Value: 0
1	NS	Secure/on-secure access control: '0': secure. '1': non-secure. This field is set with the secure/non-secure access control of the transaction that writes this register; i.e. the 'write data' is ignored and instead the access control is inherited from the write transaction (note the field attributes should be HW:RW, SW:R). All transactions for this channel use the NS field for the secure/non-secure access control ("hprot[4]"). Default Value: 1
0	P	User/privileged access control: '0': user mode. '1': privileged mode. This field is set with the user/privileged access control of the transaction that writes this register; i.e. the 'write data' is ignored and instead the access control is inherited from the write transaction (note the field attributes should be HW:RW, SW:R). All transactions for this channel use the P field for the user/privileged access control ("hprot[1]"). Default Value: 0

12.1.15 DW0_CH_STRUCT0_CH_STATUS

Channel status

Address: 0x40280804

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R			
HW Access	None				W			
Name	None [7:4]				INTR_CAUSE [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	INTR_CAUSE	Specifies the source of the interrupt cause: "0": NO_INTR "1": COMPLETION "2": SRC_BUS_ERROR "3": DST_BUS_ERROR "4": SRC_MISAL "5": DST_MISAL "6": CURR_PTR_NULL "7": ACTIVE_CH_DISABLED "8": DESCR_BUS_ERROR "9"-"15": Not used. For error related interrupt causes (INTR_CAUSE is "2", "3", ..., "8"), the channel is disabled (HW sets CH_CTL.ENABLED to '0'). Default Value: Undefined

12.1.16 DW0_CH_STRUCT0_CH_IDX

Channel current indices

Address: 0x40280808

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	X_IDX [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	Y_IDX [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 8	Y_IDX	Specifies the Y loop index, with X_COUNT taken from the current descriptor. Note: HW sets this field to "0" when it updates the current descriptor pointer CH_CURR_PTR with DESCR_NEXT_PTR after execution of the current descriptor. Note: SW should set this field to "0" when it updates CH_CURR_PTR. Default Value: Undefined
7 : 0	X_IDX	Specifies the X loop index. In the range of [0, X_COUNT], with X_COUNT taken from the current descriptor. Note: HW sets this field to "0" when it updates the current descriptor pointer CH_CURR_PTR with DESCR_NEXT_PTR after execution of the current descriptor. Note: SW should set this field to "0" when it updates CH_CURR_PTR. Default Value: Undefined

12.1.17 DW0_CH_STRUCT0_CH_CURR_PTR

Channel current descriptor pointer

Address: 0x4028080C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW						None	
HW Access	RW						None	
Name	ADDR [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 2	ADDR	Address of current descriptor. When this field is "0", there is no valid descriptor. Note: HW updates the current descriptor pointer CH_CURR_PTR with DESCR_NEXT_PTR after execution of the current descriptor. Note: Typically, when SW updates the current descriptor pointer CH_CURR_PTR, it also sets CH_IDX.X_IDX and CH_IDX.Y_IDX to "0". Default Value: Undefined

12.1.18 DW0_CH_STRUCT0_INTR

Interrupt

Address: 0x40280810

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1C
HW Access	None							RW1S
Name	None [7:1]							CH

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	CH	Set to '1', when event (as specified by CH_STATUS.INTR_CAUSE) is detected. Write INTR.CH field with '1', to clear bit. Write INTR_SET.CH field with '1', to set bit. Default Value: 0

12.1.19 DW0_CH_STRUCT0_INTR_SET

Interrupt set

Address: 0x40280814

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1S
HW Access	None							A
Name	None [7:1]							CH

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	CH	Write INTR_SET field with '1' to set corresponding INTR.CH field (a write of '0' has no effect). Default Value: 0

12.1.20 DW0_CH_STRUCT0_INTR_MASK

Interrupt mask

Address: 0x40280818

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							CH

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	CH	Mask for corresponding field in INTR register. Default Value: 0

12.1.21 DW0_CH_STRUCT0_INTR_MASKED

Interrupt masked

Address: 0x4028081C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							W
Name	None [7:1]							CH

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	CH	Logical and of corresponding INTR and INTR_MASK fields. Default Value: 0

13 eFuse Registers

This section discusses the eFuse registers. It lists all the registers in mapping tables, in address order.

13.1 Register Details

Register	Address	Description
EFUSE_DATA_DEAD_ACCESS_RESTRICT0	0x402C0827	DEAD access restrictions
EFUSE_DATA_DEAD_ACCESS_RESTRICT1	0x402C0828	DEAD access restrictions
EFUSE_DATA_SECURE_ACCESS_RESTRICT0	0x402C0829	SECURE access restrictions
EFUSE_DATA_SECURE_ACCESS_RESTRICT1	0x402C082A	SECURE access restrictions
EFUSE_DATA_LIFECYCLE_STAGE	0x402C082B	NORMAL, SECURE_WITH_DEBUG, and SECURE fuse bits
EFUSE_DATA_CUSTOMER_DATA0	0x402C0840	Customer data
EFUSE_DATA_CUSTOMER_DATA1	0x402C0841	Customer data. See EFUSE_DATA_CUSTOMER_DATA0 for the details of bit fields.
EFUSE_DATA_CUSTOMER_DATA2	0x402C0842	Customer data. See EFUSE_DATA_CUSTOMER_DATA0 for the details of bit fields.
EFUSE_DATA_CUSTOMER_DATA3	0x402C0843	Customer data. See EFUSE_DATA_CUSTOMER_DATA0 for the details of bit fields.
EFUSE_DATA_CUSTOMER_DATA4	0x402C0844	Customer data. See EFUSE_DATA_CUSTOMER_DATA0 for the details of bit fields.
EFUSE_DATA_CUSTOMER_DATA5	0x402C0845	Customer data. See EFUSE_DATA_CUSTOMER_DATA0 for the details of bit fields.
EFUSE_DATA_CUSTOMER_DATA6	0x402C0846	Customer data. See EFUSE_DATA_CUSTOMER_DATA0 for the details of bit fields.
EFUSE_DATA_CUSTOMER_DATA7	0x402C0847	Customer data. See EFUSE_DATA_CUSTOMER_DATA0 for the details of bit fields.
EFUSE_DATA_CUSTOMER_DATA8	0x402C0848	Customer data. See EFUSE_DATA_CUSTOMER_DATA0 for the details of bit fields.
EFUSE_DATA_CUSTOMER_DATA9	0x402C0849	Customer data. See EFUSE_DATA_CUSTOMER_DATA0 for the details of bit fields.
EFUSE_DATA_CUSTOMER_DATA10	0x402C084A	Customer data. See EFUSE_DATA_CUSTOMER_DATA0 for the details of bit fields.
EFUSE_DATA_CUSTOMER_DATA11	0x402C084B	Customer data. See EFUSE_DATA_CUSTOMER_DATA0 for the details of bit fields.
EFUSE_DATA_CUSTOMER_DATA12	0x402C084C	Customer data. See EFUSE_DATA_CUSTOMER_DATA0 for the details of bit fields.
EFUSE_DATA_CUSTOMER_DATA13	0x402C084D	Customer data. See EFUSE_DATA_CUSTOMER_DATA0 for the details of bit fields.
EFUSE_DATA_CUSTOMER_DATA14	0x402C084E	Customer data. See EFUSE_DATA_CUSTOMER_DATA0 for the details of bit fields.
EFUSE_DATA_CUSTOMER_DATA15	0x402C084F	Customer data. See EFUSE_DATA_CUSTOMER_DATA0 for the details of bit fields.
EFUSE_DATA_CUSTOMER_DATA16	0x402C0850	Customer data. See EFUSE_DATA_CUSTOMER_DATA0 for the details of bit fields.
EFUSE_DATA_CUSTOMER_DATA17	0x402C0851	Customer data. See EFUSE_DATA_CUSTOMER_DATA0 for the details of bit fields.
EFUSE_DATA_CUSTOMER_DATA18	0x402C0852	Customer data. See EFUSE_DATA_CUSTOMER_DATA0 for the details of bit fields.
EFUSE_DATA_CUSTOMER_DATA19	0x402C0853	Customer data. See EFUSE_DATA_CUSTOMER_DATA0 for the details of bit fields.
EFUSE_DATA_CUSTOMER_DATA20	0x402C0854	Customer data. See EFUSE_DATA_CUSTOMER_DATA0 for the details of bit fields.
EFUSE_DATA_CUSTOMER_DATA21	0x402C0855	Customer data. See EFUSE_DATA_CUSTOMER_DATA0 for the details of bit fields.

Register	Address	Description
EFUSE_DATA_CUSTOMER_DATA22	0x402C0856	Customer data. See EFUSE_DATA_CUSTOMER_DATA0 for the details of bit fields.
EFUSE_DATA_CUSTOMER_DATA23	0x402C0857	Customer data. See EFUSE_DATA_CUSTOMER_DATA0 for the details of bit fields.
EFUSE_DATA_CUSTOMER_DATA24	0x402C0858	Customer data. See EFUSE_DATA_CUSTOMER_DATA0 for the details of bit fields.
EFUSE_DATA_CUSTOMER_DATA25	0x402C0859	Customer data. See EFUSE_DATA_CUSTOMER_DATA0 for the details of bit fields.
EFUSE_DATA_CUSTOMER_DATA26	0x402C085A	Customer data. See EFUSE_DATA_CUSTOMER_DATA0 for the details of bit fields.
EFUSE_DATA_CUSTOMER_DATA27	0x402C085B	Customer data. See EFUSE_DATA_CUSTOMER_DATA0 for the details of bit fields.
EFUSE_DATA_CUSTOMER_DATA28	0x402C085C	Customer data. See EFUSE_DATA_CUSTOMER_DATA0 for the details of bit fields.
EFUSE_DATA_CUSTOMER_DATA29	0x402C085D	Customer data. See EFUSE_DATA_CUSTOMER_DATA0 for the details of bit fields.
EFUSE_DATA_CUSTOMER_DATA30	0x402C085E	Customer data. See EFUSE_DATA_CUSTOMER_DATA0 for the details of bit fields.
EFUSE_DATA_CUSTOMER_DATA31	0x402C085F	Customer data. See EFUSE_DATA_CUSTOMER_DATA0 for the details of bit fields.
EFUSE_DATA_CUSTOMER_DATA32	0x402C0860	Customer data. See EFUSE_DATA_CUSTOMER_DATA0 for the details of bit fields.
EFUSE_DATA_CUSTOMER_DATA33	0x402C0861	Customer data. See EFUSE_DATA_CUSTOMER_DATA0 for the details of bit fields.
EFUSE_DATA_CUSTOMER_DATA34	0x402C0862	Customer data. See EFUSE_DATA_CUSTOMER_DATA0 for the details of bit fields.
EFUSE_DATA_CUSTOMER_DATA35	0x402C0863	Customer data. See EFUSE_DATA_CUSTOMER_DATA0 for the details of bit fields.
EFUSE_DATA_CUSTOMER_DATA36	0x402C0864	Customer data. See EFUSE_DATA_CUSTOMER_DATA0 for the details of bit fields.
EFUSE_DATA_CUSTOMER_DATA37	0x402C0865	Customer data. See EFUSE_DATA_CUSTOMER_DATA0 for the details of bit fields.
EFUSE_DATA_CUSTOMER_DATA38	0x402C0866	Customer data. See EFUSE_DATA_CUSTOMER_DATA0 for the details of bit fields.
EFUSE_DATA_CUSTOMER_DATA39	0x402C0867	Customer data. See EFUSE_DATA_CUSTOMER_DATA0 for the details of bit fields.
EFUSE_DATA_CUSTOMER_DATA40	0x402C0868	Customer data. See EFUSE_DATA_CUSTOMER_DATA0 for the details of bit fields.
EFUSE_DATA_CUSTOMER_DATA41	0x402C0869	Customer data. See EFUSE_DATA_CUSTOMER_DATA0 for the details of bit fields.
EFUSE_DATA_CUSTOMER_DATA42	0x402C086A	Customer data. See EFUSE_DATA_CUSTOMER_DATA0 for the details of bit fields.
EFUSE_DATA_CUSTOMER_DATA43	0x402C086B	Customer data. See EFUSE_DATA_CUSTOMER_DATA0 for the details of bit fields.
EFUSE_DATA_CUSTOMER_DATA44	0x402C086C	Customer data. See EFUSE_DATA_CUSTOMER_DATA0 for the details of bit fields.
EFUSE_DATA_CUSTOMER_DATA45	0x402C086D	Customer data. See EFUSE_DATA_CUSTOMER_DATA0 for the details of bit fields.
EFUSE_DATA_CUSTOMER_DATA46	0x402C086E	Customer data. See EFUSE_DATA_CUSTOMER_DATA0 for the details of bit fields.
EFUSE_DATA_CUSTOMER_DATA47	0x402C086F	Customer data. See EFUSE_DATA_CUSTOMER_DATA0 for the details of bit fields.
EFUSE_DATA_CUSTOMER_DATA48	0x402C0870	Customer data. See EFUSE_DATA_CUSTOMER_DATA0 for the details of bit fields.
EFUSE_DATA_CUSTOMER_DATA49	0x402C0871	Customer data. See EFUSE_DATA_CUSTOMER_DATA0 for the details of bit fields.
EFUSE_DATA_CUSTOMER_DATA50	0x402C0872	Customer data. See EFUSE_DATA_CUSTOMER_DATA0 for the details of bit fields.
EFUSE_DATA_CUSTOMER_DATA51	0x402C0873	Customer data. See EFUSE_DATA_CUSTOMER_DATA0 for the details of bit fields.
EFUSE_DATA_CUSTOMER_DATA52	0x402C0874	Customer data. See EFUSE_DATA_CUSTOMER_DATA0 for the details of bit fields.
EFUSE_DATA_CUSTOMER_DATA53	0x402C0875	Customer data. See EFUSE_DATA_CUSTOMER_DATA0 for the details of bit fields.
EFUSE_DATA_CUSTOMER_DATA54	0x402C0876	Customer data. See EFUSE_DATA_CUSTOMER_DATA0 for the details of bit fields.
EFUSE_DATA_CUSTOMER_DATA55	0x402C0877	Customer data. See EFUSE_DATA_CUSTOMER_DATA0 for the details of bit fields.
EFUSE_DATA_CUSTOMER_DATA56	0x402C0878	Customer data. See EFUSE_DATA_CUSTOMER_DATA0 for the details of bit fields.
EFUSE_DATA_CUSTOMER_DATA57	0x402C0879	Customer data. See EFUSE_DATA_CUSTOMER_DATA0 for the details of bit fields.
EFUSE_DATA_CUSTOMER_DATA58	0x402C087A	Customer data. See EFUSE_DATA_CUSTOMER_DATA0 for the details of bit fields.
EFUSE_DATA_CUSTOMER_DATA59	0x402C087B	Customer data. See EFUSE_DATA_CUSTOMER_DATA0 for the details of bit fields.
EFUSE_DATA_CUSTOMER_DATA60	0x402C087C	Customer data. See EFUSE_DATA_CUSTOMER_DATA0 for the details of bit fields.
EFUSE_DATA_CUSTOMER_DATA61	0x402C087D	Customer data. See EFUSE_DATA_CUSTOMER_DATA0 for the details of bit fields.
EFUSE_DATA_CUSTOMER_DATA62	0x402C087E	Customer data. See EFUSE_DATA_CUSTOMER_DATA0 for the details of bit fields.
EFUSE_DATA_CUSTOMER_DATA63	0x402C087F	Customer data. See EFUSE_DATA_CUSTOMER_DATA0 for the details of bit fields.

13.1.1 EFUSE_DATA_DEAD_ACCESS_RESTRICT0

DEAD access restrictions

Address: 0x402C0827

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW	RW	RW	RW
HW Access	R		R		R	R	R	R
Name	MMIO_ALLOWED [7:6]		SFLASH_ALLOWED [5:4]		SYS-_AP_M-PU_ENABLE	SYS_DIS-ABLE	CM4_DIS-ABLE	CM0_DIS-ABLE

Bits	Name	Description
7 : 6	MMIO_ALLOWED	This field indicates what portion of the MMIO region is accessible through the system debug access port. Encoding is as follows: 0: All MMIO registers 1: Only IPC MMIO registers accessible (system calls) 2, 3: No MMIO access Default Value: 0
5 : 4	SFLASH_ALLOWED	This field indicates what portion of Supervisory Flash is accessible through the system debug access port. Only a portion of Supervisory Flash starting at the bottom of the area is exposed. Encoding is as follows: 0: entire region 1: 1/2 2: 1/4th 3: nothing Default Value: 0
3	SYS_AP_MPU_ENABLE	Indicates that the MPU on the system debug access port must be programmed and locked according to the settings in the next 5 fields. Default Value: 0
2	SYS_DISABLE	Indicates that this device does not allow access to the system debug access port (DAP). Default Value: 0
1	CM4_DISABLE	Indicates that this device does not allow access to the M4 debug access port (DAP). Default Value: 0
0	CM0_DISABLE	Indicates that this device does not allow access to the M0+ debug access port (DAP). Default Value: 0

13.1.2 EFUSE_DATA_DEAD_ACCESS_RESTRICT1

DEAD access restrictions

Address: 0x402C0828

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW			RW		
HW Access	R	R	R			R		
Name	DI-RECT_EX-ECUTE_DISABLE	UNUSED	SRAM_ALLOWED [5:3]			FLASH_ALLOWED [2:0]		

Bits	Name	Description
7	DIRECT_EXECUTE_DIS-ABLE	Disables DirectExecute system call functionality (implemented in software). Default Value: 0
6	UNUSED	UNUSED Default Value: 0
5 : 3	SRAM_ALLOWED	This field indicates what portion of SRAM 0 is accessible through the system debug access port. Only a portion of SRAM starting at the bottom of the area is exposed. Encoding is the same as FLASH_ALLOWED. Default Value: 0
2 : 0	FLASH_ALLOWED	This field indicates what portion of Main Flash is accessible through the system debug access port. Only a portion of Main Flash starting at the bottom of the area is exposed. Encoding is as follows: 0: entire region 1: 7/8th 2: 3/4th 3: 1/2 4: 1/4th 5: 1/8th 6: 1/16th 7: nothing Default Value: 0

13.1.3 EFUSE_DATA_SECURE_ACCESS_RESTRICT0

SECURE access restrictions

Address: 0x402C0829

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW	RW	RW	RW
HW Access	R		R		R	R	R	R
Name	MMIO_ALLOWED [7:6]		SFLASH_ALLOWED [5:4]		SYS-_AP_M-PU_ENABLE	SYS_DIS-ABLE	CM4_DIS-ABLE	CM0_DIS-ABLE

Bits	Name	Description
7 : 6	MMIO_ALLOWED	This field indicates what portion of the MMIO region is accessible through the system debug access port. Encoding is as follows: 0: All MMIO registers 1: Only IPC MMIO registers accessible (system calls) 2, 3: No MMIO access Default Value: 0
5 : 4	SFLASH_ALLOWED	This field indicates what portion of Supervisory Flash is accessible through the system debug access port. Only a portion of Supervisory Flash starting at the bottom of the area is exposed. Encoding is as follows: 0: entire region 1: 1/2 2: 1/4th 3: nothing Default Value: 0
3	SYS_AP_MPU_ENABLE	Indicates that the MPU on the system debug access port must be programmed and locked according to the settings in the next 5 fields. Default Value: 0
2	SYS_DISABLE	Indicates that this device does not allow access to the system debug access port. Default Value: 0
1	CM4_DISABLE	Indicates that this device does not allow access to the M4 debug access port. Default Value: 0
0	CM0_DISABLE	Indicates that this device does not allow access to the M0+ debug access port. Default Value: 0

13.1.4 EFUSE_DATA_SECURE_ACCESS_RESTRICT1

SECURE access restrictions

Address: 0x402C082A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW			RW		
HW Access	R	R	R			R		
Name	DI-RECT_EX-ECUTE_DI SABLE	SMIF_X-IP_AL-LOWED	SRAM_ALLOWED [5:3]			FLASH_ALLOWED [2:0]		

Bits	Name	Description
7	DIRECT_EXECUTE_DIS-ABLE	Disables DirectExecute system call functionality (implemented in software). Default Value: 0
6	SMIF_XIP_ALLOWED	This field indicates what portion of SMIF_XIP is accessible through the system debug access port. Encoding is as follows: 0: entire region 1: nothing Default Value: 0
5 : 3	SRAM_ALLOWED	This field indicates what portion of SRAM 0 is accessible through the system debug access port. Only a portion of SRAM starting at the bottom of the area is exposed. Encoding is the same as FLASH_ALLOWED. Default Value: 0
2 : 0	FLASH_ALLOWED	This field indicates what portion of Main Flash is accessible through the system debug access port. Only a portion of Main Flash starting at the bottom of the area is exposed. Encoding is as follows: 0: entire region 1: 7/8th 2: 3/4th 3: 1/2 4: 1/4th 5: 1/8th 6: 1/16th 7: nothing Default Value: 0

13.1.5 EFUSE_DATA_LIFECYCLE_STAGE

NORMAL, SECURE_WITH_DEBUG, and SECURE fuse bits

Address: 0x402C082B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [7:4]				RMA	SECURE	SE-CURE_WITH_DEBUG	NORMAL

Bits	Name	Description
3	RMA	This life cycle stage allows one to perform Failure Analysis (FA). The customer transitions the part to RMA life cycle stage when the customer wants Cypress to perform failure analysis on the part. The customer erases all the sensitive data prior to invoking the system call that transitions the part to RMA. Default Value: 0
2	SECURE	This is the life cycle stage of a secure device. Prior to transitioning to this stage, the SE-CURE_HASH must have been programmed in eFuse and valid application code must have been programmed in the Main Flash Default Value: 0
1	SECURE_WITH_DEBUG	This is same as SECURE life cycle stage, except the device allows for debugging. Prior to transitioning to this stage, the SECURE_HASH must have been programmed in eFuse and valid application code must have been programmed in the Main Flash. Default Value: 0
0	NORMAL	This is the life cycle stage of a device after trimming and testing is complete in the factory. All configuration and trimming information is complete. Valid FLASH boot code has been programmed in the Supervisory Flash. Default Value: 0

13.1.6 EFUSE_DATA_CUSTOMER_DATA0

Customer data

Address: 0x402C0840

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CUSTOMER_USE [7:0]							

Bits	Name	Description
7 : 0	CUSTOMER_USE	Fuses left over are available for customer use. Default Value: 0

14 Profiler Registers

This section discusses the Profiler registers. It lists all the registers in mapping tables, in address order

14.1 Register Details

Register	Address	Description
PROFILE_CTL	0x402D0000	Profile control
PROFILE_STATUS	0x402D0004	Profile status
PROFILE_CMD	0x402D0010	Profile command
PROFILE_INTR	0x402D07C0	Profile interrupt
PROFILE_INTR_SET	0x402D07C4	Profile interrupt set
PROFILE_INTR_MASK	0x402D07C8	Profile interrupt mask
PROFILE_INTR_MASKED	0x402D07CC	Profile interrupt masked
PROFILE_CNT_STRUCT0_CTL	0x402D0800	Profile counter configuration
PROFILE_CNT_STRUCT0_CNT	0x402D0808	Profile counter value
PROFILE_CNT_STRUCT1_CTL	0x402D0810	Profile counter configuration. See PROFILE_CNT_STRUCT0_CTL for the details of bit fields.
PROFILE_CNT_STRUCT1_CNT	0x402D0818	Profile counter value. See PROFILE_CNT_STRUCT0_CNT for the details of bit fields.
PROFILE_CNT_STRUCT2_CTL	0x402D0820	Profile counter configuration. See PROFILE_CNT_STRUCT0_CTL for the details of bit fields.
PROFILE_CNT_STRUCT2_CNT	0x402D0828	Profile counter value. See PROFILE_CNT_STRUCT0_CNT for the details of bit fields.
PROFILE_CNT_STRUCT3_CTL	0x402D0830	Profile counter configuration. See PROFILE_CNT_STRUCT0_CTL for the details of bit fields.
PROFILE_CNT_STRUCT3_CNT	0x402D0838	Profile counter value. See PROFILE_CNT_STRUCT0_CNT for the details of bit fields.
PROFILE_CNT_STRUCT4_CTL	0x402D0840	Profile counter configuration. See PROFILE_CNT_STRUCT0_CTL for the details of bit fields.
PROFILE_CNT_STRUCT4_CNT	0x402D0848	Profile counter value. See PROFILE_CNT_STRUCT0_CNT for the details of bit fields.
PROFILE_CNT_STRUCT5_CTL	0x402D0850	Profile counter configuration. See PROFILE_CNT_STRUCT0_CTL for the details of bit fields.
PROFILE_CNT_STRUCT5_CNT	0x402D0858	Profile counter value. See PROFILE_CNT_STRUCT0_CNT for the details of bit fields.
PROFILE_CNT_STRUCT6_CTL	0x402D0860	Profile counter configuration. See PROFILE_CNT_STRUCT0_CTL for the details of bit fields.
PROFILE_CNT_STRUCT6_CNT	0x402D0868	Profile counter value. See PROFILE_CNT_STRUCT0_CNT for the details of bit fields.
PROFILE_CNT_STRUCT7_CTL	0x402D0870	Profile counter configuration. See PROFILE_CNT_STRUCT0_CTL for the details of bit fields.
PROFILE_CNT_STRUCT7_CNT	0x402D0878	Profile counter value. See PROFILE_CNT_STRUCT0_CNT for the details of bit fields.

14.1.1 PROFILE_CTL

Profile control

Address: 0x402D0000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							WIN_MODE

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	ENABLED	None [30:24]						

Bits	Name	Description
31	ENABLED	Enables the profiling block: '0': Disabled. '1': Enabled. Default Value: 0
0	WIN_MODE	Specifies the profiling time window mode: '0': Start / stop mode. The profiling time window is started when a rising edge of the start trigger signal occurs and stopped when a rising edge of the stop trigger signal occurs. In case both rising edges (of start and stop trigger signals) occur in the same cycle, the profiling time window is stopped. '1': Enable mode. The profiling time window is active as long as the start 'trigger' signal is active. The stop trigger signal has no effect. Default Value: 0

14.1.2 PROFILE_STATUS

Profile status

Address: 0x402D0004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							W
Name	None [7:1]							WIN_AC-TIVE

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	WIN_ACTIVE	Indicates if the profiling time window is active. '0': Not active. '1': Active. Default Value: 0

14.1.3 PROFILE_CMD

Profile command

Address: 0x402D0010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1S	RW1S
HW Access	None						RW1C	RW1C
Name	None [7:2]						STOP_TR	START_TR

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1S
HW Access	None							RW1C
Name	None [15:9]							CL-R_ALL_CNT

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	CLR_ALL_CNT	Counter clear. When written with '1', all profiling counter registers are cleared to 0x00. Default Value: 0
1	STOP_TR	Software stop trigger for the profiling time window. When written with '1', the profiling time window is stopped. Can only be used in start / stop mode (PROFILE_WIN_MODE=0). Has no effect in enable mode (PROFILE_WIN_MODE=1). Default Value: 0
0	START_TR	Software start trigger for the profiling time window. When written with '1', the profiling time window is started. Can only be used in start / stop mode (PROFILE_WIN_MODE=0). Has no effect in enable mode (PROFILE_WIN_MODE=1). Default Value: 0

14.1.4 PROFILE_INTR

Profile interrupt

Address: 0x402D07C0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C							
HW Access	RW1S							
Name	CNT_OVFLW [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	CNT_OVFLW	This interrupt cause field is activated (HW sets the field to '1') when an profiling counter overflow (from 0xFFFFFFFF to 0x00000000) is captured. There is one bit per profling counter. SW writes a '1' to a bit of this field to clear this bit to '0' (writing 0xFFFFFFFF clears all interrupt causes to '0'). Default Value: 0

14.1.5 PROFILE_INTR_SET

Profile interrupt set

Address: 0x402D07C4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S							
HW Access	A							
Name	CNT_OVFLW [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	CNT_OVFLW	SW writes a '1' to a bit of this field to set the corresponding bit in the INTR register. Default Value: 0

14.1.6 PROFILE_INTR_MASK

Profile interrupt mask

Address: 0x402D07C8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CNT_OVFLW [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	CNT_OVFLW	Mask bit for corresponding field in the INTR register. Default Value: 0

14.1.7 PROFILE_INTR_MASKED

Profile interrupt masked

Address: 0x402D07CC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	CNT_OVFLW [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	CNT_OVFLW	Logical and of corresponding INTR and INTR_MASK fields. Default Value: 0

14.1.8 PROFILE_CNT_STRUCT0_CTL

Profile counter configuration

Address: 0x402D0800

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None			RW
HW Access	None	R			None			R
Name	None	REF_CLK_SEL [6:4]			None [3:1]			CNT_DU-RATION

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None	RW						
HW Access	None	R						
Name	None	MON_SEL [22:16]						

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	ENABLED	None [30:24]						

Bits	Name	Description
31	ENABLED	Enables the profiling counter: '0': Disabled. '1': Enabled. Default Value: 0
22 : 16	MON_SEL	This field specifies the montior input signal to be observed by the profiling counter. The monitor signals are product specific, see product definition spreadsheet tab "Monitor" for details. Default Value: 0
6 : 4	REF_CLK_SEL	This field specifies the reference clock used for a counting time base when counting durations. Has no effect when CTL.CNT_DURATION=0. Default Value: 0 **0x0: CLK_TIMER :** Timer clock (divided or undivided high frequency clock, e.g. from IMO). Selection is done in SRSS register CLK_TIMER_CTL.TIMER_SEL. **0x1: CLK_IMO :** IMO - Internal Main Oscillator

14.1.8 PROFILE_CNT_STRUCT0_CTL (continued)

		0x2: CLK_ECO : ECO - External-Crystal Oscillator **0x3: CLK_LF :** Low frequency clock (ILO, WCO or ALTLF). Selection is done in SRSS register CLK_SELECT.LFCLK_SEL. **0x4: CLK_HF :** High frequuency clock ("clk_hfx"). **0x5: CLK_PERI :** Peripheral clock ("clk_peri"). **0x6: RESERVED_6 :** Reserved. Do not use. When using, the behavior of this profiling counter is undefined. **0x7: RESERVED_7 :** Reserved. Do not use. When using, the behavior of this profiling counter is undefined.
0	CNT_DURATION	This field specifies if events (edges) or a duration of the monitor signal is counted. '0': Events are monitored. An edge detection is done. All edges of the selected monitor signal are counted. '1': A duration is monitored. No edge detection is done. The monitored signal is taken as a (high active) level signal for enabling the profiling counter. Note: All monitor signals which only can represent events are edge encoded in hardware, therefore a selection of CTL.CNT_DURATION=1 will not produce meaningful results. Default Value: 0

14.1.9 PROFILE_CNT_STRUCT0_CNT

Profile counter value

Address: 0x402D0808

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	CNT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	CNT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	A							
Name	CNT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	A							
Name	CNT [31:24]							

Bits	Name	Description
31 : 0	CNT	This field shows / specifies the actual value of the profiling counter. It allows reading as well as writing the profiling counter. Default Value: 0

Section E: Peripheral Group 3

This section encompasses the following chapters:

15 High Speed IO Matrix (HSIOM) Registers

This section discusses the High-Speed I/O Matrix (HSIOM) registers. It lists all the registers in mapping tables, in address order.

15.1 Register Details

Register	Address	Description
HSIOM_PRT0_PORT_SEL0	0x40310000	Port selection 0
HSIOM_PRT0_PORT_SEL1	0x40310004	Port selection 1
HSIOM_PRT1_PORT_SEL0	0x40310010	Port selection 0. See HSIOM_PRT0_PORT_SEL0 for the details of bit fields.
HSIOM_PRT1_PORT_SEL1	0x40310014	Port selection 1. See HSIOM_PRT0_PORT_SEL1 for the details of bit fields.
HSIOM_PRT2_PORT_SEL0	0x40310020	Port selection 0. See HSIOM_PRT0_PORT_SEL0 for the details of bit fields.
HSIOM_PRT2_PORT_SEL1	0x40310024	Port selection 1
HSIOM_PRT3_PORT_SEL0	0x40310030	Port selection 0. See HSIOM_PRT0_PORT_SEL0 for the details of bit fields.
HSIOM_PRT3_PORT_SEL1	0x40310034	Port selection 1. See HSIOM_PRT0_PORT_SEL1 for the details of bit fields.
HSIOM_PRT4_PORT_SEL0	0x40310040	Port selection 0. See HSIOM_PRT0_PORT_SEL0 for the details of bit fields.
HSIOM_PRT5_PORT_SEL0	0x40310050	Port selection 0. See HSIOM_PRT0_PORT_SEL0 for the details of bit fields.
HSIOM_PRT5_PORT_SEL1	0x40310054	Port selection 1. See HSIOM_PRT2_PORT_SEL1 for the details of bit fields.
HSIOM_PRT6_PORT_SEL0	0x40310060	Port selection 0. See HSIOM_PRT0_PORT_SEL0 for the details of bit fields.
HSIOM_PRT6_PORT_SEL1	0x40310064	Port selection 1. See HSIOM_PRT2_PORT_SEL1 for the details of bit fields.
HSIOM_PRT7_PORT_SEL0	0x40310070	Port selection 0. See HSIOM_PRT0_PORT_SEL0 for the details of bit fields.
HSIOM_PRT7_PORT_SEL1	0x40310074	Port selection 1. See HSIOM_PRT2_PORT_SEL1 for the details of bit fields.
HSIOM_PRT8_PORT_SEL0	0x40310080	Port selection 0. See HSIOM_PRT0_PORT_SEL0 for the details of bit fields.
HSIOM_PRT8_PORT_SEL1	0x40310084	Port selection 1. See HSIOM_PRT2_PORT_SEL1 for the details of bit fields.
HSIOM_PRT9_PORT_SEL0	0x40310090	Port selection 0. See HSIOM_PRT0_PORT_SEL0 for the details of bit fields.
HSIOM_PRT9_PORT_SEL1	0x40310094	Port selection 1. See HSIOM_PRT2_PORT_SEL1 for the details of bit fields.
HSIOM_PRT10_PORT_SEL0	0x403100A0	Port selection 0. See HSIOM_PRT0_PORT_SEL0 for the details of bit fields.
HSIOM_PRT10_PORT_SEL1	0x403100A4	Port selection 1. See HSIOM_PRT2_PORT_SEL1 for the details of bit fields.
HSIOM_PRT11_PORT_SEL0	0x403100B0	Port selection 0. See HSIOM_PRT0_PORT_SEL0 for the details of bit fields.
HSIOM_PRT11_PORT_SEL1	0x403100B4	Port selection 1. See HSIOM_PRT2_PORT_SEL1 for the details of bit fields.
HSIOM_PRT12_PORT_SEL0	0x403100C0	Port selection 0. See HSIOM_PRT0_PORT_SEL0 for the details of bit fields.
HSIOM_PRT12_PORT_SEL1	0x403100C4	Port selection 1. See HSIOM_PRT2_PORT_SEL1 for the details of bit fields.
HSIOM_PRT13_PORT_SEL0	0x403100D0	Port selection 0. See HSIOM_PRT0_PORT_SEL0 for the details of bit fields.

Register	Address	Description
HSIOM_PRT13_PORT_SEL1	0x403100D4	Port selection 1. See HSIOM_PRT2_PORT_SEL1 for the details of bit fields.
HSIOM_PRT14_PORT_SEL0	0x403100E0	Port selection 0
HSIOM_AMUX_SPLIT_CTL0	0x40312000	AMUX splitter cell control
HSIOM_AMUX_SPLIT_CTL1	0x40312004	AMUX splitter cell control. See HSIOM_AMUX_SPLIT_CTL0 for the details of bit fields.
HSIOM_AMUX_SPLIT_CTL2	0x40312008	AMUX splitter cell control. See HSIOM_AMUX_SPLIT_CTL0 for the details of bit fields.
HSIOM_AMUX_SPLIT_CTL3	0x4031200C	AMUX splitter cell control. See HSIOM_AMUX_SPLIT_CTL0 for the details of bit fields.
HSIOM_AMUX_SPLIT_CTL4	0x40312010	AMUX splitter cell control. See HSIOM_AMUX_SPLIT_CTL0 for the details of bit fields.
HSIOM_AMUX_SPLIT_CTL5	0x40312014	AMUX splitter cell control. See HSIOM_AMUX_SPLIT_CTL0 for the details of bit fields.
HSIOM_AMUX_SPLIT_CTL6	0x40312018	AMUX splitter cell control. See HSIOM_AMUX_SPLIT_CTL0 for the details of bit fields.
HSIOM_AMUX_SPLIT_CTL7	0x4031201C	AMUX splitter cell control. See HSIOM_AMUX_SPLIT_CTL0 for the details of bit fields.
HSIOM_AMUX_SPLIT_CTL8	0x40312020	AMUX splitter cell control. See HSIOM_AMUX_SPLIT_CTL0 for the details of bit fields.

15.1.1 HSIOM_PRT0_PORT_SEL0

Port selection 0

Address: 0x40310000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			RW				
Name	None [7:5]			IO0_SEL [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW				
HW Access	None			RW				
Name	None [15:13]			IO1_SEL [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW				
HW Access	None			RW				
Name	None [23:21]			IO2_SEL [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	None			RW				
HW Access	None			RW				
Name	None [31:29]			IO3_SEL [28:24]				

Bits	Name	Description
28 : 24	IO3_SEL	Selects connection for IO pin 3 route. Default Value: 0
20 : 16	IO2_SEL	Selects connection for IO pin 2 route. Default Value: 0
12 : 8	IO1_SEL	Selects connection for IO pin 1 route. Default Value: 0
4 : 0	IO0_SEL	Selects connection for IO pin 0 route. Default Value: 0 **0x0: GPIO :** GPIO controls "out" **0x1: GPIO_DSI :** GPIO controls "out", DSI controls "output enable" **0x2: DSI_DSI :** DSI controls "out" and "output enable" **0x3: DSI_GPIO :** DSI controls "out", GPIO controls "output enable"

15.1.1 HSIOM_PRT0_PORT_SEL0 (continued)

0x4: AMUXA :
Analog mux bus A

0x5: AMUXB :
Analog mux bus B

0x6: AMUXA_DSI :
Analog mux bus A, DSI control

0x7: AMUXB_DSI :
Analog mux bus B, DSI control

0x8: ACT_0 :
Active functionality 0

0x9: ACT_1 :
Active functionality 1

0xa: ACT_2 :
Active functionality 2

0xb: ACT_3 :
Active functionality 3

0xc: DS_0 :
DeepSleep functionality 0

0xd: DS_1 :
DeepSleep functionality 1

0xe: DS_2 :
DeepSleep functionality 2

0xf: DS_3 :
DeepSleep functionality 3

0x10: ACT_4 :
Active functionality 4

0x11: ACT_5 :
Active functionality 5

0x12: ACT_6 :
Active functionality 6

0x13: ACT_7 :
Active functionality 7

0x14: ACT_8 :
Active functionality 8

0x15: ACT_9 :
Active functionality 9

0x16: ACT_10 :
Active functionality 10

0x17: ACT_11 :
Active functionality 11

0x18: ACT_12 :
Active functionality 12

0x19: ACT_13 :
Active functionality 13

15.1.1 HSIOM_PRT0_PORT_SEL0 (continued)

0x1a: ACT_14 :
Active functionality 14

0x1b: ACT_15 :
Active functionality 15

0x1c: DS_4 :
DeepSleep functionality 4

0x1d: DS_5 :
DeepSleep functionality 5

0x1e: DS_6 :
DeepSleep functionality 6

0x1f: DS_7 :
DeepSleep functionality 7

15.1.2 HSIOM_PRT0_PORT_SEL1

Port selection 1

Address: 0x40310004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			RW				
Name	None [7:5]			IO4_SEL [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW				
HW Access	None			RW				
Name	None [15:13]			IO5_SEL [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
12 : 8	IO5_SEL	Selects connection for IO pin 5 route. Default Value: 0
4 : 0	IO4_SEL	Selects connection for IO pin 4 route. See PORT_SEL0 for connection details. Default Value: 0

15.1.3 HSIOM_PRT2_PORT_SEL1

Port selection 1

Address: 0x40310024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			RW				
Name	None [7:5]			IO4_SEL [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW				
HW Access	None			RW				
Name	None [15:13]			IO5_SEL [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW				
HW Access	None			RW				
Name	None [23:21]			IO6_SEL [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	None			RW				
HW Access	None			RW				
Name	None [31:29]			IO7_SEL [28:24]				

Bits	Name	Description
28 : 24	IO7_SEL	Selects connection for IO pin 7 route. Default Value: 0
20 : 16	IO6_SEL	Selects connection for IO pin 6 route. Default Value: 0
12 : 8	IO5_SEL	Selects connection for IO pin 5 route. Default Value: 0
4 : 0	IO4_SEL	Selects connection for IO pin 4 route. See PORT_SEL0 for connection details. Default Value: 0

15.1.4 HSIOM_PRT14_PORT_SEL0

Port selection 0

Address: 0x403100E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			RW				
Name	None [7:5]			IO0_SEL [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW				
HW Access	None			RW				
Name	None [15:13]			IO1_SEL [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
12 : 8	IO1_SEL	Selects connection for IO pin 1 route. Default Value: 0
4 : 0	IO0_SEL	Selects connection for IO pin 0 route. Default Value: 0 **0x0: GPIO :** GPIO controls "out" **0x1: GPIO_DSI :** GPIO controls "out", DSI controls "output enable" **0x2: DSI_DSI :** DSI controls "out" and "output enable" **0x3: DSI_GPIO :** DSI controls "out", GPIO controls "output enable" **0x4: AMUXA :** Analog mux bus A **0x5: AMUXB :** Analog mux bus B

0x6: AMUXA_DSI :
Analog mux bus A, DSI control

0x7: AMUXB_DSI :
Analog mux bus B, DSI control

0x8: ACT_0 :
Active functionality 0

0x9: ACT_1 :
Active functionality 1

0xa: ACT_2 :
Active functionality 2

0xb: ACT_3 :
Active functionality 3

0xc: DS_0 :
DeepSleep functionality 0

0xd: DS_1 :
DeepSleep functionality 1

0xe: DS_2 :
DeepSleep functionality 2

0xf: DS_3 :
DeepSleep functionality 3

0x10: ACT_4 :
Active functionality 4

0x11: ACT_5 :
Active functionality 5

0x12: ACT_6 :
Active functionality 6

0x13: ACT_7 :
Active functionality 7

0x14: ACT_8 :
Active functionality 8

0x15: ACT_9 :
Active functionality 9

0x16: ACT_10 :
Active functionality 10

0x17: ACT_11 :
Active functionality 11

0x18: ACT_12 :
Active functionality 12

0x19: ACT_13 :
Active functionality 13

0x1a: ACT_14 :
Active functionality 14

0x1b: ACT_15 :
Active functionality 15

0x1c: DS_4 :
DeepSleep functionality 4

15.1.4 HSIOM_PRT14_PORT_SEL0 (continued)

0x1d: DS_5 :
DeepSleep functionality 5

0x1e: DS_6 :
DeepSleep functionality 6

0x1f: DS_7 :
DeepSleep functionality 7

15.1.5 HSIOM_AMUX_SPLIT_CTL0

AMUX splitter cell control

Address: 0x40312000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	RW	RW	None	RW	RW	RW
HW Access	None	R	R	R	None	R	R	R
Name	None	SWITCH_B-B_S0	SWITCH_B-B_SR	SWITCH_B-B_SL	None	SWITCH_AA_S0	SWITCH_AA_SR	SWITCH_AA_SL

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
6	SWITCH_BB_S0	T-switch control for AMUXBUSB vssa/ground switch. Default Value: 0
5	SWITCH_BB_SR	T-switch control for Right AMUXBUSB switch. Default Value: 0
4	SWITCH_BB_SL	T-switch control for Left AMUXBUSB switch. Default Value: 0
2	SWITCH_AA_S0	T-switch control for AMUXBUSA vssa/ground switch: '0': switch open. '1': switch closed. Default Value: 0
1	SWITCH_AA_SR	T-switch control for Right AMUXBUSA switch: '0': switch open. '1': switch closed. Default Value: 0

15.1.5 HSIOM_AMUX_SPLIT_CTL0 (continued)

0	SWITCH_AA_SL	T-switch control for Left AMUXBUSA switch: '0': switch open. '1': switch closed. Default Value: 0

16 General Purpose I/O (GPIO) Registers

This section discusses the General Purpose I/O (GPIO) registers. It lists all the registers in mapping tables, in address order.

16.1 Register Details

Register	Address	Description
GPIO_PRT0_OUT	0x40320000	Port output data register
GPIO_PRT0_OUT_CLR	0x40320004	Port output data clear register
GPIO_PRT0_OUT_SET	0x40320008	Port output data set register
GPIO_PRT0_OUT_INV	0x4032000C	Port output data invert register
GPIO_PRT0_IN	0x40320010	Port input state register
GPIO_PRT0_INTR	0x40320014	Port interrupt status register
GPIO_PRT0_INTR_MASK	0x40320018	Port interrupt mask register
GPIO_PRT0_INTR_MASKED	0x4032001C	Port interrupt masked status register
GPIO_PRT0_INTR_SET	0x40320020	Port interrupt set register
GPIO_PRT0_INTR_CFG	0x40320024	Port interrupt configuration register
GPIO_PRT0_CFG	0x40320028	Port configuration register
GPIO_PRT0_CFG_IN	0x4032002C	Port input buffer configuration register
GPIO_PRT0_CFG_OUT	0x40320030	Port output buffer configuration register
GPIO_PRT1_OUT	0x40320080	Port output data register. See GPIO_PRT0_OUT for the details of bit fields.
GPIO_PRT1_OUT_CLR	0x40320084	Port output data clear register. See GPIO_PRT0_OUT_CLR for the details of bit fields.
GPIO_PRT1_OUT_SET	0x40320088	Port output data set register. See GPIO_PRT0_OUT_SET for the details of bit fields.
GPIO_PRT1_OUT_INV	0x4032008C	Port output data invert register. See GPIO_PRT0_OUT_INV for the details of bit fields.
GPIO_PRT1_IN	0x40320090	Port input state register. See GPIO_PRT0_IN for the details of bit fields.
GPIO_PRT1_INTR	0x40320094	Port interrupt status register. See GPIO_PRT0_INTR for the details of bit fields.
GPIO_PRT1_INTR_MASK	0x40320098	Port interrupt mask register. See GPIO_PRT0_INTR_MASK for the details of bit fields.
GPIO_PRT1_INTR_MASKED	0x4032009C	Port interrupt masked status register. See GPIO_PRT0_INTR_MASKED for the details of bit fields.
GPIO_PRT1_INTR_SET	0x403200A0	Port interrupt set register. See GPIO_PRT0_INTR_SET for the details of bit fields.
GPIO_PRT1_INTR_CFG	0x403200A4	Port interrupt configuration register. See GPIO_PRT0_INTR_CFG for the details of bit fields.
GPIO_PRT1_CFG	0x403200A8	Port configuration register. See GPIO_PRT0_CFG for the details of bit fields.
GPIO_PRT1_CFG_IN	0x403200AC	Port input buffer configuration register. See GPIO_PRT0_CFG_IN for the details of bit fields.
GPIO_PRT1_CFG_OUT	0x403200B0	Port output buffer configuration register. See GPIO_PRT0_CFG_OUT for the details of bit fields.
GPIO_PRT2_OUT	0x40320100	Port output data register

Register	Address	Description
GPIO_PRT2_OUT_CLR	0x40320104	Port output data clear register. See GPIO_PRT0_OUT_CLR for the details of bit fields.
GPIO_PRT2_OUT_SET	0x40320108	Port output data set register. See GPIO_PRT0_OUT_SET for the details of bit fields.
GPIO_PRT2_OUT_INV	0x4032010C	Port output data invert register. See GPIO_PRT0_OUT_INV for the details of bit fields.
GPIO_PRT2_IN	0x40320110	Port input state register
GPIO_PRT2_INTR	0x40320114	Port interrupt status register
GPIO_PRT2_INTR_MASK	0x40320118	Port interrupt mask register
GPIO_PRT2_INTR_MASKEDT	0x4032011C	Port interrupt masked status register
GPIO_PRT2_INTR_SET	0x40320120	Port interrupt set register
GPIO_PRT2_INTR_CFG	0x40320124	Port interrupt configuration register
GPIO_PRT2_CFG	0x40320128	Port configuration register
GPIO_PRT2_CFG_IN	0x4032012C	Port input buffer configuration register
GPIO_PRT2_CFG_OUT	0x40320130	Port output buffer configuration register
GPIO_PRT3_OUT	0x40320180	Port output data register. See GPIO_PRT0_OUT for the details of bit fields.
GPIO_PRT3_OUT_CLR	0x40320184	Port output data clear register. See GPIO_PRT0_OUT_CLR for the details of bit fields.
GPIO_PRT3_OUT_SET	0x40320188	Port output data set register. See GPIO_PRT0_OUT_SET for the details of bit fields.
GPIO_PRT3_OUT_INV	0x4032018C	Port output data invert register. See GPIO_PRT0_OUT_INV for the details of bit fields.
GPIO_PRT3_IN	0x40320190	Port input state register. See GPIO_PRT0_IN for the details of bit fields.
GPIO_PRT3_INTR	0x40320194	Port interrupt status register. See GPIO_PRT0_INTR for the details of bit fields.
GPIO_PRT3_INTR_MASK	0x40320198	Port interrupt mask register. See GPIO_PRT0_INTR_MASK for the details of bit fields.
GPIO_PRT3_INTR_MASKED	0x4032019C	Port interrupt masked status register. See GPIO_PRT0_INTR_MASKED for the details of bit fields.
GPIO_PRT3_INTR_SET	0x403201A0	Port interrupt set register. See GPIO_PRT0_INTR_SET for the details of bit fields.
GPIO_PRT3_INTR_CFG	0x403201A4	Port interrupt configuration register. See GPIO_PRT0_INTR_CFG for the details of bit fields.
GPIO_PRT3_CFG	0x403201A8	Port configuration register. See GPIO_PRT0_CFG for the details of bit fields.
GPIO_PRT3_CFG_IN	0x403201AC	Port input buffer configuration register. See GPIO_PRT0_CFG_IN for the details of bit fields.
GPIO_PRT3_CFG_OUT	0x403201B0	Port output buffer configuration register. See GPIO_PRT0_CFG_OUT for the details of bit fields.
GPIO_PRT4_OUT	0x40320200	Port output data register
GPIO_PRT4_OUT_CLR	0x40320204	Port output data clear register. See GPIO_PRT0_OUT_CLR for the details of bit fields.
GPIO_PRT4_OUT_SET	0x40320208	Port output data set register. See GPIO_PRT0_OUT_SET for the details of bit fields.
GPIO_PRT4_OUT_INV	0x4032020C	Port output data invert register. See GPIO_PRT0_OUT_INV for the details of bit fields.
GPIO_PRT4_IN	0x40320210	Port input state register
GPIO_PRT4_INTR	0x40320214	Port interrupt status register
GPIO_PRT4_INTR_MASK	0x40320218	Port interrupt mask register
GPIO_PRT4_INTR_MASKED	0x4032021C	Port interrupt masked status register
GPIO_PRT4_INTR_SET	0x40320220	Port interrupt set register
GPIO_PRT4_INTR_CFG	0x40320224	Port interrupt configuration register
GPIO_PRT4_CFG	0x40320228	Port configuration register
GPIO_PRT4_CFG_IN	0x4032022C	Port input buffer configuration register
GPIO_PRT4_CFG_OUT	0x40320230	Port output buffer configuration register
GPIO_PRT5_OUT	0x40320280	Port output data register. See GPIO_PRT2_OUT for the details of bit fields.
GPIO_PRT5_OUT_CLR	0x40320284	Port output data clear register. See GPIO_PRT0_OUT_CLR for the details of bit fields.
GPIO_PRT5_OUT_SET	0x40320288	Port output data set register. See GPIO_PRT0_OUT_SET for the details of bit fields.
GPIO_PRT5_OUT_INV	0x4032028C	Port output data invert register. See GPIO_PRT0_OUT_INV for the details of bit fields.

Register	Address	Description
GPIO_PRT5_IN	0x40320290	Port input state register. See GPIO_PRT2_IN for the details of bit fields.
GPIO_PRT5_INTR	0x40320294	Port interrupt status register. See GPIO_PRT2_INTR for the details of bit fields.
GPIO_PRT5_INTR_MASK	0x40320298	Port interrupt mask register. See GPIO_PRT2_INTR_MASK for the details of bit fields.
GPIO_PRT5_INTR_MASKED	0x4032029C	Port interrupt masked status register. See GPIO_PRT2_INTR_MASKED for the details of bit fields.
GPIO_PRT5_INTR_SET	0x403202A0	Port interrupt set register. See GPIO_PRT2_INTR_SET for the details of bit fields.
GPIO_PRT5_INTR_CFG	0x403202A4	Port interrupt configuration register. See GPIO_PRT2_INTR_CFG for the details of bit fields.
GPIO_PRT5_CFG	0x403202A8	Port configuration register. See GPIO_PRT2_CFG for the details of bit fields.
GPIO_PRT5_CFG_IN	0x403202AC	Port input buffer configuration register. See GPIO_PRT2_CFG_IN for the details of bit fields.
GPIO_PRT5_CFG_OUT	0x403202B0	Port output buffer configuration register. See GPIO_PRT2_CFG_OUT for the details of bit fields.
GPIO_PRT6_OUT	0x40320300	Port output data register. See GPIO_PRT2_OUT for the details of bit fields.
GPIO_PRT6_OUT_CLR	0x40320304	Port output data clear register. See GPIO_PRT0_OUT_CLR for the details of bit fields.
GPIO_PRT6_OUT_SET	0x40320308	Port output data set register. See GPIO_PRT0_OUT_SET for the details of bit fields.
GPIO_PRT6_OUT_INV	0x4032030C	Port output data invert register. See GPIO_PRT0_OUT_INV for the details of bit fields.
GPIO_PRT6_IN	0x40320310	Port input state register. See GPIO_PRT2_IN for the details of bit fields.
GPIO_PRT6_INTR	0x40320314	Port interrupt status register. See GPIO_PRT2_INTR for the details of bit fields.
GPIO_PRT6_INTR_MASK	0x40320318	Port interrupt mask register. See GPIO_PRT2_INTR_MASK for the details of bit fields.
GPIO_PRT6_INTR_MASKED	0x4032031C	Port interrupt masked status register. See GPIO_PRT2_INTR_MASKED for the details of bit fields.
GPIO_PRT6_INTR_SET	0x40320320	Port interrupt set register. See GPIO_PRT2_INTR_SET for the details of bit fields.
GPIO_PRT6_INTR_CFG	0x40320324	Port interrupt configuration register. See GPIO_PRT2_INTR_CFG for the details of bit fields.
GPIO_PRT6_CFG	0x40320328	Port configuration register. See GPIO_PRT2_CFG for the details of bit fields.
GPIO_PRT6_CFG_IN	0x4032032C	Port input buffer configuration register. See GPIO_PRT2_CFG_IN for the details of bit fields.
GPIO_PRT6_CFG_OUT	0x40320330	Port output buffer configuration register. See GPIO_PRT2_CFG_OUT for the details of bit fields.
GPIO_PRT7_OUT	0x40320380	Port output data register. See GPIO_PRT2_OUT for the details of bit fields.
GPIO_PRT7_OUT_CLR	0x40320384	Port output data clear register. See GPIO_PRT0_OUT_CLR for the details of bit fields.
GPIO_PRT7_OUT_SET	0x40320388	Port output data set register. See GPIO_PRT0_OUT_SET for the details of bit fields.
GPIO_PRT7_OUT_INV	0x4032038C	Port output data invert register. See GPIO_PRT0_OUT_INV for the details of bit fields.
GPIO_PRT7_IN	0x40320390	Port input state register. See GPIO_PRT2_IN for the details of bit fields.
GPIO_PRT7_INTR	0x40320394	Port interrupt status register. See GPIO_PRT2_INTR for the details of bit fields.
GPIO_PRT7_INTR_MASK	0x40320398	Port interrupt mask register. See GPIO_PRT2_INTR_MASK for the details of bit fields.
GPIO_PRT7_INTR_MASKED	0x4032039C	Port interrupt masked status register. See GPIO_PRT2_INTR_MASKED for the details of bit fields.
GPIO_PRT7_INTR_SET	0x403203A0	Port interrupt set register. See GPIO_PRT2_INTR_SET for the details of bit fields.
GPIO_PRT7_INTR_CFG	0x403203A4	Port interrupt configuration register. See GPIO_PRT2_INTR_CFG for the details of bit fields.
GPIO_PRT7_CFG	0x403203A8	Port configuration register. See GPIO_PRT2_CFG for the details of bit fields.
GPIO_PRT7_CFG_IN	0x403203AC	Port input buffer configuration register. See GPIO_PRT2_CFG_IN for the details of bit fields.
GPIO_PRT7_CFG_OUT	0x403203B0	Port output buffer configuration register. See GPIO_PRT2_CFG_OUT for the details of bit fields.
GPIO_PRT8_OUT	0x40320400	Port output data register. See GPIO_PRT2_OUT for the details of bit fields.
GPIO_PRT8_OUT_CLR	0x40320404	Port output data clear register. See GPIO_PRT0_OUT_CLR for the details of bit fields.
GPIO_PRT8_OUT_SET	0x40320408	Port output data set register. See GPIO_PRT0_OUT_SET for the details of bit fields.
GPIO_PRT8_OUT_INV	0x4032040C	Port output data invert register. See GPIO_PRT0_OUT_INV for the details of bit fields.
GPIO_PRT8_IN	0x40320410	Port input state register. See GPIO_PRT2_IN for the details of bit fields.
GPIO_PRT8_INTR	0x40320414	Port interrupt status register. See GPIO_PRT2_INTR for the details of bit fields.
GPIO_PRT8_INTR_MASK	0x40320418	Port interrupt mask register. See GPIO_PRT2_INTR_MASK for the details of bit fields.

Register	Address	Description
GPIO_PRT8_INTR_MASKED	0x4032041C	Port interrupt masked status register. See GPIO_PRT2_INTR_MASKED for the details of bit fields.
GPIO_PRT8_INTR_SET	0x40320420	Port interrupt set register. See GPIO_PRT2_INTR_SET for the details of bit fields.
GPIO_PRT8_INTR_CFG	0x40320424	Port interrupt configuration register. See GPIO_PRT2_INTR_CFG for the details of bit fields.
GPIO_PRT8_CFG	0x40320428	Port configuration register. See GPIO_PRT2_CFG for the details of bit fields.
GPIO_PRT8_CFG_IN	0x4032042C	Port input buffer configuration register. See GPIO_PRT2_CFG_IN for the details of bit fields.
GPIO_PRT8_CFG_OUT	0x40320430	Port output buffer configuration register. See GPIO_PRT2_CFG_OUT for the details of bit fields.
GPIO_PRT9_OUT	0x40320480	Port output data register. See GPIO_PRT2_OUT for the details of bit fields.
GPIO_PRT9_OUT_CLR	0x40320484	Port output data clear register. See GPIO_PRT0_OUT_CLR for the details of bit fields.
GPIO_PRT9_OUT_SET	0x40320488	Port output data set register. See GPIO_PRT0_OUT_SET for the details of bit fields.
GPIO_PRT9_OUT_INV	0x4032048C	Port output data invert register. See GPIO_PRT0_OUT_INV for the details of bit fields.
GPIO_PRT9_IN	0x40320490	Port input state register. See GPIO_PRT2_IN for the details of bit fields.
GPIO_PRT9_INTR	0x40320494	Port interrupt status register. See GPIO_PRT2_INTR for the details of bit fields.
GPIO_PRT9_INTR_MASK	0x40320498	Port interrupt mask register. See GPIO_PRT2_INTR_MASK for the details of bit fields.
GPIO_PRT9_INTR_MASKED	0x4032049C	Port interrupt masked status register. See GPIO_PRT2_INTR_MASKED for the details of bit fields.
GPIO_PRT9_INTR_SET	0x403204A0	Port interrupt set register. See GPIO_PRT2_INTR_SET for the details of bit fields.
GPIO_PRT9_INTR_CFG	0x403204A4	Port interrupt configuration register. See GPIO_PRT2_INTR_CFG for the details of bit fields.
GPIO_PRT9_CFG	0x403204A8	Port configuration register. See GPIO_PRT2_CFG for the details of bit fields.
GPIO_PRT9_CFG_IN	0x403204AC	Port input buffer configuration register. See GPIO_PRT2_CFG_IN for the details of bit fields.
GPIO_PRT9_CFG_OUT	0x403204B0	Port output buffer configuration register. See GPIO_PRT2_CFG_OUT for the details of bit fields.
GPIO_PRT10_OUT	0x40320500	Port output data register. See GPIO_PRT2_OUT for the details of bit fields.
GPIO_PRT10_OUT_CLR	0x40320504	Port output data clear register. See GPIO_PRT0_OUT_CLR for the details of bit fields.
GPIO_PRT10_OUT_SET	0x40320508	Port output data set register. See GPIO_PRT0_OUT_SET for the details of bit fields.
GPIO_PRT10_OUT_INV	0x4032050C	Port output data invert register. See GPIO_PRT0_OUT_INV for the details of bit fields.
GPIO_PRT10_IN	0x40320510	Port input state register. See GPIO_PRT2_IN for the details of bit fields.
GPIO_PRT10_INTR	0x40320514	Port interrupt status register. See GPIO_PRT2_INTR for the details of bit fields.
GPIO_PRT10_INTR_MASK	0x40320518	Port interrupt mask register. See GPIO_PRT2_INTR_MASK for the details of bit fields.
GPIO_PRT10_INTR_MASKED	0x4032051C	Port interrupt masked status register. See GPIO_PRT2_INTR_MASKED for the details of bit fields.
GPIO_PRT10_INTR_SET	0x40320520	Port interrupt set register. See GPIO_PRT2_INTR_SET for the details of bit fields.
GPIO_PRT10_INTR_CFG	0x40320524	Port interrupt configuration register. See GPIO_PRT2_INTR_CFG for the details of bit fields.
GPIO_PRT10_CFG	0x40320528	Port configuration register. See GPIO_PRT2_CFG for the details of bit fields.
GPIO_PRT10_CFG_IN	0x4032052C	Port input buffer configuration register. See GPIO_PRT2_CFG_IN for the details of bit fields.
GPIO_PRT10_CFG_OUT	0x40320530	Port output buffer configuration register. See GPIO_PRT2_CFG_OUT for the details of bit fields.
GPIO_PRT11_OUT	0x40320580	Port output data register. See GPIO_PRT2_OUT for the details of bit fields.
GPIO_PRT11_OUT_CLR	0x40320584	Port output data clear register. See GPIO_PRT0_OUT_CLR for the details of bit fields.
GPIO_PRT11_OUT_SET	0x40320588	Port output data set register. See GPIO_PRT0_OUT_SET for the details of bit fields.
GPIO_PRT11_OUT_INV	0x4032058C	Port output data invert register. See GPIO_PRT0_OUT_INV for the details of bit fields.
GPIO_PRT11_IN	0x40320590	Port input state register. See GPIO_PRT2_IN for the details of bit fields.
GPIO_PRT11_INTR	0x40320594	Port interrupt status register. See GPIO_PRT2_INTR for the details of bit fields.
GPIO_PRT11_INTR_MASK	0x40320598	Port interrupt mask register. See GPIO_PRT2_INTR_MASK for the details of bit fields.
GPIO_PRT11_INTR_MASKED	0x4032059C	Port interrupt masked status register. See GPIO_PRT2_INTR_MASKED for the details of bit fields.
GPIO_PRT11_INTR_SET	0x403205A0	Port interrupt set register. See GPIO_PRT2_INTR_SET for the details of bit fields.
GPIO_PRT11_INTR_CFG	0x403205A4	Port interrupt configuration register. See GPIO_PRT2_INTR_CFG for the details of bit fields.

Register	Address	Description
GPIO_PRT11_CFG	0x403205A8	Port configuration register. See GPIO_PRT2_CFG for the details of bit fields.
GPIO_PRT11_CFG_IN	0x403205AC	Port input buffer configuration register. See GPIO_PRT2_CFG_IN for the details of bit fields.
GPIO_PRT11_CFG_OUT	0x403205B0	Port output buffer configuration register. See GPIO_PRT2_CFG_OUT for the details of bit fields.
GPIO_PRT12_OUT	0x40320600	Port output data register. See GPIO_PRT2_OUT for the details of bit fields.
GPIO_PRT12_OUT_CLR	0x40320604	Port output data clear register. See GPIO_PRT0_OUT_CLR for the details of bit fields.
GPIO_PRT12_OUT_SET	0x40320608	Port output data set register. See GPIO_PRT0_OUT_SET for the details of bit fields.
GPIO_PRT12_OUT_INV	0x4032060C	Port output data invert register. See GPIO_PRT0_OUT_INV for the details of bit fields.
GPIO_PRT12_IN	0x40320610	Port input state register. See GPIO_PRT2_IN for the details of bit fields.
GPIO_PRT12_INTR	0x40320614	Port interrupt status register. See GPIO_PRT2_INTR for the details of bit fields.
GPIO_PRT12_INTR_MASK	0x40320618	Port interrupt mask register. See GPIO_PRT2_INTR_MASK for the details of bit fields.
GPIO_PRT12_INTR_MASKED	0x4032061C	Port interrupt masked status register. See GPIO_PRT2_INTR_MASKED for the details of bit fields.
GPIO_PRT12_INTR_SET	0x40320620	Port interrupt set register. See GPIO_PRT2_INTR_SET for the details of bit fields.
GPIO_PRT12_INTR_CFG	0x40320624	Port interrupt configuration register. See GPIO_PRT2_INTR_CFG for the details of bit fields.
GPIO_PRT12_CFG	0x40320628	Port configuration register. See GPIO_PRT2_CFG for the details of bit fields.
GPIO_PRT12_CFG_IN	0x4032062C	Port input buffer configuration register. See GPIO_PRT2_CFG_IN for the details of bit fields.
GPIO_PRT12_CFG_OUT	0x40320630	Port output buffer configuration register. See GPIO_PRT2_CFG_OUT for the details of bit fields.
GPIO_PRT13_OUT	0x40320680	Port output data register. See GPIO_PRT2_OUT for the details of bit fields.
GPIO_PRT13_OUT_CLR	0x40320684	Port output data clear register. See GPIO_PRT0_OUT_CLR for the details of bit fields.
GPIO_PRT13_OUT_SET	0x40320688	Port output data set register. See GPIO_PRT0_OUT_SET for the details of bit fields.
GPIO_PRT13_OUT_INV	0x4032068C	Port output data invert register. See GPIO_PRT0_OUT_INV for the details of bit fields.
GPIO_PRT13_IN	0x40320690	Port input state register. See GPIO_PRT2_IN for the details of bit fields.
GPIO_PRT13_INTR	0x40320694	Port interrupt status register. See GPIO_PRT2_INTR for the details of bit fields.
GPIO_PRT13_INTR_MASK	0x40320698	Port interrupt mask register. See GPIO_PRT2_INTR_MASK for the details of bit fields.
GPIO_PRT13_INTR_MASKED	0x4032069C	Port interrupt masked status register. See GPIO_PRT2_INTR_MASKED for the details of bit fields.
GPIO_PRT13_INTR_SET	0x403206A0	Port interrupt set register. See GPIO_PRT2_INTR_SET for the details of bit fields.
GPIO_PRT13_INTR_CFG	0x403206A4	Port interrupt configuration register. See GPIO_PRT2_INTR_CFG for the details of bit fields.
GPIO_PRT13_CFG	0x403206A8	Port configuration register. See GPIO_PRT2_CFG for the details of bit fields.
GPIO_PRT13_CFG_IN	0x403206AC	Port input buffer configuration register. See GPIO_PRT2_CFG_IN for the details of bit fields.
GPIO_PRT13_CFG_OUT	0x403206B0	Port output buffer configuration register. See GPIO_PRT2_CFG_OUT for the details of bit fields.
GPIO_PRT14_OUT	0x40320700	Port output data register
GPIO_PRT14_OUT_CLR	0x40320704	Port output data clear register. See GPIO_PRT0_OUT_CLR for the details of bit fields.
GPIO_PRT14_OUT_SET	0x40320708	Port output data set register. See GPIO_PRT0_OUT_SET for the details of bit fields.
GPIO_PRT14_OUT_INV	0x4032070C	Port output data invert register. See GPIO_PRT0_OUT_INV for the details of bit fields.
GPIO_PRT14_IN	0x40320710	Port input state register
GPIO_PRT14_INTR	0x40320714	Port interrupt status register
GPIO_PRT14_INTR_MASK	0x40320718	Port interrupt mask register
GPIO_PRT14_INTR_MASKED	0x4032071C	Port interrupt masked status register
GPIO_PRT14_INTR_SET	0x40320720	Port interrupt set register
GPIO_PRT14_INTR_CFG	0x40320724	Port interrupt configuration register
GPIO_PRT14_CFG	0x40320728	Port configuration register
GPIO_INTR_CAUSE0	0x40324000	Interrupt port cause register 0
GPIO_VDD_ACTIVE	0x40324010	Extern power supply detection register

Register	Address	Description
GPIO_VDD_INTR	0x40324014	Supply detection interrupt register
GPIO_VDD_INTR_MASK	0x40324018	Supply detection interrupt mask register
GPIO_VDD_INTR_MASKED	0x4032401C	Supply detection interrupt masked register
.GPIO_VDD_INTR_SET	0x40324020	Supply detection interrupt set register

16.1.1 GPIO_PRT0_OUT

Port output data register

Address: 0x40320000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		RW	RW	RW	RW	RW	RW
Name	None [7:6]		OUT5	OUT4	OUT3	OUT2	OUT1	OUT0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	OUT5	IO output data for pin 5 Default Value: 0
4	OUT4	IO output data for pin 4 Default Value: 0
3	OUT3	IO output data for pin 3 Default Value: 0
2	OUT2	IO output data for pin 2 Default Value: 0
1	OUT1	IO output data for pin 1 Default Value: 0
0	OUT0	IO output data for pin 0 '0': Output state set to '0' '1': Output state set to '1' Default Value: 0

16.1.2 GPIO_PRT0_OUT_CLR

Port output data clear register

Address: 0x40320004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	A	A	A	A	A	A	A	A
Name	OUT7	OUT6	OUT5	OUT4	OUT3	OUT2	OUT1	OUT0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	OUT7	IO clear output for pin 7 Default Value: 0
6	OUT6	IO clear output for pin 6 Default Value: 0
5	OUT5	IO clear output for pin 5 Default Value: 0
4	OUT4	IO clear output for pin 4 Default Value: 0
3	OUT3	IO clear output for pin 3 Default Value: 0
2	OUT2	IO clear output for pin 2 Default Value: 0
1	OUT1	IO clear output for pin 1 Default Value: 0

16.1.2 GPIO_PRT0_OUT_CLR (continued)

0	OUT0	IO clear output for pin 0: '0': Output state not affected. '1': Output state set to '0'. Default Value: 0

16.1.3 GPIO_PRT0_OUT_SET

Port output data set register

Address: 0x40320008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	A	A	A	A	A	A	A	A
Name	OUT7	OUT6	OUT5	OUT4	OUT3	OUT2	OUT1	OUT0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	OUT7	IO set output for pin 7 Default Value: 0
6	OUT6	IO set output for pin 6 Default Value: 0
5	OUT5	IO set output for pin 5 Default Value: 0
4	OUT4	IO set output for pin 4 Default Value: 0
3	OUT3	IO set output for pin 3 Default Value: 0
2	OUT2	IO set output for pin 2 Default Value: 0
1	OUT1	IO set output for pin 1 Default Value: 0

16.1.3 GPIO_PRT0_OUT_SET (continued)

0	OUT0	IO set output for pin 0: '0': Output state not affected. '1': Output state set to '1'. Default Value: 0

16.1.4 GPIO_PRT0_OUT_INV

Port output data invert register

Address: 0x4032000C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	A	A	A	A	A	A	A	A
Name	OUT7	OUT6	OUT5	OUT4	OUT3	OUT2	OUT1	OUT0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	OUT7	IO invert output for pin 7 Default Value: 0
6	OUT6	IO invert output for pin 6 Default Value: 0
5	OUT5	IO invert output for pin 5 Default Value: 0
4	OUT4	IO invert output for pin 4 Default Value: 0
3	OUT3	IO invert output for pin 3 Default Value: 0
2	OUT2	IO invert output for pin 2 Default Value: 0
1	OUT1	IO invert output for pin 1 Default Value: 0

16.1.4 GPIO_PRT0_OUT_INV (continued)

0	OUT0	IO invert output for pin 0: '0': Output state not affected. '1': Output state inverted ('0' => '1', '1' => '0'). Default Value: 0

16.1.5 GPIO_PRT0_IN

Port input state register

Address: 0x40320010

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R	R	R	R	R	R
HW Access	None		W	W	W	W	W	W
Name	None [7:6]		IN5	IN4	IN3	IN2	IN1	IN0

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							FLT_IN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_IN	Reads of this register return the logical state of the filtered pin as selected in the IN-TR_CFG.FLT_SEL register. Default Value: 0
5	IN5	IO pin state for pin 5 Default Value: 0
4	IN4	IO pin state for pin 4 Default Value: 0
3	IN3	IO pin state for pin 3 Default Value: 0
2	IN2	IO pin state for pin 2 Default Value: 0
1	IN1	IO pin state for pin 1 Default Value: 0
0	IN0	IO pin state for pin 0 '0': Low logic level present on pin. '1': High logic level present on pin. Default Value: 0

16.1.6 GPIO_PRT0_INTR

Port interrupt status register

Address: 0x40320014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	None		A	A	A	A	A	A
Name	None [7:6]		EDGE5	EDGE4	EDGE3	EDGE2	EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1C
HW Access	None							A
Name	None [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	None		R	R	R	R	R	R
HW Access	None		W	W	W	W	W	W
Name	None [23:22]		IN_IN5	IN_IN4	IN_IN3	IN_IN2	IN_IN1	IN_IN0

Bits	31	30	29	28	27	26	25	24
SW Access	None							R
HW Access	None							W
Name	None [31:25]							FLT_IN_IN

Bits	Name	Description
24	FLT_IN_IN	Filtered pin state for pin selected by INTR_CFG.FLT_SEL Default Value: 0
21	IN_IN5	IO pin state for pin 5 Default Value: 0
20	IN_IN4	IO pin state for pin 4 Default Value: 0
19	IN_IN3	IO pin state for pin 3 Default Value: 0
18	IN_IN2	IO pin state for pin 2 Default Value: 0
17	IN_IN1	IO pin state for pin 1 Default Value: 0
16	IN_IN0	IO pin state for pin 0 Default Value: 0
8	FLT_EDGE	Edge detected on filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0

16.1.6 GPIO_PRT0_INTR (continued)

5	EDGE5	Edge detect for IO pin 5 Default Value: 0
4	EDGE4	Edge detect for IO pin 4 Default Value: 0
3	EDGE3	Edge detect for IO pin 3 Default Value: 0
2	EDGE2	Edge detect for IO pin 2 Default Value: 0
1	EDGE1	Edge detect for IO pin 1 Default Value: 0
0	EDGE0	Edge detect for IO pin 0 '0': No edge was detected on pin. '1': An edge was detected on pin. Default Value: 0

16.1.7 GPIO_PRT0_INTR_MASK

Port interrupt mask register

Address: 0x40320018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		R	R	R	R	R	R
Name	None [7:6]		EDGE5	EDGE4	EDGE3	EDGE2	EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_EDGE	Masks edge interrupt on filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
5	EDGE5	Masks edge interrupt on IO pin 5 Default Value: 0
4	EDGE4	Masks edge interrupt on IO pin 4 Default Value: 0
3	EDGE3	Masks edge interrupt on IO pin 3 Default Value: 0
2	EDGE2	Masks edge interrupt on IO pin 2 Default Value: 0
1	EDGE1	Masks edge interrupt on IO pin 1 Default Value: 0
0	EDGE0	Masks edge interrupt on IO pin 0 '0': Pin interrupt forwarding disabled '1': Pin interrupt forwarding enabled Default Value: 0

16.1.8 GPIO_PRT0_INTR_MASKED

Port interrupt masked status register

Address: 0x4032001C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R	R	R	R	R	R
HW Access	None		W	W	W	W	W	W
Name	None [7:6]		EDGE5	EDGE4	EDGE3	EDGE2	EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_EDGE	Edge detected and masked on filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
5	EDGE5	Edge detected and masked on IO pin 5 Default Value: 0
4	EDGE4	Edge detected and masked on IO pin 4 Default Value: 0
3	EDGE3	Edge detected and masked on IO pin 3 Default Value: 0
2	EDGE2	Edge detected and masked on IO pin 2 Default Value: 0
1	EDGE1	Edge detected and masked on IO pin 1 Default Value: 0
0	EDGE0	Edge detected AND masked on IO pin 0 '0': Interrupt was not forwarded to CPU '1': Interrupt occurred and was forwarded to CPU Default Value: 0

16.1.9 GPIO_PRT0_INTR_SET (continued)

16.1.9 GPIO_PRT0_INTR_SET

Port interrupt set register

Address: 0x40320020

Retention: Retained

Bits	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SW Access	None		RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	None		A	A	A	A	A	A
Name	None [7:6]		EDGE5	EDGE4	EDGE3	EDGE2	EDGE1	EDGE0

Bits	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SW Access	None							RW1S
HW Access	None							A
Name	None [15:9]							FLT_EDGE

Bits	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	**Name**	**Description**
8	FLT_EDGE	Sets edge detect interrupt for filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
5	EDGE5	Sets edge detect interrupt for IO pin 5 Default Value: 0
4	EDGE4	Sets edge detect interrupt for IO pin 4 Default Value: 0
3	EDGE3	Sets edge detect interrupt for IO pin 3 Default Value: 0
2	EDGE2	Sets edge detect interrupt for IO pin 2 Default Value: 0
1	EDGE1	Sets edge detect interrupt for IO pin 1 Default Value: 0

16.1.9 GPIO_PRT0_INTR_SET (continued)

0	EDGE0	Sets edge detect interrupt for IO pin 0 '0': Interrupt state not affected '1': Interrupt set Default Value: 0

16.1.10 GPIO_PRT0_INTR_CFG

Port interrupt configuration register

Address: 0x40320024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	EDGE3_SEL [7:6]		EDGE2_SEL [5:4]		EDGE1_SEL [3:2]		EDGE0_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW		RW	
HW Access	None				R		R	
Name	None [15:12]				EDGE5_SEL [11:10]		EDGE4_SEL [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW			RW	
HW Access	None			R			R	
Name	None [23:21]			FLT_SEL [20:18]			FLT_EDGE_SEL [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
20 : 18	FLT_SEL	Selects which pin is routed through the 50ns glitch filter to provide a glitch-safe interrupt. Default Value: 0
17 : 16	FLT_EDGE_SEL	Sets which edge will trigger an IRQ for the glitch filtered pin (selected by INTR_CFG.FLT_SEL Default Value: 0 **0x0: DISABLE :** Disabled **0x1: RISING :** Rising edge **0x2: FALLING :** Falling edge

16.1.10 GPIO_PRT0_INTR_CFG (continued)

		0x3: BOTH : Both rising and falling edges
11 : 10	EDGE5_SEL	Sets which edge will trigger an IRQ for IO pin 5 Default Value: 0
9 : 8	EDGE4_SEL	Sets which edge will trigger an IRQ for IO pin 4 Default Value: 0
7 : 6	EDGE3_SEL	Sets which edge will trigger an IRQ for IO pin 3 Default Value: 0
5 : 4	EDGE2_SEL	Sets which edge will trigger an IRQ for IO pin 2 Default Value: 0
3 : 2	EDGE1_SEL	Sets which edge will trigger an IRQ for IO pin 1 Default Value: 0
1 : 0	EDGE0_SEL	Sets which edge will trigger an IRQ for IO pin 0 Default Value: 0 **0x0: DISABLE :** Disabled **0x1: RISING :** Rising edge **0x2: FALLING :** Falling edge **0x3: BOTH :** Both rising and falling edges

16.1.11 GPIO_PRT0_CFG

Port configuration register

Address: 0x40320028

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW			RW	RW		
HW Access	R	R			R	R		
Name	IN_EN1	DRIVE_MODE1 [6:4]			IN_EN0	DRIVE_MODE0 [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW			RW	RW		
HW Access	R	R			R	R		
Name	IN_EN3	DRIVE_MODE3 [14:12]			IN_EN2	DRIVE_MODE2 [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW			RW	RW		
HW Access	R	R			R	R		
Name	IN_EN5	DRIVE_MODE5 [22:20]			IN_EN4	DRIVE_MODE4 [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23	IN_EN5	Enables the input buffer for IO pin 5 Default Value: 0
22 : 20	DRIVE_MODE5	The GPIO drive mode for IO pin 5 Default Value: 0
19	IN_EN4	Enables the input buffer for IO pin 4 Default Value: 0
18 : 16	DRIVE_MODE4	The GPIO drive mode for IO pin4 Default Value: 0
15	IN_EN3	Enables the input buffer for IO pin 3 Default Value: 0
14 : 12	DRIVE_MODE3	The GPIO drive mode for IO pin 3 Default Value: 0
11	IN_EN2	Enables the input buffer for IO pin 2 Default Value: 0
10 : 8	DRIVE_MODE2	The GPIO drive mode for IO pin 2 Default Value: 0

16.1.11 GPIO_PRT0_CFG (continued)

7	IN_EN1	Enables the input buffer for IO pin 1 Default Value: 0
6 : 4	DRIVE_MODE1	The GPIO drive mode for IO pin 1 Default Value: 0
3	IN_EN0	Enables the input buffer for IO pin 0. This bit should be cleared when analog signals are present on the pin to avoid crowbar currents. The output buffer can be used to drive analog signals high or low without issue. '0': Input buffer disabled '1': Input buffer enabled Default Value: 0
2 : 0	DRIVE_MODE0	The GPIO drive mode for IO pin 0. Resistive pull-up and pull-down is selected in the drive mode. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the peripheral and HSIOM (HSIOM_PRT_SELx) is properly configured before turning the IO on here to avoid producing glitches on the bus. Note: that peripherals other than GPIO & UDB/DSI directly control both the output and output-enable of the output buffer (peripherals can drive strong 0 or strong 1 in any mode except OFF='0'). Note: D_OUT, D_OUT_EN are pins of GPIO cell. Default Value: 0 **0x0: HIGHZ :** Output buffer is off creating a high impedance input D_OUT = '0': High Impedance D_OUT = '1': High Impedance **0x1: RESERVED :** This mode is reserved and should not be used. No damage will occur if this mode is selected. The pin will generally perform the same as the STRONG drive mode although this is not guaranteed for all use cases. For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance

16.1.11 GPIO_PRT0_CFG (continued)

0x2: PULLUP :

Resistive pull up
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
 D_OUT = '0': Strong pull down
 D_OUT = '1': Weak/resistive pull up
When D_OUT_EN = 0:
 D_OUT = '0': High impedance
 D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
 D_OUT = '0': Strong pull down
 D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
 D_OUT = '0': Weak/resistive pull up
 D_OUT = '1': Weak/resistive pull up

0x3: PULLDOWN :

Resistive pull down
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
 D_OUT = '0': Weak/resistive pull down
 D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
 D_OUT = '0': High impedance
 D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
 D_OUT = '0': Strong pull down
 D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
 D_OUT = '0': Weak/resistive pull down
 D_OUT = '1': Weak/resistive pull down

0x4: OD_DRIVESLOW :

Open drain, drives low
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
 D_OUT = '0': Strong pull down
 D_OUT = '1': High Impedance
When D_OUT_EN = 0:
 D_OUT = '0': High impedance
 D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
 D_OUT = '0': Strong pull down
 D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
 D_OUT = '0': High Impedance
 D_OUT = '1': High Impedance

16.1.11 GPIO_PRT0_CFG (continued)

0x5: OD_DRIVESHIGH :

Open drain, drives high
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
 D_OUT = '0': High Impedance
 D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
 D_OUT = '0': High impedance
 D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
 D_OUT = '0': Strong pull down
 D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
 D_OUT = '0': High Impedance
 D_OUT = '1': High Impedance

0x6: STRONG :

Strong D_OUTput buffer
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
 D_OUT = '0': Strong pull down
 D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
 D_OUT = '0': High impedance
 D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
 D_OUT = '0': Strong pull down
 D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
 D_OUT = '0': High Impedance
 D_OUT = '1': High Impedance

0x7: PULLUP_DOWN :

Pull up or pull down
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = '0':
 GPIO_DSI_OUT = '0': Weak/resistive pull down
 GPIO_DSI_OUT = '1': Weak/resistive pull up
where "GPIO_DSI_OUT" is a function of PORT_SEL, OUT & DSI_DATA_OUT.
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
 D_OUT = '0': Strong pull down
 D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
 D_OUT = '0': Weak/resistive pull down
 D_OUT = '1': Weak/resistive pull up

16.1.12 GPIO_PRT0_CFG_IN

Port input buffer configuration register

Address: 0x4032002C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		R	R	R	R	R	R
Name	None [7:6]		VTRIP_-SEL5_0	VTRIP_-SEL4_0	VTRIP_-SEL3_0	VTRIP_-SEL2_0	VTRIP_-SEL1_0	VTRIP_-SEL0_0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	VTRIP_SEL5_0	Configures the pin 5 input buffer mode (trip points and hysteresis) Default Value: 0
4	VTRIP_SEL4_0	Configures the pin 4 input buffer mode (trip points and hysteresis) Default Value: 0
3	VTRIP_SEL3_0	Configures the pin 3 input buffer mode (trip points and hysteresis) Default Value: 0
2	VTRIP_SEL2_0	Configures the pin 2 input buffer mode (trip points and hysteresis) Default Value: 0
1	VTRIP_SEL1_0	Configures the pin 1 input buffer mode (trip points and hysteresis) Default Value: 0
0	VTRIP_SEL0_0	Configures the pin 0 input buffer mode (trip points and hysteresis) Default Value: 0

16.1.12 GPIO_PRT0_CFG_IN (continued)

0x0: CMOS :

S40E: {CFG_IN_GPIO5V.VTRIP_SEL0_1, CFG_IN.VTRIP_SEL0_0}
0,0: CMOS
0,1: TTL
1,0: input buffer is compatible with automotive.
1,1: input buffer is compatible with automotvie

0x1: TTL :

S40S: Input buffer compatible with TTL and MediaLB interfaces

16.1.13 GPIO_PRT0_CFG_OUT

Port output buffer configuration register

Address: 0x40320030

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		R	R	R	R	R	R
Name	None [7:6]		SLOW5	SLOW4	SLOW3	SLOW2	SLOW1	SLOW0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	DRIVE_SEL3 [23:22]		DRIVE_SEL2 [21:20]		DRIVE_SEL1 [19:18]		DRIVE_SEL0 [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None				RW		RW	
HW Access	None				R		R	
Name	None [31:28]				DRIVE_SEL5 [27:26]		DRIVE_SEL4 [25:24]	

Bits	Name	Description
27 : 26	DRIVE_SEL5	Sets the GPIO drive strength for IO pin 5 Default Value: 0
25 : 24	DRIVE_SEL4	Sets the GPIO drive strength for IO pin 4 Default Value: 0
23 : 22	DRIVE_SEL3	Sets the GPIO drive strength for IO pin 3 Default Value: 0
21 : 20	DRIVE_SEL2	Sets the GPIO drive strength for IO pin 2 Default Value: 0
19 : 18	DRIVE_SEL1	Sets the GPIO drive strength for IO pin 1 Default Value: 0
17 : 16	DRIVE_SEL0	Sets the GPIO drive strength for IO pin 0 Default Value: 0 **0x0: FULL_DRIVE :** Full drive strength: GPIO drives current at its max rated spec.

16.1.13 GPIO_PRT0_CFG_OUT (continued)

		0x1: ONE_HALF_DRIVE : 1/2 drive strength: GPIO drives current at 1/2 of its max rated spec **0x2: ONE_QUARTER_DRIVE :** 1/4 drive strength: GPIO drives current at 1/4 of its max rated spec. **0x3: ONE_EIGHTH_DRIVE :** 1/8 drive strength: GPIO drives current at 1/8 of its max rated spec.
5	SLOW5	Enables slow slew rate for IO pin 5 Default Value: 0
4	SLOW4	Enables slow slew rate for IO pin 4 Default Value: 0
3	SLOW3	Enables slow slew rate for IO pin 3 Default Value: 0
2	SLOW2	Enables slow slew rate for IO pin 2 Default Value: 0
1	SLOW1	Enables slow slew rate for IO pin 1 Default Value: 0
0	SLOW0	Enables slow slew rate for IO pin 0 '0': Fast slew rate '1': Slow slew rate Default Value: 0

16.1.14 GPIO_PRT2_OUT

Port output data register

Address: 0x40320100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	OUT7	OUT6	OUT5	OUT4	OUT3	OUT2	OUT1	OUT0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	OUT7	IO output data for pin 7 Default Value: 0
6	OUT6	IO output data for pin 6 Default Value: 0
5	OUT5	IO output data for pin 5 Default Value: 0
4	OUT4	IO output data for pin 4 Default Value: 0
3	OUT3	IO output data for pin 3 Default Value: 0
2	OUT2	IO output data for pin 2 Default Value: 0
1	OUT1	IO output data for pin 1 Default Value: 0

16.1.14 GPIO_PRT2_OUT (continued)

0	OUT0	IO output data for pin 0 '0': Output state set to '0' '1': Output state set to '1' Default Value: 0

16.1.15 GPIO_PRT2_IN

Port input state register

Address: 0x40320110

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	IN7	IN6	IN5	IN4	IN3	IN2	IN1	IN0

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							FLT_IN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_IN	Reads of this register return the logical state of the filtered pin as selected in the INTR_CFG.FLT_SEL register. Default Value: 0
7	IN7	IO pin state for pin 7 Default Value: 0
6	IN6	IO pin state for pin 6 Default Value: 0
5	IN5	IO pin state for pin 5 Default Value: 0
4	IN4	IO pin state for pin 4 Default Value: 0
3	IN3	IO pin state for pin 3 Default Value: 0
2	IN2	IO pin state for pin 2 Default Value: 0

16.1.15 GPIO_PRT2_IN (continued)

1	IN1	IO pin state for pin 1 Default Value: 0
0	IN0	IO pin state for pin 0 '0': Low logic level present on pin. '1': High logic level present on pin. Default Value: 0

16.1.16 GPIO_PRT2_INTR

Port interrupt status register

Address: 0x40320114

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	A	A	A	A	A	A	A	A
Name	EDGE7	EDGE6	EDGE5	EDGE4	EDGE3	EDGE2	EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1C
HW Access	None							A
Name	None [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	IN_IN7	IN_IN6	IN_IN5	IN_IN4	IN_IN3	IN_IN2	IN_IN1	IN_IN0

Bits	31	30	29	28	27	26	25	24
SW Access	None							R
HW Access	None							W
Name	None [31:25]							FLT_IN_IN

Bits	Name	Description
24	FLT_IN_IN	Filtered pin state for pin selected by INTR_CFG.FLT_SEL Default Value: 0
23	IN_IN7	IO pin state for pin 7 Default Value: 0
22	IN_IN6	IO pin state for pin 6 Default Value: 0
21	IN_IN5	IO pin state for pin 5 Default Value: 0
20	IN_IN4	IO pin state for pin 4 Default Value: 0
19	IN_IN3	IO pin state for pin 3 Default Value: 0
18	IN_IN2	IO pin state for pin 2 Default Value: 0
17	IN_IN1	IO pin state for pin 1 Default Value: 0

16.1.16 GPIO_PRT2_INTR (continued)

16	IN_IN0	IO pin state for pin 0 Default Value: 0
8	FLT_EDGE	Edge detected on filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
7	EDGE7	Edge detect for IO pin 7 Default Value: 0
6	EDGE6	Edge detect for IO pin 6 Default Value: 0
5	EDGE5	Edge detect for IO pin 5 Default Value: 0
4	EDGE4	Edge detect for IO pin 4 Default Value: 0
3	EDGE3	Edge detect for IO pin 3 Default Value: 0
2	EDGE2	Edge detect for IO pin 2 Default Value: 0
1	EDGE1	Edge detect for IO pin 1 Default Value: 0
0	EDGE0	Edge detect for IO pin 0 '0': No edge was detected on pin. '1': An edge was detected on pin. Default Value: 0

16.1.17 GPIO_PRT2_INTR_MASK

Port interrupt mask register

Address: 0x40320118

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	EDGE7	EDGE6	EDGE5	EDGE4	EDGE3	EDGE2	EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_EDGE	Masks edge interrupt on filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
7	EDGE7	Masks edge interrupt on IO pin 7 Default Value: 0
6	EDGE6	Masks edge interrupt on IO pin 6 Default Value: 0
5	EDGE5	Masks edge interrupt on IO pin 5 Default Value: 0
4	EDGE4	Masks edge interrupt on IO pin 4 Default Value: 0
3	EDGE3	Masks edge interrupt on IO pin 3 Default Value: 0
2	EDGE2	Masks edge interrupt on IO pin 2 Default Value: 0
1	EDGE1	Masks edge interrupt on IO pin 1 Default Value: 0

16.1.17 GPIO_PRT2_INTR_MASK (continued)

0	EDGE0	Masks edge interrupt on IO pin 0 '0': Pin interrupt forwarding disabled '1': Pin interrupt forwarding enabled Default Value: 0

16.1.18 GPIO_PRT2_INTR_MASKED

Port interrupt masked status register

Address: 0x4032011C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	EDGE7	EDGE6	EDGE5	EDGE4	EDGE3	EDGE2	EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_EDGE	Edge detected and masked on filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
7	EDGE7	Edge detected and masked on IO pin 7 Default Value: 0
6	EDGE6	Edge detected and masked on IO pin 6 Default Value: 0
5	EDGE5	Edge detected and masked on IO pin 5 Default Value: 0
4	EDGE4	Edge detected and masked on IO pin 4 Default Value: 0
3	EDGE3	Edge detected and masked on IO pin 3 Default Value: 0
2	EDGE2	Edge detected and masked on IO pin 2 Default Value: 0
1	EDGE1	Edge detected and masked on IO pin 1 Default Value: 0

16.1.18 GPIO_PRT2_INTR_MASKED (continued)

0	EDGE0	Edge detected AND masked on IO pin 0 '0': Interrupt was not forwarded to CPU '1': Interrupt occurred and was forwarded to CPU Default Value: 0

16.1.19 GPIO_PRT2_INTR_SET

Port interrupt set register

Address: 0x40320120

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	A	A	A	A	A	A	A	A
Name	EDGE7	EDGE6	EDGE5	EDGE4	EDGE3	EDGE2	EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1S
HW Access	None							A
Name	None [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_EDGE	Sets edge detect interrupt for filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
7	EDGE7	Sets edge detect interrupt for IO pin 7 Default Value: 0
6	EDGE6	Sets edge detect interrupt for IO pin 6 Default Value: 0
5	EDGE5	Sets edge detect interrupt for IO pin 5 Default Value: 0
4	EDGE4	Sets edge detect interrupt for IO pin 4 Default Value: 0
3	EDGE3	Sets edge detect interrupt for IO pin 3 Default Value: 0
2	EDGE2	Sets edge detect interrupt for IO pin 2 Default Value: 0
1	EDGE1	Sets edge detect interrupt for IO pin 1 Default Value: 0

16.1.19 GPIO_PRT2_INTR_SET (continued)

0	EDGE0	Sets edge detect interrupt for IO pin 0 '0': Interrupt state not affected '1': Interrupt set Default Value: 0

16.1.20 GPIO_PRT2_INTR_CFG

Port interrupt configuration register

Address: 0x40320124

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	EDGE3_SEL [7:6]		EDGE2_SEL [5:4]		EDGE1_SEL [3:2]		EDGE0_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	EDGE7_SEL [15:14]		EDGE6_SEL [13:12]		EDGE5_SEL [11:10]		EDGE4_SEL [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW			RW	
HW Access	None			R			R	
Name	None [23:21]			FLT_SEL [20:18]			FLT_EDGE_SEL [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
20 : 18	FLT_SEL	Selects which pin is routed through the 50ns glitch filter to provide a glitch-safe interrupt. Default Value: 0
17 : 16	FLT_EDGE_SEL	Sets which edge will trigger an IRQ for the glitch filtered pin (selected by INTR_CFG.FLT_SEL Default Value: 0 **0x0: DISABLE :** Disabled **0x1: RISING :** Rising edge **0x2: FALLING :** Falling edge

16.1.20 GPIO_PRT2_INTR_CFG (continued)

		0x3: BOTH : Both rising and falling edges
15 : 14	EDGE7_SEL	Sets which edge will trigger an IRQ for IO pin 7 Default Value: 0
13 : 12	EDGE6_SEL	Sets which edge will trigger an IRQ for IO pin 6 Default Value: 0
11 : 10	EDGE5_SEL	Sets which edge will trigger an IRQ for IO pin 5 Default Value: 0
9 : 8	EDGE4_SEL	Sets which edge will trigger an IRQ for IO pin 4 Default Value: 0
7 : 6	EDGE3_SEL	Sets which edge will trigger an IRQ for IO pin 3 Default Value: 0
5 : 4	EDGE2_SEL	Sets which edge will trigger an IRQ for IO pin 2 Default Value: 0
3 : 2	EDGE1_SEL	Sets which edge will trigger an IRQ for IO pin 1 Default Value: 0
1 : 0	EDGE0_SEL	Sets which edge will trigger an IRQ for IO pin 0 Default Value: 0 **0x0: DISABLE :** Disabled **0x1: RISING :** Rising edge **0x2: FALLING :** Falling edge **0x3: BOTH :** Both rising and falling edges

16.1.21 GPIO_PRT2_CFG

Port configuration register

Address: 0x40320128

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW			RW	RW		
HW Access	R	R			R	R		
Name	IN_EN1	DRIVE_MODE1 [6:4]			IN_EN0	DRIVE_MODE0 [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW			RW	RW		
HW Access	R	R			R	R		
Name	IN_EN3	DRIVE_MODE3 [14:12]			IN_EN2	DRIVE_MODE2 [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW			RW	RW		
HW Access	R	R			R	R		
Name	IN_EN5	DRIVE_MODE5 [22:20]			IN_EN4	DRIVE_MODE4 [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW			RW	RW		
HW Access	R	R			R	R		
Name	IN_EN7	DRIVE_MODE7 [30:28]			IN_EN6	DRIVE_MODE6 [26:24]		

Bits	Name	Description
31	IN_EN7	Enables the input buffer for IO pin 7 Default Value: 0
30 : 28	DRIVE_MODE7	The GPIO drive mode for IO pin 7 Default Value: 0
27	IN_EN6	Enables the input buffer for IO pin 6 Default Value: 0
26 : 24	DRIVE_MODE6	The GPIO drive mode for IO pin 6 Default Value: 0
23	IN_EN5	Enables the input buffer for IO pin 5 Default Value: 0
22 : 20	DRIVE_MODE5	The GPIO drive mode for IO pin 5 Default Value: 0
19	IN_EN4	Enables the input buffer for IO pin 4 Default Value: 0
18 : 16	DRIVE_MODE4	The GPIO drive mode for IO pin4 Default Value: 0

16.1.21 GPIO_PRT2_CFG (continued)

15	IN_EN3	Enables the input buffer for IO pin 3 Default Value: 0
14 : 12	DRIVE_MODE3	The GPIO drive mode for IO pin 3 Default Value: 0
11	IN_EN2	Enables the input buffer for IO pin 2 Default Value: 0
10 : 8	DRIVE_MODE2	The GPIO drive mode for IO pin 2 Default Value: 0
7	IN_EN1	Enables the input buffer for IO pin 1 Default Value: 0
6 : 4	DRIVE_MODE1	The GPIO drive mode for IO pin 1 Default Value: 0
3	IN_EN0	Enables the input buffer for IO pin 0. This bit should be cleared when analog signals are present on the pin to avoid crowbar currents. The output buffer can be used to drive analog signals high or low without issue. '0': Input buffer disabled '1': Input buffer enabled Default Value: 0
2 : 0	DRIVE_MODE0	The GPIO drive mode for IO pin 0. Resistive pull-up and pull-down is selected in the drive mode. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the peripheral and HSIOM (HSIOM_PRT_SELx) is properly configured before turning the IO on here to avoid producing glitches on the bus. Note: that peripherals other than GPIO & UDB/DSI directly control both the output and output-enable of the output buffer (peripherals can drive strong 0 or strong 1 in any mode except OFF='0'). Note: D_OUT, D_OUT_EN are pins of GPIO cell. Default Value: 0 **0x0: HIGHZ :** Output buffer is off creating a high impedance input D_OUT = '0': High Impedance D_OUT = '1': High Impedance **0x1: RESERVED :** This mode is reserved and should not be used. No damage will occur if this mode is selected. The pin will generally perform the same as the STRONG drive mode although this is not guaranteed for all use cases. For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance

16.1.21 GPIO_PRT2_CFG (continued)

0x2: PULLUP :

Resistive pull up
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Weak/resistive pull up
When D_OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': Weak/resistive pull up
D_OUT = '1': Weak/resistive pull up

0x3: PULLDOWN :

Resistive pull down
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
D_OUT = '0': Weak/resistive pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': Weak/resistive pull down
D_OUT = '1': Weak/resistive pull down

0x4: OD_DRIVESLOW :

Open drain, drives low
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': High Impedance
When D_OUT_EN = 0:
D_OUT = '0': High impedance
D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
D_OUT = '0': Strong pull down
D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
D_OUT = '0': High Impedance
D_OUT = '1': High Impedance

16.1.21 GPIO_PRT2_CFG (continued)

0x5: OD_DRIVESHIGH :

Open drain, drives high
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
 D_OUT = '0': High Impedance
 D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
 D_OUT = '0': High impedance
 D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
 D_OUT = '0': Strong pull down
 D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
 D_OUT = '0': High Impedance
 D_OUT = '1': High Impedance

0x6: STRONG :

Strong D_OUTput buffer
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
 D_OUT = '0': Strong pull down
 D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
 D_OUT = '0': High impedance
 D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
 D_OUT = '0': Strong pull down
 D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
 D_OUT = '0': High Impedance
 D_OUT = '1': High Impedance

0x7: PULLUP_DOWN :

Pull up or pull down
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = '0':
 GPIO_DSI_OUT = '0': Weak/resistive pull down
 GPIO_DSI_OUT = '1': Weak/resistive pull up
where "GPIO_DSI_OUT" is a function of PORT_SEL, OUT & DSI_DATA_OUT.
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
 D_OUT = '0': Strong pull down
 D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
 D_OUT = '0': Weak/resistive pull down
 D_OUT = '1': Weak/resistive pull up

16.1.22 GPIO_PRT2_CFG_IN

Port input buffer configuration register

Address: 0x4032012C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	VTRIP_-SEL7_0	VTRIP_-SEL6_0	VTRIP_-SEL5_0	VTRIP_-SEL4_0	VTRIP_-SEL3_0	VTRIP_-SEL2_0	VTRIP_-SEL1_0	VTRIP_-SEL0_0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	VTRIP_SEL7_0	Configures the pin 7 input buffer mode (trip points and hysteresis) Default Value: 0
6	VTRIP_SEL6_0	Configures the pin 6 input buffer mode (trip points and hysteresis) Default Value: 0
5	VTRIP_SEL5_0	Configures the pin 5 input buffer mode (trip points and hysteresis) Default Value: 0
4	VTRIP_SEL4_0	Configures the pin 4 input buffer mode (trip points and hysteresis) Default Value: 0
3	VTRIP_SEL3_0	Configures the pin 3 input buffer mode (trip points and hysteresis) Default Value: 0
2	VTRIP_SEL2_0	Configures the pin 2 input buffer mode (trip points and hysteresis) Default Value: 0
1	VTRIP_SEL1_0	Configures the pin 1 input buffer mode (trip points and hysteresis) Default Value: 0

16.1.22 GPIO_PRT2_CFG_IN (continued)

0	VTRIP_SEL0_0	Configures the pin 0 input buffer mode (trip points and hysteresis) Default Value: 0 **0x0: CMOS :** S40E: {CFG_IN_GPIO5V.VTRIP_SEL0_1, CFG_IN.VTRIP_SEL0_0} 0,0: CMOS 0,1: TTL 1,0: input buffer is compatible with automotive. 1,1: input buffer is compatible with automotvie **0x1: TTL :** S40S: Input buffer compatible with TTL and MediaLB interfaces

16.1.23 GPIO_PRT2_CFG_OUT

Port output buffer configuration register

Address: 0x40320130

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	SLOW7	SLOW6	SLOW5	SLOW4	SLOW3	SLOW2	SLOW1	SLOW0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	DRIVE_SEL3 [23:22]		DRIVE_SEL2 [21:20]		DRIVE_SEL1 [19:18]		DRIVE_SEL0 [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	DRIVE_SEL7 [31:30]		DRIVE_SEL6 [29:28]		DRIVE_SEL5 [27:26]		DRIVE_SEL4 [25:24]	

Bits	Name	Description
31 : 30	DRIVE_SEL7	Sets the GPIO drive strength for IO pin 7 Default Value: 0
29 : 28	DRIVE_SEL6	Sets the GPIO drive strength for IO pin 6 Default Value: 0
27 : 26	DRIVE_SEL5	Sets the GPIO drive strength for IO pin 5 Default Value: 0
25 : 24	DRIVE_SEL4	Sets the GPIO drive strength for IO pin 4 Default Value: 0
23 : 22	DRIVE_SEL3	Sets the GPIO drive strength for IO pin 3 Default Value: 0
21 : 20	DRIVE_SEL2	Sets the GPIO drive strength for IO pin 2 Default Value: 0
19 : 18	DRIVE_SEL1	Sets the GPIO drive strength for IO pin 1 Default Value: 0
17 : 16	DRIVE_SEL0	Sets the GPIO drive strength for IO pin 0 Default Value: 0

16.1.23 GPIO_PRT2_CFG_OUT (continued)

		0x0: FULL_DRIVE : Full drive strength: GPIO drives current at its max rated spec. **0x1: ONE_HALF_DRIVE :** 1/2 drive strength: GPIO drives current at 1/2 of its max rated spec **0x2: ONE_QUARTER_DRIVE :** 1/4 drive strength: GPIO drives current at 1/4 of its max rated spec. **0x3: ONE_EIGHTH_DRIVE :** 1/8 drive strength: GPIO drives current at 1/8 of its max rated spec.
7	SLOW7	Enables slow slew rate for IO pin 7 Default Value: 0
6	SLOW6	Enables slow slew rate for IO pin 6 Default Value: 0
5	SLOW5	Enables slow slew rate for IO pin 5 Default Value: 0
4	SLOW4	Enables slow slew rate for IO pin 4 Default Value: 0
3	SLOW3	Enables slow slew rate for IO pin 3 Default Value: 0
2	SLOW2	Enables slow slew rate for IO pin 2 Default Value: 0
1	SLOW1	Enables slow slew rate for IO pin 1 Default Value: 0
0	SLOW0	Enables slow slew rate for IO pin 0 '0': Fast slew rate '1': Slow slew rate Default Value: 0

16.1.24 GPIO_PRT4_OUT

Port output data register

Address: 0x40320200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				RW	RW	RW	RW
Name	None [7:4]				OUT3	OUT2	OUT1	OUT0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	OUT3	IO output data for pin 3 Default Value: 0
2	OUT2	IO output data for pin 2 Default Value: 0
1	OUT1	IO output data for pin 1 Default Value: 0
0	OUT0	IO output data for pin 0 '0': Output state set to '0' '1': Output state set to '1' Default Value: 0

16.1.25 GPIO_PRT4_IN

Port input state register

Address: 0x40320210

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R	R	R	R
HW Access	None				W	W	W	W
Name	None [7:4]				IN3	IN2	IN1	IN0

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							FLT_IN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_IN	Reads of this register return the logical state of the filtered pin as selected in the IN-TR_CFG.FLT_SEL register. Default Value: 0
3	IN3	IO pin state for pin 3 Default Value: 0
2	IN2	IO pin state for pin 2 Default Value: 0
1	IN1	IO pin state for pin 1 Default Value: 0
0	IN0	IO pin state for pin 0 '0': Low logic level present on pin. '1': High logic level present on pin. Default Value: 0

16.1.26 GPIO_PRT4_INTR

Port interrupt status register

Address: 0x40320214

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1C	RW1C	RW1C	RW1C
HW Access	None				A	A	A	A
Name	None [7:4]				EDGE3	EDGE2	EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1C
HW Access	None							A
Name	None [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	None				R	R	R	R
HW Access	None				W	W	W	W
Name	None [23:20]				IN_IN3	IN_IN2	IN_IN1	IN_IN0

Bits	31	30	29	28	27	26	25	24
SW Access	None							R
HW Access	None							W
Name	None [31:25]							FLT_IN_IN

Bits	Name	Description
24	FLT_IN_IN	Filtered pin state for pin selected by INTR_CFG.FLT_SEL Default Value: 0
19	IN_IN3	IO pin state for pin 3 Default Value: 0
18	IN_IN2	IO pin state for pin 2 Default Value: 0
17	IN_IN1	IO pin state for pin 1 Default Value: 0
16	IN_IN0	IO pin state for pin 0 Default Value: 0
8	FLT_EDGE	Edge detected on filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
3	EDGE3	Edge detect for IO pin 3 Default Value: 0
2	EDGE2	Edge detect for IO pin 2 Default Value: 0

16.1.26 GPIO_PRT4_INTR (continued)

1	EDGE1	Edge detect for IO pin 1 Default Value: 0
0	EDGE0	Edge detect for IO pin 0 '0': No edge was detected on pin. '1': An edge was detected on pin. Default Value: 0

16.1.27 GPIO_PRT4_INTR_MASK

Port interrupt mask register

Address: 0x40320218

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [7:4]				EDGE3	EDGE2	EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_EDGE	Masks edge interrupt on filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
3	EDGE3	Masks edge interrupt on IO pin 3 Default Value: 0
2	EDGE2	Masks edge interrupt on IO pin 2 Default Value: 0
1	EDGE1	Masks edge interrupt on IO pin 1 Default Value: 0
0	EDGE0	Masks edge interrupt on IO pin 0 '0': Pin interrupt forwarding disabled '1': Pin interrupt forwarding enabled Default Value: 0

16.1.28 GPIO_PRT4_INTR_MASKED

Port interrupt masked status register

Address: 0x4032021C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R	R	R	R
HW Access	None				W	W	W	W
Name	None [7:4]				EDGE3	EDGE2	EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_EDGE	Edge detected and masked on filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
3	EDGE3	Edge detected and masked on IO pin 3 Default Value: 0
2	EDGE2	Edge detected and masked on IO pin 2 Default Value: 0
1	EDGE1	Edge detected and masked on IO pin 1 Default Value: 0
0	EDGE0	Edge detected AND masked on IO pin 0 '0': Interrupt was not forwarded to CPU '1': Interrupt occurred and was forwarded to CPU Default Value: 0

16.1.29 GPIO_PRT4_INTR_SET

Port interrupt set register

Address: 0x40320220

Retention: Retained

Bits	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SW Access	None				RW1S	RW1S	RW1S	RW1S
HW Access	None				A	A	A	A
Name	None [7:4]				EDGE3	EDGE2	EDGE1	EDGE0

Bits	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SW Access	None							RW1S
HW Access	None							A
Name	None [15:9]							FLT_EDGE

Bits	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	**Name**	**Description**
8	FLT_EDGE	Sets edge detect interrupt for filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
3	EDGE3	Sets edge detect interrupt for IO pin 3 Default Value: 0
2	EDGE2	Sets edge detect interrupt for IO pin 2 Default Value: 0
1	EDGE1	Sets edge detect interrupt for IO pin 1 Default Value: 0
0	EDGE0	Sets edge detect interrupt for IO pin 0 '0': Interrupt state not affected '1': Interrupt set Default Value: 0

16.1.30 GPIO_PRT4_INTR_CFG (continued)

16.1.30 GPIO_PRT4_INTR_CFG

Port interrupt configuration register

Address: 0x40320224

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	EDGE3_SEL [7:6]		EDGE2_SEL [5:4]		EDGE1_SEL [3:2]		EDGE0_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW			RW	
HW Access	None			R			R	
Name	None [23:21]			FLT_SEL [20:18]			FLT_EDGE_SEL [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
20 : 18	FLT_SEL	Selects which pin is routed through the 50ns glitch filter to provide a glitch-safe interrupt. Default Value: 0
17 : 16	FLT_EDGE_SEL	Sets which edge will trigger an IRQ for the glitch filtered pin (selected by INTR_CFG.FLT_SEL Default Value: 0 **0x0: DISABLE :** Disabled **0x1: RISING :** Rising edge **0x2: FALLING :** Falling edge

16.1.30 GPIO_PRT4_INTR_CFG (continued)

		0x3: BOTH : Both rising and falling edges
7 : 6	EDGE3_SEL	Sets which edge will trigger an IRQ for IO pin 3 Default Value: 0
5 : 4	EDGE2_SEL	Sets which edge will trigger an IRQ for IO pin 2 Default Value: 0
3 : 2	EDGE1_SEL	Sets which edge will trigger an IRQ for IO pin 1 Default Value: 0
1 : 0	EDGE0_SEL	Sets which edge will trigger an IRQ for IO pin 0 Default Value: 0 **0x0: DISABLE :** Disabled **0x1: RISING :** Rising edge **0x2: FALLING :** Falling edge **0x3: BOTH :** Both rising and falling edges

16.1.31 GPIO_PRT4_CFG

Port configuration register

Address: 0x40320228

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW			RW	RW		
HW Access	R	R			R	R		
Name	IN_EN1	DRIVE_MODE1 [6:4]			IN_EN0	DRIVE_MODE0 [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW			RW	RW		
HW Access	R	R			R	R		
Name	IN_EN3	DRIVE_MODE3 [14:12]			IN_EN2	DRIVE_MODE2 [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15	IN_EN3	Enables the input buffer for IO pin 3 Default Value: 0
14 : 12	DRIVE_MODE3	The GPIO drive mode for IO pin 3 Default Value: 0
11	IN_EN2	Enables the input buffer for IO pin 2 Default Value: 0
10 : 8	DRIVE_MODE2	The GPIO drive mode for IO pin 2 Default Value: 0
7	IN_EN1	Enables the input buffer for IO pin 1 Default Value: 0
6 : 4	DRIVE_MODE1	The GPIO drive mode for IO pin 1 Default Value: 0

16.1.31 GPIO_PRT4_CFG (continued)

3	IN_EN0	Enables the input buffer for IO pin 0. This bit should be cleared when analog signals are present on the pin to avoid crowbar currents. The output buffer can be used to drive analog signals high or low without issue. '0': Input buffer disabled '1': Input buffer enabled Default Value: 0
2 : 0	DRIVE_MODE0	The GPIO drive mode for IO pin 0. Resistive pull-up and pull-down is selected in the drive mode. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the peripheral and HSIOM (HSIOM_PRT_SELx) is properly configured before turning the IO on here to avoid producing glitches on the bus. Note: that peripherals other than GPIO & UDB/DSI directly control both the output and output-enable of the output buffer (peripherals can drive strong 0 or strong 1 in any mode except OFF='0'). Note: D_OUT, D_OUT_EN are pins of GPIO cell. Default Value: 0 **0x0: HIGHZ :** Output buffer is off creating a high impedance input D_OUT = '0': High Impedance D_OUT = '1': High Impedance **0x1: RESERVED :** This mode is reserved and should not be used. No damage will occur if this mode is selected. The pin will generally perform the same as the STRONG drive mode although this is not guaranteed for all use cases. For GPIO & UDB/DSI peripherals: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When D_OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance For peripherals other than GPIO & UDB/DSI: When D_OUT_EN = 1: D_OUT = '0': Strong pull down D_OUT = '1': Strong pull up When OUT_EN = 0: D_OUT = '0': High impedance D_OUT = '1': High impedance

16.1.31 GPIO_PRT4_CFG (continued)

0x2: PULLUP :

Resistive pull up
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
 D_OUT = '0': Strong pull down
 D_OUT = '1': Weak/resistive pull up
When D_OUT_EN = 0:
 D_OUT = '0': High impedance
 D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
 D_OUT = '0': Strong pull down
 D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
 D_OUT = '0': Weak/resistive pull up
 D_OUT = '1': Weak/resistive pull up

0x3: PULLDOWN :

Resistive pull down
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
 D_OUT = '0': Weak/resistive pull down
 D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
 D_OUT = '0': High impedance
 D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
 D_OUT = '0': Strong pull down
 D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
 D_OUT = '0': Weak/resistive pull down
 D_OUT = '1': Weak/resistive pull down

0x4: OD_DRIVESLOW :

Open drain, drives low
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
 D_OUT = '0': Strong pull down
 D_OUT = '1': High Impedance
When D_OUT_EN = 0:
 D_OUT = '0': High impedance
 D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
 D_OUT = '0': Strong pull down
 D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
 D_OUT = '0': High Impedance
 D_OUT = '1': High Impedance

16.1.31 GPIO_PRT4_CFG (continued)

0x5: OD_DRIVESHIGH :

Open drain, drives high
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
 D_OUT = '0': High Impedance
 D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
 D_OUT = '0': High impedance
 D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
 D_OUT = '0': Strong pull down
 D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
 D_OUT = '0': High Impedance
 D_OUT = '1': High Impedance

0x6: STRONG :

Strong D_OUTput buffer
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
 D_OUT = '0': Strong pull down
 D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
 D_OUT = '0': High impedance
 D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
 D_OUT = '0': Strong pull down
 D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
 D_OUT = '0': High Impedance
 D_OUT = '1': High Impedance

0x7: PULLUP_DOWN :

Pull up or pull down
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = '0':
 GPIO_DSI_OUT = '0': Weak/resistive pull down
 GPIO_DSI_OUT = '1': Weak/resistive pull up
where "GPIO_DSI_OUT" is a function of PORT_SEL, OUT & DSI_DATA_OUT.
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
 D_OUT = '0': Strong pull down
 D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
 D_OUT = '0': Weak/resistive pull down
 D_OUT = '1': Weak/resistive pull up

16.1.32 GPIO_PRT4_CFG_IN

Port input buffer configuration register

Address: 0x4032022C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [7:4]				VTRIP_-SEL3_0	VTRIP_-SEL2_0	VTRIP_-SEL1_0	VTRIP_-SEL0_0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	VTRIP_SEL3_0	Configures the pin 3 input buffer mode (trip points and hysteresis) Default Value: 0
2	VTRIP_SEL2_0	Configures the pin 2 input buffer mode (trip points and hysteresis) Default Value: 0
1	VTRIP_SEL1_0	Configures the pin 1 input buffer mode (trip points and hysteresis) Default Value: 0
0	VTRIP_SEL0_0	Configures the pin 0 input buffer mode (trip points and hysteresis) Default Value: 0 **0x0: CMOS :** S40E: {CFG_IN_GPIO5V.VTRIP_SEL0_1, CFG_IN.VTRIP_SEL0_0} 0,0: CMOS 0,1: TTL 1,0: input buffer is compatible with automotive. 1,1: input buffer is compatible with automotvie

16.1.32 GPIO_PRT4_CFG_IN (continued)

0x1: TTL :

S40S: Input buffer compatible with TTL and MediaLB interfaces

16.1.33 GPIO_PRT4_CFG_OUT

Port output buffer configuration register

Address: 0x40320230

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [7:4]				SLOW3	SLOW2	SLOW1	SLOW0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	DRIVE_SEL3 [23:22]		DRIVE_SEL2 [21:20]		DRIVE_SEL1 [19:18]		DRIVE_SEL0 [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 22	DRIVE_SEL3	Sets the GPIO drive strength for IO pin 3 Default Value: 0
21 : 20	DRIVE_SEL2	Sets the GPIO drive strength for IO pin 2 Default Value: 0
19 : 18	DRIVE_SEL1	Sets the GPIO drive strength for IO pin 1 Default Value: 0
17 : 16	DRIVE_SEL0	Sets the GPIO drive strength for IO pin 0 Default Value: 0 **0x0: FULL_DRIVE :** Full drive strength: GPIO drives current at its max rated spec. **0x1: ONE_HALF_DRIVE :** 1/2 drive strength: GPIO drives current at 1/2 of its max rated spec

16.1.33 GPIO_PRT4_CFG_OUT (continued)

		0x2: ONE_QUARTER_DRIVE : 1/4 drive strength: GPIO drives current at 1/4 of its max rated spec. **0x3: ONE_EIGHTH_DRIVE :** 1/8 drive strength: GPIO drives current at 1/8 of its max rated spec.
3	SLOW3	Enables slow slew rate for IO pin 3 Default Value: 0
2	SLOW2	Enables slow slew rate for IO pin 2 Default Value: 0
1	SLOW1	Enables slow slew rate for IO pin 1 Default Value: 0
0	SLOW0	Enables slow slew rate for IO pin 0 '0': Fast slew rate '1': Slow slew rate Default Value: 0

16.1.34 GPIO_PRT14_OUT

Port output data register

Address: 0x40320700

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						RW	RW
Name	None [7:2]						OUT1	OUT0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	OUT1	IO output data for pin 1 Default Value: 0
0	OUT0	IO output data for pin 0 '0': Output state set to '0' '1': Output state set to '1' Default Value: 0

16.1.35 GPIO_PRT14_IN

Port input state register

Address: 0x40320710

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						W	W
Name	None [7:2]						IN1	IN0

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							FLT_IN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_IN	Reads of this register return the logical state of the filtered pin as selected in the INTR_CFG.FLT_SEL register. Default Value: 0
1	IN1	IO pin state for pin 1 Default Value: 0
0	IN0	IO pin state for pin 0 '0': Low logic level present on pin. '1': High logic level present on pin. Default Value: 0

16.1.36 GPIO_PRT14_INTR

Port interrupt status register

Address: 0x40320714

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1C	RW1C
HW Access	None						A	A
Name	None [7:2]						EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1C
HW Access	None							A
Name	None [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	None						R	R
HW Access	None						W	W
Name	None [23:18]						IN_IN1	IN_IN0

Bits	31	30	29	28	27	26	25	24
SW Access	None							R
HW Access	None							W
Name	None [31:25]							FLT_IN_IN

Bits	Name	Description
24	FLT_IN_IN	Filtered pin state for pin selected by INTR_CFG.FLT_SEL Default Value: 0
17	IN_IN1	IO pin state for pin 1 Default Value: 0
16	IN_IN0	IO pin state for pin 0 Default Value: 0
8	FLT_EDGE	Edge detected on filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
1	EDGE1	Edge detect for IO pin 1 Default Value: 0
0	EDGE0	Edge detect for IO pin 0 '0': No edge was detected on pin. '1': An edge was detected on pin. Default Value: 0

16.1.37 GPIO_PRT14_INTR_MASK

Port interrupt mask register

Address: 0x40320718

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_EDGE	Masks edge interrupt on filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
1	EDGE1	Masks edge interrupt on IO pin 1 Default Value: 0
0	EDGE0	Masks edge interrupt on IO pin 0 '0': Pin interrupt forwarding disabled '1': Pin interrupt forwarding enabled Default Value: 0

16.1.38 GPIO_PRT14_INTR_MASKED

Port interrupt masked status register

Address: 0x4032071C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						W	W
Name	None [7:2]						EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_EDGE	Edge detected and masked on filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
1	EDGE1	Edge detected and masked on IO pin 1 Default Value: 0
0	EDGE0	Edge detected AND masked on IO pin 0 '0': Interrupt was not forwarded to CPU '1': Interrupt occurred and was forwarded to CPU Default Value: 0

16.1.39 GPIO_PRT14_INTR_SET

Port interrupt set register

Address: 0x40320720

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1S	RW1S
HW Access	None						A	A
Name	None [7:2]						EDGE1	EDGE0

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1S
HW Access	None							A
Name	None [15:9]							FLT_EDGE

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_EDGE	Sets edge detect interrupt for filtered pin selected by INTR_CFG.FLT_SEL Default Value: 0
1	EDGE1	Sets edge detect interrupt for IO pin 1 Default Value: 0
0	EDGE0	Sets edge detect interrupt for IO pin 0 '0': Interrupt state not affected '1': Interrupt set Default Value: 0

16.1.40 GPIO_PRT14_INTR_CFG

Port interrupt configuration register

Address: 0x40320724

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW		RW	
HW Access	None				R		R	
Name	None [7:4]				EDGE1_SEL [3:2]		EDGE0_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW			RW	
HW Access	None			R			R	
Name	None [23:21]			FLT_SEL [20:18]			FLT_EDGE_SEL [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
20 : 18	FLT_SEL	Selects which pin is routed through the 50ns glitch filter to provide a glitch-safe interrupt. Default Value: 0
17 : 16	FLT_EDGE_SEL	Sets which edge will trigger an IRQ for the glitch filtered pin (selected by INTR_CFG.FLT_SEL Default Value: 0 **0x0: DISABLE :** Disabled **0x1: RISING :** Rising edge **0x2: FALLING :** Falling edge

16.1.40 GPIO_PRT14_INTR_CFG (continued)

		0x3: BOTH : Both rising and falling edges
3 : 2	EDGE1_SEL	Sets which edge will trigger an IRQ for IO pin 1 Default Value: 0
1 : 0	EDGE0_SEL	Sets which edge will trigger an IRQ for IO pin 0 Default Value: 0 **0x0: DISABLE :** Disabled **0x1: RISING :** Rising edge **0x2: FALLING :** Falling edge **0x3: BOTH :** Both rising and falling edges

16.1.41 GPIO_PRT14_CFG

Port configuration register

Address: 0x40320728

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW			RW	RW		
HW Access	R	R			R	R		
Name	IN_EN1	DRIVE_MODE1 [6:4]			IN_EN0	DRIVE_MODE0 [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	IN_EN1	Enables the input buffer for IO pin 1 Default Value: 0
6 : 4	DRIVE_MODE1	The GPIO drive mode for IO pin 1 Default Value: 0
3	IN_EN0	Enables the input buffer for IO pin 0. This bit should be cleared when analog signals are present on the pin to avoid crowbar currents. The output buffer can be used to drive analog signals high or low without issue. '0': Input buffer disabled '1': Input buffer enabled Default Value: 0
2 : 0	DRIVE_MODE0	The GPIO drive mode for IO pin 0. Resistive pull-up and pull-down is selected in the drive mode. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the peripheral and HSIOM (HSIOM_PRT_SELx) is properly configured before turning the IO on here to avoid producing glitches on the bus. Note: that peripherals other than GPIO & UDB/DSI directly control both the output and output-enable of the output buffer (peripherals can drive strong 0 or strong 1 in any mode except OFF='0'). Note: D_OUT, D_OUT_EN are pins of GPIO cell. Default Value: 0

16.1.41 GPIO_PRT14_CFG (continued)

0x0: HIGHZ :

Output buffer is off creating a high impedance input
D_OUT = '0': High Impedance
D_OUT = '1': High Impedance

0x1: RESERVED :

This mode is reserved and should not be used. No damage will occur if this mode is selected. The pin will generally perform the same as the STRONG drive mode although this is not guaranteed for all use cases.
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
 D_OUT = '0': Strong pull down
 D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
 D_OUT = '0': High impedance
 D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
 D_OUT = '0': Strong pull down
 D_OUT = '1': Strong pull up
When OUT_EN = 0:
 D_OUT = '0': High impedance
 D_OUT = '1': High impedance

0x2: PULLUP :

Resistive pull up
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
 D_OUT = '0': Strong pull down
 D_OUT = '1': Weak/resistive pull up
When D_OUT_EN = 0:
 D_OUT = '0': High impedance
 D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
 D_OUT = '0': Strong pull down
 D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
 D_OUT = '0': Weak/resistive pull up
 D_OUT = '1': Weak/resistive pull up

16.1.41 GPIO_PRT14_CFG (continued)

0x3: PULLDOWN :

Resistive pull down
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
 D_OUT = '0': Weak/resistive pull down
 D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
 D_OUT = '0': High impedance
 D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
 D_OUT = '0': Strong pull down
 D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
 D_OUT = '0': Weak/resistive pull down
 D_OUT = '1': Weak/resistive pull down

0x4: OD_DRIVESLOW :

Open drain, drives low
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
 D_OUT = '0': Strong pull down
 D_OUT = '1': High Impedance
When D_OUT_EN = 0:
 D_OUT = '0': High impedance
 D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
 D_OUT = '0': Strong pull down
 D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
 D_OUT = '0': High Impedance
 D_OUT = '1': High Impedance

0x5: OD_DRIVESHIGH :

Open drain, drives high
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
 D_OUT = '0': High Impedance
 D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
 D_OUT = '0': High impedance
 D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
 D_OUT = '0': Strong pull down
 D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
 D_OUT = '0': High Impedance
 D_OUT = '1': High Impedance

16.1.41 GPIO_PRT14_CFG (continued)

0x6: STRONG :

Strong D_OUTput buffer
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = 1:
 D_OUT = '0': Strong pull down
 D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
 D_OUT = '0': High impedance
 D_OUT = '1': High impedance
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
 D_OUT = '0': Strong pull down
 D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
 D_OUT = '0': High Impedance
 D_OUT = '1': High Impedance

0x7: PULLUP_DOWN :

Pull up or pull down
For GPIO & UDB/DSI peripherals:
When D_OUT_EN = '0':
 GPIO_DSI_OUT = '0': Weak/resistive pull down
 GPIO_DSI_OUT = '1': Weak/resistive pull up
where "GPIO_DSI_OUT" is a function of PORT_SEL, OUT & DSI_DATA_OUT.
For peripherals other than GPIO & UDB/DSI:
When D_OUT_EN = 1:
 D_OUT = '0': Strong pull down
 D_OUT = '1': Strong pull up
When D_OUT_EN = 0:
 D_OUT = '0': Weak/resistive pull down
 D_OUT = '1': Weak/resistive pull up

16.1.42 GPIO_INTR_CAUSE0

Interrupt port cause register 0

Address: 0x40324000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	PORT_INT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None	R						
HW Access	None	W						
Name	None	PORT_INT [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
14 : 0	PORT_INT	Each IO port has an associated bit field in this register. The bit field reflects the IO port's interrupt line (bit field i reflects "gpio_interrupts[i]" for IO port i). The register is used when the system uses a combined interrupt line "gpio_interrupt". The software ISR reads the register to determine which IO port(s) is responsible for the combined interrupt line. Once, the IO port(s) is determined, the IO port's GPIO_PRT_INTR register is read to determine the IO pin(s) in the IO port that caused the interrupt. '0': Port has no pending interrupt '1': Port has pending interrupt Default Value: 0

16.1.43 GPIO_VDD_ACTIVE

Extern power supply detection register

Address: 0x40324010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R					
HW Access	None		W					
Name	None [7:6]		VDDIO_ACTIVE [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	None					
HW Access	W	W	None					
Name	VDDD_ACTIVE	VDDA_ACTIVE	None [29:24]					

Bits	Name	Description
31	VDDD_ACTIVE	This bit indicates presence of the VDDD supply. This bit will always read-back 1. The VDDD supply has robust brown-out protection monitoring and it is not possible to read back this register without a valid supply. (This bit is used in certain test-modes to observe the brown-out detector status.) Default Value: 0
30	VDDA_ACTIVE	Same as VDDIO_ACTIVE for the analog supply VDDA. Default Value: 0

16.1.43 GPIO_VDD_ACTIVE (continued)

5 : 0	VDDIO_ACTIVE	Indicates presence or absence of VDDIO supplies (i.e. other than VDDD, VDDA) on the device (supplies are numbered 0..n-1). Note that VDDIO supplies have basic (crude) supply detectors only. If separate, robust, brown-out detection is desired on IO supplies, on-chip or off-chip analog resources need to provide it. For these bits to work reliable, the supply must be within valid spec range (per datasheet) or held at ground. Any in-between voltage has an undefined result. '0': Supply is not present '1': Supply is present When multiple VDDIO supplies are present, they will be assigned in alphanumeric ascending order to these bits during implementation. For example "vddusb, vddio_0, vddio_a, vbackup, vddio_r, vddio_1" are present then they will be assigned to these bits as below: 0: vbackup, 1: vddio_0, 2: vddio_1, 3: vddio_a, 4: vddio_r, 5: vddusb" Default Value: 0

16.1.44 GPIO_VDD_INTR

Supply detection interrupt register

Address: 0x40324014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW1C					
HW Access	None		A					
Name	None [7:6]		VDDIO_ACTIVE [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1C	RW1C	None					
HW Access	A	A	None					
Name	VDDD_ACTIVE	VDDA_ACTIVE	None [29:24]					

Bits	Name	Description
31	VDDD_ACTIVE	The VDDD supply is always present during operation so a supply transition can not occur. This bit will always read back '1'. Default Value: 0
30	VDDA_ACTIVE	Same as VDDIO_ACTIVE for the analog supply VDDA. Default Value: 0
5 : 0	VDDIO_ACTIVE	Supply state change detected. '0': No change to supply detected '1': Change to supply detected Default Value: 0

16.1.45 GPIO_VDD_INTR_MASK

Supply detection interrupt mask register

Address: 0x40324018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		VDDIO_ACTIVE [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None					
HW Access	R	R	None					
Name	VDDD_AC-TIVE	VDDA_AC-TIVE	None [29:24]					

Bits	Name	Description
31	VDDD_ACTIVE	Same as VDDIO_ACTIVE for the digital supply VDDD. Default Value: 0
30	VDDA_ACTIVE	Same as VDDIO_ACTIVE for the analog supply VDDA. Default Value: 0
5 : 0	VDDIO_ACTIVE	Masks supply interrupt on VDDIO. '0': VDDIO interrupt forwarding disabled '1': VDDIO interrupt forwarding enabled Default Value: 0

16.1.46 GPIO_VDD_INTR_MASKED

Supply detection interrupt masked register

Address: 0x4032401C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R					
HW Access	None		W					
Name	None [7:6]		VDDIO_ACTIVE [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	None					
HW Access	W	W	None					
Name	VDDD_ACTIVE	VDDA_ACTIVE	None [29:24]					

Bits	Name	Description
31	VDDD_ACTIVE	Same as VDDIO_ACTIVE for the digital supply VDDD. Default Value: 0
30	VDDA_ACTIVE	Same as VDDIO_ACTIVE for the analog supply VDDA. Default Value: 0
5 : 0	VDDIO_ACTIVE	Supply transition detected AND masked '0': Interrupt was not forwarded to CPU '1': Interrupt occurred and was forwarded to CPU Default Value: 0

16.1.47 GPIO_VDD_INTR_SET

Supply detection interrupt set register

Address: 0x40324020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW1S					
HW Access	None		A					
Name	None [7:6]		VDDIO_ACTIVE [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1S	RW1S	None					
HW Access	A	A	None					
Name	VDDD_AC-TIVE	VDDA_AC-TIVE	None [29:24]					

Bits	Name	Description
31	VDDD_ACTIVE	Same as VDDIO_ACTIVE for the digital supply VDDD. Default Value: 0
30	VDDA_ACTIVE	Same as VDDIO_ACTIVE for the analog supply VDDA. Default Value: 0
5 : 0	VDDIO_ACTIVE	Sets supply interrupt. '0': Interrupt state not affected '1': Interrupt set Default Value: 0

17 Smart I/O Registers

This section discusses the Smart I/O registers. It lists all the registers in mapping tables, in address order.

17.1 Register Details

Register	Address	Description
SMARTIO_PRT8_CTL	0x40330800	Control register
SMARTIO_PRT8_SYNC_CTL	0x40330810	Synchronization control register
SMARTIO_PRT8_LUT_SEL0	0x40330820	LUT component input selection
SMARTIO_PRT8_LUT_SEL1	0x40330824	LUT component input selection. See SMARTIO_PRT8_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT8_LUT_SEL2	0x40330828	LUT component input selection. See SMARTIO_PRT8_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT8_LUT_SEL3	0x4033082C	LUT component input selection. See SMARTIO_PRT8_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT8_LUT_SEL4	0x40330830	LUT component input selection. See SMARTIO_PRT8_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT8_LUT_SEL5	0x40330834	LUT component input selection. See SMARTIO_PRT8_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT8_LUT_SEL6	0x40330838	LUT component input selection. See SMARTIO_PRT8_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT8_LUT_SEL7	0x4033083C	LUT component input selection. See SMARTIO_PRT8_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT8_LUT_CTL0	0x40330840	LUT component control register
SMARTIO_PRT8_LUT_CTL1	0x40330844	LUT component control register. See SMARTIO_PRT8_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT8_LUT_CTL2	0x40330848	LUT component control register. See SMARTIO_PRT8_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT8_LUT_CTL3	0x4033084C	LUT component control register. See SMARTIO_PRT8_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT8_LUT_CTL4	0x40330850	LUT component control register. See SMARTIO_PRT8_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT8_LUT_CTL5	0x40330854	LUT component control register. See SMARTIO_PRT8_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT8_LUT_CTL6	0x40330858	LUT component control register. See SMARTIO_PRT8_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT8_LUT_CTL7	0x4033085C	LUT component control register. See SMARTIO_PRT8_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT8_DU_SEL	0x403308C0	Data unit component input selection
SMARTIO_PRT8_DU_CTL	0x403308C4	Data unit component control register
SMARTIO_PRT8_DATA	0x403308F0	Data register
SMARTIO_PRT9_CTL	0x40330900	Control register. See SMARTIO_PRT8_CTL for the details of bit fields.
SMARTIO_PRT9_SYNC_CTL	0x40330910	Synchronization control register. See SMARTIO_PRT8_SYNC_CTL for the details of bit fields.
SMARTIO_PRT9_LUT_SEL0	0x40330920	LUT component input selection. See SMARTIO_PRT8_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT9_LUT_SEL1	0x40330924	LUT component input selection. See SMARTIO_PRT8_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT9_LUT_SEL2	0x40330928	LUT component input selection. See SMARTIO_PRT8_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT9_LUT_SEL3	0x4033092C	LUT component input selection. See SMARTIO_PRT8_LUT_SEL0 for the details of bit fields.

Register	Address	Description
SMARTIO_PRT9_LUT_SEL4	0x40330930	LUT component input selection. See SMARTIO_PRT8_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT9_LUT_SEL5	0x40330934	LUT component input selection. See SMARTIO_PRT8_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT9_LUT_SEL6	0x40330938	LUT component input selection. See SMARTIO_PRT8_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT9_LUT_SEL7	0x4033093C	LUT component input selection. See SMARTIO_PRT8_LUT_SEL0 for the details of bit fields.
SMARTIO_PRT9_LUT_CTL0	0x40330940	LUT component control register. See SMARTIO_PRT8_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT9_LUT_CTL1	0x40330944	LUT component control register. See SMARTIO_PRT8_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT9_LUT_CTL2	0x40330948	LUT component control register. See SMARTIO_PRT8_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT9_LUT_CTL3	0x4033094C	LUT component control register. See SMARTIO_PRT8_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT9_LUT_CTL4	0x40330950	LUT component control register. See SMARTIO_PRT8_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT9_LUT_CTL5	0x40330954	LUT component control register. See SMARTIO_PRT8_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT9_LUT_CTL6	0x40330958	LUT component control register. See SMARTIO_PRT8_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT9_LUT_CTL7	0x4033095C	LUT component control register. See SMARTIO_PRT8_LUT_CTL0 for the details of bit fields.
SMARTIO_PRT9_DU_SEL	0x403309C0	Data unit component input selection. See SMARTIO_PRT8_DU_SEL for the details of bit fields.
SMARTIO_PRT9_DU_CTL	0x403309C4	Data unit component control register. See SMARTIO_PRT8_DU_CTL for the details of bit fields.
SMARTIO_PRT9_DATA	0x403309F0	Data register. See SMARTIO_PRT8_DATA for the details of bit fields.

17.1.1 SMARTIO_PRT8_CTL

Control register

Address: 0x40330800

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	BYPASS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW				
HW Access	None			R				
Name	None [15:13]			CLOCK_SRC [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None					RW	RW
HW Access	R	None					R	R
Name	ENABLED	None [30:26]					PIPE-LINE_EN	HLD_OVR

Bits	Name	Description
31	ENABLED	Enable for programmable IO. Should only be set to '1' when the programmable IO is completely configured: '0': Disabled (signals are bypassed; behavior as if BYPASS is 0xFF). When disabled, the fabric (data unit and LUTs) reset is activated. If the IP is disabled: - The PIPELINE_EN register field should be set to '1', to ensure low power consumption by preventing combinatorial loops. - The CLOCK_SRC register field should be set to "20"-"30" (clock is constant '0'), to ensure low power consumption. '1': Enabled. Once enabled, it takes 3 "clk_fabric" clock cycles till the fabric reset is de-activated and the fabric becomes fully functional. This ensures that the IO pins' input synchronizer states are flushed when the fabric is fully functional. Default Value: 0
25	PIPELINE_EN	Enable for pipeline register: '0': Disabled (register is bypassed). '1': Enabled. Default Value: 1

17.1.1 SMARTIO_PRT8_CTL (continued)

24	HLD_OVR	IO cell hold override functionality. In DeepSleep power mode, the HSIOM holds the IO cell output and output enable signals if Active functionality is connected to the IO pads. This is undesirable if the SMARTIO is supposed to deliver DeepSleep output functionality on these IO pads. This field is used to control the hold override functionality from the SMARTIO: '0': The HSIOM controls the IO cell hold override functionality ("hsiom_hld_ovr"). '1': The SMARTIO controls the IO cel hold override functionality: - In bypass mode (ENABLED is '0' or BYPASS[i] is '1'), the HSIOM control is used. - In NON bypass mode (ENABLED is '1' and BYPASS[i] is '0'), the SMARTIO sets hold override to "pwr_hld_ovr_hib" to enable SMARTIO functionality in DeepSleep power mode (but disables it in Hibernate or Stop power mode). Default Value: Undefined
12 : 8	CLOCK_SRC	Clock ("clk_fabric") and reset ("rst_fabric_n") source selection: "0": io_data_in[0]/'1'. ... "7": io_data_in[7]/'1'. "8": chip_data[0]/'1'. ... "15": chip_data[7]/'1'. "16": clk_smartio/rst_sys_act_n. Used for both Active functionality synchronous logic on "clk_smartio". This selection is intended for synchronous operation on a PCLK specified clock frequency ("clock_smartio_pos_en"). Note that the fabric's clocked elements are frequency aligned, but NOT phase aligned to "clk_sys". "17": clk_smartio/rst_sys_dpslp_n. Used for both DeepSleep functionality synchronous logic on "clk_smartio" (note that "clk_smartio" is NOT available in DeepSleep and Hibernate power modes). This selection is intended for synchronous operation on a PCLK specified clock frequency ("clock_smartio_pos_en"). Note that the fabric's clocked elements are frequency aligned, but NOT phase aligned to "clk_sys". "18": Same as "17". "19": clk_lf/rst_lf_dpslp_n (note that "clk_lf" is available in DeepSleep power mode). This selection is intended for synchronous operation on"clk_lf". Note that the fabric's clocked elements are frequency aligned, but NOT phase aligned to other "clk_lf" clocked elements. "20"-"30": Clock source is constant '0'. Any of these clock sources should be selected when the IP is disabled to ensure low power consumption. "31": asynchronous mode/'1'. Select this when clockless operation is configured. NOTE: Two positive edges of the selected clock are required for the block to be enabled (to deactivate reset). In asynchronous (clockless) mode clk_sys is used to enable the block, but is not available for clocking. Default Value: 20
7 : 0	BYPASS	Bypass of the programmable IO, one bit for each IO pin: BYPASS[i] is for IO pin i. When ENABLED is '1', this field is used. When ENABLED is '0', this field is NOT used and SMARTIO fabric is always bypassed. '0': No bypass (programmable SMARTIO fabric is exposed). '1': Bypass (programmable SMARTIOIO fabric is hidden). Default Value: Undefined

17.1.2 SMARTIO_PRT8_SYNC_CTL

Synchronization control register

Address: 0x40330810

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	IO_SYNC_EN [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CHIP_SYNC_EN [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 8	CHIP_SYNC_EN	Synchronization of the chip input signals to "clk_fabric", one bit for each input: CHIP_SYNC_EN[i] is for input i. '0': No synchronization. '1': Synchronization. Default Value: Undefined
7 : 0	IO_SYNC_EN	Synchronization of the IO pin input signals to "clk_fabric", one bit for each IO pin: IO_SYNC_EN[i] is for IO pin i. '0': No synchronization. '1': Synchronization. Default Value: Undefined

17.1.3 SMARTIO_PRT8_LUT_SEL0

LUT component input selection

Address: 0x40330820

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				LUT_TR0_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				LUT_TR1_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				LUT_TR2_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	LUT_TR2_SEL	LUT input signal "tr2_in" source selection. Encoding is the same as for LUT_TR1_SEL. Default Value: Undefined
11 : 8	LUT_TR1_SEL	LUT input signal "tr1_in" source selection: "0": LUT 0 output. "1": LUT 1 output. "2": LUT 2 output. "3": LUT 3 output. "4": LUT 4 output. "5": LUT 5 output. "6": LUT 6 output. "7": LUT 7 output. "8": chip_data[0] (for LUTs 0, 1, 2, 3); chip_data[4] (for LUTs 4, 5, 6, 7). "9": chip_data[1] (for LUTs 0, 1, 2, 3); chip_data[5] (for LUTs 4, 5, 6, 7). "10": chip_data[2] (for LUTs 0, 1, 2, 3); chip_data[6] (for LUTs 4, 5, 6, 7). "11": chip_data[3] (for LUTs 0, 1, 2, 3); chip_data[7] (for LUTs 4, 5, 6, 7). "12": io_data_in[0] (for LUTs 0, 1, 2, 3); io_data_in[4] (for LUTs 4, 5, 6, 7). "13": io_data_in[1] (for LUTs 0, 1, 2, 3); io_data_in[5] (for LUTs 4, 5, 6, 7). "14": io_data_in[2] (for LUTs 0, 1, 2, 3); io_data_in[6] (for LUTs 4, 5, 6, 7). "15": io_data_in[3] (for LUTs 0, 1, 2, 3); io_data_in[7] (for LUTs 4, 5, 6, 7). Default Value: Undefined

17.1.3 SMARTIO_PRT8_LUT_SEL0 (continued)

3 : 0	LUT_TR0_SEL	LUT input signal "tr0_in" source selection: "0": Data unit output. "1": LUT 1 output. "2": LUT 2 output. "3": LUT 3 output. "4": LUT 4 output. "5": LUT 5 output. "6": LUT 6 output. "7": LUT 7 output. "8": chip_data[0] (for LUTs 0, 1, 2, 3); chip_data[4] (for LUTs 4, 5, 6, 7). "9": chip_data[1] (for LUTs 0, 1, 2, 3); chip_data[5] (for LUTs 4, 5, 6, 7). "10": chip_data[2] (for LUTs 0, 1, 2, 3); chip_data[6] (for LUTs 4, 5, 6, 7). "11": chip_data[3] (for LUTs 0, 1, 2, 3); chip_data[7] (for LUTs 4, 5, 6, 7). "12": io_data_in[0] (for LUTs 0, 1, 2, 3); io_data_in[4] (for LUTs 4, 5, 6, 7). "13": io_data_in[1] (for LUTs 0, 1, 2, 3); io_data_in[5] (for LUTs 4, 5, 6, 7). "14": io_data_in[2] (for LUTs 0, 1, 2, 3); io_data_in[6] (for LUTs 4, 5, 6, 7). "15": io_data_in[3] (for LUTs 0, 1, 2, 3); io_data_in[7] (for LUTs 4, 5, 6, 7). Default Value: Undefined

17.1.4 SMARTIO_PRT8_LUT_CTL0

LUT component control register

Address: 0x40330840

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	LUT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						LUT_OPC [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 8	LUT_OPC	LUT opcode specifies the LUT operation: "0": Combinatoral output, no feedback. tr_out = LUT[{tr2_in, tr1_in, tr0_in}]. "1": Combinatorial output, feedback. tr_out = LUT[{lut_reg, tr1_in, tr0_in}]. On clock: lut_reg <= tr_in2. "2": Sequential output, no feedback. temp = LUT[{tr2_in, tr1_in, tr0_in}]. tr_out = lut_reg. On clock: lut_reg <= temp. "3": Register with asynchronous set and reset. tr_out = lut_reg. enable = (tr2_in ^ LUT[4]) | LUT[5]. set = enable & (tr1_in ^ LUT[2]) & LUT[3]. clr = enable & (tr0_in ^ LUT[0]) & LUT[1]. Asynchronously (no clock required): lut_reg <= if (clr) '0' else if (set) '1' Default Value: Undefined

17.1.4 SMARTIO_PRT8_LUT_CTL0 (continued)

7 : 0	LUT	LUT configuration. Depending on the LUT opcode LUT_OPC, the internal state lut_reg (captured in a flip-flop) and the LUT input signals tr0_in, tr1_in, tr2_in, the LUT configuration is used to determine the LUT output signal and the next sequential state (lut_reg). Default Value: Undefined

17.1.5 SMARTIO_PRT8_DU_SEL

Data unit component input selection

Address: 0x403308C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				DU_TR0_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				DU_TR1_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				DU_TR2_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None		RW		None		RW	
HW Access	None		R		None		R	
Name	None [31:30]		DU_DATA1_SEL [29:28]		None [27:26]		DU_DATA0_SEL [25:24]	

Bits	Name	Description
29 : 28	DU_DATA1_SEL	Data unit input data "data1_in" source selection. Encoding is the same as for DU_DATA0_SEL. Default Value: Undefined
25 : 24	DU_DATA0_SEL	Data unit input data "data0_in" source selection: "0": Constant "0". "1": chip_data[7:0]. "2": io_data_in[7:0]. "3": DATA.DATA MMIO register field. Default Value: Undefined
19 : 16	DU_TR2_SEL	Data unit input signal "tr2_in" source selection. Encoding is the same as for DU_TR0_SEL. Default Value: Undefined
11 : 8	DU_TR1_SEL	Data unit input signal "tr1_in" source selection. Encoding is the same as for DU_TR0_SEL. Default Value: Undefined

17.1.5 SMARTIO_PRT8_DU_SEL (continued)

3 : 0	DU_TR0_SEL	Data unit input signal "tr0_in" source selection: "0": Constant '0'. "1": Constant '1'. "2": Data unit output. "10-3": LUT 7 - 0 outputs. Otherwise: Undefined. Default Value: Undefined

17.1.6 SMARTIO_PRT8_DU_CTL

Data unit component control register

Address: 0x403308C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW		
HW Access	None					R		
Name	None [7:3]					DU_SIZE [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				DU_OPC [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11 : 8	DU_OPC	Data unit opcode specifies the data unit operation: "1": INCR "2": DECR "3": INCR_WRAP "4": DECR_WRAP "5": INCR_DECR "6": INCR_DECR_WRAP "7": ROR "8": SHR "9": AND_OR "10": SHR_MAJ3 "11": SHR_EQL. Otherwise: Undefined. Default Value: Undefined
2 : 0	DU_SIZE	Size/width of the data unit data operands (in bits) is DU_SIZE+1. E.g., if DU_SIZE is 7, the width is 8 bits. Default Value: Undefined

17.1.7 SMARTIO_PRT8_DATA

Data register

Address: 0x403308F0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	Data unit input data source. Default Value: Undefined

18 Universal Digital Block (UDB) Registers

This section discusses the Universal Digital Block (UDB) registers. It lists all the registers in mapping tables, in address order.

18.1 Register Details

Register	Address	Description
UDB_WRKONE_A0	0x40340000	Accumulator Registers {A1,A0}
UDB_WRKONE_A1	0x40340004	Accumulator Registers {A1,A0}. See UDB_WRKONE_A0 for the details of bit fields.
UDB_WRKONE_A2	0x40340008	Accumulator Registers {A1,A0}. See UDB_WRKONE_A0 for the details of bit fields.
UDB_WRKONE_A3	0x4034000C	Accumulator Registers {A1,A0}. See UDB_WRKONE_A0 for the details of bit fields.
UDB_WRKONE_A4	0x40340010	Accumulator Registers {A1,A0}. See UDB_WRKONE_A0 for the details of bit fields.
UDB_WRKONE_A5	0x40340014	Accumulator Registers {A1,A0}. See UDB_WRKONE_A0 for the details of bit fields.
UDB_WRKONE_A6	0x40340018	Accumulator Registers {A1,A0}. See UDB_WRKONE_A0 for the details of bit fields.
UDB_WRKONE_A7	0x4034001C	Accumulator Registers {A1,A0}. See UDB_WRKONE_A0 for the details of bit fields.
UDB_WRKONE_A8	0x40340020	Accumulator Registers {A1,A0}. See UDB_WRKONE_A0 for the details of bit fields.
UDB_WRKONE_A9	0x40340024	Accumulator Registers {A1,A0}. See UDB_WRKONE_A0 for the details of bit fields.
UDB_WRKONE_A10	0x40340028	Accumulator Registers {A1,A0}. See UDB_WRKONE_A0 for the details of bit fields.
UDB_WRKONE_A11	0x4034002C	Accumulator Registers {A1,A0}. See UDB_WRKONE_A0 for the details of bit fields.
UDB_WRKONE_D0	0x40340100	Data Registers {D1,D0}
UDB_WRKONE_D1	0x40340104	Data Registers {D1,D0}. See UDB_WRKONE_D0 for the details of bit fields.
UDB_WRKONE_D2	0x40340108	Data Registers {D1,D0}. See UDB_WRKONE_D0 for the details of bit fields.
UDB_WRKONE_D3	0x4034010C	Data Registers {D1,D0}. See UDB_WRKONE_D0 for the details of bit fields.
UDB_WRKONE_D4	0x40340110	Data Registers {D1,D0}. See UDB_WRKONE_D0 for the details of bit fields.
UDB_WRKONE_D5	0x40340114	Data Registers {D1,D0}. See UDB_WRKONE_D0 for the details of bit fields.
UDB_WRKONE_D6	0x40340118	Data Registers {D1,D0}. See UDB_WRKONE_D0 for the details of bit fields.

Register	Address	Description
UDB_WRKONE_D7	0x4034011C	Data Registers {D1,D0}. See UDB_WRKONE_D0 for the details of bit fields.
UDB_WRKONE_D8	0x40340120	Data Registers {D1,D0}. See UDB_WRKONE_D0 for the details of bit fields.
UDB_WRKONE_D9	0x40340124	Data Registers {D1,D0}. See UDB_WRKONE_D0 for the details of bit fields.
UDB_WRKONE_D10	0x40340128	Data Registers {D1,D0}. See UDB_WRKONE_D0 for the details of bit fields.
UDB_WRKONE_D11	0x4034012C	Data Registers {D1,D0}. See UDB_WRKONE_D0 for the details of bit fields.
UDB_WRKONE_F0	0x40340200	FIFOs {F1,F0}
UDB_WRKONE_F1	0x40340204	FIFOs {F1,F0}. See UDB_WRKONE_F0 for the details of bit fields.
UDB_WRKONE_F2	0x40340208	FIFOs {F1,F0}. See UDB_WRKONE_F0 for the details of bit fields.
UDB_WRKONE_F3	0x4034020C	FIFOs {F1,F0}. See UDB_WRKONE_F0 for the details of bit fields.
UDB_WRKONE_F4	0x40340210	FIFOs {F1,F0}. See UDB_WRKONE_F0 for the details of bit fields.
UDB_WRKONE_F5	0x40340214	FIFOs {F1,F0}. See UDB_WRKONE_F0 for the details of bit fields.
UDB_WRKONE_F6	0x40340218	FIFOs {F1,F0}. See UDB_WRKONE_F0 for the details of bit fields.
UDB_WRKONE_F7	0x4034021C	FIFOs {F1,F0}. See UDB_WRKONE_F0 for the details of bit fields.
UDB_WRKONE_F8	0x40340220	FIFOs {F1,F0}. See UDB_WRKONE_F0 for the details of bit fields.
UDB_WRKONE_F9	0x40340224	FIFOs {F1,F0}. See UDB_WRKONE_F0 for the details of bit fields.
UDB_WRKONE_F10	0x40340228	FIFOs {F1,F0}. See UDB_WRKONE_F0 for the details of bit fields.
UDB_WRKONE_F11	0x4034022C	FIFOs {F1,F0}. See UDB_WRKONE_F0 for the details of bit fields.
UDB_WRKONE_CTL_ST0	0x40340300	Status and Control Registers {CTL,ST}
UDB_WRKONE_CTL_ST1	0x40340304	Status and Control Registers {CTL,ST}. See UDB_WRKONE_CTL_ST0 for the details of bit fields.
UDB_WRKONE_CTL_ST2	0x40340308	Status and Control Registers {CTL,ST}. See UDB_WRKONE_CTL_ST0 for the details of bit fields.
UDB_WRKONE_CTL_ST3	0x4034030C	Status and Control Registers {CTL,ST}. See UDB_WRKONE_CTL_ST0 for the details of bit fields.
UDB_WRKONE_CTL_ST4	0x40340310	Status and Control Registers {CTL,ST}. See UDB_WRKONE_CTL_ST0 for the details of bit fields.
UDB_WRKONE_CTL_ST5	0x40340314	Status and Control Registers {CTL,ST}. See UDB_WRKONE_CTL_ST0 for the details of bit fields.
UDB_WRKONE_CTL_ST6	0x40340318	Status and Control Registers {CTL,ST}. See UDB_WRKONE_CTL_ST0 for the details of bit fields.
UDB_WRKONE_CTL_ST7	0x4034031C	Status and Control Registers {CTL,ST}. See UDB_WRKONE_CTL_ST0 for the details of bit fields.
UDB_WRKONE_CTL_ST8	0x40340320	Status and Control Registers {CTL,ST}. See UDB_WRKONE_CTL_ST0 for the details of bit fields.
UDB_WRKONE_CTL_ST9	0x40340324	Status and Control Registers {CTL,ST}. See UDB_WRKONE_CTL_ST0 for the details of bit fields.
UDB_WRKONE_CTL_ST10	0x40340328	Status and Control Registers {CTL,ST}. See UDB_WRKONE_CTL_ST0 for the details of bit fields.
UDB_WRKONE_CTL_ST11	0x4034032C	Status and Control Registers {CTL,ST}. See UDB_WRKONE_CTL_ST0 for the details of bit fields.

Register	Address	Description
UDB_WRKONE_ACTL_MSK0	0x40340400	Mask and Auxiliary Control Registers {ACTL,MSK}
UDB_WRKONE_ACTL_MSK1	0x40340404	Mask and Auxiliary Control Registers {ACTL,MSK}. See UDB_WRKONE_ACTL_MSK0 for the details of bit fields.
UDB_WRKONE_ACTL_MSK2	0x40340408	Mask and Auxiliary Control Registers {ACTL,MSK}. See UDB_WRKONE_ACTL_MSK0 for the details of bit fields.
UDB_WRKONE_ACTL_MSK3	0x4034040C	Mask and Auxiliary Control Registers {ACTL,MSK}. See UDB_WRKONE_ACTL_MSK0 for the details of bit fields.
UDB_WRKONE_ACTL_MSK4	0x40340410	Mask and Auxiliary Control Registers {ACTL,MSK}. See UDB_WRKONE_ACTL_MSK0 for the details of bit fields.
UDB_WRKONE_ACTL_MSK5	0x40340414	Mask and Auxiliary Control Registers {ACTL,MSK}. See UDB_WRKONE_ACTL_MSK0 for the details of bit fields.
UDB_WRKONE_ACTL_MSK6	0x40340418	Mask and Auxiliary Control Registers {ACTL,MSK}. See UDB_WRKONE_ACTL_MSK0 for the details of bit fields.
UDB_WRKONE_ACTL_MSK7	0x4034041C	Mask and Auxiliary Control Registers {ACTL,MSK}. See UDB_WRKONE_ACTL_MSK0 for the details of bit fields.
UDB_WRKONE_ACTL_MSK8	0x40340420	Mask and Auxiliary Control Registers {ACTL,MSK}. See UDB_WRKONE_ACTL_MSK0 for the details of bit fields.
UDB_WRKONE_ACTL_MSK9	0x40340424	Mask and Auxiliary Control Registers {ACTL,MSK}. See UDB_WRKONE_ACTL_MSK0 for the details of bit fields.
UDB_WRKONE_ACTL_MSK10	0x40340428	Mask and Auxiliary Control Registers {ACTL,MSK}. See UDB_WRKONE_ACTL_MSK0 for the details of bit fields.
UDB_WRKONE_ACTL_MSK11	0x4034042C	Mask and Auxiliary Control Registers {ACTL,MSK}. See UDB_WRKONE_ACTL_MSK0 for the details of bit fields.
UDB_WRKONE_MC0	0x40340500	PLD Macrocell Read Registers {00,MC}
UDB_WRKONE_MC1	0x40340504	PLD Macrocell Read Registers {00,MC}. See UDB_WRKONE_MC0 for the details of bit fields.
UDB_WRKONE_MC2	0x40340508	PLD Macrocell Read Registers {00,MC}. See UDB_WRKONE_MC0 for the details of bit fields.
UDB_WRKONE_MC3	0x4034050C	PLD Macrocell Read Registers {00,MC}. See UDB_WRKONE_MC0 for the details of bit fields.
UDB_WRKONE_MC4	0x40340510	PLD Macrocell Read Registers {00,MC}. See UDB_WRKONE_MC0 for the details of bit fields.
UDB_WRKONE_MC5	0x40340514	PLD Macrocell Read Registers {00,MC}. See UDB_WRKONE_MC0 for the details of bit fields.
UDB_WRKONE_MC6	0x40340518	PLD Macrocell Read Registers {00,MC}. See UDB_WRKONE_MC0 for the details of bit fields.
UDB_WRKONE_MC7	0x4034051C	PLD Macrocell Read Registers {00,MC}. See UDB_WRKONE_MC0 for the details of bit fields.
UDB_WRKONE_MC8	0x40340520	PLD Macrocell Read Registers {00,MC}. See UDB_WRKONE_MC0 for the details of bit fields.
UDB_WRKONE_MC9	0x40340524	PLD Macrocell Read Registers {00,MC}. See UDB_WRKONE_MC0 for the details of bit fields.
UDB_WRKONE_MC10	0x40340528	PLD Macrocell Read Registers {00,MC}. See UDB_WRKONE_MC0 for the details of bit fields.
UDB_WRKONE_MC11	0x4034052C	PLD Macrocell Read Registers {00,MC}. See UDB_WRKONE_MC0 for the details of bit fields.
UDB_WRKMULT_A00	0x40341000	Accumulator 0
UDB_WRKMULT_A01	0x40341004	Accumulator 0. See UDB_WRKMULT_A00 for the details of bit fields.
UDB_WRKMULT_A02	0x40341008	Accumulator 0. See UDB_WRKMULT_A00 for the details of bit fields.
UDB_WRKMULT_A03	0x4034100C	Accumulator 0. See UDB_WRKMULT_A00 for the details of bit fields.
UDB_WRKMULT_A04	0x40341010	Accumulator 0. See UDB_WRKMULT_A00 for the details of bit fields.

Register	Address	Description
UDB_WRKMULT_A05	0x40341014	Accumulator 0. See UDB_WRKMULT_A00 for the details of bit fields.
UDB_WRKMULT_A06	0x40341018	Accumulator 0. See UDB_WRKMULT_A00 for the details of bit fields.
UDB_WRKMULT_A07	0x4034101C	Accumulator 0. See UDB_WRKMULT_A00 for the details of bit fields.
UDB_WRKMULT_A08	0x40341020	Accumulator 0. See UDB_WRKMULT_A00 for the details of bit fields.
UDB_WRKMULT_A09	0x40341024	Accumulator 0. See UDB_WRKMULT_A00 for the details of bit fields.
UDB_WRKMULT_A010	0x40341028	Accumulator 0. See UDB_WRKMULT_A00 for the details of bit fields.
UDB_WRKMULT_A011	0x4034102C	Accumulator 0. See UDB_WRKMULT_A00 for the details of bit fields.
UDB_WRKMULT_A10	0x40341100	Accumulator 1
UDB_WRKMULT_A11	0x40341104	Accumulator 1. See UDB_WRKMULT_A10 for the details of bit fields.
UDB_WRKMULT_A12	0x40341108	Accumulator 1. See UDB_WRKMULT_A10 for the details of bit fields.
UDB_WRKMULT_A13	0x4034110C	Accumulator 1. See UDB_WRKMULT_A10 for the details of bit fields.
UDB_WRKMULT_A14	0x40341110	Accumulator 1. See UDB_WRKMULT_A10 for the details of bit fields.
UDB_WRKMULT_A15	0x40341114	Accumulator 1. See UDB_WRKMULT_A10 for the details of bit fields.
UDB_WRKMULT_A16	0x40341118	Accumulator 1. See UDB_WRKMULT_A10 for the details of bit fields.
UDB_WRKMULT_A17	0x4034111C	Accumulator 1. See UDB_WRKMULT_A10 for the details of bit fields.
UDB_WRKMULT_A18	0x40341120	Accumulator 1. See UDB_WRKMULT_A10 for the details of bit fields.
UDB_WRKMULT_A19	0x40341124	Accumulator 1. See UDB_WRKMULT_A10 for the details of bit fields.
UDB_WRKMULT_A110	0x40341128	Accumulator 1. See UDB_WRKMULT_A10 for the details of bit fields.
UDB_WRKMULT_A111	0x4034112C	Accumulator 1. See UDB_WRKMULT_A10 for the details of bit fields.
UDB_WRKMULT_D00	0x40341200	Data 0
UDB_WRKMULT_D01	0x40341204	Data 0. See UDB_WRKMULT_D00 for the details of bit fields.
UDB_WRKMULT_D02	0x40341208	Data 0. See UDB_WRKMULT_D00 for the details of bit fields.
UDB_WRKMULT_D03	0x4034120C	Data 0. See UDB_WRKMULT_D00 for the details of bit fields.
UDB_WRKMULT_D04	0x40341210	Data 0. See UDB_WRKMULT_D00 for the details of bit fields.
UDB_WRKMULT_D05	0x40341214	Data 0. See UDB_WRKMULT_D00 for the details of bit fields.
UDB_WRKMULT_D06	0x40341218	Data 0. See UDB_WRKMULT_D00 for the details of bit fields.
UDB_WRKMULT_D07	0x4034121C	Data 0. See UDB_WRKMULT_D00 for the details of bit fields.
UDB_WRKMULT_D08	0x40341220	Data 0. See UDB_WRKMULT_D00 for the details of bit fields.
UDB_WRKMULT_D09	0x40341224	Data 0. See UDB_WRKMULT_D00 for the details of bit fields.

Register	Address	Description
UDB_WRKMULT_D010	0x40341228	Data 0. See UDB_WRKMULT_D00 for the details of bit fields.
UDB_WRKMULT_D011	0x4034122C	Data 0. See UDB_WRKMULT_D00 for the details of bit fields.
UDB_WRKMULT_D10	0x40341300	Data 1
UDB_WRKMULT_D11	0x40341304	Data 1. See UDB_WRKMULT_D10 for the details of bit fields.
UDB_WRKMULT_D12	0x40341308	Data 1. See UDB_WRKMULT_D10 for the details of bit fields.
UDB_WRKMULT_D13	0x4034130C	Data 1. See UDB_WRKMULT_D10 for the details of bit fields.
UDB_WRKMULT_D14	0x40341310	Data 1. See UDB_WRKMULT_D10 for the details of bit fields.
UDB_WRKMULT_D15	0x40341314	Data 1. See UDB_WRKMULT_D10 for the details of bit fields.
UDB_WRKMULT_D16	0x40341318	Data 1. See UDB_WRKMULT_D10 for the details of bit fields.
UDB_WRKMULT_D17	0x4034131C	Data 1. See UDB_WRKMULT_D10 for the details of bit fields.
UDB_WRKMULT_D18	0x40341320	Data 1. See UDB_WRKMULT_D10 for the details of bit fields.
UDB_WRKMULT_D19	0x40341324	Data 1. See UDB_WRKMULT_D10 for the details of bit fields.
UDB_WRKMULT_D110	0x40341328	Data 1. See UDB_WRKMULT_D10 for the details of bit fields.
UDB_WRKMULT_D111	0x4034132C	Data 1. See UDB_WRKMULT_D10 for the details of bit fields.
UDB_WRKMULT_F00	0x40341400	FIFO 0
UDB_WRKMULT_F01	0x40341404	FIFO 0. See UDB_WRKMULT_F00 for the details of bit fields.
UDB_WRKMULT_F02	0x40341408	FIFO 0. See UDB_WRKMULT_F00 for the details of bit fields.
UDB_WRKMULT_F03	0x4034140C	FIFO 0. See UDB_WRKMULT_F00 for the details of bit fields.
UDB_WRKMULT_F04	0x40341410	FIFO 0. See UDB_WRKMULT_F00 for the details of bit fields.
UDB_WRKMULT_F05	0x40341414	FIFO 0. See UDB_WRKMULT_F00 for the details of bit fields.
UDB_WRKMULT_F06	0x40341418	FIFO 0. See UDB_WRKMULT_F00 for the details of bit fields.
UDB_WRKMULT_F07	0x4034141C	FIFO 0. See UDB_WRKMULT_F00 for the details of bit fields.
UDB_WRKMULT_F08	0x40341420	FIFO 0. See UDB_WRKMULT_F00 for the details of bit fields.
UDB_WRKMULT_F09	0x40341424	FIFO 0. See UDB_WRKMULT_F00 for the details of bit fields.
UDB_WRKMULT_F010	0x40341428	FIFO 0. See UDB_WRKMULT_F00 for the details of bit fields.
UDB_WRKMULT_F011	0x4034142C	FIFO 0. See UDB_WRKMULT_F00 for the details of bit fields.
UDB_WRKMULT_F10	0x40341500	FIFO 1
UDB_WRKMULT_F11	0x40341504	FIFO 1. See UDB_WRKMULT_F10 for the details of bit fields.
UDB_WRKMULT_F12	0x40341508	FIFO 1. See UDB_WRKMULT_F10 for the details of bit fields.

Register	Address	Description
UDB_WRKMULT_F13	0x4034150C	FIFO 1. See UDB_WRKMULT_F10 for the details of bit fields.
UDB_WRKMULT_F14	0x40341510	FIFO 1. See UDB_WRKMULT_F10 for the details of bit fields.
UDB_WRKMULT_F15	0x40341514	FIFO 1. See UDB_WRKMULT_F10 for the details of bit fields.
UDB_WRKMULT_F16	0x40341518	FIFO 1. See UDB_WRKMULT_F10 for the details of bit fields.
UDB_WRKMULT_F17	0x4034151C	FIFO 1. See UDB_WRKMULT_F10 for the details of bit fields.
UDB_WRKMULT_F18	0x40341520	FIFO 1. See UDB_WRKMULT_F10 for the details of bit fields.
UDB_WRKMULT_F19	0x40341524	FIFO 1. See UDB_WRKMULT_F10 for the details of bit fields.
UDB_WRKMULT_F110	0x40341528	FIFO 1. See UDB_WRKMULT_F10 for the details of bit fields.
UDB_WRKMULT_F111	0x4034152C	FIFO 1. See UDB_WRKMULT_F10 for the details of bit fields.
UDB_WRKMULT_ST0	0x40341600	Status Register
UDB_WRKMULT_ST1	0x40341604	Status Register. See UDB_WRKMULT_ST0 for the details of bit fields.
UDB_WRKMULT_ST2	0x40341608	Status Register. See UDB_WRKMULT_ST0 for the details of bit fields.
UDB_WRKMULT_ST3	0x4034160C	Status Register. See UDB_WRKMULT_ST0 for the details of bit fields.
UDB_WRKMULT_ST4	0x40341610	Status Register. See UDB_WRKMULT_ST0 for the details of bit fields.
UDB_WRKMULT_ST5	0x40341614	Status Register. See UDB_WRKMULT_ST0 for the details of bit fields.
UDB_WRKMULT_ST6	0x40341618	Status Register. See UDB_WRKMULT_ST0 for the details of bit fields.
UDB_WRKMULT_ST7	0x4034161C	Status Register. See UDB_WRKMULT_ST0 for the details of bit fields.
UDB_WRKMULT_ST8	0x40341620	Status Register. See UDB_WRKMULT_ST0 for the details of bit fields.
UDB_WRKMULT_ST9	0x40341624	Status Register. See UDB_WRKMULT_ST0 for the details of bit fields.
UDB_WRKMULT_ST10	0x40341628	Status Register. See UDB_WRKMULT_ST0 for the details of bit fields.
UDB_WRKMULT_ST11	0x4034162C	Status Register. See UDB_WRKMULT_ST0 for the details of bit fields.
UDB_WRKMULT_CTL0	0x40341700	Control Register
UDB_WRKMULT_CTL1	0x40341704	Control Register. See UDB_WRKMULT_CTL0 for the details of bit fields.
UDB_WRKMULT_CTL2	0x40341708	Control Register. See UDB_WRKMULT_CTL0 for the details of bit fields.
UDB_WRKMULT_CTL3	0x4034170C	Control Register. See UDB_WRKMULT_CTL0 for the details of bit fields.
UDB_WRKMULT_CTL4	0x40341710	Control Register. See UDB_WRKMULT_CTL0 for the details of bit fields.
UDB_WRKMULT_CTL5	0x40341714	Control Register. See UDB_WRKMULT_CTL0 for the details of bit fields.
UDB_WRKMULT_CTL6	0x40341718	Control Register. See UDB_WRKMULT_CTL0 for the details of bit fields.
UDB_WRKMULT_CTL7	0x4034171C	Control Register. See UDB_WRKMULT_CTL0 for the details of bit fields.

Register	Address	Description
UDB_WRKMULT_CTL8	0x40341720	Control Register. See UDB_WRKMULT_CTL0 for the details of bit fields.
UDB_WRKMULT_CTL9	0x40341724	Control Register. See UDB_WRKMULT_CTL0 for the details of bit fields.
UDB_WRKMULT_CTL10	0x40341728	Control Register. See UDB_WRKMULT_CTL0 for the details of bit fields.
UDB_WRKMULT_CTL11	0x4034172C	Control Register. See UDB_WRKMULT_CTL0 for the details of bit fields.
UDB_WRKMULT_MSK0	0x40341800	Interrupt Mask
UDB_WRKMULT_MSK1	0x40341804	Interrupt Mask. See UDB_WRKMULT_MSK0 for the details of bit fields.
UDB_WRKMULT_MSK2	0x40341808	Interrupt Mask. See UDB_WRKMULT_MSK0 for the details of bit fields.
UDB_WRKMULT_MSK3	0x4034180C	Interrupt Mask. See UDB_WRKMULT_MSK0 for the details of bit fields.
UDB_WRKMULT_MSK4	0x40341810	Interrupt Mask. See UDB_WRKMULT_MSK0 for the details of bit fields.
UDB_WRKMULT_MSK5	0x40341814	Interrupt Mask. See UDB_WRKMULT_MSK0 for the details of bit fields.
UDB_WRKMULT_MSK6	0x40341818	Interrupt Mask. See UDB_WRKMULT_MSK0 for the details of bit fields.
UDB_WRKMULT_MSK7	0x4034181C	Interrupt Mask. See UDB_WRKMULT_MSK0 for the details of bit fields.
UDB_WRKMULT_MSK8	0x40341820	Interrupt Mask. See UDB_WRKMULT_MSK0 for the details of bit fields.
UDB_WRKMULT_MSK9	0x40341824	Interrupt Mask. See UDB_WRKMULT_MSK0 for the details of bit fields.
UDB_WRKMULT_MSK10	0x40341828	Interrupt Mask. See UDB_WRKMULT_MSK0 for the details of bit fields.
UDB_WRKMULT_MSK11	0x4034182C	Interrupt Mask. See UDB_WRKMULT_MSK0 for the details of bit fields.
UDB_WRKMULT_ACTL0	0x40341900	Auxiliary Control
UDB_WRKMULT_ACTL1	0x40341904	Auxiliary Control. See UDB_WRKMULT_ACTL0 for the details of bit fields.
UDB_WRKMULT_ACTL2	0x40341908	Auxiliary Control. See UDB_WRKMULT_ACTL0 for the details of bit fields.
UDB_WRKMULT_ACTL3	0x4034190C	Auxiliary Control. See UDB_WRKMULT_ACTL0 for the details of bit fields.
UDB_WRKMULT_ACTL4	0x40341910	Auxiliary Control. See UDB_WRKMULT_ACTL0 for the details of bit fields.
UDB_WRKMULT_ACTL5	0x40341914	Auxiliary Control. See UDB_WRKMULT_ACTL0 for the details of bit fields.
UDB_WRKMULT_ACTL6	0x40341918	Auxiliary Control. See UDB_WRKMULT_ACTL0 for the details of bit fields.
UDB_WRKMULT_ACTL7	0x4034191C	Auxiliary Control. See UDB_WRKMULT_ACTL0 for the details of bit fields.
UDB_WRKMULT_ACTL8	0x40341920	Auxiliary Control. See UDB_WRKMULT_ACTL0 for the details of bit fields.
UDB_WRKMULT_ACTL9	0x40341924	Auxiliary Control. See UDB_WRKMULT_ACTL0 for the details of bit fields.
UDB_WRKMULT_ACTL10	0x40341928	Auxiliary Control. See UDB_WRKMULT_ACTL0 for the details of bit fields.
UDB_WRKMULT_ACTL11	0x4034192C	Auxiliary Control. See UDB_WRKMULT_ACTL0 for the details of bit fields.
UDB_WRKMULT_MC0	0x40341A00	PLD Macrocell reading

Register	Address	Description
UDB_WRKMULT_MC1	0x40341A04	PLD Macrocell reading. See UDB_WRKMULT_MC0 for the details of bit fields.
UDB_WRKMULT_MC2	0x40341A08	PLD Macrocell reading. See UDB_WRKMULT_MC0 for the details of bit fields.
UDB_WRKMULT_MC3	0x40341A0C	PLD Macrocell reading. See UDB_WRKMULT_MC0 for the details of bit fields.
UDB_WRKMULT_MC4	0x40341A10	PLD Macrocell reading. See UDB_WRKMULT_MC0 for the details of bit fields.
UDB_WRKMULT_MC5	0x40341A14	PLD Macrocell reading. See UDB_WRKMULT_MC0 for the details of bit fields.
UDB_WRKMULT_MC6	0x40341A18	PLD Macrocell reading. See UDB_WRKMULT_MC0 for the details of bit fields.
UDB_WRKMULT_MC7	0x40341A1C	PLD Macrocell reading. See UDB_WRKMULT_MC0 for the details of bit fields.
UDB_WRKMULT_MC8	0x40341A20	PLD Macrocell reading. See UDB_WRKMULT_MC0 for the details of bit fields.
UDB_WRKMULT_MC9	0x40341A24	PLD Macrocell reading. See UDB_WRKMULT_MC0 for the details of bit fields.
UDB_WRKMULT_MC10	0x40341A28	PLD Macrocell reading. See UDB_WRKMULT_MC0 for the details of bit fields.
UDB_WRKMULT_MC11	0x40341A2C	PLD Macrocell reading. See UDB_WRKMULT_MC0 for the details of bit fields.
UDB_UDBPAIR0_UDBSNG0_PLD_IT0	0x40342000	PLD Input Terms
UDB_UDBPAIR0_UDBSNG0_PLD_IT1	0x40342004	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR0_UDBSNG0_PLD_IT2	0x40342008	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR0_UDBSNG0_PLD_IT3	0x4034200C	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR0_UDBSNG0_PLD_IT4	0x40342010	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR0_UDBSNG0_PLD_IT5	0x40342014	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR0_UDBSNG0_PLD_IT6	0x40342018	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR0_UDBSNG0_PLD_IT7	0x4034201C	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR0_UDBSNG0_PLD_IT8	0x40342020	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR0_UDBSNG0_PLD_IT9	0x40342024	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR0_UDBSNG0_PLD_IT10	0x40342028	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR0_UDBSNG0_PLD_IT11	0x4034202C	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR0_UDBSNG0_PLD_ORT0	0x40342030	PLD OR Terms
UDB_UDBPAIR0_UDBSNG0_PLD_ORT1	0x40342034	PLD OR Terms
UDB_UDBPAIR0_UDBSNG0_PLD_CFG0	0x40342038	PLD configuration for Carry Enable, Constant, and XOR feedback
UDB_UDBPAIR0_UDBSNG0_PLD_CFG1	0x4034203C	PLD configuration for Set / Reset selection, and Bypass control
UDB_UDBPAIR0_UDBSNG0_DPATH_CFG0	0x40342040	Datapath input selections (RAD0, RAD1, RAD2, F0_LD, F1_LD, D0_LD, D1_LD)
UDB_UDBPAIR0_UDBSNG0_DPATH_CFG1	0x40342044	Datapath input and output selections (SCI_MUX, SI_MUX, OUT0 thru OUT5)

Register	Address	Description
UDB_UDBPAIR0_UDBSNG0_DPATH_CFG2	0x40342048	Datapath output synchronization, ALU mask, compare 0 and 1 masks
UDB_UDBPAIR0_UDBSNG0_DPATH_CFG3	0x4034204C	Datapath mask enables, shift in, carry in, compare, chaining, MSB configs; FIFO, shift and parallel input control
UDB_UDBPAIR0_UDBSNG0_DPATH_CFG4	0x40342050	Datapath FIFO and register access configuration control
UDB_UDBPAIR0_UDBSNG0_SC_CFG0	0x40342054	SC Mode 0 and 1 control registers; status register input mode; general SC configuration
UDB_UDBPAIR0_UDBSNG0_SC_CFG1	0x40342058	SC counter control
UDB_UDBPAIR0_UDBSNG0_RC_CFG0	0x4034205C	PLD0, PLD1, Datatpath, and SC clock and reset control
UDB_UDBPAIR0_UDBSNG0_RC_CFG1	0x40342060	PLD0, PLD1, Datatpath, and SC clock selection, general reset control
UDB_UDBPAIR0_UDBSNG0_DPATH_OPC0	0x40342064	Datapath opcode configuration
UDB_UDBPAIR0_UDBSNG0_DPATH_OPC1	0x40342068	Datapath opcode configuration. See UDB_UDBPAIR0_UDBSNG0_DPATH_OPC0 for the details of bit fields.
UDB_UDBPAIR0_UDBSNG0_DPATH_OPC2	0x4034206C	Datapath opcode configuration. See UDB_UDBPAIR0_UDBSNG0_DPATH_OPC0 for the details of bit fields.
UDB_UDBPAIR0_UDBSNG0_DPATH_OPC3	0x40342070	Datapath opcode configuration. See UDB_UDBPAIR0_UDBSNG0_DPATH_OPC0 for the details of bit fields.
UDB_UDBPAIR0_UDBSNG1_PLD_IT0	0x40342080	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR0_UDBSNG1_PLD_IT1	0x40342084	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR0_UDBSNG1_PLD_IT2	0x40342088	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR0_UDBSNG1_PLD_IT3	0x4034208C	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR0_UDBSNG1_PLD_IT4	0x40342090	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR0_UDBSNG1_PLD_IT5	0x40342094	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR0_UDBSNG1_PLD_IT6	0x40342098	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR0_UDBSNG1_PLD_IT7	0x4034209C	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR0_UDBSNG1_PLD_IT8	0x403420A0	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR0_UDBSNG1_PLD_IT9	0x403420A4	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR0_UDBSNG1_PLD_IT10	0x403420A8	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR0_UDBSNG1_PLD_IT11	0x403420AC	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR0_UDBSNG1_PLD_ORT0	0x403420B0	PLD OR Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_ORT0 for the details of bit fields.
UDB_UDBPAIR0_UDBSNG1_PLD_ORT1	0x403420B4	PLD OR Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_ORT1 for the details of bit fields.
UDB_UDBPAIR0_UDBSNG1_PLD_CFG0	0x403420B8	PLD configuration for Carry Enable, Constant, and XOR feedback. See UDB_UDB-PAIR0_UDBSNG0_PLD_CFG0 for the details of bit fields.
UDB_UDBPAIR0_UDBSNG1_PLD_CFG1	0x403420BC	PLD configuration for Set / Reset selection, and Bypass control. See UDB_UDB-PAIR0_UDBSNG0_PLD_CFG1 for the details of bit fields.
UDB_UDBPAIR0_UDBSNG1_DPATH_CFG0	0x403420C0	Datapath input selections (RAD0, RAD1, RAD2, F0_LD, F1_LD, D0_LD, D1_LD). See UDB_UDBPAIR0_UDBSNG0_DPATH_CFG0 for the details of bit fields.
UDB_UDBPAIR0_UDBSNG1_DPATH_CFG1	0x403420C4	Datapath input and output selections (SCI_MUX, SI_MUX, OUT0 thru OUT5). See UDB_UDBPAIR0_UDBSNG0_DPATH_CFG1 for the details of bit fields.

Register	Address	Description
UDB_UDBPAIR0_UDBSNG1_DPATH_CFG2	0x403420C8	Datapath output synchronization, ALU mask, compare 0 and 1 masks. See UDB_UDB-PAIR0_UDBSNG0_DPATH_CFG2 for the details of bit fields.
UDB_UDBPAIR0_UDBSNG1_DPATH_CFG3	0x403420CC	Datapath mask enables, shift in, carry in, compare, chaining, MSB configs; FIFO, shift and parallel input control. See UDB_UDBPAIR0_UDBSNG0_DPATH_CFG3 for the details of bit fields.
UDB_UDBPAIR0_UDBSNG1_DPATH_CFG4	0x403420D0	Datapath FIFO and register access configuration control. See UDB_UDB-PAIR0_UDBSNG0_DPATH_CFG4 for the details of bit fields.
UDB_UDBPAIR0_UDBSNG1_SC_CFG0	0x403420D4	SC Mode 0 and 1 control registers; status register input mode; general SC configuration. See UDB_UDBPAIR0_UDBSNG0_SC_CFG0 for the details of bit fields.
UDB_UDBPAIR0_UDBSNG1_SC_CFG1	0x403420D8	SC counter control. See UDB_UDBPAIR0_UDBSNG0_SC_CFG1 for the details of bit fields.
UDB_UDBPAIR0_UDBSNG1_RC_CFG0	0x403420DC	PLD0, PLD1, Datatpath, and SC clock and reset control. See UDB_UDB-PAIR0_UDBSNG0_RC_CFG0 for the details of bit fields.
UDB_UDBPAIR0_UDBSNG1_RC_CFG1	0x403420E0	PLD0, PLD1, Datatpath, and SC clock selection, general reset control. See UDB_UDB-PAIR0_UDBSNG0_RC_CFG1 for the details of bit fields.
UDB_UDBPAIR0_UDBSNG1_DPATH_OPC0	0x403420E4	Datapath opcode configuration. See UDB_UDBPAIR0_UDBSNG0_DPATH_OPC0 for the details of bit fields.
UDB_UDBPAIR0_UDBSNG1_DPATH_OPC1	0x403420E8	Datapath opcode configuration. See UDB_UDBPAIR0_UDBSNG0_DPATH_OPC0 for the details of bit fields.
UDB_UDBPAIR0_UDBSNG1_DPATH_OPC2	0x403420EC	Datapath opcode configuration. See UDB_UDBPAIR0_UDBSNG0_DPATH_OPC0 for the details of bit fields.
UDB_UDBPAIR0_UDBSNG1_DPATH_OPC3	0x403420F0	Datapath opcode configuration. See UDB_UDBPAIR0_UDBSNG0_DPATH_OPC0 for the details of bit fields.
UDB_UDBPAIR0_ROUTE_TOP_V_BOT	0x40342100	Top Vertical Input (TVI) vs Bottom Vertical Input (BVI) muxing
UDB_UDBPAIR0_ROUTE_LVO1_V_2	0x40342104	Left Vertical Ouput (LVO) 1 vs 2 muxing for certain horizontals
UDB_UDBPAIR0_ROUTE_RVO1_V_2	0x40342108	Right Vertical Ouput (RVO) 1 vs 2 muxing for certain horizontals
UDB_UDBPAIR0_ROUTE_TUI_CFG0	0x4034210C	Top UDB Input (TUI) selection
UDB_UDBPAIR0_ROUTE_TUI_CFG1	0x40342110	Top UDB Input (TUI) selection
UDB_UDBPAIR0_ROUTE_TUI_CFG2	0x40342114	Top UDB Input (TUI) selection
UDB_UDBPAIR0_ROUTE_TUI_CFG3	0x40342118	Top UDB Input (TUI) selection
UDB_UDBPAIR0_ROUTE_TUI_CFG4	0x4034211C	Top UDB Input (TUI) selection
UDB_UDBPAIR0_ROUTE_TUI_CFG5	0x40342120	Top UDB Input (TUI) selection
UDB_UDBPAIR0_ROUTE_BUI_CFG0	0x40342124	Bottom UDB Input (BUI) selection
UDB_UDBPAIR0_ROUTE_BUI_CFG1	0x40342128	Bottom UDB Input (BUI) selection
UDB_UDBPAIR0_ROUTE_BUI_CFG2	0x4034212C	Bottom UDB Input (BUI) selection
UDB_UDBPAIR0_ROUTE_BUI_CFG3	0x40342130	Bottom UDB Input (BUI) selection
UDB_UDBPAIR0_ROUTE_BUI_CFG4	0x40342134	Bottom UDB Input (BUI) selection
UDB_UDBPAIR0_ROUTE_BUI_CFG5	0x40342138	Bottom UDB Input (BUI) selection
UDB_UDBPAIR0_ROUTE_RVO_CFG0	0x4034213C	Right Vertical Ouput (RVO) selection
UDB_UDBPAIR0_ROUTE_RVO_CFG1	0x40342140	Right Vertical Ouput (RVO) selection
UDB_UDBPAIR0_ROUTE_RVO_CFG2	0x40342144	Right Vertical Ouput (RVO) selection

Register	Address	Description
UDB_UDBPAIR0_ROUTE_RVO_CFG3	0x40342148	Right Vertical Ouput (RVO) selection
UDB_UDBPAIR0_ROUTE_LVO_CFG0	0x4034214C	Left Vertical Ouput (LVO) selection
UDB_UDBPAIR0_ROUTE_LVO_CFG1	0x40342150	Left Vertical Ouput (LVO) selection
UDB_UDBPAIR0_ROUTE_RHO_CFG0	0x40342154	Right Horizontal Out (RHO) selection
UDB_UDBPAIR0_ROUTE_RHO_CFG1	0x40342158	Right Horizontal Out (RHO) selection
UDB_UDBPAIR0_ROUTE_RHO_CFG2	0x4034215C	Right Horizontal Out (RHO) selection
UDB_UDBPAIR0_ROUTE_LHO_CFG0	0x40342160	Left Horizontal Out (LHO) selection
UDB_UDBPAIR0_ROUTE_LHO_CFG1	0x40342164	Left Horizontal Out (LHO) selection
UDB_UDBPAIR0_ROUTE_LHO_CFG2	0x40342168	Left Horizontal Out (LHO) selection
UDB_UDBPAIR0_ROUTE_LHO_CFG3	0x4034216C	Left Horizontal Out (LHO) selection
UDB_UDBPAIR0_ROUTE_LHO_CFG4	0x40342170	Left Horizontal Out (LHO) selection
UDB_UDBPAIR0_ROUTE_LHO_CFG5	0x40342174	Left Horizontal Out (LHO) selection
UDB_UDBPAIR0_ROUTE_LHO_CFG6	0x40342178	Left Horizontal Out (LHO) selection
UDB_UDBPAIR0_ROUTE_LHO_CFG7	0x4034217C	Left Horizontal Out (LHO) selection
UDB_UDBPAIR0_ROUTE_LHO_CFG8	0x40342180	Left Horizontal Out (LHO) selection
UDB_UDBPAIR0_ROUTE_LHO_CFG9	0x40342184	Left Horizontal Out (LHO) selection
UDB_UDBPAIR0_ROUTE_LHO_CFG10	0x40342188	Left Horizontal Out (LHO) selection
UDB_UDBPAIR0_ROUTE_LHO_CFG11	0x4034218C	Left Horizontal Out (LHO) selection
UDB_UDBPAIR1_UDBSNG0_PLD_IT0	0x40342200	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR1_UDBSNG0_PLD_IT1	0x40342204	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR1_UDBSNG0_PLD_IT2	0x40342208	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR1_UDBSNG0_PLD_IT3	0x4034220C	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR1_UDBSNG0_PLD_IT4	0x40342210	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR1_UDBSNG0_PLD_IT5	0x40342214	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR1_UDBSNG0_PLD_IT6	0x40342218	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR1_UDBSNG0_PLD_IT7	0x4034221C	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR1_UDBSNG0_PLD_IT8	0x40342220	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR1_UDBSNG0_PLD_IT9	0x40342224	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR1_UDBSNG0_PLD_IT10	0x40342228	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.

Register	Address	Description
UDB_UDBPAIR1_UDBSNG0_PLD_IT11	0x4034222C	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR1_UDBSNG0_PLD_ORT0	0x40342230	PLD OR Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_ORT0 for the details of bit fields.
UDB_UDBPAIR1_UDBSNG0_PLD_ORT1	0x40342234	PLD OR Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_ORT1 for the details of bit fields.
UDB_UDBPAIR1_UDBSNG0_PLD_CFG0	0x40342238	PLD configuration for Carry Enable, Constant, and XOR feedback. See UDB_UDB-PAIR0_UDBSNG0_PLD_CFG0 for the details of bit fields.
UDB_UDBPAIR1_UDBSNG0_PLD_CFG1	0x4034223C	PLD configuration for Set / Reset selection, and Bypass control. See UDB_UDB-PAIR0_UDBSNG0_PLD_CFG1 for the details of bit fields.
UDB_UDBPAIR1_UDBSNG0_DPATH_CFG0	0x40342240	Datapath input selections (RAD0, RAD1, RAD2, F0_LD, F1_LD, D0_LD, D1_LD). See UDB_UDBPAIR0_UDBSNG0_DPATH_CFG0 for the details of bit fields.
UDB_UDBPAIR1_UDBSNG0_DPATH_CFG1	0x40342244	Datapath input and output selections (SCI_MUX, SI_MUX, OUT0 thru OUT5). See UDB_UDBPAIR0_UDBSNG0_DPATH_CFG1 for the details of bit fields.
UDB_UDBPAIR1_UDBSNG0_DPATH_CFG2	0x40342248	Datapath output synchronization, ALU mask, compare 0 and 1 masks. See UDB_UDB-PAIR0_UDBSNG0_DPATH_CFG2 for the details of bit fields.
UDB_UDBPAIR1_UDBSNG0_DPATH_CFG3	0x4034224C	Datapath mask enables, shift in, carry in, compare, chaining, MSB configs; FIFO, shift and parallel input control. See UDB_UDBPAIR0_UDBSNG0_DPATH_CFG3 for the details of bit fields.
UDB_UDBPAIR1_UDBSNG0_DPATH_CFG4	0x40342250	Datapath FIFO and register access configuration control. See UDB_UDB-PAIR0_UDBSNG0_DPATH_CFG4 for the details of bit fields.
UDB_UDBPAIR1_UDBSNG0_SC_CFG0	0x40342254	SC Mode 0 and 1 control registers; status register input mode; general SC configuration. See UDB_UDBPAIR0_UDBSNG0_SC_CFG0 for the details of bit fields.
UDB_UDBPAIR1_UDBSNG0_SC_CFG1	0x40342258	SC counter control. See UDB_UDBPAIR0_UDBSNG0_SC_CFG1 for the details of bit fields.
UDB_UDBPAIR1_UDBSNG0_RC_CFG0	0x4034225C	PLD0, PLD1, Datatpath, and SC clock and reset control. See UDB_UDB-PAIR0_UDBSNG0_RC_CFG0 for the details of bit fields.
UDB_UDBPAIR1_UDBSNG0_RC_CFG1	0x40342260	PLD0, PLD1, Datatpath, and SC clock selection, general reset control. See UDB_UDB-PAIR0_UDBSNG0_RC_CFG1 for the details of bit fields.
UDB_UDBPAIR1_UDBSNG0_DPATH_OPC0	0x40342264	Datapath opcode configuration. See UDB_UDBPAIR0_UDBSNG0_DPATH_OPC0 for the details of bit fields.
UDB_UDBPAIR1_UDBSNG0_DPATH_OPC1	0x40342268	Datapath opcode configuration. See UDB_UDBPAIR0_UDBSNG0_DPATH_OPC0 for the details of bit fields.
UDB_UDBPAIR1_UDBSNG0_DPATH_OPC2	0x4034226C	Datapath opcode configuration. See UDB_UDBPAIR0_UDBSNG0_DPATH_OPC0 for the details of bit fields.
UDB_UDBPAIR1_UDBSNG0_DPATH_OPC3	0x40342270	Datapath opcode configuration. See UDB_UDBPAIR0_UDBSNG0_DPATH_OPC0 for the details of bit fields.
UDB_UDBPAIR1_UDBSNG1_PLD_IT0	0x40342280	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR1_UDBSNG1_PLD_IT1	0x40342284	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR1_UDBSNG1_PLD_IT2	0x40342288	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR1_UDBSNG1_PLD_IT3	0x4034228C	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR1_UDBSNG1_PLD_IT4	0x40342290	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR1_UDBSNG1_PLD_IT5	0x40342294	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR1_UDBSNG1_PLD_IT6	0x40342298	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR1_UDBSNG1_PLD_IT7	0x4034229C	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR1_UDBSNG1_PLD_IT8	0x403422A0	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR1_UDBSNG1_PLD_IT9	0x403422A4	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR1_UDBSNG1_PLD_IT10	0x403422A8	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.

Register	Address	Description
UDB_UDBPAIR1_UDBSNG1_PLD_IT11	0x403422AC	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR1_UDBSNG1_PLD_ORT0	0x403422B0	PLD OR Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_ORT0 for the details of bit fields.
UDB_UDBPAIR1_UDBSNG1_PLD_ORT1	0x403422B4	PLD OR Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_ORT1 for the details of bit fields.
UDB_UDBPAIR1_UDBSNG1_PLD_CFG0	0x403422B8	PLD configuration for Carry Enable, Constant, and XOR feedback. See UDB_UDB-PAIR0_UDBSNG0_PLD_CFG0 for the details of bit fields.
UDB_UDBPAIR1_UDBSNG1_PLD_CFG1	0x403422BC	PLD configuration for Set / Reset selection, and Bypass control. See UDB_UDB-PAIR0_UDBSNG0_PLD_CFG1 for the details of bit fields.
UDB_UDBPAIR1_UDBSNG1_DPATH_CFG0	0x403422C0	Datapath input selections (RAD0, RAD1, RAD2, F0_LD, F1_LD, D0_LD, D1_LD). See UDB_UDBPAIR0_UDBSNG0_DPATH_CFG0 for the details of bit fields.
UDB_UDBPAIR1_UDBSNG1_DPATH_CFG1	0x403422C4	Datapath input and output selections (SCI_MUX, SI_MUX, OUT0 thru OUT5). See UDB_UDBPAIR0_UDBSNG0_DPATH_CFG1 for the details of bit fields.
UDB_UDBPAIR1_UDBSNG1_DPATH_CFG2	0x403422C8	Datapath output synchronization, ALU mask, compare 0 and 1 masks. See UDB_UDB-PAIR0_UDBSNG0_DPATH_CFG2 for the details of bit fields.
UDB_UDBPAIR1_UDBSNG1_DPATH_CFG3	0x403422CC	Datapath mask enables, shift in, carry in, compare, chaining, MSB configs; FIFO, shift and parallel input control. See UDB_UDBPAIR0_UDBSNG0_DPATH_CFG3 for the details of bit fields.
UDB_UDBPAIR1_UDBSNG1_DPATH_CFG4	0x403422D0	Datapath FIFO and register access configuration control. See UDB_UDB-PAIR0_UDBSNG0_DPATH_CFG4 for the details of bit fields.
UDB_UDBPAIR1_UDBSNG1_SC_CFG0	0x403422D4	SC Mode 0 and 1 control registers; status register input mode; general SC configuration. See UDB_UDBPAIR0_UDBSNG0_SC_CFG0 for the details of bit fields.
UDB_UDBPAIR1_UDBSNG1_SC_CFG1	0x403422D8	SC counter control. See UDB_UDBPAIR0_UDBSNG0_SC_CFG1 for the details of bit fields.
UDB_UDBPAIR1_UDBSNG1_RC_CFG0	0x403422DC	PLD0, PLD1, Datatpath, and SC clock and reset control. See UDB_UDB-PAIR0_UDBSNG0_RC_CFG0 for the details of bit fields.
UDB_UDBPAIR1_UDBSNG1_RC_CFG1	0x403422E0	PLD0, PLD1, Datatpath, and SC clock selection, general reset control. See UDB_UDB-PAIR0_UDBSNG0_RC_CFG1 for the details of bit fields.
UDB_UDBPAIR1_UDBSNG1_DPATH_OPC0	0x403422E4	Datapath opcode configuration. See UDB_UDBPAIR0_UDBSNG0_DPATH_OPC0 for the details of bit fields.
UDB_UDBPAIR1_UDBSNG1_DPATH_OPC1	0x403422E8	Datapath opcode configuration. See UDB_UDBPAIR0_UDBSNG0_DPATH_OPC0 for the details of bit fields.
UDB_UDBPAIR1_UDBSNG1_DPATH_OPC2	0x403422EC	Datapath opcode configuration. See UDB_UDBPAIR0_UDBSNG0_DPATH_OPC0 for the details of bit fields.
UDB_UDBPAIR1_UDBSNG1_DPATH_OPC3	0x403422F0	Datapath opcode configuration. See UDB_UDBPAIR0_UDBSNG0_DPATH_OPC0 for the details of bit fields.
UDB_UDBPAIR1_ROUTE_TOP_V_BOT	0x40342300	Top Vertical Input (TVI) vs Bottom Vertical Input (BVI) muxing. See UDB_UDB-PAIR0_ROUTE_TOP_V_BOT for the details of bit fields.
UDB_UDBPAIR1_ROUTE_LVO1_V_2	0x40342304	Left Vertical Ouput (LVO) 1 vs 2 muxing for certain horizontals. See UDB_UDB-PAIR0_ROUTE_LVO1_V_2 for the details of bit fields.
UDB_UDBPAIR1_ROUTE_RVO1_V_2	0x40342308	Right Vertical Ouput (RVO) 1 vs 2 muxing for certain horizontals. See UDB_UDB-PAIR0_ROUTE_RVO1_V_2 for the details of bit fields.
UDB_UDBPAIR1_ROUTE_TUI_CFG0	0x4034230C	Top UDB Input (TUI) selection. See UDB_UDBPAIR0_ROUTE_TUI_CFG0 for the details of bit fields.
UDB_UDBPAIR1_ROUTE_TUI_CFG1	0x40342310	Top UDB Input (TUI) selection. See UDB_UDBPAIR0_ROUTE_TUI_CFG1 for the details of bit fields.
UDB_UDBPAIR1_ROUTE_TUI_CFG2	0x40342314	Top UDB Input (TUI) selection. See UDB_UDBPAIR0_ROUTE_TUI_CFG2 for the details of bit fields.
UDB_UDBPAIR1_ROUTE_TUI_CFG3	0x40342318	Top UDB Input (TUI) selection. See UDB_UDBPAIR0_ROUTE_TUI_CFG3 for the details of bit fields.
UDB_UDBPAIR1_ROUTE_TUI_CFG4	0x4034231C	Top UDB Input (TUI) selection. See UDB_UDBPAIR0_ROUTE_TUI_CFG4 for the details of bit fields.
UDB_UDBPAIR1_ROUTE_TUI_CFG5	0x40342320	Top UDB Input (TUI) selection. See UDB_UDBPAIR0_ROUTE_TUI_CFG5 for the details of bit fields.
UDB_UDBPAIR1_ROUTE_BUI_CFG0	0x40342324	Bottom UDB Input (BUI) selection. See UDB_UDBPAIR0_ROUTE_BUI_CFG0 for the details of bit fields.
UDB_UDBPAIR1_ROUTE_BUI_CFG1	0x40342328	Bottom UDB Input (BUI) selection. See UDB_UDBPAIR0_ROUTE_BUI_CFG1 for the details of bit fields.

Register	Address	Description
UDB_UDBPAIR1_ROUTE_BUI_CFG2	0x4034232C	Bottom UDB Input (BUI) selection. See UDB_UDBPAIR0_ROUTE_BUI_CFG2 for the details of bit fields.
UDB_UDBPAIR1_ROUTE_BUI_CFG3	0x40342330	Bottom UDB Input (BUI) selection. See UDB_UDBPAIR0_ROUTE_BUI_CFG3 for the details of bit fields.
UDB_UDBPAIR1_ROUTE_BUI_CFG4	0x40342334	Bottom UDB Input (BUI) selection. See UDB_UDBPAIR0_ROUTE_BUI_CFG4 for the details of bit fields.
UDB_UDBPAIR1_ROUTE_BUI_CFG5	0x40342338	Bottom UDB Input (BUI) selection. See UDB_UDBPAIR0_ROUTE_BUI_CFG5 for the details of bit fields.
UDB_UDBPAIR1_ROUTE_RVO_CFG0	0x4034233C	Right Vertical Ouput (RVO) selection. See UDB_UDBPAIR0_ROUTE_RVO_CFG0 for the details of bit fields.
UDB_UDBPAIR1_ROUTE_RVO_CFG1	0x40342340	Right Vertical Ouput (RVO) selection. See UDB_UDBPAIR0_ROUTE_RVO_CFG1 for the details of bit fields.
UDB_UDBPAIR1_ROUTE_RVO_CFG2	0x40342344	Right Vertical Ouput (RVO) selection. See UDB_UDBPAIR0_ROUTE_RVO_CFG2 for the details of bit fields.
UDB_UDBPAIR1_ROUTE_RVO_CFG3	0x40342348	Right Vertical Ouput (RVO) selection. See UDB_UDBPAIR0_ROUTE_RVO_CFG3 for the details of bit fields.
UDB_UDBPAIR1_ROUTE_LVO_CFG0	0x4034234C	Left Vertical Ouput (LVO) selection. See UDB_UDBPAIR0_ROUTE_LVO_CFG0 for the details of bit fields.
UDB_UDBPAIR1_ROUTE_LVO_CFG1	0x40342350	Left Vertical Ouput (LVO) selection. See UDB_UDBPAIR0_ROUTE_LVO_CFG1 for the details of bit fields.
UDB_UDBPAIR1_ROUTE_RHO_CFG0	0x40342354	Right Horizontal Out (RHO) selection. See UDB_UDBPAIR0_ROUTE_RHO_CFG0 for the details of bit fields.
UDB_UDBPAIR1_ROUTE_RHO_CFG1	0x40342358	Right Horizontal Out (RHO) selection. See UDB_UDBPAIR0_ROUTE_RHO_CFG1 for the details of bit fields.
UDB_UDBPAIR1_ROUTE_RHO_CFG2	0x4034235C	Right Horizontal Out (RHO) selection. See UDB_UDBPAIR0_ROUTE_RHO_CFG2 for the details of bit fields.
UDB_UDBPAIR1_ROUTE_LHO_CFG0	0x40342360	Left Horizontal Out (LHO) selection. See UDB_UDBPAIR0_ROUTE_LHO_CFG0 for the details of bit fields.
UDB_UDBPAIR1_ROUTE_LHO_CFG1	0x40342364	Left Horizontal Out (LHO) selection. See UDB_UDBPAIR0_ROUTE_LHO_CFG1 for the details of bit fields.
UDB_UDBPAIR1_ROUTE_LHO_CFG2	0x40342368	Left Horizontal Out (LHO) selection. See UDB_UDBPAIR0_ROUTE_LHO_CFG2 for the details of bit fields.
UDB_UDBPAIR1_ROUTE_LHO_CFG3	0x4034236C	Left Horizontal Out (LHO) selection. See UDB_UDBPAIR0_ROUTE_LHO_CFG3 for the details of bit fields.
UDB_UDBPAIR1_ROUTE_LHO_CFG4	0x40342370	Left Horizontal Out (LHO) selection. See UDB_UDBPAIR0_ROUTE_LHO_CFG4 for the details of bit fields.
UDB_UDBPAIR1_ROUTE_LHO_CFG5	0x40342374	Left Horizontal Out (LHO) selection. See UDB_UDBPAIR0_ROUTE_LHO_CFG5 for the details of bit fields.
UDB_UDBPAIR1_ROUTE_LHO_CFG6	0x40342378	Left Horizontal Out (LHO) selection. See UDB_UDBPAIR0_ROUTE_LHO_CFG6 for the details of bit fields.
UDB_UDBPAIR1_ROUTE_LHO_CFG7	0x4034237C	Left Horizontal Out (LHO) selection. See UDB_UDBPAIR0_ROUTE_LHO_CFG7 for the details of bit fields.
UDB_UDBPAIR1_ROUTE_LHO_CFG8	0x40342380	Left Horizontal Out (LHO) selection. See UDB_UDBPAIR0_ROUTE_LHO_CFG8 for the details of bit fields.
UDB_UDBPAIR1_ROUTE_LHO_CFG9	0x40342384	Left Horizontal Out (LHO) selection. See UDB_UDBPAIR0_ROUTE_LHO_CFG9 for the details of bit fields.
UDB_UDBPAIR1_ROUTE_LHO_CFG10	0x40342388	Left Horizontal Out (LHO) selection. See UDB_UDBPAIR0_ROUTE_LHO_CFG10 for the details of bit fields.
UDB_UDBPAIR1_ROUTE_LHO_CFG11	0x4034238C	Left Horizontal Out (LHO) selection. See UDB_UDBPAIR0_ROUTE_LHO_CFG11 for the details of bit fields.
UDB_UDBPAIR2_UDBSNG0_PLD_IT0	0x40342400	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR2_UDBSNG0_PLD_IT1	0x40342404	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR2_UDBSNG0_PLD_IT2	0x40342408	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR2_UDBSNG0_PLD_IT3	0x4034240C	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.

Register	Address	Description
UDB_UDBPAIR2_UDBSNG0_PLD_IT4	0x40342410	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR2_UDBSNG0_PLD_IT5	0x40342414	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR2_UDBSNG0_PLD_IT6	0x40342418	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR2_UDBSNG0_PLD_IT7	0x4034241C	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR2_UDBSNG0_PLD_IT8	0x40342420	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR2_UDBSNG0_PLD_IT9	0x40342424	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR2_UDBSNG0_PLD_IT10	0x40342428	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR2_UDBSNG0_PLD_IT11	0x4034242C	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR2_UDBSNG0_PLD_ORT0	0x40342430	PLD OR Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_ORT0 for the details of bit fields.
UDB_UDBPAIR2_UDBSNG0_PLD_ORT1	0x40342434	PLD OR Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_ORT1 for the details of bit fields.
UDB_UDBPAIR2_UDBSNG0_PLD_CFG0	0x40342438	PLD configuration for Carry Enable, Constant, and XOR feedback. See UDB_UDB-PAIR0_UDBSNG0_PLD_CFG0 for the details of bit fields.
UDB_UDBPAIR2_UDBSNG0_PLD_CFG1	0x4034243C	PLD configuration for Set / Reset selection, and Bypass control. See UDB_UDB-PAIR0_UDBSNG0_PLD_CFG1 for the details of bit fields.
UDB_UDBPAIR2_UDBSNG0_DPATH_CFG0	0x40342440	Datapath input selections (RAD0, RAD1, RAD2, F0_LD, F1_LD, D0_LD, D1_LD). See UDB_UDBPAIR0_UDBSNG0_DPATH_CFG0 for the details of bit fields.
UDB_UDBPAIR2_UDBSNG0_DPATH_CFG1	0x40342444	Datapath input and output selections (SCI_MUX, SI_MUX, OUT0 thru OUT5). See UDB_UDBPAIR0_UDBSNG0_DPATH_CFG1 for the details of bit fields.
UDB_UDBPAIR2_UDBSNG0_DPATH_CFG2	0x40342448	Datapath output synchronization, ALU mask, compare 0 and 1 masks. See UDB_UDB-PAIR0_UDBSNG0_DPATH_CFG2 for the details of bit fields.
UDB_UDBPAIR2_UDBSNG0_DPATH_CFG3	0x4034244C	Datapath mask enables, shift in, carry in, compare, chaining, MSB configs; FIFO, shift and parallel input control. See UDB_UDBPAIR0_UDBSNG0_DPATH_CFG3 for the details of bit fields.
UDB_UDBPAIR2_UDBSNG0_DPATH_CFG4	0x40342450	Datapath FIFO and register access configuration control. See UDB_UDB-PAIR0_UDBSNG0_DPATH_CFG4 for the details of bit fields.
UDB_UDBPAIR2_UDBSNG0_SC_CFG0	0x40342454	SC Mode 0 and 1 control registers; status register input mode; general SC configuration. See UDB_UDBPAIR0_UDBSNG0_SC_CFG0 for the details of bit fields.
UDB_UDBPAIR2_UDBSNG0_SC_CFG1	0x40342458	SC counter control. See UDB_UDBPAIR0_UDBSNG0_SC_CFG1 for the details of bit fields.
UDB_UDBPAIR2_UDBSNG0_RC_CFG0	0x4034245C	PLD0, PLD1, Datatpath, and SC clock and reset control. See UDB_UDB-PAIR0_UDBSNG0_RC_CFG0 for the details of bit fields.
UDB_UDBPAIR2_UDBSNG0_RC_CFG1	0x40342460	PLD0, PLD1, Datatpath, and SC clock selection, general reset control. See UDB_UDB-PAIR0_UDBSNG0_RC_CFG1 for the details of bit fields.
UDB_UDBPAIR2_UDBSNG0_DPATH_OPC0	0x40342464	Datapath opcode configuration. See UDB_UDBPAIR0_UDBSNG0_DPATH_OPC0 for the details of bit fields.
UDB_UDBPAIR2_UDBSNG0_DPATH_OPC1	0x40342468	Datapath opcode configuration. See UDB_UDBPAIR0_UDBSNG0_DPATH_OPC0 for the details of bit fields.
UDB_UDBPAIR2_UDBSNG0_DPATH_OPC2	0x4034246C	Datapath opcode configuration. See UDB_UDBPAIR0_UDBSNG0_DPATH_OPC0 for the details of bit fields.
UDB_UDBPAIR2_UDBSNG0_DPATH_OPC3	0x40342470	Datapath opcode configuration. See UDB_UDBPAIR0_UDBSNG0_DPATH_OPC0 for the details of bit fields.
UDB_UDBPAIR2_UDBSNG1_PLD_IT0	0x40342480	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR2_UDBSNG1_PLD_IT1	0x40342484	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR2_UDBSNG1_PLD_IT2	0x40342488	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR2_UDBSNG1_PLD_IT3	0x4034248C	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.

Register	Address	Description
UDB_UDBPAIR2_UDBSNG1_PLD_IT4	0x40342490	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR2_UDBSNG1_PLD_IT5	0x40342494	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR2_UDBSNG1_PLD_IT6	0x40342498	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR2_UDBSNG1_PLD_IT7	0x4034249C	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR2_UDBSNG1_PLD_IT8	0x403424A0	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR2_UDBSNG1_PLD_IT9	0x403424A4	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR2_UDBSNG1_PLD_IT10	0x403424A8	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR2_UDBSNG1_PLD_IT11	0x403424AC	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR2_UDBSNG1_PLD_ORT0	0x403424B0	PLD OR Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_ORT0 for the details of bit fields.
UDB_UDBPAIR2_UDBSNG1_PLD_ORT1	0x403424B4	PLD OR Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_ORT1 for the details of bit fields.
UDB_UDBPAIR2_UDBSNG1_PLD_CFG0	0x403424B8	PLD configuration for Carry Enable, Constant, and XOR feedback. See UDB_UDB-PAIR0_UDBSNG0_PLD_CFG0 for the details of bit fields.
UDB_UDBPAIR2_UDBSNG1_PLD_CFG1	0x403424BC	PLD configuration for Set / Reset selection, and Bypass control. See UDB_UDB-PAIR0_UDBSNG0_PLD_CFG1 for the details of bit fields.
UDB_UDBPAIR2_UDBSNG1_DPATH_CFG0	0x403424C0	Datapath input selections (RAD0, RAD1, RAD2, F0_LD, F1_LD, D0_LD, D1_LD). See UDB_UDBPAIR0_UDBSNG0_DPATH_CFG0 for the details of bit fields.
UDB_UDBPAIR2_UDBSNG1_DPATH_CFG1	0x403424C4	Datapath input and output selections (SCI_MUX, SI_MUX, OUT0 thru OUT5). See UDB_UDBPAIR0_UDBSNG0_DPATH_CFG1 for the details of bit fields.
UDB_UDBPAIR2_UDBSNG1_DPATH_CFG2	0x403424C8	Datapath output synchronization, ALU mask, compare 0 and 1 masks. See UDB_UDB-PAIR0_UDBSNG0_DPATH_CFG2 for the details of bit fields.
UDB_UDBPAIR2_UDBSNG1_DPATH_CFG3	0x403424CC	Datapath mask enables, shift in, carry in, compare, chaining, MSB configs; FIFO, shift and parallel input control. See UDB_UDBPAIR0_UDBSNG0_DPATH_CFG3 for the details of bit fields.
UDB_UDBPAIR2_UDBSNG1_DPATH_CFG4	0x403424D0	Datapath FIFO and register access configuration control. See UDB_UDB-PAIR0_UDBSNG0_DPATH_CFG4 for the details of bit fields.
UDB_UDBPAIR2_UDBSNG1_SC_CFG0	0x403424D4	SC Mode 0 and 1 control registers; status register input mode; general SC configuration. See UDB_UDBPAIR0_UDBSNG0_SC_CFG0 for the details of bit fields.
UDB_UDBPAIR2_UDBSNG1_SC_CFG1	0x403424D8	SC counter control. See UDB_UDBPAIR0_UDBSNG0_SC_CFG1 for the details of bit fields.
UDB_UDBPAIR2_UDBSNG1_RC_CFG0	0x403424DC	PLD0, PLD1, Datatpath, and SC clock and reset control. See UDB_UDB-PAIR0_UDBSNG0_RC_CFG0 for the details of bit fields.
UDB_UDBPAIR2_UDBSNG1_RC_CFG1	0x403424E0	PLD0, PLD1, Datatpath, and SC clock selection, general reset control. See UDB_UDB-PAIR0_UDBSNG0_RC_CFG1 for the details of bit fields.
UDB_UDBPAIR2_UDBSNG1_DPATH_OPC0	0x403424E4	Datapath opcode configuration. See UDB_UDBPAIR0_UDBSNG0_DPATH_OPC0 for the details of bit fields.
UDB_UDBPAIR2_UDBSNG1_DPATH_OPC1	0x403424E8	Datapath opcode configuration. See UDB_UDBPAIR0_UDBSNG0_DPATH_OPC0 for the details of bit fields.
UDB_UDBPAIR2_UDBSNG1_DPATH_OPC2	0x403424EC	Datapath opcode configuration. See UDB_UDBPAIR0_UDBSNG0_DPATH_OPC0 for the details of bit fields.
UDB_UDBPAIR2_UDBSNG1_DPATH_OPC3	0x403424F0	Datapath opcode configuration. See UDB_UDBPAIR0_UDBSNG0_DPATH_OPC0 for the details of bit fields.
UDB_UDBPAIR2_ROUTE_TOP_V_BOT	0x40342500	Top Vertical Input (TVI) vs Bottom Vertical Input (BVI) muxing. See UDB_UDB-PAIR0_ROUTE_TOP_V_BOT for the details of bit fields.
UDB_UDBPAIR2_ROUTE_LVO1_V_2	0x40342504	Left Vertical Ouput (LVO) 1 vs 2 muxing for certain horizontals. See UDB_UDB-PAIR0_ROUTE_LVO1_V_2 for the details of bit fields.
UDB_UDBPAIR2_ROUTE_RVO1_V_2	0x40342508	Right Vertical Ouput (RVO) 1 vs 2 muxing for certain horizontals. See UDB_UDB-PAIR0_ROUTE_RVO1_V_2 for the details of bit fields.
UDB_UDBPAIR2_ROUTE_TUI_CFG0	0x4034250C	Top UDB Input (TUI) selection. See UDB_UDBPAIR0_ROUTE_TUI_CFG0 for the details of bit fields.

Register	Address	Description
UDB_UDBPAIR2_ROUTE_TUI_CFG1	0x40342510	Top UDB Input (TUI) selection. See UDB_UDBPAIR0_ROUTE_TUI_CFG1 for the details of bit fields.
UDB_UDBPAIR2_ROUTE_TUI_CFG2	0x40342514	Top UDB Input (TUI) selection. See UDB_UDBPAIR0_ROUTE_TUI_CFG2 for the details of bit fields.
UDB_UDBPAIR2_ROUTE_TUI_CFG3	0x40342518	Top UDB Input (TUI) selection. See UDB_UDBPAIR0_ROUTE_TUI_CFG3 for the details of bit fields.
UDB_UDBPAIR2_ROUTE_TUI_CFG4	0x4034251C	Top UDB Input (TUI) selection. See UDB_UDBPAIR0_ROUTE_TUI_CFG4 for the details of bit fields.
UDB_UDBPAIR2_ROUTE_TUI_CFG5	0x40342520	Top UDB Input (TUI) selection. See UDB_UDBPAIR0_ROUTE_TUI_CFG5 for the details of bit fields.
UDB_UDBPAIR2_ROUTE_BUI_CFG0	0x40342524	Bottom UDB Input (BUI) selection. See UDB_UDBPAIR0_ROUTE_BUI_CFG0 for the details of bit fields.
UDB_UDBPAIR2_ROUTE_BUI_CFG1	0x40342528	Bottom UDB Input (BUI) selection. See UDB_UDBPAIR0_ROUTE_BUI_CFG1 for the details of bit fields.
UDB_UDBPAIR2_ROUTE_BUI_CFG2	0x4034252C	Bottom UDB Input (BUI) selection. See UDB_UDBPAIR0_ROUTE_BUI_CFG2 for the details of bit fields.
UDB_UDBPAIR2_ROUTE_BUI_CFG3	0x40342530	Bottom UDB Input (BUI) selection. See UDB_UDBPAIR0_ROUTE_BUI_CFG3 for the details of bit fields.
UDB_UDBPAIR2_ROUTE_BUI_CFG4	0x40342534	Bottom UDB Input (BUI) selection. See UDB_UDBPAIR0_ROUTE_BUI_CFG4 for the details of bit fields.
UDB_UDBPAIR2_ROUTE_BUI_CFG5	0x40342538	Bottom UDB Input (BUI) selection. See UDB_UDBPAIR0_ROUTE_BUI_CFG5 for the details of bit fields.
UDB_UDBPAIR2_ROUTE_RVO_CFG0	0x4034253C	Right Vertical Ouput (RVO) selection. See UDB_UDBPAIR0_ROUTE_RVO_CFG0 for the details of bit fields.
UDB_UDBPAIR2_ROUTE_RVO_CFG1	0x40342540	Right Vertical Ouput (RVO) selection. See UDB_UDBPAIR0_ROUTE_RVO_CFG1 for the details of bit fields.
UDB_UDBPAIR2_ROUTE_RVO_CFG2	0x40342544	Right Vertical Ouput (RVO) selection. See UDB_UDBPAIR0_ROUTE_RVO_CFG2 for the details of bit fields.
UDB_UDBPAIR2_ROUTE_RVO_CFG3	0x40342548	Right Vertical Ouput (RVO) selection. See UDB_UDBPAIR0_ROUTE_RVO_CFG3 for the details of bit fields.
UDB_UDBPAIR2_ROUTE_LVO_CFG0	0x4034254C	Left Vertical Ouput (LVO) selection. See UDB_UDBPAIR0_ROUTE_LVO_CFG0 for the details of bit fields.
UDB_UDBPAIR2_ROUTE_LVO_CFG1	0x40342550	Left Vertical Ouput (LVO) selection. See UDB_UDBPAIR0_ROUTE_LVO_CFG1 for the details of bit fields.
UDB_UDBPAIR2_ROUTE_RHO_CFG0	0x40342554	Right Horizontal Out (RHO) selection. See UDB_UDBPAIR0_ROUTE_RHO_CFG0 for the details of bit fields.
UDB_UDBPAIR2_ROUTE_RHO_CFG1	0x40342558	Right Horizontal Out (RHO) selection. See UDB_UDBPAIR0_ROUTE_RHO_CFG1 for the details of bit fields.
UDB_UDBPAIR2_ROUTE_RHO_CFG2	0x4034255C	Right Horizontal Out (RHO) selection. See UDB_UDBPAIR0_ROUTE_RHO_CFG2 for the details of bit fields.
UDB_UDBPAIR2_ROUTE_LHO_CFG0	0x40342560	Left Horizontal Out (LHO) selection. See UDB_UDBPAIR0_ROUTE_LHO_CFG0 for the details of bit fields.
UDB_UDBPAIR2_ROUTE_LHO_CFG1	0x40342564	Left Horizontal Out (LHO) selection. See UDB_UDBPAIR0_ROUTE_LHO_CFG1 for the details of bit fields.
UDB_UDBPAIR2_ROUTE_LHO_CFG2	0x40342568	Left Horizontal Out (LHO) selection. See UDB_UDBPAIR0_ROUTE_LHO_CFG2 for the details of bit fields.
UDB_UDBPAIR2_ROUTE_LHO_CFG3	0x4034256C	Left Horizontal Out (LHO) selection. See UDB_UDBPAIR0_ROUTE_LHO_CFG3 for the details of bit fields.
UDB_UDBPAIR2_ROUTE_LHO_CFG4	0x40342570	Left Horizontal Out (LHO) selection. See UDB_UDBPAIR0_ROUTE_LHO_CFG4 for the details of bit fields.
UDB_UDBPAIR2_ROUTE_LHO_CFG5	0x40342574	Left Horizontal Out (LHO) selection. See UDB_UDBPAIR0_ROUTE_LHO_CFG5 for the details of bit fields.
UDB_UDBPAIR2_ROUTE_LHO_CFG6	0x40342578	Left Horizontal Out (LHO) selection. See UDB_UDBPAIR0_ROUTE_LHO_CFG6 for the details of bit fields.
UDB_UDBPAIR2_ROUTE_LHO_CFG7	0x4034257C	Left Horizontal Out (LHO) selection. See UDB_UDBPAIR0_ROUTE_LHO_CFG7 for the details of bit fields.
UDB_UDBPAIR2_ROUTE_LHO_CFG8	0x40342580	Left Horizontal Out (LHO) selection. See UDB_UDBPAIR0_ROUTE_LHO_CFG8 for the details of bit fields.

Register	Address	Description
UDB_UDBPAIR2_ROUTE_LHO_CFG9	0x40342584	Left Horizontal Out (LHO) selection. See UDB_UDBPAIR0_ROUTE_LHO_CFG9 for the details of bit fields.
UDB_UDBPAIR2_ROUTE_LHO_CFG10	0x40342588	Left Horizontal Out (LHO) selection. See UDB_UDBPAIR0_ROUTE_LHO_CFG10 for the details of bit fields.
UDB_UDBPAIR2_ROUTE_LHO_CFG11	0x4034258C	Left Horizontal Out (LHO) selection. See UDB_UDBPAIR0_ROUTE_LHO_CFG11 for the details of bit fields.
UDB_UDBPAIR3_UDBSNG0_PLD_IT0	0x40342600	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR3_UDBSNG0_PLD_IT1	0x40342604	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR3_UDBSNG0_PLD_IT2	0x40342608	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR3_UDBSNG0_PLD_IT3	0x4034260C	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR3_UDBSNG0_PLD_IT4	0x40342610	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR3_UDBSNG0_PLD_IT5	0x40342614	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR3_UDBSNG0_PLD_IT6	0x40342618	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR3_UDBSNG0_PLD_IT7	0x4034261C	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR3_UDBSNG0_PLD_IT8	0x40342620	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR3_UDBSNG0_PLD_IT9	0x40342624	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR3_UDBSNG0_PLD_IT10	0x40342628	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR3_UDBSNG0_PLD_IT11	0x4034262C	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR3_UDBSNG0_PLD_ORT0	0x40342630	PLD OR Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_ORT0 for the details of bit fields.
UDB_UDBPAIR3_UDBSNG0_PLD_ORT1	0x40342634	PLD OR Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_ORT1 for the details of bit fields.
UDB_UDBPAIR3_UDBSNG0_PLD_CFG0	0x40342638	PLD configuration for Carry Enable, Constant, and XOR feedback. See UDB_UDB-PAIR0_UDBSNG0_PLD_CFG0 for the details of bit fields.
UDB_UDBPAIR3_UDBSNG0_PLD_CFG1	0x4034263C	PLD configuration for Set / Reset selection, and Bypass control. See UDB_UDB-PAIR0_UDBSNG0_PLD_CFG1 for the details of bit fields.
UDB_UDBPAIR3_UDBSNG0_DPATH_CFG0	0x40342640	Datapath input selections (RAD0, RAD1, RAD2, F0_LD, F1_LD, D0_LD, D1_LD). See UDB_UDBPAIR0_UDBSNG0_DPATH_CFG0 for the details of bit fields.
UDB_UDBPAIR3_UDBSNG0_DPATH_CFG1	0x40342644	Datapath input and output selections (SCI_MUX, SI_MUX, OUT0 thru OUT5). See UDB_UDBPAIR0_UDBSNG0_DPATH_CFG1 for the details of bit fields.
UDB_UDBPAIR3_UDBSNG0_DPATH_CFG2	0x40342648	Datapath output synchronization, ALU mask, compare 0 and 1 masks. See UDB_UDB-PAIR0_UDBSNG0_DPATH_CFG2 for the details of bit fields.
UDB_UDBPAIR3_UDBSNG0_DPATH_CFG3	0x4034264C	Datapath mask enables, shift in, carry in, compare, chaining, MSB configs; FIFO, shift and parallel input control. See UDB_UDBPAIR0_UDBSNG0_DPATH_CFG3 for the details of bit fields.
UDB_UDBPAIR3_UDBSNG0_DPATH_CFG4	0x40342650	Datapath FIFO and register access configuration control. See UDB_UDB-PAIR0_UDBSNG0_DPATH_CFG4 for the details of bit fields.
UDB_UDBPAIR3_UDBSNG0_SC_CFG0	0x40342654	SC Mode 0 and 1 control registers; status register input mode; general SC configuration. See UDB_UDBPAIR0_UDBSNG0_SC_CFG0 for the details of bit fields.
UDB_UDBPAIR3_UDBSNG0_SC_CFG1	0x40342658	SC counter control. See UDB_UDBPAIR0_UDBSNG0_SC_CFG1 for the details of bit fields.
UDB_UDBPAIR3_UDBSNG0_RC_CFG0	0x4034265C	PLD0, PLD1, Datatpath, and SC clock and reset control. See UDB_UDB-PAIR0_UDBSNG0_RC_CFG0 for the details of bit fields.
UDB_UDBPAIR3_UDBSNG0_RC_CFG1	0x40342660	PLD0, PLD1, Datatpath, and SC clock selection, general reset control. See UDB_UDB-PAIR0_UDBSNG0_RC_CFG1 for the details of bit fields.
UDB_UDBPAIR3_UDBSNG0_DPATH_OPC0	0x40342664	Datapath opcode configuration. See UDB_UDBPAIR0_UDBSNG0_DPATH_OPC0 for the details of bit fields.

Register	Address	Description
UDB_UDBPAIR3_UDBSNG0_DPATH_OPC1	0x40342668	Datapath opcode configuration. See UDB_UDBPAIR0_UDBSNG0_DPATH_OPC0 for the details of bit fields.
UDB_UDBPAIR3_UDBSNG0_DPATH_OPC2	0x4034266C	Datapath opcode configuration. See UDB_UDBPAIR0_UDBSNG0_DPATH_OPC0 for the details of bit fields.
UDB_UDBPAIR3_UDBSNG0_DPATH_OPC3	0x40342670	Datapath opcode configuration. See UDB_UDBPAIR0_UDBSNG0_DPATH_OPC0 for the details of bit fields.
UDB_UDBPAIR3_UDBSNG1_PLD_IT0	0x40342680	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR3_UDBSNG1_PLD_IT1	0x40342684	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR3_UDBSNG1_PLD_IT2	0x40342688	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR3_UDBSNG1_PLD_IT3	0x4034268C	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR3_UDBSNG1_PLD_IT4	0x40342690	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR3_UDBSNG1_PLD_IT5	0x40342694	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR3_UDBSNG1_PLD_IT6	0x40342698	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR3_UDBSNG1_PLD_IT7	0x4034269C	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR3_UDBSNG1_PLD_IT8	0x403426A0	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR3_UDBSNG1_PLD_IT9	0x403426A4	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR3_UDBSNG1_PLD_IT10	0x403426A8	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR3_UDBSNG1_PLD_IT11	0x403426AC	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR3_UDBSNG1_PLD_ORT0	0x403426B0	PLD OR Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_ORT0 for the details of bit fields.
UDB_UDBPAIR3_UDBSNG1_PLD_ORT1	0x403426B4	PLD OR Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_ORT1 for the details of bit fields.
UDB_UDBPAIR3_UDBSNG1_PLD_CFG0	0x403426B8	PLD configuration for Carry Enable, Constant, and XOR feedback. See UDB_UDB-PAIR0_UDBSNG0_PLD_CFG0 for the details of bit fields.
UDB_UDBPAIR3_UDBSNG1_PLD_CFG1	0x403426BC	PLD configuration for Set / Reset selection, and Bypass control. See UDB_UDB-PAIR0_UDBSNG0_PLD_CFG1 for the details of bit fields.
UDB_UDBPAIR3_UDBSNG1_DPATH_CFG0	0x403426C0	Datapath input selections (RAD0, RAD1, RAD2, F0_LD, F1_LD, D0_LD, D1_LD). See UDB_UDBPAIR0_UDBSNG0_DPATH_CFG0 for the details of bit fields.
UDB_UDBPAIR3_UDBSNG1_DPATH_CFG1	0x403426C4	Datapath input and output selections (SCI_MUX, SI_MUX, OUT0 thru OUT5). See UDB_UDBPAIR0_UDBSNG0_DPATH_CFG1 for the details of bit fields.
UDB_UDBPAIR3_UDBSNG1_DPATH_CFG2	0x403426C8	Datapath output synchronization, ALU mask, compare 0 and 1 masks. See UDB_UDB-PAIR0_UDBSNG0_DPATH_CFG2 for the details of bit fields.
UDB_UDBPAIR3_UDBSNG1_DPATH_CFG3	0x403426CC	Datapath mask enables, shift in, carry in, compare, chaining, MSB configs; FIFO, shift and parallel input control. See UDB_UDBPAIR0_UDBSNG0_DPATH_CFG3 for the details of bit fields.
UDB_UDBPAIR3_UDBSNG1_DPATH_CFG4	0x403426D0	Datapath FIFO and register access configuration control. See UDB_UDB-PAIR0_UDBSNG0_DPATH_CFG4 for the details of bit fields.
UDB_UDBPAIR3_UDBSNG1_SC_CFG0	0x403426D4	SC Mode 0 and 1 control registers; status register input mode; general SC configuration. See UDB_UDBPAIR0_UDBSNG0_SC_CFG0 for the details of bit fields.
UDB_UDBPAIR3_UDBSNG1_SC_CFG1	0x403426D8	SC counter control. See UDB_UDBPAIR0_UDBSNG0_SC_CFG1 for the details of bit fields.
UDB_UDBPAIR3_UDBSNG1_RC_CFG0	0x403426DC	PLD0, PLD1, Datatpath, and SC clock and reset control. See UDB_UDB-PAIR0_UDBSNG0_RC_CFG0 for the details of bit fields.
UDB_UDBPAIR3_UDBSNG1_RC_CFG1	0x403426E0	PLD0, PLD1, Datatpath, and SC clock selection, general reset control. See UDB_UDB-PAIR0_UDBSNG0_RC_CFG1 for the details of bit fields.
UDB_UDBPAIR3_UDBSNG1_DPATH_OPC0	0x403426E4	Datapath opcode configuration. See UDB_UDBPAIR0_UDBSNG0_DPATH_OPC0 for the details of bit fields.

Register	Address	Description
UDB_UDBPAIR3_UDBSNG1_DPATH_OPC1	0x403426E8	Datapath opcode configuration. See UDB_UDBPAIR0_UDBSNG0_DPATH_OPC0 for the details of bit fields.
UDB_UDBPAIR3_UDBSNG1_DPATH_OPC2	0x403426EC	Datapath opcode configuration. See UDB_UDBPAIR0_UDBSNG0_DPATH_OPC0 for the details of bit fields.
UDB_UDBPAIR3_UDBSNG1_DPATH_OPC3	0x403426F0	Datapath opcode configuration. See UDB_UDBPAIR0_UDBSNG0_DPATH_OPC0 for the details of bit fields.
UDB_UDBPAIR3_ROUTE_TOP_V_BOT	0x40342700	Top Vertical Input (TVI) vs Bottom Vertical Input (BVI) muxing. See UDB_UDB-PAIR0_ROUTE_TOP_V_BOT for the details of bit fields.
UDB_UDBPAIR3_ROUTE_LVO1_V_2	0x40342704	Left Vertical Ouput (LVO) 1 vs 2 muxing for certain horizontals. See UDB_UDB-PAIR0_ROUTE_LVO1_V_2 for the details of bit fields.
UDB_UDBPAIR3_ROUTE_RVO1_V_2	0x40342708	Right Vertical Ouput (RVO) 1 vs 2 muxing for certain horizontals. See UDB_UDB-PAIR0_ROUTE_RVO1_V_2 for the details of bit fields.
UDB_UDBPAIR3_ROUTE_TUI_CFG0	0x4034270C	Top UDB Input (TUI) selection. See UDB_UDBPAIR0_ROUTE_TUI_CFG0 for the details of bit fields.
UDB_UDBPAIR3_ROUTE_TUI_CFG1	0x40342710	Top UDB Input (TUI) selection. See UDB_UDBPAIR0_ROUTE_TUI_CFG1 for the details of bit fields.
UDB_UDBPAIR3_ROUTE_TUI_CFG2	0x40342714	Top UDB Input (TUI) selection. See UDB_UDBPAIR0_ROUTE_TUI_CFG2 for the details of bit fields.
UDB_UDBPAIR3_ROUTE_TUI_CFG3	0x40342718	Top UDB Input (TUI) selection. See UDB_UDBPAIR0_ROUTE_TUI_CFG3 for the details of bit fields.
UDB_UDBPAIR3_ROUTE_TUI_CFG4	0x4034271C	Top UDB Input (TUI) selection. See UDB_UDBPAIR0_ROUTE_TUI_CFG4 for the details of bit fields.
UDB_UDBPAIR3_ROUTE_TUI_CFG5	0x40342720	Top UDB Input (TUI) selection. See UDB_UDBPAIR0_ROUTE_TUI_CFG5 for the details of bit fields.
UDB_UDBPAIR3_ROUTE_BUI_CFG0	0x40342724	Bottom UDB Input (BUI) selection. See UDB_UDBPAIR0_ROUTE_BUI_CFG0 for the details of bit fields.
UDB_UDBPAIR3_ROUTE_BUI_CFG1	0x40342728	Bottom UDB Input (BUI) selection. See UDB_UDBPAIR0_ROUTE_BUI_CFG1 for the details of bit fields.
UDB_UDBPAIR3_ROUTE_BUI_CFG2	0x4034272C	Bottom UDB Input (BUI) selection. See UDB_UDBPAIR0_ROUTE_BUI_CFG2 for the details of bit fields.
UDB_UDBPAIR3_ROUTE_BUI_CFG3	0x40342730	Bottom UDB Input (BUI) selection. See UDB_UDBPAIR0_ROUTE_BUI_CFG3 for the details of bit fields.
UDB_UDBPAIR3_ROUTE_BUI_CFG4	0x40342734	Bottom UDB Input (BUI) selection. See UDB_UDBPAIR0_ROUTE_BUI_CFG4 for the details of bit fields.
UDB_UDBPAIR3_ROUTE_BUI_CFG5	0x40342738	Bottom UDB Input (BUI) selection. See UDB_UDBPAIR0_ROUTE_BUI_CFG5 for the details of bit fields.
UDB_UDBPAIR3_ROUTE_RVO_CFG0	0x4034273C	Right Vertical Ouput (RVO) selection. See UDB_UDBPAIR0_ROUTE_RVO_CFG0 for the details of bit fields.
UDB_UDBPAIR3_ROUTE_RVO_CFG1	0x40342740	Right Vertical Ouput (RVO) selection. See UDB_UDBPAIR0_ROUTE_RVO_CFG1 for the details of bit fields.
UDB_UDBPAIR3_ROUTE_RVO_CFG2	0x40342744	Right Vertical Ouput (RVO) selection. See UDB_UDBPAIR0_ROUTE_RVO_CFG2 for the details of bit fields.
UDB_UDBPAIR3_ROUTE_RVO_CFG3	0x40342748	Right Vertical Ouput (RVO) selection. See UDB_UDBPAIR0_ROUTE_RVO_CFG3 for the details of bit fields.
UDB_UDBPAIR3_ROUTE_LVO_CFG0	0x4034274C	Left Vertical Ouput (LVO) selection. See UDB_UDBPAIR0_ROUTE_LVO_CFG0 for the details of bit fields.
UDB_UDBPAIR3_ROUTE_LVO_CFG1	0x40342750	Left Vertical Ouput (LVO) selection. See UDB_UDBPAIR0_ROUTE_LVO_CFG1 for the details of bit fields.
UDB_UDBPAIR3_ROUTE_RHO_CFG0	0x40342754	Right Horizontal Out (RHO) selection. See UDB_UDBPAIR0_ROUTE_RHO_CFG0 for the details of bit fields.
UDB_UDBPAIR3_ROUTE_RHO_CFG1	0x40342758	Right Horizontal Out (RHO) selection. See UDB_UDBPAIR0_ROUTE_RHO_CFG1 for the details of bit fields.
UDB_UDBPAIR3_ROUTE_RHO_CFG2	0x4034275C	Right Horizontal Out (RHO) selection. See UDB_UDBPAIR0_ROUTE_RHO_CFG2 for the details of bit fields.
UDB_UDBPAIR3_ROUTE_LHO_CFG0	0x40342760	Left Horizontal Out (LHO) selection. See UDB_UDBPAIR0_ROUTE_LHO_CFG0 for the details of bit fields.
UDB_UDBPAIR3_ROUTE_LHO_CFG1	0x40342764	Left Horizontal Out (LHO) selection. See UDB_UDBPAIR0_ROUTE_LHO_CFG1 for the details of bit fields.

Register	Address	Description
UDB_UDBPAIR3_ROUTE_LHO_CFG2	0x40342768	Left Horizontal Out (LHO) selection. See UDB_UDBPAIR0_ROUTE_LHO_CFG2 for the details of bit fields.
UDB_UDBPAIR3_ROUTE_LHO_CFG3	0x4034276C	Left Horizontal Out (LHO) selection. See UDB_UDBPAIR0_ROUTE_LHO_CFG3 for the details of bit fields.
UDB_UDBPAIR3_ROUTE_LHO_CFG4	0x40342770	Left Horizontal Out (LHO) selection. See UDB_UDBPAIR0_ROUTE_LHO_CFG4 for the details of bit fields.
UDB_UDBPAIR3_ROUTE_LHO_CFG5	0x40342774	Left Horizontal Out (LHO) selection. See UDB_UDBPAIR0_ROUTE_LHO_CFG5 for the details of bit fields.
UDB_UDBPAIR3_ROUTE_LHO_CFG6	0x40342778	Left Horizontal Out (LHO) selection. See UDB_UDBPAIR0_ROUTE_LHO_CFG6 for the details of bit fields.
UDB_UDBPAIR3_ROUTE_LHO_CFG7	0x4034277C	Left Horizontal Out (LHO) selection. See UDB_UDBPAIR0_ROUTE_LHO_CFG7 for the details of bit fields.
UDB_UDBPAIR3_ROUTE_LHO_CFG8	0x40342780	Left Horizontal Out (LHO) selection. See UDB_UDBPAIR0_ROUTE_LHO_CFG8 for the details of bit fields.
UDB_UDBPAIR3_ROUTE_LHO_CFG9	0x40342784	Left Horizontal Out (LHO) selection. See UDB_UDBPAIR0_ROUTE_LHO_CFG9 for the details of bit fields.
UDB_UDBPAIR3_ROUTE_LHO_CFG10	0x40342788	Left Horizontal Out (LHO) selection. See UDB_UDBPAIR0_ROUTE_LHO_CFG10 for the details of bit fields.
UDB_UDBPAIR3_ROUTE_LHO_CFG11	0x4034278C	Left Horizontal Out (LHO) selection. See UDB_UDBPAIR0_ROUTE_LHO_CFG11 for the details of bit fields.
UDB_UDBPAIR4_UDBSNG0_PLD_IT0	0x40342800	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR4_UDBSNG0_PLD_IT1	0x40342804	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR4_UDBSNG0_PLD_IT2	0x40342808	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR4_UDBSNG0_PLD_IT3	0x4034280C	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR4_UDBSNG0_PLD_IT4	0x40342810	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR4_UDBSNG0_PLD_IT5	0x40342814	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR4_UDBSNG0_PLD_IT6	0x40342818	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR4_UDBSNG0_PLD_IT7	0x4034281C	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR4_UDBSNG0_PLD_IT8	0x40342820	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR4_UDBSNG0_PLD_IT9	0x40342824	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR4_UDBSNG0_PLD_IT10	0x40342828	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR4_UDBSNG0_PLD_IT11	0x4034282C	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR4_UDBSNG0_PLD_ORT0	0x40342830	PLD OR Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_ORT0 for the details of bit fields.
UDB_UDBPAIR4_UDBSNG0_PLD_ORT1	0x40342834	PLD OR Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_ORT1 for the details of bit fields.
UDB_UDBPAIR4_UDBSNG0_PLD_CFG0	0x40342838	PLD configuration for Carry Enable, Constant, and XOR feedback. See UDB_UDB-PAIR0_UDBSNG0_PLD_CFG0 for the details of bit fields.
UDB_UDBPAIR4_UDBSNG0_PLD_CFG1	0x4034283C	PLD configuration for Set / Reset selection, and Bypass control. See UDB_UDB-PAIR0_UDBSNG0_PLD_CFG1 for the details of bit fields.
UDB_UDBPAIR4_UDBSNG0_DPATH_CFG0	0x40342840	Datapath input selections (RAD0, RAD1, RAD2, F0_LD, F1_LD, D0_LD, D1_LD). See UDB_UDBPAIR0_UDBSNG0_DPATH_CFG0 for the details of bit fields.
UDB_UDBPAIR4_UDBSNG0_DPATH_CFG1	0x40342844	Datapath input and output selections (SCI_MUX, SI_MUX, OUT0 thru OUT5). See UDB_UDBPAIR0_UDBSNG0_DPATH_CFG1 for the details of bit fields.
UDB_UDBPAIR4_UDBSNG0_DPATH_CFG2	0x40342848	Datapath output synchronization, ALU mask, compare 0 and 1 masks. See UDB_UDB-PAIR0_UDBSNG0_DPATH_CFG2 for the details of bit fields.

Register	Address	Description
UDB_UDBPAIR4_UDBSNG0_DPATH_CFG3	0x4034284C	Datapath mask enables, shift in, carry in, compare, chaining, MSB configs; FIFO, shift and parallel input control. See UDB_UDBPAIR0_UDBSNG0_DPATH_CFG3 for the details of bit fields.
UDB_UDBPAIR4_UDBSNG0_DPATH_CFG4	0x40342850	Datapath FIFO and register access configuration control. See UDB_UDB-PAIR0_UDBSNG0_DPATH_CFG4 for the details of bit fields.
UDB_UDBPAIR4_UDBSNG0_SC_CFG0	0x40342854	SC Mode 0 and 1 control registers; status register input mode; general SC configuration. See UDB_UDBPAIR0_UDBSNG0_SC_CFG0 for the details of bit fields.
UDB_UDBPAIR4_UDBSNG0_SC_CFG1	0x40342858	SC counter control. See UDB_UDBPAIR0_UDBSNG0_SC_CFG1 for the details of bit fields.
UDB_UDBPAIR4_UDBSNG0_RC_CFG0	0x4034285C	PLD0, PLD1, Datatpath, and SC clock and reset control. See UDB_UDB-PAIR0_UDBSNG0_RC_CFG0 for the details of bit fields.
UDB_UDBPAIR4_UDBSNG0_RC_CFG1	0x40342860	PLD0, PLD1, Datatpath, and SC clock selection, general reset control. See UDB_UDB-PAIR0_UDBSNG0_RC_CFG1 for the details of bit fields.
UDB_UDBPAIR4_UDBSNG0_DPATH_OPC0	0x40342864	Datapath opcode configuration. See UDB_UDBPAIR0_UDBSNG0_DPATH_OPC0 for the details of bit fields.
UDB_UDBPAIR4_UDBSNG0_DPATH_OPC1	0x40342868	Datapath opcode configuration. See UDB_UDBPAIR0_UDBSNG0_DPATH_OPC0 for the details of bit fields.
UDB_UDBPAIR4_UDBSNG0_DPATH_OPC2	0x4034286C	Datapath opcode configuration. See UDB_UDBPAIR0_UDBSNG0_DPATH_OPC0 for the details of bit fields.
UDB_UDBPAIR4_UDBSNG0_DPATH_OPC3	0x40342870	Datapath opcode configuration. See UDB_UDBPAIR0_UDBSNG0_DPATH_OPC0 for the details of bit fields.
UDB_UDBPAIR4_UDBSNG1_PLD_IT0	0x40342880	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR4_UDBSNG1_PLD_IT1	0x40342884	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR4_UDBSNG1_PLD_IT2	0x40342888	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR4_UDBSNG1_PLD_IT3	0x4034288C	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR4_UDBSNG1_PLD_IT4	0x40342890	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR4_UDBSNG1_PLD_IT5	0x40342894	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR4_UDBSNG1_PLD_IT6	0x40342898	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR4_UDBSNG1_PLD_IT7	0x4034289C	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR4_UDBSNG1_PLD_IT8	0x403428A0	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR4_UDBSNG1_PLD_IT9	0x403428A4	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR4_UDBSNG1_PLD_IT10	0x403428A8	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR4_UDBSNG1_PLD_IT11	0x403428AC	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR4_UDBSNG1_PLD_ORT0	0x403428B0	PLD OR Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_ORT0 for the details of bit fields.
UDB_UDBPAIR4_UDBSNG1_PLD_ORT1	0x403428B4	PLD OR Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_ORT1 for the details of bit fields.
UDB_UDBPAIR4_UDBSNG1_PLD_CFG0	0x403428B8	PLD configuration for Carry Enable, Constant, and XOR feedback. See UDB_UDB-PAIR0_UDBSNG0_PLD_CFG0 for the details of bit fields.
UDB_UDBPAIR4_UDBSNG1_PLD_CFG1	0x403428BC	PLD configuration for Set / Reset selection, and Bypass control. See UDB_UDB-PAIR0_UDBSNG0_PLD_CFG1 for the details of bit fields.
UDB_UDBPAIR4_UDBSNG1_DPATH_CFG0	0x403428C0	Datapath input selections (RAD0, RAD1, RAD2, F0_LD, F1_LD, D0_LD, D1_LD). See UDB_UDBPAIR0_UDBSNG0_DPATH_CFG0 for the details of bit fields.
UDB_UDBPAIR4_UDBSNG1_DPATH_CFG1	0x403428C4	Datapath input and output selections (SCI_MUX, SI_MUX, OUT0 thru OUT5). See UDB_UDBPAIR0_UDBSNG0_DPATH_CFG1 for the details of bit fields.
UDB_UDBPAIR4_UDBSNG1_DPATH_CFG2	0x403428C8	Datapath output synchronization, ALU mask, compare 0 and 1 masks. See UDB_UDB-PAIR0_UDBSNG0_DPATH_CFG2 for the details of bit fields.

Register	Address	Description
UDB_UDBPAIR4_UDBSNG1_DPATH_CFG3	0x403428CC	Datapath mask enables, shift in, carry in, compare, chaining, MSB configs; FIFO, shift and parallel input control. See UDB_UDBPAIR0_UDBSNG0_DPATH_CFG3 for the details of bit fields.
UDB_UDBPAIR4_UDBSNG1_DPATH_CFG4	0x403428D0	Datapath FIFO and register access configuration control. See UDB_UDBPAIR0_UDBSNG0_DPATH_CFG4 for the details of bit fields.
UDB_UDBPAIR4_UDBSNG1_SC_CFG0	0x403428D4	SC Mode 0 and 1 control registers; status register input mode; general SC configuration. See UDB_UDBPAIR0_UDBSNG0_SC_CFG0 for the details of bit fields.
UDB_UDBPAIR4_UDBSNG1_SC_CFG1	0x403428D8	SC counter control. See UDB_UDBPAIR0_UDBSNG0_SC_CFG1 for the details of bit fields.
UDB_UDBPAIR4_UDBSNG1_RC_CFG0	0x403428DC	PLD0, PLD1, Datatpath, and SC clock and reset control. See UDB_UDBPAIR0_UDBSNG0_RC_CFG0 for the details of bit fields.
UDB_UDBPAIR4_UDBSNG1_RC_CFG1	0x403428E0	PLD0, PLD1, Datatpath, and SC clock selection, general reset control. See UDB_UDBPAIR0_UDBSNG0_RC_CFG1 for the details of bit fields.
UDB_UDBPAIR4_UDBSNG1_DPATH_OPC0	0x403428E4	Datapath opcode configuration. See UDB_UDBPAIR0_UDBSNG0_DPATH_OPC0 for the details of bit fields.
UDB_UDBPAIR4_UDBSNG1_DPATH_OPC1	0x403428E8	Datapath opcode configuration. See UDB_UDBPAIR0_UDBSNG0_DPATH_OPC0 for the details of bit fields.
UDB_UDBPAIR4_UDBSNG1_DPATH_OPC2	0x403428EC	Datapath opcode configuration. See UDB_UDBPAIR0_UDBSNG0_DPATH_OPC0 for the details of bit fields.
UDB_UDBPAIR4_UDBSNG1_DPATH_OPC3	0x403428F0	Datapath opcode configuration. See UDB_UDBPAIR0_UDBSNG0_DPATH_OPC0 for the details of bit fields.
UDB_UDBPAIR4_ROUTE_TOP_V_BOT	0x40342900	Top Vertical Input (TVI) vs Bottom Vertical Input (BVI) muxing. See UDB_UDBPAIR0_ROUTE_TOP_V_BOT for the details of bit fields.
UDB_UDBPAIR4_ROUTE_LVO1_V_2	0x40342904	Left Vertical Ouput (LVO) 1 vs 2 muxing for certain horizontals. See UDB_UDBPAIR0_ROUTE_LVO1_V_2 for the details of bit fields.
UDB_UDBPAIR4_ROUTE_RVO1_V_2	0x40342908	Right Vertical Ouput (RVO) 1 vs 2 muxing for certain horizontals. See UDB_UDBPAIR0_ROUTE_RVO1_V_2 for the details of bit fields.
UDB_UDBPAIR4_ROUTE_TUI_CFG0	0x4034290C	Top UDB Input (TUI) selection. See UDB_UDBPAIR0_ROUTE_TUI_CFG0 for the details of bit fields.
UDB_UDBPAIR4_ROUTE_TUI_CFG1	0x40342910	Top UDB Input (TUI) selection. See UDB_UDBPAIR0_ROUTE_TUI_CFG1 for the details of bit fields.
UDB_UDBPAIR4_ROUTE_TUI_CFG2	0x40342914	Top UDB Input (TUI) selection. See UDB_UDBPAIR0_ROUTE_TUI_CFG2 for the details of bit fields.
UDB_UDBPAIR4_ROUTE_TUI_CFG3	0x40342918	Top UDB Input (TUI) selection. See UDB_UDBPAIR0_ROUTE_TUI_CFG3 for the details of bit fields.
UDB_UDBPAIR4_ROUTE_TUI_CFG4	0x4034291C	Top UDB Input (TUI) selection. See UDB_UDBPAIR0_ROUTE_TUI_CFG4 for the details of bit fields.
UDB_UDBPAIR4_ROUTE_TUI_CFG5	0x40342920	Top UDB Input (TUI) selection. See UDB_UDBPAIR0_ROUTE_TUI_CFG5 for the details of bit fields.
UDB_UDBPAIR4_ROUTE_BUI_CFG0	0x40342924	Bottom UDB Input (BUI) selection. See UDB_UDBPAIR0_ROUTE_BUI_CFG0 for the details of bit fields.
UDB_UDBPAIR4_ROUTE_BUI_CFG1	0x40342928	Bottom UDB Input (BUI) selection. See UDB_UDBPAIR0_ROUTE_BUI_CFG1 for the details of bit fields.
UDB_UDBPAIR4_ROUTE_BUI_CFG2	0x4034292C	Bottom UDB Input (BUI) selection. See UDB_UDBPAIR0_ROUTE_BUI_CFG2 for the details of bit fields.
UDB_UDBPAIR4_ROUTE_BUI_CFG3	0x40342930	Bottom UDB Input (BUI) selection. See UDB_UDBPAIR0_ROUTE_BUI_CFG3 for the details of bit fields.
UDB_UDBPAIR4_ROUTE_BUI_CFG4	0x40342934	Bottom UDB Input (BUI) selection. See UDB_UDBPAIR0_ROUTE_BUI_CFG4 for the details of bit fields.
UDB_UDBPAIR4_ROUTE_BUI_CFG5	0x40342938	Bottom UDB Input (BUI) selection. See UDB_UDBPAIR0_ROUTE_BUI_CFG5 for the details of bit fields.
UDB_UDBPAIR4_ROUTE_RVO_CFG0	0x4034293C	Right Vertical Ouput (RVO) selection. See UDB_UDBPAIR0_ROUTE_RVO_CFG0 for the details of bit fields.
UDB_UDBPAIR4_ROUTE_RVO_CFG1	0x40342940	Right Vertical Ouput (RVO) selection. See UDB_UDBPAIR0_ROUTE_RVO_CFG1 for the details of bit fields.
UDB_UDBPAIR4_ROUTE_RVO_CFG2	0x40342944	Right Vertical Ouput (RVO) selection. See UDB_UDBPAIR0_ROUTE_RVO_CFG2 for the details of bit fields.
UDB_UDBPAIR4_ROUTE_RVO_CFG3	0x40342948	Right Vertical Ouput (RVO) selection. See UDB_UDBPAIR0_ROUTE_RVO_CFG3 for the details of bit fields.

Register	Address	Description
UDB_UDBPAIR4_ROUTE_LVO_CFG0	0x4034294C	Left Vertical Ouput (LVO) selection. See UDB_UDBPAIR0_ROUTE_LVO_CFG0 for the details of bit fields.
UDB_UDBPAIR4_ROUTE_LVO_CFG1	0x40342950	Left Vertical Ouput (LVO) selection. See UDB_UDBPAIR0_ROUTE_LVO_CFG1 for the details of bit fields.
UDB_UDBPAIR4_ROUTE_RHO_CFG0	0x40342954	Right Horizontal Out (RHO) selection. See UDB_UDBPAIR0_ROUTE_RHO_CFG0 for the details of bit fields.
UDB_UDBPAIR4_ROUTE_RHO_CFG1	0x40342958	Right Horizontal Out (RHO) selection. See UDB_UDBPAIR0_ROUTE_RHO_CFG1 for the details of bit fields.
UDB_UDBPAIR4_ROUTE_RHO_CFG2	0x4034295C	Right Horizontal Out (RHO) selection. See UDB_UDBPAIR0_ROUTE_RHO_CFG2 for the details of bit fields.
UDB_UDBPAIR4_ROUTE_LHO_CFG0	0x40342960	Left Horizontal Out (LHO) selection. See UDB_UDBPAIR0_ROUTE_LHO_CFG0 for the details of bit fields.
UDB_UDBPAIR4_ROUTE_LHO_CFG1	0x40342964	Left Horizontal Out (LHO) selection. See UDB_UDBPAIR0_ROUTE_LHO_CFG1 for the details of bit fields.
UDB_UDBPAIR4_ROUTE_LHO_CFG2	0x40342968	Left Horizontal Out (LHO) selection. See UDB_UDBPAIR0_ROUTE_LHO_CFG2 for the details of bit fields.
UDB_UDBPAIR4_ROUTE_LHO_CFG3	0x4034296C	Left Horizontal Out (LHO) selection. See UDB_UDBPAIR0_ROUTE_LHO_CFG3 for the details of bit fields.
UDB_UDBPAIR4_ROUTE_LHO_CFG4	0x40342970	Left Horizontal Out (LHO) selection. See UDB_UDBPAIR0_ROUTE_LHO_CFG4 for the details of bit fields.
UDB_UDBPAIR4_ROUTE_LHO_CFG5	0x40342974	Left Horizontal Out (LHO) selection. See UDB_UDBPAIR0_ROUTE_LHO_CFG5 for the details of bit fields.
UDB_UDBPAIR4_ROUTE_LHO_CFG6	0x40342978	Left Horizontal Out (LHO) selection. See UDB_UDBPAIR0_ROUTE_LHO_CFG6 for the details of bit fields.
UDB_UDBPAIR4_ROUTE_LHO_CFG7	0x4034297C	Left Horizontal Out (LHO) selection. See UDB_UDBPAIR0_ROUTE_LHO_CFG7 for the details of bit fields.
UDB_UDBPAIR4_ROUTE_LHO_CFG8	0x40342980	Left Horizontal Out (LHO) selection. See UDB_UDBPAIR0_ROUTE_LHO_CFG8 for the details of bit fields.
UDB_UDBPAIR4_ROUTE_LHO_CFG9	0x40342984	Left Horizontal Out (LHO) selection. See UDB_UDBPAIR0_ROUTE_LHO_CFG9 for the details of bit fields.
UDB_UDBPAIR4_ROUTE_LHO_CFG10	0x40342988	Left Horizontal Out (LHO) selection. See UDB_UDBPAIR0_ROUTE_LHO_CFG10 for the details of bit fields.
UDB_UDBPAIR4_ROUTE_LHO_CFG11	0x4034298C	Left Horizontal Out (LHO) selection. See UDB_UDBPAIR0_ROUTE_LHO_CFG11 for the details of bit fields.
UDB_UDBPAIR5_UDBSNG0_PLD_IT0	0x40342A00	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR5_UDBSNG0_PLD_IT1	0x40342A04	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR5_UDBSNG0_PLD_IT2	0x40342A08	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR5_UDBSNG0_PLD_IT3	0x40342A0C	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR5_UDBSNG0_PLD_IT4	0x40342A10	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR5_UDBSNG0_PLD_IT5	0x40342A14	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR5_UDBSNG0_PLD_IT6	0x40342A18	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR5_UDBSNG0_PLD_IT7	0x40342A1C	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR5_UDBSNG0_PLD_IT8	0x40342A20	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR5_UDBSNG0_PLD_IT9	0x40342A24	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR5_UDBSNG0_PLD_IT10	0x40342A28	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR5_UDBSNG0_PLD_IT11	0x40342A2C	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.

Register	Address	Description
UDB_UDBPAIR5_UDBSNG0_PLD_ORT0	0x40342A30	PLD OR Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_ORT0 for the details of bit fields.
UDB_UDBPAIR5_UDBSNG0_PLD_ORT1	0x40342A34	PLD OR Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_ORT1 for the details of bit fields.
UDB_UDBPAIR5_UDBSNG0_PLD_CFG0	0x40342A38	PLD configuration for Carry Enable, Constant, and XOR feedback. See UDB_UDB-PAIR0_UDBSNG0_PLD_CFG0 for the details of bit fields.
UDB_UDBPAIR5_UDBSNG0_PLD_CFG1	0x40342A3C	PLD configuration for Set / Reset selection, and Bypass control. See UDB_UDB-PAIR0_UDBSNG0_PLD_CFG1 for the details of bit fields.
UDB_UDBPAIR5_UDBSNG0_DPATH_CFG0	0x40342A40	Datapath input selections (RAD0, RAD1, RAD2, F0_LD, F1_LD, D0_LD, D1_LD). See UDB_UDBPAIR0_UDBSNG0_DPATH_CFG0 for the details of bit fields.
UDB_UDBPAIR5_UDBSNG0_DPATH_CFG1	0x40342A44	Datapath input and output selections (SCI_MUX, SI_MUX, OUT0 thru OUT5). See UDB_UDBPAIR0_UDBSNG0_DPATH_CFG1 for the details of bit fields.
UDB_UDBPAIR5_UDBSNG0_DPATH_CFG2	0x40342A48	Datapath output synchronization, ALU mask, compare 0 and 1 masks. See UDB_UDB-PAIR0_UDBSNG0_DPATH_CFG2 for the details of bit fields.
UDB_UDBPAIR5_UDBSNG0_DPATH_CFG3	0x40342A4C	Datapath mask enables, shift in, carry in, compare, chaining, MSB configs; FIFO, shift and parallel input control. See UDB_UDBPAIR0_UDBSNG0_DPATH_CFG3 for the details of bit fields.
UDB_UDBPAIR5_UDBSNG0_DPATH_CFG4	0x40342A50	Datapath FIFO and register access configuration control. See UDB_UDB-PAIR0_UDBSNG0_DPATH_CFG4 for the details of bit fields.
UDB_UDBPAIR5_UDBSNG0_SC_CFG0	0x40342A54	SC Mode 0 and 1 control registers; status register input mode; general SC configuration. See UDB_UDBPAIR0_UDBSNG0_SC_CFG0 for the details of bit fields.
UDB_UDBPAIR5_UDBSNG0_SC_CFG1	0x40342A58	SC counter control. See UDB_UDBPAIR0_UDBSNG0_SC_CFG1 for the details of bit fields.
UDB_UDBPAIR5_UDBSNG0_RC_CFG0	0x40342A5C	PLD0, PLD1, Datatpath, and SC clock and reset control. See UDB_UDB-PAIR0_UDBSNG0_RC_CFG0 for the details of bit fields.
UDB_UDBPAIR5_UDBSNG0_RC_CFG1	0x40342A60	PLD0, PLD1, Datatpath, and SC clock selection, general reset control. See UDB_UDB-PAIR0_UDBSNG0_RC_CFG1 for the details of bit fields.
UDB_UDBPAIR5_UDBSNG0_DPATH_OPC0	0x40342A64	Datapath opcode configuration. See UDB_UDBPAIR0_UDBSNG0_DPATH_OPC0 for the details of bit fields.
UDB_UDBPAIR5_UDBSNG0_DPATH_OPC1	0x40342A68	Datapath opcode configuration. See UDB_UDBPAIR0_UDBSNG0_DPATH_OPC0 for the details of bit fields.
UDB_UDBPAIR5_UDBSNG0_DPATH_OPC2	0x40342A6C	Datapath opcode configuration. See UDB_UDBPAIR0_UDBSNG0_DPATH_OPC0 for the details of bit fields.
UDB_UDBPAIR5_UDBSNG0_DPATH_OPC3	0x40342A70	Datapath opcode configuration. See UDB_UDBPAIR0_UDBSNG0_DPATH_OPC0 for the details of bit fields.
UDB_UDBPAIR5_UDBSNG1_PLD_IT0	0x40342A80	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR5_UDBSNG1_PLD_IT1	0x40342A84	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR5_UDBSNG1_PLD_IT2	0x40342A88	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR5_UDBSNG1_PLD_IT3	0x40342A8C	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR5_UDBSNG1_PLD_IT4	0x40342A90	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR5_UDBSNG1_PLD_IT5	0x40342A94	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR5_UDBSNG1_PLD_IT6	0x40342A98	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR5_UDBSNG1_PLD_IT7	0x40342A9C	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR5_UDBSNG1_PLD_IT8	0x40342AA0	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR5_UDBSNG1_PLD_IT9	0x40342AA4	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR5_UDBSNG1_PLD_IT10	0x40342AA8	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.
UDB_UDBPAIR5_UDBSNG1_PLD_IT11	0x40342AAC	PLD Input Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_IT0 for the details of bit fields.

Register	Address	Description
UDB_UDBPAIR5_UDBSNG1_PLD_ORT0	0x40342AB0	PLD OR Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_ORT0 for the details of bit fields.
UDB_UDBPAIR5_UDBSNG1_PLD_ORT1	0x40342AB4	PLD OR Terms. See UDB_UDBPAIR0_UDBSNG0_PLD_ORT1 for the details of bit fields.
UDB_UDBPAIR5_UDBSNG1_PLD_CFG0	0x40342AB8	PLD configuration for Carry Enable, Constant, and XOR feedback. See UDB_UDBPAIR0_UDBSNG0_PLD_CFG0 for the details of bit fields.
UDB_UDBPAIR5_UDBSNG1_PLD_CFG1	0x40342ABC	PLD configuration for Set / Reset selection, and Bypass control. See UDB_UDBPAIR0_UDBSNG0_PLD_CFG1 for the details of bit fields.
UDB_UDBPAIR5_UDBSNG1_DPATH_CFG0	0x40342AC0	Datapath input selections (RAD0, RAD1, RAD2, F0_LD, F1_LD, D0_LD, D1_LD). See UDB_UDBPAIR0_UDBSNG0_DPATH_CFG0 for the details of bit fields.
UDB_UDBPAIR5_UDBSNG1_DPATH_CFG1	0x40342AC4	Datapath input and output selections (SCI_MUX, SI_MUX, OUT0 thru OUT5). See UDB_UDBPAIR0_UDBSNG0_DPATH_CFG1 for the details of bit fields.
UDB_UDBPAIR5_UDBSNG1_DPATH_CFG2	0x40342AC8	Datapath output synchronization, ALU mask, compare 0 and 1 masks. See UDB_UDBPAIR0_UDBSNG0_DPATH_CFG2 for the details of bit fields.
UDB_UDBPAIR5_UDBSNG1_DPATH_CFG3	0x40342ACC	Datapath mask enables, shift in, carry in, compare, chaining, MSB configs; FIFO, shift and parallel input control. See UDB_UDBPAIR0_UDBSNG0_DPATH_CFG3 for the details of bit fields.
UDB_UDBPAIR5_UDBSNG1_DPATH_CFG4	0x40342AD0	Datapath FIFO and register access configuration control. See UDB_UDBPAIR0_UDBSNG0_DPATH_CFG4 for the details of bit fields.
UDB_UDBPAIR5_UDBSNG1_SC_CFG0	0x40342AD4	SC Mode 0 and 1 control registers; status register input mode; general SC configuration. See UDB_UDBPAIR0_UDBSNG0_SC_CFG0 for the details of bit fields.
UDB_UDBPAIR5_UDBSNG1_SC_CFG1	0x40342AD8	SC counter control. See UDB_UDBPAIR0_UDBSNG0_SC_CFG1 for the details of bit fields.
UDB_UDBPAIR5_UDBSNG1_RC_CFG0	0x40342ADC	PLD0, PLD1, Datatpath, and SC clock and reset control. See UDB_UDBPAIR0_UDBSNG0_RC_CFG0 for the details of bit fields.
UDB_UDBPAIR5_UDBSNG1_RC_CFG1	0x40342AE0	PLD0, PLD1, Datatpath, and SC clock selection, general reset control. See UDB_UDBPAIR0_UDBSNG0_RC_CFG1 for the details of bit fields.
UDB_UDBPAIR5_UDBSNG1_DPATH_OPC0	0x40342AE4	Datapath opcode configuration. See UDB_UDBPAIR0_UDBSNG0_DPATH_OPC0 for the details of bit fields.
UDB_UDBPAIR5_UDBSNG1_DPATH_OPC1	0x40342AE8	Datapath opcode configuration. See UDB_UDBPAIR0_UDBSNG0_DPATH_OPC0 for the details of bit fields.
UDB_UDBPAIR5_UDBSNG1_DPATH_OPC2	0x40342AEC	Datapath opcode configuration. See UDB_UDBPAIR0_UDBSNG0_DPATH_OPC0 for the details of bit fields.
UDB_UDBPAIR5_UDBSNG1_DPATH_OPC3	0x40342AF0	Datapath opcode configuration. See UDB_UDBPAIR0_UDBSNG0_DPATH_OPC0 for the details of bit fields.
UDB_UDBPAIR5_ROUTE_TOP_V_BOT	0x40342B00	Top Vertical Input (TVI) vs Bottom Vertical Input (BVI) muxing. See UDB_UDBPAIR0_ROUTE_TOP_V_BOT for the details of bit fields.
UDB_UDBPAIR5_ROUTE_LVO1_V_2	0x40342B04	Left Vertical Ouput (LVO) 1 vs 2 muxing for certain horizontals. See UDB_UDBPAIR0_ROUTE_LVO1_V_2 for the details of bit fields.
UDB_UDBPAIR5_ROUTE_RVO1_V_2	0x40342B08	Right Vertical Ouput (RVO) 1 vs 2 muxing for certain horizontals. See UDB_UDBPAIR0_ROUTE_RVO1_V_2 for the details of bit fields.
UDB_UDBPAIR5_ROUTE_TUI_CFG0	0x40342B0C	Top UDB Input (TUI) selection. See UDB_UDBPAIR0_ROUTE_TUI_CFG0 for the details of bit fields.
UDB_UDBPAIR5_ROUTE_TUI_CFG1	0x40342B10	Top UDB Input (TUI) selection. See UDB_UDBPAIR0_ROUTE_TUI_CFG1 for the details of bit fields.
UDB_UDBPAIR5_ROUTE_TUI_CFG2	0x40342B14	Top UDB Input (TUI) selection. See UDB_UDBPAIR0_ROUTE_TUI_CFG2 for the details of bit fields.
UDB_UDBPAIR5_ROUTE_TUI_CFG3	0x40342B18	Top UDB Input (TUI) selection. See UDB_UDBPAIR0_ROUTE_TUI_CFG3 for the details of bit fields.
UDB_UDBPAIR5_ROUTE_TUI_CFG4	0x40342B1C	Top UDB Input (TUI) selection. See UDB_UDBPAIR0_ROUTE_TUI_CFG4 for the details of bit fields.
UDB_UDBPAIR5_ROUTE_TUI_CFG5	0x40342B20	Top UDB Input (TUI) selection. See UDB_UDBPAIR0_ROUTE_TUI_CFG5 for the details of bit fields.
UDB_UDBPAIR5_ROUTE_BUI_CFG0	0x40342B24	Bottom UDB Input (BUI) selection. See UDB_UDBPAIR0_ROUTE_BUI_CFG0 for the details of bit fields.
UDB_UDBPAIR5_ROUTE_BUI_CFG1	0x40342B28	Bottom UDB Input (BUI) selection. See UDB_UDBPAIR0_ROUTE_BUI_CFG1 for the details of bit fields.
UDB_UDBPAIR5_ROUTE_BUI_CFG2	0x40342B2C	Bottom UDB Input (BUI) selection. See UDB_UDBPAIR0_ROUTE_BUI_CFG2 for the details of bit fields.

Register	Address	Description
UDB_UDBPAIR5_ROUTE_BUI_CFG3	0x40342B30	Bottom UDB Input (BUI) selection. See UDB_UDBPAIR0_ROUTE_BUI_CFG3 for the details of bit fields.
UDB_UDBPAIR5_ROUTE_BUI_CFG4	0x40342B34	Bottom UDB Input (BUI) selection. See UDB_UDBPAIR0_ROUTE_BUI_CFG4 for the details of bit fields.
UDB_UDBPAIR5_ROUTE_BUI_CFG5	0x40342B38	Bottom UDB Input (BUI) selection. See UDB_UDBPAIR0_ROUTE_BUI_CFG5 for the details of bit fields.
UDB_UDBPAIR5_ROUTE_RVO_CFG0	0x40342B3C	Right Vertical Ouput (RVO) selection. See UDB_UDBPAIR0_ROUTE_RVO_CFG0 for the details of bit fields.
UDB_UDBPAIR5_ROUTE_RVO_CFG1	0x40342B40	Right Vertical Ouput (RVO) selection. See UDB_UDBPAIR0_ROUTE_RVO_CFG1 for the details of bit fields.
UDB_UDBPAIR5_ROUTE_RVO_CFG2	0x40342B44	Right Vertical Ouput (RVO) selection. See UDB_UDBPAIR0_ROUTE_RVO_CFG2 for the details of bit fields.
UDB_UDBPAIR5_ROUTE_RVO_CFG3	0x40342B48	Right Vertical Ouput (RVO) selection. See UDB_UDBPAIR0_ROUTE_RVO_CFG3 for the details of bit fields.
UDB_UDBPAIR5_ROUTE_LVO_CFG0	0x40342B4C	Left Vertical Ouput (LVO) selection. See UDB_UDBPAIR0_ROUTE_LVO_CFG0 for the details of bit fields.
UDB_UDBPAIR5_ROUTE_LVO_CFG1	0x40342B50	Left Vertical Ouput (LVO) selection. See UDB_UDBPAIR0_ROUTE_LVO_CFG1 for the details of bit fields.
UDB_UDBPAIR5_ROUTE_RHO_CFG0	0x40342B54	Right Horizontal Out (RHO) selection. See UDB_UDBPAIR0_ROUTE_RHO_CFG0 for the details of bit fields.
UDB_UDBPAIR5_ROUTE_RHO_CFG1	0x40342B58	Right Horizontal Out (RHO) selection. See UDB_UDBPAIR0_ROUTE_RHO_CFG1 for the details of bit fields.
UDB_UDBPAIR5_ROUTE_RHO_CFG2	0x40342B5C	Right Horizontal Out (RHO) selection. See UDB_UDBPAIR0_ROUTE_RHO_CFG2 for the details of bit fields.
UDB_UDBPAIR5_ROUTE_LHO_CFG0	0x40342B60	Left Horizontal Out (LHO) selection. See UDB_UDBPAIR0_ROUTE_LHO_CFG0 for the details of bit fields.
UDB_UDBPAIR5_ROUTE_LHO_CFG1	0x40342B64	Left Horizontal Out (LHO) selection. See UDB_UDBPAIR0_ROUTE_LHO_CFG1 for the details of bit fields.
UDB_UDBPAIR5_ROUTE_LHO_CFG2	0x40342B68	Left Horizontal Out (LHO) selection. See UDB_UDBPAIR0_ROUTE_LHO_CFG2 for the details of bit fields.
UDB_UDBPAIR5_ROUTE_LHO_CFG3	0x40342B6C	Left Horizontal Out (LHO) selection. See UDB_UDBPAIR0_ROUTE_LHO_CFG3 for the details of bit fields.
UDB_UDBPAIR5_ROUTE_LHO_CFG4	0x40342B70	Left Horizontal Out (LHO) selection. See UDB_UDBPAIR0_ROUTE_LHO_CFG4 for the details of bit fields.
UDB_UDBPAIR5_ROUTE_LHO_CFG5	0x40342B74	Left Horizontal Out (LHO) selection. See UDB_UDBPAIR0_ROUTE_LHO_CFG5 for the details of bit fields.
UDB_UDBPAIR5_ROUTE_LHO_CFG6	0x40342B78	Left Horizontal Out (LHO) selection. See UDB_UDBPAIR0_ROUTE_LHO_CFG6 for the details of bit fields.
UDB_UDBPAIR5_ROUTE_LHO_CFG7	0x40342B7C	Left Horizontal Out (LHO) selection. See UDB_UDBPAIR0_ROUTE_LHO_CFG7 for the details of bit fields.
UDB_UDBPAIR5_ROUTE_LHO_CFG8	0x40342B80	Left Horizontal Out (LHO) selection. See UDB_UDBPAIR0_ROUTE_LHO_CFG8 for the details of bit fields.
UDB_UDBPAIR5_ROUTE_LHO_CFG9	0x40342B84	Left Horizontal Out (LHO) selection. See UDB_UDBPAIR0_ROUTE_LHO_CFG9 for the details of bit fields.
UDB_UDBPAIR5_ROUTE_LHO_CFG10	0x40342B88	Left Horizontal Out (LHO) selection. See UDB_UDBPAIR0_ROUTE_LHO_CFG10 for the details of bit fields.
UDB_UDBPAIR5_ROUTE_LHO_CFG11	0x40342B8C	Left Horizontal Out (LHO) selection. See UDB_UDBPAIR0_ROUTE_LHO_CFG11 for the details of bit fields.
UDB_DSI0_LVO1_V_2	0x40346000	Left Vertical Ouput (LVO) 1 vs 2 muxing for certain horizontals
UDB_DSI0_RVO1_V_2	0x40346004	Right Vertical Ouput (RVO) 1 vs 2 muxing for certain horizontals
UDB_DSI0_DOP_CFG0	0x40346008	DSI Out Pair (DOP) selection
UDB_DSI0_DOP_CFG1	0x4034600C	DSI Out Pair (DOP) selection
UDB_DSI0_DOP_CFG2	0x40346010	DSI Out Pair (DOP) selection

Register	Address	Description
UDB_DSI0_DOP_CFG3	0x40346014	DSI Out Pair (DOP) selection
UDB_DSI0_DOT_CFG0	0x40346018	DSI Out Triplet (DOT) selection
UDB_DSI0_DOT_CFG1	0x4034601C	DSI Out Triplet (DOT) selection
UDB_DSI0_DOT_CFG2	0x40346020	DSI Out Triplet (DOT) selection
UDB_DSI0_DOT_CFG3	0x40346024	DSI Out Triplet (DOT) selection
UDB_DSI0_RVO_CFG0	0x40346028	Right Vertical Ouput (RVO) selection
UDB_DSI0_RVO_CFG1	0x4034602C	Right Vertical Ouput (RVO) selection
UDB_DSI0_RVO_CFG2	0x40346030	Right Vertical Ouput (RVO) selection
UDB_DSI0_RVO_CFG3	0x40346034	Right Vertical Ouput (RVO) selection
UDB_DSI0_LVO_CFG0	0x40346038	Left Vertical Ouput (LVO) selection
UDB_DSI0_LVO_CFG1	0x4034603C	Left Vertical Ouput (LVO) selection
UDB_DSI0_RHO_CFG0	0x40346040	Right Horizontal Out (RHO) selection
UDB_DSI0_RHO_CFG1	0x40346044	Right Horizontal Out (RHO) selection
UDB_DSI0_RHO_CFG2	0x40346048	Right Horizontal Out (RHO) selection
UDB_DSI0_LHO_CFG0	0x4034604C	Left Horizontal Out (LHO) selection
UDB_DSI0_LHO_CFG1	0x40346050	Left Horizontal Out (LHO) selection
UDB_DSI0_LHO_CFG2	0x40346054	Left Horizontal Out (LHO) selection
UDB_DSI0_LHO_CFG3	0x40346058	Left Horizontal Out (LHO) selection
UDB_DSI0_LHO_CFG4	0x4034605C	Left Horizontal Out (LHO) selection
UDB_DSI0_LHO_CFG5	0x40346060	Left Horizontal Out (LHO) selection
UDB_DSI0_LHO_CFG6	0x40346064	Left Horizontal Out (LHO) selection
UDB_DSI0_LHO_CFG7	0x40346068	Left Horizontal Out (LHO) selection
UDB_DSI0_LHO_CFG8	0x4034606C	Left Horizontal Out (LHO) selection
UDB_DSI0_LHO_CFG9	0x40346070	Left Horizontal Out (LHO) selection
UDB_DSI0_LHO_CFG10	0x40346074	Left Horizontal Out (LHO) selection
UDB_DSI0_LHO_CFG11	0x40346078	Left Horizontal Out (LHO) selection
UDB_DSI1_LVO1_V_2	0x40346080	Left Vertical Ouput (LVO) 1 vs 2 muxing for certain horizontals. See UDB_DSI0_LVO1_V_2 for the details of bit fields.
UDB_DSI1_RVO1_V_2	0x40346084	Right Vertical Ouput (RVO) 1 vs 2 muxing for certain horizontals. See UDB_DSI0_RVO1_V_2 for the details of bit fields.
UDB_DSI1_DOP_CFG0	0x40346088	DSI Out Pair (DOP) selection. See UDB_DSI0_DOP_CFG0 for the details of bit fields.

Register	Address	Description
UDB_DSI1_DOP_CFG1	0x4034608C	DSI Out Pair (DOP) selection. See UDB_DSI0_DOP_CFG1 for the details of bit fields.
UDB_DSI1_DOP_CFG2	0x40346090	DSI Out Pair (DOP) selection. See UDB_DSI0_DOP_CFG2 for the details of bit fields.
UDB_DSI1_DOP_CFG3	0x40346094	DSI Out Pair (DOP) selection. See UDB_DSI0_DOP_CFG3 for the details of bit fields.
UDB_DSI1_DOT_CFG0	0x40346098	DSI Out Triplet (DOT) selection. See UDB_DSI0_DOT_CFG0 for the details of bit fields.
UDB_DSI1_DOT_CFG1	0x4034609C	DSI Out Triplet (DOT) selection. See UDB_DSI0_DOT_CFG1 for the details of bit fields.
UDB_DSI1_DOT_CFG2	0x403460A0	DSI Out Triplet (DOT) selection. See UDB_DSI0_DOT_CFG2 for the details of bit fields.
UDB_DSI1_DOT_CFG3	0x403460A4	DSI Out Triplet (DOT) selection. See UDB_DSI0_DOT_CFG3 for the details of bit fields.
UDB_DSI1_RVO_CFG0	0x403460A8	Right Vertical Ouput (RVO) selection. See UDB_DSI0_RVO_CFG0 for the details of bit fields.
UDB_DSI1_RVO_CFG1	0x403460AC	Right Vertical Ouput (RVO) selection. See UDB_DSI0_RVO_CFG1 for the details of bit fields.
UDB_DSI1_RVO_CFG2	0x403460B0	Right Vertical Ouput (RVO) selection. See UDB_DSI0_RVO_CFG2 for the details of bit fields.
UDB_DSI1_RVO_CFG3	0x403460B4	Right Vertical Ouput (RVO) selection. See UDB_DSI0_RVO_CFG3 for the details of bit fields.
UDB_DSI1_LVO_CFG0	0x403460B8	Left Vertical Ouput (LVO) selection. See UDB_DSI0_LVO_CFG0 for the details of bit fields.
UDB_DSI1_LVO_CFG1	0x403460BC	Left Vertical Ouput (LVO) selection. See UDB_DSI0_LVO_CFG1 for the details of bit fields.
UDB_DSI1_RHO_CFG0	0x403460C0	Right Horizontal Out (RHO) selection. See UDB_DSI0_RHO_CFG0 for the details of bit fields.
UDB_DSI1_RHO_CFG1	0x403460C4	Right Horizontal Out (RHO) selection. See UDB_DSI0_RHO_CFG1 for the details of bit fields.
UDB_DSI1_RHO_CFG2	0x403460C8	Right Horizontal Out (RHO) selection. See UDB_DSI0_RHO_CFG2 for the details of bit fields.
UDB_DSI1_LHO_CFG0	0x403460CC	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG0 for the details of bit fields.
UDB_DSI1_LHO_CFG1	0x403460D0	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG1 for the details of bit fields.
UDB_DSI1_LHO_CFG2	0x403460D4	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG2 for the details of bit fields.
UDB_DSI1_LHO_CFG3	0x403460D8	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG3 for the details of bit fields.
UDB_DSI1_LHO_CFG4	0x403460DC	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG4 for the details of bit fields.
UDB_DSI1_LHO_CFG5	0x403460E0	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG5 for the details of bit fields.
UDB_DSI1_LHO_CFG6	0x403460E4	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG6 for the details of bit fields.
UDB_DSI1_LHO_CFG7	0x403460E8	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG7 for the details of bit fields.
UDB_DSI1_LHO_CFG8	0x403460EC	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG8 for the details of bit fields.
UDB_DSI1_LHO_CFG9	0x403460F0	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG9 for the details of bit fields.
UDB_DSI1_LHO_CFG10	0x403460F4	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG10 for the details of bit fields.
UDB_DSI1_LHO_CFG11	0x403460F8	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG11 for the details of bit fields.
UDB_DSI2_LVO1_V_2	0x40346100	Left Vertical Ouput (LVO) 1 vs 2 muxing for certain horizontals. See UDB_DSI0_LVO1_V_2 for the details of bit fields.

Register	Address	Description
UDB_DSI2_RVO1_V_2	0x40346104	Right Vertical Ouput (RVO) 1 vs 2 muxing for certain horizontals. See UDB_DSI0_RVO1_V_2 for the details of bit fields.
UDB_DSI2_DOP_CFG0	0x40346108	DSI Out Pair (DOP) selection. See UDB_DSI0_DOP_CFG0 for the details of bit fields.
UDB_DSI2_DOP_CFG1	0x4034610C	DSI Out Pair (DOP) selection. See UDB_DSI0_DOP_CFG1 for the details of bit fields.
UDB_DSI2_DOP_CFG2	0x40346110	DSI Out Pair (DOP) selection. See UDB_DSI0_DOP_CFG2 for the details of bit fields.
UDB_DSI2_DOP_CFG3	0x40346114	DSI Out Pair (DOP) selection. See UDB_DSI0_DOP_CFG3 for the details of bit fields.
UDB_DSI2_DOT_CFG0	0x40346118	DSI Out Triplet (DOT) selection. See UDB_DSI0_DOT_CFG0 for the details of bit fields.
UDB_DSI2_DOT_CFG1	0x4034611C	DSI Out Triplet (DOT) selection. See UDB_DSI0_DOT_CFG1 for the details of bit fields.
UDB_DSI2_DOT_CFG2	0x40346120	DSI Out Triplet (DOT) selection. See UDB_DSI0_DOT_CFG2 for the details of bit fields.
UDB_DSI2_DOT_CFG3	0x40346124	DSI Out Triplet (DOT) selection. See UDB_DSI0_DOT_CFG3 for the details of bit fields.
UDB_DSI2_RVO_CFG0	0x40346128	Right Vertical Ouput (RVO) selection. See UDB_DSI0_RVO_CFG0 for the details of bit fields.
UDB_DSI2_RVO_CFG1	0x4034612C	Right Vertical Ouput (RVO) selection. See UDB_DSI0_RVO_CFG1 for the details of bit fields.
UDB_DSI2_RVO_CFG2	0x40346130	Right Vertical Ouput (RVO) selection. See UDB_DSI0_RVO_CFG2 for the details of bit fields.
UDB_DSI2_RVO_CFG3	0x40346134	Right Vertical Ouput (RVO) selection. See UDB_DSI0_RVO_CFG3 for the details of bit fields.
UDB_DSI2_LVO_CFG0	0x40346138	Left Vertical Ouput (LVO) selection. See UDB_DSI0_LVO_CFG0 for the details of bit fields.
UDB_DSI2_LVO_CFG1	0x4034613C	Left Vertical Ouput (LVO) selection. See UDB_DSI0_LVO_CFG1 for the details of bit fields.
UDB_DSI2_RHO_CFG0	0x40346140	Right Horizontal Out (RHO) selection. See UDB_DSI0_RHO_CFG0 for the details of bit fields.
UDB_DSI2_RHO_CFG1	0x40346144	Right Horizontal Out (RHO) selection. See UDB_DSI0_RHO_CFG1 for the details of bit fields.
UDB_DSI2_RHO_CFG2	0x40346148	Right Horizontal Out (RHO) selection. See UDB_DSI0_RHO_CFG2 for the details of bit fields.
UDB_DSI2_LHO_CFG0	0x4034614C	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG0 for the details of bit fields.
UDB_DSI2_LHO_CFG1	0x40346150	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG1 for the details of bit fields.
UDB_DSI2_LHO_CFG2	0x40346154	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG2 for the details of bit fields.
UDB_DSI2_LHO_CFG3	0x40346158	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG3 for the details of bit fields.
UDB_DSI2_LHO_CFG4	0x4034615C	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG4 for the details of bit fields.
UDB_DSI2_LHO_CFG5	0x40346160	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG5 for the details of bit fields.
UDB_DSI2_LHO_CFG6	0x40346164	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG6 for the details of bit fields.
UDB_DSI2_LHO_CFG7	0x40346168	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG7 for the details of bit fields.
UDB_DSI2_LHO_CFG8	0x4034616C	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG8 for the details of bit fields.
UDB_DSI2_LHO_CFG9	0x40346170	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG9 for the details of bit fields.
UDB_DSI2_LHO_CFG10	0x40346174	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG10 for the details of bit fields.

Register	Address	Description
UDB_DSI2_LHO_CFG11	0x40346178	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG11 for the details of bit fields.
UDB_DSI3_LVO1_V_2	0x40346180	Left Vertical Ouput (LVO) 1 vs 2 muxing for certain horizontals. See UDB_DSI0_LVO1_V_2 for the details of bit fields.
UDB_DSI3_RVO1_V_2	0x40346184	Right Vertical Ouput (RVO) 1 vs 2 muxing for certain horizontals. See UDB_DSI0_RVO1_V_2 for the details of bit fields.
UDB_DSI3_DOP_CFG0	0x40346188	DSI Out Pair (DOP) selection. See UDB_DSI0_DOP_CFG0 for the details of bit fields.
UDB_DSI3_DOP_CFG1	0x4034618C	DSI Out Pair (DOP) selection. See UDB_DSI0_DOP_CFG1 for the details of bit fields.
UDB_DSI3_DOP_CFG2	0x40346190	DSI Out Pair (DOP) selection. See UDB_DSI0_DOP_CFG2 for the details of bit fields.
UDB_DSI3_DOP_CFG3	0x40346194	DSI Out Pair (DOP) selection. See UDB_DSI0_DOP_CFG3 for the details of bit fields.
UDB_DSI3_DOT_CFG0	0x40346198	DSI Out Triplet (DOT) selection. See UDB_DSI0_DOT_CFG0 for the details of bit fields.
UDB_DSI3_DOT_CFG1	0x4034619C	DSI Out Triplet (DOT) selection. See UDB_DSI0_DOT_CFG1 for the details of bit fields.
UDB_DSI3_DOT_CFG2	0x403461A0	DSI Out Triplet (DOT) selection. See UDB_DSI0_DOT_CFG2 for the details of bit fields.
UDB_DSI3_DOT_CFG3	0x403461A4	DSI Out Triplet (DOT) selection. See UDB_DSI0_DOT_CFG3 for the details of bit fields.
UDB_DSI3_RVO_CFG0	0x403461A8	Right Vertical Ouput (RVO) selection. See UDB_DSI0_RVO_CFG0 for the details of bit fields.
UDB_DSI3_RVO_CFG1	0x403461AC	Right Vertical Ouput (RVO) selection. See UDB_DSI0_RVO_CFG1 for the details of bit fields.
UDB_DSI3_RVO_CFG2	0x403461B0	Right Vertical Ouput (RVO) selection. See UDB_DSI0_RVO_CFG2 for the details of bit fields.
UDB_DSI3_RVO_CFG3	0x403461B4	Right Vertical Ouput (RVO) selection. See UDB_DSI0_RVO_CFG3 for the details of bit fields.
UDB_DSI3_LVO_CFG0	0x403461B8	Left Vertical Ouput (LVO) selection. See UDB_DSI0_LVO_CFG0 for the details of bit fields.
UDB_DSI3_LVO_CFG1	0x403461BC	Left Vertical Ouput (LVO) selection. See UDB_DSI0_LVO_CFG1 for the details of bit fields.
UDB_DSI3_RHO_CFG0	0x403461C0	Right Horizontal Out (RHO) selection. See UDB_DSI0_RHO_CFG0 for the details of bit fields.
UDB_DSI3_RHO_CFG1	0x403461C4	Right Horizontal Out (RHO) selection. See UDB_DSI0_RHO_CFG1 for the details of bit fields.
UDB_DSI3_RHO_CFG2	0x403461C8	Right Horizontal Out (RHO) selection. See UDB_DSI0_RHO_CFG2 for the details of bit fields.
UDB_DSI3_LHO_CFG0	0x403461CC	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG0 for the details of bit fields.
UDB_DSI3_LHO_CFG1	0x403461D0	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG1 for the details of bit fields.
UDB_DSI3_LHO_CFG2	0x403461D4	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG2 for the details of bit fields.
UDB_DSI3_LHO_CFG3	0x403461D8	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG3 for the details of bit fields.
UDB_DSI3_LHO_CFG4	0x403461DC	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG4 for the details of bit fields.
UDB_DSI3_LHO_CFG5	0x403461E0	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG5 for the details of bit fields.
UDB_DSI3_LHO_CFG6	0x403461E4	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG6 for the details of bit fields.
UDB_DSI3_LHO_CFG7	0x403461E8	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG7 for the details of bit fields.
UDB_DSI3_LHO_CFG8	0x403461EC	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG8 for the details of bit fields.

Register	Address	Description
UDB_DSI3_LHO_CFG9	0x403461F0	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG9 for the details of bit fields.
UDB_DSI3_LHO_CFG10	0x403461F4	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG10 for the details of bit fields.
UDB_DSI3_LHO_CFG11	0x403461F8	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG11 for the details of bit fields.
UDB_DSI4_LVO1_V_2	0x40346200	Left Vertical Ouput (LVO) 1 vs 2 muxing for certain horizontals. See UDB_DSI0_LVO1_V_2 for the details of bit fields.
UDB_DSI4_RVO1_V_2	0x40346204	Right Vertical Ouput (RVO) 1 vs 2 muxing for certain horizontals. See UDB_DSI0_RVO1_V_2 for the details of bit fields.
UDB_DSI4_DOP_CFG0	0x40346208	DSI Out Pair (DOP) selection. See UDB_DSI0_DOP_CFG0 for the details of bit fields.
UDB_DSI4_DOP_CFG1	0x4034620C	DSI Out Pair (DOP) selection. See UDB_DSI0_DOP_CFG1 for the details of bit fields.
UDB_DSI4_DOP_CFG2	0x40346210	DSI Out Pair (DOP) selection. See UDB_DSI0_DOP_CFG2 for the details of bit fields.
UDB_DSI4_DOP_CFG3	0x40346214	DSI Out Pair (DOP) selection. See UDB_DSI0_DOP_CFG3 for the details of bit fields.
UDB_DSI4_DOT_CFG0	0x40346218	DSI Out Triplet (DOT) selection. See UDB_DSI0_DOT_CFG0 for the details of bit fields.
UDB_DSI4_DOT_CFG1	0x4034621C	DSI Out Triplet (DOT) selection. See UDB_DSI0_DOT_CFG1 for the details of bit fields.
UDB_DSI4_DOT_CFG2	0x40346220	DSI Out Triplet (DOT) selection. See UDB_DSI0_DOT_CFG2 for the details of bit fields.
UDB_DSI4_DOT_CFG3	0x40346224	DSI Out Triplet (DOT) selection. See UDB_DSI0_DOT_CFG3 for the details of bit fields.
UDB_DSI4_RVO_CFG0	0x40346228	Right Vertical Ouput (RVO) selection. See UDB_DSI0_RVO_CFG0 for the details of bit fields.
UDB_DSI4_RVO_CFG1	0x4034622C	Right Vertical Ouput (RVO) selection. See UDB_DSI0_RVO_CFG1 for the details of bit fields.
UDB_DSI4_RVO_CFG2	0x40346230	Right Vertical Ouput (RVO) selection. See UDB_DSI0_RVO_CFG2 for the details of bit fields.
UDB_DSI4_RVO_CFG3	0x40346234	Right Vertical Ouput (RVO) selection. See UDB_DSI0_RVO_CFG3 for the details of bit fields.
UDB_DSI4_LVO_CFG0	0x40346238	Left Vertical Ouput (LVO) selection. See UDB_DSI0_LVO_CFG0 for the details of bit fields.
UDB_DSI4_LVO_CFG1	0x4034623C	Left Vertical Ouput (LVO) selection. See UDB_DSI0_LVO_CFG1 for the details of bit fields.
UDB_DSI4_RHO_CFG0	0x40346240	Right Horizontal Out (RHO) selection. See UDB_DSI0_RHO_CFG0 for the details of bit fields.
UDB_DSI4_RHO_CFG1	0x40346244	Right Horizontal Out (RHO) selection. See UDB_DSI0_RHO_CFG1 for the details of bit fields.
UDB_DSI4_RHO_CFG2	0x40346248	Right Horizontal Out (RHO) selection. See UDB_DSI0_RHO_CFG2 for the details of bit fields.
UDB_DSI4_LHO_CFG0	0x4034624C	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG0 for the details of bit fields.
UDB_DSI4_LHO_CFG1	0x40346250	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG1 for the details of bit fields.
UDB_DSI4_LHO_CFG2	0x40346254	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG2 for the details of bit fields.
UDB_DSI4_LHO_CFG3	0x40346258	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG3 for the details of bit fields.
UDB_DSI4_LHO_CFG4	0x4034625C	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG4 for the details of bit fields.
UDB_DSI4_LHO_CFG5	0x40346260	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG5 for the details of bit fields.
UDB_DSI4_LHO_CFG6	0x40346264	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG6 for the details of bit fields.

Register	Address	Description
UDB_DSI4_LHO_CFG7	0x40346268	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG7 for the details of bit fields.
UDB_DSI4_LHO_CFG8	0x4034626C	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG8 for the details of bit fields.
UDB_DSI4_LHO_CFG9	0x40346270	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG9 for the details of bit fields.
UDB_DSI4_LHO_CFG10	0x40346274	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG10 for the details of bit fields.
UDB_DSI4_LHO_CFG11	0x40346278	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG11 for the details of bit fields.
UDB_DSI5_LVO1_V_2	0x40346280	Left Vertical Ouput (LVO) 1 vs 2 muxing for certain horizontals. See UDB_DSI0_LVO1_V_2 for the details of bit fields.
UDB_DSI5_RVO1_V_2	0x40346284	Right Vertical Ouput (RVO) 1 vs 2 muxing for certain horizontals. See UDB_DSI0_RVO1_V_2 for the details of bit fields.
UDB_DSI5_DOP_CFG0	0x40346288	DSI Out Pair (DOP) selection. See UDB_DSI0_DOP_CFG0 for the details of bit fields.
UDB_DSI5_DOP_CFG1	0x4034628C	DSI Out Pair (DOP) selection. See UDB_DSI0_DOP_CFG1 for the details of bit fields.
UDB_DSI5_DOP_CFG2	0x40346290	DSI Out Pair (DOP) selection. See UDB_DSI0_DOP_CFG2 for the details of bit fields.
UDB_DSI5_DOP_CFG3	0x40346294	DSI Out Pair (DOP) selection. See UDB_DSI0_DOP_CFG3 for the details of bit fields.
UDB_DSI5_DOT_CFG0	0x40346298	DSI Out Triplet (DOT) selection. See UDB_DSI0_DOT_CFG0 for the details of bit fields.
UDB_DSI5_DOT_CFG1	0x4034629C	DSI Out Triplet (DOT) selection. See UDB_DSI0_DOT_CFG1 for the details of bit fields.
UDB_DSI5_DOT_CFG2	0x403462A0	DSI Out Triplet (DOT) selection. See UDB_DSI0_DOT_CFG2 for the details of bit fields.
UDB_DSI5_DOT_CFG3	0x403462A4	DSI Out Triplet (DOT) selection. See UDB_DSI0_DOT_CFG3 for the details of bit fields.
UDB_DSI5_RVO_CFG0	0x403462A8	Right Vertical Ouput (RVO) selection. See UDB_DSI0_RVO_CFG0 for the details of bit fields.
UDB_DSI5_RVO_CFG1	0x403462AC	Right Vertical Ouput (RVO) selection. See UDB_DSI0_RVO_CFG1 for the details of bit fields.
UDB_DSI5_RVO_CFG2	0x403462B0	Right Vertical Ouput (RVO) selection. See UDB_DSI0_RVO_CFG2 for the details of bit fields.
UDB_DSI5_RVO_CFG3	0x403462B4	Right Vertical Ouput (RVO) selection. See UDB_DSI0_RVO_CFG3 for the details of bit fields.
UDB_DSI5_LVO_CFG0	0x403462B8	Left Vertical Ouput (LVO) selection. See UDB_DSI0_LVO_CFG0 for the details of bit fields.
UDB_DSI5_LVO_CFG1	0x403462BC	Left Vertical Ouput (LVO) selection. See UDB_DSI0_LVO_CFG1 for the details of bit fields.
UDB_DSI5_RHO_CFG0	0x403462C0	Right Horizontal Out (RHO) selection. See UDB_DSI0_RHO_CFG0 for the details of bit fields.
UDB_DSI5_RHO_CFG1	0x403462C4	Right Horizontal Out (RHO) selection. See UDB_DSI0_RHO_CFG1 for the details of bit fields.
UDB_DSI5_RHO_CFG2	0x403462C8	Right Horizontal Out (RHO) selection. See UDB_DSI0_RHO_CFG2 for the details of bit fields.
UDB_DSI5_LHO_CFG0	0x403462CC	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG0 for the details of bit fields.
UDB_DSI5_LHO_CFG1	0x403462D0	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG1 for the details of bit fields.
UDB_DSI5_LHO_CFG2	0x403462D4	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG2 for the details of bit fields.
UDB_DSI5_LHO_CFG3	0x403462D8	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG3 for the details of bit fields.
UDB_DSI5_LHO_CFG4	0x403462DC	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG4 for the details of bit fields.

Register	Address	Description
UDB_DSI5_LHO_CFG5	0x403462E0	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG5 for the details of bit fields.
UDB_DSI5_LHO_CFG6	0x403462E4	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG6 for the details of bit fields.
UDB_DSI5_LHO_CFG7	0x403462E8	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG7 for the details of bit fields.
UDB_DSI5_LHO_CFG8	0x403462EC	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG8 for the details of bit fields.
UDB_DSI5_LHO_CFG9	0x403462F0	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG9 for the details of bit fields.
UDB_DSI5_LHO_CFG10	0x403462F4	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG10 for the details of bit fields.
UDB_DSI5_LHO_CFG11	0x403462F8	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG11 for the details of bit fields.
UDB_DSI6_LVO1_V_2	0x40346300	Left Vertical Ouput (LVO) 1 vs 2 muxing for certain horizontals. See UDB_DSI0_LVO1_V_2 for the details of bit fields.
UDB_DSI6_RVO1_V_2	0x40346304	Right Vertical Ouput (RVO) 1 vs 2 muxing for certain horizontals. See UDB_DSI0_RVO1_V_2 for the details of bit fields.
UDB_DSI6_DOP_CFG0	0x40346308	DSI Out Pair (DOP) selection. See UDB_DSI0_DOP_CFG0 for the details of bit fields.
UDB_DSI6_DOP_CFG1	0x4034630C	DSI Out Pair (DOP) selection. See UDB_DSI0_DOP_CFG1 for the details of bit fields.
UDB_DSI6_DOP_CFG2	0x40346310	DSI Out Pair (DOP) selection. See UDB_DSI0_DOP_CFG2 for the details of bit fields.
UDB_DSI6_DOP_CFG3	0x40346314	DSI Out Pair (DOP) selection. See UDB_DSI0_DOP_CFG3 for the details of bit fields.
UDB_DSI6_DOT_CFG0	0x40346318	DSI Out Triplet (DOT) selection. See UDB_DSI0_DOT_CFG0 for the details of bit fields.
UDB_DSI6_DOT_CFG1	0x4034631C	DSI Out Triplet (DOT) selection. See UDB_DSI0_DOT_CFG1 for the details of bit fields.
UDB_DSI6_DOT_CFG2	0x40346320	DSI Out Triplet (DOT) selection. See UDB_DSI0_DOT_CFG2 for the details of bit fields.
UDB_DSI6_DOT_CFG3	0x40346324	DSI Out Triplet (DOT) selection. See UDB_DSI0_DOT_CFG3 for the details of bit fields.
UDB_DSI6_RVO_CFG0	0x40346328	Right Vertical Ouput (RVO) selection. See UDB_DSI0_RVO_CFG0 for the details of bit fields.
UDB_DSI6_RVO_CFG1	0x4034632C	Right Vertical Ouput (RVO) selection. See UDB_DSI0_RVO_CFG1 for the details of bit fields.
UDB_DSI6_RVO_CFG2	0x40346330	Right Vertical Ouput (RVO) selection. See UDB_DSI0_RVO_CFG2 for the details of bit fields.
UDB_DSI6_RVO_CFG3	0x40346334	Right Vertical Ouput (RVO) selection. See UDB_DSI0_RVO_CFG3 for the details of bit fields.
UDB_DSI6_LVO_CFG0	0x40346338	Left Vertical Ouput (LVO) selection. See UDB_DSI0_LVO_CFG0 for the details of bit fields.
UDB_DSI6_LVO_CFG1	0x4034633C	Left Vertical Ouput (LVO) selection. See UDB_DSI0_LVO_CFG1 for the details of bit fields.
UDB_DSI6_RHO_CFG0	0x40346340	Right Horizontal Out (RHO) selection. See UDB_DSI0_RHO_CFG0 for the details of bit fields.
UDB_DSI6_RHO_CFG1	0x40346344	Right Horizontal Out (RHO) selection. See UDB_DSI0_RHO_CFG1 for the details of bit fields.
UDB_DSI6_RHO_CFG2	0x40346348	Right Horizontal Out (RHO) selection. See UDB_DSI0_RHO_CFG2 for the details of bit fields.
UDB_DSI6_LHO_CFG0	0x4034634C	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG0 for the details of bit fields.
UDB_DSI6_LHO_CFG1	0x40346350	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG1 for the details of bit fields.
UDB_DSI6_LHO_CFG2	0x40346354	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG2 for the details of bit fields.

Register	Address	Description
UDB_DSI6_LHO_CFG3	0x40346358	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG3 for the details of bit fields.
UDB_DSI6_LHO_CFG4	0x4034635C	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG4 for the details of bit fields.
UDB_DSI6_LHO_CFG5	0x40346360	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG5 for the details of bit fields.
UDB_DSI6_LHO_CFG6	0x40346364	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG6 for the details of bit fields.
UDB_DSI6_LHO_CFG7	0x40346368	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG7 for the details of bit fields.
UDB_DSI6_LHO_CFG8	0x4034636C	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG8 for the details of bit fields.
UDB_DSI6_LHO_CFG9	0x40346370	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG9 for the details of bit fields.
UDB_DSI6_LHO_CFG10	0x40346374	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG10 for the details of bit fields.
UDB_DSI6_LHO_CFG11	0x40346378	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG11 for the details of bit fields.
UDB_DSI7_LVO1_V_2	0x40346380	Left Vertical Ouput (LVO) 1 vs 2 muxing for certain horizontals. See UDB_DSI0_LVO1_V_2 for the details of bit fields.
UDB_DSI7_RVO1_V_2	0x40346384	Right Vertical Ouput (RVO) 1 vs 2 muxing for certain horizontals. See UDB_DSI0_RVO1_V_2 for the details of bit fields.
UDB_DSI7_DOP_CFG0	0x40346388	DSI Out Pair (DOP) selection. See UDB_DSI0_DOP_CFG0 for the details of bit fields.
UDB_DSI7_DOP_CFG1	0x4034638C	DSI Out Pair (DOP) selection. See UDB_DSI0_DOP_CFG1 for the details of bit fields.
UDB_DSI7_DOP_CFG2	0x40346390	DSI Out Pair (DOP) selection. See UDB_DSI0_DOP_CFG2 for the details of bit fields.
UDB_DSI7_DOP_CFG3	0x40346394	DSI Out Pair (DOP) selection. See UDB_DSI0_DOP_CFG3 for the details of bit fields.
UDB_DSI7_DOT_CFG0	0x40346398	DSI Out Triplet (DOT) selection. See UDB_DSI0_DOT_CFG0 for the details of bit fields.
UDB_DSI7_DOT_CFG1	0x4034639C	DSI Out Triplet (DOT) selection. See UDB_DSI0_DOT_CFG1 for the details of bit fields.
UDB_DSI7_DOT_CFG2	0x403463A0	DSI Out Triplet (DOT) selection. See UDB_DSI0_DOT_CFG2 for the details of bit fields.
UDB_DSI7_DOT_CFG3	0x403463A4	DSI Out Triplet (DOT) selection. See UDB_DSI0_DOT_CFG3 for the details of bit fields.
UDB_DSI7_RVO_CFG0	0x403463A8	Right Vertical Ouput (RVO) selection. See UDB_DSI0_RVO_CFG0 for the details of bit fields.
UDB_DSI7_RVO_CFG1	0x403463AC	Right Vertical Ouput (RVO) selection. See UDB_DSI0_RVO_CFG1 for the details of bit fields.
UDB_DSI7_RVO_CFG2	0x403463B0	Right Vertical Ouput (RVO) selection. See UDB_DSI0_RVO_CFG2 for the details of bit fields.
UDB_DSI7_RVO_CFG3	0x403463B4	Right Vertical Ouput (RVO) selection. See UDB_DSI0_RVO_CFG3 for the details of bit fields.
UDB_DSI7_LVO_CFG0	0x403463B8	Left Vertical Ouput (LVO) selection. See UDB_DSI0_LVO_CFG0 for the details of bit fields.
UDB_DSI7_LVO_CFG1	0x403463BC	Left Vertical Ouput (LVO) selection. See UDB_DSI0_LVO_CFG1 for the details of bit fields.
UDB_DSI7_RHO_CFG0	0x403463C0	Right Horizontal Out (RHO) selection. See UDB_DSI0_RHO_CFG0 for the details of bit fields.
UDB_DSI7_RHO_CFG1	0x403463C4	Right Horizontal Out (RHO) selection. See UDB_DSI0_RHO_CFG1 for the details of bit fields.
UDB_DSI7_RHO_CFG2	0x403463C8	Right Horizontal Out (RHO) selection. See UDB_DSI0_RHO_CFG2 for the details of bit fields.
UDB_DSI7_LHO_CFG0	0x403463CC	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG0 for the details of bit fields.

Register	Address	Description
UDB_DSI7_LHO_CFG1	0x403463D0	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG1 for the details of bit fields.
UDB_DSI7_LHO_CFG2	0x403463D4	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG2 for the details of bit fields.
UDB_DSI7_LHO_CFG3	0x403463D8	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG3 for the details of bit fields.
UDB_DSI7_LHO_CFG4	0x403463DC	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG4 for the details of bit fields.
UDB_DSI7_LHO_CFG5	0x403463E0	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG5 for the details of bit fields.
UDB_DSI7_LHO_CFG6	0x403463E4	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG6 for the details of bit fields.
UDB_DSI7_LHO_CFG7	0x403463E8	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG7 for the details of bit fields.
UDB_DSI7_LHO_CFG8	0x403463EC	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG8 for the details of bit fields.
UDB_DSI7_LHO_CFG9	0x403463F0	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG9 for the details of bit fields.
UDB_DSI7_LHO_CFG10	0x403463F4	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG10 for the details of bit fields.
UDB_DSI7_LHO_CFG11	0x403463F8	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG11 for the details of bit fields.
UDB_DSI8_LVO1_V_2	0x40346400	Left Vertical Ouput (LVO) 1 vs 2 muxing for certain horizontals. See UDB_DSI0_LVO1_V_2 for the details of bit fields.
UDB_DSI8_RVO1_V_2	0x40346404	Right Vertical Ouput (RVO) 1 vs 2 muxing for certain horizontals. See UDB_DSI0_RVO1_V_2 for the details of bit fields.
UDB_DSI8_DOP_CFG0	0x40346408	DSI Out Pair (DOP) selection. See UDB_DSI0_DOP_CFG0 for the details of bit fields.
UDB_DSI8_DOP_CFG1	0x4034640C	DSI Out Pair (DOP) selection. See UDB_DSI0_DOP_CFG1 for the details of bit fields.
UDB_DSI8_DOP_CFG2	0x40346410	DSI Out Pair (DOP) selection. See UDB_DSI0_DOP_CFG2 for the details of bit fields.
UDB_DSI8_DOP_CFG3	0x40346414	DSI Out Pair (DOP) selection. See UDB_DSI0_DOP_CFG3 for the details of bit fields.
UDB_DSI8_DOT_CFG0	0x40346418	DSI Out Triplet (DOT) selection. See UDB_DSI0_DOT_CFG0 for the details of bit fields.
UDB_DSI8_DOT_CFG1	0x4034641C	DSI Out Triplet (DOT) selection. See UDB_DSI0_DOT_CFG1 for the details of bit fields.
UDB_DSI8_DOT_CFG2	0x40346420	DSI Out Triplet (DOT) selection. See UDB_DSI0_DOT_CFG2 for the details of bit fields.
UDB_DSI8_DOT_CFG3	0x40346424	DSI Out Triplet (DOT) selection. See UDB_DSI0_DOT_CFG3 for the details of bit fields.
UDB_DSI8_RVO_CFG0	0x40346428	Right Vertical Ouput (RVO) selection. See UDB_DSI0_RVO_CFG0 for the details of bit fields.
UDB_DSI8_RVO_CFG1	0x4034642C	Right Vertical Ouput (RVO) selection. See UDB_DSI0_RVO_CFG1 for the details of bit fields.
UDB_DSI8_RVO_CFG2	0x40346430	Right Vertical Ouput (RVO) selection. See UDB_DSI0_RVO_CFG2 for the details of bit fields.
UDB_DSI8_RVO_CFG3	0x40346434	Right Vertical Ouput (RVO) selection. See UDB_DSI0_RVO_CFG3 for the details of bit fields.
UDB_DSI8_LVO_CFG0	0x40346438	Left Vertical Ouput (LVO) selection. See UDB_DSI0_LVO_CFG0 for the details of bit fields.
UDB_DSI8_LVO_CFG1	0x4034643C	Left Vertical Ouput (LVO) selection. See UDB_DSI0_LVO_CFG1 for the details of bit fields.
UDB_DSI8_RHO_CFG0	0x40346440	Right Horizontal Out (RHO) selection. See UDB_DSI0_RHO_CFG0 for the details of bit fields.
UDB_DSI8_RHO_CFG1	0x40346444	Right Horizontal Out (RHO) selection. See UDB_DSI0_RHO_CFG1 for the details of bit fields.

Register	Address	Description
UDB_DSI8_RHO_CFG2	0x40346448	Right Horizontal Out (RHO) selection. See UDB_DSI0_RHO_CFG2 for the details of bit fields.
UDB_DSI8_LHO_CFG0	0x4034644C	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG0 for the details of bit fields.
UDB_DSI8_LHO_CFG1	0x40346450	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG1 for the details of bit fields.
UDB_DSI8_LHO_CFG2	0x40346454	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG2 for the details of bit fields.
UDB_DSI8_LHO_CFG3	0x40346458	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG3 for the details of bit fields.
UDB_DSI8_LHO_CFG4	0x4034645C	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG4 for the details of bit fields.
UDB_DSI8_LHO_CFG5	0x40346460	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG5 for the details of bit fields.
UDB_DSI8_LHO_CFG6	0x40346464	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG6 for the details of bit fields.
UDB_DSI8_LHO_CFG7	0x40346468	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG7 for the details of bit fields.
UDB_DSI8_LHO_CFG8	0x4034646C	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG8 for the details of bit fields.
UDB_DSI8_LHO_CFG9	0x40346470	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG9 for the details of bit fields.
UDB_DSI8_LHO_CFG10	0x40346474	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG10 for the details of bit fields.
UDB_DSI8_LHO_CFG11	0x40346478	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG11 for the details of bit fields.
UDB_DSI9_LVO1_V_2	0x40346480	Left Vertical Ouput (LVO) 1 vs 2 muxing for certain horizontals. See UDB_DSI0_LVO1_V_2 for the details of bit fields.
UDB_DSI9_RVO1_V_2	0x40346484	Right Vertical Ouput (RVO) 1 vs 2 muxing for certain horizontals. See UDB_DSI0_RVO1_V_2 for the details of bit fields.
UDB_DSI9_DOP_CFG0	0x40346488	DSI Out Pair (DOP) selection. See UDB_DSI0_DOP_CFG0 for the details of bit fields.
UDB_DSI9_DOP_CFG1	0x4034648C	DSI Out Pair (DOP) selection. See UDB_DSI0_DOP_CFG1 for the details of bit fields.
UDB_DSI9_DOP_CFG2	0x40346490	DSI Out Pair (DOP) selection. See UDB_DSI0_DOP_CFG2 for the details of bit fields.
UDB_DSI9_DOP_CFG3	0x40346494	DSI Out Pair (DOP) selection. See UDB_DSI0_DOP_CFG3 for the details of bit fields.
UDB_DSI9_DOT_CFG0	0x40346498	DSI Out Triplet (DOT) selection. See UDB_DSI0_DOT_CFG0 for the details of bit fields.
UDB_DSI9_DOT_CFG1	0x4034649C	DSI Out Triplet (DOT) selection. See UDB_DSI0_DOT_CFG1 for the details of bit fields.
UDB_DSI9_DOT_CFG2	0x403464A0	DSI Out Triplet (DOT) selection. See UDB_DSI0_DOT_CFG2 for the details of bit fields.
UDB_DSI9_DOT_CFG3	0x403464A4	DSI Out Triplet (DOT) selection. See UDB_DSI0_DOT_CFG3 for the details of bit fields.
UDB_DSI9_RVO_CFG0	0x403464A8	Right Vertical Ouput (RVO) selection. See UDB_DSI0_RVO_CFG0 for the details of bit fields.
UDB_DSI9_RVO_CFG1	0x403464AC	Right Vertical Ouput (RVO) selection. See UDB_DSI0_RVO_CFG1 for the details of bit fields.
UDB_DSI9_RVO_CFG2	0x403464B0	Right Vertical Ouput (RVO) selection. See UDB_DSI0_RVO_CFG2 for the details of bit fields.
UDB_DSI9_RVO_CFG3	0x403464B4	Right Vertical Ouput (RVO) selection. See UDB_DSI0_RVO_CFG3 for the details of bit fields.
UDB_DSI9_LVO_CFG0	0x403464B8	Left Vertical Ouput (LVO) selection. See UDB_DSI0_LVO_CFG0 for the details of bit fields.
UDB_DSI9_LVO_CFG1	0x403464BC	Left Vertical Ouput (LVO) selection. See UDB_DSI0_LVO_CFG1 for the details of bit fields.

Register	Address	Description
UDB_DSI9_RHO_CFG0	0x403464C0	Right Horizontal Out (RHO) selection. See UDB_DSI0_RHO_CFG0 for the details of bit fields.
UDB_DSI9_RHO_CFG1	0x403464C4	Right Horizontal Out (RHO) selection. See UDB_DSI0_RHO_CFG1 for the details of bit fields.
UDB_DSI9_RHO_CFG2	0x403464C8	Right Horizontal Out (RHO) selection. See UDB_DSI0_RHO_CFG2 for the details of bit fields.
UDB_DSI9_LHO_CFG0	0x403464CC	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG0 for the details of bit fields.
UDB_DSI9_LHO_CFG1	0x403464D0	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG1 for the details of bit fields.
UDB_DSI9_LHO_CFG2	0x403464D4	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG2 for the details of bit fields.
UDB_DSI9_LHO_CFG3	0x403464D8	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG3 for the details of bit fields.
UDB_DSI9_LHO_CFG4	0x403464DC	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG4 for the details of bit fields.
UDB_DSI9_LHO_CFG5	0x403464E0	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG5 for the details of bit fields.
UDB_DSI9_LHO_CFG6	0x403464E4	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG6 for the details of bit fields.
UDB_DSI9_LHO_CFG7	0x403464E8	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG7 for the details of bit fields.
UDB_DSI9_LHO_CFG8	0x403464EC	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG8 for the details of bit fields.
UDB_DSI9_LHO_CFG9	0x403464F0	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG9 for the details of bit fields.
UDB_DSI9_LHO_CFG10	0x403464F4	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG10 for the details of bit fields.
UDB_DSI9_LHO_CFG11	0x403464F8	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG11 for the details of bit fields.
UDB_DSI10_LVO1_V_2	0x40346500	Left Vertical Ouput (LVO) 1 vs 2 muxing for certain horizontals. See UDB_DSI0_LVO1_V_2 for the details of bit fields.
UDB_DSI10_RVO1_V_2	0x40346504	Right Vertical Ouput (RVO) 1 vs 2 muxing for certain horizontals. See UDB_DSI0_RVO1_V_2 for the details of bit fields.
UDB_DSI10_DOP_CFG0	0x40346508	DSI Out Pair (DOP) selection. See UDB_DSI0_DOP_CFG0 for the details of bit fields.
UDB_DSI10_DOP_CFG1	0x4034650C	DSI Out Pair (DOP) selection. See UDB_DSI0_DOP_CFG1 for the details of bit fields.
UDB_DSI10_DOP_CFG2	0x40346510	DSI Out Pair (DOP) selection. See UDB_DSI0_DOP_CFG2 for the details of bit fields.
UDB_DSI10_DOP_CFG3	0x40346514	DSI Out Pair (DOP) selection. See UDB_DSI0_DOP_CFG3 for the details of bit fields.
UDB_DSI10_DOT_CFG0	0x40346518	DSI Out Triplet (DOT) selection. See UDB_DSI0_DOT_CFG0 for the details of bit fields.
UDB_DSI10_DOT_CFG1	0x4034651C	DSI Out Triplet (DOT) selection. See UDB_DSI0_DOT_CFG1 for the details of bit fields.
UDB_DSI10_DOT_CFG2	0x40346520	DSI Out Triplet (DOT) selection. See UDB_DSI0_DOT_CFG2 for the details of bit fields.
UDB_DSI10_DOT_CFG3	0x40346524	DSI Out Triplet (DOT) selection. See UDB_DSI0_DOT_CFG3 for the details of bit fields.
UDB_DSI10_RVO_CFG0	0x40346528	Right Vertical Ouput (RVO) selection. See UDB_DSI0_RVO_CFG0 for the details of bit fields.
UDB_DSI10_RVO_CFG1	0x4034652C	Right Vertical Ouput (RVO) selection. See UDB_DSI0_RVO_CFG1 for the details of bit fields.
UDB_DSI10_RVO_CFG2	0x40346530	Right Vertical Ouput (RVO) selection. See UDB_DSI0_RVO_CFG2 for the details of bit fields.
UDB_DSI10_RVO_CFG3	0x40346534	Right Vertical Ouput (RVO) selection. See UDB_DSI0_RVO_CFG3 for the details of bit fields.

Register	Address	Description
UDB_DSI10_LVO_CFG0	0x40346538	Left Vertical Ouput (LVO) selection. See UDB_DSI0_LVO_CFG0 for the details of bit fields.
UDB_DSI10_LVO_CFG1	0x4034653C	Left Vertical Ouput (LVO) selection. See UDB_DSI0_LVO_CFG1 for the details of bit fields.
UDB_DSI10_RHO_CFG0	0x40346540	Right Horizontal Out (RHO) selection. See UDB_DSI0_RHO_CFG0 for the details of bit fields.
UDB_DSI10_RHO_CFG1	0x40346544	Right Horizontal Out (RHO) selection. See UDB_DSI0_RHO_CFG1 for the details of bit fields.
UDB_DSI10_RHO_CFG2	0x40346548	Right Horizontal Out (RHO) selection. See UDB_DSI0_RHO_CFG2 for the details of bit fields.
UDB_DSI10_LHO_CFG0	0x4034654C	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG0 for the details of bit fields.
UDB_DSI10_LHO_CFG1	0x40346550	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG1 for the details of bit fields.
UDB_DSI10_LHO_CFG2	0x40346554	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG2 for the details of bit fields.
UDB_DSI10_LHO_CFG3	0x40346558	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG3 for the details of bit fields.
UDB_DSI10_LHO_CFG4	0x4034655C	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG4 for the details of bit fields.
UDB_DSI10_LHO_CFG5	0x40346560	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG5 for the details of bit fields.
UDB_DSI10_LHO_CFG6	0x40346564	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG6 for the details of bit fields.
UDB_DSI10_LHO_CFG7	0x40346568	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG7 for the details of bit fields.
UDB_DSI10_LHO_CFG8	0x4034656C	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG8 for the details of bit fields.
UDB_DSI10_LHO_CFG9	0x40346570	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG9 for the details of bit fields.
UDB_DSI10_LHO_CFG10	0x40346574	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG10 for the details of bit fields.
UDB_DSI10_LHO_CFG11	0x40346578	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG11 for the details of bit fields.
UDB_DSI11_LVO1_V_2	0x40346580	Left Vertical Ouput (LVO) 1 vs 2 muxing for certain horizontals. See UDB_DSI0_LVO1_V_2 for the details of bit fields.
UDB_DSI11_RVO1_V_2	0x40346584	Right Vertical Ouput (RVO) 1 vs 2 muxing for certain horizontals. See UDB_DSI0_RVO1_V_2 for the details of bit fields.
UDB_DSI11_DOP_CFG0	0x40346588	DSI Out Pair (DOP) selection. See UDB_DSI0_DOP_CFG0 for the details of bit fields.
UDB_DSI11_DOP_CFG1	0x4034658C	DSI Out Pair (DOP) selection. See UDB_DSI0_DOP_CFG1 for the details of bit fields.
UDB_DSI11_DOP_CFG2	0x40346590	DSI Out Pair (DOP) selection. See UDB_DSI0_DOP_CFG2 for the details of bit fields.
UDB_DSI11_DOP_CFG3	0x40346594	DSI Out Pair (DOP) selection. See UDB_DSI0_DOP_CFG3 for the details of bit fields.
UDB_DSI11_DOT_CFG0	0x40346598	DSI Out Triplet (DOT) selection. See UDB_DSI0_DOT_CFG0 for the details of bit fields.
UDB_DSI11_DOT_CFG1	0x4034659C	DSI Out Triplet (DOT) selection. See UDB_DSI0_DOT_CFG1 for the details of bit fields.
UDB_DSI11_DOT_CFG2	0x403465A0	DSI Out Triplet (DOT) selection. See UDB_DSI0_DOT_CFG2 for the details of bit fields.
UDB_DSI11_DOT_CFG3	0x403465A4	DSI Out Triplet (DOT) selection. See UDB_DSI0_DOT_CFG3 for the details of bit fields.
UDB_DSI11_RVO_CFG0	0x403465A8	Right Vertical Ouput (RVO) selection. See UDB_DSI0_RVO_CFG0 for the details of bit fields.
UDB_DSI11_RVO_CFG1	0x403465AC	Right Vertical Ouput (RVO) selection. See UDB_DSI0_RVO_CFG1 for the details of bit fields.

Register	Address	Description
UDB_DSI11_RVO_CFG2	0x403465B0	Right Vertical Ouput (RVO) selection. See UDB_DSI0_RVO_CFG2 for the details of bit fields.
UDB_DSI11_RVO_CFG3	0x403465B4	Right Vertical Ouput (RVO) selection. See UDB_DSI0_RVO_CFG3 for the details of bit fields.
UDB_DSI11_LVO_CFG0	0x403465B8	Left Vertical Ouput (LVO) selection. See UDB_DSI0_LVO_CFG0 for the details of bit fields.
UDB_DSI11_LVO_CFG1	0x403465BC	Left Vertical Ouput (LVO) selection. See UDB_DSI0_LVO_CFG1 for the details of bit fields.
UDB_DSI11_RHO_CFG0	0x403465C0	Right Horizontal Out (RHO) selection. See UDB_DSI0_RHO_CFG0 for the details of bit fields.
UDB_DSI11_RHO_CFG1	0x403465C4	Right Horizontal Out (RHO) selection. See UDB_DSI0_RHO_CFG1 for the details of bit fields.
UDB_DSI11_RHO_CFG2	0x403465C8	Right Horizontal Out (RHO) selection. See UDB_DSI0_RHO_CFG2 for the details of bit fields.
UDB_DSI11_LHO_CFG0	0x403465CC	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG0 for the details of bit fields.
UDB_DSI11_LHO_CFG1	0x403465D0	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG1 for the details of bit fields.
UDB_DSI11_LHO_CFG2	0x403465D4	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG2 for the details of bit fields.
UDB_DSI11_LHO_CFG3	0x403465D8	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG3 for the details of bit fields.
UDB_DSI11_LHO_CFG4	0x403465DC	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG4 for the details of bit fields.
UDB_DSI11_LHO_CFG5	0x403465E0	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG5 for the details of bit fields.
UDB_DSI11_LHO_CFG6	0x403465E4	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG6 for the details of bit fields.
UDB_DSI11_LHO_CFG7	0x403465E8	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG7 for the details of bit fields.
UDB_DSI11_LHO_CFG8	0x403465EC	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG8 for the details of bit fields.
UDB_DSI11_LHO_CFG9	0x403465F0	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG9 for the details of bit fields.
UDB_DSI11_LHO_CFG10	0x403465F4	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG10 for the details of bit fields.
UDB_DSI11_LHO_CFG11	0x403465F8	Left Horizontal Out (LHO) selection. See UDB_DSI0_LHO_CFG11 for the details of bit fields.
UDB_PA0_CFG0	0x40347000	PA Data In Clock Control Register
UDB_PA0_CFG1	0x40347004	PA Data Out Clock Control Register
UDB_PA0_CFG2	0x40347008	PA Clock Select Register
UDB_PA0_CFG3	0x4034700C	PA Reset Select Register
UDB_PA0_CFG4	0x40347010	PA Reset Enable Register
UDB_PA0_CFG5	0x40347014	PA Reset Pin Select Register
UDB_PA0_CFG6	0x40347018	PA Input Data Sync Control Register - Low
UDB_PA0_CFG7	0x4034701C	PA Input Data Sync Control Register - High
UDB_PA0_CFG8	0x40347020	PA Output Data Sync Control Register - Low
UDB_PA0_CFG9	0x40347024	PA Output Data Sync Control Register - High

Register	Address	Description
UDB_PA0_CFG10	0x40347028	PA Output Data Select Register - Low
UDB_PA0_CFG11	0x4034702C	PA Output Data Select Register - High
UDB_PA0_CFG12	0x40347030	PA OE Select Register - Low
UDB_PA0_CFG13	0x40347034	PA OE Select Register - High
UDB_PA0_CFG14	0x40347038	PA OE Sync Register
UDB_PA1_CFG0	0x40347040	PA Data In Clock Control Register. See UDB_PA0_CFG0 for the details of bit fields.
UDB_PA1_CFG1	0x40347044	PA Data Out Clock Control Register. See UDB_PA0_CFG1 for the details of bit fields.
UDB_PA1_CFG2	0x40347048	PA Clock Select Register. See UDB_PA0_CFG2 for the details of bit fields.
UDB_PA1_CFG3	0x4034704C	PA Reset Select Register. See UDB_PA0_CFG3 for the details of bit fields.
UDB_PA1_CFG4	0x40347050	PA Reset Enable Register. See UDB_PA0_CFG4 for the details of bit fields.
UDB_PA1_CFG5	0x40347054	PA Reset Pin Select Register. See UDB_PA0_CFG5 for the details of bit fields.
UDB_PA1_CFG6	0x40347058	PA Input Data Sync Control Register - Low. See UDB_PA0_CFG6 for the details of bit fields.
UDB_PA1_CFG7	0x4034705C	PA Input Data Sync Control Register - High. See UDB_PA0_CFG7 for the details of bit fields.
UDB_PA1_CFG8	0x40347060	PA Output Data Sync Control Register - Low. See UDB_PA0_CFG8 for the details of bit fields.
UDB_PA1_CFG9	0x40347064	PA Output Data Sync Control Register - High. See UDB_PA0_CFG9 for the details of bit fields.
UDB_PA1_CFG10	0x40347068	PA Output Data Select Register - Low. See UDB_PA0_CFG10 for the details of bit fields.
UDB_PA1_CFG11	0x4034706C	PA Output Data Select Register - High. See UDB_PA0_CFG11 for the details of bit fields.
UDB_PA1_CFG12	0x40347070	PA OE Select Register - Low. See UDB_PA0_CFG12 for the details of bit fields.
UDB_PA1_CFG13	0x40347074	PA OE Select Register - High. See UDB_PA0_CFG13 for the details of bit fields.
UDB_PA1_CFG14	0x40347078	PA OE Sync Register. See UDB_PA0_CFG14 for the details of bit fields.
UDB_PA2_CFG0	0x40347080	PA Data In Clock Control Register. See UDB_PA0_CFG0 for the details of bit fields.
UDB_PA2_CFG1	0x40347084	PA Data Out Clock Control Register. See UDB_PA0_CFG1 for the details of bit fields.
UDB_PA2_CFG2	0x40347088	PA Clock Select Register. See UDB_PA0_CFG2 for the details of bit fields.
UDB_PA2_CFG3	0x4034708C	PA Reset Select Register. See UDB_PA0_CFG3 for the details of bit fields.
UDB_PA2_CFG4	0x40347090	PA Reset Enable Register. See UDB_PA0_CFG4 for the details of bit fields.
UDB_PA2_CFG5	0x40347094	PA Reset Pin Select Register. See UDB_PA0_CFG5 for the details of bit fields.
UDB_PA2_CFG6	0x40347098	PA Input Data Sync Control Register - Low. See UDB_PA0_CFG6 for the details of bit fields.
UDB_PA2_CFG7	0x4034709C	PA Input Data Sync Control Register - High. See UDB_PA0_CFG7 for the details of bit fields.
UDB_PA2_CFG8	0x403470A0	PA Output Data Sync Control Register - Low. See UDB_PA0_CFG8 for the details of bit fields.

Register	Address	Description
UDB_PA2_CFG9	0x403470A4	PA Output Data Sync Control Register - High. See UDB_PA0_CFG9 for the details of bit fields.
UDB_PA2_CFG10	0x403470A8	PA Output Data Select Register - Low. See UDB_PA0_CFG10 for the details of bit fields.
UDB_PA2_CFG11	0x403470AC	PA Output Data Select Register - High. See UDB_PA0_CFG11 for the details of bit fields.
UDB_PA2_CFG12	0x403470B0	PA OE Select Register - Low. See UDB_PA0_CFG12 for the details of bit fields.
UDB_PA2_CFG13	0x403470B4	PA OE Select Register - High. See UDB_PA0_CFG13 for the details of bit fields.
UDB_PA2_CFG14	0x403470B8	PA OE Sync Register. See UDB_PA0_CFG14 for the details of bit fields.
UDB_PA3_CFG0	0x403470C0	PA Data In Clock Control Register. See UDB_PA0_CFG0 for the details of bit fields.
UDB_PA3_CFG1	0x403470C4	PA Data Out Clock Control Register. See UDB_PA0_CFG1 for the details of bit fields.
UDB_PA3_CFG2	0x403470C8	PA Clock Select Register. See UDB_PA0_CFG2 for the details of bit fields.
UDB_PA3_CFG3	0x403470CC	PA Reset Select Register. See UDB_PA0_CFG3 for the details of bit fields.
UDB_PA3_CFG4	0x403470D0	PA Reset Enable Register. See UDB_PA0_CFG4 for the details of bit fields.
UDB_PA3_CFG5	0x403470D4	PA Reset Pin Select Register. See UDB_PA0_CFG5 for the details of bit fields.
UDB_PA3_CFG6	0x403470D8	PA Input Data Sync Control Register - Low. See UDB_PA0_CFG6 for the details of bit fields.
UDB_PA3_CFG7	0x403470DC	PA Input Data Sync Control Register - High. See UDB_PA0_CFG7 for the details of bit fields.
UDB_PA3_CFG8	0x403470E0	PA Output Data Sync Control Register - Low. See UDB_PA0_CFG8 for the details of bit fields.
UDB_PA3_CFG9	0x403470E4	PA Output Data Sync Control Register - High. See UDB_PA0_CFG9 for the details of bit fields.
UDB_PA3_CFG10	0x403470E8	PA Output Data Select Register - Low. See UDB_PA0_CFG10 for the details of bit fields.
UDB_PA3_CFG11	0x403470EC	PA Output Data Select Register - High. See UDB_PA0_CFG11 for the details of bit fields.
UDB_PA3_CFG12	0x403470F0	PA OE Select Register - Low. See UDB_PA0_CFG12 for the details of bit fields.
UDB_PA3_CFG13	0x403470F4	PA OE Select Register - High. See UDB_PA0_CFG13 for the details of bit fields.
UDB_PA3_CFG14	0x403470F8	PA OE Sync Register. See UDB_PA0_CFG14 for the details of bit fields.
UDB_PA4_CFG0	0x40347100	PA Data In Clock Control Register. See UDB_PA0_CFG0 for the details of bit fields.
UDB_PA4_CFG1	0x40347104	PA Data Out Clock Control Register. See UDB_PA0_CFG1 for the details of bit fields.
UDB_PA4_CFG2	0x40347108	PA Clock Select Register. See UDB_PA0_CFG2 for the details of bit fields.
UDB_PA4_CFG3	0x4034710C	PA Reset Select Register. See UDB_PA0_CFG3 for the details of bit fields.
UDB_PA4_CFG4	0x40347110	PA Reset Enable Register. See UDB_PA0_CFG4 for the details of bit fields.
UDB_PA4_CFG5	0x40347114	PA Reset Pin Select Register. See UDB_PA0_CFG5 for the details of bit fields.
UDB_PA4_CFG6	0x40347118	PA Input Data Sync Control Register - Low. See UDB_PA0_CFG6 for the details of bit fields.
UDB_PA4_CFG7	0x4034711C	PA Input Data Sync Control Register - High. See UDB_PA0_CFG7 for the details of bit fields.

Register	Address	Description
UDB_PA4_CFG8	0x40347120	PA Output Data Sync Control Register - Low. See UDB_PA0_CFG8 for the details of bit fields.
UDB_PA4_CFG9	0x40347124	PA Output Data Sync Control Register - High. See UDB_PA0_CFG9 for the details of bit fields.
UDB_PA4_CFG10	0x40347128	PA Output Data Select Register - Low. See UDB_PA0_CFG10 for the details of bit fields.
UDB_PA4_CFG11	0x4034712C	PA Output Data Select Register - High. See UDB_PA0_CFG11 for the details of bit fields.
UDB_PA4_CFG12	0x40347130	PA OE Select Register - Low. See UDB_PA0_CFG12 for the details of bit fields.
UDB_PA4_CFG13	0x40347134	PA OE Select Register - High. See UDB_PA0_CFG13 for the details of bit fields.
UDB_PA4_CFG14	0x40347138	PA OE Sync Register. See UDB_PA0_CFG14 for the details of bit fields.
UDB_PA5_CFG0	0x40347140	PA Data In Clock Control Register. See UDB_PA0_CFG0 for the details of bit fields.
UDB_PA5_CFG1	0x40347144	PA Data Out Clock Control Register. See UDB_PA0_CFG1 for the details of bit fields.
UDB_PA5_CFG2	0x40347148	PA Clock Select Register. See UDB_PA0_CFG2 for the details of bit fields.
UDB_PA5_CFG3	0x4034714C	PA Reset Select Register. See UDB_PA0_CFG3 for the details of bit fields.
UDB_PA5_CFG4	0x40347150	PA Reset Enable Register. See UDB_PA0_CFG4 for the details of bit fields.
UDB_PA5_CFG5	0x40347154	PA Reset Pin Select Register. See UDB_PA0_CFG5 for the details of bit fields.
UDB_PA5_CFG6	0x40347158	PA Input Data Sync Control Register - Low. See UDB_PA0_CFG6 for the details of bit fields.
UDB_PA5_CFG7	0x4034715C	PA Input Data Sync Control Register - High. See UDB_PA0_CFG7 for the details of bit fields.
UDB_PA5_CFG8	0x40347160	PA Output Data Sync Control Register - Low. See UDB_PA0_CFG8 for the details of bit fields.
UDB_PA5_CFG9	0x40347164	PA Output Data Sync Control Register - High. See UDB_PA0_CFG9 for the details of bit fields.
UDB_PA5_CFG10	0x40347168	PA Output Data Select Register - Low. See UDB_PA0_CFG10 for the details of bit fields.
UDB_PA5_CFG11	0x4034716C	PA Output Data Select Register - High. See UDB_PA0_CFG11 for the details of bit fields.
UDB_PA5_CFG12	0x40347170	PA OE Select Register - Low. See UDB_PA0_CFG12 for the details of bit fields.
UDB_PA5_CFG13	0x40347174	PA OE Select Register - High. See UDB_PA0_CFG13 for the details of bit fields.
UDB_PA5_CFG14	0x40347178	PA OE Sync Register. See UDB_PA0_CFG14 for the details of bit fields.
UDB_PA6_CFG0	0x40347180	PA Data In Clock Control Register. See UDB_PA0_CFG0 for the details of bit fields.
UDB_PA6_CFG1	0x40347184	PA Data Out Clock Control Register. See UDB_PA0_CFG1 for the details of bit fields.
UDB_PA6_CFG2	0x40347188	PA Clock Select Register. See UDB_PA0_CFG2 for the details of bit fields.
UDB_PA6_CFG3	0x4034718C	PA Reset Select Register. See UDB_PA0_CFG3 for the details of bit fields.
UDB_PA6_CFG4	0x40347190	PA Reset Enable Register. See UDB_PA0_CFG4 for the details of bit fields.
UDB_PA6_CFG5	0x40347194	PA Reset Pin Select Register. See UDB_PA0_CFG5 for the details of bit fields.
UDB_PA6_CFG6	0x40347198	PA Input Data Sync Control Register - Low. See UDB_PA0_CFG6 for the details of bit fields.

Register	Address	Description
UDB_PA6_CFG7	0x4034719C	PA Input Data Sync Control Register - High. See UDB_PA0_CFG7 for the details of bit fields.
UDB_PA6_CFG8	0x403471A0	PA Output Data Sync Control Register - Low. See UDB_PA0_CFG8 for the details of bit fields.
UDB_PA6_CFG9	0x403471A4	PA Output Data Sync Control Register - High. See UDB_PA0_CFG9 for the details of bit fields.
UDB_PA6_CFG10	0x403471A8	PA Output Data Select Register - Low. See UDB_PA0_CFG10 for the details of bit fields.
UDB_PA6_CFG11	0x403471AC	PA Output Data Select Register - High. See UDB_PA0_CFG11 for the details of bit fields.
UDB_PA6_CFG12	0x403471B0	PA OE Select Register - Low. See UDB_PA0_CFG12 for the details of bit fields.
UDB_PA6_CFG13	0x403471B4	PA OE Select Register - High. See UDB_PA0_CFG13 for the details of bit fields.
UDB_PA6_CFG14	0x403471B8	PA OE Sync Register. See UDB_PA0_CFG14 for the details of bit fields.
UDB_PA7_CFG0	0x403471C0	PA Data In Clock Control Register. See UDB_PA0_CFG0 for the details of bit fields.
UDB_PA7_CFG1	0x403471C4	PA Data Out Clock Control Register. See UDB_PA0_CFG1 for the details of bit fields.
UDB_PA7_CFG2	0x403471C8	PA Clock Select Register. See UDB_PA0_CFG2 for the details of bit fields.
UDB_PA7_CFG3	0x403471CC	PA Reset Select Register. See UDB_PA0_CFG3 for the details of bit fields.
UDB_PA7_CFG4	0x403471D0	PA Reset Enable Register. See UDB_PA0_CFG4 for the details of bit fields.
UDB_PA7_CFG5	0x403471D4	PA Reset Pin Select Register. See UDB_PA0_CFG5 for the details of bit fields.
UDB_PA7_CFG6	0x403471D8	PA Input Data Sync Control Register - Low. See UDB_PA0_CFG6 for the details of bit fields.
UDB_PA7_CFG7	0x403471DC	PA Input Data Sync Control Register - High. See UDB_PA0_CFG7 for the details of bit fields.
UDB_PA7_CFG8	0x403471E0	PA Output Data Sync Control Register - Low. See UDB_PA0_CFG8 for the details of bit fields.
UDB_PA7_CFG9	0x403471E4	PA Output Data Sync Control Register - High. See UDB_PA0_CFG9 for the details of bit fields.
UDB_PA7_CFG10	0x403471E8	PA Output Data Select Register - Low. See UDB_PA0_CFG10 for the details of bit fields.
UDB_PA7_CFG11	0x403471EC	PA Output Data Select Register - High. See UDB_PA0_CFG11 for the details of bit fields.
UDB_PA7_CFG12	0x403471F0	PA OE Select Register - Low. See UDB_PA0_CFG12 for the details of bit fields.
UDB_PA7_CFG13	0x403471F4	PA OE Select Register - High. See UDB_PA0_CFG13 for the details of bit fields.
UDB_PA7_CFG14	0x403471F8	PA OE Sync Register. See UDB_PA0_CFG14 for the details of bit fields.
UDB_PA8_CFG0	0x40347200	PA Data In Clock Control Register. See UDB_PA0_CFG0 for the details of bit fields.
UDB_PA8_CFG1	0x40347204	PA Data Out Clock Control Register. See UDB_PA0_CFG1 for the details of bit fields.
UDB_PA8_CFG2	0x40347208	PA Clock Select Register. See UDB_PA0_CFG2 for the details of bit fields.
UDB_PA8_CFG3	0x4034720C	PA Reset Select Register. See UDB_PA0_CFG3 for the details of bit fields.
UDB_PA8_CFG4	0x40347210	PA Reset Enable Register. See UDB_PA0_CFG4 for the details of bit fields.
UDB_PA8_CFG5	0x40347214	PA Reset Pin Select Register. See UDB_PA0_CFG5 for the details of bit fields.

Register	Address	Description
UDB_PA8_CFG6	0x40347218	PA Input Data Sync Control Register - Low. See UDB_PA0_CFG6 for the details of bit fields.
UDB_PA8_CFG7	0x4034721C	PA Input Data Sync Control Register - High. See UDB_PA0_CFG7 for the details of bit fields.
UDB_PA8_CFG8	0x40347220	PA Output Data Sync Control Register - Low. See UDB_PA0_CFG8 for the details of bit fields.
UDB_PA8_CFG9	0x40347224	PA Output Data Sync Control Register - High. See UDB_PA0_CFG9 for the details of bit fields.
UDB_PA8_CFG10	0x40347228	PA Output Data Select Register - Low. See UDB_PA0_CFG10 for the details of bit fields.
UDB_PA8_CFG11	0x4034722C	PA Output Data Select Register - High. See UDB_PA0_CFG11 for the details of bit fields.
UDB_PA8_CFG12	0x40347230	PA OE Select Register - Low. See UDB_PA0_CFG12 for the details of bit fields.
UDB_PA8_CFG13	0x40347234	PA OE Select Register - High. See UDB_PA0_CFG13 for the details of bit fields.
UDB_PA8_CFG14	0x40347238	PA OE Sync Register. See UDB_PA0_CFG14 for the details of bit fields.
UDB_PA9_CFG0	0x40347240	PA Data In Clock Control Register. See UDB_PA0_CFG0 for the details of bit fields.
UDB_PA9_CFG1	0x40347244	PA Data Out Clock Control Register. See UDB_PA0_CFG1 for the details of bit fields.
UDB_PA9_CFG2	0x40347248	PA Clock Select Register. See UDB_PA0_CFG2 for the details of bit fields.
UDB_PA9_CFG3	0x4034724C	PA Reset Select Register. See UDB_PA0_CFG3 for the details of bit fields.
UDB_PA9_CFG4	0x40347250	PA Reset Enable Register. See UDB_PA0_CFG4 for the details of bit fields.
UDB_PA9_CFG5	0x40347254	PA Reset Pin Select Register. See UDB_PA0_CFG5 for the details of bit fields.
UDB_PA9_CFG6	0x40347258	PA Input Data Sync Control Register - Low. See UDB_PA0_CFG6 for the details of bit fields.
UDB_PA9_CFG7	0x4034725C	PA Input Data Sync Control Register - High. See UDB_PA0_CFG7 for the details of bit fields.
UDB_PA9_CFG8	0x40347260	PA Output Data Sync Control Register - Low. See UDB_PA0_CFG8 for the details of bit fields.
UDB_PA9_CFG9	0x40347264	PA Output Data Sync Control Register - High. See UDB_PA0_CFG9 for the details of bit fields.
UDB_PA9_CFG10	0x40347268	PA Output Data Select Register - Low. See UDB_PA0_CFG10 for the details of bit fields.
UDB_PA9_CFG11	0x4034726C	PA Output Data Select Register - High. See UDB_PA0_CFG11 for the details of bit fields.
UDB_PA9_CFG12	0x40347270	PA OE Select Register - Low. See UDB_PA0_CFG12 for the details of bit fields.
UDB_PA9_CFG13	0x40347274	PA OE Select Register - High. See UDB_PA0_CFG13 for the details of bit fields.
UDB_PA9_CFG14	0x40347278	PA OE Sync Register. See UDB_PA0_CFG14 for the details of bit fields.
UDB_PA10_CFG0	0x40347280	PA Data In Clock Control Register. See UDB_PA0_CFG0 for the details of bit fields.
UDB_PA10_CFG1	0x40347284	PA Data Out Clock Control Register. See UDB_PA0_CFG1 for the details of bit fields.
UDB_PA10_CFG2	0x40347288	PA Clock Select Register. See UDB_PA0_CFG2 for the details of bit fields.
UDB_PA10_CFG3	0x4034728C	PA Reset Select Register. See UDB_PA0_CFG3 for the details of bit fields.
UDB_PA10_CFG4	0x40347290	PA Reset Enable Register. See UDB_PA0_CFG4 for the details of bit fields.

Register	Address	Description
UDB_PA10_CFG5	0x40347294	PA Reset Pin Select Register. See UDB_PA0_CFG5 for the details of bit fields.
UDB_PA10_CFG6	0x40347298	PA Input Data Sync Control Register - Low. See UDB_PA0_CFG6 for the details of bit fields.
UDB_PA10_CFG7	0x4034729C	PA Input Data Sync Control Register - High. See UDB_PA0_CFG7 for the details of bit fields.
UDB_PA10_CFG8	0x403472A0	PA Output Data Sync Control Register - Low. See UDB_PA0_CFG8 for the details of bit fields.
UDB_PA10_CFG9	0x403472A4	PA Output Data Sync Control Register - High. See UDB_PA0_CFG9 for the details of bit fields.
UDB_PA10_CFG10	0x403472A8	PA Output Data Select Register - Low. See UDB_PA0_CFG10 for the details of bit fields.
UDB_PA10_CFG11	0x403472AC	PA Output Data Select Register - High. See UDB_PA0_CFG11 for the details of bit fields.
UDB_PA10_CFG12	0x403472B0	PA OE Select Register - Low. See UDB_PA0_CFG12 for the details of bit fields.
UDB_PA10_CFG13	0x403472B4	PA OE Select Register - High. See UDB_PA0_CFG13 for the details of bit fields.
UDB_PA10_CFG14	0x403472B8	PA OE Sync Register. See UDB_PA0_CFG14 for the details of bit fields.
UDB_PA11_CFG0	0x403472C0	PA Data In Clock Control Register. See UDB_PA0_CFG0 for the details of bit fields.
UDB_PA11_CFG1	0x403472C4	PA Data Out Clock Control Register. See UDB_PA0_CFG1 for the details of bit fields.
UDB_PA11_CFG2	0x403472C8	PA Clock Select Register. See UDB_PA0_CFG2 for the details of bit fields.
UDB_PA11_CFG3	0x403472CC	PA Reset Select Register. See UDB_PA0_CFG3 for the details of bit fields.
UDB_PA11_CFG4	0x403472D0	PA Reset Enable Register. See UDB_PA0_CFG4 for the details of bit fields.
UDB_PA11_CFG5	0x403472D4	PA Reset Pin Select Register. See UDB_PA0_CFG5 for the details of bit fields.
UDB_PA11_CFG6	0x403472D8	PA Input Data Sync Control Register - Low. See UDB_PA0_CFG6 for the details of bit fields.
UDB_PA11_CFG7	0x403472DC	PA Input Data Sync Control Register - High. See UDB_PA0_CFG7 for the details of bit fields.
UDB_PA11_CFG8	0x403472E0	PA Output Data Sync Control Register - Low. See UDB_PA0_CFG8 for the details of bit fields.
UDB_PA11_CFG9	0x403472E4	PA Output Data Sync Control Register - High. See UDB_PA0_CFG9 for the details of bit fields.
UDB_PA11_CFG10	0x403472E8	PA Output Data Select Register - Low. See UDB_PA0_CFG10 for the details of bit fields.
UDB_PA11_CFG11	0x403472EC	PA Output Data Select Register - High. See UDB_PA0_CFG11 for the details of bit fields.
UDB_PA11_CFG12	0x403472F0	PA OE Select Register - Low. See UDB_PA0_CFG12 for the details of bit fields.
UDB_PA11_CFG13	0x403472F4	PA OE Select Register - High. See UDB_PA0_CFG13 for the details of bit fields.
UDB_PA11_CFG14	0x403472F8	PA OE Sync Register. See UDB_PA0_CFG14 for the details of bit fields.
UDB_BCTL_MDCLK_EN	0x40347800	Master Digital Clock Enable Register
UDB_BCTL_MBCLK_EN	0x40347804	Master clk_peri_app Enable Register
UDB_BCTL_BOTSEL_L	0x40347808	Lower Nibble Bottom Digital Clock Select Register
UDB_BCTL_BOTSEL_U	0x4034780C	Upper Nibble Bottom Digital Clock Select Register

Register	Address	Description
UDB_BCTL_QCLK_EN0	0x40347810	Quadrant Digital Clock Enable Registers
UDB_BCTL_QCLK_EN1	0x40347814	Quadrant Digital Clock Enable Registers. See UDB_BCTL_QCLK_EN0 for the details of bit fields.
UDB_BCTL_QCLK_EN2	0x40347818	Quadrant Digital Clock Enable Registers. See UDB_BCTL_QCLK_EN0 for the details of bit fields.
UDB_UDBIF_BANK_CTL	0x40347900	Bank Control
UDB_UDBIF_INT_CLK_CTL	0x40347904	Interrupt Clock Control
UDB_UDBIF_INT_CFG	0x40347908	Interrupt Configuration
UDB_UDBIF_TR_CLK_CTL	0x4034790C	Trigger Clock Control
UDB_UDBIF_TR_CFG	0x40347910	Trigger Configuration
UDB_UDBIF_PRIVATE	0x40347914	Internal use only

18.1.1 UDB_WRKONE_A0

Accumulator Registers {A1,A0}

Address: 0x40340000

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	A0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW875a							
HW Access	RW							
Name	A1 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 8	A1	Accumulator 1 Register Default Value: 0
7 : 0	A0	Accumulator 0 Register Default Value: 0

18.1.2 UDB_WRKONE_D0

Data Registers {D1,D0}

Address: 0x40340100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	D0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	D1 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 8	D1	Data 1 Register Default Value: 0
7 : 0	D0	Data 0 Register Default Value: 0

18.1.3 UDB_WRKONE_F0

FIFOs {F1,F0}

Address: 0x40340200

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	F0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	F1 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 8	F1	FIFO 1 Default Value: X
7 : 0	F0	FIFO 0 Default Value: X

18.1.4 UDB_WRKONE_CTL_ST0

Status and Control Registers {CTL,ST}

Address: 0x40340300

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	ST [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CTL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 8	CTL	Control Register Default Value: 0
7 : 0	ST	Status Register Default Value: 0

18.1.5 UDB_WRKONE_ACTL_MSK0

Mask and Auxiliary Control Registers {ACTL,MSK}

Address: 0x40340400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW						
HW Access	None	R						
Name	None	MSK [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		R	R	R	R	R	R
Name	None [15:14]		CNT_START	INT_EN	FIFO1_LVL	FIFO0_LVL	FIFO1_CLR	FIFO0_CLR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
13	CNT_START	Control Register Counter Enable Default Value: 0 **0x0: DISABLE :** Counter disabled **0x1: ENABLE :** Counter enabled
12	INT_EN	enable interrupt Default Value: 0 **0x0: DISABLE :** Interrupt disabled **0x1: ENABLE :** Interrupt enabled
11	FIFO1_LVL	FIFO fill status level control Default Value: 0

18.1.5 UDB_WRKONE_ACTL_MSK0 (continued)

		0x0: NORMAL : input mode: FIFO not full; output mode: FIFO not empty **0x1: MID :** input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full
10	FIFO0_LVL	FIFO fill status level control Default Value: 0 **0x0: NORMAL :** input mode: FIFO not full; output mode: FIFO not empty **0x1: MID :** input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full
9	FIFO1_CLR	FIFO clear Default Value: 0 **0x0: NORMAL :** Normal FIFO operation **0x1: CLEAR :** Clear FIFO state
8	FIFO0_CLR	FIFO clear Default Value: 0 **0x0: NORMAL :** Normal FIFO operation **0x1: CLEAR :** Clear FIFO state
6 : 0	MSK	Interrupt Mask Register Default Value: 0

18.1.6 UDB_WRKONE_MC0

PLD Macrocell Read Registers {00,MC}

Address: 0x40340500

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	W				W			
Name	PLD1_MC [7:4]				PLD0_MC [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	PLD1_MC	PLD1 Macrocell Read Register Default Value: 0
3 : 0	PLD0_MC	PLD0 Macrocell Read Register Default Value: 0

18.1.7 UDB_WRKMULT_A00

Accumulator 0

Address: 0x40341000

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	A0_0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	A0_1 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	A0_2 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	A0_3 [31:24]							

Bits	Name	Description
31 : 24	A0_3	Accumulator 0 for UDB[n+3] Default Value: 0
23 : 16	A0_2	Accumulator 0 for UDB[n+2] Default Value: 0
15 : 8	A0_1	Accumulator 0 for UDB[n+1] Default Value: 0
7 : 0	A0_0	Accumulator 0 for UDB[n] Default Value: 0

18.1.8 UDB_WRKMULT_A10

Accumulator 1

Address: 0x40341100

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	A1_0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	A1_1 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	A1_2 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	A1_3 [31:24]							

Bits	Name	Description
31 : 24	A1_3	Accumulator 1 for UDB[n+3] Default Value: 0
23 : 16	A1_2	Accumulator 1 for UDB[n+2] Default Value: 0
15 : 8	A1_1	Accumulator 1 for UDB[n+1] Default Value: 0
7 : 0	A1_0	Accumulator 1 for UDB[n] Default Value: 0

18.1.9 UDB_WRKMULT_D00

Data 0

Address: 0x40341200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	D0_0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	D0_1 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	D0_2 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	D0_3 [31:24]							

Bits	Name	Description
31 : 24	D0_3	Data 0 for UDB[n+3] Default Value: 0
23 : 16	D0_2	Data 0 for UDB[n+2] Default Value: 0
15 : 8	D0_1	Data 0 for UDB[n+1] Default Value: 0
7 : 0	D0_0	Data 0 for UDB[n] Default Value: 0

18.1.10 UDB_WRKMULT_D10

Data 1

Address: 0x40341300

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	D1_0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	D1_1 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	D1_2 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	D1_3 [31:24]							

Bits	Name	Description
31 : 24	D1_3	Data 1 for UDB[n+3] Default Value: 0
23 : 16	D1_2	Data 1 for UDB[n+2] Default Value: 0
15 : 8	D1_1	Data 1 for UDB[n+1] Default Value: 0
7 : 0	D1_0	Data 1 for UDB[n] Default Value: 0

18.1.11 UDB_WRKMULT_F00

FIFO 0

Address: 0x40341400

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	F0_0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	F0_1 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	F0_2 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	F0_3 [31:24]							

Bits	Name	Description
31 : 24	F0_3	Fifo 0 for UDB[n+3] Default Value: X
23 : 16	F0_2	Fifo 0 for UDB[n+2] Default Value: X
15 : 8	F0_1	Fifo 0 for UDB[n+1] Default Value: X
7 : 0	F0_0	Fifo 0 for UDB[n] Default Value: X

18.1.12 UDB_WRKMULT_F10

FIFO 1

Address: 0x40341500

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	F1_0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	F1_1 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	F1_2 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	F1_3 [31:24]							

Bits	Name	Description
31 : 24	F1_3	Fifo 1 for UDB[n+3] Default Value: X
23 : 16	F1_2	Fifo 1 for UDB[n+2] Default Value: X
15 : 8	F1_1	Fifo 1 for UDB[n+1] Default Value: X
7 : 0	F1_0	Fifo 1 for UDB[n] Default Value: X

18.1.13 UDB_WRKMULT_ST0

Status Register

Address: 0x40341600

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	ST_0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	ST_1 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	ST_2 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	ST_3 [31:24]							

Bits	Name	Description
31 : 24	ST_3	Status register for UDB[n+3] Default Value: 0
23 : 16	ST_2	Status register for UDB[n+2] Default Value: 0
15 : 8	ST_1	Status register for UDB[n+1] Default Value: 0
7 : 0	ST_0	Status register for UDB[n] Default Value: 0

18.1.14 UDB_WRKMULT_CTL0

Control Register

Address: 0x40341700

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CTL_0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CTL_1 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	CTL_2 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	CTL_3 [31:24]							

Bits	Name	Description
31 : 24	CTL_3	Control register for UDB[n+3] Default Value: 0
23 : 16	CTL_2	Control register for UDB[n+2] Default Value: 0
15 : 8	CTL_1	Control register for UDB[n+1] Default Value: 0
7 : 0	CTL_0	Control register for UDB[n] Default Value: 0

18.1.15 UDB_WRKMULT_MSK0

Interrupt Mask

Address: 0x40341800

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW						
HW Access	None	R						
Name	None	MSK_0 [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW						
HW Access	None	R						
Name	None	MSK_1 [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	None	RW						
HW Access	None	R						
Name	None	MSK_2 [22:16]						

Bits	31	30	29	28	27	26	25	24
SW Access	None	RW						
HW Access	None	R						
Name	None	MSK_3 [30:24]						

Bits	Name	Description
30 : 24	MSK_3	Interrupt Mask Register Default Value: 0
22 : 16	MSK_2	Interrupt Mask Register Default Value: 0
14 : 8	MSK_1	Interrupt Mask Register Default Value: 0
6 : 0	MSK_0	Interrupt Mask Register Default Value: 0

18.1.16 UDB_WRKMULT_ACTL0

Auxiliary Control

Address: 0x40341900

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		R	R	R	R	R	R
Name	None [7:6]		CNT_START_0	INT_EN_0	FIFO1_LVL_0	FIFO0_LVL_0	FIFO1_CLR_0	FIFO0_CLR_0

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		R	R	R	R	R	R
Name	None [15:14]		CNT_START_1	INT_EN_1	FIFO1_LVL_1	FIFO0_LVL_1	FIFO1_CLR_1	FIFO0_CLR_1

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		R	R	R	R	R	R
Name	None [23:22]		CNT_START_2	INT_EN_2	FIFO1_LVL_2	FIFO0_LVL_2	FIFO1_CLR_2	FIFO0_CLR_2

Bits	31	30	29	28	27	26	25	24
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		R	R	R	R	R	R
Name	None [31:30]		CNT_START_3	INT_EN_3	FIFO1_LVL_3	FIFO0_LVL_3	FIFO1_CLR_3	FIFO0_CLR_3

Bits	Name	Description
29	CNT_START_3	Control Register Counter Enable Default Value: 0 **0x0: DISABLE :** Counter disabled **0x1: ENABLE :** Counter enabled
28	INT_EN_3	enable interrupt Default Value: 0 **0x0: DISABLE :** Interrupt disabled **0x1: ENABLE :** Interrupt enabled

18.1.16 UDB_WRKMULT_ACTL0 (continued)

27	FIFO1_LVL_3	FIFO fill status level control Default Value: 0 **0x0: NORMAL :** input mode: FIFO not full; output mode: FIFO not empty **0x1: MID :** input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full
26	FIFO0_LVL_3	FIFO fill status level control Default Value: 0 **0x0: NORMAL :** input mode: FIFO not full; output mode: FIFO not empty **0x1: MID :** input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full
25	FIFO1_CLR_3	FIFO clear Default Value: 0 **0x0: NORMAL :** Normal FIFO operation **0x1: CLEAR :** Clear FIFO state
24	FIFO0_CLR_3	FIFO clear Default Value: 0 **0x0: NORMAL :** Normal FIFO operation **0x1: CLEAR :** Clear FIFO state
21	CNT_START_2	Control Register Counter Enable Default Value: 0 **0x0: DISABLE :** Counter disabled **0x1: ENABLE :** Counter enabled
20	INT_EN_2	enable interrupt Default Value: 0 **0x0: DISABLE :** Interrupt disabled **0x1: ENABLE :** Interrupt enabled
19	FIFO1_LVL_2	FIFO fill status level control Default Value: 0 **0x0: NORMAL :** input mode: FIFO not full; output mode: FIFO not empty **0x1: MID :** input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full
18	FIFO0_LVL_2	FIFO fill status level control Default Value: 0

18.1.16 UDB_WRKMULT_ACTL0 (continued)

		0x0: NORMAL : input mode: FIFO not full; output mode: FIFO not empty **0x1: MID :** input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full
17	FIFO1_CLR_2	FIFO clear Default Value: 0 **0x0: NORMAL :** Normal FIFO operation **0x1: CLEAR :** Clear FIFO state
16	FIFO0_CLR_2	FIFO clear Default Value: 0 **0x0: NORMAL :** Normal FIFO operation **0x1: CLEAR :** Clear FIFO state
13	CNT_START_1	Control Register Counter Enable Default Value: 0 **0x0: DISABLE :** Counter disabled **0x1: ENABLE :** Counter enabled
12	INT_EN_1	enable interrupt Default Value: 0 **0x0: DISABLE :** Interrupt disabled **0x1: ENABLE :** Interrupt enabled
11	FIFO1_LVL_1	FIFO fill status level control Default Value: 0 **0x0: NORMAL :** input mode: FIFO not full; output mode: FIFO not empty **0x1: MID :** input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full
10	FIFO0_LVL_1	FIFO fill status level control Default Value: 0 **0x0: NORMAL :** input mode: FIFO not full; output mode: FIFO not empty **0x1: MID :** input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full
9	FIFO1_CLR_1	FIFO clear Default Value: 0 **0x0: NORMAL :** Normal FIFO operation

18.1.16 UDB_WRKMULT_ACTL0 (continued)

		0x1: CLEAR : Clear FIFO state
8	FIFO0_CLR_1	FIFO clear Default Value: 0
		0x0: NORMAL : Normal FIFO operation
		0x1: CLEAR : Clear FIFO state
5	CNT_START_0	Control Register Counter Enable Default Value: 0
		0x0: DISABLE : Counter disabled
		0x1: ENABLE : Counter enabled
4	INT_EN_0	enable interrupt Default Value: 0
		0x0: DISABLE : Interrupt disabled
		0x1: ENABLE : Interrupt enabled
3	FIFO1_LVL_0	FIFO fill status level control Default Value: 0
		0x0: NORMAL : input mode: FIFO not full; output mode: FIFO not empty
		0x1: MID : input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full
2	FIFO0_LVL_0	FIFO fill status level control Default Value: 0
		0x0: NORMAL : input mode: FIFO not full; output mode: FIFO not empty
		0x1: MID : input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full
1	FIFO1_CLR_0	FIFO clear Default Value: 0
		0x0: NORMAL : Normal FIFO operation
		0x1: CLEAR : Clear FIFO state
0	FIFO0_CLR_0	FIFO clear Default Value: 0
		0x0: NORMAL : Normal FIFO operation
		0x1: CLEAR : Clear FIFO state

18.1.17 UDB_WRKMULT_MC0

PLD Macrocell reading

Address: 0x40341A00

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	RW				RW			
Name	PLD1_MC_0 [7:4]				PLD0_MC_0 [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	R				R			
HW Access	RW				RW			
Name	PLD1_MC_1 [15:12]				PLD0_MC_1 [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	R				R			
HW Access	RW				RW			
Name	PLD1_MC_2 [23:20]				PLD0_MC_2 [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	R				R			
HW Access	RW				RW			
Name	PLD1_MC_3 [31:28]				PLD0_MC_3 [27:24]			

Bits	Name	Description
31 : 28	PLD1_MC_3	Read Macrocell 1 for UDB[n+3] Default Value: 0
27 : 24	PLD0_MC_3	Read Macrocell 0 for UDB[n+3] Default Value: 0
23 : 20	PLD1_MC_2	Read Macrocell 1 for UDB[n+2] Default Value: 0
19 : 16	PLD0_MC_2	Read Macrocell 0 for UDB[n+2] Default Value: 0
15 : 12	PLD1_MC_1	Read Macrocell 1 for UDB[n+1] Default Value: 0
11 : 8	PLD0_MC_1	Read Macrocell 0 for UDB[n+1] Default Value: 0
7 : 4	PLD1_MC_0	Read Macrocell 1 for UDB[n] Default Value: 0
3 : 0	PLD0_MC_0	Read Macrocell 0 for UDB[n] Default Value: 0

18.1.18 UDB_UDBPAIR0_UDBSNG0_PLD_IT0

PLD Input Terms

Address: 0x40342000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_INx-_C_-FOR_PT7	PLD0_INx-_C_-FOR_PT6	PLD0_INx-_C_-FOR_PT5	PLD0_INx-_C_-FOR_PT4	PLD0_INx-_C_-FOR_PT3	PLD0_INx-_C_-FOR_PT2	PLD0_INx-_C_-FOR_PT1	PLD0_INx-_C_-FOR_PT0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_INx-_C_-FOR_PT7	PLD1_INx-_C_-FOR_PT6	PLD1_INx-_C_-FOR_PT5	PLD1_INx-_C_-FOR_PT4	PLD1_INx-_C_-FOR_PT3	PLD1_INx-_C_-FOR_PT2	PLD1_INx-_C_-FOR_PT1	PLD1_INx-_C_-FOR_PT0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_INx-_T_-FOR_PT7	PLD0_INx-_T_-FOR_PT6	PLD0_INx-_T_-FOR_PT5	PLD0_INx-_T_-FOR_PT4	PLD0_INx-_T_-FOR_PT3	PLD0_INx-_T_-FOR_PT2	PLD0_INx-_T_-FOR_PT1	PLD0_INx-_T_-FOR_PT0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_INx-_T_-FOR_PT7	PLD1_INx-_T_-FOR_PT6	PLD1_INx-_T_-FOR_PT5	PLD1_INx-_T_-FOR_PT4	PLD1_INx-_T_-FOR_PT3	PLD1_INx-_T_-FOR_PT2	PLD1_INx-_T_-FOR_PT1	PLD1_INx-_T_-FOR_PT0

Bits	Name	Description
31	PLD1_INx_T_FOR_PT7	True input term Default Value: X
30	PLD1_INx_T_FOR_PT6	True input term Default Value: X
29	PLD1_INx_T_FOR_PT5	True input term Default Value: X
28	PLD1_INx_T_FOR_PT4	True input term Default Value: X
27	PLD1_INx_T_FOR_PT3	True input term Default Value: X

18.1.18 UDB_UDBPAIR0_UDBSNG0_PLD_IT0 (continued)

26	PLD1_INx_T_FOR_PT2	True input term Default Value: X
25	PLD1_INx_T_FOR_PT1	True input term Default Value: X
24	PLD1_INx_T_FOR_PT0	True input term Default Value: X
23	PLD0_INx_T_FOR_PT7	True input term Default Value: X
22	PLD0_INx_T_FOR_PT6	True input term Default Value: X
21	PLD0_INx_T_FOR_PT5	True input term Default Value: X
20	PLD0_INx_T_FOR_PT4	True input term Default Value: X
19	PLD0_INx_T_FOR_PT3	True input term Default Value: X
18	PLD0_INx_T_FOR_PT2	True input term Default Value: X
17	PLD0_INx_T_FOR_PT1	True input term Default Value: X
16	PLD0_INx_T_FOR_PT0	True input term Default Value: X
15	PLD1_INx_C_FOR_PT7	Complement input term Default Value: X
14	PLD1_INx_C_FOR_PT6	Complement input term Default Value: X
13	PLD1_INx_C_FOR_PT5	Complement input term Default Value: X
12	PLD1_INx_C_FOR_PT4	Complement input term Default Value: X
11	PLD1_INx_C_FOR_PT3	Complement input term Default Value: X
10	PLD1_INx_C_FOR_PT2	Complement input term Default Value: X
9	PLD1_INx_C_FOR_PT1	Complement input term Default Value: X
8	PLD1_INx_C_FOR_PT0	Complement input term Default Value: X
7	PLD0_INx_C_FOR_PT7	Complement input term Default Value: X
6	PLD0_INx_C_FOR_PT6	Complement input term Default Value: X
5	PLD0_INx_C_FOR_PT5	Complement input term Default Value: X

18.1.18 UDB_UDBPAIR0_UDBSNG0_PLD_IT0 (continued)

4	PLD0_INx_C_FOR_PT4	Complement input term Default Value: X
3	PLD0_INx_C_FOR_PT3	Complement input term Default Value: X
2	PLD0_INx_C_FOR_PT2	Complement input term Default Value: X
1	PLD0_INx_C_FOR_PT1	Complement input term Default Value: X
0	PLD0_INx_C_FOR_PT0	Complement input term Default Value: X

18.1.19 UDB_UDBPAIR0_UDBSNG0_PLD_ORT0

PLD OR Terms

Address: 0x40342030

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_PT7_T_-FOR_OUT0	PLD0_PT6_T_-FOR_OUT0	PLD0_PT5_T_-FOR_OUT0	PLD0_PT4_T_-FOR_OUT0	PLD0_PT3_T_-FOR_OUT0	PLD0_PT2_T_-FOR_OUT0	PLD0_PT1_T_-FOR_OUT0	PLD0_PT0_T_-FOR_OUT0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_PT7_T_-FOR_OUT0	PLD1_PT6_T_-FOR_OUT0	PLD1_PT5_T_-FOR_OUT0	PLD1_PT4_T_-FOR_OUT0	PLD1_PT3_T_-FOR_OUT0	PLD1_PT2_T_-FOR_OUT0	PLD1_PT1_T_-FOR_OUT0	PLD1_PT0_T_-FOR_OUT0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_PT7_T_-FOR_OUT1	PLD0_PT6_T_-FOR_OUT1	PLD0_PT5_T_-FOR_OUT1	PLD0_PT4_T_-FOR_OUT1	PLD0_PT3_T_-FOR_OUT1	PLD0_PT2_T_-FOR_OUT1	PLD0_PT1_T_-FOR_OUT1	PLD0_PT0_T_-FOR_OUT1

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_PT7_T_-FOR_OUT1	PLD1_PT6_T_-FOR_OUT1	PLD1_PT5_T_-FOR_OUT1	PLD1_PT4_T_-FOR_OUT1	PLD1_PT3_T_-FOR_OUT1	PLD1_PT2_T_-FOR_OUT1	PLD1_PT1_T_-FOR_OUT1	PLD1_PT0_T_-FOR_OUT1

Bits	Name	Description
31	PLD1_PT7_T_-FOR_OUT1	OR term Default Value: X
30	PLD1_PT6_T_-FOR_OUT1	OR term Default Value: X
29	PLD1_PT5_T_-FOR_OUT1	OR term Default Value: X
28	PLD1_PT4_T_-FOR_OUT1	OR term Default Value: X
27	PLD1_PT3_T_-FOR_OUT1	OR term Default Value: X

18.1.19 UDB_UDBPAIR0_UDBSNG0_PLD_ORT0 (continued)

26	PLD1_PT2_T_-FOR_OUT1	OR term Default Value: X
25	PLD1_PT1_T_-FOR_OUT1	OR term Default Value: X
24	PLD1_PT0_T_-FOR_OUT1	OR term Default Value: X
23	PLD0_PT7_T_-FOR_OUT1	OR term Default Value: X
22	PLD0_PT6_T_-FOR_OUT1	OR term Default Value: X
21	PLD0_PT5_T_-FOR_OUT1	OR term Default Value: X
20	PLD0_PT4_T_-FOR_OUT1	OR term Default Value: X
19	PLD0_PT3_T_-FOR_OUT1	OR term Default Value: X
18	PLD0_PT2_T_-FOR_OUT1	OR term Default Value: X
17	PLD0_PT1_T_-FOR_OUT1	OR term Default Value: X
16	PLD0_PT0_T_-FOR_OUT1	OR term Default Value: X
15	PLD1_PT7_T_-FOR_OUT0	OR term Default Value: X
14	PLD1_PT6_T_-FOR_OUT0	OR term Default Value: X
13	PLD1_PT5_T_-FOR_OUT0	OR term Default Value: X
12	PLD1_PT4_T_-FOR_OUT0	OR term Default Value: X
11	PLD1_PT3_T_-FOR_OUT0	OR term Default Value: X
10	PLD1_PT2_T_-FOR_OUT0	OR term Default Value: X
9	PLD1_PT1_T_-FOR_OUT0	OR term Default Value: X
8	PLD1_PT0_T_-FOR_OUT0	OR term Default Value: X
7	PLD0_PT7_T_-FOR_OUT0	OR term Default Value: X
6	PLD0_PT6_T_-FOR_OUT0	OR term Default Value: X
5	PLD0_PT5_T_-FOR_OUT0	OR term Default Value: X

18.1.19 UDB_UDBPAIR0_UDBSNG0_PLD_ORT0 (continued)

4	PLD0_PT4_T_- FOR_OUT0	OR term Default Value: X
3	PLD0_PT3_T_- FOR_OUT0	OR term Default Value: X
2	PLD0_PT2_T_- FOR_OUT0	OR term Default Value: X
1	PLD0_PT1_T_- FOR_OUT0	OR term Default Value: X
0	PLD0_PT0_T_- FOR_OUT0	OR term Default Value: X

18.1.20 UDB_UDBPAIR0_UDBSNG0_PLD_ORT1

PLD OR Terms

Address: 0x40342034

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_PT7_T_-FOR_OUT2	PLD0_PT6_T_-FOR_OUT2	PLD0_PT5_T_-FOR_OUT2	PLD0_PT4_T_-FOR_OUT2	PLD0_PT3_T_-FOR_OUT2	PLD0_PT2_T_-FOR_OUT2	PLD0_PT1_T_-FOR_OUT2	PLD0_PT0_T_-FOR_OUT2

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_PT7_T_-FOR_OUT2	PLD1_PT6_T_-FOR_OUT2	PLD1_PT5_T_-FOR_OUT2	PLD1_PT4_T_-FOR_OUT2	PLD1_PT3_T_-FOR_OUT2	PLD1_PT2_T_-FOR_OUT2	PLD1_PT1_T_-FOR_OUT2	PLD1_PT0_T_-FOR_OUT2

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_PT7_T_-FOR_OUT3	PLD0_PT6_T_-FOR_OUT3	PLD0_PT5_T_-FOR_OUT3	PLD0_PT4_T_-FOR_OUT3	PLD0_PT3_T_-FOR_OUT3	PLD0_PT2_T_-FOR_OUT3	PLD0_PT1_T_-FOR_OUT3	PLD0_PT0_T_-FOR_OUT3

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_PT7_T_-FOR_OUT3	PLD1_PT6_T_-FOR_OUT3	PLD1_PT5_T_-FOR_OUT3	PLD1_PT4_T_-FOR_OUT3	PLD1_PT3_T_-FOR_OUT3	PLD1_PT2_T_-FOR_OUT3	PLD1_PT1_T_-FOR_OUT3	PLD1_PT0_T_-FOR_OUT3

Bits	Name	Description
31	PLD1_PT7_T_-FOR_OUT3	OR term Default Value: X
30	PLD1_PT6_T_-FOR_OUT3	OR term Default Value: X
29	PLD1_PT5_T_-FOR_OUT3	OR term Default Value: X
28	PLD1_PT4_T_-FOR_OUT3	OR term Default Value: X
27	PLD1_PT3_T_-FOR_OUT3	OR term Default Value: X

18.1.20 UDB_UDBPAIR0_UDBSNG0_PLD_ORT1 (continued)

26	PLD1_PT2_T_-FOR_OUT3	OR term Default Value: X
25	PLD1_PT1_T_-FOR_OUT3	OR term Default Value: X
24	PLD1_PT0_T_-FOR_OUT3	OR term Default Value: X
23	PLD0_PT7_T_-FOR_OUT3	OR term Default Value: X
22	PLD0_PT6_T_-FOR_OUT3	OR term Default Value: X
21	PLD0_PT5_T_-FOR_OUT3	OR term Default Value: X
20	PLD0_PT4_T_-FOR_OUT3	OR term Default Value: X
19	PLD0_PT3_T_-FOR_OUT3	OR term Default Value: X
18	PLD0_PT2_T_-FOR_OUT3	OR term Default Value: X
17	PLD0_PT1_T_-FOR_OUT3	OR term Default Value: X
16	PLD0_PT0_T_-FOR_OUT3	OR term Default Value: X
15	PLD1_PT7_T_-FOR_OUT2	OR term Default Value: X
14	PLD1_PT6_T_-FOR_OUT2	OR term Default Value: X
13	PLD1_PT5_T_-FOR_OUT2	OR term Default Value: X
12	PLD1_PT4_T_-FOR_OUT2	OR term Default Value: X
11	PLD1_PT3_T_-FOR_OUT2	OR term Default Value: X
10	PLD1_PT2_T_-FOR_OUT2	OR term Default Value: X
9	PLD1_PT1_T_-FOR_OUT2	OR term Default Value: X
8	PLD1_PT0_T_-FOR_OUT2	OR term Default Value: X
7	PLD0_PT7_T_-FOR_OUT2	OR term Default Value: X
6	PLD0_PT6_T_-FOR_OUT2	OR term Default Value: X
5	PLD0_PT5_T_-FOR_OUT2	OR term Default Value: X

4	PLD0_PT4_T_-FOR_OUT2	OR term Default Value: X
3	PLD0_PT3_T_-FOR_OUT2	OR term Default Value: X
2	PLD0_PT2_T_-FOR_OUT2	OR term Default Value: X
1	PLD0_PT1_T_-FOR_OUT2	OR term Default Value: X
0	PLD0_PT0_T_-FOR_OUT2	OR term Default Value: X

18.1.21 UDB_UDBPAIR0_UDBSNG0_PLD_CFG0

PLD configuration for Carry Enable, Constant, and XOR feedback

Address: 0x40342038

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_MC3_DFF_C	PLD0_MC3_CEN	PLD0_MC2_DFF_C	PLD0_MC2_CEN	PLD0_MC1_DFF_C	PLD0_MC1_CEN	PLD0_MC0_DFF_C	PLD0_MC0_CEN

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_MC3_DFF_C	PLD1_MC3_CEN	PLD1_MC2_DFF_C	PLD1_MC2_CEN	PLD1_MC1_DFF_C	PLD1_MC1_CEN	PLD1_MC0_DFF_C	PLD1_MC0_CEN

Bits	23	22	21	20	19	18	17	16
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	PLD0_MC3_XORFB [23:22]		PLD0_MC2_XORFB [21:20]		PLD0_MC1_XORFB [19:18]		PLD0_MC0_XORFB [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	PLD1_MC3_XORFB [31:30]		PLD1_MC2_XORFB [29:28]		PLD1_MC1_XORFB [27:26]		PLD1_MC0_XORFB [25:24]	

Bits	Name	Description
31 : 30	PLD1_MC3_XORFB	XOR feedback Default Value: X **0x0: DFF :** DFF **0x1: CARRY :** Carry **0x2: TFF_H :** TFF on high **0x3: TFF_L :** TFF on low
29 : 28	PLD1_MC2_XORFB	XOR feedback Default Value: X

18.1.21 UDB_UDBPAIR0_UDBSNG0_PLD_CFG0 (continued)

		0x0: DFF : DFF **0x1: CARRY :** Carry **0x2: TFF_H :** TFF on high **0x3: TFF_L :** TFF on low
27 : 26	PLD1_MC1_XORFB	XOR feedback Default Value: X **0x0: DFF :** DFF **0x1: CARRY :** Carry **0x2: TFF_H :** TFF on high **0x3: TFF_L :** TFF on low
25 : 24	PLD1_MC0_XORFB	XOR feedback Default Value: X **0x0: DFF :** DFF **0x1: CARRY :** Carry **0x2: TFF_H :** TFF on high **0x3: TFF_L :** TFF on low
23 : 22	PLD0_MC3_XORFB	XOR feedback Default Value: X **0x0: DFF :** DFF **0x1: CARRY :** Carry **0x2: TFF_H :** TFF on high **0x3: TFF_L :** TFF on low
21 : 20	PLD0_MC2_XORFB	XOR feedback Default Value: X **0x0: DFF :** DFF **0x1: CARRY :** Carry

18.1.21 UDB_UDBPAIR0_UDBSNG0_PLD_CFG0 (continued)

		0x2: TFF_H : TFF on high
		0x3: TFF_L : TFF on low
19 : 18	PLD0_MC1_XORFB	XOR feedback Default Value: X
		0x0: DFF : DFF
		0x1: CARRY : Carry
		0x2: TFF_H : TFF on high
		0x3: TFF_L : TFF on low
17 : 16	PLD0_MC0_XORFB	XOR feedback Default Value: X
		0x0: DFF : DFF
		0x1: CARRY : Carry
		0x2: TFF_H : TFF on high
		0x3: TFF_L : TFF on low
15	PLD1_MC3_DFF_C	DFF Constant Default Value: X
		0x0: NOINV : DFF non-inverted
		0x1: INVERTED : DFF inverted
14	PLD1_MC3_CEN	Carry enable Default Value: X
		0x0: DISABLE : Disabled
		0x1: ENABLE : Enabled
13	PLD1_MC2_DFF_C	DFF Constant Default Value: X
		0x0: NOINV : DFF non-inverted
		0x1: INVERTED : DFF inverted
12	PLD1_MC2_CEN	Carry enable Default Value: X

18.1.21 UDB_UDBPAIR0_UDBSNG0_PLD_CFG0 (continued)

		0x0: DISABLE : Disabled **0x1: ENABLE :** Enabled
11	PLD1_MC1_DFF_C	DFF Constant Default Value: X **0x0: NOINV :** DFF non-inverted **0x1: INVERTED :** DFF inverted
10	PLD1_MC1_CEN	Carry enable Default Value: X **0x0: DISABLE :** Disabled **0x1: ENABLE :** Enabled
9	PLD1_MC0_DFF_C	DFF Constant Default Value: X **0x0: NOINV :** DFF non-inverted **0x1: INVERTED :** DFF inverted
8	PLD1_MC0_CEN	Carry enable Default Value: X **0x0: DISABLE :** Disabled **0x1: ENABLE :** Enabled
7	PLD0_MC3_DFF_C	DFF Constant Default Value: X **0x0: NOINV :** DFF non-inverted **0x1: INVERTED :** DFF inverted
6	PLD0_MC3_CEN	Carry enable Default Value: X **0x0: DISABLE :** Disabled **0x1: ENABLE :** Enabled
5	PLD0_MC2_DFF_C	DFF Constant Default Value: X **0x0: NOINV :** DFF non-inverted

18.1.21 UDB_UDBPAIR0_UDBSNG0_PLD_CFG0 (continued)

		0x1: INVERTED : DFF inverted
4	PLD0_MC2_CEN	Carry enable Default Value: X **0x0: DISABLE :** Disabled **0x1: ENABLE :** Enabled
3	PLD0_MC1_DFF_C	DFF Constant Default Value: X **0x0: NOINV :** DFF non-inverted **0x1: INVERTED :** DFF inverted
2	PLD0_MC1_CEN	Carry enable Default Value: X **0x0: DISABLE :** Disabled **0x1: ENABLE :** Enabled
1	PLD0_MC0_DFF_C	DFF Constant Default Value: X **0x0: NOINV :** DFF non-inverted **0x1: INVERTED :** DFF inverted
0	PLD0_MC0_CEN	Carry enable Default Value: X **0x0: DISABLE :** Disabled **0x1: ENABLE :** Enabled

18.1.22 UDB_UDBPAIR0_UDBSNG0_PLD_CFG1

PLD configuration for Set / Reset selection, and Bypass control

Address: 0x4034203C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_MC3_RESET_SEL	PLD0_MC3_SET_SEL	PLD0_MC2_RESET_SEL	PLD0_MC2_SET_SEL	PLD0_MC1_RESET_SEL	PLD0_MC1_SET_SEL	PLD0_MC0_RESET_SEL	PLD0_MC0_SET_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_MC3_RESET_SEL	PLD1_MC3_SET_SEL	PLD1_MC2_RESET_SEL	PLD1_MC2_SET_SEL	PLD1_MC1_RESET_SEL	PLD1_MC1_SET_SEL	PLD1_MC0_RESET_SEL	PLD1_MC0_SET_SEL

Bits	23	22	21	20	19	18	17	16
SW Access	None	RW	None	RW	None	RW	None	RW
HW Access	None	R	None	R	None	R	None	R
Name	None	PLD0_MC3_BYPASS	None	PLD0_MC2_BYPASS	None	PLD0_MC1_BYPASS	None	PLD0_MC0_BYPASS

Bits	31	30	29	28	27	26	25	24
SW Access	None	RW	None	RW	None	RW	None	RW
HW Access	None	R	None	R	None	R	None	R
Name	None	PLD1_MC3_BYPASS	None	PLD1_MC2_BYPASS	None	PLD1_MC1_BYPASS	None	PLD1_MC0_BYPASS

Bits	Name	Description
30	PLD1_MC3_BYPASS	Bypass selection Default Value: X **0x0: REGISTER :** Registered output **0x1: COMBINATIONAL :** Combinational output
28	PLD1_MC2_BYPASS	Bypass selection Default Value: X **0x0: REGISTER :** Registered output **0x1: COMBINATIONAL :** Combinational output

18.1.22 UDB_UDBPAIR0_UDBSNG0_PLD_CFG1 (continued)

26	PLD1_MC1_BYPASS	Bypass selection Default Value: X **0x0: REGISTER :** Registered output **0x1: COMBINATIONAL :** Combinational output
24	PLD1_MC0_BYPASS	Bypass selection Default Value: X **0x0: REGISTER :** Registered output **0x1: COMBINATIONAL :** Combinational output
22	PLD0_MC3_BYPASS	Bypass selection Default Value: X **0x0: REGISTER :** Registered output **0x1: COMBINATIONAL :** Combinational output
20	PLD0_MC2_BYPASS	Bypass selection Default Value: X **0x0: REGISTER :** Registered output **0x1: COMBINATIONAL :** Combinational output
18	PLD0_MC1_BYPASS	Bypass selection Default Value: X **0x0: REGISTER :** Registered output **0x1: COMBINATIONAL :** Combinational output
16	PLD0_MC0_BYPASS	Bypass selection Default Value: X **0x0: REGISTER :** Registered output **0x1: COMBINATIONAL :** Combinational output
15	PLD1_MC3_RESET_SEL	Reset select enable Default Value: X **0x0: DISABLE :** Reset not used **0x1: ENABLE :** Reset enabled
14	PLD1_MC3_SET_SEL	Set select enable Default Value: X

18.1.22 UDB_UDBPAIR0_UDBSNG0_PLD_CFG1 (continued)

		0x0: DISABLE: Set not used **0x1: ENABLE :** Set enabled
13	PLD1_MC2_RESET_SEL	Reset select enable Default Value: X **0x0: DISABLE :** Reset not used **0x1: ENABLE :** Reset enabled
12	PLD1_MC2_SET_SEL	Set select enable Default Value: X **0x0: DISABLE :** Set not used **0x1: ENABLE :** Set enabled
11	PLD1_MC1_RESET_SEL	Reset select enable Default Value: X **0x0: DISABLE :** Reset not used **0x1: ENABLE :** Reset enabled
10	PLD1_MC1_SET_SEL	Set select enable Default Value: X **0x0: DISABLE :** Set not used **0x1: ENABLE :** Set enabled
9	PLD1_MC0_RESET_SEL	Reset select enable Default Value: X **0x0: DISABLE :** Reset not used **0x1: ENABLE :** Reset enabled
8	PLD1_MC0_SET_SEL	Set select enable Default Value: X **0x0: DISABLE :** Set not used **0x1: ENABLE :** Set enabled
7	PLD0_MC3_RESET_SEL	Reset select enable Default Value: X **0x0: DISABLE :** Reset not used

18.1.22 UDB_UDBPAIR0_UDBSNG0_PLD_CFG1 (continued)

		0x1: ENABLE : Reset enabled
6	PLD0_MC3_SET_SEL	Set select enable Default Value: X **0x0: DISABLE :** Set not used **0x1: ENABLE :** Set enabled
5	PLD0_MC2_RESET_SEL	Reset select enable Default Value: X **0x0: DISABLE :** Reset not used **0x1: ENABLE :** Reset enabled
4	PLD0_MC2_SET_SEL	Set select enable Default Value: X **0x0: DISABLE :** Set not used **0x1: ENABLE :** Set enabled
3	PLD0_MC1_RESET_SEL	Reset select enable Default Value: X **0x0: DISABLE :** Reset not used **0x1: ENABLE :** Reset enabled
2	PLD0_MC1_SET_SEL	Set select enable Default Value: X **0x0: DISABLE :** Set not used **0x1: ENABLE :** Set enabled
1	PLD0_MC0_RESET_SEL	Reset select enable Default Value: X **0x0: DISABLE :** Reset not used **0x1: ENABLE :** Reset enabled
0	PLD0_MC0_SET_SEL	Set select enable Default Value: X **0x0: DISABLE :** Set not used **0x1: ENABLE :** Set enabled

18.1.23 UDB_UDBPAIR0_UDBSNG0_DPATH_CFG0

Datapath input selections (RAD0, RAD1, RAD2, F0_LD, F1_LD, D0_LD, D1_LD)

Address: 0x40342040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	RAD1 [6:4]			None	RAD0 [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW		
HW Access	R	R	R	R	R	R		
Name	DP_RTE_BYPASS4	DP_RTE_BYPASS3	DP_RTE_BYPASS2	DP_RTE_BYPASS1	DP_RTE_BYPASS0	RAD2 [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	None	RW			RW	RW		
HW Access	None	R			R	R		
Name	None	F1_LD [22:20]			DP_RTE_BYPASS5	F0_LD [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	D1_LD [30:28]			None	D0_LD [26:24]		

Bits	Name	Description
30 : 28	D1_LD	Datapath Permutable Input Mux Default Value: 0 **0x0: OFF :** Input off **0x1: DP_IN0 :** Set to dp_in[0] **0x2: DP_IN1 :** Set to dp_in[1] **0x3: DP_IN2 :** Set to dp_in[2] **0x4: DP_IN3 :** Set to dp_in[3] **0x5: DP_IN4 :** Set to dp_in[4]

18.1.23 UDB_UDBPAIR0_UDBSNG0_DPATH_CFG0 (continued)

		0x6: DP_IN5 : Set to dp_in[5] **0x7: RESERVED :** Reserved
26 : 24	D0_LD	Datapath Permutable Input Mux Default Value: 0 **0x0: OFF :** Input off **0x1: DP_IN0 :** Set to dp_in[0] **0x2: DP_IN1 :** Set to dp_in[1] **0x3: DP_IN2 :** Set to dp_in[2] **0x4: DP_IN3 :** Set to dp_in[3] **0x5: DP_IN4 :** Set to dp_in[4] **0x6: DP_IN5 :** Set to dp_in[5] **0x7: RESERVED :** Reserved
22 : 20	F1_LD	Datapath Permutable Input Mux Default Value: 0 **0x0: OFF :** Input off **0x1: DP_IN0 :** Set to dp_in[0] **0x2: DP_IN1 :** Set to dp_in[1] **0x3: DP_IN2 :** Set to dp_in[2] **0x4: DP_IN3 :** Set to dp_in[3] **0x5: DP_IN4 :** Set to dp_in[4] **0x6: DP_IN5 :** Set to dp_in[5] **0x7: RESERVED :** Reserved
19	DP_RTE_BYPASS5	DP_In bypass control Default Value: 0 **0x0: DP_IN5_ROUTE :** Use dp_in[5]

18.1.23 UDB_UDBPAIR0_UDBSNG0_DPATH_CFG0 (continued)

		0x1: DP_IN5_BYPASS : Use dp_out[5] via bypass
18 : 16	F0_LD	Datapath Permutable Input Mux Default Value: 0 **0x0: OFF :** Input off **0x1: DP_IN0 :** Set to dp_in[0] **0x2: DP_IN1 :** Set to dp_in[1] **0x3: DP_IN2 :** Set to dp_in[2] **0x4: DP_IN3 :** Set to dp_in[3] **0x5: DP_IN4 :** Set to dp_in[4] **0x6: DP_IN5 :** Set to dp_in[5] **0x7: RESERVED :** Reserved
15	DP_RTE_BYPASS4	DP_In bypass control Default Value: 0 **0x0: DP_IN4_ROUTE :** Use dp_in[4] **0x1: DP_IN4_BYPASS :** Use dp_out[4] as input via bypass
14	DP_RTE_BYPASS3	DP_In bypass control Default Value: 0 **0x0: DP_IN3_ROUTE :** Use dp_in[3] **0x1: DP_IN3_BYPASS :** Use dp_out[3] as input via bypass
13	DP_RTE_BYPASS2	DP_In bypass control Default Value: 0 **0x0: DP_IN2_ROUTE :** Use dp_in[2] **0x1: DP_IN2_BYPASS :** Use dp_out[2] as input via bypass
12	DP_RTE_BYPASS1	DP_In bypass control Default Value: 0 **0x0: DP_IN1_ROUTE :** Use dp_in[1] **0x1: DP_IN1_BYPASS :** Use dp_out[1] as input via bypass

18.1.23 UDB_UDBPAIR0_UDBSNG0_DPATH_CFG0 (continued)

11	DP_RTE_BYPASS0	DP_In bypass control Default Value: 0 **0x0: DP_IN0_ROUTE :** Use dp_in[0] **0x1: DP_IN0_BYPASS :** Use dp_out[0] as input via bypass
10 : 8	RAD2	Datapath Permutable Input Mux Default Value: 0 **0x0: OFF :** Input off **0x1: DP_IN0 :** Set to dp_in[0] **0x2: DP_IN1 :** Set to dp_in[1] **0x3: DP_IN2 :** Set to dp_in[2] **0x4: DP_IN3 :** Set to dp_in[3] **0x5: DP_IN4 :** Set to dp_in[4] **0x6: DP_IN5 :** Set to dp_in[5] **0x7: RESERVED :** Reserved
6 : 4	RAD1	Datapath Permutable Input Mux Default Value: 0 **0x0: OFF :** Input off **0x1: DP_IN0 :** Set to dp_in[0] **0x2: DP_IN1 :** Set to dp_in[1] **0x3: DP_IN2 :** Set to dp_in[2] **0x4: DP_IN3 :** Set to dp_in[3] **0x5: DP_IN4 :** Set to dp_in[4] **0x6: DP_IN5 :** Set to dp_in[5] **0x7: RESERVED :** Reserved
2 : 0	RAD0	Datapath Permutable Input Mux Default Value: 0

18.1.23 UDB_UDBPAIR0_UDBSNG0_DPATH_CFG0 (continued)

0x0: OFF :
Input off

0x1: DP_IN0 :
Set to dp_in[0]

0x2: DP_IN1 :
Set to dp_in[1]

0x3: DP_IN2 :
Set to dp_in[2]

0x4: DP_IN3 :
Set to dp_in[3]

0x5: DP_IN4 :
Set to dp_in[4]

0x6: DP_IN5 :
Set to dp_in[5]

0x7: RESERVED :
Reserved

18.1.24 UDB_UDBPAIR0_UDBSNG0_DPATH_CFG1

Datapath input and output selections (SCI_MUX, SI_MUX, OUT0 thru OUT5)

Address: 0x40342044

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	CI_MUX [6:4]			None	SI_MUX [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	OUT1 [15:12]				OUT0 [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW			
HW Access	R				R			
Name	OUT3 [23:20]				OUT2 [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	R				R			
Name	OUT5 [31:28]				OUT4 [27:24]			

Bits	Name	Description
31 : 28	OUT5	Datapath Permutable Output Mux Default Value: 0 **0x0: CE0 :** Comparator 0 equal **0x1: CL0 :** Comparator 0 less than **0x2: Z0 :** Accumulator 0 zero detect **0x3: FF0 :** Accumulator 0 ones detect **0x4: CE1 :** Comparator 1 equal **0x5: CL1 :** Comparator 1 less than **0x6: Z1 :** Accumulator 1 zero detect

18.1.24 UDB_UDBPAIR0_UDBSNG0_DPATH_CFG1 (continued)

		0x7: FF1 : Accumulator 1 ones detect **0x8: OV_MSB :** Overflow of MSB **0x9: CO_MSB :** Carry out of MSB **0xa: CMSBO :** CRC MSB **0xb: SO :** Shift out **0xc: F0_BLK_STAT :** FIFO 0 block status defined by direction **0xd: F1_BLK_STAT :** FIFO 1 block status defined by direction **0xe: F0_BUS_STAT :** FIFO 0 bus status defined by direction and level **0xf: F1_BUS_STAT :** FIFO 1 bus status defined by direction and level
27 : 24	OUT4	Datapath Permutable Output Mux Default Value: 0 **0x0: CE0 :** Comparator 0 equal **0x1: CL0 :** Comparator 0 less than **0x2: Z0 :** Accumulator 0 zero detect **0x3: FF0 :** Accumulator 0 ones detect **0x4: CE1 :** Comparator 1 equal **0x5: CL1 :** Comparator 1 less than **0x6: Z1 :** Accumulator 1 zero detect **0x7: FF1 :** Accumulator 1 ones detect **0x8: OV_MSB :** Overflow of MSB **0x9: CO_MSB :** Carry out of MSB **0xa: CMSBO :** CRC MSB **0xb: SO :** Shift out

18.1.24 UDB_UDBPAIR0_UDBSNG0_DPATH_CFG1 (continued)

		0xc: F0_BLK_STAT : FIFO 0 block status defined by direction **0xd: F1_BLK_STAT :** FIFO 1 block status defined by direction **0xe: F0_BUS_STAT :** FIFO 0 bus status defined by direction and level **0xf: F1_BUS_STAT :** FIFO 1 bus status defined by direction and level
23 : 20	OUT3	Datapath Permutable Output Mux Default Value: 0 **0x0: CE0 :** Comparator 0 equal **0x1: CL0 :** Comparator 0 less than **0x2: Z0 :** Accumulator 0 zero detect **0x3: FF0 :** Accumulator 0 ones detect **0x4: CE1 :** Comparator 1 equal **0x5: CL1 :** Comparator 1 less than **0x6: Z1 :** Accumulator 1 zero detect **0x7: FF1 :** Accumulator 1 ones detect **0x8: OV_MSB :** Overflow of MSB **0x9: CO_MSB :** Carry out of MSB **0xa: CMSBO :** CRC MSB **0xb: SO :** Shift out **0xc: F0_BLK_STAT :** FIFO 0 block status defined by direction **0xd: F1_BLK_STAT :** FIFO 1 block status defined by direction **0xe: F0_BUS_STAT :** FIFO 0 bus status defined by direction and level **0xf: F1_BUS_STAT :** FIFO 1 bus status defined by direction and level
19 : 16	OUT2	Datapath Permutable Output Mux Default Value: 0

18.1.24 UDB_UDBPAIR0_UDBSNG0_DPATH_CFG1 (continued)

		0x0: CE0 : Comparator 0 equal **0x1: CL0 :** Comparator 0 less than **0x2: Z0 :** Accumulator 0 zero detect **0x3: FF0 :** Accumulator 0 ones detect **0x4: CE1 :** Comparator 1 equal **0x5: CL1 :** Comparator 1 less than **0x6: Z1 :** Accumulator 1 zero detect **0x7: FF1 :** Accumulator 1 ones detect **0x8: OV_MSB :** Overflow of MSB **0x9: CO_MSB :** Carry out of MSB **0xa: CMSBO :** CRC MSB **0xb: SO :** Shift out **0xc: F0_BLK_STAT :** FIFO 0 block status defined by direction **0xd: F1_BLK_STAT :** FIFO 1 block status defined by direction **0xe: F0_BUS_STAT :** FIFO 0 bus status defined by direction and level **0xf: F1_BUS_STAT :** FIFO 1 bus status defined by direction and level
15 : 12	OUT1	Datapath Permutable Output Mux Default Value: 0 **0x0: CE0 :** Comparator 0 equal **0x1: CL0 :** Comparator 0 less than **0x2: Z0 :** Accumulator 0 zero detect **0x3: FF0 :** Accumulator 0 ones detect **0x4: CE1 :** Comparator 1 equal

18.1.24 UDB_UDBPAIR0_UDBSNG0_DPATH_CFG1 (continued)

		0x5: CL1 : Comparator 1 less than **0x6: Z1 :** Accumulator 1 zero detect **0x7: FF1 :** Accumulator 1 ones detect **0x8: OV_MSB :** Overflow of MSB **0x9: CO_MSB :** Carry out of MSB **0xa: CMSBO :** CRC MSB **0xb: SO :** Shift out **0xc: F0_BLK_STAT :** FIFO 0 block status defined by direction **0xd: F1_BLK_STAT :** FIFO 1 block status defined by direction **0xe: F0_BUS_STAT :** FIFO 0 bus status defined by direction and level **0xf: F1_BUS_STAT :** FIFO 1 bus status defined by direction and level
11 : 8	OUT0	Datapath Permutable Output Mux Default Value: 0 **0x0: CE0 :** Comparator 0 equal **0x1: CL0 :** Comparator 0 less than **0x2: Z0 :** Accumulator 0 zero detect **0x3: FF0 :** Accumulator 0 ones detect **0x4: CE1 :** Comparator 1 equal **0x5: CL1 :** Comparator 1 less than **0x6: Z1 :** Accumulator 1 zero detect **0x7: FF1 :** Accumulator 1 ones detect **0x8: OV_MSB :** Overflow of MSB **0x9: CO_MSB :** Carry out of MSB

18.1.24 UDB_UDBPAIR0_UDBSNG0_DPATH_CFG1 (continued)

		0xa: CMSBO : CRC MSB **0xb: SO :** Shift out **0xc: F0_BLK_STAT :** FIFO 0 block status defined by direction **0xd: F1_BLK_STAT :** FIFO 1 block status defined by direction **0xe: F0_BUS_STAT :** FIFO 0 bus status defined by direction and level **0xf: F1_BUS_STAT :** FIFO 1 bus status defined by direction and level
6 : 4	CI_MUX	Datapath Permutable Input Mux Default Value: 0 **0x0: OFF :** Input off **0x1: DP_IN0 :** Set to dp_in[0] **0x2: DP_IN1 :** Set to dp_in[1] **0x3: DP_IN2 :** Set to dp_in[2] **0x4: DP_IN3 :** Set to dp_in[3] **0x5: DP_IN4 :** Set to dp_in[4] **0x6: DP_IN5 :** Set to dp_in[5] **0x7: RESERVED :** Reserved
2 : 0	SI_MUX	Datapath Permutable Input Mux Default Value: 0 **0x0: OFF :** Input off **0x1: DP_IN0 :** Set to dp_in[0] **0x2: DP_IN1 :** Set to dp_in[1] **0x3: DP_IN2 :** Set to dp_in[2] **0x4: DP_IN3 :** Set to dp_in[3] **0x5: DP_IN4 :** Set to dp_in[4]

18.1.24 UDB_UDBPAIR0_UDBSNG0_DPATH_CFG1 (continued)

0x6: DP_IN5 :
Set to dp_in[5]

0x7: RESERVED :
Reserved

18.1.25 UDB_UDBPAIR0_UDBSNG0_DPATH_CFG2

Datapath output synchronization, ALU mask, compare 0 and 1 masks

Address: 0x40342048

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		OUT_SYNC [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	AMASK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	CMASK0 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	CMASK1 [31:24]							

Bits	Name	Description
31 : 24	CMASK1	Datapath Compare 1 Mask. The mask value in this register is applied to the Accumulator 0 vs Accumulator 1 mux output before it is used for Compare 1 (it does not apply to the Accumulator 0 vs. Data 1 mux output). The CMASK1_EN bit (DPATH_CFG3) must be set for the mask to be operational. Default Value: 0
23 : 16	CMASK0	Datapath Compare 0 Mask. The mask value in this register is applied to the output of the Accumulator 0 before it is used for comparison in Compare block 0. The CMASK0_EN bit (DPATH_CFG3) must be set for the mask to be operational. Default Value: 0
15 : 8	AMASK	Datapath ALU Mask. The mask value in this register is applied to the output of the Datapath ALU result before the result is stored. The AMASK_EN bit (DPATH_CFG3) must be set for the mask to be operational. Default Value: 0
5 : 0	OUT_SYNC	Datapath Output Synchronization. Each datapath output can be registered (default,0), or combinational (1) Default Value: 0

0x0: REGISTERED :
registered

0x1: COMBINATIONAL :
combinational

18.1.26 UDB_UDBPAIR0_UDBSNG0_DPATH_CFG3

Datapath mask enables, shift in, carry in, compare, chaining, MSB configs; FIFO, shift and parallel input control

Address: 0x4034204C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW		RW	
HW Access	R	R	R	R	R		R	
Name	CMASK1_EN	CMASK0_EN	AMASK_EN	DEF_SI	SI_SELB [3:2]		SI_SELA [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	CMP_SELB [15:14]		CMP_SELA [13:12]		CI_SELB [11:10]		CI_SELA [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW			RW	RW	RW	RW
HW Access	R	R			R	R	R	R
Name	MSB_EN	MSB_SEL [22:20]			CHAIN_CMSB	CHAIN_FB	CHAIN1	CHAIN0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW		RW	
HW Access	R	R	R	R	R		R	
Name	PI_SEL	SHIFT_SEL	PI_DYN	MSB_SI	F1_INSEL [27:26]		F0_INSEL [25:24]	

Bits	Name	Description
31	PI_SEL	Datapath parallel input selection Default Value: 0 **0x0: NORMAL :** Normal operation, ALU source is from accumulator selection **0x1: PARALLEL :** ALU source A input is from the parallel data input
30	SHIFT_SEL	Datapath shift out selection Default Value: 0 **0x0: SOL_MSB :** Routed shift out is shift out left (sol_msb) **0x1: SOR :** Routed shift out is shift out right (sor)
29	PI_DYN	Enable for dynamic control of parallel data input (PI) mux. Default Value: 0

18.1.26 UDB_UDBPAIR0_UDBSNG0_DPATH_CFG3 (continued)

		0x0: DISABLE : Parallel input mux select is only controlled by static configuration (PI_SEL). **0x1: ENABLE :** Parallel input mux to the Datapath is controlled by CFB_EN field in Datapath Dynamic RAM. When this mode is enabled, the CFB_EN usage for CRC/PRS functionality is disabled.
28	MSB_SI	Arithmetic shift right operation shift in selection Default Value: 0 **0x0: DEFAULT :** Shift in default value (when SI_SELA and/or SI_SELB == 0) **0x1: MSB :** Override default and shift in MSB value
27 : 26	F1_INSEL	Datapath FIFO Configuration Default Value: 0 **0x0: INPUT :** Input Mode: Write source is the system bus; read destination is corresponding data register or accumulator **0x1: OUTPUT_A0 :** Output Mode: Write source is A0, read destination is the system bus **0x2: OUTPUT_A1 :** Output Mode: Write source is A1, read destination is the system bus **0x3: OUTPUT_ALU :** Output Mode: Write source is the ALU output, read destination is the system bus
25 : 24	F0_INSEL	Datapath FIFO Configuration Default Value: 0 **0x0: INPUT :** Input Mode: Write source is the system bus; read destination is corresponding data register or accumulator **0x1: OUTPUT_A0 :** Output Mode: Write source is A0, read destination is the system bus **0x2: OUTPUT_A1 :** Output Mode: Write source is A1, read destination is the system bus **0x3: OUTPUT_ALU :** Output Mode: Write source is the ALU output, read destination is the system bus
23	MSB_EN	Datapath MSB selection enable Default Value: 0 **0x0: DISABLE :** MSB selection is disabled, MSB is bit 7 **0x1: ENABLE :** MSB selection is controlled by MSB_SEL
22 : 20	MSB_SEL	Datapath MSB Selection Default Value: 0 **0x0: BIT0 :** MSB is bit 0

18.1.26 UDB_UDBPAIR0_UDBSNG0_DPATH_CFG3 (continued)

		0x1: BIT1 : MSB is bit 1 **0x2: BIT2 :** MSB is bit 2 **0x3: BIT3 :** MSB is bit 3 **0x4: BIT4 :** MSB is bit 4 **0x5: BIT5 :** MSB is bit 5 **0x6: BIT6 :** MSB is bit 6 **0x7: BIT7 :** MSB is bit 7 - equivalent to MSB_EN=0
19	CHAIN_CMSB	Datapath CRC MSB chaining enable Default Value: 0 **0x0: DISABLE :** CRC MSB is not chained **0x1: ENABLE :** CRC MSB is chained from the next (MSB) datapath
18	CHAIN_FB	Datapath CRC feedback chaining enable Default Value: 0 **0x0: DISABLE :** CRC feedback is not chained **0x1: ENABLE :** CRC feedback is chained from the previous (LSB) datapath
17	CHAIN1	Datapath condition chaining enable Default Value: 0 **0x0: DISABLE :** Conditions are not chained **0x1: ENABLE :** Conditions are chained from the previous (LSB) datapath
16	CHAIN0	Datapath condition chaining enable Default Value: 0 **0x0: DISABLE :** Conditions are not chained **0x1: ENABLE :** Conditions are chained from the previous (LSB) datapath
15 : 14	CMP_SELB	Datapath compare select Default Value: 0 **0x0: A1_D1 :** Compare A1 to D1 **0x1: A1_A0 :** Compare A1 to A0

18.1.26 UDB_UDBPAIR0_UDBSNG0_DPATH_CFG3 (continued)

		0x2: A0_D1 : Compare A0 to D1
		0x3: A0_A0 : Compare A0 to A0
13 : 12	CMP_SELA	Datapath compare select Default Value: 0
		0x0: A1_D1 : Compare A1 to D1
		0x1: A1_A0 : Compare A1 to A0
		0x2: A0_D1 : Compare A0 to D1
		0x3: A0_A0 : Compare A0 to A0
11 : 10	CI_SELB	Datapath carry in source select Default Value: 0
		0x0: DEFAULT : Default arithmetic mode
		0x1: REGISTERED : Carry in is the carry out registered from previous cycle
		0x2: ROUTE : Carry in is selected from datapath routing input
		0x3: CHAIN : Carry in is chained from the previous datapath
9 : 8	CI_SELA	Datapath carry in source select Default Value: 0
		0x0: DEFAULT : Default arithmetic mode
		0x1: REGISTERED : Carry in is the carry out registered from previous cycle
		0x2: ROUTE : Carry in is selected from datapath routing input
		0x3: CHAIN : Carry in is chained from the previous datapath
7	CMASK1_EN	Datapath mask enable Default Value: 0
		0x0: DISABLE : Masking disabled
		0x1: ENABLE : Masking enabled
6	CMASK0_EN	Datapath mask enable Default Value: 0
		0x0: DISABLE : Masking disabled

18.1.26 UDB_UDBPAIR0_UDBSNG0_DPATH_CFG3 (continued)

		0x1: ENABLE : Masking enabled
5	AMASK_EN	Datapath mask enable Default Value: 0
		0x0: DISABLE : Masking disabled
		0x1: ENABLE : Masking enabled
4	DEF_SI	Datapath default shift value Default Value: 0
		0x0: DEFAULT_0 : Default shift is 0
		0x1: DEFAULT_1 : Default shift is 1
3 : 2	SI_SELB	Datapath shift in source select Default Value: 0
		0x0: DEFAULT : Default value specified in default shift field
		0x1: REGISTERED : Shift in is the shift out registered from previous cycle
		0x2: ROUTE : Shift in is selected from datapath routing input
		0x3: CHAIN : Shift in is chained from the previous datapath
1 : 0	SI_SELA	Datapath shift in source select Default Value: 0
		0x0: DEFAULT : Default value specified in default shift field
		0x1: REGISTERED : Shift in is the shift out registered from previous cycle
		0x2: ROUTE : Shift in is selected from datapath routing input
		0x3: CHAIN : Shift in is chained from the previous datapath

18.1.27 UDB_UDBPAIR0_UDBSNG0_DPATH_CFG4

Datapath FIFO and register access configuration control

Address: 0x40342050

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	None
HW Access	R	R	R	R	R	R	R	None
Name	F1_CK_INV	F0_CK_INV	FIFO_FAST	FIFO_CAP	FI-FO_EDGE	FI-FO_ASYNC	EX-T_CRCPRS	None

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	None		RW	RW
HW Access	None			R	None		R	R
Name	None [15:13]			FIFO_AD-D_SYNC	None [11:10]		F1_DYN	F0_DYN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
12	FIFO_ADD_SYNC	Adds a flop stage to FIFO block status if additional timing margin is needed Default Value: 0 **0x0: DISABLE :** No flop stage is added to the block status calculation **0x1: ENABLE :** 1 flop stage is added to the block status calculation
9	F1_DYN	Default Value: 0 **0x0: STATIC :** Default. FIFO direction is static and controlled by the associated Fx_INSEL bits (DPATH_CFG3). **0x1: DYNAMIC :** The associated FIFO direction is dynamically controlled by the associated 'dx_load' Datapath input signal. When the 'dx_load' signal is '0', the access is internal, where the FIFO is both a source and destination for the Datapath. When the 'dx_load' signal is '1', the access is extenal, where the FIFO is both a source and destination for AHB.

18.1.27 UDB_UDBPAIR0_UDBSNG0_DPATH_CFG4 (continued)

8	F0_DYN	When this bit is set, the associated FIFO configuration may be dynamically controlled. Default Value: 0 **0x0: STATIC :** Default. FIFO direction is static and controlled by the associated Fx_INSEL bits (DPATH_CFG3). **0x1: DYNAMIC :** The associated FIFO direction is dynamically controlled by the associated 'dx_load' Datapath input signal. When the 'dx_load' signal is '0', the access is internal, where the FIFO is both a source and destination for the Datapath. When the 'dx_load' signal is '1', the access is extenal, where the FIFO is both a source and destination for AHB.
7	F1_CK_INV	FIFO Clock Invert. When this bit is set, the polarity of the clock for the given FIFO will be inverted, with respect to the polarity of the selected Datapath clock. Default Value: 0 **0x0: NORMAL :** FIFO clock is the same polarity as the Datapath clock. **0x1: INVERT :** FIFO clock is inverted with respect to the Datapath clock.
6	F0_CK_INV	FIFO Clock Invert. When this bit is set, the polarity of the clock for the given FIFO will be inverted, with respect to the polarity of the selected Datapath clock. Default Value: 0 **0x0: NORMAL :** FIFO clock is the same polarity as the Datapath clock. **0x1: INVERT :** FIFO clock is inverted with respect to the Datapath clock.
5	FIFO_FAST	FIFO Fast Mode. When this bit is set, the FIFO write logic is clocked by the application bus clock. Lowers the latency of capture timing, at the expense of additional power. Default Value: 0 **0x0: DISABLE :** FIFO is clocked with selected Datapath clock. **0x1: ENABLE :** FIFO is clocked with application bus clock. Master and quadrant bus clock gating must be enabled.
4	FIFO_CAP	FIFO Software Capture Mode. When this bit is set, a read of A0 or A1 triggers a capture into F0 or F1 respectively. This function follows the chaining configuration. All accumulators in the chain from a given block to the MS block in the chain are capture Default Value: 0 **0x0: DISABLE :** FIFO capture is disabled. **0x1: ENABLE :** FIFO capture is enabled (FIFO must be in output mode). A read of A0 or A1 will write into F0 or F1.
3	FIFO_EDGE	Edge/level sensitive FIFO write control (Fx_LD). Only applies to FIFO configured in output mode Default Value: 0 **0x0: LEVEL :** FIFO write from accumulators/ALU is level sensitive. FIFO write occurs on a clock edge whenever the write control is sampled high on that edge.

18.1.27 UDB_UDBPAIR0_UDBSNG0_DPATH_CFG4 (continued)

		0x1: EDGE : FIFO write from accumulators/ALU is edge sensitive. FIFO write occurs on a clock edge following a 0 to 1 transition on the write control. The write control must be negated for at least one full cycle of the FIFO clock for a subsequent transition to be deleted.
2	FIFO_ASYNC	Asynchronous FIFO clocking support Default Value: 0
		0x0: DISABLE : FIFO clocks are synchronous
		0x1: ENABLE : FIFO clocks are asynchronous
1	EXT_CRCPRS	External CRC/PRS mode Default Value: 0
		0x0: INTERNAL : Internal CRC/PRS routing
		0x1: EXTERNAL : External CRC/PRS routing

18.1.28 UDB_UDBPAIR0_UDBSNG0_SC_CFG0

SC Mode 0 and 1 control registers; status register input mode; general SC configuration

Address: 0x40342054

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CTL_MD0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CTL_MD1 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	STAT_MD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None			RW	RW	RW	RW	
HW Access	None			R	R	R	R	
Name	None [31:29]			SC_EX-T_RES	SC_SYN-C_MD	SC_INT_MD	SC_OUT_CTL [25:24]	

Bits	Name	Description
28	SC_EXT_RES	Control register external reset operation. This bit supports autonomous usage of the control register, where a routed reset should clear the writable input registers. By default this is off because the CPU writable register can be cleared in firmware. Default Value: 0 **0x0: DISABLED :** When a routed reset is applied to the control register, only embedded state (sampling registers) are cleared **0x1: ENABLED :** When a routed reset is applied to the control register, all state is cleared, including the CPU writable control bits.
27	SC_SYNC_MD	SC Sync Mode - controls when the status register operates as a 4-bit double synchronizer module Default Value: 0 **0x0: NORMAL :** Normal Mode - Status register operation

18.1.28 UDB_UDBPAIR0_UDBSNG0_SC_CFG0 (continued)

		0x1: SYNC_MODE : Sync Mode - Routing inputs sc_in[3:0] are the 4 sync inputs, and connections sc_io[3:0] operate as the sync outputs
26	SC_INT_MD	SC Interrupt Mode - controls when the UDB driving an interrupt generated from the masked OR reduction of status bits 6 to 0 Default Value: 0 **0x0: NORMAL :** Normal Mode - Routing connection sc_io[3] is a normal input to the status register **0x1: INT_MODE :** Interrupt Mode - Routing connection sc_io[3] operates as the UDB interrupt output
25 : 24	SC_OUT_CTL	Selects the output source for the Status and Control routing connections Default Value: 0 **0x0: CONTROL :** Control out, 8-bits of control are driven to the routing connections **0x1: PARALLEL :** Datapath parallel output, 8-bits of datapath parallel output data are driven to the routing connections **0x2: COUNTER :** Counter out, 7-bits of count and 1 bit (MSB) of terminal count are driven to the routing connections **0x3: RESERVED :** Reserved
23 : 16	STAT_MD	Mode selection for each bit of the status register. A '0' is transparent mode, where internal routing is read indrectly by CPU firmware. A '1' is sticky-clear-on-read mode, where once the given bit is set, it will stay set until the CPU reads the bit. Default Value: 0
15 : 8	CTL_MD1	CTL_MD1 and CTL_MD0 are concatenated to form an encoding for the mode of each control bit in the control register. Default Value: 0 **0x0: DIRECT :** The value written to that bit drives directly into the routing. **0x1: SYNC :** The value written is resampled by the selected SC clock. The resampled value is driven into the routing. **0x2: DOUBLE_SYNC :** The value written is doubly synced by the selected SC clock. The synched value is driven into the routing. **0x3: PULSE :** The value written is resampled and a synchronous pulse is generated and driven into the routing based on the selected SC clock. At the end of the generated pulse, the control register bit is automatically reset.
7 : 0	CTL_MD0	CTL_MD1 and CTL_MD0 are concatenated to form an encoding for the mode of each control bit in the control register. Default Value: 0 **0x0: DIRECT :** The value written to that bit drives directly into the routing.

18.1.28 UDB_UDBPAIR0_UDBSNG0_SC_CFG0 (continued)

0x1: SYNC :
The value written is resampled by the selected SC clock. The resampled value is driven into the routing.

0x2: DOUBLE_SYNC :
The value written is doubly synced by the selected SC clock. The synched value is driven into the routing.

0x3: PULSE :
The value written is resampled and a synchronous pulse is generated and driven into the routing based on the selected SC clock. At the end of the generated pulse, the control register bit is automatically reset.

18.1.29 UDB_UDBPAIR0_UDBSNG0_SC_CFG1

SC counter control

Address: 0x40342058

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	RW	RW	RW		RW	
HW Access	None	R	R	R	R		R	
Name	None	ALT_CNT	ROUTE_EN	ROUTE_LD	CNT_EN_SEL [3:2]		CNT_LD_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
6	ALT_CNT	Configure the alternate operating mode of the counter Default Value: 0 **0x0: DEFAULT_MODE :** Default counter operating mode **0x1: ALT_MODE :** Alternate counter operating mode
5	ROUTE_EN	Configure the counter enable signal for routing input Default Value: 0 **0x0: DISABLE :** Routed EN signal is not used. EN signal is only controlled by firmware CNT START (ACTL register) **0x1: ROUTED :** Routed EN signal is used, CNT START must be set
4	ROUTE_LD	Configure the counter load signal for routing input Default Value: 0

18.1.29 UDB_UDBPAIR0_UDBSNG0_SC_CFG1 (continued)

		0x0: DISABLE : Routed LD signal is not used **0x1: ROUTED :** Routed LD signal is used
3 : 2	CNT_EN_SEL	Selects the routing inputs for the counter enable signal Default Value: 0 **0x0: SC_IN4 :** sc_io_in[0] **0x1: SC_IN5 :** sc_io_in[1] **0x2: SC_IN6 :** sc_io_in[2] **0x3: SC_IO :** sc_io_in[3]
1 : 0	CNT_LD_SEL	Selects the routing inputs for the counter load signal Default Value: 0 **0x0: SC_IN0 :** sc_in[0] **0x1: SC_IN1 :** sc_in[1] **0x2: SC_IN2 :** sc_in[2] **0x3: SC_IN3 :** sc_in[3]

18.1.30 UDB_UDBPAIR0_UDBSNG0_RC_CFG0

PLD0, PLD1, Datatpath, and SC clock and reset control

Address: 0x4034205C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW		RW	
HW Access	R	R	R	R	R		R	
Name	PLD0_RC_RES_SEL1	PLD0_RC_RES_-SEL0_OR_-FRES	PLD0_RC_-INV	PLD0_RC_EN_INV	PLD0_RC_EN_MODE [3:2]		PLD0_RC_EN_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW	RW	RW	RW		RW	
HW Access	None	R	R	R	R		R	
Name	None	PLD1_RC_RES_-SEL0_OR_-FRES	PLD1_RC_-INV	PLD1_RC_EN_INV	PLD1_RC_EN_MODE [11:10]		PLD1_RC_EN_SEL [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW		RW	
HW Access	R	R	R	R	R		R	
Name	DP_RC_RES_SEL1	DP_RC_RES_-SEL0_OR_-FRES	DP_RC_-INV	DP_RC_EN_INV	DP_RC_EN_MODE [19:18]		DP_RC_EN_SEL [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW		RW	
HW Access	R	R	R	R	R		R	
Name	SC_RC_RES_SEL1	SC_RC_RES_-SEL0_OR_-FRES	SC_RC_-INV	SC_RC_EN_INV	SC_RC_EN_MODE [27:26]		SC_RC_EN_SEL [25:24]	

Bits	Name	Description

18.1.30 UDB_UDBPAIR0_UDBSNG0_RC_CFG0 (continued)

31	SC_RC_RES_SEL1	Configures the routed reset for the associated UDB component block. The meaning of this bit depends on the value of ALT RES (RC_CFG1). When ALT RES = '0' - This bit is not used. When ALT RES = '1' - The bits {RC_SEL1,RC_SEL0_OR_FRES} select the RC routing for routed reset control according to the following: 00 : rc_in [0] 01 : rc_in [1] 10 : rc_in [2] 11 : rc_in [3] Default Value: 0
30	SC_RC_RES_-SEL0_OR_FRES	Configures the routed or firmware reset for the associated UDB component block. The meaning of this bit depends on the value of ALT RES (RC_CFG1). When ALT RES = '0' - This bit is a firmware reset. When ALT RES = '1' - The bits {RC_SEL1,RC_SEL0_OR_FRES} select the RC routing for routed reset control according to the following: 00 : rc_in [0] 01 : rc_in [1] 10 : rc_in [2] 11 : rc_in [3] Default Value: 0
29	SC_RC_INV	Optionally inverts the clock selection for the associated UDB component block. Default Value: 0 **0x0: NOINV :** Non-inverted **0x1: INVERT :** Inverted
28	SC_RC_EN_INV	Optionally inverts the clock enable selection for the associated UDB component blocks. Default Value: 0 **0x0: NOINV :** Non-inverted **0x1: INVERT :** Inverted
27 : 26	SC_RC_EN_MODE	Selects the operating mode for the clock to the associated UDB component block. Default Value: 0 **0x0: OFF :** Always off **0x1: ON :** Always on **0x2: POSEDGE :** Positive edge **0x3: LEVEL :** Level sensitive
25 : 24	SC_RC_EN_SEL	Selects channel route for enable control to the associated UDB component block Default Value: 0 **0x0: RC_IN0 :** rc_in[0] **0x1: RC_IN1 :** rc_in[1]

18.1.30 UDB_UDBPAIR0_UDBSNG0_RC_CFG0 (continued)

		0x2: RC_IN2 : rc_in[2] **0x3: RC_IN3 :** rc_in[3]
23	DP_RC_RES_SEL1	Configures the routed reset for the associated UDB component block. The meaning of this bit depends on the value of ALT RES (RC_CFG1). When ALT RES = '0' - This bit is not used. When ALT RES = '1' - The bits {RC_SEL1,RC_SEL0_OR_FRES} select the RC routing for routed reset control according to the following: 00 : rc_in [0] 01 : rc_in [1] 10 : rc_in [2] 11 : rc_in [3] Default Value: 0
22	DP_RC_RES_-SEL0_OR_FRES	Configures the routed or firmware reset for the associated UDB component block. The meaning of this bit depends on the value of ALT RES (RC_CFG1). When ALT RES = '0' - This bit is a firmware reset. When ALT RES = '1' - The bits {RC_SEL1,RC_SEL0_OR_FRES} select the RC routing for routed reset control according to the following: 00 : rc_in [0] 01 : rc_in [1] 10 : rc_in [2] 11 : rc_in [3] Default Value: 0
21	DP_RC_INV	Optionally inverts the clock selection for the associated UDB component block. Default Value: 0 **0x0: NOINV :** Non-inverted **0x1: INVERT :** Inverted
20	DP_RC_EN_INV	Optionally inverts the clock enable selection for the associated UDB component blocks. Default Value: 0 **0x0: NOINV :** Non-inverted **0x1: INVERT :** Inverted
19 : 18	DP_RC_EN_MODE	Selects the operating mode for the clock to the associated UDB component block. Default Value: 0 **0x0: OFF :** Always off **0x1: ON :** Always on **0x2: POSEDGE :** Positive edge **0x3: LEVEL :** Level sensitive
17 : 16	DP_RC_EN_SEL	Selects channel route for enable control to the associated UDB component block Default Value: 0

18.1.30 UDB_UDBPAIR0_UDBSNG0_RC_CFG0 (continued)

		0x0: RC_IN0 : rc_in[0] **0x1: RC_IN1 :** rc_in[1] **0x2: RC_IN2 :** rc_in[2] **0x3: RC_IN3 :** rc_in[3]
14	PLD1_RC_RES_-SEL0_OR_FRES	Configures the routed or firmware reset for the associated UDB component block. The meaning of this bit depends on the value of ALT RES (RC_CFG1). When ALT RES = '0' - This bit is a firmware reset. When ALT RES = '1' - The bits {RC_SEL1,RC_SEL0_OR_FRES} select the RC routing for routed reset control according to the following: 00 : rc_in [0] 01 : rc_in [1] 10 : rc_in [2] 11 : rc_in [3] Default Value: 0
13	PLD1_RC_INV	Optionally inverts the clock selection for the associated UDB component block. Default Value: 0 **0x0: NOINV :** Non-inverted **0x1: INVERT :** Inverted
12	PLD1_RC_EN_INV	Optionally inverts the clock enable selection for the associated UDB component blocks. Default Value: 0 **0x0: NOINV :** Non-inverted **0x1: INVERT :** Inverted
11 : 10	PLD1_RC_EN_MODE	Selects the operating mode for the clock to the associated UDB component block. Default Value: 0 **0x0: OFF :** Always off **0x1: ON :** Always on **0x2: POSEDGE :** Positive edge **0x3: LEVEL :** Level sensitive
9 : 8	PLD1_RC_EN_SEL	Selects channel route for enable control to the associated UDB component block Default Value: 0 **0x0: RC_IN0 :** rc_in[0] **0x1: RC_IN1 :** rc_in[1]

18.1.30 UDB_UDBPAIR0_UDBSNG0_RC_CFG0 (continued)

		0x2: RC_IN2 : rc_in[2] **0x3: RC_IN3 :** rc_in[3]
7	PLD0_RC_RES_SEL1	Configures the routed reset for the associated UDB component block. The meaning of this bit depends on the value of ALT RES (RC_CFG1). When ALT RES = '0' - This bit is not used. When ALT RES = '1' - The bits {RC_SEL1,RC_SEL0_OR_FRES} select the RC routing for routed reset control according to the following: 00 : rc_in [0] 01 : rc_in [1] 10 : rc_in [2] 11 : rc_in [3] Default Value: 0
6	PLD0_RC_RES_-SEL0_OR_FRES	Configures the routed or firmware reset for the associated UDB component block. The meaning of this bit depends on the value of ALT RES (RC_CFG1). When ALT RES = '0' - This bit is a firmware reset. When ALT RES = '1' - The bits {RC_SEL1,RC_SEL0_OR_FRES} select the RC routing for routed reset control according to the following: 00 : rc_in [0] 01 : rc_in [1] 10 : rc_in [2] 11 : rc_in [3] Default Value: 0
5	PLD0_RC_INV	Optionally inverts the clock selection for the associated UDB component block. Default Value: 0 **0x0: NOINV :** Non-inverted **0x1: INVERT :** Inverted
4	PLD0_RC_EN_INV	Optionally inverts the clock enable selection for the associated UDB component blocks. Default Value: 0 **0x0: NOINV :** Non-inverted **0x1: INVERT :** Inverted
3 : 2	PLD0_RC_EN_MODE	Selects the operating mode for the clock to the associated UDB component block. Default Value: 0 **0x0: OFF :** Always off **0x1: ON :** Always on **0x2: POSEDGE :** Positive edge **0x3: LEVEL :** Level sensitive
1 : 0	PLD0_RC_EN_SEL	Selects channel route for enable control to the associated UDB component block Default Value: 0

18.1.30 UDB_UDBPAIR0_UDBSNG0_RC_CFG0 (continued)

0x0: RC_IN0 :
rc_in[0]

0x1: RC_IN1 :
rc_in[1]

0x2: RC_IN2 :
rc_in[2]

0x3: RC_IN3 :
rc_in[3]

18.1.31 UDB_UDBPAIR0_UDBSNG0_RC_CFG1

PLD0, PLD1, Datatpath, and SC clock selection, general reset control

Address: 0x40342060

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PLD1_CK_SEL [7:4]				PLD0_CK_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	SC_CK_SEL [15:12]				DP_CK_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	None		RW	RW	RW	
HW Access	R	R	None		R	R	R	
Name	SC_RES_POL	DP_RES_POL	None [21:20]		EN_RES_CNTCTL	RES_POL	RES_SEL [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None	RW	RW		RW	RW	RW	RW
HW Access	None	R	R		R	R	R	R
Name	None	PLD0_RES_POL	EXT_CK_SEL [29:28]		EN_RES_DP	EN_RES_STAT	EXT_SYNC	ALT_RES

Bits	Name	Description
30	PLD0_RES_POL	The meaning of this bit depends on the value of ALT RES. When ALT RES is '1', this bit controls the polarity of the selected PLD0 routed reset. NOTE: There is only one routed reset available to both PLDs in the UDB. When ALT RES is '1', PLD0 RES SEL controls the polarity of the routed reset for both PLDs. Therefore a "PLD1_RES_POL" bit does not exist. Default Value: 0 **0x0: NOINV :** Routed reset to the PLD0/PLD1 block is true polarity. **0x1: INVERT :** Routed reset to the PLD0/PLD1 block is inverted polarity.
29 : 28	EXT_CK_SEL	External clock selection Default Value: 0 **0x0: RC_IN0 :** rc_in[0] **0x1: RC_IN1 :** rc_in[1]

18.1.31 UDB_UDBPAIR0_UDBSNG0_RC_CFG1 (continued)

		0x2: RC_IN2 : rc_in[2]
		0x3: RC_IN3 : rc_in[3]
27	EN_RES_DP	Only valid when ALT RES is '1'. This bit gates the routed reset to the Datapath block. Default Value: 0
		0x0: DISABLE : Routed reset to the Datapath block is gated off.
		0x1: ENABLE : Routed reset to the Datapath block is on. ALT RES must be '1' and routed reset must be selected in RC_CFG0 (DP_RC_RES_SEL1, DP_RC_RES_SEL0_OR_FRES)
26	EN_RES_STAT	Only valid when ALT RES is '1'. This bit gates the routed reset to the status register. Default Value: 0
		0x0: NEGATED : Status register routed reset is gated off
		0x1: ASSERTED : Status register routed reset is on
25	EXT_SYNC	Enable synchronization of selected external clock Default Value: 0
		0x0: DISABLE : Selected external clock input is not synchronized
		0x1: ENABLE : Selected external clock input is synchronized
24	ALT_RES	This bit toggles between two reset configurations. When this bit is '0', one routed reset is shared by all components in this UDB (compatible mode). When this bit is a 1, each block can select a unique routed reset from the available RC inputs. Default Value: 0
		0x0: COMPATIBLE : All UDB blocks share a common routed reset.
		0x1: ALTERNATE : Each UDB component block can select and control its individual routed reset.
23	SC_RES_POL	Only valid when ALT RES is '1'. This bit controls the polarity of the selected SC routed reset. Default Value: 0
		0x0: NOINV : Routed reset to the Status and Control block is true polarity.
		0x1: INVERT : Routed reset to the Status and Control block is inverted polarity.
22	DP_RES_POL	Only valid when ALT RES is '1'. This bit controls the polarity of the selected Datapath routed reset. Default Value: 0
		0x0: NOINV : Routed reset to the Datapath block is true polarity.
		0x1: INVERT : Routed reset to the Datapath block is inverted polarity.

18.1.31 UDB_UDBPAIR0_UDBSNG0_RC_CFG1 (continued)

19	EN_RES_CNTCTL	This bit gates the routed reset to the counter/control register. By default, the operation is compatible, i.e., it only applies to the counter. However, if the updated control regisiter modes are used (sync mode, pulse mode, or the ext res bit) then the routed reset applies to the control register also. Default Value: 0 **0x0: DISABLE :** Routed reset is not applied to counter/control register **0x1: ENABLE :** Routed reset is applied to the counter/control register
18	RES_POL	The meaning of this bit depends on the value of the ALT RES bit. When ALT RES is '0' (compatible mode), this bit sets the polarity of the routed reset. When ALT RES is '1', this bit is unused. Default Value: 0 **0x0: NEGATED :** Polarity of the routed reset is true. **0x1: ASSERTED :** Polarity of the routed reset is inverted.
17 : 16	RES_SEL	The meaning of this bit depends on the value of ALT RES. When ALT RES is '0' (compatible mode), this 2 bit field selects the RC routing input for the compatible reset scheme. When the ALT RES bit is '1', these bits are not used. Default Value: 0 **0x0: RC_IN0 :** rc_in[0] **0x1: RC_IN1 :** rc_in[1] **0x2: RC_IN2 :** rc_in[2] **0x3: RC_IN3 :** rc_in[3]
15 : 12	SC_CK_SEL	Clock selection registers Default Value: 0 **0x0: GCLK0 :** gclk[0] **0x1: GCLK1 :** gclk[1] **0x2: GCLK2 :** gclk[2] **0x3: GCLK3 :** gclk[3] **0x4: GCLK4 :** gclk[4] **0x5: GCLK5 :** gclk[5] **0x6: GCLK6 :** gclk[6] **0x7: GCLK7 :** gclk[7]

18.1.31 UDB_UDBPAIR0_UDBSNG0_RC_CFG1 (continued)

		0x8: CLK_EXT : clk_ext
		0x9: CLK_PERI_APP : clk_peri_app
11 : 8	DP_CK_SEL	Clock selection registers Default Value: 0
		0x0: GCLK0 : gclk[0]
		0x1: GCLK1 : gclk[1]
		0x2: GCLK2 : gclk[2]
		0x3: GCLK3 : gclk[3]
		0x4: GCLK4 : gclk[4]
		0x5: GCLK5 : gclk[5]
		0x6: GCLK6 : gclk[6]
		0x7: GCLK7 : gclk[7]
		0x8: CLK_EXT : clk_ext
		0x9: CLK_PERI_APP : clk_peri_app
7 : 4	PLD1_CK_SEL	Clock selection registers Default Value: 0
		0x0: GCLK0 : gclk[0]
		0x1: GCLK1 : gclk[1]
		0x2: GCLK2 : gclk[2]
		0x3: GCLK3 : gclk[3]
		0x4: GCLK4 : gclk[4]
		0x5: GCLK5 : gclk[5]
		0x6: GCLK6 : gclk[6]
		0x7: GCLK7 : gclk[7]

18.1.31 UDB_UDBPAIR0_UDBSNG0_RC_CFG1 (continued)

		0x8: CLK_EXT : clk_ext
		0x9: CLK_PERI_APP : clk_peri_app
3 : 0	PLD0_CK_SEL	Clock selection registers Default Value: 0
		0x0: GCLK0 : gclk[0]
		0x1: GCLK1 : gclk[1]
		0x2: GCLK2 : gclk[2]
		0x3: GCLK3 : gclk[3]
		0x4: GCLK4 : gclk[4]
		0x5: GCLK5 : gclk[5]
		0x6: GCLK6 : gclk[6]
		0x7: GCLK7 : gclk[7]
		0x8: CLK_EXT : clk_ext
		0x9: CLK_PERI_APP : clk_peri_app

18.1.32 UDB_UDBPAIR0_UDBSNG0_DPATH_OPC0

Datapath opcode configuration

Address: 0x40342064

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW	RW	RW	RW
HW Access	R		R		R	R	R	R
Name	OPC0_A0_WR_SRC [7:6]		OPC0_A1_WR_SRC [5:4]		OPC0_CF-B_EN	OPC0_CI_-SEL	OPC0_SI_-SEL	OPC0_C-MP_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW	RW		RW	
HW Access	R			R	R		R	
Name	OPC0_FUNC [15:13]			OPC0_S-RC_A	OPC0_SRC_B [11:10]		OPC0_SHIFT [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	RW		RW		RW	RW	RW	RW
HW Access	R		R		R	R	R	R
Name	OPC1_A0_WR_SRC [23:22]		OPC1_A1_WR_SRC [21:20]		OPC1_CF-B_EN	OPC1_CI_-SEL	OPC1_SI_-SEL	OPC1_C-MP_SEL

Bits	31	30	29	28	27	26	25	24
SW Access	RW			RW	RW		RW	
HW Access	R			R	R		R	
Name	OPC1_FUNC [31:29]			OPC1_S-RC_A	OPC1_SRC_B [27:26]		OPC1_SHIFT [25:24]	

Bits	Name	Description
31 : 29	OPC1_FUNC	Dynamic ALU function selection Default Value: X **0x0: PASS :** Pass **0x1: INC_A :** Increment source A **0x2: DEC_A :** Decrement source A **0x3: ADD :** Add **0x4: SUB :** Subtract

18.1.32 UDB_UDBPAIR0_UDBSNG0_DPATH_OPC0 (continued)

		0x5: XOR : Bitwise XOR **0x6: AND :** Bitwise AND **0x7: OR :** Bitwise OR
28	OPC1_SRC_A	Dynamic ALU source A selection Default Value: X **0x0: A0 :** ALU source A is A0 **0x1: A1 :** ALU source A is A1
27 : 26	OPC1_SRC_B	Dynamic ALU source B selection Default Value: X **0x0: D0 :** ALU source B is D0 **0x1: D1 :** ALU source B is D1 **0x2: A0 :** ALU source B is A0 **0x3: A1 :** ALU source B is A1
25 : 24	OPC1_SHIFT	Dynamic shift selection Default Value: X **0x0: NOSHIFT :** No shift **0x1: LEFT :** Left Shift **0x2: RIGHT :** Right Shift **0x3: SWAP :** Nibble swap
23 : 22	OPC1_A0_WR_SRC	Dynamic A0 write source selection Default Value: X **0x0: NOWRITE :** no value written to A0 **0x1: ALU :** ALU output written to A0 **0x2: D0 :** D0 value written to A0 **0x3: F0 :** F0 value written to A0
21 : 20	OPC1_A1_WR_SRC	Dynamic A1 write source selection Default Value: X

18.1.32 UDB_UDBPAIR0_UDBSNG0_DPATH_OPC0 (continued)

		0x0: NOWRITE : no value written to A1 **0x1: ALU :** ALU output written to A1 **0x2: D1 :** D1 value written to A1 **0x3: F1 :** F1 value written to A1
19	OPC1_CFB_EN	Dynamic CRC feedback selection Default Value: X **0x0: DISABLE :** CRC feedback disabled **0x1: ENABLE :** CRC feedback enabled
18	OPC1_CI_SEL	Dynamic carry in selection Default Value: X **0x0: CFG_A :** Configuration A **0x1: CFG_B :** Configuration B
17	OPC1_SI_SEL	Dynamic shift in selection Default Value: X **0x0: CFG_A :** Configuration A **0x1: CFG_B :** Configuration B
16	OPC1_CMP_SEL	Dynamic compare selection Default Value: X **0x0: CFG_A :** Configuration A **0x1: CFG_B :** Configuration B
15 : 13	OPC0_FUNC	Dynamic ALU function selection Default Value: X **0x0: PASS :** Pass **0x1: INC_A :** Increment source A **0x2: DEC_A :** Decrement source A **0x3: ADD :** Add **0x4: SUB :** Subtract

18.1.32 UDB_UDBPAIR0_UDBSNG0_DPATH_OPC0 (continued)

		0x5: XOR : Bitwise XOR **0x6: AND :** Bitwise AND **0x7: OR :** Bitwise OR
12	OPC0_SRC_A	Dynamic ALU source A selection Default Value: X **0x0: A0 :** ALU source A is A0 **0x1: A1 :** ALU source A is A1
11 : 10	OPC0_SRC_B	Dynamic ALU source B selection Default Value: X **0x0: D0 :** ALU source B is D0 **0x1: D1 :** ALU source B is D1 **0x2: A0 :** ALU source B is A0 **0x3: A1 :** ALU source B is A1
9 : 8	OPC0_SHIFT	Dynamic shift selection Default Value: X **0x0: NOSHIFT :** No shift **0x1: LEFT :** Left Shift **0x2: RIGHT :** Right Shift **0x3: SWAP :** Nibble swap
7 : 6	OPC0_A0_WR_SRC	Dynamic A0 write source selection Default Value: X **0x0: NOWRITE :** no value written to A0 **0x1: ALU :** ALU output written to A0 **0x2: D0 :** D0 value written to A0 **0x3: F0 :** F0 value written to A0
5 : 4	OPC0_A1_WR_SRC	Dynamic A1 write source selection Default Value: X

18.1.32 UDB_UDBPAIR0_UDBSNG0_DPATH_OPC0 (continued)

		0x0: NOWRITE : no value written to A1 **0x1: ALU :** ALU output written to A1 **0x2: D1 :** D1 value written to A1 **0x3: F1 :** F1 value written to A1
3	OPC0_CFB_EN	Dynamic CRC feedback selection Default Value: X **0x0: DISABLE :** CRC feedback disabled **0x1: ENABLE :** CRC feedback enabled
2	OPC0_CI_SEL	Dynamic carry in selection Default Value: X **0x0: CFG_A :** Configuration A **0x1: CFG_B :** Configuration B
1	OPC0_SI_SEL	Dynamic shift in selection Default Value: X **0x0: CFG_A :** Configuration A **0x1: CFG_B :** Configuration B
0	OPC0_CMP_SEL	Dynamic compare selection Default Value: X **0x0: CFG_A :** Configuration A **0x1: CFG_B :** Configuration B

18.1.33 UDB_UDBPAIR0_ROUTE_TOP_V_BOT

Top Vertical Input (TVI) vs Bottom Vertical Input (BVI) muxing

Address: 0x40342100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	TOP_V_BOT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	TOP_V_BOT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	TOP_V_BOT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	TOP_V_BOT [31:24]							

Bits	Name	Description
31 : 0	TOP_V_BOT	Default Value: X

18.1.34 UDB_UDBPAIR0_ROUTE_LVO1_V_2

Left Vertical Ouput (LVO) 1 vs 2 muxing for certain horizontals

Address: 0x40342104

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	LVO1_V_2 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	LVO1_V_2 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	LVO1_V_2 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	LVO1_V_2 [31:24]							

Bits	Name	Description
31 : 0	LVO1_V_2	Default Value: X

18.1.35 UDB_UDBPAIR0_ROUTE_RVO1_V_2

Right Vertical Ouput (RVO) 1 vs 2 muxing for certain horizontals

Address: 0x40342108

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	RVO1_V_2 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	RVO1_V_2 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	RVO1_V_2 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	RVO1_V_2 [31:24]							

Bits	Name	Description
31 : 0	RVO1_V_2	Default Value: X

18.1.36 UDB_UDBPAIR0_ROUTE_TUI_CFG0

Top UDB Input (TUI) selection

Address: 0x4034210C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	TUI1SEL [7:4]				TUI0SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	TUI3SEL [15:12]				TUI2SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW			
HW Access	R				R			
Name	TUI5SEL [23:20]				TUI4SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	R				R			
Name	TUI7SEL [31:28]				TUI6SEL [27:24]			

Bits	Name	Description
31 : 28	TUI7SEL	Default Value: X
27 : 24	TUI6SEL	Default Value: X
23 : 20	TUI5SEL	Default Value: X
19 : 16	TUI4SEL	Default Value: X
15 : 12	TUI3SEL	Default Value: X
11 : 8	TUI2SEL	Default Value: X
7 : 4	TUI1SEL	Default Value: X
3 : 0	TUI0SEL	Default Value: X

18.1.37 UDB_UDBPAIR0_ROUTE_TUI_CFG1

Top UDB Input (TUI) selection

Address: 0x40342110

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	TUI9SEL [7:4]				TUI8SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	TUI11SEL [15:12]				TUI10SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW			
HW Access	R				R			
Name	TUI13SEL [23:20]				TUI12SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	R				R			
Name	TUI15SEL [31:28]				TUI14SEL [27:24]			

Bits	Name	Description
31 : 28	TUI15SEL	Default Value: X
27 : 24	TUI14SEL	Default Value: X
23 : 20	TUI13SEL	Default Value: X
19 : 16	TUI12SEL	Default Value: X
15 : 12	TUI11SEL	Default Value: X
11 : 8	TUI10SEL	Default Value: X
7 : 4	TUI9SEL	Default Value: X
3 : 0	TUI8SEL	Default Value: X

18.1.38 UDB_UDBPAIR0_ROUTE_TUI_CFG2

Top UDB Input (TUI) selection

Address: 0x40342114

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	TUI17SEL [7:4]				TUI16SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	TUI19SEL [15:12]				TUI18SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW			
HW Access	R				R			
Name	TUI21SEL [23:20]				TUI20SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	R				R			
Name	TUI23SEL [31:28]				TUI22SEL [27:24]			

Bits	Name	Description
31 : 28	TUI23SEL	Default Value: X
27 : 24	TUI22SEL	Default Value: X
23 : 20	TUI21SEL	Default Value: X
19 : 16	TUI20SEL	Default Value: X
15 : 12	TUI19SEL	Default Value: X
11 : 8	TUI18SEL	Default Value: X
7 : 4	TUI17SEL	Default Value: X
3 : 0	TUI16SEL	Default Value: X

18.1.39 UDB_UDBPAIR0_ROUTE_TUI_CFG3

Top UDB Input (TUI) selection

Address: 0x40342118

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	TUI25SEL [7:4]				TUI24SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	TUI27SEL [15:12]				TUI26SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW			
HW Access	R				R			
Name	TUI29SEL [23:20]				TUI28SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	R				R			
Name	TUI31SEL [31:28]				TUI30SEL [27:24]			

Bits	Name	Description
31 : 28	TUI31SEL	Default Value: X
27 : 24	TUI30SEL	Default Value: X
23 : 20	TUI29SEL	Default Value: X
19 : 16	TUI28SEL	Default Value: X
15 : 12	TUI27SEL	Default Value: X
11 : 8	TUI26SEL	Default Value: X
7 : 4	TUI25SEL	Default Value: X
3 : 0	TUI24SEL	Default Value: X

18.1.40 UDB_UDBPAIR0_ROUTE_TUI_CFG4

Top UDB Input (TUI) selection

Address: 0x4034211C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	TUI33SEL [7:4]				TUI32SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	TUI35SEL [15:12]				TUI34SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW			
HW Access	R				R			
Name	TUI37SEL [23:20]				TUI36SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	R				R			
Name	TUI39SEL [31:28]				TUI38SEL [27:24]			

Bits	Name	Description
31 : 28	TUI39SEL	Default Value: X
27 : 24	TUI38SEL	Default Value: X
23 : 20	TUI37SEL	Default Value: X
19 : 16	TUI36SEL	Default Value: X
15 : 12	TUI35SEL	Default Value: X
11 : 8	TUI34SEL	Default Value: X
7 : 4	TUI33SEL	Default Value: X
3 : 0	TUI32SEL	Default Value: X

18.1.41 UDB_UDBPAIR0_ROUTE_TUI_CFG5

Top UDB Input (TUI) selection

Address: 0x40342120

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	TUI41SEL [7:4]				TUI40SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	TUI41SEL	Default Value: X
3 : 0	TUI40SEL	Default Value: X

18.1.42 UDB_UDBPAIR0_ROUTE_BUI_CFG0

Bottom UDB Input (BUI) selection

Address: 0x40342124

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	BUI1SEL [7:4]				BUI0SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	BUI3SEL [15:12]				BUI2SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW			
HW Access	R				R			
Name	BUI5SEL [23:20]				BUI4SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	R				R			
Name	BUI7SEL [31:28]				BUI6SEL [27:24]			

Bits	Name	Description
31 : 28	BUI7SEL	Default Value: X
27 : 24	BUI6SEL	Default Value: X
23 : 20	BUI5SEL	Default Value: X
19 : 16	BUI4SEL	Default Value: X
15 : 12	BUI3SEL	Default Value: X
11 : 8	BUI2SEL	Default Value: X
7 : 4	BUI1SEL	Default Value: X
3 : 0	BUI0SEL	Default Value: X

18.1.43 UDB_UDBPAIR0_ROUTE_BUI_CFG1

Bottom UDB Input (BUI) selection

Address: 0x40342128

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	BUI9SEL [7:4]				BUI8SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	BUI11SEL [15:12]				BUI10SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW			
HW Access	R				R			
Name	BUI13SEL [23:20]				BUI12SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	R				R			
Name	BUI15SEL [31:28]				BUI14SEL [27:24]			

Bits	Name	Description
31 : 28	BUI15SEL	Default Value: X
27 : 24	BUI14SEL	Default Value: X
23 : 20	BUI13SEL	Default Value: X
19 : 16	BUI12SEL	Default Value: X
15 : 12	BUI11SEL	Default Value: X
11 : 8	BUI10SEL	Default Value: X
7 : 4	BUI9SEL	Default Value: X
3 : 0	BUI8SEL	Default Value: X

18.1.44 UDB_UDBPAIR0_ROUTE_BUI_CFG2

Bottom UDB Input (BUI) selection

Address: 0x4034212C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	BUI17SEL [7:4]				BUI16SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	BUI19SEL [15:12]				BUI18SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW			
HW Access	R				R			
Name	BUI21SEL [23:20]				BUI20SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	R				R			
Name	BUI23SEL [31:28]				BUI22SEL [27:24]			

Bits	Name	Description
31 : 28	BUI23SEL	Default Value: X
27 : 24	BUI22SEL	Default Value: X
23 : 20	BUI21SEL	Default Value: X
19 : 16	BUI20SEL	Default Value: X
15 : 12	BUI19SEL	Default Value: X
11 : 8	BUI18SEL	Default Value: X
7 : 4	BUI17SEL	Default Value: X
3 : 0	BUI16SEL	Default Value: X

18.1.45 UDB_UDBPAIR0_ROUTE_BUI_CFG3

Bottom UDB Input (BUI) selection

Address: 0x40342130

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	BUI25SEL [7:4]				BUI24SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	BUI27SEL [15:12]				BUI26SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW			
HW Access	R				R			
Name	BUI29SEL [23:20]				BUI28SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	R				R			
Name	BUI31SEL [31:28]				BUI30SEL [27:24]			

Bits	Name	Description
31 : 28	BUI31SEL	Default Value: X
27 : 24	BUI30SEL	Default Value: X
23 : 20	BUI29SEL	Default Value: X
19 : 16	BUI28SEL	Default Value: X
15 : 12	BUI27SEL	Default Value: X
11 : 8	BUI26SEL	Default Value: X
7 : 4	BUI25SEL	Default Value: X
3 : 0	BUI24SEL	Default Value: X

18.1.46 UDB_UDBPAIR0_ROUTE_BUI_CFG4

Bottom UDB Input (BUI) selection

Address: 0x40342134

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	BUI33SEL [7:4]				BUI32SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	BUI35SEL [15:12]				BUI34SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW			
HW Access	R				R			
Name	BUI37SEL [23:20]				BUI36SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	R				R			
Name	BUI39SEL [31:28]				BUI38SEL [27:24]			

Bits	Name	Description
31 : 28	BUI39SEL	Default Value: X
27 : 24	BUI38SEL	Default Value: X
23 : 20	BUI37SEL	Default Value: X
19 : 16	BUI36SEL	Default Value: X
15 : 12	BUI35SEL	Default Value: X
11 : 8	BUI34SEL	Default Value: X
7 : 4	BUI33SEL	Default Value: X
3 : 0	BUI32SEL	Default Value: X

18.1.47 UDB_UDBPAIR0_ROUTE_BUI_CFG5

Bottom UDB Input (BUI) selection

Address: 0x40342138

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	BUI41SEL [7:4]				BUI40SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	BUI41SEL	Default Value: X
3 : 0	BUI40SEL	Default Value: X

18.1.48 UDB_UDBPAIR0_ROUTE_RVO_CFG0

Right Vertical Ouput (RVO) selection

Address: 0x4034213C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			R				
Name	None [7:5]			RVO0SEL [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW				
HW Access	None			R				
Name	None [15:13]			RVO1SEL [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW				
HW Access	None			R				
Name	None [23:21]			RVO2SEL [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	None			RW				
HW Access	None			R				
Name	None [31:29]			RVO3SEL [28:24]				

Bits	Name	Description
28 : 24	RVO3SEL	Default Value: X
20 : 16	RVO2SEL	Default Value: X
12 : 8	RVO1SEL	Default Value: X
4 : 0	RVO0SEL	Default Value: X

18.1.49 UDB_UDBPAIR0_ROUTE_RVO_CFG1

Right Vertical Ouput (RVO) selection

Address: 0x40342140

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			R				
Name	None [7:5]			RVO4SEL [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW				
HW Access	None			R				
Name	None [15:13]			RVO5SEL [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW				
HW Access	None			R				
Name	None [23:21]			RVO6SEL [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	None			RW				
HW Access	None			R				
Name	None [31:29]			RVO7SEL [28:24]				

Bits	Name	Description
28 : 24	RVO7SEL	Default Value: X
20 : 16	RVO6SEL	Default Value: X
12 : 8	RVO5SEL	Default Value: X
4 : 0	RVO4SEL	Default Value: X

18.1.50 UDB_UDBPAIR0_ROUTE_RVO_CFG2

Right Vertical Ouput (RVO) selection

Address: 0x40342144

Retention: Retained

Bits	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SW Access	None			RW				
HW Access	None			R				
Name	None [7:5]			RVO8SEL [4:0]				

Bits	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SW Access	None			RW				
HW Access	None			R				
Name	None [15:13]			RVO9SEL [12:8]				

Bits	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SW Access	None			RW				
HW Access	None			R				
Name	None [23:21]			RVO10SEL [20:16]				

Bits	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**
SW Access	None			RW				
HW Access	None			R				
Name	None [31:29]			RVO11SEL [28:24]				

Bits	**Name**	**Description**
28 : 24	RVO11SEL	Default Value: X
20 : 16	RVO10SEL	Default Value: X
12 : 8	RVO9SEL	Default Value: X
4 : 0	RVO8SEL	Default Value: X

18.1.51 UDB_UDBPAIR0_ROUTE_RVO_CFG3

Right Vertical Ouput (RVO) selection

Address: 0x40342148

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			R				
Name	None [7:5]			RVO12SEL [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW				
HW Access	None			R				
Name	None [15:13]			RVO13SEL [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW				
HW Access	None			R				
Name	None [23:21]			RVO14SEL [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	None			RW				
HW Access	None			R				
Name	None [31:29]			RVO15SEL [28:24]				

Bits	Name	Description
28 : 24	RVO15SEL	Default Value: X
20 : 16	RVO14SEL	Default Value: X
12 : 8	RVO13SEL	Default Value: X
4 : 0	RVO12SEL	Default Value: X

18.1.52 UDB_UDBPAIR0_ROUTE_LVO_CFG0

Left Vertical Ouput (LVO) selection

Address: 0x4034214C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	LVO1SEL [7:4]				LVO0SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	LVO3SEL [15:12]				LVO2SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW			
HW Access	R				R			
Name	LVO5SEL [23:20]				LVO4SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	R				R			
Name	LVO7SEL [31:28]				LVO6SEL [27:24]			

Bits	Name	Description
31 : 28	LVO7SEL	Default Value: X
27 : 24	LVO6SEL	Default Value: X
23 : 20	LVO5SEL	Default Value: X
19 : 16	LVO4SEL	Default Value: X
15 : 12	LVO3SEL	Default Value: X
11 : 8	LVO2SEL	Default Value: X
7 : 4	LVO1SEL	Default Value: X
3 : 0	LVO0SEL	Default Value: X

18.1.53 UDB_UDBPAIR0_ROUTE_LVO_CFG1

Left Vertical Ouput (LVO) selection

Address: 0x40342150

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	LVO9SEL [7:4]				LVO8SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	LVO11SEL [15:12]				LVO10SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW			
HW Access	R				R			
Name	LVO13SEL [23:20]				LVO12SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	R				R			
Name	LVO15SEL [31:28]				LVO14SEL [27:24]			

Bits	Name	Description
31 : 28	LVO15SEL	Default Value: X
27 : 24	LVO14SEL	Default Value: X
23 : 20	LVO13SEL	Default Value: X
19 : 16	LVO12SEL	Default Value: X
15 : 12	LVO11SEL	Default Value: X
11 : 8	LVO10SEL	Default Value: X
7 : 4	LVO9SEL	Default Value: X
3 : 0	LVO8SEL	Default Value: X

18.1.54 UDB_UDBPAIR0_ROUTE_RHO_CFG0

Right Horizontal Out (RHO) selection

Address: 0x40342154

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	RHOSEL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	RHOSEL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	RHOSEL [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	RHOSEL [31:24]							

Bits	Name	Description
31 : 0	RHOSEL	Right Horizontal Output select for bits 31:0 Default Value: X

18.1.55 UDB_UDBPAIR0_ROUTE_RHO_CFG1

Right Horizontal Out (RHO) selection

Address: 0x40342158

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	RHOSEL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	RHOSEL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	RHOSEL [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	RHOSEL [31:24]							

Bits	Name	Description
31 : 0	RHOSEL	Right Horizontal Output select for bits 63:32 Default Value: X

18.1.56 UDB_UDBPAIR0_ROUTE_RHO_CFG2

Right Horizontal Out (RHO) selection

Address: 0x4034215C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	RHOSEL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	RHOSEL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	RHOSEL [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	RHOSEL [31:24]							

Bits	Name	Description
31 : 0	RHOSEL	Right Horizontal Output select for bits 95:64 Default Value: X

18.1.57 UDB_UDBPAIR0_ROUTE_LHO_CFG0

Left Horizontal Out (LHO) selection

Address: 0x40342160

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	LHO1SEL [7:4]				LHO0SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	LHO3SEL [15:12]				LHO2SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW			
HW Access	R				R			
Name	LHO5SEL [23:20]				LHO4SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	R				R			
Name	LHO7SEL [31:28]				LHO6SEL [27:24]			

Bits	Name	Description
31 : 28	LHO7SEL	Default Value: X
27 : 24	LHO6SEL	Default Value: X
23 : 20	LHO5SEL	Default Value: X
19 : 16	LHO4SEL	Default Value: X
15 : 12	LHO3SEL	Default Value: X
11 : 8	LHO2SEL	Default Value: X
7 : 4	LHO1SEL	Default Value: X
3 : 0	LHO0SEL	Default Value: X

18.1.58 UDB_UDBPAIR0_ROUTE_LHO_CFG1

Left Horizontal Out (LHO) selection

Address: 0x40342164

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	LHO9SEL [7:4]				LHO8SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	LHO11SEL [15:12]				LHO10SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW			
HW Access	R				R			
Name	LHO13SEL [23:20]				LHO12SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	R				R			
Name	LHO15SEL [31:28]				LHO14SEL [27:24]			

Bits	Name	Description
31 : 28	LHO15SEL	Default Value: X
27 : 24	LHO14SEL	Default Value: X
23 : 20	LHO13SEL	Default Value: X
19 : 16	LHO12SEL	Default Value: X
15 : 12	LHO11SEL	Default Value: X
11 : 8	LHO10SEL	Default Value: X
7 : 4	LHO9SEL	Default Value: X
3 : 0	LHO8SEL	Default Value: X

18.1.59 UDB_UDBPAIR0_ROUTE_LHO_CFG2

Left Horizontal Out (LHO) selection

Address: 0x40342168

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	LHO17SEL [7:4]				LHO16SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	LHO19SEL [15:12]				LHO18SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW			
HW Access	R				R			
Name	LHO21SEL [23:20]				LHO20SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	R				R			
Name	LHO23SEL [31:28]				LHO22SEL [27:24]			

Bits	Name	Description
31 : 28	LHO23SEL	Default Value: X
27 : 24	LHO22SEL	Default Value: X
23 : 20	LHO21SEL	Default Value: X
19 : 16	LHO20SEL	Default Value: X
15 : 12	LHO19SEL	Default Value: X
11 : 8	LHO18SEL	Default Value: X
7 : 4	LHO17SEL	Default Value: X
3 : 0	LHO16SEL	Default Value: X

18.1.60 UDB_UDBPAIR0_ROUTE_LHO_CFG3

Left Horizontal Out (LHO) selection

Address: 0x4034216C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	LHO25SEL [7:4]				LHO24SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	LHO27SEL [15:12]				LHO26SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW			
HW Access	R				R			
Name	LHO29SEL [23:20]				LHO28SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	R				R			
Name	LHO31SEL [31:28]				LHO30SEL [27:24]			

Bits	Name	Description
31 : 28	LHO31SEL	Default Value: X
27 : 24	LHO30SEL	Default Value: X
23 : 20	LHO29SEL	Default Value: X
19 : 16	LHO28SEL	Default Value: X
15 : 12	LHO27SEL	Default Value: X
11 : 8	LHO26SEL	Default Value: X
7 : 4	LHO25SEL	Default Value: X
3 : 0	LHO24SEL	Default Value: X

18.1.61 UDB_UDBPAIR0_ROUTE_LHO_CFG4

Left Horizontal Out (LHO) selection

Address: 0x40342170

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	LHO33SEL [7:4]				LHO32SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	LHO35SEL [15:12]				LHO34SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW			
HW Access	R				R			
Name	LHO37SEL [23:20]				LHO36SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	R				R			
Name	LHO39SEL [31:28]				LHO38SEL [27:24]			

Bits	Name	Description
31 : 28	LHO39SEL	Default Value: X
27 : 24	LHO38SEL	Default Value: X
23 : 20	LHO37SEL	Default Value: X
19 : 16	LHO36SEL	Default Value: X
15 : 12	LHO35SEL	Default Value: X
11 : 8	LHO34SEL	Default Value: X
7 : 4	LHO33SEL	Default Value: X
3 : 0	LHO32SEL	Default Value: X

18.1.62 UDB_UDBPAIR0_ROUTE_LHO_CFG5

Left Horizontal Out (LHO) selection

Address: 0x40342174

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	LHO41SEL [7:4]				LHO40SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	LHO43SEL [15:12]				LHO42SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW			
HW Access	R				R			
Name	LHO45SEL [23:20]				LHO44SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	R				R			
Name	LHO47SEL [31:28]				LHO46SEL [27:24]			

Bits	Name	Description
31 : 28	LHO47SEL	Default Value: X
27 : 24	LHO46SEL	Default Value: X
23 : 20	LHO45SEL	Default Value: X
19 : 16	LHO44SEL	Default Value: X
15 : 12	LHO43SEL	Default Value: X
11 : 8	LHO42SEL	Default Value: X
7 : 4	LHO41SEL	Default Value: X
3 : 0	LHO40SEL	Default Value: X

18.1.63 UDB_UDBPAIR0_ROUTE_LHO_CFG6

Left Horizontal Out (LHO) selection

Address: 0x40342178

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	LHO49SEL [7:4]				LHO48SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	LHO51SEL [15:12]				LHO50SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW			
HW Access	R				R			
Name	LHO53SEL [23:20]				LHO52SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	R				R			
Name	LHO55SEL [31:28]				LHO54SEL [27:24]			

Bits	Name	Description
31 : 28	LHO55SEL	Default Value: X
27 : 24	LHO54SEL	Default Value: X
23 : 20	LHO53SEL	Default Value: X
19 : 16	LHO52SEL	Default Value: X
15 : 12	LHO51SEL	Default Value: X
11 : 8	LHO50SEL	Default Value: X
7 : 4	LHO49SEL	Default Value: X
3 : 0	LHO48SEL	Default Value: X

18.1.64 UDB_UDBPAIR0_ROUTE_LHO_CFG7

Left Horizontal Out (LHO) selection

Address: 0x4034217C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	LHO57SEL [7:4]				LHO56SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	LHO59SEL [15:12]				LHO58SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW			
HW Access	R				R			
Name	LHO61SEL [23:20]				LHO60SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	R				R			
Name	LHO63SEL [31:28]				LHO62SEL [27:24]			

Bits	Name	Description
31 : 28	LHO63SEL	Default Value: X
27 : 24	LHO62SEL	Default Value: X
23 : 20	LHO61SEL	Default Value: X
19 : 16	LHO60SEL	Default Value: X
15 : 12	LHO59SEL	Default Value: X
11 : 8	LHO58SEL	Default Value: X
7 : 4	LHO57SEL	Default Value: X
3 : 0	LHO56SEL	Default Value: X

18.1.65 UDB_UDBPAIR0_ROUTE_LHO_CFG8

Left Horizontal Out (LHO) selection

Address: 0x40342180

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	LHO65SEL [7:4]				LHO64SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	LHO67SEL [15:12]				LHO66SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW			
HW Access	R				R			
Name	LHO69SEL [23:20]				LHO68SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	R				R			
Name	LHO71SEL [31:28]				LHO70SEL [27:24]			

Bits	Name	Description
31 : 28	LHO71SEL	Default Value: X
27 : 24	LHO70SEL	Default Value: X
23 : 20	LHO69SEL	Default Value: X
19 : 16	LHO68SEL	Default Value: X
15 : 12	LHO67SEL	Default Value: X
11 : 8	LHO66SEL	Default Value: X
7 : 4	LHO65SEL	Default Value: X
3 : 0	LHO64SEL	Default Value: X

18.1.66 UDB_UDBPAIR0_ROUTE_LHO_CFG9

Left Horizontal Out (LHO) selection

Address: 0x40342184

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	LHO73SEL [7:4]				LHO72SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	LHO75SEL [15:12]				LHO74SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW			
HW Access	R				R			
Name	LHO77SEL [23:20]				LHO76SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	R				R			
Name	LHO79SEL [31:28]				LHO78SEL [27:24]			

Bits	Name	Description
31 : 28	LHO79SEL	Default Value: X
27 : 24	LHO78SEL	Default Value: X
23 : 20	LHO77SEL	Default Value: X
19 : 16	LHO76SEL	Default Value: X
15 : 12	LHO75SEL	Default Value: X
11 : 8	LHO74SEL	Default Value: X
7 : 4	LHO73SEL	Default Value: X
3 : 0	LHO72SEL	Default Value: X

18.1.67 UDB_UDBPAIR0_ROUTE_LHO_CFG10

Left Horizontal Out (LHO) selection

Address: 0x40342188

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	LHO81SEL [7:4]				LHO80SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	LHO83SEL [15:12]				LHO82SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW			
HW Access	R				R			
Name	LHO85SEL [23:20]				LHO84SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	R				R			
Name	LHO87SEL [31:28]				LHO86SEL [27:24]			

Bits	Name	Description
31 : 28	LHO87SEL	Default Value: X
27 : 24	LHO86SEL	Default Value: X
23 : 20	LHO85SEL	Default Value: X
19 : 16	LHO84SEL	Default Value: X
15 : 12	LHO83SEL	Default Value: X
11 : 8	LHO82SEL	Default Value: X
7 : 4	LHO81SEL	Default Value: X
3 : 0	LHO80SEL	Default Value: X

18.1.68 UDB_UDBPAIR0_ROUTE_LHO_CFG11

Left Horizontal Out (LHO) selection

Address: 0x4034218C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	LHO89SEL [7:4]				LHO88SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	LHO91SEL [15:12]				LHO90SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW			
HW Access	R				R			
Name	LHO93SEL [23:20]				LHO92SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	R				R			
Name	LHO95SEL [31:28]				LHO94SEL [27:24]			

Bits	Name	Description
31 : 28	LHO95SEL	Default Value: X
27 : 24	LHO94SEL	Default Value: X
23 : 20	LHO93SEL	Default Value: X
19 : 16	LHO92SEL	Default Value: X
15 : 12	LHO91SEL	Default Value: X
11 : 8	LHO90SEL	Default Value: X
7 : 4	LHO89SEL	Default Value: X
3 : 0	LHO88SEL	Default Value: X

18.1.69 UDB_DSI0_LVO1_V_2

Left Vertical Ouput (LVO) 1 vs 2 muxing for certain horizontals

Address: 0x40346000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	LVO1_V_2 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	LVO1_V_2 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	LVO1_V_2 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	LVO1_V_2 [31:24]							

Bits	Name	Description
31 : 0	LVO1_V_2	Default Value: X

18.1.70 UDB_DSI0_RVO1_V_2

Right Vertical Ouput (RVO) 1 vs 2 muxing for certain horizontals

Address: 0x40346004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	RVO1_V_2 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	RVO1_V_2 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	RVO1_V_2 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	RVO1_V_2 [31:24]							

Bits	Name	Description
31 : 0	RVO1_V_2	Default Value: X

18.1.71 UDB_DSI0_DOP_CFG0

DSI Out Pair (DOP) selection

Address: 0x40346008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			R				
Name	None [7:5]			DOP0SEL [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW				
HW Access	None			R				
Name	None [15:13]			DOP1SEL [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW				
HW Access	None			R				
Name	None [23:21]			DOP2SEL [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	None			RW				
HW Access	None			R				
Name	None [31:29]			DOP3SEL [28:24]				

Bits	Name	Description
28 : 24	DOP3SEL	Default Value: X
20 : 16	DOP2SEL	Default Value: X
12 : 8	DOP1SEL	Default Value: X
4 : 0	DOP0SEL	Default Value: X

18.1.72 UDB_DSI0_DOP_CFG1

DSI Out Pair (DOP) selection

Address: 0x4034600C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			R				
Name	None [7:5]			DOP4SEL [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW				
HW Access	None			R				
Name	None [15:13]			DOP5SEL [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW				
HW Access	None			R				
Name	None [23:21]			DOP6SEL [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	None			RW				
HW Access	None			R				
Name	None [31:29]			DOP7SEL [28:24]				

Bits	Name	Description
28 : 24	DOP7SEL	Default Value: X
20 : 16	DOP6SEL	Default Value: X
12 : 8	DOP5SEL	Default Value: X
4 : 0	DOP4SEL	Default Value: X

18.1.73 UDB_DSI0_DOP_CFG2

DSI Out Pair (DOP) selection

Address: 0x40346010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			R				
Name	None [7:5]			DOP8SEL [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW				
HW Access	None			R				
Name	None [15:13]			DOP9SEL [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW				
HW Access	None			R				
Name	None [23:21]			DOP10SEL [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	None			RW				
HW Access	None			R				
Name	None [31:29]			DOP11SEL [28:24]				

Bits	Name	Description
28 : 24	DOP11SEL	Default Value: X
20 : 16	DOP10SEL	Default Value: X
12 : 8	DOP9SEL	Default Value: X
4 : 0	DOP8SEL	Default Value: X

18.1.74 UDB_DSI0_DOP_CFG3

DSI Out Pair (DOP) selection

Address: 0x40346014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			R				
Name	None [7:5]			DOP12SEL [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW				
HW Access	None			R				
Name	None [15:13]			DOP13SEL [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW				
HW Access	None			R				
Name	None [23:21]			DOP14SEL [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	None			RW				
HW Access	None			R				
Name	None [31:29]			DOP15SEL [28:24]				

Bits	Name	Description
28 : 24	DOP15SEL	Default Value: X
20 : 16	DOP14SEL	Default Value: X
12 : 8	DOP13SEL	Default Value: X
4 : 0	DOP12SEL	Default Value: X

18.1.75 UDB_DSI0_DOT_CFG0

DSI Out Triplet (DOT) selection

Address: 0x40346018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			R				
Name	None [7:5]			DOT0SEL [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW				
HW Access	None			R				
Name	None [15:13]			DOT1SEL [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW				
HW Access	None			R				
Name	None [23:21]			DOT2SEL [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	None			RW				
HW Access	None			R				
Name	None [31:29]			DOT3SEL [28:24]				

Bits	Name	Description
28 : 24	DOT3SEL	Default Value: X
20 : 16	DOT2SEL	Default Value: X
12 : 8	DOT1SEL	Default Value: X
4 : 0	DOT0SEL	Default Value: X

18.1.76 UDB_DSI0_DOT_CFG1

DSI Out Triplet (DOT) selection

Address: 0x4034601C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			R				
Name	None [7:5]			DOT4SEL [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW				
HW Access	None			R				
Name	None [15:13]			DOT5SEL [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW				
HW Access	None			R				
Name	None [23:21]			DOT6SEL [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	None			RW				
HW Access	None			R				
Name	None [31:29]			DOT7SEL [28:24]				

Bits	Name	Description
28 : 24	DOT7SEL	Default Value: X
20 : 16	DOT6SEL	Default Value: X
12 : 8	DOT5SEL	Default Value: X
4 : 0	DOT4SEL	Default Value: X

18.1.77 UDB_DSI0_DOT_CFG2

DSI Out Triplet (DOT) selection

Address: 0x40346020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			R				
Name	None [7:5]			DOT8SEL [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW				
HW Access	None			R				
Name	None [15:13]			DOT9SEL [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW				
HW Access	None			R				
Name	None [23:21]			DOT10SEL [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	None			RW				
HW Access	None			R				
Name	None [31:29]			DOT11SEL [28:24]				

Bits	Name	Description
28 : 24	DOT11SEL	Default Value: X
20 : 16	DOT10SEL	Default Value: X
12 : 8	DOT9SEL	Default Value: X
4 : 0	DOT8SEL	Default Value: X

18.1.78 UDB_DSI0_DOT_CFG3

DSI Out Triplet (DOT) selection

Address: 0x40346024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			R				
Name	None [7:5]			DOT12SEL [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW				
HW Access	None			R				
Name	None [15:13]			DOT13SEL [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW				
HW Access	None			R				
Name	None [23:21]			DOT14SEL [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	None			RW				
HW Access	None			R				
Name	None [31:29]			DOT15SEL [28:24]				

Bits	Name	Description
28 : 24	DOT15SEL	Default Value: X
20 : 16	DOT14SEL	Default Value: X
12 : 8	DOT13SEL	Default Value: X
4 : 0	DOT12SEL	Default Value: X

18.1.79 UDB_DSI0_RVO_CFG0

Right Vertical Ouput (RVO) selection

Address: 0x40346028

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			R				
Name	None [7:5]			RVO0SEL [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW				
HW Access	None			R				
Name	None [15:13]			RVO1SEL [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW				
HW Access	None			R				
Name	None [23:21]			RVO2SEL [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	None			RW				
HW Access	None			R				
Name	None [31:29]			RVO3SEL [28:24]				

Bits	Name	Description
28 : 24	RVO3SEL	Default Value: X
20 : 16	RVO2SEL	Default Value: X
12 : 8	RVO1SEL	Default Value: X
4 : 0	RVO0SEL	Default Value: X

18.1.80 UDB_DSI0_RVO_CFG1

Right Vertical Ouput (RVO) selection

Address: 0x4034602C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			R				
Name	None [7:5]			RVO4SEL [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW				
HW Access	None			R				
Name	None [15:13]			RVO5SEL [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW				
HW Access	None			R				
Name	None [23:21]			RVO6SEL [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	None			RW				
HW Access	None			R				
Name	None [31:29]			RVO7SEL [28:24]				

Bits	Name	Description
28 : 24	RVO7SEL	Default Value: X
20 : 16	RVO6SEL	Default Value: X
12 : 8	RVO5SEL	Default Value: X
4 : 0	RVO4SEL	Default Value: X

18.1.81 UDB_DSI0_RVO_CFG2

Right Vertical Ouput (RVO) selection

Address: 0x40346030

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			R				
Name	None [7:5]			RVO8SEL [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW				
HW Access	None			R				
Name	None [15:13]			RVO9SEL [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW				
HW Access	None			R				
Name	None [23:21]			RVO10SEL [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	None			RW				
HW Access	None			R				
Name	None [31:29]			RVO11SEL [28:24]				

Bits	Name	Description
28 : 24	RVO11SEL	Default Value: X
20 : 16	RVO10SEL	Default Value: X
12 : 8	RVO9SEL	Default Value: X
4 : 0	RVO8SEL	Default Value: X

18.1.82 UDB_DSI0_RVO_CFG3

Right Vertical Ouput (RVO) selection

Address: 0x40346034

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			R				
Name	None [7:5]			RVO12SEL [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW				
HW Access	None			R				
Name	None [15:13]			RVO13SEL [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW				
HW Access	None			R				
Name	None [23:21]			RVO14SEL [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	None			RW				
HW Access	None			R				
Name	None [31:29]			RVO15SEL [28:24]				

Bits	Name	Description
28 : 24	RVO15SEL	Default Value: X
20 : 16	RVO14SEL	Default Value: X
12 : 8	RVO13SEL	Default Value: X
4 : 0	RVO12SEL	Default Value: X

18.1.83 UDB_DSI0_LVO_CFG0

Left Vertical Ouput (LVO) selection

Address: 0x40346038

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	LVO1SEL [7:4]				LVO0SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	LVO3SEL [15:12]				LVO2SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW			
HW Access	R				R			
Name	LVO5SEL [23:20]				LVO4SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	R				R			
Name	LVO7SEL [31:28]				LVO6SEL [27:24]			

Bits	Name	Description
31 : 28	LVO7SEL	Default Value: X
27 : 24	LVO6SEL	Default Value: X
23 : 20	LVO5SEL	Default Value: X
19 : 16	LVO4SEL	Default Value: X
15 : 12	LVO3SEL	Default Value: X
11 : 8	LVO2SEL	Default Value: X
7 : 4	LVO1SEL	Default Value: X
3 : 0	LVO0SEL	Default Value: X

18.1.84 UDB_DSI0_LVO_CFG1

Left Vertical Ouput (LVO) selection

Address: 0x4034603C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	LVO9SEL [7:4]				LVO8SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	LVO11SEL [15:12]				LVO10SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW			
HW Access	R				R			
Name	LVO13SEL [23:20]				LVO12SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	R				R			
Name	LVO15SEL [31:28]				LVO14SEL [27:24]			

Bits	Name	Description
31 : 28	LVO15SEL	Default Value: X
27 : 24	LVO14SEL	Default Value: X
23 : 20	LVO13SEL	Default Value: X
19 : 16	LVO12SEL	Default Value: X
15 : 12	LVO11SEL	Default Value: X
11 : 8	LVO10SEL	Default Value: X
7 : 4	LVO9SEL	Default Value: X
3 : 0	LVO8SEL	Default Value: X

18.1.85 UDB_DSI0_RHO_CFG0

Right Horizontal Out (RHO) selection

Address: 0x40346040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	RHOSEL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	RHOSEL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	RHOSEL [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	RHOSEL [31:24]							

Bits	Name	Description
31 : 0	RHOSEL	Right Horizontal Output select for bits 31:0 Default Value: X

18.1.86 UDB_DSI0_RHO_CFG1

Right Horizontal Out (RHO) selection

Address: 0x40346044

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	RHOSEL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	RHOSEL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	RHOSEL [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	RHOSEL [31:24]							

Bits	Name	Description
31 : 0	RHOSEL	Right Horizontal Output select for bits 63:32 Default Value: X

18.1.87 UDB_DSI0_RHO_CFG2

Right Horizontal Out (RHO) selection

Address: 0x40346048

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	RHOSEL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	RHOSEL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	RHOSEL [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	RHOSEL [31:24]							

Bits	Name	Description
31 : 0	RHOSEL	Right Horizontal Output select for bits 95:64 Default Value: X

18.1.88 UDB_DSI0_LHO_CFG0

Left Horizontal Out (LHO) selection

Address: 0x4034604C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	LHO1SEL [7:4]				LHO0SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	LHO3SEL [15:12]				LHO2SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW			
HW Access	R				R			
Name	LHO5SEL [23:20]				LHO4SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	R				R			
Name	LHO7SEL [31:28]				LHO6SEL [27:24]			

Bits	Name	Description
31 : 28	LHO7SEL	Default Value: X
27 : 24	LHO6SEL	Default Value: X
23 : 20	LHO5SEL	Default Value: X
19 : 16	LHO4SEL	Default Value: X
15 : 12	LHO3SEL	Default Value: X
11 : 8	LHO2SEL	Default Value: X
7 : 4	LHO1SEL	Default Value: X
3 : 0	LHO0SEL	Default Value: X

18.1.89 UDB_DSI0_LHO_CFG1

Left Horizontal Out (LHO) selection

Address: 0x40346050

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	LHO9SEL [7:4]				LHO8SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	LHO11SEL [15:12]				LHO10SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW			
HW Access	R				R			
Name	LHO13SEL [23:20]				LHO12SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	R				R			
Name	LHO15SEL [31:28]				LHO14SEL [27:24]			

Bits	Name	Description
31 : 28	LHO15SEL	Default Value: X
27 : 24	LHO14SEL	Default Value: X
23 : 20	LHO13SEL	Default Value: X
19 : 16	LHO12SEL	Default Value: X
15 : 12	LHO11SEL	Default Value: X
11 : 8	LHO10SEL	Default Value: X
7 : 4	LHO9SEL	Default Value: X
3 : 0	LHO8SEL	Default Value: X

18.1.90 UDB_DSI0_LHO_CFG2

Left Horizontal Out (LHO) selection

Address: 0x40346054

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	LHO17SEL [7:4]				LHO16SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	LHO19SEL [15:12]				LHO18SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW			
HW Access	R				R			
Name	LHO21SEL [23:20]				LHO20SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	R				R			
Name	LHO23SEL [31:28]				LHO22SEL [27:24]			

Bits	Name	Description
31 : 28	LHO23SEL	Default Value: X
27 : 24	LHO22SEL	Default Value: X
23 : 20	LHO21SEL	Default Value: X
19 : 16	LHO20SEL	Default Value: X
15 : 12	LHO19SEL	Default Value: X
11 : 8	LHO18SEL	Default Value: X
7 : 4	LHO17SEL	Default Value: X
3 : 0	LHO16SEL	Default Value: X

18.1.91 UDB_DSI0_LHO_CFG3

Left Horizontal Out (LHO) selection

Address: 0x40346058

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	LHO25SEL [7:4]				LHO24SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	LHO27SEL [15:12]				LHO26SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW			
HW Access	R				R			
Name	LHO29SEL [23:20]				LHO28SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	R				R			
Name	LHO31SEL [31:28]				LHO30SEL [27:24]			

Bits	Name	Description
31 : 28	LHO31SEL	Default Value: X
27 : 24	LHO30SEL	Default Value: X
23 : 20	LHO29SEL	Default Value: X
19 : 16	LHO28SEL	Default Value: X
15 : 12	LHO27SEL	Default Value: X
11 : 8	LHO26SEL	Default Value: X
7 : 4	LHO25SEL	Default Value: X
3 : 0	LHO24SEL	Default Value: X

18.1.92 UDB_DSI0_LHO_CFG4

Left Horizontal Out (LHO) selection

Address: 0x4034605C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	LHO33SEL [7:4]				LHO32SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	LHO35SEL [15:12]				LHO34SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW			
HW Access	R				R			
Name	LHO37SEL [23:20]				LHO36SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	R				R			
Name	LHO39SEL [31:28]				LHO38SEL [27:24]			

Bits	Name	Description
31 : 28	LHO39SEL	Default Value: X
27 : 24	LHO38SEL	Default Value: X
23 : 20	LHO37SEL	Default Value: X
19 : 16	LHO36SEL	Default Value: X
15 : 12	LHO35SEL	Default Value: X
11 : 8	LHO34SEL	Default Value: X
7 : 4	LHO33SEL	Default Value: X
3 : 0	LHO32SEL	Default Value: X

18.1.93 UDB_DSI0_LHO_CFG5

Left Horizontal Out (LHO) selection

Address: 0x40346060

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	LHO41SEL [7:4]				LHO40SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	LHO43SEL [15:12]				LHO42SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW			
HW Access	R				R			
Name	LHO45SEL [23:20]				LHO44SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	R				R			
Name	LHO47SEL [31:28]				LHO46SEL [27:24]			

Bits	Name	Description
31 : 28	LHO47SEL	Default Value: X
27 : 24	LHO46SEL	Default Value: X
23 : 20	LHO45SEL	Default Value: X
19 : 16	LHO44SEL	Default Value: X
15 : 12	LHO43SEL	Default Value: X
11 : 8	LHO42SEL	Default Value: X
7 : 4	LHO41SEL	Default Value: X
3 : 0	LHO40SEL	Default Value: X

18.1.94 UDB_DSI0_LHO_CFG6

Left Horizontal Out (LHO) selection

Address: 0x40346064

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	LHO49SEL [7:4]				LHO48SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	LHO51SEL [15:12]				LHO50SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW			
HW Access	R				R			
Name	LHO53SEL [23:20]				LHO52SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	R				R			
Name	LHO55SEL [31:28]				LHO54SEL [27:24]			

Bits	Name	Description
31 : 28	LHO55SEL	Default Value: X
27 : 24	LHO54SEL	Default Value: X
23 : 20	LHO53SEL	Default Value: X
19 : 16	LHO52SEL	Default Value: X
15 : 12	LHO51SEL	Default Value: X
11 : 8	LHO50SEL	Default Value: X
7 : 4	LHO49SEL	Default Value: X
3 : 0	LHO48SEL	Default Value: X

18.1.95 UDB_DSI0_LHO_CFG7

Left Horizontal Out (LHO) selection

Address: 0x40346068

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	LHO57SEL [7:4]				LHO56SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	LHO59SEL [15:12]				LHO58SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW			
HW Access	R				R			
Name	LHO61SEL [23:20]				LHO60SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	R				R			
Name	LHO63SEL [31:28]				LHO62SEL [27:24]			

Bits	Name	Description
31 : 28	LHO63SEL	Default Value: X
27 : 24	LHO62SEL	Default Value: X
23 : 20	LHO61SEL	Default Value: X
19 : 16	LHO60SEL	Default Value: X
15 : 12	LHO59SEL	Default Value: X
11 : 8	LHO58SEL	Default Value: X
7 : 4	LHO57SEL	Default Value: X
3 : 0	LHO56SEL	Default Value: X

18.1.96 UDB_DSI0_LHO_CFG8

Left Horizontal Out (LHO) selection

Address: 0x4034606C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	LHO65SEL [7:4]				LHO64SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	LHO67SEL [15:12]				LHO66SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW			
HW Access	R				R			
Name	LHO69SEL [23:20]				LHO68SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	R				R			
Name	LHO71SEL [31:28]				LHO70SEL [27:24]			

Bits	Name	Description
31 : 28	LHO71SEL	Default Value: X
27 : 24	LHO70SEL	Default Value: X
23 : 20	LHO69SEL	Default Value: X
19 : 16	LHO68SEL	Default Value: X
15 : 12	LHO67SEL	Default Value: X
11 : 8	LHO66SEL	Default Value: X
7 : 4	LHO65SEL	Default Value: X
3 : 0	LHO64SEL	Default Value: X

18.1.97 UDB_DSI0_LHO_CFG9

Left Horizontal Out (LHO) selection

Address: 0x40346070

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	LHO73SEL [7:4]				LHO72SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	LHO75SEL [15:12]				LHO74SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW			
HW Access	R				R			
Name	LHO77SEL [23:20]				LHO76SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	R				R			
Name	LHO79SEL [31:28]				LHO78SEL [27:24]			

Bits	Name	Description
31 : 28	LHO79SEL	Default Value: X
27 : 24	LHO78SEL	Default Value: X
23 : 20	LHO77SEL	Default Value: X
19 : 16	LHO76SEL	Default Value: X
15 : 12	LHO75SEL	Default Value: X
11 : 8	LHO74SEL	Default Value: X
7 : 4	LHO73SEL	Default Value: X
3 : 0	LHO72SEL	Default Value: X

18.1.98 UDB_DSI0_LHO_CFG10

Left Horizontal Out (LHO) selection

Address: 0x40346074

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	LHO81SEL [7:4]				LHO80SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	LHO83SEL [15:12]				LHO82SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW			
HW Access	R				R			
Name	LHO85SEL [23:20]				LHO84SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	R				R			
Name	LHO87SEL [31:28]				LHO86SEL [27:24]			

Bits	Name	Description
31 : 28	LHO87SEL	Default Value: X
27 : 24	LHO86SEL	Default Value: X
23 : 20	LHO85SEL	Default Value: X
19 : 16	LHO84SEL	Default Value: X
15 : 12	LHO83SEL	Default Value: X
11 : 8	LHO82SEL	Default Value: X
7 : 4	LHO81SEL	Default Value: X
3 : 0	LHO80SEL	Default Value: X

18.1.99 UDB_DSI0_LHO_CFG11

Left Horizontal Out (LHO) selection

Address: 0x40346078

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	LHO89SEL [7:4]				LHO88SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	LHO91SEL [15:12]				LHO90SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW			
HW Access	R				R			
Name	LHO93SEL [23:20]				LHO92SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	R				R			
Name	LHO95SEL [31:28]				LHO94SEL [27:24]			

Bits	Name	Description
31 : 28	LHO95SEL	Default Value: X
27 : 24	LHO94SEL	Default Value: X
23 : 20	LHO93SEL	Default Value: X
19 : 16	LHO92SEL	Default Value: X
15 : 12	LHO91SEL	Default Value: X
11 : 8	LHO90SEL	Default Value: X
7 : 4	LHO89SEL	Default Value: X
3 : 0	LHO88SEL	Default Value: X

18.1.100 UDB_PA0_CFG0

PA Data In Clock Control Register

Address: 0x40347000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	RW		RW	
HW Access	None		R	R	R		R	
Name	None [7:6]		CLKIN_INV	CLKIN_EN_INV	CLKIN_EN_MODE [3:2]		CLKIN_EN_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	CLKIN_INV	Determines whether the selected clock is inverted or not. Default Value: 0 **0x0: NOINV :** Not Inverted **0x1: INV :** Inverted
4	CLKIN_EN_INV	Determines whether the selected enable is inverted or not. Default Value: 0 **0x0: NOINV :** Not Inverted **0x1: INV :** Inverted
3 : 2	CLKIN_EN_MODE	Select one of four operating modes Default Value: 0

18.1.100 UDB_PA0_CFG0 (continued)

		0x0: OFF : Always off **0x1: ON :** Always on **0x2: POSEDGE :** Positive edge - A clock is output on a 0 to 1 transition on the enable input **0x3: LEVEL :** Level sensitive - A clock is output when the enable is high.
1 : 0	CLKIN_EN_SEL	Select one of four choices for clock enable Default Value: 0 **0x0: PIN_RC :** pin_rc - port pin multiplexer output **0x1: DSI_RC_0 :** dsi_rc[0] - dsi_xx_out_p[4] **0x2: DSI_RC_1 :** dsi_rc[1] - dsi_xx_out_p[5] **0x3: DSI_RC_2 :** dsi_rc{1} - dsi_xx_out_p[6]

18.1.101 UDB_PA0_CFG1

PA Data Out Clock Control Register

Address: 0x40347004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	RW		RW	
HW Access	None		R	R	R		R	
Name	None [7:6]		CLKOUT_-INV	CLK-OUT_EN_-INV	CLKOUT_EN_MODE [3:2]		CLKOUT_EN_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	CLKOUT_INV	Determines whether the selected clock is inverted or not. Default Value: 0 **0x0: NOINV :** Not Inverted **0x1: INV :** Inverted
4	CLKOUT_EN_INV	Determines whether the selected enable is inverted or not. Default Value: 0 **0x0: NOINV :** Not Inverted **0x1: INV :** Inverted
3 : 2	CLKOUT_EN_MODE	Select one of four operating modes Default Value: 0

18.1.101 UDB_PA0_CFG1 (continued)

		0x0: OFF : Always off **0x1: ON :** Always on **0x2: POSEDGE :** Positive edge - A clock is output on a 0 to 1 transition on the enable input **0x3: LEVEL :** Level sensitive - A clock is output when the enable is high.
1 : 0	CLKOUT_EN_SEL	Select one of four choices for clock enable Default Value: 0 **0x0: PIN_RC :** pin_rc - port pin multiplexer output **0x1: DSI_RC_0 :** dsi_rc[0] - dsi_xx_out_p[4] **0x2: DSI_RC_1 :** dsi_rc[1] - dsi_xx_out_p[5] **0x3: DSI_RC_2 :** dsi_rc{1} - dsi_xx_out_p[6]

18.1.102 UDB_PA0_CFG2

PA Clock Select Register

Address: 0x40347008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	CLKOUT_SEL [7:4]				CLKIN_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	CLKOUT_SEL	Select one of four choices for clock enable Default Value: 0 **0x0: GCLK0 :** gclk[0] **0x1: GCLK1 :** gclk[1] **0x2: GCLK2 :** gclk[2] **0x3: GCLK3 :** gclk[3] **0x4: GCLK4 :** gclk[4] **0x5: GCLK5 :** gclk[5] **0x6: GCLK6 :** gclk[6]

18.1.102 UDB_PA0_CFG2 (continued)

		0x7: GCLK7 : gclk[7]
		0x9: BUS_CLK_APP : bus_clk_app
		0xc: PIN_RC : pin_rc - port pin multiplexer output
		0xd: DSI_RC_0 : dsi_rc[0] - dsi_xx_out_p[4]
		0xe: DSI_RC_1 : dsi_rc[1] - dsi_xx_out_p[5]
		0xf: DSI_RC_2 : dsi_rc{1} - dsi_xx_out_p[6]
3 : 0	CLKIN_SEL	Select one of four choices for clock enable Default Value: 0
		0x0: GCLK0 : gclk[0]
		0x1: GCLK1 : gclk[1]
		0x2: GCLK2 : gclk[2]
		0x3: GCLK3 : gclk[3]
		0x4: GCLK4 : gclk[4]
		0x5: GCLK5 : gclk[5]
		0x6: GCLK6 : gclk[6]
		0x7: GCLK7 : gclk[7]
		0x9: BUS_CLK_APP : bus_clk_app
		0xc: PIN_RC : pin_rc - port pin multiplexer output
		0xd: DSI_RC_0 : dsi_rc[0] - dsi_xx_out_p[4]
		0xe: DSI_RC_1 : dsi_rc[1] - dsi_xx_out_p[5]
		0xf: DSI_RC_2 : dsi_rc{1} - dsi_xx_out_p[6]

18.1.103 UDB_PA0_CFG3

PA Reset Select Register

Address: 0x4034700C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	RW		None	RW	RW	
HW Access	None	R	R		None	R	R	
Name	None	RES_OUT_INV	RES_OUT_SEL [5:4]		None	RES_IN_INV	RES_IN_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
6	RES_OUT_INV	Select the polarity of the reset control. Default Value: 0 **0x0: NOINV :** Not Inverted **0x1: INV :** Inverted
5 : 4	RES_OUT_SEL	Select one of four inputs to serve as the reset control to the block. Default Value: 0 **0x0: PIN_RC :** pin_rc - port pin multiplexer output **0x1: DSI_RC_0 :** dsi_rc[0] - dsi_xx_out_p[4] **0x2: DSI_RC_1 :** dsi_rc[1] - dsi_xx_out_p[5]

		0x3: DSI_RC_2 : dsi_rc{1} - dsi_xx_out_p[6]
2	RES_IN_INV	Select the polarity of the reset control. Default Value: 0
		0x0: NOINV : Not Inverted
		0x1: INV : Inverted
1 : 0	RES_IN_SEL	Select one of four inputs to serve as the reset control to the block. Default Value: 0
		0x0: PIN_RC : pin_rc - port pin multiplexer output
		0x1: DSI_RC_0 : dsi_rc[0] - dsi_xx_out_p[4]
		0x2: DSI_RC_1 : dsi_rc[1] - dsi_xx_out_p[5]
		0x3: DSI_RC_2 : dsi_rc{1} - dsi_xx_out_p[6]

18.1.104 UDB_PA0_CFG4

PA Reset Enable Register

Address: 0x40347010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [7:3]					RES_OE_EN	RES_OUT_EN	RES_IN_EN

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	RES_OE_EN	Enable the selected reset Default Value: 0 **0x0: DISABLE :** Reset Disabled **0x1: ENABLE :** Reset Enabled
1	RES_OUT_EN	Enable the selected reset Default Value: 0 **0x0: DISABLE :** Reset Disabled **0x1: ENABLE :** Reset Enabled
0	RES_IN_EN	Enable the selected reset Default Value: 0

0x0: DISABLE :
Reset Disabled

0x1: ENABLE :
Reset Enabled

18.1.105 UDB_PA0_CFG5

PA Reset Pin Select Register

Address: 0x40347014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW		
HW Access	None					R		
Name	None [7:3]					PIN_SEL [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2 : 0	PIN_SEL	Select port input to route to reset multiplexer (dsi_xx_input_p[7:0]) Default Value: 0 **0x0: PIN0 :** dsi_from_port_pin[0] **0x1: PIN1 :** dsi_from_port_pin[1] **0x2: PIN2 :** dsi_from_port_pin[2] **0x3: PIN3 :** dsi_from_port_pin[3] **0x4: PIN4 :** dsi_from_port_pin[4] **0x5: PIN5 :** dsi_from_port_pin[5]

0x6: PIN6 :
dsi_from_port_pin[6]

0x7: PIN7 :
dsi_from_port_pin[7]

18.1.106 UDB_PA0_CFG6

PA Input Data Sync Control Register - Low

Address: 0x40347018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	IN_SYNC3 [7:6]		IN_SYNC2 [5:4]		IN_SYNC1 [3:2]		IN_SYNC0 [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	IN_SYNC3	Synchronization selection for PA input 3 Default Value: 0 **0x0: TRANSPARENT :** transparent **0x1: SINGLESYNC :** single sync **0x2: DOUBLESYNC :** double sync **0x3: RESERVED :** reserved
5 : 4	IN_SYNC2	Synchronization selection for PA input 2 Default Value: 0 **0x0: TRANSPARENT :** transparent **0x1: SINGLESYNC :** single sync

18.1.106 UDB_PA0_CFG6 (continued)

		0x2: DOUBLESYNC : double sync
		0x3: RESERVED : reserved
3 : 2	IN_SYNC1	Synchronization selection for PA input 1 Default Value: 0
		0x0: TRANSPARENT : transparent
		0x1: SINGLESYNC : single sync
		0x2: DOUBLESYNC : double sync
		0x3: RESERVED : reserved
1 : 0	IN_SYNC0	Synchronization selection for PA input 0 Default Value: 0
		0x0: TRANSPARENT : transparent
		0x1: SINGLESYNC : single sync
		0x2: DOUBLESYNC : double sync
		0x3: RESERVED : reserved

18.1.107 UDB_PA0_CFG7

PA Input Data Sync Control Register - High

Address: 0x4034701C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	IN_SYNC7 [7:6]		IN_SYNC6 [5:4]		IN_SYNC5 [3:2]		IN_SYNC4 [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	IN_SYNC7	Synchronization selection for PA input 7 Default Value: 0 **0x0: TRANSPARENT :** transparent **0x1: SINGLESYNC :** single sync **0x2: DOUBLESYNC :** double sync **0x3: RESERVED :** reserved
5 : 4	IN_SYNC6	Synchronization selection for PA input 6 Default Value: 0 **0x0: TRANSPARENT :** transparent **0x1: SINGLESYNC :** single sync

18.1.107 UDB_PA0_CFG7 (continued)

		0x2: DOUBLESYNC : double sync
		0x3: RESERVED : reserved
3 : 2	IN_SYNC5	Synchronization selection for PA input 5 Default Value: 0
		0x0: TRANSPARENT : transparent
		0x1: SINGLESYNC : single sync
		0x2: DOUBLESYNC : double sync
		0x3: RESERVED : reserved
1 : 0	IN_SYNC4	Synchronization selection for PA input 4 Default Value: 0
		0x0: TRANSPARENT : transparent
		0x1: SINGLESYNC : single sync
		0x2: DOUBLESYNC : double sync
		0x3: RESERVED : reserved

18.1.108 UDB_PA0_CFG8

PA Output Data Sync Control Register - Low

Address: 0x40347020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	OUT_SYNC3 [7:6]		OUT_SYNC2 [5:4]		OUT_SYNC1 [3:2]		OUT_SYNC0 [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	OUT_SYNC3	Synchronization selection for PA output 3 Default Value: 0 **0x0: TRANSPARENT :** transparent **0x1: SINGLESYNC :** single sync **0x2: CLOCK :** clock **0x3: CLOCKINV :** clock inverted
5 : 4	OUT_SYNC2	Synchronization selection for PA output 2 Default Value: 0 **0x0: TRANSPARENT :** transparent **0x1: SINGLESYNC :** single sync

18.1.108 UDB_PA0_CFG8 (continued)

		0x2: CLOCK : clock
		0x3: CLOCKINV : clock inverted
3 : 2	OUT_SYNC1	Synchronization selection for PA output 1 Default Value: 0
		0x0: TRANSPARENT : transparent
		0x1: SINGLESYNC : single sync
		0x2: CLOCK : clock
		0x3: CLOCKINV : clock inverted
1 : 0	OUT_SYNC0	Synchronization selection for PA output 0 Default Value: 0
		0x0: TRANSPARENT : transparent
		0x1: SINGLESYNC : single sync
		0x2: CLOCK : clock
		0x3: CLOCKINV : clock inverted

18.1.109 UDB_PA0_CFG9

PA Output Data Sync Control Register - High

Address: 0x40347024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	OUT_SYNC7 [7:6]		OUT_SYNC6 [5:4]		OUT_SYNC5 [3:2]		OUT_SYNC4 [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	OUT_SYNC7	Synchronization selection for PA output 7 Default Value: 0 **0x0: TRANSPARENT :** transparent **0x1: SINGLESYNC :** single sync **0x2: CLOCK :** clock **0x3: CLOCKINV :** clock inverted
5 : 4	OUT_SYNC6	Synchronization selection for PA output 6 Default Value: 0 **0x0: TRANSPARENT :** transparent **0x1: SINGLESYNC :** single sync

18.1.109 UDB_PA0_CFG9 (continued)

		0x2: CLOCK : clock **0x3: CLOCKINV :** clock inverted
3 : 2	OUT_SYNC5	Synchronization selection for PA output 5 Default Value: 0 **0x0: TRANSPARENT :** transparent **0x1: SINGLESYNC :** single sync **0x2: CLOCK :** clock **0x3: CLOCKINV :** clock inverted
1 : 0	OUT_SYNC4	Synchronization selection for PA output 4 Default Value: 0 **0x0: TRANSPARENT :** transparent **0x1: SINGLESYNC :** single sync **0x2: CLOCK :** clock **0x3: CLOCKINV :** clock inverted

18.1.110 UDB_PA0_CFG10

PA Output Data Select Register - Low

Address: 0x40347028

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	DATA_SEL3 [7:6]		DATA_SEL2 [5:4]		DATA_SEL1 [3:2]		DATA_SEL0 [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	DATA_SEL3	Data selection for PA output 3 Default Value: 0 **0x0: DSI_OUTPUT0 :** dsi output 0 **0x1: DSI_OUTPUT1 :** dsi output 1 **0x2: DSI_OUTPUT2 :** dsi output 2 **0x3: DSI_OUTPUT3 :** dsi output 3
5 : 4	DATA_SEL2	Data selection for PA output 2 Default Value: 0 **0x0: DSI_OUTPUT0 :** dsi output 0 **0x1: DSI_OUTPUT1 :** dsi output 1

18.1.110 UDB_PA0_CFG10 (continued)

		0x2: DSI_OUTPUT2 : dsi output 2
		0x3: DSI_OUTPUT3 : dsi output 3
3 : 2	DATA_SEL1	Data selection for PA output 1 Default Value: 0
		0x0: DSI_OUTPUT0 : dsi output 0
		0x1: DSI_OUTPUT1 : dsi output 1
		0x2: DSI_OUTPUT2 : dsi output 2
		0x3: DSI_OUTPUT3 : dsi output 3
1 : 0	DATA_SEL0	Data selection for PA output 0 Default Value: 0
		0x0: DSI_OUTPUT0 : dsi output 0
		0x1: DSI_OUTPUT1 : dsi output 1
		0x2: DSI_OUTPUT2 : dsi output 2
		0x3: DSI_OUTPUT3 : dsi output 3

18.1.111 UDB_PA0_CFG11

PA Output Data Select Register - High

Address: 0x4034702C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	DATA_SEL7 [7:6]		DATA_SEL6 [5:4]		DATA_SEL5 [3:2]		DATA_SEL4 [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	DATA_SEL7	Data selection for PA output 7 Default Value: 0 **0x0: DSI_OUTPUT4 :** dsi output 4 **0x1: DSI_OUTPUT5 :** dsi output 5 **0x2: DSI_OUTPUT6 :** dsi output 6 **0x3: DSI_OUTPUT7 :** dsi output 7
5 : 4	DATA_SEL6	Data selection for PA output 6 Default Value: 0 **0x0: DSI_OUTPUT4 :** dsi output 4 **0x1: DSI_OUTPUT5 :** dsi output 5

18.1.111 UDB_PA0_CFG11 (continued)

		0x2: DSI_OUTPUT6 : dsi output 6
		0x3: DSI_OUTPUT7 : dsi output 7
3 : 2	DATA_SEL5	Data selection for PA output 5 Default Value: 0
		0x0: DSI_OUTPUT4 : dsi output 4
		0x1: DSI_OUTPUT5 : dsi output 5
		0x2: DSI_OUTPUT6 : dsi output 6
		0x3: DSI_OUTPUT7 : dsi output 7
1 : 0	DATA_SEL4	Data selection for PA output 4 Default Value: 0
		0x0: DSI_OUTPUT4 : dsi output 4
		0x1: DSI_OUTPUT5 : dsi output 5
		0x2: DSI_OUTPUT6 : dsi output 6
		0x3: DSI_OUTPUT7 : dsi output 7

18.1.112 UDB_PA0_CFG12

PA OE Select Register - Low

Address: 0x40347030

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	OE_SEL3 [7:6]		OE_SEL2 [5:4]		OE_SEL1 [3:2]		OE_SEL0 [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	OE_SEL3	Data selection for PA oe 3 Default Value: 0 **0x0: DSI_OE_OUT0 :** synchronized dsi oe output 0 **0x1: DSI_OE_OUT1 :** synchronized dsi oe output 1 **0x2: DSI_OE_OUT2 :** synchronized dsi oe output 2 **0x3: DSI_OE_OUT3 :** synchronized dsi oe output 3
5 : 4	OE_SEL2	Data selection for PA oe 2 Default Value: 0 **0x0: DSI_OE_OUT0 :** synchronized dsi oe output 0 **0x1: DSI_OE_OUT1 :** synchronized dsi oe output 1

18.1.112 UDB_PA0_CFG12 (continued)

		0x2: DSI_OE_OUT2 : synchronized dsi oe output 2
		0x3: DSI_OE_OUT3 : synchronized dsi oe output 3
3 : 2	OE_SEL1	Data selection for PA oe 1 Default Value: 0
		0x0: DSI_OE_OUT0 : synchronized dsi oe output 0
		0x1: DSI_OE_OUT1 : synchronized dsi oe output 1
		0x2: DSI_OE_OUT2 : synchronized dsi oe output 2
		0x3: DSI_OE_OUT3 : synchronized dsi oe output 3
1 : 0	OE_SEL0	Data selection for PA oe 0 Default Value: 0
		0x0: DSI_OE_OUT0 : synchronized dsi oe output 0
		0x1: DSI_OE_OUT1 : synchronized dsi oe output 1
		0x2: DSI_OE_OUT2 : synchronized dsi oe output 2
		0x3: DSI_OE_OUT3 : synchronized dsi oe output 3

18.1.113 UDB_PA0_CFG13

PA OE Select Register - High

Address: 0x40347034

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	OE_SEL7 [7:6]		OE_SEL6 [5:4]		OE_SEL5 [3:2]		OE_SEL4 [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	OE_SEL7	Data selection for PA oe 7 Default Value: 0 **0x0: DSI_OE_OUT0 :** synchronized dsi oe output 0 **0x1: DSI_OE_OUT1 :** synchronized dsi oe output 1 **0x2: DSI_OE_OUT2 :** synchronized dsi oe output 2 **0x3: DSI_OE_OUT3 :** synchronized dsi oe output 3
5 : 4	OE_SEL6	Data selection for PA oe 6 Default Value: 0 **0x0: DSI_OE_OUT0 :** synchronized dsi oe output 0 **0x1: DSI_OE_OUT1 :** synchronized dsi oe output 1

18.1.113 UDB_PA0_CFG13 (continued)

		0x2: DSI_OE_OUT2 : synchronized dsi oe output 2
		0x3: DSI_OE_OUT3 : synchronized dsi oe output 3
3 : 2	OE_SEL5	Data selection for PA oe 5 Default Value: 0
		0x0: DSI_OE_OUT0 : synchronized dsi oe output 0
		0x1: DSI_OE_OUT1 : synchronized dsi oe output 1
		0x2: DSI_OE_OUT2 : synchronized dsi oe output 2
		0x3: DSI_OE_OUT3 : synchronized dsi oe output 3
1 : 0	OE_SEL4	Data selection for PA oe 4 Default Value: 0
		0x0: DSI_OE_OUT0 : synchronized dsi oe output 0
		0x1: DSI_OE_OUT1 : synchronized dsi oe output 1
		0x2: DSI_OE_OUT2 : synchronized dsi oe output 2
		0x3: DSI_OE_OUT3 : synchronized dsi oe output 3

18.1.114 UDB_PA0_CFG14

PA OE Sync Register

Address: 0x40347038

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	OE_SYNC3 [7:6]		OE_SYNC2 [5:4]		OE_SYNC1 [3:2]		OE_SYNC0 [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	OE_SYNC3	Synchronization options for dsi_to_oe[3] Default Value: 0 **0x0: TRANSPARENT :** transparent **0x1: SINGLESYNC :** single sync **0x2: CONSTANT1 :** 1: (Active high OE Enabled) **0x3: CONSTANT0 :** 0: (Active high OE Disabled)
5 : 4	OE_SYNC2	Synchronization options for dsi_to_oe[2] Default Value: 0 **0x0: TRANSPARENT :** transparent **0x1: SINGLESYNC :** single sync

18.1.114 UDB_PA0_CFG14 (continued)

		0x2: CONSTANT1 : 1: (Active high OE Enabled) **0x3: CONSTANT0 :** 0: (Active high OE Disabled)
3 : 2	OE_SYNC1	Synchronization options for dsi_to_oe[1] Default Value: 0 **0x0: TRANSPARENT :** transparent **0x1: SINGLESYNC :** single sync **0x2: CONSTANT1 :** 1: (Active high OE Enabled) **0x3: CONSTANT0 :** 0: (Active high OE Disabled)
1 : 0	OE_SYNC0	Synchronization options for dsi_to_oe[0] Default Value: 0 **0x0: TRANSPARENT :** transparent **0x1: SINGLESYNC :** single sync **0x2: CONSTANT1 :** 1: (Active high OE Enabled) **0x3: CONSTANT0 :** 0: (Active high OE Disabled)

18.1.115 UDB_BCTL_MDCLK_EN

Master Digital Clock Enable Register

Address: 0x40347800

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DCEN [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DCEN	Master digital clock enable for the digital clock that matches the index. Default Value: 0 **0x0: DISABLE :** Disabled **0x1: ENABLE :** Enabled

18.1.116 UDB_BCTL_MBCLK_EN

Master clk_peri_app Enable Register

Address: 0x40347804

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							BCEN

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	BCEN	clk_peri_app master enable Default Value: 0 **0x0: DISABLE :** Disabled **0x1: ENABLE :** Enabled

18.1.117 UDB_BCTL_BOTSEL_L

Lower Nibble Bottom Digital Clock Select Register

Address: 0x40347808

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	CLK_SEL3 [7:6]		CLK_SEL2 [5:4]		CLK_SEL1 [3:2]		CLK_SEL0 [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	CLK_SEL3	Clock selection control for digital clock Default Value: 0 **0x0: EDGE_ENABLES :** clock generated from edge enables from clock distribution block **0x1: PORT_INPUT :** Port input **0x2: DSI_OUTPUT :** DSI output **0x3: SYNC_DSI_OUTPUT :** synchronized DSI output
5 : 4	CLK_SEL2	Clock selection control for digital clock Default Value: 0 **0x0: EDGE_ENABLES :** clock generated from edge enables from clock distribution block **0x1: PORT_INPUT :** Port input

18.1.117 UDB_BCTL_BOTSEL_L (continued)

		0x2: DSI_OUTPUT : DSI output
		0x3: SYNC_DSI_OUTPUT : synchronized DSI output
3 : 2	CLK_SEL1	Clock selection control for digital clock Default Value: 0
		0x0: EDGE_ENABLES : clock generated from edge enables from clock distribution block
		0x1: PORT_INPUT : Port input
		0x2: DSI_OUTPUT : DSI output
		0x3: SYNC_DSI_OUTPUT : synchronized DSI output
1 : 0	CLK_SEL0	Clock selection control for digital clock Default Value: 0
		0x0: EDGE_ENABLES : clock generated from edge enables from clock distribution block
		0x1: PORT_INPUT : Port input
		0x2: DSI_OUTPUT : DSI output
		0x3: SYNC_DSI_OUTPUT : synchronized DSI output

18.1.118 UDB_BCTL_BOTSEL_U

Upper Nibble Bottom Digital Clock Select Register

Address: 0x4034780C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	CLK_SEL7 [7:6]		CLK_SEL6 [5:4]		CLK_SEL5 [3:2]		CLK_SEL4 [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	CLK_SEL7	Clock selection control for digital clock Default Value: 0 **0x0: EDGE_ENABLES :** clock generated from edge enables from clock distribution block **0x1: PORT_INPUT :** Port input **0x2: DSI_OUTPUT :** DSI output **0x3: SYNC_DSI_OUTPUT :** synchronized DSI output
5 : 4	CLK_SEL6	Clock selection control for digital clock Default Value: 0 **0x0: EDGE_ENABLES :** clock generated from edge enables from clock distribution block **0x1: PORT_INPUT :** Port input

18.1.118 UDB_BCTL_BOTSEL_U (continued)

		0x2: DSI_OUTPUT : DSI output
		0x3: SYNC_DSI_OUTPUT : synchronized DSI output
3 : 2	CLK_SEL5	Clock selection control for digital clock Default Value: 0
		0x0: EDGE_ENABLES : clock generated from edge enables from clock distribution block
		0x1: PORT_INPUT : Port input
		0x2: DSI_OUTPUT : DSI output
		0x3: SYNC_DSI_OUTPUT : synchronized DSI output
1 : 0	CLK_SEL4	Clock selection control for digital clock Default Value: 0
		0x0: EDGE_ENABLES : clock generated from edge enables from clock distribution block
		0x1: PORT_INPUT : Port input
		0x2: DSI_OUTPUT : DSI output
		0x3: SYNC_DSI_OUTPUT : synchronized DSI output

18.1.119 UDB_BCTL_QCLK_EN0

Quadrant Digital Clock Enable Registers

Address: 0x40347810

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DCEN_Q [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	None		RW
HW Access	None				R	None		R
Name	None [15:12]				DIS-ABLE_ROUTE	None [10:9]		BCEN_Q

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	DISABLE_ROUTE	By default, when this bit is set to '0', the quadrant routing (for 2 channels in the quadrant) are enabled when the global route enable for the bank is set. However, when this bit is set to '1', the routing in the associated quadrant is disabled and is not enabled by the global route enable bit. The routing will remain in a benign state until it is subsequently configured and then enabled by clearing this bit. Default Value: 0 **0x0: DISABLE :** The routing in this quadrant can be enabled with the bank route enable bit. (default) **0x1: ENABLE :** The routing in this quadrant is disabled and held in a benign state.
8	BCEN_Q	clk_peri_app quadrant enable Default Value: 0 **0x0: DISABLE :** clk_peri_app to the quadrant is disabled **0x1: ENABLE :** clk_peri_app to the quadrant is enabled

18.1.119 UDB_BCTL_QCLK_EN0 (continued)

7 : 0	DCEN_Q	Digital clock enable for indexed digital clock for the associated quadrant. Default Value: 0 **0x0: DISABLE :** Disabled **0x1: ENABLE :** Enabled

18.1.120 UDB_UDBIF_BANK_CTL

Bank Control

Address: 0x40347900

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [7:3]					BANK_EN	ROUTE_EN	DIS_COR

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							READ_WAIT

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	READ_WAIT	AHB wait states for read operations. This is required to be set if any of the following conditions are true (substitute 20 MHz for 50 MHz if in ULP mode voltage): 1. clk_sys > 50 MHz 2. Reads from WRKONE/WRKMULT.A0/A1/D0/D1 if those are being clocked on clk_dpath and clk_dpath > 50 MHz. 3. Reads from WRKONE/WRKMULT.CTL when the control register is configured in pulse mode and clk_peri > 50 MHz. 4. Reads from WRKONE/WRKMULT.MC if clk_pld > 50 MHz. Default Value: 1 **0x0: ZERO_WAIT_STATES :** Zero wait states **0x1: ONE_WAIT_STATE :** One wait state
2	BANK_EN	Enable Bank Default Value: 0 **0x0: DISABLE :** Bank disabled

18.1.120 UDB_UDBIF_BANK_CTL (continued)

		0x1: ENABLE : Bank enabled
1	ROUTE_EN	Enable Routing Default Value: 0
		0x0: DISABLE : Routing disabled
		0x1: ENABLE : Routing enabled
0	DIS_COR	If Clear-On-Read is enabled it will prevent any changes to the Status registers or FIFOs anywhere in the array as a result of reads. This aids in SW debug. Default Value: 0
		0x0: NORMAL : Clear-On-Read enabled
		0x1: DISABLE : Clear-On-Read disabled

18.1.121 UDB_UDBIF_INT_CLK_CTL

Interrupt Clock Control

Address: 0x40347904

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							INT_-CLK_EN-ABLE

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	INT_CLK_ENABLE	This bit enables the interrupt synchronizer in the UDB interface. It needs to be set whenever UDB/DSI interrupts are used. Disabling the interrupt synchronizer saves power in Active/Sleep mode. Default Value: 0

18.1.122 UDB_UDBIF_INT_CFG

Interrupt Configuration

Address: 0x40347908

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	INT_MODE_CFG [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INT_MODE_CFG [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	INT_MODE_CFG	Interrupt Mode; bit position corresponds to interrupt Default Value: 0 **0x0: LEVEL :** Level **0x1: PULSE :** Pulse

18.1.123 UDB_UDBIF_TR_CLK_CTL

Trigger Clock Control

Address: 0x4034790C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							TR_-CLOCK_ENABLE

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	TR_CLOCK_ENABLE	This bit enables/disables the clock and reset of the DMA request logic. Default Value: 0

18.1.124 UDB_UDBIF_TR_CFG

Trigger Configuration

Address: 0x40347910

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	TR_MODE_CFG [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	TR_MODE_CFG [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	TR_MODE_CFG	Trigger Mode Configuration '0' : dsi_tr[i] is tied to udb_tr_out[i] '1' : dsi_tr[i] is synchronized to clk_tr before being sourced to dsi_tr[i] Default Value: 0

18.1.125 UDB_UDBIF_PRIVATE

Internal use only

Address: 0x40347914

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							PIPE-LINE_MD

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	PIPELINE_MD	Implements pipeline stages to breakup timing loops to aid internal design analysis. '0' : Normal functional mode. '1' : Pipeline stages muxed in (not for customer use) Default Value: 0

19 Low-Power Comparator Registers

This section discusses the Low-Power Comparator (LPCOMP) registers. It lists all the registers in mapping tables, in address order.

19.1 Register Details

Register	Address	Description
LPCOMP_CONFIG	0x40350000	LPCOMP Configuration Register
LPCOMP_STATUS	0x40350004	LPCOMP Status Register
LPCOMP_INTR	0x40350010	LPCOMP Interrupt request register
LPCOMP_INTR_SET	0x40350014	LPCOMP Interrupt set register
LPCOMP_INTR_MASK	0x40350018	LPCOMP Interrupt request mask
LPCOMP_INTR_MASKED	0x4035001C	LPCOMP Interrupt request masked
LPCOMP_CMP0_CTRL	0x40350040	Comparator 0 control Register
LPCOMP_CMP0_SW	0x40350050	Comparator 0 switch control
LPCOMP_CMP0_SW_CLEAR	0x40350054	Comparator 0 switch control clear
LPCOMP_CMP1_CTRL	0x40350080	Comparator 1 control Register
LPCOMP_CMP1_SW	0x40350090	Comparator 1 switch control
LPCOMP_CMP1_SW_CLEAR	0x40350094	Comparator 1 switch control clear

19.1.1 LPCOMP_CONFIG

LPCOMP Configuration Register

Address: 0x40350000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None					
HW Access	R	R	None					
Name	ENABLED	LPREF_EN	None					

Bits	Name	Description
31	ENABLED	- 0: LPCOMP disabled (puts analog in power down, opens all switches, all clocks turned off) - 1: LPCOMP enabled Default Value: 0
30	LPREF_EN	Enable the local reference generator circuit to generate the local Vref and Ibias. Ibias current is an alternative to the reference current IREF generated by SRSS. This bit must be set for System Deep Sleep and System Hibernate operation. Default Value: 0

19.1.2 LPCOMP_STATUS

LPCOMP Status Register

Address: 0x40350004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							OUT0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							R
HW Access	None							RW
Name	None [23:17]							OUT1

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
16	OUT1	Current output value of the comparator 1. Default Value: 0
0	OUT0	Current output value of the comparator 0. Default Value: 0

19.1.3 LPCOMP_INTR

LPCOMP Interrupt request register

Address: 0x40350010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1C	RW1C
HW Access	None						RW1S	RW1S
Name	None [7:2]						COMP1	COMP0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	COMP1	Comparator 1 Interrupt: hardware sets this interrupt when comparator 1 triggers. Write with '1' to clear bit. Default Value: 0
0	COMP0	Comparator 0 Interrupt: hardware sets this interrupt when comparator 0 triggers. Write with '1' to clear bit. Default Value: 0

19.1.4 LPCOMP_INTR_SET

LPCOMP Interrupt set register

Address: 0x40350014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1S	RW1S
HW Access	None						A	A
Name	None [7:2]						COMP1	COMP0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	COMP1	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	COMP0	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

19.1.5 LPCOMP_INTR_MASK

LPCOMP Interrupt request mask

Address: 0x40350018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						COMP1_MASK	COMP0_MASK

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	COMP1_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	COMP0_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0

19.1.6 LPCOMP_INTR_MASKED

LPCOMP Interrupt request masked

Address: 0x4035001C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						W	W
Name	None [7:2]						COMP1_MASKED	COMP0_MASKED

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	COMP1_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
0	COMP0_MASKED	Logical and of corresponding request and mask bits. Default Value: 0

19.1.7 LPCOMP_CMP0_CTRL

Comparator 0 control Register

Address: 0x40350040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW	None			RW	
HW Access	R		R	None			R	
Name	INTTYPE0 [7:6]		HYST0	None [4:2]			MODE0 [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	RW	None	
HW Access	None				R	R	None	
Name	None [15:12]				DSI_LEV-EL0	DSI_BY-PASS0	None [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	DSI_LEVEL0	Synchronous comparator output (trigger): 0=pulse 1=level Default Value: 0
10	DSI_BYPASS0	Asynchronous: bypass comparator output synchronization: 0=synchronize (level or pulse) 1=bypass (output async) Note that in System Deep Sleep mode, this bit needs to be set to observe the output on the ded-icated pin. Default Value: 0
7 : 6	INTTYPE0	Sets which edge will trigger an IRQ Default Value: 0 **0x0: DISABLE :** Disabled, no interrupts will be detected

19.1.7 LPCOMP_CMP0_CTRL (continued)

		0x1: RISING : Rising edge **0x2: FALLING :** Falling edge **0x3: BOTH :** Both rising and falling edges
5	HYST0	Add hysteresis to the comparator 0= Disable Hysteresis 1= Enable Hysteresis Default Value: 0
1 : 0	MODE0	Operating mode for the comparator Default Value: 0 **0x0: OFF :** Off **0x1: ULP :** Ultra low power operating mode. This mode must be used for System Deep Sleep and System Hibernate operation. In this mode, local Ibias is used. **0x2: LP :** Low Power operating mode. In this mode, IREF from SRSS is used. **0x3: NORMAL :** Normal power, full speed operating mode. In this mode, IREF from SRSS is used.

19.1.8 LPCOMP_CMP0_SW

Comparator 0 switch control

Address: 0x40350050

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	RW1S	None	RW1S	RW1S	RW1S
HW Access	RW1C	RW1C	RW1C	RW1C	None	RW1C	RW1C	RW1C
Name	CMP0_VN0	CMP0_BN0	CMP0_AN0	CMP0_IN0	None	CMP0_BP0	CMP0_AP0	CMP0_IP0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	CMP0_VN0	Comparator 0 negative terminal switch to local Vref (LPREF_EN must be set) Default Value: 0
6	CMP0_BN0	Comparator 0 negative terminal switch to amuxbusB Default Value: 0
5	CMP0_AN0	Comparator 0 negative terminal switch to amuxbusA Default Value: 0
4	CMP0_IN0	Comparator 0 negative terminal isolation switch to GPIO Default Value: 0
2	CMP0_BP0	Comparator 0 positive terminal switch to amuxbusB Default Value: 0
1	CMP0_AP0	Comparator 0 positive terminal switch to amuxbusA Default Value: 0
0	CMP0_IP0	Comparator 0 positive terminal isolation switch to GPIO Default Value: 0

19.1.9 LPCOMP_CMP0_SW_CLEAR

Comparator 0 switch control clear

Address: 0x40350054

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	None	RW1C	RW1C	RW1C
HW Access	A	A	A	A	None	A	A	A
Name	CMP0_VN0	CMP0_BN0	CMP0_AN0	CMP0_IN0	None	CMP0_BP0	CMP0_AP0	CMP0_IP0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	CMP0_VN0	see corresponding bit in CMP0_SW Default Value: 0
6	CMP0_BN0	see corresponding bit in CMP0_SW Default Value: 0
5	CMP0_AN0	see corresponding bit in CMP0_SW Default Value: 0
4	CMP0_IN0	see corresponding bit in CMP0_SW Default Value: 0
2	CMP0_BP0	see corresponding bit in CMP0_SW Default Value: 0
1	CMP0_AP0	see corresponding bit in CMP0_SW Default Value: 0
0	CMP0_IP0	see corresponding bit in CMP0_SW Default Value: 0

19.1.10 LPCOMP_CMP1_CTRL

Comparator 1 control Register

Address: 0x40350080

Retention: Retained

Bits	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SW Access	RW		RW	None			RW	
HW Access	R		R	None			R	
Name	INTTYPE1 [7:6]		HYST1	None [4:2]			MODE1 [1:0]	

Bits	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SW Access	None				RW	RW	None	
HW Access	None				R	R	None	
Name	None [15:12]				DSI_LEV-EL1	DSI_BY-PASS1	None [9:8]	

Bits	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	**Name**	**Description**
11	DSI_LEVEL1	Synchronous comparator output (trigger): 0=pulse 1=level Default Value: 0
10	DSI_BYPASS1	Asynchronous: bypass comparator output synchronization: 0=synchronize (level or pulse) 1=bypass (output async) Note that in System Deep Sleep mode, this bit needs to be set to observe the output on the dedicated pin. Default Value: 0
7 : 6	INTTYPE1	Sets which edge will trigger an IRQ Default Value: 0 **0x0: DISABLE :** Disabled, no interrupts will be detected

19.1.10 LPCOMP_CMP1_CTRL (continued)

		0x1: RISING : Rising edge **0x2: FALLING :** Falling edge **0x3: BOTH :** Both rising and falling edges
5	HYST1	Add hysteresis to the comparator 0= Disable Hysteresis 1= Enable Hysteresis Default Value: 0
1 : 0	MODE1	Operating mode for the comparator Default Value: 0 **0x0: OFF :** Off **0x1: ULP :** Ultra low power operating mode. This mode must be used for System Deep Sleep and System Hibernate operation. In this mode, local Ibias is used. **0x2: LP :** Low Power operating mode. In this mode, IREF from SRSS is used. **0x3: NORMAL :** Normal power, full speed operating mode. In this mode, IREF from SRSS is used.

19.1.11 LPCOMP_CMP1_SW

Comparator 1 switch control

Address: 0x40350090

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	RW1S	None	RW1S	RW1S	RW1S
HW Access	RW1C	RW1C	RW1C	RW1C	None	RW1C	RW1C	RW1C
Name	CMP1_VN1	CMP1_BN1	CMP1_AN1	CMP1_IN1	None	CMP1_BP1	CMP1_AP1	CMP1_IP1

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	CMP1_VN1	Comparator 1 negative terminal switch to local Vref (LPREF_EN must be set) Default Value: 0
6	CMP1_BN1	Comparator 1 negative terminal switch to amuxbusB Default Value: 0
5	CMP1_AN1	Comparator 1 negative terminal switch to amuxbusA Default Value: 0
4	CMP1_IN1	Comparator 1 negative terminal isolation switch to GPIO Default Value: 0
2	CMP1_BP1	Comparator 1 positive terminal switch to amuxbusB Default Value: 0
1	CMP1_AP1	Comparator 1 positive terminal switch to amuxbusA Default Value: 0
0	CMP1_IP1	Comparator 1 positive terminal isolation switch to GPIO Default Value: 0

19.1.12 LPCOMP_CMP1_SW_CLEAR

Comparator 1 switch control clear

Address: 0x40350094

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	None	RW1C	RW1C	RW1C
HW Access	A	A	A	A	None	A	A	A
Name	CMP1_VN1	CMP1_BN1	CMP1_AN1	CMP1_IN1	None	CMP1_BP1	CMP1_AP1	CMP1_IP1

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	CMP1_VN1	see corresponding bit in CMP1_SW Default Value: 0
6	CMP1_BN1	see corresponding bit in CMP1_SW Default Value: 0
5	CMP1_AN1	see corresponding bit in CMP1_SW Default Value: 0
4	CMP1_IN1	see corresponding bit in CMP1_SW Default Value: 0
2	CMP1_BP1	see corresponding bit in CMP1_SW Default Value: 0
1	CMP1_AP1	see corresponding bit in CMP1_SW Default Value: 0
0	CMP1_IP1	see corresponding bit in CMP1_SW Default Value: 0

20 Timer, Counter, PWM (TCPWM) Registers

This section discusses the Timer, Counter, PWM (TCPWM) registers. It lists all the registers in mapping tables, in address order.

20.1 Register Details

Register	Address	Description
TCPWM0_CTRL	0x40380000	TCPWM control register
TCPWM0_CTRL_CLR	0x40380004	TCPWM control clear register
TCPWM0_CTRL_SET	0x40380008	TCPWM control set register
TCPWM0_CMD_CAPTURE	0x4038000C	TCPWM capture command register
TCPWM0_CMD_RELOAD	0x40380010	TCPWM reload command register
TCPWM0_CMD_STOP	0x40380014	TCPWM stop command register
TCPWM0_CMD_START	0x40380018	TCPWM start command register
TCPWM0_INTR_CAUSE	0x4038001C	TCPWM Counter interrupt cause register
TCPWM0_CNT0_CTRL	0x40380100	Counter control register
TCPWM0_CNT0_STATUS	0x40380104	Counter status register
TCPWM0_CNT0_COUNTER	0x40380108	Counter count register
TCPWM0_CNT0_CC	0x4038010C	Counter compare/capture register
TCPWM0_CNT0_CC_BUFF	0x40380110	Counter buffered compare/capture register
TCPWM0_CNT0_PERIOD	0x40380114	Counter period register
TCPWM0_CNT0_PERIOD_BUFF	0x40380118	Counter buffered period register
TCPWM0_CNT0_TR_CTRL0	0x40380120	Counter trigger control register 0
TCPWM0_CNT0_TR_CTRL1	0x40380124	Counter trigger control register 1
TCPWM0_CNT0_TR_CTRL2	0x40380128	Counter trigger control register 2
TCPWM0_CNT0_INTR	0x40380130	Interrupt request register
TCPWM0_CNT0_INTR_SET	0x40380134	Interrupt set request register
TCPWM0_CNT0_INTR_MASK	0x40380138	Interrupt mask register
TCPWM0_CNT0_INTR_MASKED	0x4038013C	Interrupt masked request register
TCPWM0_CNT1_CTRL	0x40380140	Counter control register. See TCPWM0_CNT0_CTRL for the details of bit fields.
TCPWM0_CNT1_STATUS	0x40380144	Counter status register. See TCPWM0_CNT0_STATUS for the details of bit fields.
TCPWM0_CNT1_COUNTER	0x40380148	Counter count register. See TCPWM0_CNT0_COUNTER for the details of bit fields.
TCPWM0_CNT1_CC	0x4038014C	Counter compare/capture register. See TCPWM0_CNT0_CCfor the details of bit fields.
TCPWM0_CNT1_CC_BUFF	0x40380150	Counter buffered compare/capture register. See TCPWM0_CNT0_CC_BUFFfor the details of bit fields.

Register	Address	Description
TCPWM0_CNT1_PERIOD	0x40380154	Counter period register. See TCPWM0_CNT0_PERIODfor the details of bit fields.
TCPWM0_CNT1_PERIOD_BUFF	0x40380158	Counter buffered period register. See TCPWM0_CNT0_PERIOD_BUFFfor the details of bit fields.
TCPWM0_CNT1_TR_CTRL0	0x40380160	Counter trigger control register 0. See TCPWM0_CNT0_TR_CTRL0 for the details of bit fields.
TCPWM0_CNT1_TR_CTRL1	0x40380164	Counter trigger control register 1. See TCPWM0_CNT0_TR_CTRL1 for the details of bit fields.
TCPWM0_CNT1_TR_CTRL2	0x40380168	Counter trigger control register 2. See TCPWM0_CNT0_TR_CTRL2 for the details of bit fields.
TCPWM0_CNT1_INTR	0x40380170	Interrupt request register. See TCPWM0_CNT0_INTRfor the details of bit fields.
TCPWM0_CNT1_INTR_SET	0x40380174	Interrupt set request register. See TCPWM0_CNT0_INTR_SETfor the details of bit fields.
TCPWM0_CNT1_INTR_MASK	0x40380178	Interrupt mask register. See TCPWM0_CNT0_INTR_MASKfor the details of bit fields.
TCPWM0_CNT1_INTR_MASKED	0x4038017C	Interrupt masked request register. See TCPWM0_CNT0_INTR_MASKED for the details of bit fields.
TCPWM0_CNT2_CTRL	0x40380180	Counter control register. See TCPWM0_CNT0_CTRL for the details of bit fields.
TCPWM0_CNT2_STATUS	0x40380184	Counter status register. See TCPWM0_CNT0_STATUS for the details of bit fields.
TCPWM0_CNT2_COUNTER	0x40380188	Counter count register. See TCPWM0_CNT0_COUNTER for the details of bit fields.
TCPWM0_CNT2_CC	0x4038018C	Counter compare/capture register. See TCPWM0_CNT0_CC for the details of bit fields.
TCPWM0_CNT2_CC_BUFF	0x40380190	Counter buffered compare/capture register. See TCPWM0_CNT0_CC_BUFFfor the details of bit fields.
TCPWM0_CNT2_PERIOD	0x40380194	Counter period register. See TCPWM0_CNT0_PERIOD for the details of bit fields.
TCPWM0_CNT2_PERIOD_BUF F	0x40380198	Counter buffered period register. See TCPWM0_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM0_CNT2_TR_CTRL0	0x403801A0	Counter trigger control register 0. See TCPWM0_CNT0_TR_CTRL0 for the details of bit fields.
TCPWM0_CNT2_TR_CTRL1	0x403801A4	Counter trigger control register 1. See TCPWM0_CNT0_TR_CTRL1 for the details of bit fields.
TCPWM0_CNT2_TR_CTRL2	0x403801A8	Counter trigger control register 2. See TCPWM0_CNT0_TR_CTRL2 for the details of bit fields.
TCPWM0_CNT2_INTR	0x403801B0	Interrupt request register. See TCPWM0_CNT0_INTR for the details of bit fields.
TCPWM0_CNT2_INTR_SET	0x403801B4	Interrupt set request register. See TCPWM0_CNT0_INTR_SETfor the details of bit fields.
TCPWM0_CNT2_INTR_MASK	0x403801B8	Interrupt mask register. See TCPWM0_CNT0_INTR_MASK for the details of bit fields.
TCPWM0_CNT2_INTR_MASKED	0x403801BC	Interrupt masked request register. See TCPWM0_CNT0_INTR_MASKEDfor the details of bit fields.
TCPWM0_CNT3_CTRL	0x403801C0	Counter control register. See TCPWM0_CNT0_CTRL for the details of bit fields.
TCPWM0_CNT3_STATUS	0x403801C4	Counter status register. See TCPWM0_CNT0_STATUS for the details of bit fields.
TCPWM0_CNT3_COUNTER	0x403801C8	Counter count register. See TCPWM0_CNT0_COUNTER for the details of bit fields.
TCPWM0_CNT3_CC	0x403801CC	Counter compare/capture register. See TCPWM0_CNT0_CCfor the details of bit fields.
TCPWM0_CNT3_CC_BUFF	0x403801D0	Counter buffered compare/capture register. See TCPWM0_CNT0_CC_BUFFfor the details of bit fields.
TCPWM0_CNT3_PERIOD	0x403801D4	Counter period register. See TCPWM0_CNT0_PERIODfor the details of bit fields.

Register	Address	Description
TCPWM0_CNT3_PERIOD_BUFF	0x403801D8	Counter buffered period register. See TCPWM0_CNT0_PERIOD_BUFFfor the details of bit fields.
TCPWM0_CNT3_TR_CTRL0	0x403801E0	Counter trigger control register 0. See TCPWM0_CNT0_TR_CTRL0 for the details of bit fields.
TCPWM0_CNT3_TR_CTRL1	0x403801E4	Counter trigger control register 1. See TCPWM0_CNT0_TR_CTRL1 for the details of bit fields.
TCPWM0_CNT3_TR_CTRL2	0x403801E8	Counter trigger control register 2. See TCPWM0_CNT0_TR_CTRL2 for the details of bit fields.
TCPWM0_CNT3_INTR	0x403801F0	Interrupt request register. See TCPWM0_CNT0_INTRfor the details of bit fields.
TCPWM0_CNT3_INTR_SET	0x403801F4	Interrupt set request register. See TCPWM0_CNT0_INTR_SETfor the details of bit fields.
TCPWM0_CNT3_INTR_MASK	0x403801F8	Interrupt mask register. See TCPWM0_CNT0_INTR_MASKfor the details of bit fields.
TCPWM0_CNT3_INTR_MASKED	0x403801FC	Interrupt masked request register. See TCPWM0_CNT0_INTR_MASKEDfor the details of bit fields.
TCPWM0_CNT4_CTRL	0x40380200	Counter control register. See TCPWM0_CNT0_CTRL for the details of bit fields.
TCPWM0_CNT4_STATUS	0x40380204	Counter status register. See TCPWM0_CNT0_STATUS for the details of bit fields.
TCPWM0_CNT4_COUNTER	0x40380208	Counter count register. See TCPWM0_CNT0_COUNTER for the details of bit fields.
TCPWM0_CNT4_CC	0x4038020C	Counter compare/capture register. See TCPWM0_CNT0_CCfor the details of bit fields.
TCPWM0_CNT4_CC_BUFF	0x40380210	Counter buffered compare/capture register. See TCPWM0_CNT0_CC_BUFFfor the details of bit fields.
TCPWM0_CNT4_PERIOD	0x40380214	Counter period register. See TCPWM0_CNT0_PERIODfor the details of bit fields.
TCPWM0_CNT4_PERIOD_BUFF	0x40380218	Counter buffered period register. See TCPWM0_CNT0_PERIOD_BUFFfor the details of bit fields.
TCPWM0_CNT4_TR_CTRL0	0x40380220	Counter trigger control register 0. See TCPWM0_CNT0_TR_CTRL0 for the details of bit fields.
TCPWM0_CNT4_TR_CTRL1	0x40380224	Counter trigger control register 1. See TCPWM0_CNT0_TR_CTRL1 for the details of bit fields.
TCPWM0_CNT4_TR_CTRL2	0x40380228	Counter trigger control register 2. See TCPWM0_CNT0_TR_CTRL2 for the details of bit fields.
TCPWM0_CNT4_INTR	0x40380230	Interrupt request register. See TCPWM0_CNT0_INTRfor the details of bit fields.
TCPWM0_CNT4_INTR_SET	0x40380234	Interrupt set request register. See TCPWM0_CNT0_INTR_SETfor the details of bit fields.
TCPWM0_CNT4_INTR_MASK	0x40380238	Interrupt mask register. See TCPWM0_CNT0_INTR_MASKfor the details of bit fields.
TCPWM0_CNT4_INTR_MASKED	0x4038023C	Interrupt masked request register. See TCPWM0_CNT0_INTR_MASKEDfor the details of bit fields.
TCPWM0_CNT5_CTRL	0x40380240	Counter control register. See TCPWM0_CNT0_CTRL for the details of bit fields.
TCPWM0_CNT5_STATUS	0x40380244	Counter status register. See TCPWM0_CNT0_STATUS for the details of bit fields.
TCPWM0_CNT5_COUNTER	0x40380248	Counter count register. See TCPWM0_CNT0_COUNTER for the details of bit fields.
TCPWM0_CNT5_CC	0x4038024C	Counter compare/capture register. See TCPWM0_CNT0_CCfor the details of bit fields.
TCPWM0_CNT5_CC_BUFF	0x40380250	Counter buffered compare/capture register. See TCPWM0_CNT0_CC_BUFFfor the details of bit fields.
TCPWM0_CNT5_PERIOD	0x40380254	Counter period register. See TCPWM0_CNT0_PERIODfor the details of bit fields.
TCPWM0_CNT5_PERIOD_BUFF	0x40380258	Counter buffered period register. See TCPWM0_CNT0_PERIOD_BUFFfor the details of bit fields.

Register	Address	Description
TCPWM0_CNT5_TR_CTRL0	0x40380260	Counter trigger control register 0. See TCPWM0_CNT0_TR_CTRL0 for the details of bit fields.
TCPWM0_CNT5_TR_CTRL1	0x40380264	Counter trigger control register 1. See TCPWM0_CNT0_TR_CTRL1 for the details of bit fields.
TCPWM0_CNT5_TR_CTRL2	0x40380268	Counter trigger control register 2. See TCPWM0_CNT0_TR_CTRL2 for the details of bit fields.
TCPWM0_CNT5_INTR	0x40380270	Interrupt request register. See TCPWM0_CNT0_INTRfor the details of bit fields.
TCPWM0_CNT5_INTR_SET	0x40380274	Interrupt set request register. See TCPWM0_CNT0_INTR_SETfor the details of bit fields.
TCPWM0_CNT5_INTR_MASK	0x40380278	Interrupt mask register. See TCPWM0_CNT0_INTR_MASKfor the details of bit fields.
TCPWM0_CNT5_INTR_MASKED	0x4038027C	Interrupt masked request register. See TCPWM0_CNT0_INTR_MASKEDfor the details of bit fields.
TCPWM0_CNT6_CTRL	0x40380280	Counter control register. See TCPWM0_CNT0_CTRL for the details of bit fields.
TCPWM0_CNT6_STATUS	0x40380284	Counter status register. See TCPWM0_CNT0_STATUS for the details of bit fields.
TCPWM0_CNT6_COUNTER	0x40380288	Counter count register. See TCPWM0_CNT0_COUNTER for the details of bit fields.
TCPWM0_CNT6_CC	0x4038028C	Counter compare/capture register. See TCPWM0_CNT0_CCfor the details of bit fields.
TCPWM0_CNT6_CC_BUFF	0x40380290	Counter buffered compare/capture register. See TCPWM0_CNT0_CC_BUFFfor the details of bit fields.
TCPWM0_CNT6_PERIOD	0x40380294	Counter period register. See TCPWM0_CNT0_PERIODfor the details of bit fields.
TCPWM0_CNT6_PERIOD_BUFF	0x40380298	Counter buffered period register. See TCPWM0_CNT0_PERIOD_BUFFfor the details of bit fields.
TCPWM0_CNT6_TR_CTRL0	0x403802A0	Counter trigger control register 0. See TCPWM0_CNT0_TR_CTRL0 for the details of bit fields.
TCPWM0_CNT6_TR_CTRL1	0x403802A4	Counter trigger control register 1. See TCPWM0_CNT0_TR_CTRL1 for the details of bit fields.
TCPWM0_CNT6_TR_CTRL2	0x403802A8	Counter trigger control register 2. See TCPWM0_CNT0_TR_CTRL2 for the details of bit fields.
TCPWM0_CNT6_INTR	0x403802B0	Interrupt request register. See TCPWM0_CNT0_INTRfor the details of bit fields.
TCPWM0_CNT6_INTR_SET	0x403802B4	Interrupt set request register. See TCPWM0_CNT0_INTR_SETfor the details of bit fields.
TCPWM0_CNT6_INTR_MASK	0x403802B8	Interrupt mask register. See TCPWM0_CNT0_INTR_MASKfor the details of bit fields.
TCPWM0_CNT6_INTR_MASKED	0x403802BC	Interrupt masked request register. See TCPWM0_CNT0_INTR_MASKEDfor the details of bit fields.
TCPWM0_CNT7_CTRL	0x403802C0	Counter control register. See TCPWM0_CNT0_CTRL for the details of bit fields.
TCPWM0_CNT7_STATUS	0x403802C4	Counter status register. See TCPWM0_CNT0_STATUS for the details of bit fields.
TCPWM0_CNT7_COUNTER	0x403802C8	Counter count register. See TCPWM0_CNT0_COUNTER for the details of bit fields.
TCPWM0_CNT7_CC	0x403802CC	Counter compare/capture register. See TCPWM0_CNT0_CCfor the details of bit fields.
TCPWM0_CNT7_CC_BUFF	0x403802D0	Counter buffered compare/capture register. See TCPWM0_CNT0_CC_BUFFfor the details of bit fields.
TCPWM0_CNT7_PERIOD	0x403802D4	Counter period register. See TCPWM0_CNT0_PERIODfor the details of bit fields.
TCPWM0_CNT7_PERIOD_BUFF	0x403802D8	Counter buffered period register. See TCPWM0_CNT0_PERIOD_BUFFfor the details of bit fields.
TCPWM0_CNT7_TR_CTRL0	0x403802E0	Counter trigger control register 0. See TCPWM0_CNT0_TR_CTRL0 for the details of bit fields.

Register	Address	Description
TCPWM0_CNT7_TR_CTRL1	0x403802E4	Counter trigger control register 1. See TCPWM0_CNT0_TR_CTRL1 for the details of bit fields.
TCPWM0_CNT7_TR_CTRL2	0x403802E8	Counter trigger control register 2. See TCPWM0_CNT0_TR_CTRL2 for the details of bit fields.
TCPWM0_CNT7_INTR	0x403802F0	Interrupt request register. See TCPWM0_CNT0_INTRfor the details of bit fields.
TCPWM0_CNT7_INTR_SET	0x403802F4	Interrupt set request register. See TCPWM0_CNT0_INTR_SETfor the details of bit fields.
TCPWM0_CNT7_INTR_MASK	0x403802F8	Interrupt mask register. See TCPWM0_CNT0_INTR_MASKfor the details of bit fields.
TCPWM0_CNT7_INTR_MASKED	0x403802FC	Interrupt masked request register. See TCPWM0_CNT0_INTR_MASKED for the details of bit fields.
TCPWM1_CTRL	0x40390000	TCPWM control register
TCPWM1_CTRL_CLR	0x40390004	TCPWM control clear register
TCPWM1_CTRL_SET	0x40390008	TCPWM control set register
TCPWM1_CMD_CAPTURE	0x4039000C	TCPWM capture command register
TCPWM1_CMD_RELOAD	0x40390010	TCPWM reload command register
TCPWM1_CMD_STOP	0x40390014	TCPWM stop command register
TCPWM1_CMD_START	0x40390018	TCPWM start command register
TCPWM1_INTR_CAUSE	0x4039001C	TCPWM Counter interrupt cause register
TCPWM1_CNT0_CTRL	0x40390100	Counter control register. See TCPWM0_CNT0_CTRL for the details of bit fields.
TCPWM1_CNT0_STATUS	0x40390104	Counter status register. See TCPWM0_CNT0_STATUS for the details of bit fields.
TCPWM1_CNT0_COUNTER	0x40390108	Counter count register
TCPWM1_CNT0_CC	0x4039010C	Counter compare/capture register
TCPWM1_CNT0_CC_BUFF	0x40390110	Counter buffered compare/capture register
TCPWM1_CNT0_PERIOD	0x40390114	Counter period register
TCPWM1_CNT0_PERIOD_BUFF	0x40390118	Counter buffered period register
TCPWM1_CNT0_TR_CTRL0	0x40390120	Counter trigger control register 0. See TCPWM0_CNT0_TR_CTRL0 for the details of bit fields.
TCPWM1_CNT0_TR_CTRL1	0x40390124	Counter trigger control register 1. See TCPWM0_CNT0_TR_CTRL1 for the details of bit fields.
TCPWM1_CNT0_TR_CTRL2	0x40390128	Counter trigger control register 2. See TCPWM0_CNT0_TR_CTRL2 for the details of bit fields.
TCPWM1_CNT0_INTR	0x40390130	Interrupt request register. See TCPWM0_CNT0_INTRfor the details of bit fields.
TCPWM1_CNT0_INTR_SET	0x40390134	Interrupt set request register. See TCPWM0_CNT0_INTR_SETfor the details of bit fields.
TCPWM1_CNT0_INTR_MASK	0x40390138	Interrupt mask register. See TCPWM0_CNT0_INTR_MASKfor the details of bit fields.
TCPWM1_CNT0_INTR_MASKED	0x4039013C	Interrupt masked request register. See TCPWM0_CNT0_INTR_MASKEDfor the details of bit fields.
TCPWM1_CNT1_CTRL	0x40390140	Counter control register. See TCPWM0_CNT0_CTRL for the details of bit fields.

Register	Address	Description
TCPWM1_CNT1_STATUS	0x40390144	Counter status register. See TCPWM0_CNT0_STATUS for the details of bit fields.
TCPWM1_CNT1_COUNTER	0x40390148	Counter count register. See TCPWM1_CNT0_COUNTER for the details of bit fields.
TCPWM1_CNT1_CC	0x4039014C	Counter compare/capture register. See TCPWM1_CNT0_CCfor the details of bit fields.
TCPWM1_CNT1_CC_BUFF	0x40390150	Counter buffered compare/capture register. See TCPWM1_CNT0_CC_BUFFfor the details of bit fields.
TCPWM1_CNT1_PERIOD	0x40390154	Counter period register. See TCPWM1_CNT0_PERIODfor the details of bit fields.
TCPWM1_CNT1_PERIOD_BUFF	0x40390158	Counter buffered period register. See TCPWM1_CNT0_PERIOD_BUFFfor the details of bit fields.
TCPWM1_CNT1_TR_CTRL0	0x40390160	Counter trigger control register 0. See TCPWM0_CNT0_TR_CTRL0 for the details of bit fields.
TCPWM1_CNT1_TR_CTRL1	0x40390164	Counter trigger control register 1. See TCPWM0_CNT0_TR_CTRL1 for the details of bit fields.
TCPWM1_CNT1_TR_CTRL2	0x40390168	Counter trigger control register 2. See TCPWM0_CNT0_TR_CTRL2 for the details of bit fields.
TCPWM1_CNT1_INTR	0x40390170	Interrupt request register. See TCPWM0_CNT0_INTRfor the details of bit fields.
TCPWM1_CNT1_INTR_SET	0x40390174	Interrupt set request register. See TCPWM0_CNT0_INTR_SETfor the details of bit fields.
TCPWM1_CNT1_INTR_MASK	0x40390178	Interrupt mask register. See TCPWM0_CNT0_INTR_MASKfor the details of bit fields.
TCPWM1_CNT1_INTR_MASKED	0x4039017C	Interrupt masked request register. See TCPWM0_CNT0_INTR_MASKED for the details of bit fields.
TCPWM1_CNT2_CTRL	0x40390180	Counter control register. See TCPWM0_CNT0_CTRL for the details of bit fields.
TCPWM1_CNT2_STATUS	0x40390184	Counter status register. See TCPWM0_CNT0_STATUS for the details of bit fields.
TCPWM1_CNT2_COUNTER	0x40390188	Counter count register. See TCPWM1_CNT0_COUNTER for the details of bit fields.
TCPWM1_CNT2_CC	0x4039018C	Counter compare/capture register. See TCPWM1_CNT0_CCfor the details of bit fields.
TCPWM1_CNT2_CC_BUFF	0x40390190	Counter buffered compare/capture register. See TCPWM1_CNT0_CC_BUFFfor the details of bit fields.
TCPWM1_CNT2_PERIOD	0x40390194	Counter period register. See TCPWM1_CNT0_PERIODfor the details of bit fields.
TCPWM1_CNT2_PERIOD_BUFF	0x40390198	Counter buffered period register. See TCPWM1_CNT0_PERIOD_BUFFfor the details of bit fields.
TCPWM1_CNT2_TR_CTRL0	0x403901A0	Counter trigger control register 0. See TCPWM0_CNT0_TR_CTRL0 for the details of bit fields.
TCPWM1_CNT2_TR_CTRL1	0x403901A4	Counter trigger control register 1. See TCPWM0_CNT0_TR_CTRL1 for the details of bit fields.
TCPWM1_CNT2_TR_CTRL2	0x403901A8	Counter trigger control register 2. See TCPWM0_CNT0_TR_CTRL2 for the details of bit fields.
TCPWM1_CNT2_INTR	0x403901B0	Interrupt request register. See TCPWM0_CNT0_INTR for the details of bit fields.
TCPWM1_CNT2_INTR_SET	0x403901B4	Interrupt set request register. See TCPWM0_CNT0_INTR_SET for the details of bit fields.
TCPWM1_CNT2_INTR_MASK	0x403901B8	Interrupt mask register. See TCPWM0_CNT0_INTR_MASK for the details of bit fields.
TCPWM1_CNT2_INTR_MASKED	0x403901BC	Interrupt masked request register. See TCPWM0_CNT0_INTR_MASKEDfor the details of bit fields.
TCPWM1_CNT3_CTRL	0x403901C0	Counter control register. See TCPWM0_CNT0_CTRL for the details of bit fields.
TCPWM1_CNT3_STATUS	0x403901C4	Counter status register. See TCPWM0_CNT0_STATUS for the details of bit fields.

Register	Address	Description
TCPWM1_CNT3_COUNTER	0x403901C8	Counter count register. See TCPWM1_CNT0_COUNTER for the details of bit fields.
TCPWM1_CNT3_CC	0x403901CC	Counter compare/capture register. See TCPWM1_CNT0_CCfor the details of bit fields.
TCPWM1_CNT3_CC_BUFF	0x403901D0	Counter buffered compare/capture register. See TCPWM1_CNT0_CC_BUFFfor the details of bit fields.
TCPWM1_CNT3_PERIOD	0x403901D4	Counter period register. See TCPWM1_CNT0_PERIODfor the details of bit fields.
TCPWM1_CNT3_PERIOD_BUFF	0x403901D8	Counter buffered period register. See TCPWM1_CNT0_PERIOD_BUFFfor the details of bit fields.
TCPWM1_CNT3_TR_CTRL0	0x403901E0	Counter trigger control register 0. See TCPWM0_CNT0_TR_CTRL0 for the details of bit fields.
TCPWM1_CNT3_TR_CTRL1	0x403901E4	Counter trigger control register 1. See TCPWM0_CNT0_TR_CTRL1 for the details of bit fields.
TCPWM1_CNT3_TR_CTRL2	0x403901E8	Counter trigger control register 2. See TCPWM0_CNT0_TR_CTRL2 for the details of bit fields.
TCPWM1_CNT3_INTR	0x403901F0	Interrupt request register. See TCPWM0_CNT0_INTRfor the details of bit fields.
TCPWM1_CNT3_INTR_SET	0x403901F4	Interrupt set request register. See TCPWM0_CNT0_INTR_SETfor the details of bit fields.
TCPWM1_CNT3_INTR_MASK	0x403901F8	Interrupt mask register. See TCPWM0_CNT0_INTR_MASKfor the details of bit fields.
TCPWM1_CNT3_INTR_MASKED	0x403901FC	Interrupt masked request register. See TCPWM0_CNT0_INTR_MASKED for the details of bit fields.
TCPWM1_CNT4_CTRL	0x40390200	Counter control register. See TCPWM0_CNT0_CTRL for the details of bit fields.
TCPWM1_CNT4_STATUS	0x40390204	Counter status register. See TCPWM0_CNT0_STATUS for the details of bit fields.
TCPWM1_CNT4_COUNTER	0x40390208	Counter count register. See TCPWM1_CNT0_COUNTER for the details of bit fields.
TCPWM1_CNT4_CC	0x4039020C	Counter compare/capture register. See TCPWM1_CNT0_CCfor the details of bit fields.
TCPWM1_CNT4_CC_BUFF	0x40390210	Counter buffered compare/capture register. See TCPWM1_CNT0_CC_BUFFfor the details of bit fields.
TCPWM1_CNT4_PERIOD	0x40390214	Counter period register. See TCPWM1_CNT0_PERIODfor the details of bit fields.
TCPWM1_CNT4_PERIOD_BUFF	0x40390218	Counter buffered period register. See TCPWM1_CNT0_PERIOD_BUFFfor the details of bit fields.
TCPWM1_CNT4_TR_CTRL0	0x40390220	Counter trigger control register 0. See TCPWM0_CNT0_TR_CTRL0 for the details of bit fields.
TCPWM1_CNT4_TR_CTRL1	0x40390224	Counter trigger control register 1. See TCPWM0_CNT0_TR_CTRL1 for the details of bit fields.
TCPWM1_CNT4_TR_CTRL2	0x40390228	Counter trigger control register 2. See TCPWM0_CNT0_TR_CTRL2 for the details of bit fields.
TCPWM1_CNT4_INTR	0x40390230	Interrupt request register. See TCPWM0_CNT0_INTRfor the details of bit fields.
TCPWM1_CNT4_INTR_SET	0x40390234	Interrupt set request register. See TCPWM0_CNT0_INTR_SETfor the details of bit fields.
TCPWM1_CNT4_INTR_MASK	0x40390238	Interrupt mask register. See TCPWM0_CNT0_INTR_MASKfor the details of bit fields.
TCPWM1_CNT4_INTR_MASKED	0x4039023C	Interrupt masked request register. See TCPWM0_CNT0_INTR_MASKEDfor the details of bit fields.
TCPWM1_CNT5_CTRL	0x40390240	Counter control register. See TCPWM0_CNT0_CTRL for the details of bit fields.
TCPWM1_CNT5_STATUS	0x40390244	Counter status register. See TCPWM0_CNT0_STATUS for the details of bit fields.
TCPWM1_CNT5_COUNTER	0x40390248	Counter count register. See TCPWM1_CNT0_COUNTER for the details of bit fields.

Register	Address	Description
TCPWM1_CNT5_CC	0x4039024C	Counter compare/capture register. See TCPWM1_CNT0_CCfor the details of bit fields.
TCPWM1_CNT5_CC_BUFF	0x40390250	Counter buffered compare/capture register. See TCPWM1_CNT0_CC_BUFFfor the details of bit fields.
TCPWM1_CNT5_PERIOD	0x40390254	Counter period register. See TCPWM1_CNT0_PERIODfor the details of bit fields.
TCPWM1_CNT5_PERIOD_BUFF	0x40390258	Counter buffered period register. See TCPWM1_CNT0_PERIOD_BUFFfor the details of bit fields.
TCPWM1_CNT5_TR_CTRL0	0x40390260	Counter trigger control register 0. See TCPWM0_CNT0_TR_CTRL0 for the details of bit fields.
TCPWM1_CNT5_TR_CTRL1	0x40390264	Counter trigger control register 1. See TCPWM0_CNT0_TR_CTRL1 for the details of bit fields.
TCPWM1_CNT5_TR_CTRL2	0x40390268	Counter trigger control register 2. See TCPWM0_CNT0_TR_CTRL2 for the details of bit fields.
TCPWM1_CNT5_INTR	0x40390270	Interrupt request register. See TCPWM0_CNT0_INTRfor the details of bit fields.
TCPWM1_CNT5_INTR_SET	0x40390274	Interrupt set request register. See TCPWM0_CNT0_INTR_SETfor the details of bit fields.
TCPWM1_CNT5_INTR_MASK	0x40390278	Interrupt mask register. See TCPWM0_CNT0_INTR_MASKfor the details of bit fields.
TCPWM1_CNT5_INTR_MASKED	0x4039027C	Interrupt masked request register. See TCPWM0_CNT0_INTR_MASKEDfor the details of bit fields.
TCPWM1_CNT6_CTRL	0x40390280	Counter control register. See TCPWM0_CNT0_CTRL for the details of bit fields.
TCPWM1_CNT6_STATUS	0x40390284	Counter status register. See TCPWM0_CNT0_STATUS for the details of bit fields.
TCPWM1_CNT6_COUNTER	0x40390288	Counter count register. See TCPWM1_CNT0_COUNTER for the details of bit fields.
TCPWM1_CNT6_CC	0x4039028C	Counter compare/capture register. See TCPWM1_CNT0_CCfor the details of bit fields.
TCPWM1_CNT6_CC_BUFF	0x40390290	Counter buffered compare/capture register. See TCPWM1_CNT0_CC_BUFFfor the details of bit fields.
TCPWM1_CNT6_PERIOD	0x40390294	Counter period register. See TCPWM1_CNT0_PERIODfor the details of bit fields.
TCPWM1_CNT6_PERIOD_BUFF	0x40390298	Counter buffered period register. See TCPWM1_CNT0_PERIOD_BUFFfor the details of bit fields.
TCPWM1_CNT6_TR_CTRL0	0x403902A0	Counter trigger control register 0. See TCPWM0_CNT0_TR_CTRL0 for the details of bit fields.
TCPWM1_CNT6_TR_CTRL1	0x403902A4	Counter trigger control register 1. See TCPWM0_CNT0_TR_CTRL1 for the details of bit fields.
TCPWM1_CNT6_TR_CTRL2	0x403902A8	Counter trigger control register 2. See TCPWM0_CNT0_TR_CTRL2 for the details of bit fields.
TCPWM1_CNT6_INTR	0x403902B0	Interrupt request register. See TCPWM0_CNT0_INTRfor the details of bit fields.
TCPWM1_CNT6_INTR_SET	0x403902B4	Interrupt set request register. See TCPWM0_CNT0_INTR_SETfor the details of bit fields.
TCPWM1_CNT6_INTR_MASK	0x403902B8	Interrupt mask register. See TCPWM0_CNT0_INTR_MASKfor the details of bit fields.
TCPWM1_CNT6_INTR_MASKED	0x403902BC	Interrupt masked request register. See TCPWM0_CNT0_INTR_MASKEDfor the details of bit fields.
TCPWM1_CNT7_CTRL	0x403902C0	Counter control register. See TCPWM0_CNT0_CTRL for the details of bit fields.
TCPWM1_CNT7_STATUS	0x403902C4	Counter status register. See TCPWM0_CNT0_STATUS for the details of bit fields.
TCPWM1_CNT7_COUNTER	0x403902C8	Counter count register. See TCPWM1_CNT0_COUNTER for the details of bit fields.
TCPWM1_CNT7_CC	0x403902CC	Counter compare/capture register. See TCPWM1_CNT0_CCfor the details of bit fields.

Register	Address	Description
TCPWM1_CNT7_CC_BUFF	0x403902D0	Counter buffered compare/capture register. See TCPWM1_CNT0_CC_BUFFfor the details of bit fields.
TCPWM1_CNT7_PERIOD	0x403902D4	Counter period register. See TCPWM1_CNT0_PERIODfor the details of bit fields.
TCPWM1_CNT7_PERIOD_BUFF	0x403902D8	Counter buffered period register. See TCPWM1_CNT0_PERIOD_BUFFfor the details of bit fields.
TCPWM1_CNT7_TR_CTRL0	0x403902E0	Counter trigger control register 0. See TCPWM0_CNT0_TR_CTRL0 for the details of bit fields.
TCPWM1_CNT7_TR_CTRL1	0x403902E4	Counter trigger control register 1. See TCPWM0_CNT0_TR_CTRL1 for the details of bit fields.
TCPWM1_CNT7_TR_CTRL2	0x403902E8	Counter trigger control register 2. See TCPWM0_CNT0_TR_CTRL2 for the details of bit fields.
TCPWM1_CNT7_INTR	0x403902F0	Interrupt request register. See TCPWM0_CNT0_INTRfor the details of bit fields.
TCPWM1_CNT7_INTR_SET	0x403902F4	Interrupt set request register. See TCPWM0_CNT0_INTR_SETfor the details of bit fields.
TCPWM1_CNT7_INTR_MASK	0x403902F8	Interrupt mask register. See TCPWM0_CNT0_INTR_MASKfor the details of bit fields.
TCPWM1_CNT7_INTR_MASKED	0x403902FC	Interrupt masked request register. See TCPWM0_CNT0_INTR_MASKEDfor the details of bit fields.
TCPWM1_CNT8_CTRL	0x40390300	Counter control register. See TCPWM0_CNT0_CTRL for the details of bit fields.
TCPWM1_CNT8_STATUS	0x40390304	Counter status register. See TCPWM0_CNT0_STATUS for the details of bit fields.
TCPWM1_CNT8_COUNTER	0x40390308	Counter count register. See TCPWM1_CNT0_COUNTER for the details of bit fields.
TCPWM1_CNT8_CC	0x4039030C	Counter compare/capture register. See TCPWM1_CNT0_CCfor the details of bit fields.
TCPWM1_CNT8_CC_BUFF	0x40390310	Counter buffered compare/capture register. See TCPWM1_CNT0_CC_BUFFfor the details of bit fields.
TCPWM1_CNT8_PERIOD	0x40390314	Counter period register. See TCPWM1_CNT0_PERIODfor the details of bit fields.
TCPWM1_CNT8_PERIOD_BUFF	0x40390318	Counter buffered period register. See TCPWM1_CNT0_PERIOD_BUFFfor the details of bit fields.
TCPWM1_CNT8_TR_CTRL0	0x40390320	Counter trigger control register 0. See TCPWM0_CNT0_TR_CTRL0 for the details of bit fields.
TCPWM1_CNT8_TR_CTRL1	0x40390324	Counter trigger control register 1. See TCPWM0_CNT0_TR_CTRL1 for the details of bit fields.
TCPWM1_CNT8_TR_CTRL2	0x40390328	Counter trigger control register 2. See TCPWM0_CNT0_TR_CTRL2 for the details of bit fields.
TCPWM1_CNT8_INTR	0x40390330	Interrupt request register. See TCPWM0_CNT0_INTRfor the details of bit fields.
TCPWM1_CNT8_INTR_SET	0x40390334	Interrupt set request register. See TCPWM0_CNT0_INTR_SETfor the details of bit fields.
TCPWM1_CNT8_INTR_MASK	0x40390338	Interrupt mask register. See TCPWM0_CNT0_INTR_MASKfor the details of bit fields.
TCPWM1_CNT8_INTR_MASKED	0x4039033C	Interrupt masked request register. See TCPWM0_CNT0_INTR_MASKEDfor the details of bit fields.
TCPWM1_CNT9_CTRL	0x40390340	Counter control register. See TCPWM0_CNT0_CTRL for the details of bit fields.
TCPWM1_CNT9_STATUS	0x40390344	Counter status register. See TCPWM0_CNT0_STATUS for the details of bit fields.
TCPWM1_CNT9_COUNTER	0x40390348	Counter count register. See TCPWM1_CNT0_COUNTER for the details of bit fields.
TCPWM1_CNT9_CC	0x4039034C	Counter compare/capture register. See TCPWM1_CNT0_CCfor the details of bit fields.
TCPWM1_CNT9_CC_BUFF	0x40390350	Counter buffered compare/capture register. See TCPWM1_CNT0_CC_BUFFfor the details of bit fields.

Register	Address	Description
TCPWM1_CNT9_PERIOD	0x40390354	Counter period register. See TCPWM1_CNT0_PERIODfor the details of bit fields.
TCPWM1_CNT9_PERIOD_BUFF	0x40390358	Counter buffered period register. See TCPWM1_CNT0_PERIOD_BUFFfor the details of bit fields.
TCPWM1_CNT9_TR_CTRL0	0x40390360	Counter trigger control register 0. See TCPWM0_CNT0_TR_CTRL0 for the details of bit fields.
TCPWM1_CNT9_TR_CTRL1	0x40390364	Counter trigger control register 1. See TCPWM0_CNT0_TR_CTRL1 for the details of bit fields.
TCPWM1_CNT9_TR_CTRL2	0x40390368	Counter trigger control register 2. See TCPWM0_CNT0_TR_CTRL2 for the details of bit fields.
TCPWM1_CNT9_INTR	0x40390370	Interrupt request register. See TCPWM0_CNT0_INTRfor the details of bit fields.
TCPWM1_CNT9_INTR_SET	0x40390374	Interrupt set request register. See TCPWM0_CNT0_INTR_SETfor the details of bit fields.
TCPWM1_CNT9_INTR_MASK	0x40390378	Interrupt mask register. See TCPWM0_CNT0_INTR_MASKfor the details of bit fields.
TCPWM1_CNT9_INTR_MASKED	0x4039037C	Interrupt masked request register. See TCPWM0_CNT0_INTR_MASKEDfor the details of bit fields.
TCPWM1_CNT10_CTRL	0x40390380	Counter control register. See TCPWM0_CNT0_CTRL for the details of bit fields.
TCPWM1_CNT10_STATUS	0x40390384	Counter status register. See TCPWM0_CNT0_STATUS for the details of bit fields.
TCPWM1_CNT10_COUNTER	0x40390388	Counter count register. See TCPWM1_CNT0_COUNTER for the details of bit fields.
TCPWM1_CNT10_CC	0x4039038C	Counter compare/capture register. See TCPWM1_CNT0_CCfor the details of bit fields.
TCPWM1_CNT10_CC_BUFF	0x40390390	Counter buffered compare/capture register. See TCPWM1_CNT0_CC_BUFFfor the details of bit fields.
TCPWM1_CNT10_PERIOD	0x40390394	Counter period register. See TCPWM1_CNT0_PERIODfor the details of bit fields.
TCPWM1_CNT10_PERIOD_BUFF	0x40390398	Counter buffered period register. See TCPWM1_CNT0_PERIOD_BUFFfor the details of bit fields.
TCPWM1_CNT10_TR_CTRL0	0x403903A0	Counter trigger control register 0. See TCPWM0_CNT0_TR_CTRL0 for the details of bit fields.
TCPWM1_CNT10_TR_CTRL1	0x403903A4	Counter trigger control register 1. See TCPWM0_CNT0_TR_CTRL1 for the details of bit fields.
TCPWM1_CNT10_TR_CTRL2	0x403903A8	Counter trigger control register 2. See TCPWM0_CNT0_TR_CTRL2 for the details of bit fields.
TCPWM1_CNT10_INTR	0x403903B0	Interrupt request register. See TCPWM0_CNT0_INTRfor the details of bit fields.
TCPWM1_CNT10_INTR_SET	0x403903B4	Interrupt set request register. See TCPWM0_CNT0_INTR_SETfor the details of bit fields.
TCPWM1_CNT10_INTR_MASK	0x403903B8	Interrupt mask register. See TCPWM0_CNT0_INTR_MASKfor the details of bit fields.
TCPWM1_CNT10_INTR_MASKED	0x403903BC	Interrupt masked request register. See TCPWM0_CNT0_INTR_MASKEDfor the details of bit fields.
TCPWM1_CNT11_CTRL	0x403903C0	Counter control register. See TCPWM0_CNT0_CTRL for the details of bit fields.
TCPWM1_CNT11_STATUS	0x403903C4	Counter status register. See TCPWM0_CNT0_STATUS for the details of bit fields.
TCPWM1_CNT11_COUNTER	0x403903C8	Counter count register. See TCPWM1_CNT0_COUNTER for the details of bit fields.
TCPWM1_CNT11_CC	0x403903CC	Counter compare/capture register. See TCPWM1_CNT0_CCfor the details of bit fields.
TCPWM1_CNT11_CC_BUFF	0x403903D0	Counter buffered compare/capture register. See TCPWM1_CNT0_CC_BUFFfor the details of bit fields.
TCPWM1_CNT11_PERIOD	0x403903D4	Counter period register. See TCPWM1_CNT0_PERIODfor the details of bit fields.

Register	Address	Description
TCPWM1_CNT11_PERIOD_BUFF	0x403903D8	Counter buffered period register. See TCPWM1_CNT0_PERIOD_BUFFfor the details of bit fields.
TCPWM1_CNT11_TR_CTRL0	0x403903E0	Counter trigger control register 0. See TCPWM0_CNT0_TR_CTRL0 for the details of bit fields.
TCPWM1_CNT11_TR_CTRL1	0x403903E4	Counter trigger control register 1. See TCPWM0_CNT0_TR_CTRL1 for the details of bit fields.
TCPWM1_CNT11_TR_CTRL2	0x403903E8	Counter trigger control register 2. See TCPWM0_CNT0_TR_CTRL2 for the details of bit fields.
TCPWM1_CNT11_INTR	0x403903F0	Interrupt request register. See TCPWM0_CNT0_INTRfor the details of bit fields.
TCPWM1_CNT11_INTR_SET	0x403903F4	Interrupt set request register. See TCPWM0_CNT0_INTR_SETfor the details of bit fields.
TCPWM1_CNT11_INTR_MASK	0x403903F8	Interrupt mask register. See TCPWM0_CNT0_INTR_MASKfor the details of bit fields.
TCPWM1_CNT11_INTR_MASKED	0x403903FC	Interrupt masked request register. See TCPWM0_CNT0_INTR_MASKEDfor the details of bit fields.
TCPWM1_CNT12_CTRL	0x40390400	Counter control register. See TCPWM0_CNT0_CTRL for the details of bit fields.
TCPWM1_CNT12_STATUS	0x40390404	Counter status register. See TCPWM0_CNT0_STATUS for the details of bit fields.
TCPWM1_CNT12_COUNTER	0x40390408	Counter count register. See TCPWM1_CNT0_COUNTER for the details of bit fields.
TCPWM1_CNT12_CC	0x4039040C	Counter compare/capture register. See TCPWM1_CNT0_CCfor the details of bit fields.
TCPWM1_CNT12_CC_BUFF	0x40390410	Counter buffered compare/capture register. See TCPWM1_CNT0_CC_BUFFfor the details of bit fields.
TCPWM1_CNT12_PERIOD	0x40390414	Counter period register. See TCPWM1_CNT0_PERIODfor the details of bit fields.
TCPWM1_CNT12_PERIOD_BUFF	0x40390418	Counter buffered period register. See TCPWM1_CNT0_PERIOD_BUFFfor the details of bit fields.
TCPWM1_CNT12_TR_CTRL0	0x40390420	Counter trigger control register 0. See TCPWM0_CNT0_TR_CTRL0for the details of bit fields.
TCPWM1_CNT12_TR_CTRL1	0x40390424	Counter trigger control register 1. See TCPWM0_CNT0_TR_CTRL1for the details of bit fields.
TCPWM1_CNT12_TR_CTRL2	0x40390428	Counter trigger control register 2. See TCPWM0_CNT0_TR_CTRL2for the details of bit fields.
TCPWM1_CNT12_INTR	0x40390430	Interrupt request register. See TCPWM0_CNT0_INTRfor the details of bit fields.
TCPWM1_CNT12_INTR_SET	0x40390434	Interrupt set request register. See TCPWM0_CNT0_INTR_SETfor the details of bit fields.
TCPWM1_CNT12_INTR_MASK	0x40390438	Interrupt mask register. See TCPWM0_CNT0_INTR_MASKfor the details of bit fields.
TCPWM1_CNT12_INTR_MASKED	0x4039043C	Interrupt masked request register. See TCPWM0_CNT0_INTR_MASKEDfor the details of bit fields.
TCPWM1_CNT13_CTRL	0x40390440	Counter control register. See TCPWM0_CNT0_CTRL for the details of bit fields.
TCPWM1_CNT13_STATUS	0x40390444	Counter status register. See TCPWM0_CNT0_STATUS for the details of bit fields.
TCPWM1_CNT13_COUNTER	0x40390448	Counter count register. See TCPWM1_CNT0_COUNTER for the details of bit fields.
TCPWM1_CNT13_CC	0x4039044C	Counter compare/capture register. See TCPWM1_CNT0_CCfor the details of bit fields.
TCPWM1_CNT13_CC_BUFF	0x40390450	Counter buffered compare/capture register. See TCPWM1_CNT0_CC_BUFFfor the details of bit fields.
TCPWM1_CNT13_PERIOD	0x40390454	Counter period register. See TCPWM1_CNT0_PERIODfor the details of bit fields.
TCPWM1_CNT13_PERIOD_BUFF	0x40390458	Counter buffered period register. See TCPWM1_CNT0_PERIOD_BUFFfor the details of bit fields.

Register	Address	Description
TCPWM1_CNT13_TR_CTRL0	0x40390460	Counter trigger control register 0. See TCPWM0_CNT0_TR_CTRL0 for the details of bit fields.
TCPWM1_CNT13_TR_CTRL1	0x40390464	Counter trigger control register 1. See TCPWM0_CNT0_TR_CTRL1 for the details of bit fields.
TCPWM1_CNT13_TR_CTRL2	0x40390468	Counter trigger control register 2. See TCPWM0_CNT0_TR_CTRL2 for the details of bit fields.
TCPWM1_CNT13_INTR	0x40390470	Interrupt request register. See TCPWM0_CNT0_INTRfor the details of bit fields.
TCPWM1_CNT13_INTR_SET	0x40390474	Interrupt set request register. See TCPWM0_CNT0_INTR_SETfor the details of bit fields.
TCPWM1_CNT13_INTR_MASK	0x40390478	Interrupt mask register. See TCPWM0_CNT0_INTR_MASKfor the details of bit fields.
TCPWM1_CNT13_INTR_MASKED	0x4039047C	Interrupt masked request register. See TCPWM0_CNT0_INTR_MASKEDfor the details of bit fields.
TCPWM1_CNT14_CTRL	0x40390480	Counter control register. See TCPWM0_CNT0_CTRL for the details of bit fields.
TCPWM1_CNT14_STATUS	0x40390484	Counter status register. See TCPWM0_CNT0_STATUS for the details of bit fields.
TCPWM1_CNT14_COUNTER	0x40390488	Counter count register. See TCPWM1_CNT0_COUNTER for the details of bit fields.
TCPWM1_CNT14_CC	0x4039048C	Counter compare/capture register. See TCPWM1_CNT0_CCfor the details of bit fields.
TCPWM1_CNT14_CC_BUFF	0x40390490	Counter buffered compare/capture register. See TCPWM1_CNT0_CC_BUFFfor the details of bit fields.
TCPWM1_CNT14_PERIOD	0x40390494	Counter period register. See TCPWM1_CNT0_PERIODfor the details of bit fields.
TCPWM1_CNT14_PERIOD_BUFF	0x40390498	Counter buffered period register. See TCPWM1_CNT0_PERIOD_BUFFfor the details of bit fields.
TCPWM1_CNT14_TR_CTRL0	0x403904A0	Counter trigger control register 0. See TCPWM0_CNT0_TR_CTRL0 for the details of bit fields.
TCPWM1_CNT14_TR_CTRL1	0x403904A4	Counter trigger control register 1. See TCPWM0_CNT0_TR_CTRL1 for the details of bit fields.
TCPWM1_CNT14_TR_CTRL2	0x403904A8	Counter trigger control register 2. See TCPWM0_CNT0_TR_CTRL2 for the details of bit fields.
TCPWM1_CNT14_INTR	0x403904B0	Interrupt request register. See TCPWM0_CNT0_INTRfor the details of bit fields.
TCPWM1_CNT14_INTR_SET	0x403904B4	Interrupt set request register. See TCPWM0_CNT0_INTR_SETfor the details of bit fields.
TCPWM1_CNT14_INTR_MASK	0x403904B8	Interrupt mask register. See TCPWM0_CNT0_INTR_MASKfor the details of bit fields.
TCPWM1_CNT14_INTR_MASKED	0x403904BC	Interrupt masked request register. See TCPWM0_CNT0_INTR_MASKEDfor the details of bit fields.
TCPWM1_CNT15_CTRL	0x403904C0	Counter control register. See TCPWM0_CNT0_CTRL for the details of bit fields.
TCPWM1_CNT15_STATUS	0x403904C4	Counter status register. See TCPWM0_CNT0_STATUS for the details of bit fields.
TCPWM1_CNT15_COUNTER	0x403904C8	Counter count register. See TCPWM1_CNT0_COUNTER for the details of bit fields.
TCPWM1_CNT15_CC	0x403904CC	Counter compare/capture register. See TCPWM1_CNT0_CCfor the details of bit fields.
TCPWM1_CNT15_CC_BUFF	0x403904D0	Counter buffered compare/capture register. See TCPWM1_CNT0_CC_BUFFfor the details of bit fields.
TCPWM1_CNT15_PERIOD	0x403904D4	Counter period register. See TCPWM1_CNT0_PERIODfor the details of bit fields.
TCPWM1_CNT15_PERIOD_BUFF	0x403904D8	Counter buffered period register. See TCPWM1_CNT0_PERIOD_BUFFfor the details of bit fields.
TCPWM1_CNT15_TR_CTRL0	0x403904E0	Counter trigger control register 0. See TCPWM0_CNT0_TR_CTRL0 for the details of bit fields.

Register	Address	Description
TCPWM1_CNT15_TR_CTRL1	0x403904E4	Counter trigger control register 1. See TCPWM0_CNT0_TR_CTRL1 for the details of bit fields.
TCPWM1_CNT15_TR_CTRL2	0x403904E8	Counter trigger control register 2. See TCPWM0_CNT0_TR_CTRL2 for the details of bit fields.
TCPWM1_CNT15_INTR	0x403904F0	Interrupt request register. See TCPWM0_CNT0_INTRfor the details of bit fields.
TCPWM1_CNT15_INTR_SET	0x403904F4	Interrupt set request register. See TCPWM0_CNT0_INTR_SETfor the details of bit fields.
TCPWM1_CNT15_INTR_MASK	0x403904F8	Interrupt mask register. See TCPWM0_CNT0_INTR_MASKfor the details of bit fields.
TCPWM1_CNT15_INTR_MASKED	0x403904FC	Interrupt masked request register. See TCPWM0_CNT0_INTR_MASKEDfor the details of bit fields.
TCPWM1_CNT16_CTRL	0x40390500	Counter control register. See TCPWM0_CNT0_CTRL for the details of bit fields.
TCPWM1_CNT16_STATUS	0x40390504	Counter status register. See TCPWM0_CNT0_STATUS for the details of bit fields.
TCPWM1_CNT16_COUNTER	0x40390508	Counter count register. See TCPWM1_CNT0_COUNTER for the details of bit fields.
TCPWM1_CNT16_CC	0x4039050C	Counter compare/capture register. See TCPWM1_CNT0_CCfor the details of bit fields.
TCPWM1_CNT16_CC_BUFF	0x40390510	Counter buffered compare/capture register. See TCPWM1_CNT0_CC_BUFFfor the details of bit fields.
TCPWM1_CNT16_PERIOD	0x40390514	Counter period register. See TCPWM1_CNT0_PERIODfor the details of bit fields.
TCPWM1_CNT16_PERIOD_BUFF	0x40390518	Counter buffered period register. See TCPWM1_CNT0_PERIOD_BUFFfor the details of bit fields.
TCPWM1_CNT16_TR_CTRL0	0x40390520	Counter trigger control register 0. See TCPWM0_CNT0_TR_CTRL0 for the details of bit fields.
TCPWM1_CNT16_TR_CTRL1	0x40390524	Counter trigger control register 1. See TCPWM0_CNT0_TR_CTRL1 for the details of bit fields.
TCPWM1_CNT16_TR_CTRL2	0x40390528	Counter trigger control register 2. See TCPWM0_CNT0_TR_CTRL2 for the details of bit fields.
TCPWM1_CNT16_INTR	0x40390530	Interrupt request register. See TCPWM0_CNT0_INTRfor the details of bit fields.
TCPWM1_CNT16_INTR_SET	0x40390534	Interrupt set request register. See TCPWM0_CNT0_INTR_SETfor the details of bit fields.
TCPWM1_CNT16_INTR_MASK	0x40390538	Interrupt mask register. See TCPWM0_CNT0_INTR_MASKfor the details of bit fields.
TCPWM1_CNT16_INTR_MASKED	0x4039053C	Interrupt masked request register. See TCPWM0_CNT0_INTR_MASKEDfor the details of bit fields.
TCPWM1_CNT17_CTRL	0x40390540	Counter control register. See TCPWM0_CNT0_CTRL for the details of bit fields.
TCPWM1_CNT17_STATUS	0x40390544	Counter status register. See TCPWM0_CNT0_STATUS for the details of bit fields.
TCPWM1_CNT17_COUNTER	0x40390548	Counter count register. See TCPWM1_CNT0_COUNTER for the details of bit fields.
TCPWM1_CNT17_CC	0x4039054C	Counter compare/capture register. See TCPWM1_CNT0_CCfor the details of bit fields.
TCPWM1_CNT17_CC_BUFF	0x40390550	Counter buffered compare/capture register. See TCPWM1_CNT0_CC_BUFFfor the details of bit fields.
TCPWM1_CNT17_PERIOD	0x40390554	Counter period register. See TCPWM1_CNT0_PERIODfor the details of bit fields.
TCPWM1_CNT17_PERIOD_BUFF	0x40390558	Counter buffered period register. See TCPWM1_CNT0_PERIOD_BUFFfor the details of bit fields.
TCPWM1_CNT17_TR_CTRL0	0x40390560	Counter trigger control register 0. See TCPWM0_CNT0_TR_CTRL0 for the details of bit fields.
TCPWM1_CNT17_TR_CTRL1	0x40390564	Counter trigger control register 1. See TCPWM0_CNT0_TR_CTRL1 for the details of bit fields.

Register	Address	Description
TCPWM1_CNT17_TR_CTRL2	0x40390568	Counter trigger control register 2. See TCPWM0_CNT0_TR_CTRL2 for the details of bit fields.
TCPWM1_CNT17_INTR	0x40390570	Interrupt request register. See TCPWM0_CNT0_INTRfor the details of bit fields.
TCPWM1_CNT17_INTR_SET	0x40390574	Interrupt set request register. See TCPWM0_CNT0_INTR_SETfor the details of bit fields.
TCPWM1_CNT17_INTR_MASK	0x40390578	Interrupt mask register. See TCPWM0_CNT0_INTR_MASKfor the details of bit fields.
TCPWM1_CNT17_INTR_MASKED	0x4039057C	Interrupt masked request register. See TCPWM0_CNT0_INTR_MASKEDfor the details of bit fields.
TCPWM1_CNT18_CTRL	0x40390580	Counter control register. See TCPWM0_CNT0_CTRL for the details of bit fields.
TCPWM1_CNT18_STATUS	0x40390584	Counter status register. See TCPWM0_CNT0_STATUS for the details of bit fields.
TCPWM1_CNT18_COUNTER	0x40390588	Counter count register. See TCPWM1_CNT0_COUNTER for the details of bit fields.
TCPWM1_CNT18_CC	0x4039058C	Counter compare/capture register. See TCPWM1_CNT0_CCfor the details of bit fields.
TCPWM1_CNT18_CC_BUFF	0x40390590	Counter buffered compare/capture register. See TCPWM1_CNT0_CC_BUFFfor the details of bit fields.
TCPWM1_CNT18_PERIOD	0x40390594	Counter period register. See TCPWM1_CNT0_PERIODfor the details of bit fields.
TCPWM1_CNT18_PERIOD_BUFF	0x40390598	Counter buffered period register. See TCPWM1_CNT0_PERIOD_BUFFfor the details of bit fields.
TCPWM1_CNT18_TR_CTRL0	0x403905A0	Counter trigger control register 0. See TCPWM0_CNT0_TR_CTRL0 for the details of bit fields.
TCPWM1_CNT18_TR_CTRL1	0x403905A4	Counter trigger control register 1. See TCPWM0_CNT0_TR_CTRL1 for the details of bit fields.
TCPWM1_CNT18_TR_CTRL2	0x403905A8	Counter trigger control register 2. See TCPWM0_CNT0_TR_CTRL2 for the details of bit fields.
TCPWM1_CNT18_INTR	0x403905B0	Interrupt request register. See TCPWM0_CNT0_INTRfor the details of bit fields.
TCPWM1_CNT18_INTR_SET	0x403905B4	Interrupt set request register. See TCPWM0_CNT0_INTR_SETfor the details of bit fields.
TCPWM1_CNT18_INTR_MASK	0x403905B8	Interrupt mask register. See TCPWM0_CNT0_INTR_MASKfor the details of bit fields.
TCPWM1_CNT18_INTR_MASKED	0x403905BC	Interrupt masked request register. See TCPWM0_CNT0_INTR_MASKEDfor the details of bit fields.
TCPWM1_CNT19_CTRL	0x403905C0	Counter control register. See TCPWM0_CNT0_CTRL for the details of bit fields.
TCPWM1_CNT19_STATUS	0x403905C4	Counter status register. See TCPWM0_CNT0_STATUS for the details of bit fields.
TCPWM1_CNT19_COUNTER	0x403905C8	Counter count register. See TCPWM1_CNT0_COUNTER for the details of bit fields.
TCPWM1_CNT19_CC	0x403905CC	Counter compare/capture register. See TCPWM1_CNT0_CCfor the details of bit fields.
TCPWM1_CNT19_CC_BUFF	0x403905D0	Counter buffered compare/capture register. See TCPWM1_CNT0_CC_BUFFfor the details of bit fields.
TCPWM1_CNT19_PERIOD	0x403905D4	Counter period register. See TCPWM1_CNT0_PERIODfor the details of bit fields.
TCPWM1_CNT19_PERIOD_BUFF	0x403905D8	Counter buffered period register. See TCPWM1_CNT0_PERIOD_BUFFfor the details of bit fields.
TCPWM1_CNT19_TR_CTRL0	0x403905E0	Counter trigger control register 0. See TCPWM0_CNT0_TR_CTRL0 for the details of bit fields.
TCPWM1_CNT19_TR_CTRL1	0x403905E4	Counter trigger control register 1. See TCPWM0_CNT0_TR_CTRL1 for the details of bit fields.
TCPWM1_CNT19_TR_CTRL2	0x403905E8	Counter trigger control register 2. See TCPWM0_CNT0_TR_CTRL2 for the details of bit fields.

Register	Address	Description
TCPWM1_CNT19_INTR	0x403905F0	Interrupt request register. See TCPWM0_CNT0_INTRfor the details of bit fields.
TCPWM1_CNT19_INTR_SET	0x403905F4	Interrupt set request register. See TCPWM0_CNT0_INTR_SETfor the details of bit fields.
TCPWM1_CNT19_INTR_MASK	0x403905F8	Interrupt mask register. See TCPWM0_CNT0_INTR_MASKfor the details of bit fields.
TCPWM1_CNT19_INTR_MASKED	0x403905FC	Interrupt masked request register. See TCPWM0_CNT0_INTR_MASKEDfor the details of bit fields.
TCPWM1_CNT20_CTRL	0x40390600	Counter control register. See TCPWM0_CNT0_CTRL for the details of bit fields.
TCPWM1_CNT20_STATUS	0x40390604	Counter status register. See TCPWM0_CNT0_STATUS for the details of bit fields.
TCPWM1_CNT20_COUNTER	0x40390608	Counter count register. See TCPWM1_CNT0_COUNTER for the details of bit fields.
TCPWM1_CNT20_CC	0x4039060C	Counter compare/capture register. See TCPWM1_CNT0_CCfor the details of bit fields.
TCPWM1_CNT20_CC_BUFF	0x40390610	Counter buffered compare/capture register. See TCPWM1_CNT0_CC_BUFFfor the details of bit fields.
TCPWM1_CNT20_PERIOD	0x40390614	Counter period register. See TCPWM1_CNT0_PERIODfor the details of bit fields.
TCPWM1_CNT20_PERIOD_BUFF	0x40390618	Counter buffered period register. See TCPWM1_CNT0_PERIOD_BUFFfor the details of bit fields.
TCPWM1_CNT20_TR_CTRL0	0x40390620	Counter trigger control register 0. See TCPWM0_CNT0_TR_CTRL0 for the details of bit fields.
TCPWM1_CNT20_TR_CTRL1	0x40390624	Counter trigger control register 1. See TCPWM0_CNT0_TR_CTRL1 for the details of bit fields.
TCPWM1_CNT20_TR_CTRL2	0x40390628	Counter trigger control register 2. See TCPWM0_CNT0_TR_CTRL2 for the details of bit fields.
TCPWM1_CNT20_INTR	0x40390630	Interrupt request register. See TCPWM0_CNT0_INTRfor the details of bit fields.
TCPWM1_CNT20_INTR_SET	0x40390634	Interrupt set request register. See TCPWM0_CNT0_INTR_SETfor the details of bit fields.
TCPWM1_CNT20_INTR_MASK	0x40390638	Interrupt mask register. See TCPWM0_CNT0_INTR_MASKfor the details of bit fields.
TCPWM1_CNT20_INTR_MASKED	0x4039063C	Interrupt masked request register. See TCPWM0_CNT0_INTR_MASKEDfor the details of bit fields.
TCPWM1_CNT21_CTRL	0x40390640	Counter control register. See TCPWM0_CNT0_CTRL for the details of bit fields.
TCPWM1_CNT21_STATUS	0x40390644	Counter status register. See TCPWM0_CNT0_STATUS for the details of bit fields.
TCPWM1_CNT21_COUNTER	0x40390648	Counter count register. See TCPWM1_CNT0_COUNTER for the details of bit fields.
TCPWM1_CNT21_CC	0x4039064C	Counter compare/capture register. See TCPWM1_CNT0_CCfor the details of bit fields.
TCPWM1_CNT21_CC_BUFF	0x40390650	Counter buffered compare/capture register. See TCPWM1_CNT0_CC_BUFFfor the details of bit fields.
TCPWM1_CNT21_PERIOD	0x40390654	Counter period register. See TCPWM1_CNT0_PERIODfor the details of bit fields.
TCPWM1_CNT21_PERIOD_BUFF	0x40390658	Counter buffered period register. See TCPWM1_CNT0_PERIOD_BUFFfor the details of bit fields.
TCPWM1_CNT21_TR_CTRL0	0x40390660	Counter trigger control register 0. See TCPWM0_CNT0_TR_CTRL0 for the details of bit fields.
TCPWM1_CNT21_TR_CTRL1	0x40390664	Counter trigger control register 1. See TCPWM0_CNT0_TR_CTRL1 for the details of bit fields.
TCPWM1_CNT21_TR_CTRL2	0x40390668	Counter trigger control register 2. See TCPWM0_CNT0_TR_CTRL2 for the details of bit fields.
TCPWM1_CNT21_INTR	0x40390670	Interrupt request register. See TCPWM0_CNT0_INTRfor the details of bit fields.

Register	Address	Description
TCPWM1_CNT21_INTR_SET	0x40390674	Interrupt set request register. See TCPWM0_CNT0_INTR_SETfor the details of bit fields.
TCPWM1_CNT21_INTR_MASK	0x40390678	Interrupt mask register. See TCPWM0_CNT0_INTR_MASKfor the details of bit fields.
TCPWM1_CNT21_INTR_MASKED	0x4039067C	Interrupt masked request register. See TCPWM0_CNT0_INTR_MASKEDfor the details of bit fields.
TCPWM1_CNT22_CTRL	0x40390680	Counter control register. See TCPWM0_CNT0_CTRL for the details of bit fields.
TCPWM1_CNT22_STATUS	0x40390684	Counter status register. See TCPWM0_CNT0_STATUS for the details of bit fields.
TCPWM1_CNT22_COUNTER	0x40390688	Counter count register. See TCPWM1_CNT0_COUNTER for the details of bit fields.
TCPWM1_CNT22_CC	0x4039068C	Counter compare/capture register. See TCPWM1_CNT0_CCfor the details of bit fields.
TCPWM1_CNT22_CC_BUFF	0x40390690	Counter buffered compare/capture register. See TCPWM1_CNT0_CC_BUFFfor the details of bit fields.
TCPWM1_CNT22_PERIOD	0x40390694	Counter period register. See TCPWM1_CNT0_PERIODfor the details of bit fields.
TCPWM1_CNT22_PERIOD_BUFF	0x40390698	Counter buffered period register. See TCPWM1_CNT0_PERIOD_BUFFfor the details of bit fields.
TCPWM1_CNT22_TR_CTRL0	0x403906A0	Counter trigger control register 0. See TCPWM0_CNT0_TR_CTRL0 for the details of bit fields.
TCPWM1_CNT22_TR_CTRL1	0x403906A4	Counter trigger control register 1. See TCPWM0_CNT0_TR_CTRL1 for the details of bit fields.
TCPWM1_CNT22_TR_CTRL2	0x403906A8	Counter trigger control register 2. See TCPWM0_CNT0_TR_CTRL2 for the details of bit fields.
TCPWM1_CNT22_INTR	0x403906B0	Interrupt request register. See TCPWM0_CNT0_INTRfor the details of bit fields.
TCPWM1_CNT22_INTR_SET	0x403906B4	Interrupt set request register. See TCPWM0_CNT0_INTR_SETfor the details of bit fields.
TCPWM1_CNT22_INTR_MASK	0x403906B8	Interrupt mask register. See TCPWM0_CNT0_INTR_MASKfor the details of bit fields.
TCPWM1_CNT22_INTR_MASKED	0x403906BC	Interrupt masked request register. See TCPWM0_CNT0_INTR_MASKEDfor the details of bit fields.
TCPWM1_CNT23_CTRL	0x403906C0	Counter control register. See TCPWM0_CNT0_CTRL for the details of bit fields.
TCPWM1_CNT23_STATUS	0x403906C4	Counter status register. See TCPWM0_CNT0_STATUS for the details of bit fields.
TCPWM1_CNT23_COUNTER	0x403906C8	Counter count register. See TCPWM1_CNT0_COUNTER for the details of bit fields.
TCPWM1_CNT23_CC	0x403906CC	Counter compare/capture register. See TCPWM1_CNT0_CC for the details of bit fields.
TCPWM1_CNT23_CC_BUFF	0x403906D0	Counter buffered compare/capture register. See TCPWM1_CNT0_CC_BUFFfor the details of bit fields.
TCPWM1_CNT23_PERIOD	0x403906D4	Counter period register. See TCPWM1_CNT0_PERIOD for the details of bit fields.
TCPWM1_CNT23_PERIOD_BUFF	0x403906D8	Counter buffered period register. See TCPWM1_CNT0_PERIOD_BUFFfor the details of bit fields.
TCPWM1_CNT23_TR_CTRL0	0x403906E0	Counter trigger control register 0. See TCPWM0_CNT0_TR_CTRL0 for the details of bit fields.
TCPWM1_CNT23_TR_CTRL1	0x403906E4	Counter trigger control register 1. See TCPWM0_CNT0_TR_CTRL1 for the details of bit fields.
TCPWM1_CNT23_TR_CTRL2	0x403906E8	Counter trigger control register 2. See TCPWM0_CNT0_TR_CTRL2 for the details of bit fields.
TCPWM1_CNT23_INTR	0x403906F0	Interrupt request register. See TCPWM0_CNT0_INTR for the details of bit fields.
TCPWM1_CNT23_INTR_SET	0x403906F4	Interrupt set request register. See TCPWM0_CNT0_INTR_SET for the details of bit fields.

Register	Address	Description
TCPWM1_CNT23_INTR_MASK	0x403906F8	Interrupt mask register. See TCPWM0_CNT0_INTR_MASK for the details of bit fields.
TCPWM1_CNT23_INTR_MASKED	0x403906FC	Interrupt masked request register. See TCPWM0_CNT0_INTR_MASKED for the details of bit fields.

20.1.1 TCPWM0_CTRL

TCPWM control register

Address: 0x40380000

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	COUNTER_ENABLED [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	COUNTER_ENABLED	Counter enables for counters 0 up to CNT_NR-1. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_CTRL0, TR_CTRL1, and TR_CTRL2 register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_overflow", "tr_underflow" and "tr_compare_match"). - the counter's line outputs ("line_out" and "line_compl_out"). In multi-core environments, use the CTRL_SET/CTRL_CLR registers to avoid race-conditions on read-modify-write attempts to this register. Default Value: 0

20.1.2 TCPWM0_CTRL_CLR

TCPWM control clear register

Address: 0x40380004

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C							
HW Access	A							
Name	COUNTER_ENABLED [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	COUNTER_ENABLED	Alias of CTRL that only allows disabling of counters. A write access: '0': Does nothing. '1': Clears respective COUNTER_ENABLED field. A read access returns CTRL.COUNTER_ENABLED. Default Value: 0

20.1.3 TCPWM0_CTRL_SET

TCPWM control set register

Address: 0x40380008

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S							
HW Access	A							
Name	COUNTER_ENABLED [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	COUNTER_ENABLED	Alias of CTRL that only allows enabling of counters. A write access: '0': Does nothing. '1': Sets respective COUNTER_ENABLED field. A read access returns CTRL.COUNTER_ENABLED. Default Value: 0

20.1.4 TCPWM0_CMD_CAPTURE

TCPWM capture command register

Address: 0x4038000C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S							
HW Access	RW1C							
Name	COUNTER_CAPTURE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	COUNTER_CAPTURE	Counters SW capture trigger. When written with '1', a capture trigger is generated and the HW sets the field to '0' when the SW trigger has taken effect. It should be noted that the HW operates on the counter frequency. If the counter is disabled through CTRL.COUNTER_ENABLED, the field is immediately set to '0'. Default Value: 0

20.1.5 TCPWM0_CMD_RELOAD

TCPWM reload command register

Address: 0x40380010

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S							
HW Access	RW1C							
Name	COUNTER_RELOAD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	COUNTER_RELOAD	Counters SW reload trigger. For HW behavior, see COUNTER_CAPTURE field. Default Value: 0

20.1.6 TCPWM0_CMD_STOP

TCPWM stop command register

Address: 0x40380014

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S							
HW Access	RW1C							
Name	COUNTER_STOP [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	COUNTER_STOP	Counters SW stop trigger. For HW behavior, see COUNTER_CAPTURE field. Default Value: 0

20.1.7 TCPWM0_CMD_START

TCPWM start command register

Address: 0x40380018

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S							
HW Access	RW1C							
Name	COUNTER_START [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	COUNTER_START	Counters SW start trigger. For HW behavior, see COUNTER_CAPTURE field. Default Value: 0

20.1.8 TCPWM0_INTR_CAUSE

TCPWM Counter interrupt cause register

Address: 0x4038001C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	COUNTER_INT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	COUNTER_INT	Counters interrupt signal active. If the counter is disabled through CTRL.COUNTER_ENABLED, the associated interrupt field is immediately set to '0'. Default Value: 0

20.1.9 TCPWM0_CNT0_CTRL

Counter control register

Address: 0x40380100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [7:4]				PW-M_STOP_ON_KILL	PWM_SYN-C_KILL	AUTO_RE-LOAD_PE-RIOD	AUTO_RE-LOAD_CC

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	GENERIC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW		None	RW	RW	
HW Access	None		R		None	R	R	
Name	None [23:22]		QUADRATURE_MODE [21:20]		None	ONE_SHOT	UP_DOWN_MODE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None					RW		
HW Access	None					R		
Name	None [31:27]					MODE [26:24]		

Bits	Name	Description
26 : 24	MODE	Counter mode. Default Value: 0 **0x0: TIMER :** Timer mode **0x2: CAPTURE :** Capture mode **0x3: QUAD :** Quadrature encoding mode

20.1.9 TCPWM0_CNT0_CTRL (continued)

		0x4: PWM : Pulse width modulation (PWM) mode **0x5: PWM_DT :** PWM with deadtime insertion mode **0x6: PWM_PR :** Pseudo random pulse width modulation
21 : 20	QUADRATURE_MODE	In QUAD mode selects quadrature encoding mode (X1/X2/X4). In PWM, PWM_DT and PWM_PR modes, these two bits can be used to invert "dt_line_out" and "dt_line_compl_out". Inversion is the last step in generation of "dt_line_out" and "dt_line_compl_out"; i.e. a disabled output line "dt_line_out" has the value QUADRATURE_MODE[0] and a disabled output line "dt_line_compl_out" has the value QUADRATURE_MODE[1]. Default Value: 0 **0x0: X1 :** X1 encoding (QUAD mode) **0x1: X2 :** X2 encoding (QUAD mode) **0x2: X4 :** X4 encoding (QUAD mode) **0x1: INV_OUT :** When bit 0 is '1', QUADRATURE_MODE[0] inverts "dt_line_out" (PWM/PWM_DT modes) **0x2: INV_COMPL_OUT :** When bit 1 is '1', QUADRATURE_MODE[1] inverts "dt_line_compl_out" (PWM/PWM_DT modes)
18	ONE_SHOT	When '0', counter runs continuous. When '1', counter is turned off by hardware when a terminal count event is generated. Default Value: 0
17 : 16	UP_DOWN_MODE	Determines counter direction. Default Value: 0 **0x0: COUNT_UP :** Count up (to PERIOD). An overflow event is generated when the counter changes from a state in which COUNTER equals PERIOD. A terminal count event is generated when the counter changes from a state in which COUNTER equals PERIOD.

20.1.9 TCPWM0_CNT0_CTRL (continued)

		0x1: COUNT_DOWN : Count down (to "0"). An underflow event is generated when the counter changes from a state in which COUNTER equals "0". A terminal count event is generated when the counter changes from a state in which COUNTER equals "0". **0x2: COUNT_UPDN1 :** Count up (to PERIOD), then count down (to "0"). An overflow event is generated when the counter changes from a state in which COUNTER equals PERIOD. An underflow event is generated when the counter changes from a state in which COUNTER equals "0". A terminal count event is generated when the counter changes from a state in which COUNTER equals "0". **0x3: COUNT_UPDN2 :** Count up (to PERIOD), then count down (to "0"). An overflow event is generated when the counter changes from a state in which COUNTER equals PERIOD. An underflow event is generated when the counter changes from a state in which COUNTER equals "0". A terminal count event is generated when the counter changes from a state in which COUNTER equals "0" AND when the counter changes from a state in which COUNTER equals PERIOD (this counter direction can be used for PWM functionality with asymmetrical updates).
15 : 8	GENERIC	Generic 8-bit control field. In PWM_DT mode, this field is used to determine the dead time: amount of dead time cycles in the counter clock domain. In all other modes, the lower 3 bits of this field determine pre-scaling of the selected counter clock. Default Value: 0 **0x0: DIVBY1 :** Divide by 1 (other-than-PWM_DT mode) **0x1: DIVBY2 :** Divide by 2 (other-than-PWM_DT mode) **0x2: DIVBY4 :** Divide by 4 (other-than-PWM_DT mode) **0x3: DIVBY8 :** Divide by 8 (other-than-PWM_DT mode) **0x4: DIVBY16 :** Divide by 16 (other-than-PWM_DT mode) **0x5: DIVBY32 :** Divide by 32 (other-than-PWM_DT mode)

20.1.9 TCPWM0_CNT0_CTRL (continued)

		0x6: DIVBY64 : Divide by 64 (other-than-PWM_DT mode) **0x7: DIVBY128 :** Divide by 128 (other-than-PWM_DT mode)
3	PWM_STOP_ON_KILL	Specifies whether the counter stops on a kill events: '0': kill event does NOT stop counter. '1': kill event stops counter. This field has a function in PWM, PWM_DT and PWM_PR modes only. Default Value: 0
2	PWM_SYNC_KILL	Specifies asynchronous/synchronous kill behavior: '1': synchronous kill mode: the kill event disables the "dt_line_out" and "dt_line_compl_out" signals till the next terminal count event (synchronous kill). In synchronous kill mode, STOP_EDGE should be RISING_EDGE. '0': asynchronous kill mode: the kill event only disables the "dt_line_out" and "dt_line_compl_out" signals when present. In asynchronous kill mode, STOP_EDGE should be NO_EDGE_DET. This field has a function in PWM and PWM_DT modes only. This field is only used when PWM_STOP_ON_KILL is '0'. Default Value: 0
1	AUTO_RELOAD_PERIOD	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM, PWM_DT and PWM_PR modes. '0': never switch. '1': switch on a terminal count event with and actively pending switch event. Default Value: 0
0	AUTO_RELOAD_CC	Specifies switching of the CC and buffered CC values. This field has a function in TIMER, PWM, PWM_DT and PWM_PR modes. Timer mode: '0': never switch. '1': switch on a compare match event. PWM, PWM_DT, PWM_PR modes: '0: never switch. '1': switch on a terminal count event with an actively pending switch event. Default Value: 0

20.1.10 TCPWM0_CNT0_STATUS

Counter status register

Address: 0x40380104

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							DOWN

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	GENERIC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	RW	None						
Name	RUNNING	None [30:24]						

Bits	Name	Description
31	RUNNING	When '0', the counter is NOT running. When '1', the counter is running. Default Value: 0
15 : 8	GENERIC	Generic 8-bit counter field. In PWM_DT mode, this counter is used for dead time insertion. In all other modes, this counter is used for pre-scaling the selected counter clock. PWM_DT mode can NOT use prescaled clock functionality. Default Value: 0
0	DOWN	When '0', counter is counting up. When '1', counter is counting down. In QUAD mode, this field indicates the direction of the latest counter change: '0' when last incremented and '1' when last decremented. Default Value: 0

20.1.11 TCPWM0_CNT0_COUNTER

Counter count register

Address: 0x40380108

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	COUNTER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	COUNTER [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	COUNTER [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	COUNTER [31:24]							

Bits	Name	Description
31 : 0	COUNTER	32-bit counter value. It is advised to not write to this field when the counter is running. Default Value: 0

20.1.12 TCPWM0_CNT0_CC

Counter compare/capture register

Address: 0x4038010C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	CC [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	CC [31:24]							

Bits	Name	Description
31 : 0	CC	In CAPTURE mode, captures the counter value. In other modes, compared to counter value. Default Value: 4294967295

20.1.13 TCPWM0_CNT0_CC_BUFF

Counter buffered compare/capture register

Address: 0x40380110

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	CC [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	CC [31:24]							

Bits	Name	Description
31 : 0	CC	Additional buffer for counter CC register. Default Value: 4294967295

20.1.14 TCPWM0_CNT0_PERIOD

Counter period register

Address: 0x40380114

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	PERIOD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	PERIOD [31:24]							

Bits	Name	Description
31 : 0	PERIOD	Period value: upper value of the counter. When the counter should count for n cycles, this field should be set to n-1. Default Value: 4294967295

20.1.15 TCPWM0_CNT0_PERIOD_BUFF

Counter buffered period register

Address: 0x40380118

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	PERIOD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	PERIOD [31:24]							

Bits	Name	Description
31 : 0	PERIOD	Additional buffer for counter PERIOD register. Default Value: 4294967295

20.1.16 TCPWM0_CNT0_TR_CTRL0

Counter trigger control register 0

Address: 0x40380120

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	COUNT_SEL [7:4]				CAPTURE_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	STOP_SEL [15:12]				RELOAD_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				START_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	START_SEL	Selects one of the 16 input triggers as a start trigger. In QUAD mode, this is the second phase (phi B). Default Value: 0
15 : 12	STOP_SEL	Selects one of the 16 input triggers as a stop trigger. In PWM, PWM_DT and PWM_PR modes, this is the kill trigger. In these modes, the kill trigger is used to either temporarily block the PWM outputs (PWM_STOP_ON_KILL is '0') or stop the functionality (PWM_STOP_ON_KILL is '1'). For the PWM and PWM_DT modes, the blocking of the output signals can be asynchronous (STOP_EDGE should be NO_EDGE_DET) in which case the blocking is as long as the trigger is '1' or synchronous (STOP_EDGE should be RISING_EDGE) in which case it extends till the next terminal count event. Default Value: 0
11 : 8	RELOAD_SEL	Selects one of the 16 input triggers as a reload trigger. In QUAD mode, this is the index or revolution pulse. In this mode, it will update the counter with 0x8000 (counter midpoint). Default Value: 0
7 : 4	COUNT_SEL	Selects one of the 16 input triggers as a count trigger. In QUAD mode, this is the first phase (phi A). Default setting selects input trigger 1, which is always '1'. Default Value: 1

20.1.16 TCPWM0_CNT0_TR_CTRL0 (continued)

3 : 0	CAPTURE_SEL	Selects one of the 16 input triggers as a capture trigger. Input trigger 0 is always '0' and input trigger is always '1'. In the PWM, PWM_DT and PWM_PR modes this trigger is used to switch the values if the compare and period registers with their buffer counterparts. Default Value: 0

20.1.17 TCPWM0_CNT0_TR_CTRL1

Counter trigger control register 1

Address: 0x40380124

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	STOP_EDGE [7:6]		RELOAD_EDGE [5:4]		COUNT_EDGE [3:2]		CAPTURE_EDGE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						START_EDGE [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 8	START_EDGE	A start event will start the counter; i.e. the counter will become running. Starting does NOT enable the counter. A start event will not initialize the counter whereas the reload event does. Default Value: 3 **0x0: RISING_EDGE :** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE :** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES :** Rising AND falling edge. Any odd amount of edges generates an event.

20.1.17 TCPWM0_CNT0_TR_CTRL1 (continued)

		0x3: NO_EDGE_DET : No edge detection, use trigger as is.
7 : 6	STOP_EDGE	A stop event, will stop the counter; i.e. it will no longer be running. Stopping will NOT disable the counter. Default Value: 3 **0x0: RISING_EDGE :** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE :** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES :** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET :** No edge detection, use trigger as is.
5 : 4	RELOAD_EDGE	A reload event will initialize the counter. When counting up, the counter is initialized to "0". When counting down, the counter is initialized with PERIOD. Default Value: 3 **0x0: RISING_EDGE :** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE :** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES :** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET :** No edge detection, use trigger as is.
3 : 2	COUNT_EDGE	A counter event will increase or decrease the counter by '1'. Default Value: 3 **0x0: RISING_EDGE :** Rising edge. Any rising edge generates an event.

20.1.17 TCPWM0_CNT0_TR_CTRL1 (continued)

		0x1: FALLING_EDGE : Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES :** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET :** No edge detection, use trigger as is.
1 : 0	CAPTURE_EDGE	A capture event will copy the counter value into the CC register. Default Value: 3 **0x0: RISING_EDGE :** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE :** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES :** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET :** No edge detection, use trigger as is.

20.1.18 TCPWM0_CNT0_TR_CTRL2

Counter trigger control register 2

Address: 0x40380128

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW		RW		RW	
HW Access	None		R		R		R	
Name	None [7:6]		UNDERFLOW_MODE [5:4]		OVERFLOW_MODE [3:2]		CC_MATCH_MODE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 4	UNDERFLOW_MODE	Determines the effect of a counter underflow event (COUNTER reaches "0") on the "line_out" output signals. Default Value: 3 **0x0: SET :** Set to '1' **0x1: CLEAR :** Set to '0' **0x2: INVERT :** Invert

20.1.18 TCPWM0_CNT0_TR_CTRL2 (continued)

		0x3: NO_CHANGE : No Change
3 : 2	OVERFLOW_MODE	Determines the effect of a counter overflow event (COUNTER reaches PERIOD) on the "line_out" output signals. Default Value: 3 **0x0: SET :** Set to '1' **0x1: CLEAR :** Set to '0' **0x2: INVERT :** Invert **0x3: NO_CHANGE :** No Change
1 : 0	CC_MATCH_MODE	Determines the effect of a compare match event (COUNTER equals CC register) on the "line_out" output signals. Note that INVERT is especially useful for center aligned pulse width modulation. To generate a duty cycle of 0%, the counter CC register should be set to "0". For a 100% duty cycle, the counter CC register should be set to larger than the counter PERIOD register. Default Value: 3 **0x0: SET :** Set to '1' **0x1: CLEAR :** Set to '0' **0x2: INVERT :** Invert **0x3: NO_CHANGE :** No Change

20.1.19 TCPWM0_CNT0_INTR

Interrupt request register

Address: 0x40380130

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1C	RW1C
HW Access	None						RW1S	RW1S
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Counter matches CC register event. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
0	TC	Terminal count event. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0

20.1.20 TCPWM0_CNT0_INTR_SET

Interrupt set request register

Address: 0x40380134

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1S	RW1S
HW Access	None						A	A
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	TC	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

20.1.21 TCPWM0_CNT0_INTR_MASK

Interrupt mask register

Address: 0x40380138

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	TC	Mask bit for corresponding bit in interrupt request register. Default Value: 0

20.1.22 TCPWM0_CNT0_INTR_MASKED

Interrupt masked request register

Address: 0x4038013C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						W	W
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Logical and of corresponding request and mask bits. Default Value: 0
0	TC	Logical and of corresponding request and mask bits. Default Value: 0

20.1.23 TCPWM1_CTRL

TCPWM control register

Address: 0x40390000

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	COUNTER_ENABLED [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	COUNTER_ENABLED [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	COUNTER_ENABLED [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 0	COUNTER_ENABLED	Counter enables for counters 0 up to CNT_NR-1. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_CTRL0, TR_CTRL1, and TR_CTRL2 register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_overflow", "tr_underflow" and "tr_compare_match"). - the counter's line outputs ("line_out" and "line_compl_out"). In multi-core environments, use the CTRL_SET/CTRL_CLR registers to avoid race-conditions on read-modify-write attempts to this register. Default Value: 0

20.1.24 TCPWM1_CTRL_CLR

TCPWM control clear register

Address: 0x40390004

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C							
HW Access	A							
Name	COUNTER_ENABLED [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1C							
HW Access	A							
Name	COUNTER_ENABLED [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW1C							
HW Access	A							
Name	COUNTER_ENABLED [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 0	COUNTER_ENABLED	Alias of CTRL that only allows disabling of counters. A write access: '0': Does nothing. '1': Clears respective COUNTER_ENABLED field. A read access returns CTRL.COUNTER_ENABLED. Default Value: 0

20.1.25 TCPWM1_CTRL_SET

TCPWM control set register

Address: 0x40390008

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S							
HW Access	A							
Name	COUNTER_ENABLED [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1S							
HW Access	A							
Name	COUNTER_ENABLED [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW1S							
HW Access	A							
Name	COUNTER_ENABLED [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 0	COUNTER_ENABLED	Alias of CTRL that only allows enabling of counters. A write access: '0': Does nothing. '1': Sets respective COUNTER_ENABLED field. A read access returns CTRL.COUNTER_ENABLED. Default Value: 0

20.1.26 TCPWM1_CMD_CAPTURE

TCPWM capture command register

Address: 0x4039000C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S							
HW Access	RW1C							
Name	COUNTER_CAPTURE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1S							
HW Access	RW1C							
Name	COUNTER_CAPTURE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW1S							
HW Access	RW1C							
Name	COUNTER_CAPTURE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 0	COUNTER_CAPTURE	Counters SW capture trigger. When written with '1', a capture trigger is generated and the HW sets the field to '0' when the SW trigger has taken effect. It should be noted that the HW operates on the counter frequency. If the counter is disabled through CTRL.COUNTER_ENABLED, the field is immediately set to '0'. Default Value: 0

20.1.27 TCPWM1_CMD_RELOAD

TCPWM reload command register

Address: 0x40390010

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S							
HW Access	RW1C							
Name	COUNTER_RELOAD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1S							
HW Access	RW1C							
Name	COUNTER_RELOAD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW1S							
HW Access	RW1C							
Name	COUNTER_RELOAD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 0	COUNTER_RELOAD	Counters SW reload trigger. For HW behavior, see COUNTER_CAPTURE field. Default Value: 0

20.1.28 TCPWM1_CMD_STOP

TCPWM stop command register

Address: 0x40390014

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S							
HW Access	RW1C							
Name	COUNTER_STOP [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1S							
HW Access	RW1C							
Name	COUNTER_STOP [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW1S							
HW Access	RW1C							
Name	COUNTER_STOP [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 0	COUNTER_STOP	Counters SW stop trigger. For HW behavior, see COUNTER_CAPTURE field. Default Value: 0

20.1.29 TCPWM1_CMD_START

TCPWM start command register

Address: 0x40390018

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S							
HW Access	RW1C							
Name	COUNTER_START [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1S							
HW Access	RW1C							
Name	COUNTER_START [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW1S							
HW Access	RW1C							
Name	COUNTER_START [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 0	COUNTER_START	Counters SW start trigger. For HW behavior, see COUNTER_CAPTURE field. Default Value: 0

20.1.30 TCPWM1_INTR_CAUSE

TCPWM Counter interrupt cause register

Address: 0x4039001C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	COUNTER_INT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	COUNTER_INT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	COUNTER_INT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 0	COUNTER_INT	Counters interrupt signal active. If the counter is disabled through CTRL.COUNTER_ENABLED, the associated interrupt field is immediately set to '0'. Default Value: 0

20.1.31 TCPWM1_CNT0_COUNTER

Counter count register

Address: 0x40390108

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	COUNTER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	COUNTER [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	COUNTER	16-bit counter value. It is advised to not write to this field when the counter is running. Default Value: 0

20.1.32 TCPWM1_CNT0_CC

Counter compare/capture register

Address: 0x4039010C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CC	In CAPTURE mode, captures the counter value. In other modes, compared to counter value. Default Value: 65535

20.1.33 TCPWM1_CNT0_CC_BUFF

Counter buffered compare/capture register

Address: 0x40390110

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CC	Additional buffer for counter CC register. Default Value: 65535

20.1.34 TCPWM1_CNT0_PERIOD

Counter period register

Address: 0x40390114

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	PERIOD	Period value: upper value of the counter. When the counter should count for n cycles, this field should be set to n-1. Default Value: 65535

20.1.35 TCPWM1_CNT0_PERIOD_BUFF

Counter buffered period register

Address: 0x40390118

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	PERIOD	Additional buffer for counter PERIOD register. Default Value: 65535

21 Segment LCD Drive Registers

This section discusses the Segment LCD Drive registers. It lists all the registers in mapping tables, in address order.

21.1 Register Details

Register	Address	Description
LCD0_ID	0x403B0000	ID & Revision
LCD0_DIVIDER	0x403B0004	LCD Divider Register
LCD0_CONTROL	0x403B0008	LCD Configuration Register
LCD0_DATA00	0x403B0100	LCD Pin Data Registers
LCD0_DATA01	0x403B0104	LCD Pin Data Registers. See LCD0_DATA00 for the details of bit fields.
LCD0_DATA02	0x403B0108	LCD Pin Data Registers. See LCD0_DATA00 for the details of bit fields.
LCD0_DATA03	0x403B010C	LCD Pin Data Registers. See LCD0_DATA00 for the details of bit fields.
LCD0_DATA04	0x403B0110	LCD Pin Data Registers. See LCD0_DATA00 for the details of bit fields.
LCD0_DATA05	0x403B0114	LCD Pin Data Registers. See LCD0_DATA00 for the details of bit fields.
LCD0_DATA06	0x403B0118	LCD Pin Data Registers. See LCD0_DATA00 for the details of bit fields.
LCD0_DATA07	0x403B011C	LCD Pin Data Registers. See LCD0_DATA00 for the details of bit fields.
LCD0_DATA10	0x403B0200	LCD Pin Data Registers
LCD0_DATA11	0x403B0204	LCD Pin Data Registers. See LCD0_DATA10 for the details of bit fields.
LCD0_DATA12	0x403B0208	LCD Pin Data Registers. See LCD0_DATA10 for the details of bit fields.
LCD0_DATA13	0x403B020C	LCD Pin Data Registers. See LCD0_DATA10 for the details of bit fields.
LCD0_DATA14	0x403B0210	LCD Pin Data Registers. See LCD0_DATA10 for the details of bit fields.
LCD0_DATA15	0x403B0214	LCD Pin Data Registers. See LCD0_DATA10 for the details of bit fields.
LCD0_DATA16	0x403B0218	LCD Pin Data Registers. See LCD0_DATA10 for the details of bit fields.
LCD0_DATA17	0x403B021C	LCD Pin Data Registers. See LCD0_DATA10 for the details of bit fields.

21.1.1 LCD0_ID

ID & Revision

Address: 0x403B0000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	ID [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	REVISION [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	REVISION [31:24]							

Bits	Name	Description
31 : 16	REVISION	the version number is 0x0001 Default Value: 1
15 : 0	ID	the ID of LCD controller peripheral is 0xF0F0 Default Value: 61680

21.1.2 LCD0_DIVIDER

LCD Divider Register

Address: 0x403B0004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SUBFR_DIV [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	SUBFR_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DEAD_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	DEAD_DIV [31:24]							

Bits	Name	Description
31 : 16	DEAD_DIV	Length of the dead time period in cycles. When set to zero, no dead time period exists. Default Value: 0
15 : 0	SUBFR_DIV	Input clock frequency divide value, to generate the 1/4 sub-frame period. The sub-frame period is 4*(SUBFR_DIV+1) cycles long. Default Value: 0

21.1.3 LCD0_CONTROL

LCD Configuration Register

Address: 0x403B0008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW		RW	RW	RW	RW	RW
HW Access	None	R		R	R	R	R	R
Name	None	BIAS [6:5]		OP_MODE	TYPE	LCD_-MODE	HS_EN	LS_EN

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				COM_NUM [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	LS_EN_STAT	None [30:24]						

Bits	Name	Description
31	LS_EN_STAT	LS enable status bit. This bit is a copy of LS_EN that is synchronized to the low speed clock domain and back to the system clock domain. Firmware can use this bit to observe whether LS_EN has taken effect in the low speed clock domain. Firmware should never change the configuration for the LS generator without ensuring this bit is 0. The following procedure should be followed to disable the LS generator: 1. If LS_EN=0 we are done. Exit the procedure. 2. Check that LS_EN_STAT=1. If not, wait until it is. This will catch the case of a recent enable (LS_EN=1) that has not taken effect yet. 3. Set LS_EN=0. 4. Wait until LS_EN_STAT=0. Default Value: 0
11 : 8	COM_NUM	The number of COM connections minus 2. So: 0: 2 COM's 1: 3 COM's ... 6: 8 COM's Default Value: 0

21.1.3 LCD0_CONTROL (continued)

6 : 5	BIAS	PWM bias selection Default Value: 0 **0x0: HALF :** 1/2 Bias **0x1: THIRD :** 1/3 Bias **0x2: FOURTH :** 1/4 Bias (not supported by LS generator) **0x3: FIFTH :** 1/5 Bias (not supported by LS generator)
4	OP_MODE	Driving mode configuration Default Value: 0 **0x0: PWM :** PWM Mode **0x1: CORRELATION :** Digital Correlation Mode
3	TYPE	LCD driving waveform type configuration. Default Value: 0 **0x0: TYPE_A :** Type A - Each frame addresses each COM pin only once with a balanced (DC=0) waveform. **0x1: TYPE_B :** Type B - Each frame addresses each COM pin twice in sequence with a positive and negative waveform that together are balanced (DC=0).
2	LCD_MODE	HS/LS Mode selection Default Value: 0 **0x0: LS :** Select Low Speed (32kHz) Generator (Works in Active, Sleep and DeepSleep power modes). **0x1: HS :** Select High Speed (system clock) Generator (Works in Active and Sleep power modes only).

21.1.3 LCD0_CONTROL (continued)

1	HS_EN	High speed (HS) generator enable 1: enable 0: disable Default Value: 0
0	LS_EN	Low speed (LS) generator enable 1: enable 0: disable Default Value: 0

21.1.4 LCD0_DATA00

LCD Pin Data Registers

Address: 0x403B0100

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Bits [4i+3:4i] represent the pin data for pin [i] for COMS 0-3 (COM0 is lsb). Default Value: 0

21.1.5 LCD0_DATA10

LCD Pin Data Registers

Address: 0x403B0200

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Bits [4i+3:4i] represent the pin data for pin [i] for COMS 4-7 (COM4 is lsb). Default Value: 0

22 BLE Sub System (BLESS) Registers

This section discusses the BLE Subsystem (BLESS) registers. It lists all the registers in mapping tables, in address order.

22.1 Register Details

Register	Address	Description
BLE_RCB_CTRL	0x403C0000	RCB control register.
BLE_RCB_STATUS	0x403C0004	RCB status register.
BLE_RCB_TX_CTRL	0x403C0010	Transmitter control register.
BLE_RCB_TX_FIFO_CTRL	0x403C0014	Transmitter FIFO control register.
BLE_RCB_TX_FIFO_STATUS	0x403C0018	Transmitter FIFO status register.
BLE_RCB_TX_FIFO_WR	0x403C001C	Transmitter FIFO write register.
BLE_RCB_RX_CTRL	0x403C0020	Receiver control register.
BLE_RCB_RX_FIFO_CTRL	0x403C0024	Receiver FIFO control register.
BLE_RCB_RX_FIFO_STATUS	0x403C0028	Receiver FIFO status register.
BLE_RCB_RX_FIFO_RD	0x403C002C	Receiver FIFO read register.
BLE_RCB_RX_FIFO_RD_SILENT	0x403C0030	Receiver FIFO read register.
BLE_RCB_INTR	0x403C0040	Master interrupt request register.
BLE_RCB_INTR_SET	0x403C0044	Master interrupt set request register
BLE_RCB_INTR_MASK	0x403C0048	Master interrupt mask register.
BLE_RCB_INTR_MASKED	0x403C004C	Master interrupt masked request register
BLE_RCB_RCBLL_CTRL	0x403C0100	RCB LL control register.
BLE_RCB_RCBLL_INTR	0x403C0110	Master interrupt request register.
BLE_RCB_RCBLL_INTR_SET	0x403C0114	Master interrupt set request register
BLE_RCB_RCBLL_INTR_MASK	0x403C0118	Master interrupt mask register.
BLE_RCB_RCBLL_INTR_MASKED	0x403C011C	Master interrupt masked request register
BLE_RCB_RCBLL_RADIO_REG1_ADDR	0x403C0120	Address of Register#1 in Radio (MDON)
BLE_RCB_RCBLL_RADIO_REG2_ADDR	0x403C0124	Address of Register#2 in Radio (RSSI)
BLE_RCB_RCBLL_RADIO_REG3_ADDR	0x403C0128	Address of Register#3 in Radio (ACCL)
BLE_RCB_RCBLL_RADIO_REG4_ADDR	0x403C012C	Address of Register#4 in Radio (ACCH)
BLE_RCB_RCBLL_RADIO_REG5_ADDR	0x403C0130	Address of Register#5 in Radio (RSSI ENERGY)
BLE_RCB_RCBLL_CPU_WRITE_REG	0x403C0140	TX_Reserved 1 register
BLE_RCB_RCBLL_CPU_READ_REG	0x403C0144	TX_Reserved 2 register

Register	Address	Description
BLE_BLELL_COMMAND_REGISTER	0x403C1000	Instruction Register
BLE_BLELL_EVENT_INTR	0x403C1008	Event(Interrupt) status and Clear register
BLE_BLELL_EVENT_ENABLE	0x403C1010	Event indications enable.
BLE_BLELL_ADV_PARAMS	0x403C1018	Advertising parameters register.
BLE_BLELL_ADV_INTERVAL_TIMEOUT	0x403C101C	Advertising interval register.
BLE_BLELL_ADV_INTR	0x403C1020	Advertising interrupt status and Clear register
BLE_BLELL_ADV_NEXT_INSTANT	0x403C1024	Advertising next instant.
BLE_BLELL_SCAN_INTERVAL	0x403C1028	Scan Interval Register
BLE_BLELL_SCAN_WINDOW	0x403C102C	Scan window Register
BLE_BLELL_SCAN_PARAM	0x403C1030	Scanning parameters register
BLE_BLELL_SCAN_INTR	0x403C1038	Scan interrupt status and Clear register
BLE_BLELL_SCAN_NEXT_INSTANT	0x403C103C	Advertising next instant.
BLE_BLELL_INIT_INTERVAL	0x403C1040	Initiator Interval Register
BLE_BLELL_INIT_WINDOW	0x403C1044	Initiator window Register
BLE_BLELL_INIT_PARAM	0x403C1048	Initiator parameters register
BLE_BLELL_INIT_INTR	0x403C1050	Scan interrupt status and Clear register
BLE_BLELL_INIT_NEXT_INSTANT	0x403C1054	Initiator next instant.
BLE_BLELL_DEVICE_RAND_ADDR_L	0x403C1058	Lower 16 bit random address of the device.
BLE_BLELL_DEVICE_RAND_ADDR_M	0x403C105C	Middle 16 bit random address of the device.
BLE_BLELL_DEVICE_RAND_ADDR_H	0x403C1060	Higher 16 bit random address of the device.
BLE_BLELL_PEER_ADDR_L	0x403C1068	Lower 16 bit address of the peer device.
BLE_BLELL_PEER_ADDR_M	0x403C106C	Middle 16 bit address of the peer device.
BLE_BLELL_PEER_ADDR_H	0x403C1070	Higher 16 bit address of the peer device.
BLE_BLELL_WL_ADDR_TYPE	0x403C1078	whitelist address type
BLE_BLELL_WL_ENABLE	0x403C107C	whitelist valid entry bit
BLE_BLELL_TRANSMIT_WINDOW_OFFSET	0x403C1080	Transmit window offset
BLE_BLELL_TRANSMIT_WINDOW_SIZE	0x403C1084	Transmit window size
BLE_BLELL_DATA_CHANNELS_L0	0x403C1088	Data channel map 0 (lower word)
BLE_BLELL_DATA_CHANNELS_M0	0x403C108C	Data channel map 0 (middle word)
BLE_BLELL_DATA_CHANNELS_H0	0x403C1090	Data channel map 0 (upper word)
BLE_BLELL_DATA_CHANNELS_L1	0x403C1098	Data channel map 1 (lower word)
BLE_BLELL_DATA_CHANNELS_M1	0x403C109C	Data channel map 1 (middle word)
BLE_BLELL_DATA_CHANNELS_H1	0x403C10A0	Data channel map 1 (upper word)
BLE_BLELL_CONN_INTR	0x403C10A8	Connection interrupt status and Clear register
BLE_BLELL_CONN_STATUS	0x403C10AC	Connection channel status
BLE_BLELL_CONN_INDEX	0x403C10B0	Connection Index register
BLE_BLELL_WAKEUP_CONFIG	0x403C10B8	Wakeup configuration
BLE_BLELL_WAKEUP_CONTROL	0x403C10C0	Wakeup control
BLE_BLELL_CLOCK_CONFIG	0x403C10C4	Clock control
BLE_BLELL_TIM_COUNTER_L	0x403C10C8	Reference Clock
BLE_BLELL_WAKEUP_CONFIG_EXTD	0x403C10CC	Wakeup configuration extended
BLE_BLELL_POC_REG__TIM_CONTROL	0x403C10D8	BLE Time Control

Register	Address	Description
BLE_BLELL_ADV_TX_DATA_FIFO	0x403C10E0	Advertising data transmit FIFO. Access ADVCH_TX_FIFO.
BLE_BLELL_ADV_SCN_RSP_TX_FIFO	0x403C10E8	Advertising scan response data transmit FIFO. Access ADVCH_TX-_FIFO.
BLE_BLELL_INIT_SCN_ADV_RX_FIFO	0x403C10F8	advertising scan response data receive data FIFO. Access ADVRX-_FIFO.
BLE_BLELL_CONN_INTERVAL	0x403C1100	Connection Interval
BLE_BLELL_SUP_TIMEOUT	0x403C1104	Supervision timeout
BLE_BLELL_SLAVE_LATENCY	0x403C1108	Slave Latency
BLE_BLELL_CE_LENGTH	0x403C110C	Connection event length
BLE_BLELL_PDU_ACCESS_ADDR_L_REGISTER	0x403C1110	Access address (lower)
BLE_BLELL_PDU_ACCESS_ADDR_H_REGISTER	0x403C1114	Access address (upper)
BLE_BLELL_CONN_CE_INSTANT	0x403C1118	Connection event instant
BLE_BLELL_CE_CNFG_STS_REGISTER	0x403C111C	connection configuration & status register
BLE_BLELL_NEXT_CE_INSTANT	0x403C1120	Next connection event instant
BLE_BLELL_CONN_CE_COUNTER	0x403C1124	connection event counter
BLE_BLELL_DATA_LIST_SENT_UPDATE__STATUS	0x403C1128	data list sent update and status
BLE_BLELL_DATA_LIST_ACK_UPDATE__STATUS	0x403C112C	data list ack update and status
BLE_BLELL_CE_CNFG_STS_REGISTER_EXT	0x403C1130	connection configuration & status register
BLE_BLELL_CONN_EXT_INTR	0x403C1134	Connection extended interrupt status and Clear register
BLE_BLELL_CONN_EXT_INTR_MASK	0x403C1138	Connection Extended Interrupt mask
BLE_BLELL_DATA_MEM_DESCRIPTOR0	0x403C1140	Data buffer descriptor 0 to 4
BLE_BLELL_DATA_MEM_DESCRIPTOR1	0x403C1144	Data buffer descriptor 0 to 4. See BLE_BLELL_DATA_MEM_DESCRIPTOR0 for the details of bit fields.
BLE_BLELL_DATA_MEM_DESCRIPTOR2	0x403C1148	Data buffer descriptor 0 to 4. See BLE_BLELL_DATA_MEM_DESCRIPTOR0 for the details of bit fields.
BLE_BLELL_DATA_MEM_DESCRIPTOR3	0x403C114C	Data buffer descriptor 0 to 4. See BLE_BLELL_DATA_MEM_DESCRIPTOR0 for the details of bit fields.
BLE_BLELL_DATA_MEM_DESCRIPTOR4	0x403C1150	Data buffer descriptor 0 to 4. See BLE_BLELL_DATA_MEM_DESCRIPTOR0 for the details of bit fields.
BLE_BLELL_WINDOW_WIDEN_INTVL	0x403C1160	Window widen for interval
BLE_BLELL_WINDOW_WIDEN_WINOFF	0x403C1164	Window widen for offset
BLE_BLELL_LE_RF_TEST_MODE	0x403C1170	Direct Test Mode control
BLE_BLELL_DTM_RX_PKT_COUNT	0x403C1174	Direct Test Mode receive packet count
BLE_BLELL_LE_RF_TEST_MODE_EXT	0x403C1178	Direct Test Mode control
BLE_BLELL_TXRX_HOP	0x403C1188	Channel Address register
BLE_BLELL_TX_RX_ON_DELAY	0x403C1190	Transmit/Receive data delay
BLE_BLELL_ADV_ACCADDR_L	0x403C11A8	ADV packet access code low word
BLE_BLELL_ADV_ACCADDR_H	0x403C11AC	ADV packet access code high word
BLE_BLELL_ADV_CH_TX_POWER_LVL_LS	0x403C11B0	Advertising channel transmit power setting
BLE_BLELL_ADV_CH_TX_POWER_LVL_MS	0x403C11B4	Advertising channel transmit power setting extension
BLE_BLELL_CONN_CH_TX_POWER_LVL_LS	0x403C11B8	Connection channel transmit power setting
BLE_BLELL_CONN_CH_TX_POWER_LVL_MS	0x403C11BC	Connection channel transmit power setting extension
BLE_BLELL_DEV_PUB_ADDR_L	0x403C11C0	Device public address lower register
BLE_BLELL_DEV_PUB_ADDR_M	0x403C11C4	Device public address middle register
BLE_BLELL_DEV_PUB_ADDR_H	0x403C11C8	Device public address higher register
BLE_BLELL_OFFSET_TO_FIRST_INSTANT	0x403C11D0	Offset to first instant

Register	Address	Description
BLE_BLELL_ADV_CONFIG	0x403C11D4	Advertiser configuration register
BLE_BLELL_SCAN_CONFIG	0x403C11D8	Scan configuration register
BLE_BLELL_INIT_CONFIG	0x403C11DC	Initiator configuration register
BLE_BLELL_CONN_CONFIG	0x403C11E0	Connection configuration register
BLE_BLELL_CONN_PARAM1	0x403C11E8	Connection parameter 1
BLE_BLELL_CONN_PARAM2	0x403C11EC	Connection parameter 2
BLE_BLELL_CONN_EXT_INTR_MASK	0x403C11F0	Connection Interrupt mask
BLE_BLELL_SLAVE_TIMING_CONTROL	0x403C11F4	slave timing control
BLE_BLELL_RECEIVE_TRIG_CTRL	0x403C11F8	Receive trigger control
BLE_BLELL_LL_DBG_1	0x403C1200	LL debug register 1
BLE_BLELL_LL_DBG_2	0x403C1204	LL debug register 2
BLE_BLELL_LL_DBG_3	0x403C1208	LL debug register 3
BLE_BLELL_LL_DBG_4	0x403C120C	LL debug register 4
BLE_BLELL_LL_DBG_5	0x403C1210	LL debug register 5
BLE_BLELL_LL_DBG_6	0x403C1214	LL debug register 6
BLE_BLELL_LL_DBG_7	0x403C1218	LL debug register 7
BLE_BLELL_LL_DBG_8	0x403C121C	LL debug register 8
BLE_BLELL_LL_DBG_9	0x403C1220	LL debug register 9
BLE_BLELL_LL_DBG_10	0x403C1224	LL debug register 10
BLE_BLELL_PEER_ADDR_INIT_L	0x403C1230	Lower 16 bit address of the peer device for INIT.
BLE_BLELL_PEER_ADDR_INIT_M	0x403C1234	Middle 16 bit address of the peer device for INIT.
BLE_BLELL_PEER_ADDR_INIT_H	0x403C1238	Higher 16 bit address of the peer device for INIT.
BLE_BLELL_PEER_SEC_ADDR_ADV_L	0x403C123C	Lower 16 bits of the secondary address of the peer device for ADV_DIR.
BLE_BLELL_PEER_SEC_ADDR_ADV_M	0x403C1240	Middle 16 bits of the secondary address of the peer device for ADV_DIR.
BLE_BLELL_PEER_SEC_ADDR_ADV_H	0x403C1244	Higher 16 bits of the secondary address of the peer device for ADV_DIR.
BLE_BLELL_INIT_WINDOW_TIMER_CTRL	0x403C1248	Initiator Window NI timer control
BLE_BLELL_CONN_CONFIG_EXT	0x403C124C	Connection extended configuration register
BLE_BLELL_DPLL_CONFIG	0x403C1258	DPLL & CY Correlator configuration register
BLE_BLELL_INIT_NI_VAL	0x403C1260	Initiator Window NI instant
BLE_BLELL_TRANSMIT_WINDOW_OFFSET	0x403C1264	Initiator Window offset captured at conn request
BLE_BLELL_INIT_WINDOW_NI_ANCHOR_PT	0x403C1268	Initiator Window NI anchor point captured at conn request
BLE_BLELL_CONN_UPDATE_NEW_INTERVAL	0x403C13A4	Connection update new interval
BLE_BLELL_CONN_UPDATE_NEW_LATENCY	0x403C13A8	Connection update new latency
BLE_BLELL_CONN_UPDATE_NEW_SUP_TO	0x403C13AC	Connection update new supervision timeout
BLE_BLELL_CONN_UPDATE_NEW_SL_INTERVAL	0x403C13B0	Connection update new Slave Latency X Conn interval Value
BLE_BLELL_CONN_REQ_WORD0	0x403C13C0	Connection request address word 0
BLE_BLELL_CONN_REQ_WORD1	0x403C13C4	Connection request address word 1
BLE_BLELL_CONN_REQ_WORD2	0x403C13C8	Connection request address word 2
BLE_BLELL_CONN_REQ_WORD3	0x403C13CC	Connection request address word 3
BLE_BLELL_CONN_REQ_WORD4	0x403C13D0	Connection request address word 4
BLE_BLELL_CONN_REQ_WORD5	0x403C13D4	Connection request address word 5
BLE_BLELL_CONN_REQ_WORD6	0x403C13D8	Connection request address word 6

Register	Address	Description
BLE_BLELL_CONN_REQ_WORD7	0x403C13DC	Connection request address word 7
BLE_BLELL_CONN_REQ_WORD8	0x403C13E0	Connection request address word 8
BLE_BLELL_CONN_REQ_WORD9	0x403C13E4	Connection request address word 9
BLE_BLELL_CONN_REQ_WORD10	0x403C13E8	Connection request address word 10
BLE_BLELL_CONN_REQ_WORD11	0x403C13EC	Connection request address word 11
BLE_BLELL_PDU_RESP_TIMER	0x403C1A04	PDU response timer/Generic Timer (MMMS mode)
BLE_BLELL_NEXT_RESP_TIMER_EXP	0x403C1A08	Next response timeout instant
BLE_BLELL_NEXT_SUP_TO	0x403C1A0C	Next supervision timeout instant
BLE_BLELL_LLH_FEATURE_CONFIG	0x403C1A10	Feature enable
BLE_BLELL_WIN_MIN_STEP_SIZE	0x403C1A14	Window minimum step size
BLE_BLELL_SLV_WIN_ADJ	0x403C1A18	Slave window adjustment
BLE_BLELL_SL_CONN_INTERVAL	0x403C1A1C	Slave Latency X Conn Interval Value
BLE_BLELL_LE_PING_TIMER_ADDR	0x403C1A20	LE Ping connection timer address
BLE_BLELL_LE_PING_TIMER_OFFSET	0x403C1A24	LE Ping connection timer offset
BLE_BLELL_LE_PING_TIMER_NEXT_EXP	0x403C1A28	LE Ping timer next expiry instant
BLE_BLELL_LE_PING_TIMER_WRAP_COUNT	0x403C1A2C	LE Ping Timer wrap count
BLE_BLELL_TX_EN_EXT_DELAY	0x403C1E00	Transmit enable extension delay
BLE_BLELL_TX_RX_SYNTH_DELAY	0x403C1E04	Transmit/Receive enable delay
BLE_BLELL_EXT_PA_LNA_DLY_CNFG	0x403C1E08	External TX PA and RX LNA delay configuration
BLE_BLELL_LL_CONFIG	0x403C1E10	Link Layer additional configuration
BLE_BLELL_LL_CONTROL	0x403C1F00	LL Backward compatibility
BLE_BLELL_DEV_PA_ADDR_L	0x403C1F04	Device Resolvable/Non-Resolvable Private address lower register
BLE_BLELL_DEV_PA_ADDR_M	0x403C1F08	Device Resolvable/Non-Resolvable Private address middle register
BLE_BLELL_DEV_PA_ADDR_H	0x403C1F0C	Device Resolvable/Non-Resolvable Private address higher register
BLE_BLELL_RSLV_LIST_ENABLE0	0x403C1F10	Resolving list entry control bit
BLE_BLELL_RSLV_LIST_ENABLE1	0x403C1F14	Resolving list entry control bit. See BLE_BLELL_RSLV_LIST_ENABLE0 for the details of bit fields.
BLE_BLELL_RSLV_LIST_ENABLE2	0x403C1F18	Resolving list entry control bit. See BLE_BLELL_RSLV_LIST_ENABLE0 for the details of bit fields.
BLE_BLELL_RSLV_LIST_ENABLE3	0x403C1F1C	Resolving list entry control bit. See BLE_BLELL_RSLV_LIST_ENABLE0 for the details of bit fields.
BLE_BLELL_RSLV_LIST_ENABLE4	0x403C1F20	Resolving list entry control bit. See BLE_BLELL_RSLV_LIST_ENABLE0 for the details of bit fields.
BLE_BLELL_RSLV_LIST_ENABLE5	0x403C1F24	Resolving list entry control bit. See BLE_BLELL_RSLV_LIST_ENABLE0 for the details of bit fields.
BLE_BLELL_RSLV_LIST_ENABLE6	0x403C1F28	Resolving list entry control bit. See BLE_BLELL_RSLV_LIST_ENABLE0 for the details of bit fields.
BLE_BLELL_RSLV_LIST_ENABLE7	0x403C1F2C	Resolving list entry control bit. See BLE_BLELL_RSLV_LIST_ENABLE0 for the details of bit fields.
BLE_BLELL_RSLV_LIST_ENABLE8	0x403C1F30	Resolving list entry control bit. See BLE_BLELL_RSLV_LIST_ENABLE0 for the details of bit fields.
BLE_BLELL_RSLV_LIST_ENABLE9	0x403C1F34	Resolving list entry control bit. See BLE_BLELL_RSLV_LIST_ENABLE0 for the details of bit fields.
BLE_BLELL_RSLV_LIST_ENABLE10	0x403C1F38	Resolving list entry control bit. See BLE_BLELL_RSLV_LIST_ENABLE0 for the details of bit fields.
BLE_BLELL_RSLV_LIST_ENABLE11	0x403C1F3C	Resolving list entry control bit. See BLE_BLELL_RSLV_LIST_ENABLE0 for the details of bit fields.
BLE_BLELL_RSLV_LIST_ENABLE12	0x403C1F40	Resolving list entry control bit. See BLE_BLELL_RSLV_LIST_ENABLE0 for the details of bit fields.

Register	Address	Description
BLE_BLELL_RSLV_LIST_ENABLE13	0x403C1F44	Resolving list entry control bit. See BLE_BLELL_RSLV_LIST_ENABLE0 for the details of bit fields.
BLE_BLELL_RSLV_LIST_ENABLE14	0x403C1F48	Resolving list entry control bit. See BLE_BLELL_RSLV_LIST_ENABLE0 for the details of bit fields.
BLE_BLELL_RSLV_LIST_ENABLE15	0x403C1F4C	Resolving list entry control bit. See BLE_BLELL_RSLV_LIST_ENABLE0 for the details of bit fields.
BLE_BLELL_WL_CONNECTION_STATUS	0x403C1FA0	whitelist valid entry bit
BLE_BLELL_CONN_RXMEM_BASE_ADDR_DLE	0x403C2800	DLE Connection RX memory base address
BLE_BLELL_CONN_TXMEM_BASE_ADDR_DLE	0x403C3800	DLE Connection TX memory base address
BLE_BLELL_CONN_1_PARAM_MEM_BASE_ADDR	0x403D3800	Connection Parameter memory base address for connection 1
BLE_BLELL_CONN_2_PARAM_MEM_BASE_ADDR	0x403D3880	Connection Parameter memory base address for connection 2
BLE_BLELL_CONN_3_PARAM_MEM_BASE_ADDR	0x403D3900	Connection Parameter memory base address for connection 3
BLE_BLELL_CONN_4_PARAM_MEM_BASE_ADDR	0x403D3980	Connection Parameter memory base address for connection 4
BLE_BLELL_NI_TIMER	0x403D5000	Next Instant Timer
BLE_BLELL_US_OFFSET	0x403D5004	Micro-second Offset
BLE_BLELL_NEXT_CONN	0x403D5008	Next Connection
BLE_BLELL_NI_ABORT	0x403D500C	Abort next scheduled connection
BLE_BLELL_CONN_NI_STATUS	0x403D5020	Connection NI Status
BLE_BLELL_NEXT_SUP_TO_STATUS	0x403D5024	Next Supervision timeout Status
BLE_BLELL_MMMS_CONN_STATUS	0x403D5028	Connection Status
BLE_BLELL_BT_SLOT_CAPT_STATUS	0x403D502C	BT Slot Captured Status
BLE_BLELL_US_CAPT_STATUS	0x403D5030	Micro-second Capture Status
BLE_BLELL_US_OFFSET_STATUS	0x403D5034	Micro-second Offset Status
BLE_BLELL_ACCU_WINDOW_WIDEN_STATUS	0x403D5038	Accumulated Window Widen Status
BLE_BLELL_EARLY_INTR_STATUS	0x403D503C	Status when early interrupt is raised
BLE_BLELL_MMMS_CONFIG	0x403D5040	Multi-Master Multi-Slave Config
BLE_BLELL_US_COUNTER	0x403D5044	Running US of the current BT Slot
BLE_BLELL_US_CAPT_PREV	0x403D5048	Previous captured US of the BT Slot
BLE_BLELL_EARLY_INTR_NI	0x403D504C	NI at early interrupt
BLE_BLELL_MMMS_MASTER_CREATE_BT_CAPT	0x403D5080	BT slot capture for master connection creation
BLE_BLELL_MMMS_SLAVE_CREATE_BT_CAPT	0x403D5084	BT slot capture for slave connection creation
BLE_BLELL_MMMS_SLAVE_CREATE_US_CAPT	0x403D5088	Micro second capture for slave connection creation
BLE_BLELL_MMMS_DATA_MEM_DESCRIPTOR0	0x403D5100	Data buffer descriptor 0 to 15
BLE_BLELL_MMMS_DATA_MEM_DESCRIPTOR1	0x403D5104	Data buffer descriptor 0 to 15. See BLE_BLELL_MMMS_DATA_MEM_-DESCRIPTOR0 for the details of bit fields.
BLE_BLELL_MMMS_DATA_MEM_DESCRIPTOR2	0x403D5108	Data buffer descriptor 0 to 15. See BLE_BLELL_MMMS_DATA_MEM_-DESCRIPTOR0 for the details of bit fields.
BLE_BLELL_MMMS_DATA_MEM_DESCRIPTOR3	0x403D510C	Data buffer descriptor 0 to 15. See BLE_BLELL_MMMS_DATA_MEM_-DESCRIPTOR0 for the details of bit fields.
BLE_BLELL_MMMS_DATA_MEM_DESCRIPTOR4	0x403D5110	Data buffer descriptor 0 to 15. See BLE_BLELL_MMMS_DATA_MEM_-DESCRIPTOR0 for the details of bit fields.
BLE_BLELL_MMMS_DATA_MEM_DESCRIPTOR5	0x403D5114	Data buffer descriptor 0 to 15. See BLE_BLELL_MMMS_DATA_MEM_-DESCRIPTOR0 for the details of bit fields.
BLE_BLELL_MMMS_DATA_MEM_DESCRIPTOR6	0x403D5118	Data buffer descriptor 0 to 15. See BLE_BLELL_MMMS_DATA_MEM_-DESCRIPTOR0 for the details of bit fields.
BLE_BLELL_MMMS_DATA_MEM_DESCRIPTOR7	0x403D511C	Data buffer descriptor 0 to 15. See BLE_BLELL_MMMS_DATA_MEM_-DESCRIPTOR0 for the details of bit fields.

Register	Address	Description
BLE_BLELL_MMMS_DATA_MEM_DESCRIPTOR8	0x403D5120	Data buffer descriptor 0 to 15. See BLE_BLELL_MMMS_DATA_MEM_-DESCRIPTOR0 for the details of bit fields.
BLE_BLELL_MMMS_DATA_MEM_DESCRIPTOR9	0x403D5124	Data buffer descriptor 0 to 15. See BLE_BLELL_MMMS_DATA_MEM_-DESCRIPTOR0 for the details of bit fields.
BLE_BLELL_MMMS_DATA_MEM_DESCRIPTOR10	0x403D5128	Data buffer descriptor 0 to 15. See BLE_BLELL_MMMS_DATA_MEM_-DESCRIPTOR0 for the details of bit fields.
BLE_BLELL_MMMS_DATA_MEM_DESCRIPTOR11	0x403D512C	Data buffer descriptor 0 to 15. See BLE_BLELL_MMMS_DATA_MEM_-DESCRIPTOR0 for the details of bit fields.
BLE_BLELL_MMMS_DATA_MEM_DESCRIPTOR12	0x403D5130	Data buffer descriptor 0 to 15. See BLE_BLELL_MMMS_DATA_MEM_-DESCRIPTOR0 for the details of bit fields.
BLE_BLELL_MMMS_DATA_MEM_DESCRIPTOR13	0x403D5134	Data buffer descriptor 0 to 15. See BLE_BLELL_MMMS_DATA_MEM_-DESCRIPTOR0 for the details of bit fields.
BLE_BLELL_MMMS_DATA_MEM_DESCRIPTOR14	0x403D5138	Data buffer descriptor 0 to 15. See BLE_BLELL_MMMS_DATA_MEM_-DESCRIPTOR0 for the details of bit fields.
BLE_BLELL_MMMS_DATA_MEM_DESCRIPTOR15	0x403D513C	Data buffer descriptor 0 to 15. See BLE_BLELL_MMMS_DATA_MEM_-DESCRIPTOR0 for the details of bit fields.
BLE_BLELL_CONN_1_DATA_LIST_SENT	0x403D5200	data list sent update and status for connection 1
BLE_BLELL_CONN_1_DATA_LIST_ACK	0x403D5204	data list ack update and status for connection 1
BLE_BLELL_CONN_1_CE_DATA_LIST_CFG	0x403D5208	Connection specific pause resume for connection 1
BLE_BLELL_CONN_2_DATA_LIST_SENT	0x403D5210	data list sent update and status for connection 2
BLE_BLELL_CONN_2_DATA_LIST_ACK	0x403D5214	data list ack update and status for connection 2
BLE_BLELL_CONN_2_CE_DATA_LIST_CFG	0x403D5218	Connection specific pause resume for connection 2
BLE_BLELL_CONN_3_DATA_LIST_SENT	0x403D5220	data list sent update and status for connection 3
BLE_BLELL_CONN_3_DATA_LIST_ACK	0x403D5224	data list ack update and status for connection 3
BLE_BLELL_CONN_3_CE_DATA_LIST_CFG	0x403D5228	Connection specific pause resume for connection 3
BLE_BLELL_CONN_4_DATA_LIST_SENT	0x403D5230	data list sent update and status for connection 4
BLE_BLELL_CONN_4_DATA_LIST_ACK	0x403D5234	data list ack update and status for connection 4
BLE_BLELL_CONN_4_CE_DATA_LIST_CFG	0x403D5238	Connection specific pause resume for connection 4
BLE_BLELL_MMMS_ADVCH_NI_ENABLE	0x403D5400	Enable bits for ADV_NI, SCAN_NI and INIT_NI
BLE_BLELL_MMMS_ADVCH_NI_VALID	0x403D5404	Next instant valid for ADV, SCAN, INIT
BLE_BLELL_MMMS_ADVCH_NI_ABORT	0x403D5408	Abort the next instant of ADV, SCAN, INIT
BLE_BLELL_CONN_PARAM_NEXT_SUP_TO	0x403D5410	Register to configure the supervision timeout for next scheduled connec-tion
BLE_BLELL_CONN_PARAM_ACC_WIN_WIDEN	0x403D5414	Register to configure Accumulated window widening for next scheduled connection
BLE_BLELL_HW_LOAD_OFFSET	0x403D5420	Register to configure offset from connection anchor point at which con-nection parameter memory should be read
BLE_BLELL_ADV_RAND	0x403D5424	Random number generated by Hardware for ADV NI calculation
BLE_BLELL_MMMS_RX_PKT_CNTR	0x403D5428	Packet Counter of packets in RX FIFO in MMMS mode
BLE_BLELL_CONN_RX_PKT_CNTR0	0x403D5430	Packet Counter for Individual connection index
BLE_BLELL_CONN_RX_PKT_CNTR1	0x403D5434	Packet Counter for Individual connection index. See BLE_BLELL_CON-N_RX_PKT_CNTR0 for the details of bit fields.
BLE_BLELL_CONN_RX_PKT_CNTR2	0x403D5438	Packet Counter for Individual connection index. See BLE_BLELL_CON-N_RX_PKT_CNTR0 for the details of bit fields.
BLE_BLELL_CONN_RX_PKT_CNTR3	0x403D543C	Packet Counter for Individual connection index. See BLE_BLELL_CON-N_RX_PKT_CNTR0 for the details of bit fields.
BLE_BLELL_CONN_RX_PKT_CNTR4	0x403D5440	Packet Counter for Individual connection index. See BLE_BLELL_CON-N_RX_PKT_CNTR0 for the details of bit fields.
BLE_BLELL_CONN_RX_PKT_CNTR5	0x403D5444	Packet Counter for Individual connection index. See BLE_BLELL_CON-N_RX_PKT_CNTR0 for the details of bit fields.

Register	Address	Description
BLE_BLELL_CONN_RX_PKT_CNTR6	0x403D5448	Packet Counter for Individual connection index. See BLE_BLELL_CONN_RX_PKT_CNTR0 for the details of bit fields.
BLE_BLELL_CONN_RX_PKT_CNTR7	0x403D544C	Packet Counter for Individual connection index. See BLE_BLELL_CONN_RX_PKT_CNTR0 for the details of bit fields.
BLE_BLELL_WHITELIST_BASE_ADDR	0x403D5800	Whitelist base address
BLE_BLELL_RSLV_LIST_PEER_IDNTT_BASE_ADDR	0x403D58C0	Resolving list base address for storing Peer Identity address
BLE_BLELL_RSLV_LIST_PEER_RPA_BASE_ADDR	0x403D5980	Resolving list base address for storing resolved Peer RPA address
BLE_BLELL_RSLV_LIST_RCVD_INIT_RPA_BASE_ADDR	0x403D5A40	Resolving list base address for storing Resolved received INITA RPA
BLE_BLELL_RSLV_LIST_TX_INIT_RPA_BASE_ADDR	0x403D5B00	Resolving list base address for storing generated TX INITA RPA
BLE_BLESS_XTAL_CLK_DIV_CONFIG	0x403DF064	Crystal clock divider configuration register
BLE_BLESS_INTR_STAT	0x403DF068	Link Layer interrupt status register
BLE_BLESS_INTR_MASK	0x403DF06C	Link Layer interrupt mask register
BLE_BLESS_LL_CLK_EN	0x403DF070	Link Layer primary clock enable
BLE_BLESS_LF_CLK_CTRL	0x403DF074	BLESS LF clock control and BLESS revision ID indicator
BLE_BLESS_EXT_PA_LNA_CTRL	0x403DF078	External TX PA and RX LNA control
BLE_BLESS_LL_PKT_RSSI_CH_ENERGY	0x403DF080	Link Layer Last Received packet RSSI/Channel energy and channel number
BLE_BLESS_BT_CLOCK_CAPT	0x403DF084	BT clock captured on an LL DSM exit
BLE_BLESS_MT_CFG	0x403DF0A0	MT Configuration Register
BLE_BLESS_MT_DELAY_CFG	0x403DF0A4	MT Delay configuration for state transitions
BLE_BLESS_MT_DELAY_CFG2	0x403DF0A8	MT Delay configuration for state transitions
BLE_BLESS_MT_DELAY_CFG3	0x403DF0AC	MT Delay configuration for state transitions
BLE_BLESS_MT_VIO_CTRL	0x403DF0B0	MT Configuration Register to control VIO switches
BLE_BLESS_MT_STATUS	0x403DF0B4	MT Status Register
BLE_BLESS_PWR_CTRL_SM_ST	0x403DF0B8	Link Layer Power Control FSM Status Register
BLE_BLESS_HVLDO_CTRL	0x403DF0C0	HVLDO Configuration register
BLE_BLESS_MISC_EN_CTRL	0x403DF0C4	Radio Buck and Active regulator enable control
BLE_BLESS_EFUSE_CONFIG	0x403DF0D0	EFUSE mode configuration register
BLE_BLESS_EFUSE_TIM_CTRL1	0x403DF0D4	EFUSE timing control register (common for Program and Read modes)
BLE_BLESS_EFUSE_TIM_CTRL2	0x403DF0D8	EFUSE timing control Register (for Read)
BLE_BLESS_EFUSE_TIM_CTRL3	0x403DF0DC	EFUSE timing control Register (for Program)
BLE_BLESS_EFUSE_RDATA_L	0x403DF0E0	EFUSE Lower read data

Register	Address	Description
BLE_BLESS_EFUSE_RDATA_H	0x403DF0E4	EFUSE higher read data
BLE_BLESS_EFUSE_WDATA_L	0x403DF0E8	EFUSE lower write word
BLE_BLESS_EFUSE_WDATA_H	0x403DF0EC	EFUSE higher write word
BLE_BLESS_DIV_BY_625_CFG	0x403DF0F0	Divide by 625 for FW Use
BLE_BLESS_DIV_BY_625_STS	0x403DF0F4	Output of divide by 625 divider
BLE_BLESS_PACKET_COUNTER0	0x403DF100	Packet counter 0
BLE_BLESS_PACKET_COUNTER2	0x403DF104	Packet counter 2
BLE_BLESS_IV_MASTER0	0x403DF108	Master Initialization Vector 0
BLE_BLESS_IV_SLAVE0	0x403DF10C	Slave Initialization Vector 0
BLE_BLESS_ENC_KEY0	0x403DF110	Encryption Key register 0-3
BLE_BLESS_ENC_KEY1	0x403DF114	Encryption Key register 0-3. See BLE_BLESS_ENC_KEY0 for the details of bit fields.
BLE_BLESS_ENC_KEY2	0x403DF118	Encryption Key register 0-3. See BLE_BLESS_ENC_KEY0 for the details of bit fields.
BLE_BLESS_ENC_KEY3	0x403DF11C	Encryption Key register 0-3. See BLE_BLESS_ENC_KEY0 for the details of bit fields.
BLE_BLESS_MIC_IN0	0x403DF120	MIC input register
BLE_BLESS_MIC_OUT0	0x403DF124	MIC output register
BLE_BLESS_ENC_PARAMS	0x403DF128	Encryption Parameter register
BLE_BLESS_ENC_CONFIG	0x403DF12C	Encryption Configuration
BLE_BLESS_ENC_INTR_EN	0x403DF130	Encryption Interrupt enable
BLE_BLESS_ENC_INTR	0x403DF134	Encryption Interrupt status and clear register
BLE_BLESS_B1_DATA_REG0	0x403DF140	Programmable B1 Data register (0-3)
BLE_BLESS_B1_DATA_REG1	0x403DF144	Programmable B1 Data register (0-3). See BLE_BLESS_B1_-DATA_REG0 for the details of bit fields.
BLE_BLESS_B1_DATA_REG2	0x403DF148	Programmable B1 Data register (0-3). See BLE_BLESS_B1_-DATA_REG0 for the details of bit fields.
BLE_BLESS_B1_DATA_REG3	0x403DF14C	Programmable B1 Data register (0-3). See BLE_BLESS_B1_-DATA_REG0 for the details of bit fields.
BLE_BLESS_ENC_MEM_BASE_ADDR	0x403DF150	Encryption memory base address
BLE_BLESS_TRIM_LDO_0	0x403DFF00	LDO Trim register 0
BLE_BLESS_TRIM_LDO_1	0x403DFF04	LDO Trim register 1
BLE_BLESS_TRIM_LDO_2	0x403DFF08	LDO Trim register 2
BLE_BLESS_TRIM_LDO_3	0x403DFF0C	LDO Trim register 3
BLE_BLESS_TRIM_MXD0	0x403DFF10	MXD die Trim registers

Register	Address	Description
BLE_BLESS_TRIM_MXD1	0x403DFF14	MXD die Trim registers. See BLE_BLESS_TRIM_MXD0 for the details of bit fields.
BLE_BLESS_TRIM_MXD2	0x403DFF18	MXD die Trim registers. See BLE_BLESS_TRIM_MXD0 for the details of bit fields.
BLE_BLESS_TRIM_MXD3	0x403DFF1C	MXD die Trim registers. See BLE_BLESS_TRIM_MXD0 for the details of bit fields.
BLE_BLESS_TRIM_LDO_4	0x403DFF30	LDO Trim register 4
BLE_BLESS_TRIM_LDO_5	0x403DFF34	LDO Trim register 5

22.1.1 BLE_RCB_CTRL

RCB control register.

Address: 0x403C0000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	RW	RW	RW	None
HW Access	None		R	R	R	R	R	None
Name	None [7:6]		SSEL_POLARITY	SCLK_CONTINUOUS	RX_CLK_SRC	RX_CLK_EDGE	TX_CLK_EDGE	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW	RW		RW	
HW Access	R			R	R		R	
Name	DIV [15:13]			DIV_ENABLED	LAG [11:10]		LEAD [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW				RW		
HW Access	R	R				R		
Name	DATA_WIDTH	ADDR_WIDTH [22:19]				DIV [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	ENABLED	None [30:24]						

Bits	Name	Description
31	ENABLED	IP enabled ('1') or not ('0'). The proper order in which to initialize the IP is as follows: - Program protocol specific information using CTRL except ENABLED field. - Program generic transmitter (TX_CTRL) and receiver (RX_CTRL) information. This includes enabling of the transmitter and receiver functionality. - Program transmitter FIFO (TX_FIFO_CTRL) and receiver FIFO (RX_FIFO_CTRL) information. - Program CTRL to enable IP. When the IP is enabled, no control information should be changed. Changes should be made AFTER disabling the IP, e.g. to modify the edges, dividers. The change takes effect after the IP is re-enabled. Note that disabling the IP will cause re-initialization of the design and associated state is lost (e.g. FIFO content). Default Value: 0
23	DATA_WIDTH	Width of Data phase of the transmit Dataframe width. 0 - 8 bits 1 - 16 bits Default Value: 1

22.1.1 BLE_RCB_CTRL (continued)

22 : 19	ADDR_WIDTH	Width of Address phase (includes read/write mode bit) of the Dataframe width. ADDR_WIDTH + 1 is the amount of bits in a transmitted data frame. Allowed legal values are 'd8, 'd10 and 'd15 Default Value: 15
18 : 13	DIV	The internal core clock divider factor when DIV_ENABLED=1 Divider factor: 2*DIV. Max DIV value supported is 31. DIV value of zero is not supported. Make DIV_ENABLED=0 for undivided clock Default Value: 0
12	DIV_ENABLED	Enable for RCB Clock Divider. The internal core clock divider is bypassed when DIV_ENABLED=0 Default Value: 0
11 : 10	LAG	SCLK-SSEL lag time. Indicates the time for which SSN needs to remain asserted after the last SCLK cycle including zero. Allowed values are 0,1,2. 3 is Reserved. Lag = LAG (TX_CLK_EDGE=0) LAG +0.5 (TX_CLK_EDGE=1) Default Value: 0
9 : 8	LEAD	SSEL-SCLK lead time.Indicates the time for which SSN needs to remain asserted before the first SCLK cycle. Allowed values are 0,1,2. 3 is Reserved. Lead = LEAD + 0.5 (TX_CLK_EDGE =0) LEAD + 1 (TX_CLK_EDGE =1) Default Value: 0
5	SSEL_POLARITY	Slave select polarity. SSEL_POLARITY applies to the outgoing slave select signal '0': slave select is low/'0' active. '1': slave select is high/'1' active. Default Value: 0
4	SCLK_CONTINUOUS	Controls the behaviour of the RCB clock '0': SCLK is generated, only when the RCB controller is enabled and data is transmitted. '1': SCLK is generated, when the RCB controller is enabled. Default Value: 0
3	RX_CLK_SRC	Clock to be used for sampling the received data 0: Internal clock (Default) 1: Clock from the SCK pad When Clock from the SCK pad is used, sampling is always on negedge only Default Value: 0
2	RX_CLK_EDGE	Clock edge used for sampling the received data (Sampling uses clock selected by RX_CLK_S-RC) 0: Negative Edge (Default) 1: Positive Edge Note: For RX_CLK_SRC =1, when pad clock is used as sampling clock, this field is ignored Default Value: 0
1	TX_CLK_EDGE	Clock edge used for transmitting (Transmision uses internal core clock) 0: Negative Edge (Default) 1: Positive Edge Default Value: 0

22.1.2 BLE_RCB_STATUS

RCB status register.

Address: 0x403C0004

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							W
Name	None [7:1]							BUS_BUSY

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	BUS_BUSY	RCB bus is busy. The bus is considered busy ('1') during an ongoing transaction. Default Value: Undefined

22.1.3 BLE_RCB_TX_CTRL

Transmitter control register.

Address: 0x403C0010

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW					RW	RW
HW Access	None	R					R	R
Name	None	TX_ENTRIES [6:2]					FIFO_RE-CONFIG	MSB_-FIRST

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
6 : 2	TX_ENTRIES	This field determines the depth of the TX_FIFO. Allowed legal values are 8 and 16 only Default Value: 8
1	FIFO_RECONFIG	Setting this bit, clears the FIFO and resets the pointer Default Value: 0
0	MSB_FIRST	Least significant bit first ('0') or most significant bit first ('1'). This field also affects the Address field When MSB_FIRST = 1, then [15:0] is data and [(ADDR_WIDTH+15):16] is used for address When MSB_FIRST = 0, then [15:0] is for data. No address field Default Value: 1

22.1.4 BLE_RCB_TX_FIFO_CTRL

Transmitter FIFO control register.

Address: 0x403C0014

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			R				
Name	None [7:5]			TX_TRIGGER_LEVEL [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							CLEAR

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
16	CLEAR	When '1', the transmitter FIFO and transmitter shift register are cleared/invalidated. Invalidation will last for as long as this field is '1'. If a quick clear/invalidation is required, the field should be set to '1' and be followed by a set to '0'. If a clear/invalidation is required for an extended time period, the field should be set to '1' during the complete time period. Default Value: 0
4 : 0	TX_TRIGGER_LEVEL	Trigger level. When the transmitter FIFO has less entries than the number of this field, a transmitter trigger event is generated. Default Value: 0

22.1.5 BLE_RCB_TX_FIFO_STATUS

Transmitter FIFO status register.

Address: 0x403C0018

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			R				
HW Access	None			W				
Name	None [7:5]			USED [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	R	None						
HW Access	W	None						
Name	SR_VALID	None [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	None				R			
HW Access	None				W			
Name	None [23:20]				RD_PTR [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None				R			
HW Access	None				W			
Name	None [31:28]				WR_PTR [27:24]			

Bits	Name	Description
27 : 24	WR_PTR	FIFO write pointer: FIFO location at which a new data frame is written. Default Value: 0
19 : 16	RD_PTR	FIFO read pointer: FIFO location from which a data frame is read by the hardware. Default Value: 0
15	SR_VALID	Indicates whether the TX shift registers holds a valid data frame ('1') or not ('0'). The shift register can be considered the top of the TX FIFO (the data frame is not included in the USED field of the TX FIFO). The shift register is a working register and holds the data frame that is currently transmitted (when the protocol state machine is transmitting a data frame) or the data frame that is tranmitted next (when the protocol state machine is not transmitting a data frame). Default Value: 0
4 : 0	USED	Amount of enties in the transmitter FIFO. The value of this field ranges from 0 to 16 Default Value: 0

22.1.6 BLE_RCB_TX_FIFO_WR

Transmitter FIFO write register.

Address: 0x403C001C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	W							
HW Access	R							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	W							
HW Access	R							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data frame written into the transmitter FIFO. Behavior is similar to that of a PUSH operation. A write to a full TX FIFO sets INTR_TX.OVERFLOW to '1'. Default Value: 0

22.1.7 BLE_RCB_RX_CTRL

Receiver control register.

Address: 0x403C0020

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							MSB_-FIRST

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	MSB_FIRST	Least significant bit first ('0') or most significant bit first ('1'). This field also affects the Address field When MSB_FIRST = 1, then [15:0] is data and [(ADDR_WIDTH+15):16] is used for address When MSB_FIRST = 0, then [15:0] is for data. No address field Default Value: 1

22.1.8 BLE_RCB_RX_FIFO_CTRL

Receiver FIFO control register.

Address: 0x403C0024

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				TRIGGER_LEVEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							CLEAR

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
16	CLEAR	When '1', the receiver FIFO and receiver shift register are cleared/invalidated. Invalidation will last for as long as this field is '1'. If a quick clear/invalidation is required, the field should be set to '1' and be followed by a set to '0'. If a clear/invalidation is required for an extended time period, the field should be set to '1' during the complete time period. Default Value: 0
3 : 0	TRIGGER_LEVEL	Trigger level. When the receiver FIFO has more entries than the number of this field, a receiver trigger event is generated. Default Value: 0

22.1.9 BLE_RCB_RX_FIFO_STATUS

Receiver FIFO status register.

Address: 0x403C0028

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			R				
HW Access	None			W				
Name	None [7:5]			USED [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	R	None						
HW Access	W	None						
Name	SR_VALID	None [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	None				R			
HW Access	None				W			
Name	None [23:20]				RD_PTR [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None				R			
HW Access	None				W			
Name	None [31:28]				WR_PTR [27:24]			

Bits	Name	Description
27 : 24	WR_PTR	FIFO write pointer: FIFO location at which a new data frame is written by the hardware. Default Value: 0
19 : 16	RD_PTR	FIFO read pointer: FIFO location from which a data frame is read. Default Value: 0
15	SR_VALID	Indicates whether the RX shift registers holds a (partial) valid data frame ('1') or not ('0'). The shift register can be considered the bottom of the RX FIFO (the data frame is not included in the USED field of the RX FIFO). The shift register is a working register and holds the data frame that is currently being received (when the protocol state machine is receiving a data frame). Default Value: 0
4 : 0	USED	Amount of enties in the receiver FIFO. The value of this field ranges from 0 to FF_DATA_NR. Default Value: 0

22.1.10 BLE_RCB_RX_FIFO_RD

Receiver FIFO read register.

Address: 0x403C002C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data read from the receiver FIFO. Reading a data frame will remove the data frame from the FIFO; i.e. behavior is similar to that of a POP operation. During debug it may be required to read the FIFO without a corresponding POP of the FIFO. This can be achieved by using the RX_FIFO_RD_SILENT register A read from an empty RX FIFO sets INTR_RX.UNDERFLOW to '1'. Default Value: Undefined

22.1.11 BLE_RCB_RX_FIFO_RD_SILENT

Receiver FIFO read register.

Address: 0x403C0030

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data read from the receiver FIFO. Reading a data frame will NOT remove the data frame from the FIFO; i.e. behavior is similar to that of a PEEK operation. A read from an empty RX FIFO sets INTR_RX.UNDERFLOW to '1'. Default Value: Undefined

22.1.12 BLE_RCB_INTR

Master interrupt request register.

Address: 0x403C0040

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1C
HW Access	None							RW1S
Name	None [7:1]							RCB_-DONE

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	None			RW1S	RW1S	RW1S	RW1S	RW1S
Name	None [15:13]			TX_FI-FO_UN-DERFLOW	TX_FI-FO_OVER-FLOW	TX_FI-FO_EMPTY	TX_FI-FO_NOT_-FULL	TX_FI-FO_TRIG-GER

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	None			RW1S	RW1S	RW1S	RW1S	RW1S
Name	None [23:21]			RX_FI-FO_UN-DERFLOW	RX_FI-FO_OVER-FLOW	RX_FIFO_-FULL	RX_FI-FO_NOT_E MPTY	RX_FI-FO_TRIG-GER

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
20	RX_FIFO_UNDERFLOW	Attempt to read from an empty RX FIFO. Default Value: 0
19	RX_FIFO_OVERFLOW	Attempt to write to a full RX FIFO. Default Value: 0
18	RX_FIFO_FULL	RX FIFO is full. Note that received data frames are lost when the RX FIFO is full. entries == (16-TX_ENTRIES_ Default Value: 0
17	RX_FIFO_NOT_EMPTY	RX FIFO is not empty. Default Value: 0
16	RX_FIFO_TRIGGER	More entries in the RX FIFO than the value specified by TRIGGER_LEVEL in RX_FIFO_CTL. Default Value: 0

22.1.12 BLE_RCB_INTR (continued)

12	TX_FIFO_UNDERFLOW	Attempt to read from an empty TX FIFO. This happens when the IP is ready to transfer data and EMPTY is '1'. Default Value: 0
11	TX_FIFO_OVERFLOW	Attempt to write to a full TX FIFO. Default Value: 0
10	TX_FIFO_EMPTY	TX FIFO is empty; i.e. it has 0 entries. Default Value: 1
9	TX_FIFO_NOT_FULL	TX FIFO is not full. entries != TX_ENTRIES Default Value: 1
8	TX_FIFO_TRIGGER	Less entries in the TX FIFO than the value specified by TX_FIFO_CTRL. Default Value: 0
0	RCB_DONE	RCB Controller transfer done event. On completion of every RCB transaction, this bit is set Default Value: 0

22.1.13 BLE_RCB_INTR_SET

Master interrupt set request register

Address: 0x403C0044

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1S
HW Access	None							A
Name	None [7:1]							RCB_-DONE

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	None			A	A	A	A	A
Name	None [15:13]			TX_FI-FO_UN-DERFLOW	TX_FI-FO_OVER-FLOW	TX_FI-FO_EMPTY	TX_FI-FO_NOT_-FULL	TX_FI-FO_TRIG-GER

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	None			A	A	A	A	A
Name	None [23:21]			RX_FI-FO_UN-DERFLOW	RX_FI-FO_OVER-FLOW	RX_FIFO_-FULL	RX_FI-FO_NOT_E MPTY	RX_FI-FO_TRIG-GER

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
20	RX_FIFO_UNDERFLOW	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
19	RX_FIFO_OVERFLOW	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
18	RX_FIFO_FULL	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
17	RX_FIFO_NOT_EMPTY	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
16	RX_FIFO_TRIGGER	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
12	TX_FIFO_UNDERFLOW	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

22.1.13 BLE_RCB_INTR_SET (continued)

11	TX_FIFO_OVERFLOW	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
10	TX_FIFO_EMPTY	Write with '1' to set corresponding bit in interrupt request register. Default Value: 1
9	TX_FIFO_NOT_FULL	Write with '1' to set corresponding bit in interrupt request register. Default Value: 1
8	TX_FIFO_TRIGGER	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	RCB_DONE	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

22.1.14 BLE_RCB_INTR_MASK

Master interrupt mask register.

Address: 0x403C0048

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							RCB_-DONE

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [15:13]			TX_FI-FO_UN-DERFLOW	TX_FI-FO_OVER-FLOW	TX_FI-FO_EMPTY	TX_FI-FO_NOT_-FULL	TX_FI-FO_TRIG-GER

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [23:21]			RX_FI-FO_UN-DERFLOW	RX_FI-FO_OVER-FLOW	RX_FIFO_-FULL	RX_FI-FO_NOT_E MPTY	RX_FI-FO_TRIG-GER

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
20	RX_FIFO_UNDERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
19	RX_FIFO_OVERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
18	RX_FIFO_FULL	Mask bit for corresponding bit in interrupt request register. Default Value: 0
17	RX_FIFO_NOT_EMPTY	Mask bit for corresponding bit in interrupt request register. Default Value: 0
16	RX_FIFO_TRIGGER	Mask bit for corresponding bit in interrupt request register. Default Value: 0
12	TX_FIFO_UNDERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0

22.1.14 BLE_RCB_INTR_MASK (continued)

11	TX_FIFO_OVERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
10	TX_FIFO_EMPTY	Mask bit for corresponding bit in interrupt request register. Default Value: 0
9	TX_FIFO_NOT_FULL	Mask bit for corresponding bit in interrupt request register. Default Value: 0
8	TX_FIFO_TRIGGER	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	RCB_DONE	Mask bit for corresponding bit in interrupt request register. Default Value: 0

22.1.15 BLE_RCB_INTR_MASKED

Master interrupt masked request register

Address: 0x403C004C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							W
Name	None [7:1]							RCB_-DONE

Bits	15	14	13	12	11	10	9	8
SW Access	None			R	R	R	R	R
HW Access	None			W	W	W	W	W
Name	None [15:13]			TX_FI-FO_UN-DERFLOW	TX_FI-FO_OVER-FLOW	TX_FI-FO_EMPTY	TX_FI-FO_NOT_-FULL	TX_FI-FO_TRIG-GER

Bits	23	22	21	20	19	18	17	16
SW Access	None			R	R	R	R	R
HW Access	None			W	W	W	W	W
Name	None [23:21]			RX_FI-FO_UN-DERFLOW	RX_FI-FO_OVER-FLOW	RX_FIFO_-FULL	RX_FI-FO_NOT_E MPTY	RX_FI-FO_TRIG-GER

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
20	RX_FIFO_UNDERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
19	RX_FIFO_OVERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
18	RX_FIFO_FULL	Logical and of corresponding request and mask bits. Default Value: 0
17	RX_FIFO_NOT_EMPTY	Logical and of corresponding request and mask bits. Default Value: 0
16	RX_FIFO_TRIGGER	Logical and of corresponding request and mask bits. Default Value: 0
12	TX_FIFO_UNDERFLOW	Logical and of corresponding request and mask bits. Default Value: 0

22.1.15 BLE_RCB_INTR_MASKED (continued)

11	TX_FIFO_OVERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
10	TX_FIFO_EMPTY	Logical and of corresponding request and mask bits. Default Value: 0
9	TX_FIFO_NOT_FULL	Logical and of corresponding request and mask bits. Default Value: 0
8	TX_FIFO_TRIGGER	Logical and of corresponding request and mask bits. Default Value: 0
0	RCB_DONE	Logical and of corresponding request and mask bits. Default Value: 0

22.1.16 BLE_RCB_RCBLL_CTRL

RCB LL control register.

Address: 0x403C0100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	RW1S	RW1S	RW	RW
HW Access	None		R	R	RW1C	RW1C	RW1C	RW1C
Name	None [7:6]		EN-ABLE_RA-DIO_BOD	AL-LOW_CPU_AC-CESS_TX-_RX	CPU_SIN-GLE_READ	CPU_SIN-GLE_WRITE	RC-BLL_CPU_REQ	RCBLL_C-TRL

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	ENABLE_RADIO_BOD	This bit indicates if the active logic in CYBLERD55 is reset on every TX/RX transaction. Default Value: 0
4	ALLOW_CPU_AC-CESS_TX_RX	This bit indicates if CPU Single Read/Single Write are allowed when Radio RX/TX is ongoing. By default this bit is 0 and no RCB access from CPU are allowed during BLE RX/TX. Default Value: 0
3	CPU_SINGLE_READ	Default Value: 0
2	CPU_SINGLE_WRITE	Default Value: 0
1	RCBLL_CPU_REQ	RCB register access control request by CPU FW sets this bit to take the RCB register access control Once the HW is done with the current transactions, it clears this bit to give control to CPU And also indicates this by giving RCB_LL_DONE interrupt Default Value: 0

22.1.16 BLE_RCB_RCBLL_CTRL (continued)

0	RCBLL_CTRL	RCB register access control 0: RCB registers can be accessed by CPU 1: RCB registers can be accessed by BLE Link Layer. FW sets this bit to give the access control to BLE link layer HW clears this bit to 0 to give the access control to CPU (HW clears this when the RCB controller is free abd RCB?_LL_CPU_REQ is set to 1) Default Value: 0

22.1.17 BLE_RCB_RCBLL_INTR

Master interrupt request register.

Address: 0x403C0110

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1C	RW1C	None	RW1C
HW Access	None				RW1S	RW1S	None	RW1S
Name	None [7:4]				SIN-GLE_READ_DONE	SIN-GLE_WRITE_DONE	None	RCB_LL_-DONE

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	SINGLE_READ_DONE	Default Value: 0
2	SINGLE_WRITE_DONE	Default Value: 0
0	RCB_LL_DONE	RCB_LL is done and the access is given back to CPU Default Value: 0

22.1.18 BLE_RCB_RCBLL_INTR_SET

Master interrupt set request register

Address: 0x403C0114

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1S	RW1S	None	RW1S
HW Access	None				A	A	None	A
Name	None [7:4]				SIN-GLE_READ_DONE	SIN-GLE_WRITE_DONE	None	RCB_LL_-DONE

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	SINGLE_READ_DONE	Default Value: 0
2	SINGLE_WRITE_DONE	Default Value: 0
0	RCB_LL_DONE	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

22.1.19 BLE_RCB_RCBLL_INTR_MASK

Master interrupt mask register.

Address: 0x403C0118

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	None	RW
HW Access	None				R	R	None	R
Name	None [7:4]				SIN-GLE_READ_DONE	SIN-GLE_WRITE_DONE	None	RCB_LL_-DONE

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	SINGLE_READ_DONE	Default Value: 0
2	SINGLE_WRITE_DONE	Default Value: 0
0	RCB_LL_DONE	Mask bit for corresponding bit in interrupt request register. Default Value: 0

22.1.20 BLE_RCB_RCBLL_INTR_MASKED

Master interrupt masked request register

Address: 0x403C011C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R	R	None	R
HW Access	None				W	W	None	W
Name	None [7:4]				SIN-GLE_READ_DONE	SIN-GLE_WRITE_DONE	None	RCB_LL_-DONE

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	SINGLE_READ_DONE	Default Value: 0
2	SINGLE_WRITE_DONE	Default Value: 0
0	RCB_LL_DONE	Logical and of corresponding request and mask bits. Default Value: 0

22.1.21 BLE_RCB_RCBLL_RADIO_REG1_ADDR

Address of Register#1 in Radio (MDON)

Address: 0x403C0120

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	REG_ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	REG_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	REG_ADDR	Default Value: 7682

22.1.22 BLE_RCB_RCBLL_RADIO_REG2_ADDR

Address of Register#2 in Radio (RSSI)

Address: 0x403C0124

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	REG_ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	REG_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	REG_ADDR	Default Value: 2563

22.1.23 BLE_RCB_RCBLL_RADIO_REG3_ADDR

Address of Register#3 in Radio (ACCL)

Address: 0x403C0128

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	REG_ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	REG_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	REG_ADDR	Default Value: 2084

22.1.24 BLE_RCB_RCBLL_RADIO_REG4_ADDR

Address of Register#4 in Radio (ACCH)

Address: 0x403C012C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	REG_ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	REG_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	REG_ADDR	Default Value: 2083

22.1.25 BLE_RCB_RCBLL_RADIO_REG5_ADDR

Address of Register#5 in Radio (RSSI ENERGY)

Address: 0x403C0130

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	REG_ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	REG_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	REG_ADDR	Default Value: 2563

22.1.26 BLE_RCB_RCBLL_CPU_WRITE_REG

TX_Reserved 1 register

Address: 0x403C0140

Retention: Not Retained

Bits	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SW Access	RW							
HW Access	R							
Name	ADDR [7:0]							

Bits	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SW Access	RW							
HW Access	R							
Name	ADDR [15:8]							

Bits	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SW Access	RW							
HW Access	R							
Name	WRITE_DATA [23:16]							

Bits	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**
SW Access	RW							
HW Access	R							
Name	WRITE_DATA [31:24]							

Bits	**Name**	**Description**
31 : 16	WRITE_DATA	Default Value: 0
15 : 0	ADDR	Default Value: 0

22.1.27 BLE_RCB_RCBLL_CPU_READ_REG

TX_Reserved 2 register

Address: 0x403C0144

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	READ_DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	READ_DATA [31:24]							

Bits	Name	Description
31 : 16	READ_DATA	Default Value: 0
15 : 0	ADDR	Default Value: 0

22.1.28 BLE_BLELL_COMMAND_REGISTER

Instruction Register

Address: 0x403C1000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	COMMAND [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description

22.1.28 BLE_BLELL_COMMAND_REGISTER (continued)

7 : 0	COMMAND	8-bit command from firmware to the link layer controller. See below for the list of instructions and their opcodes. The instruction results in the link layer hardware starting/stopping an operation. Notes on use Few of the commands will require other configuration registers to be set, before the command is written. Refer to the description below for details of the registers to be set before setting these instructions. --- Command Opcode Description START_ADV - 0x40: Start Advertiser operation. The associated Advertiser configuration registers are programmed before the command is issued. [refer to llh_set_adv_parameters function in lec_llh/simulation/llh_driver/ll_hardware_api.c file] STOP_ADV - 0x41: Stop advertiser operation. START_SCAN - 0x42: Start scanner operation. The associated configuration registers must be programmed before the command is issued. [refer to llh_set_scan_parameters function in lec_llh/simulation/llh_driver/ll_hardware_api.c file] STOP_SCAN - 0x43: Stop the scanner operation. START_INIT - 0x44: Start connection creation operation. The associated configuration registers must be programmed before the command is issued. [refer to create_connection function in lec_llh/simulation/llh_driver/ll_hardware_api.c file] STOP_INIT - 0x45: Cancel connection creation operation. DTM_TX_START - 0x46: Start Direct Test Mode Transmit Test. The associated configuration registers must be programmed before the command is issued. [refer to dtm_tx_test function in lec_llh/simulation/llh_driver/ll_hardware_api.c file] DTM_RX_START - 0x47: Start Direct Test Mode Receive Test. The associated configuration registers must be programmed before the command is issued. [refer to dtm_rx_test function in lec_llh/simulation/llh_driver/ll_hardware_api.c file] DTM_STOP - 0x48: Stop Direct Test Mode. UPDATE_CHAN_MAP - 0x4B: Update channel map for the connection. UPDATE_CONN_PROC - 0x4C: Start connection update procedure for the connection. PACKET_RECEIVED - 0x4D: Indicates a received connection packet is read by firmware from connection receive FIFO. UPDATE_DATARATE - 0x4E: Indicates a update the next instance for the data rate change. ENTER_DSM - 0x50: Enter deep sleep mode. ENC_CLK_ON - 0x53: Turn on clock to encryption block ENC_CLK_OFF - 0x54: Turn off clock to encryption block ADV_CLK_ON - 0x55: Turn on clock to advertiser block in NAP mode. This command needs to be initiated when ADV NI_TIMER is used ADV_CLK_OFF - 0x56: Turn off clock to advertiser block in NAP mode. SCAN_CLK_ON - 0x57: Turn on clock to scanner block in NAP mode. This command needs to be initiated when SCAN NI_TIMER is used SCAN_CLK_OFF - 0x58: Turn off clock to scanner block in NAP mode. INIT_CLK_ON - 0x59: Turn on clock to initiator block in NAP mode. This command needs to be initiated when INIT NI_TIMER is used INIT_CLK_OFF - 0x5a: Turn off clock to initiator block in NAP mode. CONN_CLK_ON - 0x5b: Turn on clock to connection block in NAP mode. CONN_CLK_OFF - 0x5c: Turn off clock to connection block in NAP mode. UPDATE_CONN - 0x68: Update connection parameters. Deprecated. KILL_CONN - 0x70: Kill connection immediately. KILL_CONN_AFTER_TX - 0x71: Kill connection after a transmit operation is over. RESP_TIMER_ON - 0x72: Start PDU response timer. The PDU_RESP_TIMER register must be pro-grammed with timeout value before issuing this command. RESP_TIMER_OFF - 0x73: Stop PDU response timer. RESET_READ_PTR - 0x74: Reset the white list memory read pointer to 0. CONN_PING_TIMER_ON - 0x75: Start connection ping timer CONN_PING_TIMER_OFF - 0x076: Stop connection ping timer SOFT_RESET - 0x80: Software reset. Resets all the hardware registers (except a few registers related to radio initializa-tion). RESET_US_COUNTER - 0xC3: Reset microsecond counter Default Value: 0

22.1.29 BLE_BLELL_EVENT_INTR

Event(Interrupt) status and Clear register

Address: 0x403C1008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	RW1C	RW1C	R	R	R	R
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	RSSI_RX_-DONE_IN-TR	ENC_INTR	DSM_INTR	SM_INTR	CONN_IN-TR	INIT_INTR	SCAN_IN-TR	ADV_INTR

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	RSSI_RX_DONE_INTR	RSSI RX done interrupt. Default Value: 0
6	ENC_INTR	Encryption module interrupt. This interrupt id deprecated and should not be used Default Value: 0
5	DSM_INTR	Read: Deep sleep mode exit interrupt. This bit is set, when link layer hardware exits from deep sleep mode. Write: Clear deep sleep mode exit interrupt. Write to the register with this bit set to 1, clears the interrupt source. Default Value: 0
4	SM_INTR	Read: Sleep-mode-exit interrupt. This bit is set, when link layer hardware exits from sleep mode. Write: Clear sleep-mode-exit interrupt. Write to the register with this bit set to 1, clears the interrupt source. This interrupt is deprecated and should not be used. Default Value: 0

22.1.29 BLE_BLELL_EVENT_INTR (continued)

3	CONN_INTR	Connection interrupt. If bit is set to 1, it indicates an event occurred in the connection operation. This interrupt is aggregation of interrupts for all the connections. The source of the event for the specific connection, needs to be read from the CONN_INTR register specific to the connection. This bit is cleared, when firmware clears ALL interrupts by writing to the CONN_INTR register. Default Value: 0
2	INIT_INTR	Initiator interrupt. If bit is set to 1, it indicates an event occurred in the initiating procedure. The source of the event needs to be read from the INIT_INTR register. This bit is cleared, when firmware clears ALL interrupts by writing to the INIT_INTR register. Default Value: 0
1	SCAN_INTR	Scanner interrupt. If bit is set to 1, it indicates an event occurred in the scanning procedure. The source of the event needs to be read from the SCAN_INTR register. This bit is cleared, when firmware clears ALL interrupts by writing to the SCAN_INTR register. Default Value: 0
0	ADV_INTR	Advertiser interrupt. If bit is set to 1, it indicates an event occurred in the advertising procedure. The source of the event needs to be read from the ADV_INTR register. This bit is cleared, when firmware clears ALL interrupts by writing to the ADV_INTR register. Default Value: 0

22.1.30 BLE_BLELL_EVENT_ENABLE

Event indications enable.

Address: 0x403C1010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	RSSI_RX_-DO-NE_INT_EN	EN-C_INT_EN	DS-M_INT_EN	SM_INT_EN	CON-N_INT_EN	INIT_INT_EN	SCN_INT_EN	AD-V_INT_EN

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	RSSI_RX_DONE_INT_EN	RSSI Rx interrupt enable. 1 Enable RSSI Rx done interrupt to firmware. 0 Disable RSSI Rx done interrupt to firmware. Default Value: 0
6	ENC_INT_EN	Encryption module interrupt enable. 1 Enable encryption module interrupt to firmware. 0 disable encryption module interrupt to firmware. This interrupt is deprecated and should not be used Default Value: 0
5	DSM_INT_EN	Deep Sleep-mode-exit interrupt enable. 1 enable deep sleep mode exit event to interrupt the firmware. 0 disable deep sleep mode exit interrupt to firmware. Default Value: 0

22.1.30 BLE_BLELL_EVENT_ENABLE (continued)

4	SM_INT_EN	Sleep-mode-exit interrupt enable. 1 enable sleep mode exit event to interrupt the firmware. 0 disable sleep mode exit interrupt to firmware. This interrupt is deprecated and should not be used. Default Value: 0
3	CONN_INT_EN	Connection interrupt enable. 1 enable connection procedure to interrupt the firmware. 0 disable connection procedure interrupt to firmware. Default Value: 0
2	INIT_INT_EN	Initiator interrupt enable. 1 enable initiator procedure to interrupt the firmware. 0 disable initiator procedure interrupt to firmware. Default Value: 0
1	SCN_INT_EN	Scanner interrupt enable. 1 enable scan procedure to interrupt the firmware. 0 disable scan procedure interrupt to firmware. Default Value: 0
0	ADV_INT_EN	Advertiser interrupt enable. 1 enable advertiser procedure to interrupt the firmware. 0 disable advertiser procedure interrupt to firmware. Default Value: 0

22.1.31 BLE_BLELL_ADV_PARAMS

Advertising parameters register.

Address: 0x403C1018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW			RW		RW		RW
HW Access	R			R		R		R
Name	ADV_CHANNEL_MAP [7:5]			ADV_FILT_POLICY [4:3]		ADV_TYPE [2:1]		TX_ADDR

Bits	15	14	13	12	11	10	9	8
SW Access	R	RW	RW	RW	RW	RW	RW	RW
HW Access	RW	R	R	R	R	R	R	R
Name	RCV_TX-_ADDR	AD-V_RPT_PEER_NR-PA_AD-DR_IN_PRIV	AD-V_RCV_IA_IN_PRIV	TX_AD-DR_PRIV	INITA_R-PA_CHECK	AD-V_LOW_DUTY_CYCLE	RX-_SEC_AD-DR	RX_ADDR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15	RCV_TX_ADDR	Transmit address field of the received packet extracted from the receive packet. This field is used by firmware to report peer_addr_type parameter in the connection complete event. Default Value: 0
14	ADV_RPT_PEER_NR-PA_ADDR_IN_PRIV	Advertiser behavior when a peer Non Resolvable Private Address is received in privacy mode. This bit is valid only if PRIV_1_2 and PRIV_1_2_ADV are set. This is applicable when whitelist is disabled. 1 - Only report the packets with peer NRPA address in privacy mode 0 - Respond to packets with peer NRPA address in privacy mode Default Value: 0
13	ADV_RCV_IA_IN_PRIV	Advertiser behavior when a peer Identity address is received in privacy mode. This bit is valid only if PRIV_1_2 and PRIV_1_2_ADV are set. 1 - Accept packets with peer identity address not in the Resolving list in privacy mode 0 - Reject packets with peer identity address not in the Resolving list in privacy mode Default Value: 0

22.1.31 BLE_BLELL_ADV_PARAMS (continued)

12	TX_ADDR_PRIV	Device own address type subtype when Address type is random. This bit is valid only if PRIV_1_2 and PRIV_1_2_ADV are set. 1 - Random Address type is private. 0 - Random Address type is static. Default Value: 0
11	INITA_RPA_CHECK	This bit field is used to specify the Advertiser behavior on receiving the same INITA in the connect_req as in the ADV_DIRECT_IND packet it sent. This bit is valid only if PRIV_1_2 and PRIV_1_2_ADV are set. 0 - Accept the connect_req packet 1 - Reject the connect_req packet Default Value: 0
10	ADV_LOW_DUTY_CYCLE	This bit field is used to specify to the Controller the Low Duty Cycle connectable directed advertising variant being used. 1 Low Duty Cycle Connectable Directed Advertising. 0 High Duty Cycle Connectable Directed Advertising. Default Value: 0
9	RX_SEC_ADDR	Peer secondary addresses type. This is the Direct_Address_type field programmed, only if ADV_DIRECT_IND type is sent. This address type corresponds to the PEER_SERC_ADDR register. Valid only if PRIV_1_2_ADV is set. 1 Rx secondary addr type is random. 0 Rx secondary addr type is public Default Value: 0
8	RX_ADDR	Peer addresses type. This is the Direct_Address_type field programmed, only if ADV_DIRECT_IND type is sent. 1 Rx addr type is random. 0 Rx addr type is public Default Value: 0
7 : 5	ADV_CHANNEL_MAP	Advertising channel map indicates the advertising channels used for advertising. By setting the bit, corresponding channel is enabled for use. Atleast one channel bit should be set. 7 - enable channel 39. 6 - enable channel 38. 5 - enable channel 37. Default Value: 7
4 : 3	ADV_FILT_POLICY	Advertising filter policy. The set of devices that the advertising procedure uses for device filtering is called the White List. 0x0 - Allow scan request from any device, allow connect request from any device. 0x1 - Allow scan request from devices in white list only, allow connect request from any device. 0x2 - Allow scan request from any device, allow connect request from devices in white list only. 0x3 - Allow scan request from devices in white list only, allow connect request from devices in white list only. Default Value: 0
2 : 1	ADV_TYPE	The Advertising type is used to determine the packet type that is used for advertising when advertising is enabled. 0x0 - Connectable undirected advertising. (adv_ind) 0x1 - Connectable directed advertising (adv_direct_ind). 0x2 - Discoverable undirected advertising (adv_discover_ind) 0x3 - Non connectable undirected advertising (adv_nonconn_ind). Default Value: 0
0	TX_ADDR	Device own address type. 1 - Address type is random. 0 - Address type is public. Default Value: 0

22.1.32 BLE_BLELL_ADV_INTERVAL_TIMEOUT

Advertising interval register.

Address: 0x403C101C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	ADV_INTERVAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW						
HW Access	None	R						
Name	None	ADV_INTERVAL [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
14 : 0	ADV_INTERVAL	Range: 0x0020 to 0x4000 (For ADV_IND) 0x00A0 to 0x4000 (For ADV_SCAN_IND and NONCONN_IND) Invalid for ADV_DIRECT_IND Time = N * 0.625 msec Time Range: 20 ms to 10.24 sec. For directed advertising, firmware programs the default value of 1.28 seconds. In MMMS mode, this register is used as ADV_NI_TIMER when the ADV_NI_VALID is set by firmware Default Value: 32

22.1.33 BLE_BLELL_ADV_INTR

Advertising interrupt status and Clear register

Address: 0x403C1020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	ADV_TIME-OUT	SLV_CON-NECTED	CON-N_REQ_RX_INTR	SCAN_REQ_RX_INTR	SCAN_R-SP_TX_IN-TR	ADV_TX-_INTR	ADV_-CLOSE_IN-TR	AD-V_STRT_IN TR

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW1C	RW1C	RW1C	RW1C	R
HW Access	None			RW	RW	RW	RW	RW
Name	None [15:13]			SCAN_AD-DR_-MATCH_PRIV_MIS-MATCH_IN-TR	INIT_AD-DR_-MATCH_PRIV_MIS-MATCH_IN-TR	SCAN_REQ_RX-_PEER_R-PA_UNMCH_INTR	SLV_CON-N_PEER_RPA_UN-MCH_INTR	ADV_ON

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
12	SCAN_ADDR_-MATCH_PRIV_MIS-MATCH_INTR	If this bit is set it indicates that an Identity address is received from an initiator and matches an entry in the resolving list, but peer IRK is set and hence a corresponding RPA is expected from the initiator Write to the register with this bit set to 1, clears the interrupt source. This bit is valid only if PRIV_1_2 and PRIV_1_2_ADV are set. Default Value: 0
11	INIT_ADDR_-MATCH_PRIV_MIS-MATCH_INTR	If this bit is set it indicates that an Identity address is received from a Scanner and matches an entry in the resolving list, but peer IRK is set and hence a corresponding RPA is expected from the Scanner Write to the register with this bit set to 1, clears the interrupt source. This bit is valid only if PRIV_1_2 and PRIV_1_2_ADV are set. Default Value: 0

22.1.33 BLE_BLELL_ADV_INTR (continued)

10	SCAN_REQ_RX-_PEER_RPA_UN-MCH_INTR	If this bit is set it indicates scan request packet received, but the peer device Resolvable Private Address is not resolved/ ID or NRPA are not matched yet. Write to the register with this bit set to 1, clears the interrupt source. This bit is valid only if PRIV_1_2 and PRIV_1_2_ADV are set. Default Value: 0
9	SLV_CONN_PEER_R-PA_UNMCH_INTR	If this bit is set it indicates that connection is created as slave, but the peer device Resolvable Private Address is not resolved/ ID or NRPA are not matched yet. If the address is not resolved prior to connection establishment, the connection will be terminated. Write to the register with this bit set to 1, clears the interrupt source. This bit is valid only if PRIV_1_2 and PRIV_1_2_ADV are set. Default Value: 0
8	ADV_ON	Advertiser procedure is ON in hardware. Indicates that advertiser procedure is ON in hardware. 1 - ON 0 - OFF Default Value: 0
7	ADV_TIMEOUT	If this bit is set it indicates that the directed advertising event has timed out after 1.28 seconds. Applicable in adv_direct_ind advertising. Write to the register with this bit set to 1, clears the interrupt source. Default Value: 0
6	SLV_CONNECTED	If this bit is set it indicates that connection is created as slave. Write to the register with this bit set to 1, clears the interrupt source. Note: On a slave connection creation, the link layer cannot enter deepsleep mode in the same slot . It can enter deepsleep mode only in the subsequent slots. Default Value: 0
5	CONN_REQ_RX_INTR	If this bit is set it indicates connect request packet is received. Write to the register with this bit set to 1, clears the interrupt source. Default Value: 0
4	SCAN_REQ_RX_INTR	If this bit is set it indicates scan request packet received. Write to the register with this bit set to 1, clears the interrupt source. Default Value: 0
3	SCAN_RSP_TX_INTR	If this bit is set it indicates scan response packet transmitted in response to previous scan request packet received. Write to the register with this bit set to 1, clears the interrupt source. Default Value: 0
2	ADV_TX_INTR	If this bit is set it indicates ADV packet is transmitted. Write to the register with this bit set to 1, clears the interrupt source. Default Value: 0
1	ADV_CLOSE_INTR	If this bit is set it indicates current advertising event is closed. Write to the register with this bit set to 1, clears the interrupt source. Default Value: 0
0	ADV_STRT_INTR	If this bit is set it indicates a new advertising event started after interval expiry. Write to the register with this bit set to 1, clears the interrupt source. Default Value: 0

22.1.34 BLE_BLELL_ADV_NEXT_INSTANT

Advertising next instant.

Address: 0x403C1024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	ADV_NEXT_INSTANT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	ADV_NEXT_INSTANT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	ADV_NEXT_INSTANT	Shows the next start of advertising event with reference to the internal reference clock. Default Value: 0

22.1.35 BLE_BLELL_SCAN_INTERVAL

Scan Interval Register

Address: 0x403C1028

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SCAN_INTERVAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	SCAN_INTERVAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	SCAN_INTERVAL	Scan interval register. Interval between two consecutive scanning events. Firmware sets the scanning interval value to this register before issuing start scan command. Range: 0x0004 to 0x4000 Default: 0x0010 (10 ms) Time = N * 0.625 msec Time Range: 2.5 msec to 10.24 sec. In MMMS mode, this register is used as SCAN_NI_TIMER when the SCAN_NI_VALID is set by firmware Default Value: 16

22.1.36 BLE_BLELL_SCAN_WINDOW

Scan window Register

Address: 0x403C102C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SCAN_WINDOW [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	SCAN_WINDOW [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	SCAN_WINDOW	Duration of scan in a scanning event, which should be less than or equal to scan interval value. Firmware sets the scan window value to this register before issuing start scan command. Range: 0x0004 to 0x4000 Default: 0x0010 (10 ms) Time = N * 0.625 msec Time Range: 2.5 msec to 10.24 sec. (To prevent ADV RX - SCAN REQ TX - SCAN RSP RX spilling over across the scan window, when not in continuous scan, the scan window must be 2 slots less that the scan interval. Default Value: 16

22.1.37 BLE_BLELL_SCAN_PARAM

Scanning parameters register

Address: 0x403C1030

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW		RW		RW
HW Access	R	R	R	R		R		R
Name	SCAN_R-SP_ADVA_-CHECK	DUP_-FILT_CH-K_ADV_DIR	DUP_-FILT_EN	SCAN_FILT_POLICY [4:3]		SCAN_TYPE [2:1]		TX_ADDR

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [15:10]						SCAN_RPT_PEER_N-RPA_AD-DR_IN_PRIV	SCAN_RCV_IA_IN_PRIV

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	SCAN_RPT_PEER_NR-PA_ADDR_IN_PRIV	Scanner behavior when a peer Non Resolvable Private Address is received in privacy mode. This bit is valid only if PRIV_1_2 and PRIV_1_2_SCAN are set. This is applicable when whitelist is disabled. 1 - Only report packets with peer NRPA address in privacy mode 0 - Respond packets with peer NRPA address in privacy mode Default Value: 0
8	SCAN_RCV_IA_IN_PRIV	Scanner behavior when a peer Identity address is received in privacy mode. This bit is valid only if PRIV_1_2 and PRIV_1_2_SCAN are set. 1 - Accept packets with peer identity address not in the Resolving list in privacy mode 0 - Reject packets with peer identity address not in the Resolving list in privacy mode Default Value: 0

22.1.37 BLE_BLELL_SCAN_PARAM (continued)

7	SCAN_RSP_ADVA_-CHECK	This bit field is used to specify the Scanner behavior with respect to ADVA while receiving a SCAN_RSP packet. This bit is valid only if PRIV_1_2 and PRIV_1_2_SCAN are set. 0 - The ADVA in SCAN_RSP packets are not verified 1 - The ADVA in SCAN_RSP packets are verified against ADVA received in ADV packet . If it fails, then abort the packet. Default Value: 0
6	DUP_FILT_CHK_AD-V_DIR	This bit field is used to specify the Scanner duplicate filter behavior for ADV_DIRECT_IND packet when duplicate DUP_FILT_EN is set. This bit is valid only if PRIV_1_2 and PRIV_1_2_SCAN are set. 0 - Do not filter ADV_DIRECT_IND duplicate packets. 1 - Filter ADV_DIRECT_IND duplicate packets Default Value: 0
5	DUP_FILT_EN	Filter duplicate packets. 1- Duplicate filtering enabled. 0- Duplicate filtering not enabled. This field is derived from the LE_set_scan_enable command. Default Value: 0
4 : 3	SCAN_FILT_POLICY	The scanner filter policy determines how the scanner processes advertising packets. 0x00 - Accept advertising packets from any device. 0x01 - Accept advertising packets from only devices in the whitelist. In the above 2 policies, the directed advertising packets which are not addressed to this device are ignored. 0x10 - Accept all undirected advertising packets and directed advertising packet addressed to this device. 0x11 - Accept undirected advertising packets from devices in the whitelist and directed advertising packet addressed to this device In the above 2 policies, the directed advertising packets where the initiator address is a resolvable private address are accepted. The above 2 policies are extended scanner filter policies. Default Value: 0
2 : 1	SCAN_TYPE	0x00 - passive scanning.(default) 0x01 - active scanning. 0x10 - RFU 0x11 - RFU Default Value: 0
0	TX_ADDR	Devices own address type. 1 - addr type is random. 0 - addr type is public. Default Value: 0

22.1.38 BLE_BLELL_SCAN_INTR

Scan interrupt status and Clear register

Address: 0x403C1038

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	SCANA_TX_ADDR_NOT_SET_INTR	ADV_RX_SELF_RPA_UNMCH_INTR	ADV_RX_PEER_RPA_UNMCH_INTR	SCAN_RSP_RX_INTR	ADV_RX_INTR	SCAN_TX_INTR	SCAN_CLOSE_INTR	SCAN_STRT_INTR

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW1C	RW1C	R
HW Access	None					RW	RW	RW
Name	None [15:11]					SELF_ADDR_MATCH_PRIV_MISMATCH_INTR	PEER_ADDR_MATCH_PRIV_MISMATCH_INTR	SCAN_ON

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10	SELF_ADDR_MATCH_PRIV_MISMATCH_INTR	If this bit is set it indicates that the self Identity address is received from an initiator and matches, but self IRK is set and hence a corresponding RPA is expected from the initiator Write to the register with this bit set to 1, clears the interrupt source. This bit is valid only if PRIV_1_2 and PRIV_1_2_SCAN are set. Default Value: 0
9	PEER_ADDR_MATCH_PRIV_MISMATCH_INTR	If this bit is set it indicates that an Identity address is received from an initiator and matches an entry in the resolving list, but peer IRK is set and hence a corresponding RPA is expected from the initiator Write to the register with this bit set to 1, clears the interrupt source. This bit is valid only if PRIV_1_2 and PRIV_1_2_SCAN are set. Default Value: 0

22.1.38 BLE_BLELL_SCAN_INTR (continued)

8	SCAN_ON	Scan procedure status. 1 scan procedure is active. 0 scan procedure is not active. Default Value: 0
7	SCANA_TX_AD-DR_NOT_SET_INTR	If this bit is set it indicates that a valid ScanA RPA to be transmitted in SCAN_REQ packet in response to an ADV packet is not present in the resolving list Write to the register with this bit set to 1, clears the interrupt source. This bit is valid only if PRIV_1_2 and PRIV_1_2_SCAN are set. Default Value: 0
6	ADV_RX_SELF_R-PA_UNMCH_INTR	If this bit is set it indicates ADV_DIRECT packet received but the self device Resolvable Private Address is not resolved yet. Firmware can read the content of the packet from the INIT_SCN_ADV_RX_FIFO. This bit is valid only if PRIV_1_2 and PRIV_1_2_SCAN are set. Write to the register with this bit set to 1, clears the interrupt source. This interrupt is generated while active/passive scanning upon receiving adv_direct packets. Default Value: 0
5	ADV_RX_PEER_R-PA_UNMCH_INTR	If this bit is set it indicates ADV packet received but the peer device Address is not match yet. Firmware can read the content of the packet from the INIT_SCN_ADV_RX_FIFO. This bit is valid only if PRIV_1_2 and PRIV_1_2_SCAN are set. Write to the register with this bit set to 1, clears the interrupt source. This interrupt is generated while active/passive scanning upon receiving adv packets. Default Value: 0
4	SCAN_RSP_RX_INTR	If this bit is set it indicates SCAN_RSP packet is received. Firmware can read the content of the packet from the INIT_SCN_ADV_RX_FIFO. Write to the register with this bit set to 1, clears the interrupt source. NOTE: This interrupt is generated while active scanning upon receiving scan response packet. Default Value: 0
3	ADV_RX_INTR	If this bit is set it indicates ADV packet received. Firmware can read the content of the packet from the INIT_SCN_ADV_RX_FIFO. Write to the register with this bit set to 1, clears the interrupt source. This interrupt is generated while active/passive scanning upon receiving adv packets. Note: Any ADV RX interrupt received after issuing SCAN_STOP command must be ignored and the ADVCH FIFO flushed. Default Value: 0
2	SCAN_TX_INTR	If this bit is set it indicates scan request packet is transmitted. Write to the register with this bit set to 1, clears the interrupt source. Default Value: 0
1	SCAN_CLOSE_INTR	If this bit is set it indicates scan window is closed. Write to the register with this bit set to 1, clears the interrupt source. Default Value: 0
0	SCAN_STRT_INTR	If this bit is set it indicates scan window is opened. Write to the register with this bit set to 1, clears the interrupt source. Default Value: 0

22.1.39 BLE_BLELL_SCAN_NEXT_INSTANT

Advertising next instant.

Address: 0x403C103C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	NEXT_SCAN_INSTANT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	NEXT_SCAN_INSTANT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	NEXT_SCAN_INSTANT	Shows the instant with respect to internal reference clock of resolution 625 us at which next scanning event begins. Default Value: 0

22.1.40 BLE_BLELL_INIT_INTERVAL

Initiator Interval Register

Address: 0x403C1040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	INIT_SCAN_INTERVAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INIT_SCAN_INTERVAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	INIT_SCAN_INTERVAL	Initiator interval register. Firmware sets the initiators scanning interval value to this regis-ter be-fore issuing create connection command. Interval between two consecutive scanning events. Range: 0x0004 to 0x4000 Time = N * 0.625 msec Time Range: 2.5 msec to 10.24 sec. In MMMS mode, this register is used as INIT_NI_TIMER when the INIT_NI_VALID is set by firm-ware Default Value: 0

22.1.41 BLE_BLELL_INIT_WINDOW

Initiator window Register

Address: 0x403C1044

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	INIT_SCAN_WINDOW [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INIT_SCAN_WINDOW [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	INIT_SCAN_WINDOW	Duration of scan in a scanning event, which should be less than or equal to scan interval value. Firmware sets the scan window value to this register before issuing create connection command. Range: 0x0004 to 0x4000 Time = N * 0.625 msec Time Range: 2.5 msec to 10.24 sec. In MMMS mode, this register is used as INIT_NI_TIMER when the INIT_NI_VALID is set by firmware Default Value: 0

22.1.42 BLE_BLELL_INIT_PARAM

Initiator parameters register

Address: 0x403C1048

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW	None	RW	RW
HW Access	None			R	R	None	RW	R
Name	None [7:5]			INIT_RCV_IA_IN_PRIV	INIT_-FILT_POLI-CY	None	RX_AD-DR__RX-_TX_ADDR	TX_ADDR

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4	INIT_RCV_IA_IN_PRIV	Init behavior when a peer Identity address is received in privacy mode. This bit is valid only if PRIV_1_2 and PRIV_1_2_INIT are set. 1 - Accept packets with peer identity address not in the Resolving list in privacy mode 0 - Reject packets with peer identity address not in the Resolving list in privacy mode & HW_RSLV_LIST_FULL is not set Default Value: 0
3	INIT_FILT_POLICY	The Initiator_Filter_Policy is used to determine whether the White List is used or not. 0 - White list is not used to determine which advertiser to connect to. Instead the Peer_Address_-Type and Peer Address fields are used to specify the address type and address of the advertis-ing device to connect to. 1 - White list is used to determine the advertising device to connect to. Peer_Address_Type and Peer_Address fields are ignored when whitelist is used. Default Value: 0

22.1.42 BLE_BLELL_INIT_PARAM (continued)

1	RX_ADDR__RX_TX_ADDR	Peer address type. The rx_addr field is updated by the receiver with the address type of the received connectable advertising packet. 1 - addr type is random. 0 - addr type is public. Default Value: 0
0	TX_ADDR	Device own address type. 1 - addr type is random. 0 - addr type is public. Default Value: 0

22.1.43 BLE_BLELL_INIT_INTR

Scan interrupt status and Clear register

Address: 0x403C1050

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	None	RW1C	RW1C	RW1C
HW Access	RW	RW	RW	RW	None	RW	RW	RW
Name	INITA_TX-_AD-DR_NOT_SET_INTR	ADV_RX-_PEER_ADDR_UN-MCH_INTR	ADV_RX_-SELF_AD-DR_UNMCH_INTR	MASTER_-CON-N_CREATED	None	INIT_TX-_START_INTR	INIT_-CLOSE_WINDOW_INR	INIT_IN-TERVAL_-EXPIRE_INTR

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW1C	RW1C
HW Access	None						RW	RW
Name	None [15:10]						INI_-SELF_AD-DR_MATCH_PRIV_MISMATCH_IN-TR	INI_PEER_ADDR_-MATCH_PRIV_MIS-MATCH_IN-TR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	INI_SELF_ADDR_-MATCH_PRIV_MIS-MATCH_INTR	If this bit is set it indicates that - an Identity address is received from an initiator and matches an entry in the resolving list, but peer IRK is set and hence a corresponding RPA is expected from the initiator - or an RPA is received from an initiator and matches an entry in the resolving list, but peer IRK is not set and hence a corresponding Identity address is expected from the initiator Write to the register with this bit set to 1, clears the interrupt source. This bit is valid only if PRIV_1_2 and PRIV_1_2_INIT are set. Default Value: 0

22.1.43 BLE_BLELL_INIT_INTR (continued)

8	INI_PEER_ADDR_-MATCH_PRIV_MIS-MATCH_INTR	If this bit is set it indicates that an Identity address is received from an initiator and matches an entry in the resolving list, but peer IRK is set and hence a corresponding RPA is expected from the initiator Write to the register with this bit set to 1, clears the interrupt source. This bit is valid only if PRIV_1_2 and PRIV_1_2_INIT are set. Default Value: 0
7	INITA_TX_AD-DR_NOT_SET_INTR	If this bit is set it indicates that a valid INITA RPA to be transmitted in CONN_REQ packet in response to an ADV packet is not present in the resolving list Write to the register with this bit set to 1, clears the interrupt source. This bit is valid only if PRIV_1_2 and PRIV_1_2_INIT are set. Default Value: 0
6	ADV_RX_PEER_AD-DR_UNMCH_INTR	If this bit is set it indicates ADV packet received but the peer device Address is not matched yet. Firmware can read the content of the packet from the INIT_SCN_ADV_RX_FIFO. This bit is valid only if PRIV_1_2 and PRIV_1_2_INIT are set. Write to the register with this bit set to 1, clears the interrupt source. This interrupt is generated while active/passive scanning upon receiving adv packets. Default Value: 0
5	ADV_RX_SELF_AD-DR_UNMCH_INTR	If this bit is set it indicates ADV_DIRECT packet received but the self device Resolvable Private Address is not resolved yet. Firmware can read the content of the packet from the INIT_SCN_ADV_RX_FIFO. This bit is valid only if PRIV_1_2 and PRIV_1_2_INIT are set. Write to the register with this bit set to 1, clears the interrupt source. This interrupt is generated while active/passive scanning upon receiving adv packets. Default Value: 0
4	MASTER_CONN_CRE-ATED	If this bit is set it indicates connection is created as master. Write to the register with this bit set to 1, clears the interrupt source. Default Value: 0
2	INIT_TX_START_INTR	If this bit is set it indicates initiator packet (CONREQ) transmission has started. Write to the register with this bit set to 1, clears the interrupt source. Default Value: 0
1	INIT_CLOSE_WIN-DOW_INR	If this bit is set it indicates initiator scan window has finished. Write to the register with this bit set to 1, clears the interrupt source. Default Value: 0
0	INIT_INTERVAL_EX-PIRE_INTR	If this bit is set it indicates initiator scan window has started. Write to the register with this bit set to 1, clears the interrupt source. Default Value: 0

22.1.44 BLE_BLELL_INIT_NEXT_INSTANT

Initiator next instant.

Address: 0x403C1054

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	INIT_NEXT_INSTANT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	INIT_NEXT_INSTANT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	INIT_NEXT_INSTANT	Shows the instant with respect to internal reference clock of resolution 625 us at which next initiator scanning event begins. Default Value: 0

22.1.45 BLE_BLELL_DEVICE_RAND_ADDR_L

Lower 16 bit random address of the device.

Address: 0x403C1058

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DEVICE_RAND_ADDR_L [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DEVICE_RAND_ADDR_L [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DEVICE_RAND_ADDR_L	Lower 16 bit of 48-bit random address of the device. Default Value: 0

22.1.46 BLE_BLELL_DEVICE_RAND_ADDR_M

Middle 16 bit random address of the device.

Address: 0x403C105C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DEVICE_RAND_ADDR_M [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DEVICE_RAND_ADDR_M [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DEVICE_RAND_ADDR_M	Middle 16 bit of 48-bit random address of the device. Default Value: 0

22.1.47 BLE_BLELL_DEVICE_RAND_ADDR_H

Higher 16 bit random address of the device.

Address: 0x403C1060

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DEVICE_RAND_ADDR_H [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DEVICE_RAND_ADDR_H [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DEVICE_RAND_ADDR_H	Higher 16 bit of 48-bit random address of the device. Default Value: 0

22.1.48 BLE_BLELL_PEER_ADDR_L

Lower 16 bit address of the peer device.

Address: 0x403C1068

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	PEER_ADDR_L [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PEER_ADDR_L [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	PEER_ADDR_L	Lower 16 bit of 48-bit address of the peer device. Default Value: 0

22.1.49 BLE_BLELL_PEER_ADDR_M

Middle 16 bit address of the peer device.

Address: 0x403C106C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	PEER_ADDR_M [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PEER_ADDR_M [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	PEER_ADDR_M	Middle 16 bit of 48-bit address of the peer device. Default Value: 0

22.1.50 BLE_BLELL_PEER_ADDR_H

Higher 16 bit address of the peer device.

Address: 0x403C1070

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	PEER_ADDR_H [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PEER_ADDR_H [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	PEER_ADDR_H	Higher 16 bit of 48-bit address of the peer device. The peer address registers are used for multiple purposes. The register is written by firmware to provide the peer address to be used for a hardware procedure. When firmware reads the register, it reads back peer address values updated by hardware. While doing directed Advertising, the firmware writes the peer address of the device specified by the Di-rect_Address parameter of the LE_Set_Advertising_Parameters command. In non MMMS mode, While device is configured as an initiator without white list filtering, the peer address specified in the peer_address field of the create connection command is programmed into this register, which is used by hard-ware procedures. In non MMMS mode, While device is configured as an initiator and white list is enabled, firmware can read this register to get the address of the peer device from which connectable ADV packet was received and to which the connection is created. When a connection is created as a slave, the firmware can read this register to get the address of the peer de-vice to which connection is created. Default Value: 0

22.1.51 BLE_BLELL_WL_ADDR_TYPE

whitelist address type

Address: 0x403C1078

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	WL_ADDR_TYPE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	WL_ADDR_TYPE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	WL_ADDR_TYPE	8 address type bits corresponding to the device address stored. 1 - Address type is random. 0 - Address type is public. Default Value: 0

22.1.52 BLE_BLELL_WL_ENABLE

whitelist valid entry bit

Address: 0x403C107C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	WL_ENABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	WL_ENABLE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	WL_ENABLE	Stores the valid entry bit corresponding to each of the eight device address stored in the whitelist. 1 - White list entry is Valid 0 - White list entry is Invalid Default Value: 0

22.1.53 BLE_BLELL_TRANSMIT_WINDOW_OFFSET

Transmit window offset

Address: 0x403C1080

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	TX_WINDOW_OFFSET [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	TX_WINDOW_OFFSET [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	TX_WINDOW_OFFSET	This is used to determine the first anchor point for the master transmission, from the time of connection creation. Range: This shall be a multiple of 1.25 ms in the range of 0 ms to connInterval value. Default Value: 0

22.1.54 BLE_BLELL_TRANSMIT_WINDOW_SIZE

Transmit window size

Address: 0x403C1084

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	TX_WINDOW_SIZE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	TX_WINDOW_SIZE	window_size along with the window_offset is used to calculate the first connection point anchor point for the master. This shall be a multiple of 1.25 ms in the range of 1.25 ms to the lesser of 10 ms and (connInter-val 1.25 ms). Values range from 0 to 10 ms. Default Value: 0

22.1.55 BLE_BLELL_DATA_CHANNELS_L0

Data channel map 0 (lower word)

Address: 0x403C1088

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA_CHANNELS_L0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA_CHANNELS_L0 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATA_CHANNELS_L0	This register field indicates which of the data channels are in use. This stores the information for the lower 16 (15:0) data channel indices. 1 indicates the corresponding data channel is used and 0 indicates the channel is unused. Default Value: 0

22.1.56 BLE_BLELL_DATA_CHANNELS_M0

Data channel map 0 (middle word)

Address: 0x403C108C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA_CHANNELS_M0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DATA_CHANNELS_M0 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATA_CHANNELS_M0	This register field indicates which of the data channels are in use. This stores the information for the middle 16 (32:16) data channel indices. 1 indicates the corresponding data channel is used and 0 indicates the channel is unused. Default Value: 0

22.1.57 BLE_BLELL_DATA_CHANNELS_H0

Data channel map 0 (upper word)

Address: 0x403C1090

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			R				
Name	None [7:5]			DATA_CHANNELS_H0 [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4 : 0	DATA_CHANNELS_H0	This register field indicates which of the data channels are in use. This stores the information for the upper 5 (36:32) data channel indices. 1 indicates the corresponding data channel is used and 0 indicates the channel is unused. Note: The Data channel map 0 and data channel map 1 are two sets of channel maps stored, common for all the connections. At any given time, only two maps can be maintained and the connections will use one of the two sets as indicated by the channel map index field in the CE_CNFG_STS registers specific to the link. Firmware must also manage to update this field along with the map. Default Value: 0

22.1.58 BLE_BLELL_DATA_CHANNELS_L1

Data channel map 1 (lower word)

Address: 0x403C1098

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA_CHANNELS_L1 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DATA_CHANNELS_L1 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATA_CHANNELS_L1	This register field indicates which of the data channels are in use. This stores the information for the lower 16 (15:0) data channel indices. 1 indicates the corresponding data channel is used and 0 indicates the channel is unused. Default Value: 0

22.1.59 BLE_BLELL_DATA_CHANNELS_M1

Data channel map 1 (middle word)

Address: 0x403C109C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA_CHANNELS_M1 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DATA_CHANNELS_M1 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATA_CHANNELS_M1	This register field indicates which of the data channels are in use. This stores the information for the middle 16 (32:16) data channel indices. 1 indicates the corresponding data channel is used and 0 indicates the channel is unused. Default Value: 0

22.1.60 BLE_BLELL_DATA_CHANNELS_H1

Data channel map 1 (upper word)

Address: 0x403C10A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			R				
Name	None [7:5]			DATA_CHANNELS_H1 [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4 : 0	DATA_CHANNELS_H1	This register field indicates which of the data channels are in use. This stores the information for the upper 5 data channel indices. 1 indicates the corresponding data channel is used and 0 indicates the channel is unused. Note: The Data channel map 0 and data channel map 1 are two sets of channel maps stored, common for all the connections. At any given time, only two maps can be maintained and the connections will use one of the two sets as indicated by the channel map index field in the CE_CNFG_STS registers specific to the link. Firmware must also manage to update this field along with the map. Default Value: 0

22.1.61 BLE_BLELL_CONN_INTR

Connection interrupt status and Clear register

Address: 0x403C10A8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	CON_UP-DT_DONE	CE_RX	CE_TX-_ACK	CLOSE_CE	START_CE	MAP_UP-DT_DONE	CON-N_ESTB	CONN_-CLOSED

Bits	15	14	13	12	11	10	9	8
SW Access	RW1C	RW1C	R			R		
HW Access	RW	RW	RW			RW		
Name	PING_NEARLY_EX-PIRD_INTR	PING_TIM-ER_EX-PIRD_INTR	RX_PDU_STATUS [13:11]			DISCON_STATUS [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15	PING_NEARLY_EX-PIRD_INTR	If this is set, it indicates that ping timer has nearly expired. If this bit is written with 1, it clears the interrupt. Default Value: 0
14	PING_TIMER_EX-PIRD_INTR	If this is set, it indicates that ping timer has expired. If this bit is written with 1, it clears the interrupt. Default Value: 0
13 : 11	RX_PDU_STATUS	Status of PDU received. This information is valid along with receive interrupt. xx1 Bad Packet (packet with CRC error) 000 empty PDU 010 - new data (non-empty) PDU 110 Duplicate Packet Default Value: 0

22.1.61 BLE_BLELL_CONN_INTR (continued)

10 : 8	DISCON_STATUS	Reason for disconnect indicates the reason the link is disconnected by hardware. 001 - connection failed to be established 010 - supervision timeout 011 - kill connection by host 100 - kill connection after ACK transmitted 101 - PDU response timer expired Default Value: 0
7	CON_UPDT_DONE	This bit is set when the last connection event with previous connec-tion parameters is reached. The bit is set immediately after the re-ceive operation at the anchor point of the last connection event. If this bit is written with 1, it clears the connection updated interrupt. Default Value: 0
6	CE_RX	If this bit is set it indicates that a packet is received in the connection event. If this bit is written with 1, it clears the connection event received interrupt. Default Value: 0
5	CE_TX_ACK	If this bit is set it indicates that the connection event transmission acknowledgement is received for the previous non-empty packet transmitted. If this bit is written with 1, it clears the ce transmission acknowledgement interrupt. Default Value: 0
4	CLOSE_CE	If this bit is set it indicates that the connection event closed interrupt has happened. If this bit is written with 1, it clears the connection event closed interrupt. Default Value: 0
3	START_CE	If this bit is set it indicates that the connection event started interrupt has happened. If this bit is written with 1, it clears the connection event started interrupt. Default Value: 0
2	MAP_UPDT_DONE	If this bit is set it indicates that the channel map update is completed at the instant specified by the firmware. If this bit is written with 1, it clears the map update done interrupt. Default Value: 0
1	CONN_ESTB	If this bit is set it indicates that the connection has been established. The bit is also set when a connection update procedure is complet-ed, at the start of the first anchor point with the updated parameters. If this bit is written with 1, it clears the connection established interrupt. Default Value: 0
0	CONN_CLOSED	If this bit is set it indicates that the link is disconnected. If this bit is written with 1, it clears the connection updated interrupt. Default Value: 0

22.1.62 BLE_BLELL_CONN_STATUS

Connection channel status

Address: 0x403C10AC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R				None			
HW Access	RW				None			
Name	RECEIVE_PACKET_COUNT [15:12]				None [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 12	RECEIVE_PACK-ET_COUNT	This field stores the count for the number of receive packets in the receive FIFO that are still not ready by firmware. The counter value is incremented by hardware for every good packet it stores in the FIFO. After firmware reads a packet, it decrements the counter by issuing the PACKET_RECEIVED command from the commander. Default Value: 0

22.1.63 BLE_BLELL_CONN_INDEX

Connection Index register

Address: 0x403C10B0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CONN_INDEX [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CONN_INDEX [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CONN_INDEX	This field is used to index the multiple connections existing. Range is 0 to maximum number of connections supported. For a single connection device, conn_index is 0. Default Value: 0

22.1.64 BLE_BLELL_WAKEUP_CONFIG

Wakeup configuration

Address: 0x403C10B8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	OSC_STARTUP_DELAY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW						None	
HW Access	R						None	
Name	DSM_OFFSET_TO_WAKEUP_INSTANT [15:10]						None [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 10	DSM_OFF-SET_TO_WAKEUP_IN-STANT	Number of slots before the wake up instant before which the hardware needs to exit from deep sleep mode. The slot is of 0.625ms period. This is a onetime configuration field, which is used every time hardware does an auto-wakeup before the next wakeup instant. Default Value: 0
7 : 0	OSC_STARTUP_DELAY	Oscillator stabilization/startup delay. This is in X.Y for-mat where X is in terms of number of BT slots (625 us) and Y is in terms of number of clock periods of 16KHz clock input, required for RF oscillator to stabilize the clock output to the controller on its output pin, after oscillator is turned ON. In this period the clock is as-sumed to be unstable, and so the controller does not turn on the clock to internal logic till this period is over. This means, the wake up from deep sleep mode must account for this delay before the wakeup instant. Osc_startup_delay[7:5] is number of slots(625us) Osc_startup_delay[4:0 is number of clock periods of 16KHz clock (Warning: Min. value of Osc_startup_delay [4:0] sup-ported is 1 and Max. value is 9. Therefore programma-ble range is 1 to 9) Default Value: 0

22.1.65 BLE_BLELL_WAKEUP_CONTROL

Wakeup control

Address: 0x403C10C0

Retention: Retained

Bits	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SW Access	RW							
HW Access	R							
Name	WAKEUP_INSTANT [7:0]							

Bits	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SW Access	RW							
HW Access	R							
Name	WAKEUP_INSTANT [15:8]							

Bits	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	**Name**	**Description**
15 : 0	WAKEUP_INSTANT	Instant, with reference to the internal 16-bit clock reference, at which the hardware must wakeup from deep sleep mode. This is calculated by firmware based on the next closest instant where a controller operation is required (like advertiser/scanner). Firmware reads the next instant of the procedures in the corresponding *_NEXT_INSTANT registers. This value is used only when hardware auto wakeup from deep sleep mode is enabled in the clock control register. Note: it is recommended to program wakeup_instant such a way that the actual instant to wake-up shall be at least two counts (two slots of 625 us) ahead of reference clock when entering DSM. The actual instant to wakeup is wakeup_instant dsm_offset_to_wakeup_instant osc_start-up_delay, and it shall be greater than reference clock + 2 Default Value: 0

22.1.66 BLE_BLELL_CLOCK_CONFIG

Clock control

Address: 0x403C10C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	RW	RW	RW	RW	RW	RW	RW
HW Access	RW	R	R	R	R	R	R	R
Name	LLH_IDLE	PHY_-CLK_GATE_EN	SY-SCLK_GATE_EN	CORE-CLK_GATE_EN	CONN_-CLK_GATE_EN	INIT_-CLK_GATE_EN	SCAN_-CLK_GATE_EN	ADV_-CLK_GATE_EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	None	RW	RW	RW
HW Access	R	R	R	R	None	R	R	R
Name	DEEP-_SLEEP_-MODE_EN	SLEEP_-MODE_EN	DEEP-_SLEEP_AUTO_WK-UP_DIS-ABLE	SM_IN-TR_EN	None	SM_AU-TO_WK-UP_EN	LPO_SEL_EXTERNAL	LPO_CLK_-FREQ_SEL

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15	DEEP_SLEEP_-MODE_EN	Enable deep sleep mode. 1 enable, 0 disable. Enables hardware logic related to deep sleep mode to control the deep sleep mode operation. If disabled, the related logic is not executed and hardware cannot enter deep sleep mode. Default Value: 0
14	SLEEP_MODE_EN	Enable sleep mode. 1 enable, 0 disable. Enables hardware to control sleep mode operation. This feature is not available. FW should never set this bit Default Value: 0
13	DEEP_SLEEP_AU-TO_WKUP_DISABLE	Disable Auto Wakeup in DEEP_SLEEP mode. 1 - Disable Auto Wakeup 0 - Auto Wakeup enabled Default Value: 0

22.1.66 BLE_BLELL_CLOCK_CONFIG (continued)

12	SM_INTR_EN	Enable SM exit interrupt. 1 enable, 0 disable. Enables hardware to generate an interrupt while exiting sleep mode irrespective of whether it is initiated by hardware or firmware. The interrupt is captured and stored till it gets cleared. Dis-abling this bit mask the sleep mode exit event from hardware & firmware. This feature is not available. FW should never set this bit Default Value: 0
10	SM_AUTO_WKUP_EN	Enable sleep mode auto wakeup enable. 1- enable, 0 disable. Enables hardware to automatically wakeup from sleep mode at the instant = wakeup_instant sm_offset_to_wakeup_instant. The wakeup_insant is the field in the wakeup control register de-scribed earlier. The sm_offset_to_wakeup_instant value is the field described in the wakeup con-figuration register. Default Value: 0
9	LPO_SEL_EXTERNAL	Select external sleep clock. 1 External clock, 0 - inter-nal generated clock. The field is used to select either the low power clock in-put on sleep_clk input pin(of frequency 16.384KHz) di-rectly to run the DSM logic or to use the internal gener-ated reference clock(of 16KHz) for the same. Default Value: 0
8	LPO_CLK_FREQ_SEL	Clock frequency select. 0 32KHz, 1 32.768KHz. Base frequency of the sleep_clk input used for generat-ing the internal reference clock of approx-imate 16Khz frequency. Default Value: 0
7	LLH_IDLE	Indicates if hardware is doing any transmit/receive operation. This information is used by firm-ware to decide to program the hardware into deep sleep mode. 1 LL hardware is idle. 0 LL hardware is busy. In this case LL hardware will not enter deep sleep mode, even if firmware gives an enter DSM command. (In this situation hardware generates dsm exit interrupt to inform firmware that DSM entry was not successful). Default Value: 1
6	PHY_CLK_GATE_EN	Digital PHY clock enable. 1- enable, 0-disable. Enable the Digital PHY to shutdown the clock. When 1, it indicates that controller has an upcom-ing activity so PHY clock must be turned ON. When 0, it indicates inactivity in the controller. Default Value: 0
5	SYSCLK_GATE_EN	Sysclk gate enable. 1- enable, 0 disable. Enables clock gating of system clock input to the link layer. If 1, it enables the DSM logic to con-trol the clock gate for system clock input from pin. If 0, the DSM logic has no control and the sys-tem clock is always ON. Default Value: 0
4	CORECLK_GATE_EN	Core clock gate enable. 1 enable, 0 disable. Enables gating of clock to the llh_core module in hard-ware. If 1, the sleep mode/deep sleep mode logic can control the clock gate to shutdown/wakeup the clock to the module. If 0, the logic has no control and clock is always turned ON. Default Value: 0
3	CONN_CLK_GATE_EN	Connection block clock gate enable. 1 enable, 0 disable. Enables gating of clock to the connection module (llh_connch_top) in hardware. If 1, the sleep mode logic can control the clock gate to shutdown/wakeup the clock to the engine. If 0, the logic has no control and clock to the module is always turned ON. Default Value: 0
2	INIT_CLK_GATE_EN	Initiator block clock gate enable. 1 enable, 0 disable. Enables gating of clock to the initiator module (llh_init). If 1, the sleep mode logic can control the clock gate to shutdown/wakeup the clock to the module. If 0, the logic has no control and clock to the module is always turned ON. Default Value: 0

22.1.66 BLE_BLELL_CLOCK_CONFIG (continued)

1	SCAN_CLK_GATE_EN	Scan block clock gate enable. 1 enable, 0 disable. Enables gating of clock to the scanner module (llh_scan) in hardware. If 1, the sleep mode logic can control the clock gate to shutdown/wakeup the clock to the module. If 0, the logic has no control and clock to the module is always turned ON. Default Value: 0
0	ADV_CLK_GATE_EN	Advertiser block clock gate enable. 1 enable, 0 disable. Enables gating of clock to the advertiser module (llh_adv) in hardware. If 1, the sleep mode logic can control the clock gate to shutdown/wakeup the clock to the module. If 0, the logic has no control and clock to the module is always turned ON. Default Value: 0

22.1.67 BLE_BLELL_TIM_COUNTER_L

Reference Clock

Address: 0x403C10C8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	TIM_REF_CLOCK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	TIM_REF_CLOCK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	TIM_REF_CLOCK	16-bit internal reference clock. The clock is a free run-ning clock, incremented by a 0.625ms pe-riodic pulse. It is used as a reference clock to derive all the timing required as per protocol. Default Value: 0

22.1.68 BLE_BLELL_WAKEUP_CONFIG_EXTD

Wakeup configuration extended

Address: 0x403C10CC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			R				
Name	None [7:5]			DSM_LF_OFFSET [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4 : 0	DSM_LF_OFFSET	Number of LF slots before the wake up instant before which the hardware needs to exit from deep sleep mode. The LF slot is of 62.5us period. This is a onetime configuration field, which is used every time hardware does an auto-wakeup before the next wakeup instant. This is in addition to the LF slots calculated by HW window widening logic. Default Value: 0

22.1.69 BLE_BLELL_POC_REG__TIM_CONTROL

BLE Time Control

Address: 0x403C10D8

Retention: Retained

Bits	7	6	5	4	3	2			1	0
SW Access	RW					None				
HW Access	RW					None				
Name	BB_CLK_FREQ_MINUS_1 [7:3]					None [2:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				RW			
Name	None [15:12]				START_SLOT_OFFSET [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11 : 8	START_SLOT_OFFSET	LLH clock configuration. The start of slot signal is offset by this value. If value is 0, the start of slot signal is generated at the 625us. The offset value is in terms of us. Default Value: 0
7 : 3	BB_CLK_FREQ_MI-NUS_1	LLH clock configuration. The clock frequency of the clock input to this design is configured in this register. This is used to derive a 1MHz clock. Default Value: 0

22.1.70 BLE_BLELL_ADV_TX_DATA_FIFO

Advertising data transmit FIFO. Access ADVCH_TX_FIFO.

Address: 0x403C10E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	ADV_TX_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	ADV_TX_DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	ADV_TX_DATA	IO mapped FIFO of depth 16 (2 byte wide), to store ADV data of maximum length 31 bytes for transmitting. Firmware writes consecutive words by writing to the same address location. Note: ADV_TX_DATA_FIFO and ADV_SCN_RSP_TX_FIFO shares same physical FIFO of depth 32. 16 locations for each FIFO are allocated. Reading this location resets the FIFO pointer. Default Value: 0

22.1.71 BLE_BLELL_ADV_SCN_RSP_TX_FIFO

Advertising scan response data transmit FIFO. Access ADVCH_TX_FIFO.

Address: 0x403C10E8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SCAN_RSP_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	SCAN_RSP_DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	SCAN_RSP_DATA	IO mapped FIFO of depth 16 (2 byte wide), to store scan response data of maximum length 31 bytes for transmitting. Firmware writes consecutive words by writing to the same location. Note: ADV_TX_DATA_FIFO and ADV_SCN_RSP_TX_FIFO shares same physical FIFO of depth 32. 16 locations for each FIFO are allocated. Reading this location resets the FIFO pointer. Default Value: 0

22.1.72 BLE_BLELL_INIT_SCN_ADV_RX_FIFO

advertising scan response data receive data FIFO. Access ADVRX_FIFO.

Address: 0x403C10F8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	ADV_SCAN_RSP_RX_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	ADV_SCAN_RSP_RX_DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	ADV_SCAN_RSP_RX_-DATA	IO mapped FIFO of depth 64, to store ADV and SCAN_RSP header and payload received by the scanner. The RSSI value at the time of reception of this packet is also stored. Firmware reads from the same address to read out consecutive words of data. Note: The 16 bit header is first loaded to the advertise channel data receive FIFO followed by the payload data and then 16 bit RSSI. Default Value: 0

22.1.73 BLE_BLELL_CONN_INTERVAL

Connection Interval

Address: 0x403C1100

Retention: Retained

Bits	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SW Access	RW							
HW Access	RW							
Name	CONNECTION_INTERVAL [7:0]							
Bits	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SW Access	RW							
HW Access	RW							
Name	CONNECTION_INTERVAL [15:8]							
Bits	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SW Access	None							
HW Access	None							
Name	None [23:16]							
Bits	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	**Name**	**Description**
15 : 0	CONNECTION_INTER-VAL	The value configured in this register determines the spacing be-tween the connection events. This shall be a multiple of 1.25 ms in the range of 7.5 ms to 4.0 s. Default Value: 0

22.1.74 BLE_BLELL_SUP_TIMEOUT

Supervision timeout

Address: 0x403C1104

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	SUPERVISION_TIMEOUT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	SUPERVISION_TIMEOUT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	SUPERVISION_TIMEOUT	This field defines the maximum time between two received Data packet PDUs before the connection is considered lost. This shall be a multiple of 10 ms in the range of 100 ms to 32.0 s and it shall be larger than (1+connSlaveLatency)*connInterval. Default Value: 0

22.1.75 BLE_BLELL_SLAVE_LATENCY

Slave Latency

Address: 0x403C1108

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	SLAVE_LATENCY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	SLAVE_LATENCY [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	SLAVE_LATENCY	The value configured in this field defines the number of consecutive connection events that the slave device is not required to listen for master. The value of connSlaveLatency should not cause a Supervision Timeout. This shall be an integer in the range of 0 to ((connSupervision Timeout/connInterval)-1). connSlaveLatency shall also be less than 500. Default Value: 0

22.1.76 BLE_BLELL_CE_LENGTH

Connection event length

Address: 0x403C110C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CONNECTION_EVENT_LENGTH [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CONNECTION_EVENT_LENGTH [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description

22.1.76 BLE_BLELL_CE_LENGTH (continued)

15 : 0	CONNECTION_EVENT_LENGTH	This field defines the length of Connection event. This value is derived from the CE length HCI parameters received from the host. This determines the number of master transmit slots in a connection event, subject to either of the MD bits being set. If both MD bits are set to 0, this has no effect. Units: 625us Note: The connection event length as specified by the CE_LENGTH shall not exceed CONN_INTERVAL 1.25 ms. The CE-length parameter, according to the Bluetooth specification, is the length of the connection event. Take an example to illustrate this scenario: Assume a connection with interval = 100ms. that the application has put allowed 20ms of CE-length. Here, the CE-length can be upto 100ms (100ms - 150us to be exact). If the connection is maintained for 5 minutes, there could be 10*60*5 = 3000 connection-intervals. The CE-length need not be maintained constant during all the 3000 connection events. Here are the typical cases that determine the value of CE-length: (1) No data packets exchanged. we are just maintaining time and frequency synchronization. In this case, only a packet pair will be exchanged every connection interval. Here, CE-length = 1. (2) Average of 10 packets to be sent per connection event. We can pump data in multiple ways here: 2.1: Send data at uniform rate : In this case, the CE-length will be enough to accommodate 10 packets, which will take about 7ms. As this is less than application enforced limit of 20ms, we can comfortably push all the 10 data packets in this connection interval. So data will be pumped to the other BT device at the same rate as is received from my application. 2.2: Can send data in bursts. Assume that we accumulate data for 1 second and pump out at the end of 1 second(this is not done by our Bluetooth stack, the application needs to buffer the data). So, at 10th connection interval, we have 100 packets accumulated. We are now ready to pump this data. 100 packets take about 70 ms. This is above the application enforced 20ms. So, the hardware can pump data that can fill up 20ms. The remaining data will be deferred to the next connection interval. So, in this case, you would see a CE-length spread over time like this (Per connection interval): 0,0,0,0,0,0,0,0,0,0, 20,20,20,10,0,0,0,0,0,0, 20,20,20,10,0,0,0,0,0,0, 20,20,20,10,0,0,0,0,0,0, and so on. (3) We are receiving data at the same rate as in (2). This case is to honor data sent by the other BT-device by giving it more time in the current connection interval. In (2) and (3) you will see non-empty packets either transmitted or received. We can also utilize the CE-length for different reasons: (4) A transaction is in progress, and we are expecting a response packet very soon. In this case, we may be exchanging only empty packets now, and in the next few packet-pairs. In this case, you will the CE-length to be large, and a non-empty packet may not be exchanged in all the slots. Default Value: 0

22.1.77 BLE_BLELL_PDU_ACCESS_ADDR_L_REGISTER

Access address (lower)

Address: 0x403C1110

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	PDU_ACCESS_ADDRESS_LOWER_BITS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PDU_ACCESS_ADDRESS_LOWER_BITS [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	PDU_ACCESS_ADDRESS_LOWER_BITS	This field defines the lower 16 bits of the access address for each Link layer connection between any two devices. Default Value: 0

22.1.78 BLE_BLELL_PDU_ACCESS_ADDR_H_REGISTER

Access address (upper)

Address: 0x403C1114

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	PDU_ACCESS_ADDRESS_HIGHER_BITS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PDU_ACCESS_ADDRESS_HIGHER_BITS [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	PDU_ACCESS_ADDRESS_HIGHER_BITS	This field defines the higher 16 bits of the access address for each Link layer connection between any two devices. Default Value: 0

22.1.79 BLE_BLELL_CONN_CE_INSTANT

Connection event instant

Address: 0x403C1118

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CE_INSTANT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CE_INSTANT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CE_INSTANT	This is the value of the free running Connection Event counter when the new parameters of connection update and/or Channel map update will be effective. Range : 0x0000 to 0xFFFF Default Value: 0

22.1.80 BLE_BLELL_CE_CNFG_STS_REGISTER

connection configuration & status register

Address: 0x403C111C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW			
HW Access	RW	R	R	R	R			
Name	MAP_IN-DEX-__CURR_INDEX	MD	SPARE	DATA_LIST_HEAD_UP	DATA_LIST_INDEX_LAST_ACK_INDEX [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	R				None	R	None	RW
HW Access	RW				None	RW	None	R
Name	CURRENT_PDU_INDEX [15:12]				None	CONN_AC-TIVE	None	PAUSE_-DATA

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 12	CURRENT_PDU_INDEX	The index of the transmit packet buffer that is currently in transmission/waiting for transmission. Default Value: 0
10	CONN_ACTIVE	This bit is 1 whenever the connection is active. Default Value: 0
8	PAUSE_DATA	Pause data. 1 - pause data, 0 - do not pause. The current_pdu_index in hardware does not move to next in-dex until pause_data is cleared. But if the SENT bit is set for the current_pdu_index as which pause is set, data will be sent out Default Value: 0
7	MAP_INDEX__CURR_IN-DEX	Written by firmware to select the map index to be used by hardware for this connection. 1 - use channel map register set 1. 0 - use channel map register set 0. When firmware reads this field, it returns the current map index being used in hardware. Default Value: 0

22.1.80 BLE_BLELL_CE_CNFG_STS_REGISTER (continued)

6	MD	MD bit set to 1 indicates device has more data to be sent. Default Value: 0
5	SPARE	This bit is unused Default Value: 0
4	DATA_LIST_HEAD_UP	Update the first packet buffer index ready for transmis-sion to start/resume data transfer after a pause. The bit must be toggled every time the firmware needs to indicate the start/resume. This requires a read modify write operation. Default Value: 0
3 : 0	DATA_LIST_INDEX-_LAST_ACK_INDEX	Data list index for start/resume. This field must be valid along with data_list_head_up and indi-cate the transmit packet buffer index at which the data is loaded. The default number of buffers in the IP is 5,but may be customized for a customer. The buffers are in-dexed 0 to 4. Hardware will start the next data transmission from the index indicated by this field. Default Value: 0

22.1.81 BLE_BLELL_NEXT_CE_INSTANT

Next connection event instant

Address: 0x403C1120

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	NEXT_CE_INSTANT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	NEXT_CE_INSTANT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	NEXT_CE_INSTANT	16-bit internal reference clock value at which the next connection event will occur on a connection. The connection index register must be programmed with index of the connection, before reading the register. The reset value is 0x0000. After reset deassertion, then the very next clock, the value assigned to the registers is 0xFFFF. Default Value: 65535

22.1.82 BLE_BLELL_CONN_CE_COUNTER

connection event counter

Address: 0x403C1124

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	CONNECTION_EVENT_COUNTER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	CONNECTION_EVENT_COUNTER [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CONNEC-TION_EVENT_COUNTER	This is the free running counter, connEventCounter as defined by Bluetooth spec. Firmware will read the instantaneous Event counter from this register, during connection update and channel map update procedure. Firmware will use this value to calculate the instant from which the new parameters (for connection update and channel map update) will be effective. Default Value: 0

22.1.83 BLE_BLELL_DATA_LIST_SENT_UPDATE__STATUS

data list sent update and status

Address: 0x403C1128

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W	None			RW			
HW Access	RW	None			RW			
Name	SET_-CLEAR	None [6:4]			LIST_INDEX__TX_SENT_3_0 [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	SET_CLEAR	Write: Used to set the SENT bit in hardware for the selected packet buffer. 1 packet queued When firmware has a packet to send, firmware first loads the next available packet buffer. Then the hardware SENT bit is set by writing 1 to this bit field along with the list_index field that identified the buffer index. This indicates that a packet has been queued in the data buffer for sending. This packet is now ready to be transmitted. The SENT bit in hardware is cleared by hardware only when it has received an acknowledgement from the remote device. Firmware typically does not clear the bit. However, It only clears the bit on its own if it needs to flush a packet from the buffer, without waiting to receive acknowledgement from the remote device, firmware clears BIT7 along with the list_index specified. Default Value: 0

22.1.83 BLE_BLELL_DATA_LIST_SENT_UPDATE__STATUS (continued)

3 : 0	LIST_INDEX__TX-_SENT_3_0	Write:Indicates the buffer index for which the SENT bit is being updated by firmware. The default number of buffers in the IP is 4. The index range is 0-3. Read: Reads TX_SENT[3:0]. The bits in this field indicate the status of the SENT bit in the hard-ware for each packet buffer. The bit values are 1 queued 0 no packet / packet ack received by hardware Example1: If the read value is : 0x03, then packets in buffer 0 and buffer 1 are in the queue to be transmitted. All the other FIFOs are empty or hardware has cleared them after receiving ac-knowledgement. NOTE: The SENT status bit and ACK status bit have to be taken together to understand the meaning of packet status. The table below describes how the two bits are sequentially updated by either hardware/firmware to complete one data transmission. SENT ACK Description 0 0 Buffer is empty. No packet is queued in the buffer 1 0 Packet is queued by firmware. 1 1 Packet is transmitted by hardware. Hardware is waiting for acknowledgement. 0 1 Hardware has received ACK. Firmware has not yet processed the ACK. 0 0 Firmware has processed the ack. The buffer is again empty. Default Value: 0

22.1.84 BLE_BLELL_DATA_LIST_ACK_UPDATE__STATUS

data list ack update and status

Address: 0x403C112C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W	None			RW			
HW Access	RW	None			RW			
Name	SET_-CLEAR	None [6:4]			LIST_INDEX__TX_ACK_3_0 [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	SET_CLEAR	Write: Firmware uses the field to clear and ACK bit in the hardware to indicate that the acknowledgement for the transmit packet has been received and processed by firmware. Firmware clears the ACK bit in the hardware by writing in this register only after the acknowledgement is processed successfully by firmware. For clearing ack for a packet transmitted in fifo-index : 3, firm-ware will write 3 in the list-index field and set this bit (BIT7) to 0. This is the indication that the corresponding packet buffer identi-fied by List-Index is cleared of previous transmission and can be re-used for another packet from now on. The ACK bit in hardware is set by hardware when it has success-fully transmitted a packet. Default Value: 0

22.1.84 BLE_BLELL_DATA_LIST_ACK_UPDATE__STATUS (continued)

3 : 0	LIST_INDEX__TX-_ACK_3_0	Write: Indicates the buffer index for which the ACK bit is being updated by firmware. The default number of buffers in the IP is 5. The index range is 0-4. Read: Reads TX_ACK[3:0] If a particular bit is set, then the packet in the selected buffer has been transmitted (at least once) by the hardware and hardware is waiting for acknowledgement. Example1 : If the read value is : 0x03, then packets in FIFO-0 and FIFO-1 are acknowledged by the remote device. These acknowledgements are pending to be processed by firmware. Example2 : If the read value is : 0x02, then packet FIFO-1 is acknowledged by the remote device. This acknowledgement is pending to be processed by firmware. NOTE: The SENT status bit and ACK status bit have to be taken together to understand the meaning of packet status. The table below describes how the two bits are sequentially updated by either hardware/firmware to complete one data transmission. SENT ACK Description 0 0 Buffer is empty. No packet is queued in the buffer 1 0 Packet is queued by firmware. 1 1 Packet is transmitted by hardware. Hardware is waiting for acknowledgement. 0 1 Hardware has received ACK. Firmware has not yet processed the ACK. 0 0 Firmware has processed the ack. The buffer is again empty. Default Value: 0

22.1.85 BLE_BLELL_CE_CNFG_STS_REGISTER_EXT

connection configuration & status register

Address: 0x403C1130

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [7:4]				NESN	SN	rx_2m	tx_2m

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW					
HW Access	None		R					
Name	None [15:14]		LAST_UNMAPPED_CHANNEL [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
13 : 8	LAST_UN-MAPPED_CHANNEL	Last unmapped channel for next scheduled connection index Default Value: 0
3	NESN	Next Sequence number for next scheduled connection index Default Value: 0
2	SN	Sequence number for next scheduled connection index Default Value: 0
1	rx_2m	receiving on 2M Default Value: 0
0	tx_2m	transmittion on 2M Default Value: 0

22.1.86 BLE_BLELL_CONN_EXT_INTR

Connection extended interrupt status and Clear register

Address: 0x403C1134

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW1C	RW1C	RW1C
HW Access	None					RW	RW	RW
Name	None [7:3]					GEN_TIM-ER_INTR	EARLY_IN-TR	DATA-RATE_UP-DATE

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	GEN_TIMER_INTR	If this bit is set it indicates that the generic timer (PDU response timer reconfigured in MMMS mode) has expired If this bit is written with 1, it clears the interrupt status bit Default Value: 0
1	EARLY_INTR	For master this bit is set on start_ce For Slave this bit is set on slave_timer_adj Default Value: 0
0	DATARATE_UPDATE	If this bit is set it indicates that the data rate is updated If this bit is written with 1, it clears the interrupt status bit Default Value: 0

22.1.87 BLE_BLELL_CONN_EXT_INTR_MASK

Connection Extended Interrupt mask

Address: 0x403C1138

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [7:3]					GEN_TIM-ER_INTR	EARLY_IN-TR	DATA-RATE_UP-DATE

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	GEN_TIMER_INTR	Generic timer (PDU response timer reconfigured in MMMS mode) expiry interrupt Default Value: 0
1	EARLY_INTR	If this bit is set connection early interrupt is enabled. Default Value: 0
0	DATARATE_UPDATE	If this bit is set connection data rate update interrupt is enabled. Default Value: 0

22.1.88 BLE_BLELL_DATA_MEM_DESCRIPTOR0

Data buffer descriptor 0 to 4

Address: 0x403C1140

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW						RW	
HW Access	R						R	
Name	DATA_LENGTH [7:2]						LLID [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						DATA_LENGTH [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 2	DATA_LENGTH	This field indicates the length of the data packet. Bits [9:7] are valid only if DLE is set. Range 0x00 to 0xFF. Default Value: 0
1 : 0	LLID	The LLID indicates whether the packet is an LL Data PDU or an LL Control PDU. 00b= Reserved. 01b=LL Data PDU: Continuation fragment of an L2CAP message or an Empty PDU. 10b=LL Data PDU: Start of an L@CAP message or a complete L2CAP message with no fragmentation. 11b=LL Control PDU. Default Value: 0

22.1.89 BLE_BLELL_WINDOW_WIDEN_INTVL

Window widen for interval

Address: 0x403C1160

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	WINDOW_WIDEN_INTVL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				WINDOW_WIDEN_INTVL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11 : 0	WINDOW_WIDEN_INTVL	This value defines the increased listening time for the slave. The window widening shall be smaller than ((connInterval/2)-T_IFS us) This value is calculated by firmware based on the drift, the connec-tion interval value. The value is the unit widening value for one con-nection interval duration. In case of slave latency, this val-ue is accu-mulated till the next anchor point at which the slave will listen. Default Value: 10

22.1.90 BLE_BLELL_WINDOW_WIDEN_WINOFF

Window widen for offset

Address: 0x403C1164

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	WINDOW_WIDEN_WINOFF [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				WINDOW_WIDEN_WINOFF [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11 : 0	WINDOW_WID-EN_WINOFF	This field stores the additional number of microseconds the slave must extend its listening win-dow to listen for a master packet. This value is calculated based on the window offset value. This is used at connection setup directly. During connection setup, this value is added with win-dow_widen_intvl register value to calculate the win-dow widening size. Default Value: 10

22.1.91 BLE_BLELL_LE_RF_TEST_MODE

Direct Test Mode control

Address: 0x403C1170

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW					
HW Access	R	RW	R					
Name	PKT_PAY-LOAD	DTM_STA-TUS__DT-M_CONT_RXEN	TEST_FREQUENCY [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	RW	None	RW	None			RW	
HW Access	R	None	R	None			R	
Name	DTM_-DATA_2MBPS	None	DTM_CON-T_TXEN	None [12:10]			PKT_PAYLOAD [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15	DTM_DATA_2MBPS	0: DTM run at 1M bps data rate 1: DTM run at 2M bps data rate Default Value: 0
13	DTM_CONT_TXEN	0: DTM run at normal DTMTX burst mode 1: DTM run at continuous TX DTM mode Default Value: 0

22.1.91 BLE_BLELL_LE_RF_TEST_MODE (continued)

9 : 7	PKT_PAYLOAD	Payload type as per the HCI parameter. 0x00 Pseudo-Random bit sequence 9 0x01 Pattern of alter-nating bits 11110000 0x02 Pattern of alternating bits 10101010 0x03 Pseudo-Random bit sequence 15 0x04 Pat-tern of All 1 bits 0x05 Pattern of All 0 bits 0x06 Pattern of alternating bits 00001111 0x07 Pattern of alternating bits 0101 0x08-0xFF Reserved for future use Default Value: 0
6	DTM_STATUS__DTM_-CONT_RXEN	This bit is overloaded. The read operation returns the staus of the DTM 1 - DTM test ON 0 - DTM test OFF The write operation contrls the DTM RX mode 0: DTM run at normal DTMRX burst mode 1: DTM run at continuous RX DTM mode Default Value: 0
5 : 0	TEST_FREQUENCY	N = (F 2402) / 2 Range: 0x00 0x27. Frequency Range : 2402 MHz to 2480 MHz Default Value: 0

22.1.92 BLE_BLELL_DTM_RX_PKT_COUNT

Direct Test Mode receive packet count

Address: 0x403C1174

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	RX_PACKET_COUNT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	RX_PACKET_COUNT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	RX_PACKET_COUNT	Number of packets received in receive test mode. Default Value: 0

22.1.93 BLE_BLELL_LE_RF_TEST_MODE_EXT

Direct Test Mode control

Address: 0x403C1178

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DTM_PACKET_LENGTH [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DTM_PACKET_LENGTH	DTM TX packet length. Bits [7:6] are accessible onle when DLE is enabled Default Value: 0

22.1.94 BLE_BLELL_TXRX_HOP

Channel Address register

Address: 0x403C1188

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	R						
HW Access	None	RW						
Name	None	HOP_CH_TX [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None	R						
HW Access	None	RW						
Name	None	HOP_CH_RX [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
14 : 8	HOP_CH_RX	Receive channel index. Channel index on which previous packet is received. Default Value: 0
6 : 0	HOP_CH_TX	Transmit channel index. Channel index on which previous packet is transmitted. Default Value: 0

22.1.95 BLE_BLELL_TX_RX_ON_DELAY

Transmit/Receive data delay

Address: 0x403C1190

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	RXON_DELAY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	TXON_DELAY [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 8	TXON_DELAY	Transmit delay Delay from start of transmit to transmission of first bit on air. It is used to control the T_IFS. The delay is in resolution of 1 microsecond. Default Value: 0
7 : 0	RXON_DELAY	Receive delay Delay from start of receive to expected first bit of receive packet at the controller. Used to control the turn on time of radio to optimize on power. The delay is in resolution of 1 microsecond. Default Value: 0

22.1.96 BLE_BLELL_ADV_ACCADDR_L

ADV packet access code low word

Address: 0x403C11A8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADV_ACCADDR_L [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADV_ACCADDR_L [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	ADV_ACCADDR_L	Lower 16 bit of ADV packet access code Default Value: 48854

22.1.97 BLE_BLELL_ADV_ACCADDR_H

ADV packet access code high word

Address: 0x403C11AC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADV_ACCADDR_H [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADV_ACCADDR_H [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	ADV_ACCADDR_H	higher 16 bit of ADV packet access code Default Value: 36489

22.1.98 BLE_BLELL_ADV_CH_TX_POWER_LVL_LS

Advertising channel transmit power setting

Address: 0x403C11B0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	ADV_TRANSMIT_POWER_LVL_LS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	ADV_TRANSMIT_POWER_LVL_LS [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	ADV_TRANSMIT_POW-ER_LVL_LS	When LL_CONFIG.TX_PA_PWR_LVL_TYPE is 1, this field represents the Advertising channel transmit power setting Least Significant 16 bits. When LL_CONFIG.TX_PA_PWR_LVL_TYPE is 0, the LS 4 bits represents the Advertising channel transmit power code 4 bits. Default Value: 0

22.1.99 BLE_BLELL_ADV_CH_TX_POWER_LVL_MS

Advertising channel transmit power setting extension

Address: 0x403C11B4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	
HW Access	None						R	
Name	None [7:2]						ADV_TRANSMIT_POWER_LVL_MS [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1 : 0	ADV_TRANSMIT_POWER_LVL_MS	Advertising channel transmit power setting Most Significant 2 bits. Default Value: 0

22.1.100 BLE_BLELL_CONN_CH_TX_POWER_LVL_LS

Connection channel transmit power setting

Address: 0x403C11B8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CONNCH_TRANSMIT_POWER_LVL_LS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CONNCH_TRANSMIT_POWER_LVL_LS [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CONNCH_TRANS-MIT_POWER_LVL_LS	When LL_CONFIG.TX_PA_PWR_LVL_TYPE is 1, this field represents the Connection channel transmit power setting Least Significant 16 bits. When LL_CONFIG.TX_PA_PWR_LVL_TYPE is 0, the LS 4 bits represents the Connection channel transmit power code 4 bits. Default Value: 0

22.1.101 BLE_BLELL_CONN_CH_TX_POWER_LVL_MS

Connection channel transmit power setting extension

Address: 0x403C11BC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	
HW Access	None						R	
Name	None [7:2]						CONNCH_TRANSMIT_POWER_LVL_MS [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1 : 0	CONNCH_TRANSMIT_POWER_LVL_MS	Connection channel transmit power setting Most Significant 2 bits. Default Value: 0

22.1.102 BLE_BLELL_DEV_PUB_ADDR_L

Device public address lower register

Address: 0x403C11C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DEV_PUB_ADDR_L [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DEV_PUB_ADDR_L [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DEV_PUB_ADDR_L	Lower 16 bit of 48-bit public address of the device. Default Value: 13330

22.1.103 BLE_BLELL_DEV_PUB_ADDR_M

Device public address middle register

Address: 0x403C11C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DEV_PUB_ADDR_M [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DEV_PUB_ADDR_M [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DEV_PUB_ADDR_M	Middle 16 bit of 48-bit public address of the device. Default Value: 86

22.1.104 BLE_BLELL_DEV_PUB_ADDR_H

Device public address higher register

Address: 0x403C11C8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DEV_PUB_ADDR_H [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DEV_PUB_ADDR_H [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DEV_PUB_ADDR_H	Higher 16 bit of 48-bit public address of the device. Default Value: 0

22.1.105 BLE_BLELL_OFFSET_TO_FIRST_INSTANT

Offset to first instant

Address: 0x403C11D0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	OFFSET_TO_FIRST_EVENT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	OFFSET_TO_FIRST_EVENT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	OFFSET_TO_- FIRST_EVENT	The offset w.r.t the internal reference clock at which instant the first event occurs. This register will give flexibility to the firmware to position the con-nection at a desired point with respect to the internal free running clock. It is optional to be updated by firmware. This is not up-dated in the current firmware. Default Value: 6

22.1.106 BLE_BLELL_ADV_CONFIG

Advertiser configuration register

Address: 0x403C11D4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	ADV_TIME-OUT_EN	SLV_CON-NECT-ED_EN	ADV_CON-N_REQ_RX_EN	AD-V_SCN_REQ_RX_EN	SCN_R-SP_TX_EN	ADV_TX-_EN	ADV_-CLS_EN	AD-V_STRT_EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW					RW	RW	RW
HW Access	R					R	R	R
Name	ADV_PKT_INTERVAL [15:11]					ADV_CON-N_PEER_RPA_UN-MCH_EN	AD-V_SCN_PEER_R-PA_UN-MCH_EN	AD-V_RAND_-DISABLE

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 11	ADV_PKT_INTERVAL	Time between the beginning of two consecutive advertising PDUs. Time = N * 0.625 msec Time Range: <=10msec. Default Value: 4
10	ADV_CONN_PEER_R-PA_UNMCH_EN	Enable connect request packet received with peer device address unmatched interrupt. This bit is valid only if PRIV_1_2 and PRIV_1_2_ADV are set. Default Value: 0
9	ADV_SCN_PEER_R-PA_UNMCH_EN	Enable scan request packet received with peer device address unmatched interrupt. This bit is valid only if PRIV_1_2 PRIV_1_2 and PRIV_1_2_ADV are set. Default Value: 0
8	ADV_RAND_DISABLE	Disable randomization of adv interval. When disabled, interval is same as programmed in ad-v_interval register. Default Value: 0

22.1.106 BLE_BLELL_ADV_CONFIG (continued)

7	ADV_TIMEOUT_EN	Enable adv_timeout interrupt. Applicable in adv_direct_ind advertising. Default Value: 1
6	SLV_CONNECTED_EN	Enable slave connected interrupt. Default Value: 1
5	ADV_CONN_REQ_RX-_EN	Enable connect request packet received interrupt. Default Value: 1
4	ADV_SCN_REQ_RX_EN	Enable scan request packet received interrupt. Default Value: 1
3	SCN_RSP_TX_EN	Enable scan response packet transmitted interrupt. Default Value: 1
2	ADV_TX_EN	Enable adv packet transmitted interrupt. Default Value: 1
1	ADV_CLS_EN	Enable advertising event stop interrupt. Default Value: 1
0	ADV_STRT_EN	Enable advertising event start interrupt. Default Value: 1

22.1.107 BLE_BLELL_SCAN_CONFIG

Scan configuration register

Address: 0x403C11D8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	SCANA_TX_AD-DR_NOT_SET_IN-TR_EN	SCN_AD-V_RX_IN-TR_SELF_RPA_UN-MCH_EN	SCN_AD-V_RX_IN-TR_PEER_RPA_UN-MCH_EN	SCN_R-SP_RX_EN	ADV_RX-_EN	SCN_TX-_EN	SCN_-CLOSE_EN	SCN_STRT_EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW			None	RW	None		RW
HW Access	R			None	R	None		R
Name	SCAN_CHANNEL_MAP [15:13]			None	BACK-OFF_EN-ABLE	None [10:9]		RPT_-SELF_AD-DR_MATCH_PRIV_MISMATCH_SCN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 13	SCAN_CHANNEL_MAP	Advertising channels that are enabled for scanning operation. Bit 15: setting 1 - enables channel 39 for use. Bit 14: setting 1 - enables channel 38 for use. Bit 13: setting 1 - enables channel 37 for use. Default Value: 7
11	BACKOFF_ENABLE	Enable random backoff feature in scanner. 1 - enable 0 - disable Default Value: 0

22.1.107 BLE_BLELL_SCAN_CONFIG (continued)

8	RPT_SELF_ADDR_-MATCH_PRIV_MIS-MATCH_SCN	This bit controls the SCAN engine behavior when an self address match occurs but a privacy mismatch occurs 0 - The packet is aborted 1 - The packet is received and reported to the Link Layer firmware This bit is valid only if PRIV_1_2 and PRIV_1_2_SCAN are set. Default Value: 0
7	SCANA_TX_AD-DR_NOT_SET_INTR_EN	Enable SCANA RPA TX not set interrupt. This bit is valid only if PRIV_1_2 and PRIV_1_2_SCAN are set. Default Value: 0
6	SCN_ADV_RX_INTR_-SELF_RPA_UNMCH_EN	Enable ADV self address unmatched interrupt. This bit is valid only if PRIV_1_2 PRIV_1_2 and PRIV_1_2_SCAN are set. Default Value: 0
5	SCN_ADV_RX_IN-TR_PEER_RPA_UN-MCH_EN	Enable ADV peer address unmatched interrupt. This bit is valid only if PRIV_1_2 PRIV_1_2 and PRIV_1_2_SCAN are set. Default Value: 0
4	SCN_RSP_RX_EN	Enable scan_rsp packet received interrupt . Default Value: 1
3	ADV_RX_EN	Enable adv packet received interrupt . Default Value: 1
2	SCN_TX_EN	Enable scan request packet transmitted interrupt. Default Value: 1
1	SCN_CLOSE_EN	Enable scan event close interrupt. Default Value: 1
0	SCN_STRT_EN	Enable scan event start interrupt. Default Value: 1

22.1.108 BLE_BLELL_INIT_CONFIG

Initiator configuration register

Address: 0x403C11DC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	None	RW	RW	RW
HW Access	R	R	R	R	None	R	R	R
Name	INITA_TX-_AD-DR_NOT_SET_IN-TR_EN	INIT_AD-V_RX_IN-TR_PEER_RPA_UN-RES_EN	INIT_AD-V_RX_IN-TR_SELF_RPA_UN-RES_EN	CON-N_CREAT-ED	None	CON-N_REQ_TX_EN	INIT_-CLOSE_EN	INIT_STRT_EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW			None				
HW Access	R			None				
Name	INIT_CHANNEL_MAP [15:13]			None [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 13	INIT_CHANNEL_MAP	Advertising channels that are enabled for initiator scanning operation. Bit 15: setting 1 - enables channel 39 for use. Bit 14: setting 1 - enables channel 38 for use. Bit 13: setting 1 - enables channel 37 for use. Default Value: 0
7	INITA_TX_AD-DR_NOT_SET_INTR_EN	Enable INITA RPA TX not set interrupt. This bit is valid only if PRIV_1_2 and PRIV_1_2_INIT are set. Default Value: 0
6	INIT_ADV_RX_IN-TR_PEER_RPA_UN-RES_EN	Enable ADV peer address RPA unresolved interrupt. This bit is valid only if PRIV_1_2 and PRIV_1_2_INIT are set. Default Value: 0
5	INIT_ADV_RX_INTR_-SELF_RPA_UNRES_EN	Enable ADV self address RPA unresolved interrupt. This bit is valid only if PRIV_1_2 and PRIV_1_2_INIT are set. Default Value: 0

22.1.108 BLE_BLELL_INIT_CONFIG (continued)

4	CONN_CREATED	Enable master connection created interrupt Default Value: 0
2	CONN_REQ_TX_EN	Enables connection request packet transmission start interrupt. Default Value: 0
1	INIT_CLOSE_EN	Enable Initiator event close interrupt. Default Value: 0
0	INIT_STRT_EN	Enable Initiator event start interrupt. Default Value: 0

22.1.109 BLE_BLELL_CONN_CONFIG

Connection configuration register

Address: 0x403C11E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	RX_INTR_THRESHOLD [7:4]				RX_PKT_LIMIT [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	None		RW
HW Access	R	R	R	R	R	None		R
Name	CON-N_REQ_1SLOT_EAR-LY	MASK_SU-TO_AT_UP-DT	EX-TEND_CU_TX_WIN	SLV_MD_-CONFIG	DS-M_SLOT_-VARIANCE	None [10:9]		MD_BIT_-CLEAR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15	CON-N_REQ_1SLOT_EARLY	This bit is used to enable extension of the Conn Request to arbiter to 1 slot early. When enabled the request length is 2 slots. 1 - Enable 0 - Disable Default Value: 1
14	MASK_SUTO_AT_UPDT	This bit is used to enable/disable masking of internal hardware supervision timeout trigger when switching from old connection parameters to new parameters. 1 - Enable 0 - Disable Default Value: 1
13	EXTEND_CU_TX_WIN	This bit is used to enable/disable extending the additional rx window on slave side during connection update in event of packet miss at the update instant. 1 - Enable 0 - Disable Default Value: 1

22.1.109 BLE_BLELL_CONN_CONFIG (continued)

12	SLV_MD_CONFIG	This bit is set to configure the MD bit control when IUT is in slave role. 1 - MD bit will be decided on packet pending status 0 - MD bit will be decided on packet queued in next buffer status This bit has effect only when CONN_CONFIG.md_bit_ctr bit is not set . Default Value: 0
11	DSM_SLOT_VARIANCE	This bit configures the DSM slot counting mode. 0 - The DSM slot count variance with respect to actual time is less than 1 slot 1 - The DSM slot count variance with respect to actual time is more than 1 slot that 2 slots Default Value: 0
8	MD_BIT_CLEAR	This register field indicates whether the MD (More Data) bit needs to be controlled by software or, hardware and soft-ware logic combined. 1 - MD bit is exclusively controlled by software, ie based on status of CE_CNFG_STS_REGIS-TER[6] - md bit. 0 - MD Bit in the transmitted pdu is controlled by software and hardware logic. MD bit is set in transmitted packet, only if the software has set the md bit in CE_CNFG_STS_REGISTER[6] and either of the following conditions is true, a) If there are packets queued for transmission. b) If there is an acknowledgement awaited from the remote side for the packet transmitted. Default Value: 1
7 : 4	RX_INTR_THRESHOLD	This register field allows setting a threshold for the packet received interrupt to the firmware. For example if the value programmed is 0x2 then HW will generate interrupt only on receiving the second packet. In any case if the received number of packets in a conn event is less than the threshold or there are still packets (less than threshold) pending in the Rx FIFO, HW will generate the interrupt at the ce_close. Min value possible is 1. Max value depends on the Rx FIFO capacity. Default Value: 1
3 : 0	RX_PKT_LIMIT	Defines a limit for the number of Rx packets that can be re-ceived by the LLH. Default maximum value is 0xF.Minimum value shall be 1 or no packet will be stored in the Rx FIFO. Default Value: 15

22.1.110 BLE_BLELL_CONN_PARAM1

Connection parameter 1

Address: 0x403C11E8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW		
HW Access	RW					RW		
Name	HOP_INCREMENT_PARAM [7:3]					SCA_PARAM [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CRC_INIT_L [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 8	CRC_INIT_L	This field defines the lower byte (7:0) of the CRC initialization vector. Default Value: 0
7 : 3	HOP_INCRE- MENT_PARAM	Hop increment for connection channel. Default Value: 0
2 : 0	SCA_PARAM	Sleep Clock Accuracy Default Value: 0

22.1.111 BLE_BLELL_CONN_PARAM2

Connection parameter 2

Address: 0x403C11EC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CRC_INIT_H [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CRC_INIT_H [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CRC_INIT_H	This field defines the upper two bytes (23:8) of the CRC initialization vector. Default Value: 0

22.1.112 BLE_BLELL_CONN_INTR_MASK

Connection Interrupt mask

Address: 0x403C11F0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	CONN_UP-DATE_IN-TR_EN	CE_RX-_INT_EN	CE_TX-_ACK_INT_EN	CLOSE_CE_INT_EN	START_CE_INT_EN	MAP_UP-DT_INT_EN	CON-N_EST-B_INT_EN	CONN_-CL_INT_EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	None			RW	RW
HW Access	R	R	R	None			R	R
Name	PING_NEARLY_EX-PIRD_INTR	PING_TIM-ER_EX-PIRD_INTR	CE_-CLOSE_NULL_RX-_INT_EN	None [12:10]			RX-_BAD_P-DU_INT_EN	RX_-GOOD_P-DU_INT_EN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15	PING_NEARLY_EX-PIRD_INTR	If this bit is set ping timer nearly expired interrupt is enabled Default Value: 0
14	PING_TIMER_EX-PIRD_INTR	If this bit is set ping timer expired interrupt is enabled. Default Value: 0
13	CE_CLOSE_NULL_RX-_INT_EN	If this but us set, the RX interrupt is triggerred for an end of connection event with a null packet Default Value: 1
9	RX_BAD_PDU_INT_EN	If this bit is set packet receive bad pdu interrupt is enabled. Effective only when bit 6 is set. Default Value: 0
8	RX_GOOD_PDU_INT_EN	If this bit is set packet receive good pdu interrupt is enabled. Effective only when bit 6 is set. Default Value: 0
7	CONN_UPDATE_IN-TR_EN	If this bit is set connection update interrupt is enabled. Default Value: 0

22.1.112 BLE_BLELL_CONN_INTR_MASK (continued)

6	CE_RX_INT_EN	If this bit is set interrupt is enabled for reception of packet in a connection event. Default Value: 0
5	CE_TX_ACK_INT_EN	If this bit is set transmission acknowledgement interrupt is enabled: This interrupt is generated to indicate to the firmware that a non-empty packet transmitted is successfully acknowledged by the remote device. For negative acknowledgements from remote device, this interrupt indication is not generated. Default Value: 0
4	CLOSE_CE_INT_EN	If this bit is set connection event closed interrupt is enabled. Default Value: 0
3	START_CE_INT_EN	If this bit is set connection event start interrupt is enabled Default Value: 0
2	MAP_UPDT_INT_EN	If this bit is set, channel map update interrupt is enabled. Default Value: 0
1	CONN_ESTB_INT_EN	If this bit is set connection establishment interrupt is enabled. Default Value: 0
0	CONN_CL_INT_EN	If this bit is set connection closed interrupt is enabled. Default Value: 0

22.1.113 BLE_BLELL_SLAVE_TIMING_CONTROL

slave timing control

Address: 0x403C11F4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SLAVE_TIME_SET_VAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	SLAVE_TIME_ADJ_VAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 8	SLAVE_TIME_ADJ_VAL	Timing adjust value. The internal micro second counter is adjusted to this value whenever slave receives a good access address match at connection anchor point. This will ensure the slave gets synchronized to master timing. Default Value: 190
7 : 0	SLAVE_TIME_SET_VAL	Programmable adjust value to the clock counter when slave is connected Default Value: 150

22.1.114 BLE_BLELL_RECEIVE_TRIG_CTRL

Receive trigger control

Address: 0x403C11F8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		ACC_TRIGGER_THRESHOLD [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	ACC_TRIGGER_TIMEOUT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 8	ACC_TRIGGER_TIME-OUT	If access address match does not occur then within this time from the start of receive operation, the receive operation times out and stops. An internal counter value of 1usec resolution is con-tinuously compared with the value programmed. Max value :0xFF Default Value: 0
5 : 0	ACC_TRIGGER_-THRESHOLD	Access address match threshold value. Number of bits of ac-cess address that should match with the expected access ad-dress to trigger an access code match. Max value : 32 (for 32-bit access address) Lower values may be programmed for bad radios or channels but care must be taken to ensure there are no false matches due to reduced number of bits required to match. Default Value: 0

22.1.115 BLE_BLELL_LL_DBG_1

LL debug register 1

Address: 0x403C1200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	CONN_RX_WR_PTR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						R	
HW Access	None						W	
Name	None [15:10]						CONN_RX_WR_PTR [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 0	CONN_RX_WR_PTR	Connection receive FIFO write pointer Default Value: 0

22.1.116 BLE_BLELL_LL_DBG_2

LL debug register 2

Address: 0x403C1204

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	CONN_RX_RD_PTR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						R	
HW Access	None						W	
Name	None [15:10]						CONN_RX_RD_PTR [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 0	CONN_RX_RD_PTR	Connection receive FIFO read pointer Default Value: 0

22.1.117 BLE_BLELL_LL_DBG_3

LL debug register 3

Address: 0x403C1208

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	CONN_RX_WR_PTR_STORE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						R	
HW Access	None						W	
Name	None [15:10]						CONN_RX_WR_PTR_-STORE [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 0	CONN_RX_WR_PTR_-STORE	Connection receive FIFO stored write pointer for pointer restore Default Value: 0

22.1.118 BLE_BLELL_LL_DBG_4

LL debug register 4

Address: 0x403C120C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		R		R			
HW Access	W		W		W			
Name	ADVER-TISER_FSM_STATE [7:6]		SLAVE_LATEN-CY_FSM_STATE [5:4]		CONNECTION_FSM_STATE [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None					R		
HW Access	None					W		
Name	None [15:11]					ADVERTISER_FSM_STATE [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10 : 6	ADVER-TISER_FSM_STATE	Advertiser FSM state Default Value: 0
5 : 4	SLAVE_LATEN-CY_FSM_STATE	Slave Latency FSM state Default Value: 0
3 : 0	CONNEC-TION_FSM_STATE	Connection FSM state Default Value: 0

22.1.119 BLE_BLELL_LL_DBG_5

LL debug register 5

Address: 0x403C1210

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R			R				
HW Access	W			W				
Name	SCAN_FSM_STATE [7:5]			INIT_FSM_STATE [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None						R	
HW Access	None						W	
Name	None [15:10]						SCAN_FSM_STATE [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 5	SCAN_FSM_STATE	Scanner FSM state Default Value: 0
4 : 0	INIT_FSM_STATE	Initiator FSM state Default Value: 0

22.1.120 BLE_BLELL_LL_DBG_6

LL debug register 6

Address: 0x403C1214

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	W				W			
Name	SCAN_RSP_TX_WR_PTR [7:4]				ADV_TX_WR_PTR [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None		R					
HW Access	None		W					
Name	None [15:14]		ADV_TX_RD_PTR [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
13 : 8	ADV_TX_RD_PTR	Advertiser/ Scan Response FIFO read pointer Default Value: 0
7 : 4	SCAN_RSP_TX-_WR_PTR	Scan Response Transmit FIFO write pointer Default Value: 0
3 : 0	ADV_TX_WR_PTR	Advertiser Transmit FIFO write pointer Default Value: 0

22.1.121 BLE_BLELL_LL_DBG_7

LL debug register 7

Address: 0x403C1218

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R						
HW Access	W	W						
Name	ADV_RX-_RD_PTR	ADV_RX_WR_PTR [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None		R					
HW Access	None		W					
Name	None [15:14]		ADV_RX_RD_PTR [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
13 : 7	ADV_RX_RD_PTR	Advertiser Receive FIFO read pointer Default Value: 0
6 : 0	ADV_RX_WR_PTR	Advertiser Receive FIFO write pointer Default Value: 0

22.1.122 BLE_BLELL_LL_DBG_8

LL debug register 8

Address: 0x403C121C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R						
HW Access	W	W						
Name	WLF_PTR	ADV_RX_WR_PTR_STORE [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None		R					
HW Access	None		W					
Name	None [15:14]		WLF_PTR [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
13 : 7	WLF_PTR	Whitelist FIFO pointer Default Value: 0
6 : 0	ADV_RX_WR_PTR_- STORE	Advertiser Receive FIFO stored write pointer for pointer restore Default Value: 0

22.1.123 BLE_BLELL_LL_DBG_9

LL debug register 9

Address: 0x403C1220

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	WINDOW_WIDEN [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	WINDOW_WIDEN [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	WINDOW_WIDEN	Window Widening value in us. The reset value of this register is 0x0000. After reset de-assertion, at the first clock cycle, the value 0x0010 is assigned to the register. Default Value: 16

22.1.124 BLE_BLELL_LL_DBG_10

LL debug register 10

Address: 0x403C1224

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R					
HW Access	None		W					
Name	None [7:6]		RF_CHANNEL_NUM [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	RF_CHANNEL_NUM	Active channel number Default Value: 0

22.1.125 BLE_BLELL_PEER_ADDR_INIT_L

Lower 16 bit address of the peer device for INIT.

Address: 0x403C1230

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	PEER_ADDR_L [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PEER_ADDR_L [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	PEER_ADDR_L	Lower 16 bit of 48-bit address of the peer device. This is used only in MMMS mode The peer address registers are used for multiple purposes. The register is written by firmware to provide the peer address to be used for a hardware procedure. When firmware reads the register, it reads back peer address values updated by hardware. While device is configured as an initiator without white list filtering, the peer address specified in the peer_address field of the create connection command is programmed into this register, which is used by hard-ware procedures. While device is configured as an initiator and white list is enabled, firmware can read this register to get the address of the peer device from which connectable ADV packet was received and to which the connection is created. Default Value: 0

22.1.126 BLE_BLELL_PEER_ADDR_INIT_M

Middle 16 bit address of the peer device for INIT.

Address: 0x403C1234

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	PEER_ADDR_M [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PEER_ADDR_M [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	PEER_ADDR_M	Middle 16 bit of 48-bit address of the peer device. This is used only in MMMS mode The peer address registers are used for multiple purposes. The register is written by firmware to provide the peer address to be used for a hardware procedure. When firmware reads the register, it reads back peer address values updated by hardware. While device is configured as an initiator without white list filtering, the peer address specified in the peer_address field of the create connection command is programmed into this register, which is used by hard-ware procedures. While device is configured as an initiator and white list is enabled, firmware can read this register to get the address of the peer device from which connectable ADV packet was received and to which the connection is created. Default Value: 0

22.1.127 BLE_BLELL_PEER_ADDR_INIT_H

Higher 16 bit address of the peer device for INIT.

Address: 0x403C1238

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	PEER_ADDR_H [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PEER_ADDR_H [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	PEER_ADDR_H	Higher 16 bit of 48-bit address of the peer device. This is used only in MMMS mode The peer address registers are used for multiple purposes. The register is written by firmware to provide the peer address to be used for a hardware procedure. When firmware reads the register, it reads back peer address values updated by hardware. While device is configured as an initiator without white list filtering, the peer address specified in the peer_address field of the create connection command is programmed into this register, which is used by hard-ware procedures. While device is configured as an initiator and white list is enabled, firmware can read this register to get the address of the peer device from which connectable ADV packet was received and to which the connection is created. Default Value: 0

22.1.128 BLE_BLELL_PEER_SEC_ADDR_ADV_L

Lower 16 bits of the secondary address of the peer device for ADV_DIR.

Address: 0x403C123C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	PEER_SEC_ADDR_L [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PEER_SEC_ADDR_L [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	PEER_SEC_ADDR_L	Lower 16 bit of 48-bit secondary address of the peer device for ADV_DIR. Default Value: 0

22.1.129 BLE_BLELL_PEER_SEC_ADDR_ADV_M

Middle 16 bits of the secondary address of the peer device for ADV_DIR.

Address: 0x403C1240

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	PEER_SEC_ADDR_M [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PEER_SEC_ADDR_M [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	PEER_SEC_ADDR_M	Middle 16 bit of 48-bit secondary address of the peer device for ADV_DIR. Default Value: 0

22.1.130 BLE_BLELL_PEER_SEC_ADDR_ADV_H

Higher 16 bits of the secondary address of the peer device for ADV_DIR.

Address: 0x403C1244

Retention: Retained

Bits	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SW Access	RW							
HW Access	RW							
Name	PEER_SEC_ADDR_H [7:0]							

Bits	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SW Access	RW							
HW Access	RW							
Name	PEER_SEC_ADDR_H [15:8]							

Bits	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	**Name**	**Description**
15 : 0	PEER_SEC_ADDR_H	Higher 16 bit of 48-bit secondary address of the peer device for ADV_DIR. While doing directed Advertising in device privacy mode, if the peer device has shared its IRK, then the peer device RPA is written into the PEER_ADDR registers and the peer device identity address is written into this register. If the peer device has not shared its IRK, then the peer identity address is written into the PEER_ADDR registers and this register must be cleared. Default Value: 0

22.1.131 BLE_BLELL_INIT_WINDOW_TIMER_CTRL

Initiator Window NI timer control

Address: 0x403C1248

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							INIT_WINDOW_OFFSET_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	INIT_WINDOW_OFFSET_SEL	Controls the INIT Window offset source 1 - Pick INIT Window Offset from HW calculated INIT_WINDOW_OFFSET 0 - Pick INIT Window Offset from FW loaded register Default Value: 0

22.1.132 BLE_BLELL_CONN_CONFIG_EXT

Connection extended configuration register

Address: 0x403C124C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW					RW	RW
HW Access	None	R					R	R
Name	None	FW_PKT_RCV_CONN_INDEX [6:2]					CON-N_REQ_3SLOT_EAR-LY	CON-N_REQ_2SLOT_EAR-LY

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW					
HW Access	R	R	R					
Name	MT_P-DU_CE_-EXPIRE	DE-BUG_CE_-EXPIRE	MMMS_RX_PKT_LIMIT [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15	MT_PDU_CE_EXPIRE	MMMS empty PDU CE expire handling control bit Default Value: 1
14	DEBUG_CE_EXPIRE	MMMS CE expire control bit Default Value: 0
13 : 8	MMMS_RX_PKT_LIMIT	Receive Packet Limit for MMMS mode. This is the RX_FIFO Limit and applies to all connections together Default Value: 32
6 : 2	FW_PKT_RCV_CON-N_INDEX	Connection Index for which the FW generates Packet Received Command. In MMMS mode, FW should write this field before giving PKT_RECEIVE_COMMAND to HW. Default Value: 0

22.1.132 BLE_BLELL_CONN_CONFIG_EXT (continued)

1	CON-N_REQ_3SLOT_EARLY	This bit is used to enable extension of the Conn Request to arbiter to 3 slot early. When enabled the request length is 4 slots, irrespective of the status of CONN_REQ_1SLOT_EARLY & CON-N_REQ_2SLOT_EARLY bits. 1 - Enable 0 - Disable Default Value: 0
0	CON-N_REQ_2SLOT_EARLY	This bit is used to enable extension of the Conn Request to arbiter to 2 slot early. When enabled the request length is 3 slots, irrespective of the status of CONN_REQ_1SLOT_EARLY bit. 1 - Enable 0 - Disable Default Value: 0

22.1.133 BLE_BLELL_DPLL_CONFIG

DPLL & CY Correlator configuration register

Address: 0x403C1258

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DPLL_CORREL_CONFIG [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DPLL_CORREL_CONFIG [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DPLL_CORREL_CONFIG	If MXD_IF_OPTION is 0: Not used If CY_CORREL_EN is 1: [11:0] CY correl Access address compare mask for LSB 12 bits. Ideal value is 0xFFF [15:12] CY correl maximum number of allowed mismatched bits in access address. Ideal value is 0x0. Default Value: 0

22.1.134 BLE_BLELL_INIT_NI_VAL

Initiator Window NI instant

Address: 0x403C1260

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	INIT_NI_VAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	INIT_NI_VAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	INIT_NI_VAL	Initiator window Next Instant value used for spacing Master connections in time, to minimize connection contention. This value is in 625us slots. The read value corresponds to the hardware updated Interval value Default Value: 0

22.1.135 BLE_BLELL_INIT_WINDOW_OFFSET

Initiator Window offset captured at conn request

Address: 0x403C1264

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	INIT_WINDOW_NI [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	INIT_WINDOW_NI [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	INIT_WINDOW_NI	Initiator Window offset captured at conn request. This value is in 1.25ms slots Default Value: 0

22.1.136 BLE_BLELL_INIT_WINDOW_NI_ANCHOR_PT

Initiator Window NI anchor point captured at conn request

Address: 0x403C1268

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	INIT_INT_OFF_CAPT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	INIT_INT_OFF_CAPT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	INIT_INT_OFF_CAPT	Initiator interval offset captured at conn request. The value indicates the master connection anchor point. This value is in 625us slots Default Value: 0

22.1.137 BLE_BLELL_CONN_UPDATE_NEW_INTERVAL

Connection update new interval

Address: 0x403C13A4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CONN_UPDT_INTERVAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CONN_UPDT_INTERVAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CONN_UPDT_INTERVAL	This register will have the new connection interval that the hardware will use after the connection update instant. Before the instant, the connection interval in the register CONN_INTERVAL will be used by hardware. Default Value: 0

22.1.138 BLE_BLELL_CONN_UPDATE_NEW_LATENCY

Connection update new latency

Address: 0x403C13A8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CONN_UPDT_SLV_LATENCY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CONN_UPDT_SLV_LATENCY [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CONN_UPDT_SLV_LATENCY	This register will have the new slave latency parameter that the hardware will use after the connection update instant. Before the instant, the connection interval in the register SLAVE_LATENCY will be used by hardware. Default Value: 0

22.1.139 BLE_BLELL_CONN_UPDATE_NEW_SUP_TO

Connection update new supervision timeout

Address: 0x403C13AC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CONN_UPDT_SUP_TO [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CONN_UPDT_SUP_TO [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CONN_UPDT_SUP_TO	This register will have the new supervision timeout that the hardware will use after the connection update instant. Before the instant, the connection interval in the register SUP_TIMEOUT will be used by hardware. Default Value: 0

22.1.140 BLE_BLELL_CONN_UPDATE_NEW_SL_INTERVAL

Connection update new Slave Latency X Conn interval Value

Address: 0x403C13B0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SL_CONN_INTERVAL_VAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	SL_CONN_INTERVAL_VAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	SL_CONN_INTER-VAL_VAL	This register will have the new Slave Latency * Conn Interval value that the hardware will use after the connection update instant. Before the instant, the connection interval in the register SL_CONN_INTERVAL will be used by hardware. Default Value: 0

22.1.141 BLE_BLELL_CONN_REQ_WORD0

Connection request address word 0

Address: 0x403C13C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ACCESS_ADDR_LOWER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ACCESS_ADDR_LOWER [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	ACCESS_ADDR_LOWER	This field defines the lower 16 bits of the access address that is to be sent in the connect request packet of the initiator. Default Value: 0

22.1.142 BLE_BLELL_CONN_REQ_WORD1

Connection request address word 1

Address: 0x403C13C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ACCESS_ADDR_UPPER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ACCESS_ADDR_UPPER [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	ACCESS_ADDR_UPPER	This field defines the upper16 bits of the access address that is to be sent in the connect request packet of the initiator. Default Value: 0

22.1.143 BLE_BLELL_CONN_REQ_WORD2

Connection request address word 2

Address: 0x403C13C8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	TX_WINDOW_SIZE_VAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CRC_INIT_LOWER [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 8	CRC_INIT_LOWER	This field defines the lower byte [7:0] of the CRC initialization value. Default Value: 0
7 : 0	TX_WINDOW_SIZE_VAL	window_size along with the window_offset is used to calculate the first connection point anchor point for the master. This shall be a multiple of 1.25 ms in the range of 1.25 ms to the lesser of 10 ms and (connInter-val 1.25 ms). Values range from 0 to 10 ms. Default Value: 0

22.1.144 BLE_BLELL_CONN_REQ_WORD3

Connection request address word 3

Address: 0x403C13CC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CRC_INIT_UPPER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CRC_INIT_UPPER [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CRC_INIT_UPPER	This field defines the upper byte [23:8] of the CRC initialization value that is to be sent in the connect request packet of the initiator. Default Value: 0

22.1.145 BLE_BLELL_CONN_REQ_WORD4

Connection request address word 4

Address: 0x403C13D0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	TX_WINDOW_OFFSET [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	TX_WINDOW_OFFSET [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	TX_WINDOW_OFFSET	This is used to determine the anchor point for the master transmission. Range: This shall be a multiple of 1.25 ms in the range of 0 ms to connInterval value. Default Value: 0

22.1.146 BLE_BLELL_CONN_REQ_WORD5

Connection request address word 5

Address: 0x403C13D4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CONNECTION_INTERVAL_VAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CONNECTION_INTERVAL_VAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CONNECTION_INTER-VAL_VAL	The value configured in this register determines the spacing between the connection events. This shall be a multiple of 1.25 ms in the range of 7.5 ms to 4.0 s. Default Value: 0

22.1.147 BLE_BLELL_CONN_REQ_WORD6

Connection request address word 6

Address: 0x403C13D8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	SLAVE_LATENCY_VAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	SLAVE_LATENCY_VAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	SLAVE_LATENCY_VAL	The value configured in this field defines the number of consecutive connection events that the slave device is not required to listen for master. The value of connSlaveLatency should not cause a Supervision Timeout. This shall be an integer in the range of 0 to ((connSupervision Timeout/ connInterval)-1). connSlaveLatency shall also be less than 500. Default Value: 0

22.1.148 BLE_BLELL_CONN_REQ_WORD7

Connection request address word 7

Address: 0x403C13DC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	SUPERVISION_TIMEOUT_VAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	SUPERVISION_TIMEOUT_VAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	SUPERVISION_TIME-OUT_VAL	This field defines the maximum time between two received Data packet PDUs before the connection is considered lost. This shall be a multiple of 10 ms in the range of 100 ms to 32.0 s and it shall be larger than (1+connSlaveLatency)*connInterval. Default Value: 0

22.1.149 BLE_BLELL_CONN_REQ_WORD8

Connection request address word 8

Address: 0x403C13E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA_CHANNELS_LOWER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA_CHANNELS_LOWER [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATA_CHANNELS_LOWER	This register field indicates which of the data channels are in use. This stores the information for the lower 16 (15:0) data channel indices. 1 indicates the corresponding data channel is used and 0 indicates the channel is unused. Default Value: 0

22.1.150 BLE_BLELL_CONN_REQ_WORD9

Connection request address word 9

Address: 0x403C13E4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA_CHANNELS_MID [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA_CHANNELS_MID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATA_CHANNELS_MID	This register field indicates which of the data channels are in use. This stores the information for the middle 16 (31:16) data channel indices. 1 indicates the corresponding data channel is used and 0 indicates the channel is unused. Default Value: 0

22.1.151 BLE_BLELL_CONN_REQ_WORD10

Connection request address word 10

Address: 0x403C13E8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			RW				
Name	None [7:5]			DATA_CHANNELS_UPPER [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4 : 0	DATA_CHANNELS_UP-PER	This register field indicates which of the data channels are in use. This stores the information for the upper 5 (36:32) data channel indices. 1 indicates the corresponding data channel is used and 0 indicates the channel is unused. Default Value: 0

22.1.152 BLE_BLELL_CONN_REQ_WORD11

Connection request address word 11

Address: 0x403C13EC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW			RW				
HW Access	RW			RW				
Name	SCA_2 [7:5]			HOP_INCREMENT_2 [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 5	SCA_2	This field defines the sleep clock accuracies given in ppm. Default Value: 0
4 : 0	HOP_INCREMENT_2	This field is used for the data channel selection process. Default Value: 0

22.1.153 BLE_BLELL_PDU_RESP_TIMER

PDU response timer/Generic Timer (MMMS mode)

Address: 0x403C1A04

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	PDU_RESP_TIME_VAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	PDU_RESP_TIME_VAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	PDU_RESP_TIME_VAL	Non MMMS mode: This register is loaded with the count value to monitor the time to get a response for a PDU from peer device. Firmware starts the timer by issuing the command, RESP_TIMER_ON, after it has queued a PDU for transmission, that requires a response. If a response is received, firmware stops and clears the timer by issuing the command RESP_TIMER_OFF. If this timer expires, it results in hardware closing the connection and triggering a conn_closed interrupt. The discon_status field in the Connection status register is set with the appropriate reason. Units : Milliseconds. Resolution : 1.25 ms MMMS mode: This register is loaded with a count value, which when matched by the internal timer, triggers the GEN_TIMER_INTR. This is recommended to be used as a one shot timer and not as a periodic timer. Firmware starts the timer by loading the expiry time and issuing the command, RESP_TIMER_ON. Once the timer expiry is triggered with the interrupt GEN_TIMER_INTR, the firmware stops the timer by issuing the command RESP_TIMER_OFF. Resolution : 625 us Default Value: 0

22.1.154 BLE_BLELL_NEXT_RESP_TIMER_EXP

Next response timeout instant

Address: 0x403C1A08

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	NEXT_RESPONSE_INSTANT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	NEXT_RESPONSE_INSTANT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	NEXT_RESPONSE_IN-STANT	This field defines the clock instant at which the next PDU response timeout event will occur on a connection. This is with reference to the 16-bit internal reference clock. Default Value: 0

22.1.155 BLE_BLELL_NEXT_SUP_TO

Next supervision timeout instant

Address: 0x403C1A0C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	NEXT_TIMEOUT_INSTANT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	NEXT_TIMEOUT_INSTANT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	NEXT_TIMEOUT_IN-STANT	This field defines the clock instant at which the next connection supervision timeout event will occur on a connection This is with reference to the 16-bit internal reference clock. Default Value: 0

22.1.156 BLE_BLELL_LLH_FEATURE_CONFIG

Feature enable

Address: 0x403C1A10

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [7:3]					US_COUNTER_OFF-SET_ADJ	SL_DS-M_EN	QUICK_TRANSMIT

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	US_COUNTER_OFF-SET_ADJ	Enable/Disable the connection US counter offset adjust. For non-MMMS mode, this bit must be tied to 1. Default Value: 1
1	SL_DSM_EN	Enable/Disable Slave Latency Period DSM. Default Value: 1
0	QUICK_TRANSMIT	Quick transmit feature in slave latency is enabled by setting this bit. When slave latency is enabled, this feature enables the slave to transmit in the immediate connection interval, in case required, instead of waiting till the end of slave latency Default Value: 0

22.1.157 BLE_BLELL_WIN_MIN_STEP_SIZE

Window minimum step size

Address: 0x403C1A14

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	STEPUP [7:4]				STEPDN [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	WINDOW_MIN_FW [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 8	WINDOW_MIN_FW	Minimum window interval value programmed by firmware. While the slave receive window is decremented, the windows_min_fw sets the lowest value of the window widen value to ensure packets are not missed. The unit is in microseconds. Default Value: 32
7 : 4	STEPUP	If packets are missed, the reference window is gradually increased by step up size, until it receives 2 consecutive good packets. The unit is in microseconds Default Value: 6
3 : 0	STEPDN	After receiving 2 consecutive good packets the reference window is gradually decremented by step down size until it reaches window minimum. The unit is in microseconds Default Value: 4

22.1.158 BLE_BLELL_SLV_WIN_ADJ

Slave window adjustment

Address: 0x403C1A18

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SLV_WIN_ADJ [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW		
HW Access	None					R		
Name	None [15:11]					SLV_WIN_ADJ [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10 : 0	SLV_WIN_ADJ	Window Adjust value. This value is added to the calculated slave window widening value to be used as final window widen value. Default Value: 16

22.1.159 BLE_BLELL_SL_CONN_INTERVAL

Slave Latency X Conn Interval Value

Address: 0x403C1A1C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	SL_CONN_INTERVAL_VAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	SL_CONN_INTERVAL_VAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	SL_CONN_INTER-VAL_VAL	This field defines the (SL*CI) product for the ongoing connection. This value is used in calculation of next connection instant during slave latency. Default Value: 0

22.1.160 BLE_BLELL_LE_PING_TIMER_ADDR

LE Ping connection timer address

Address: 0x403C1A20

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CONN_PING_TIMER_ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CONN_PING_TIMER_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CONN_PING_TIMER_AD-DR	The register used to configure the LE Au-thenticated payload Timeout (LE APTO) which is the Maximum amount of time specified between packets authenticated by a MIC. This value of ping timer is in the order of 10ms, valid range 0x1 ~ 0xFFFF Default Value: 0

22.1.161 BLE_BLELL_LE_PING_TIMER_OFFSET

LE Ping connection timer offset

Address: 0x403C1A24

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CONN_PING_TIMER_OFFSET [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CONN_PING_TIMER_OFFSET [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CONN_PING_TIM-ER_OFFSET	The value of ping timer nearly expired offset in the order of 10ms, valid range 0x0 ~ 0xFFFF. This is the time period after which the ping timer nearly expired interrupt is generated. Default Value: 0

22.1.162 BLE_BLELL_LE_PING_TIMER_NEXT_EXP

LE Ping timer next expiry instant

Address: 0x403C1A28

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	CONN_PING_TIMER_NEXT_EXP [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	CONN_PING_TIMER_NEXT_EXP [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CONN_PING_TIM-ER_NEXT_EXP	The value of ping timer next expiry instant in the terms of native clock value (least 16 bit value of the 17 bit ping counter). This together with CONN_PING_TIMER_NEXT_EXP_WRAP will provide the correct status of ping timer duration. Default Value: 0

22.1.163 BLE_BLELL_LE_PING_TIMER_WRAP_COUNT

LE Ping Timer wrap count

Address: 0x403C1A2C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	CONN_SEC_CURRENT_WRAP [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	CONN_SEC_CURRENT_WRAP [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CONN_SEC_CUR-RENT_WRAP	This register holds the current position of the Ping timer. Default Value: 0

22.1.164 BLE_BLELL_TX_EN_EXT_DELAY

Transmit enable extension delay

Address: 0x403C1E00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	RXEN_EXT_DELAY [7:4]				TXEN_EXT_DELAY [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	MOD_2M_COMP_DLY [15:12]				DEMOD_2M_COMP_DLY [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 12	MOD_2M_COMP_DLY	2Mbps modulation delay delta compare to 1Mbps demod delay. This data is 2's comp data. Default Value: 1
11 : 8	DEMOD_2M_COMP_DLY	2Mbps demod delay delta compare to 1Mbps demod delay. This data is 2's comp data. Default Value: 3
7 : 4	RXEN_EXT_DELAY	receiver enable extension delay. This is to extend the active state (high) of dbus_rx_en signal after the last bit is received from demod. The unit is in microsecond and the supported range is 00 31 us. Default Value: 4
3 : 0	TXEN_EXT_DELAY	Transmit enable extension delay. This is to extend the active state (high) of rif_tx_en signal after the last bit is sent out from LLH. The unit is in microsecond and the supported range is 00 31 us. Default Value: 5

22.1.165 BLE_BLELL_TX_RX_SYNTH_DELAY

Transmit/Receive enable delay

Address: 0x403C1E04

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	RX_EN_DELAY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	TX_EN_DELAY [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 8	TX_EN_DELAY	The delay used to assert rif_tx_en exactly Tx_tRamp micro-seconds ahead of the first bit of the tx_data, which can be used to turn on the Radio transmitter. The value to be programmed to the Tx_en_delay [7:0] = tx_on_delay - Tx_tRamp tx_on_delay[7:0] = TX_RX_ON_DELAY[15:8]) Tx_tRamp = Radio transmitter ramp_up Default Value: 0
7 : 0	RX_EN_DELAY	The delay used to assert rif_rx_en, Rx_tRamp micro-seconds, ahead of first bit of the expected rx_data, which can be used to turn on the Radio receiver. The value to be programmed to the Rx_en_delay [7:0] = rx_on_delay - Rx_tRamp rx_on_delay[7:0] = TX_RX_ON_DELAY[7:0]) Rx_tRamp = Radio receiver rampup time Default Value: 0

22.1.166 BLE_BLELL_EXT_PA_LNA_DLY_CNFG

External TX PA and RX LNA delay configuration

Address: 0x403C1E08

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	LNA_CTL_DELAY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	PA_CTL_DELAY [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 8	PA_CTL_DELAY	The delay used to assert PA_CTL exactly PA_tRamp micro-seconds ahead of the first bit of the tx_data, which can be used to turn on the external power amplifier. The value to be programmed to the pa_ctl_delay [7:0] = tx_on_delay - PA_tRamp tx_on_delay[7:0] = TX_RX_ON_DELAY[15:8]) PA_tRamp = External Power Amplifier ramp time Default Value: 0
7 : 0	LNA_CTL_DELAY	The delay used to assert LNA_CTL, LNA_tRamp micro-seconds, ahead of first bit of the expected rx_data, which can be used to turn on the external Low Noise Amplifier. The value to be programmed to the lna_ctl_delay [7:0] = rx_on_delay - LNA_tRamp rx_on_delay[7:0] = TX_RX_ON_DELAY[7:0]) LNA_tRamp = External Low Noise Amplifier startup time Default Value: 0

22.1.167 BLE_BLELL_LL_CONFIG

Link Layer additional configuration

Address: 0x403C1E10

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	None	RW	RW	RW	RW
HW Access	R	R	R	None	R	R	R	R
Name	TX_RX-_PIN_DLY	RSSI_EAR-LY_CNFG	RSSI_IN-TR_SEL	None	TIM-ER_LF_SLOT_EN-ABLE	TIFS_EN-ABLE	TX_RX_C-TRL_SEL	RSSI_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW	RW	RW	RW	RW	RW	RW
HW Access	None	R	R	R	R	R	R	R
Name	None	AD-V_DIR_DE-VICE_PRIV_EN	MUL-TI_ENGINE_LPM	CHECK_DUP_CONN	FORCE_TRIG_RC-B_UPDATE	RSSI_EACH_PKT	RSSI_EN-ERGY_RD	TX_PA_P-WR_LVL_-TYPE

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
14	ADV_DIR_DE-VICE_PRIV_EN	Controls the ADV behavior while advertising ADV_DIR and only device privacy is set. When the ADV is transmitting INITA RPA, the bahavior when an Identity address in received from the Initiator in the CONN_REQ is given below 0 - Abort the CONN_REQ and continue with advertisement 1 - Check the address against PEER_SEC_ADDR_ADV and create connection on a match. Default Value: 1
13	MULTI_ENGINE_LPM	Controls the LPM entry condition 0 - Legacy mode LPM entry check 1 - MMMS mode LPM entry check Default Value: 0

22.1.167 BLE_BLELL_LL_CONFIG (continued)

12	CHECK_DUP_CONN	Controls the duplicate connection checkin ADV and INIT 0 - Does not check if the peer is already connection before a new connection is created 1 - Checks if the peer is already connection before a new connection is created and aborts a duplicate connection creation Default Value: 0
11	FORCE_TRIG_RCB_UPDATE	Controls the RCB update to radio on TX/RX enable. Applicable only when TX_RX_CTRL_SEL is 1'b1 0 - RCB update is triggerred only when the fields change on rising edge of TX/RX enable 1 - RCB update is force triggerred on rising edge of TX/RX enable If TX_RX_CTRL_SEL is 1'b1 and ENABLE_RADIO_BOD is 1'b1, this bit needs to be set to 1'b1 Default Value: 1
10	RSSI_EACH_PKT	Controls the RSSI reads. 0 - RSSI read is not initiated for zero length and aborted packets 1 - RSSI read is initiated for zero length and aborted packets Default Value: 1
9	RSSI_ENERGY_RD	Controls the RSSI reads. 0 - Channel Energy read is not initiated if no packet is received during a receive cycle 1 - Channel Energy read is initiated at the end of the receive cycle if no packet is received Default Value: 0
8	TX_PA_PWR_LVL_TYPE	Controls the TX power level format given to the CYBLERD55 chip. 0 - The power level given to CYBLERD55 is in 4 bit code format from ADV_CH_TX_POWER for advertising channel and DTM packets & from CONN_CH_TX_POWER for connection channel packets. The power level setting is decoded and given to the PA. 1 - The power level given to CYBLERD55 is in 18 bit power level setting format from {ADV_CH_TX_POWER_LVL_MS, ADV_CH_TX_POWER_LVL_LS} channel and DTM packets & from {CONN_CH_TX_POWER_LVL_MS, CONN_CH_TX_POWER_LVL_LS} for connection channel packets. This setting is directly given to the PA. Default Value: 0
7	TX_RX_PIN_DLY	Controls the delay from DBUS_TX, DBUS_RX assertion to the assertion on the pins. This is applicable only when TX_RX_CTRL_SEL is set. 0 - The pin assertion is delayed by 4 cycles. 1 - The pin assertion is delayed by 8 cycles. Default Value: 0
6	RSSI_EARLY_CNFG	Controls the early RSSI reads. This is applicable only when RSSI_SEL is 1. 1 - RSSI read is initiated during the first CRC byte reception. 0 - RSSI read is initiated during the third CRC byte reception. Default Value: 0
5	RSSI_INTR_SEL	Controls the engine interrupt generation based on RSSI reads. This is valid only if RSSI_SEL is 0. 0 - Receive interrupts are triggerred after the RSSI read is complete 1 - Receive interrupts are triggerred after the last bit of CRC Default Value: 0
3	TIMER_LF_SLOT_ENABLE	Controls the wakeup timer configuration 1 - Wakeup time is compensated with the LF_OFFSET 0 - Wakeup time is not compensated with the LF_OFFSET as in legacy mode Default Value: 0
2	TIFS_ENABLE	Setting this bit enables the tx 1MHz pulse to match the received bpktctl from CYBLERD55. This will result is reduced TIFS variation Default Value: 0

22.1.167 BLE_BLELL_LL_CONFIG (continued)

1	TX_RX_CTRL_SEL	Controls the mode of issueing TX_EN & RX_EN to the Radio 1 - TX_EN and RX_EN are issued through direct pins 0 - TX_EN and RX_EN are issued through RCB writes Default Value: 0
0	RSSI_SEL	Controls the RSSI reads. When this bit is 1, the bit RSSI_INTR_SEL is don't care. 0 - RSSI read is initiated after the the packet is received 1 - RSSI read is completed before the packet is received. When RCB Interface is operating 4Mhz are lower this bit should be set to 1'b0. Default Value: 0

22.1.168 BLE_BLELL_LL_CONTROL

LL Backward compatibility

Address: 0x403C1F00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	RPT_PEER_ADDR_MATCH_PRIV_MISMATCH_SCN	RPT_SCAN_ADDR_MATCH_PRIV_MISMATCH_ADV	RPT_INIT_ADDR_MATCH_PRIV_MISMATCH_ADV	HW_RSLV_LIST_FULL	ADVCH_FIFO_PRIV_1_2_FLUSH_CTRL	WL_READ_AS_MEM	DLE	PRIV_1_2

Bits	15	14	13	12	11	10	9	8
SW Access	W	RW1C	RW	RW	RW	RW	RW	RW
HW Access	R	RW	R	R	R	R	R	R
Name	ADVCH_FIFO_FLUSH	SLV_CONN_PEER_RPA_NOT_RSLVD	EN_CONN_RX_EN_MOD	PRIV_1_2_INIT	PRIV_1_2_SCAN	PRIV_1_2_ADV	RPT_SELF_ADDR_MATCH_PRIV_MISMATCH_INI	RPT_PEER_ADDR_MATCH_PRIV_MISMATCH_INI

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15	ADVCH_FIFO_FLUSH	When set, flushes the ADVCH FIFO. The bit is auto cleared. Note that this should be used only when the FIFO is not read by the firmware. If firmware has started reading the FIFO, then the FIFO must be emptied exclusively by firmware reads Default Value: 0
14	SLV_CONN_PEER_RPA_NOT_RSLVD	This bit is asserted when SLV_CONN_PEER_RPA_UNMCH_INTR is set. The device does not enter into Connection established state until this bit is cleared after the RPA is resoved by the firmware. If the firmware is not able to resolve the RPA within the supervision timeout, the device aborts the connection establishement and this bit is cleared by the hardware. This bit is valid only if PRIV_1_2 is set. Default Value: 0

22.1.168 BLE_BLELL_LL_CONTROL (continued)

13	EN_CONN_RX_EN_MOD	This bit controls the Connection RX enable modification mode when SLV_CONN_PEER_R-PA_NOT_RSLVD is set. 1'b0 - The Connection RX enable is unmodified 1'b1 - The Connection RX enable is during the Peer INIT RPA unresolved state is modified, until it is resolved. Default Value: 0
12	PRIV_1_2_INIT	Enables Privacy 1.2 for INIT engine Default Value: 0
11	PRIV_1_2_SCAN	Enables Privacy 1.2 for SCAN engine Default Value: 0
10	PRIV_1_2_ADV	Enables Privacy 1.2 for ADV engine Default Value: 0
9	RPT_SELF_ADDR_-MATCH_PRIV_MIS-MATCH_INI	This bit controls the INIT engine behavior when a self address match occurs but a privacy mis-match occurs 0 - The packet is aborted 1 - The packet is received and reported to the Link Layer firmware Default Value: 0
8	RPT_PEER_ADDR_-MATCH_PRIV_MIS-MATCH_INI	This bit controls the INIT engine behavior when an peer address match occurs but a privacy mis-match occurs 0 - The packet is aborted 1 - The packet is received and reported to the Link Layer firmware Default Value: 0
7	RPT_PEER_ADDR_-MATCH_PRIV_MIS-MATCH_SCN	This bit controls the SCAN engine behavior when an peer address match occurs but a privacy mismatch occurs 0 - The packet is aborted 1 - The packet is received and reported to the Link Layer firmware Default Value: 0
6	RPT_SCAN_ADDR_-MATCH_PRIV_MIS-MATCH_ADV	This bit controls the ADV engine behavior when a scanner address match occurs but a privacy mismatch occurs 0 - The packet is aborted 1 - The packet is received and reported to the Link Layer firmware Default Value: 0
5	RPT_INIT_ADDR_-MATCH_PRIV_MIS-MATCH_ADV	This bit controls the ADV engine behavior when an initiator address match occurs but a privacy mismatch occurs 0 - The packet is aborted 1 - The packet is received and reported to the Link Layer firmware Default Value: 0
4	HW_RSLV_LIST_FULL	This bit indicates that the resolving list in the hardware is full and the list is extended in the FW. This will affect the behavior of address resolution. 0 - The resolving list in the hardware is not fully filled. When Whitelist is disabled and a peer identity address not in the resolving list is received, the packet is responded to by the hardware. 1 - The resolving list in the hardware is fully filled. All address comparisons must be extended to the Firmware list as well, Any match in the Firmware list should be followed by copying the matching entry into the hardware resolving list. Default Value: 0
3	ADVCH_FI-FO_PRIV_1_2_-FLUSH_CTRL	Controls the ADVCH FIFO flushing when PRIV_1_2 is enabled. 0 - Flushes all ADV & INIT packets, as in non privacy 1.2 mode, except those with unresolved peer or self RPA. 1 - Does not flush any CRC good packets Default Value: 0

22.1.168 BLE_BLELL_LL_CONTROL (continued)

2	WL_READ_AS_MEM	The Whilelist read logic is controlled using this bit. 0 - The reads to the whitelist address range is treated as FIFO reads and the pointers are reset by issueing the RESET_READ_PTR command. 1 - The reads to the whitelist address range is treated an memory reads. Any whilelist entry can be read. Default Value: 0
1	DLE	Enables Data Length extension feature in DTM, connection and encryption modules. This bit should always be set to 1'b1. 1'b0 is not supported. Default Value: 1
0	PRIV_1_2	Enables Privacy 1.2 Feature. Default Value: 0

22.1.169 BLE_BLELL_DEV_PA_ADDR_L

Device Resolvable/Non-Resolvable Private address lower register

Address: 0x403C1F04

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DEV_PA_ADDR_L [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DEV_PA_ADDR_L [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DEV_PA_ADDR_L	Lower 16 bit of 48-bit Random Private address of the device. Default Value: 13330

22.1.170 BLE_BLELL_DEV_PA_ADDR_M

Device Resolvable/Non-Resolvable Private address middle register

Address: 0x403C1F08

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DEV_PA_ADDR_M [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DEV_PA_ADDR_M [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DEV_PA_ADDR_M	Middle 16 bit of 48-bit Random Private address of the device. Default Value: 86

22.1.171 BLE_BLELL_DEV_PA_ADDR_H

Device Resolvable/Non-Resolvable Private address higher register

Address: 0x403C1F0C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DEV_PA_ADDR_H [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DEV_PA_ADDR_H [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DEV_PA_ADDR_H	Higher 16 bit of 48-bit Random Private address of the device. Default Value: 0

22.1.172 BLE_BLELL_RSLV_LIST_ENABLE0

Resolving list entry control bit

Address: 0x403C1F10

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	SELF_AD-DR_TX_R-PA_VAL	SELF_AD-DR_RX-D_RPA_VAL	PEER_AD-DR_R-PA_VAL	PEER_AD-DR_TYPE	WH-ITELIST-ED_PEER	SELF_AD-DR_IRK_SET_RX	PEER_AD-DR_IRK_SET	VALID_EN-TRY

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [15:11]					ENTRY_-CONNECT-ED	SELF_AD-DR_-TYPE_TX	SELF_AD-DR_INIT_R-PA_SEL

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10	ENTRY_CONNECTED	Indicates if the entry is already in connection with our device Default Value: 0
9	SELF_ADDR_TYPE_TX	Indicates the TX addr type to be used for SCANA and INITA 0 - Self Identity address is used in SCANA/INITA in SCAN_REQ/CONN_REQ packets 1 - Self RPA address provided in RSLV_LIST_TX_INIT_RPA field in the resolving list with the associated valid bit in SELF_ADDR_TX_RPA_VAL above is used in SCANA/INITA in SCAN_REQ/CONN_REQ packets Default Value: 0
8	SELF_ADDR_INIT_RPA_-SEL	When Initiator whitelist is disabled, this bit indicates the specific device to from which ADV pack-ets will be accepted. Default Value: 0
7	SELF_ADDR_TX_R-PA_VAL	Indicates that the self RPA in the list to be transmitted is valid Default Value: 0

22.1.172 BLE_BLELL_RSLV_LIST_ENABLE0 (continued)

6	SELF_ADDR_RXD_R-PA_VAL	Indicates that the received self RPA in the list is valid Default Value: 0
5	PEER_ADDR_RPA_VAL	Indicates that the peer device RPA in the list is valid Default Value: 0
4	PEER_ADDR_TYPE	Indicates the address type of the listed peer device Default Value: 0
3	WHITELISTED_PEER	Indicates if the listed peer device is in the whitelist Default Value: 0
2	SELF_AD-DR_IRK_SET_RX	Indicates if the local IRK has been shared with the listed peer device 0 - Self Identity address in a received packet is accepted. If a valid self RPA is available in the list, then the RPA in a received packet is accepted. 1 - Only the self device RPA, if available in the list, in a received packet is accepted. A Self Identity address in the received packet is reported as a privacy mismatch. Default Value: 0
1	PEER_ADDR_IRK_SET	Indicates if the listed peer device has shared its IRK. 0 - Identity address in a received packet is accepted. If a valid peer device RPA is available in the list, then the RPA in a received packet is accepted. 1 - Only the peer device RPA, if available in the list, in a received packet is accepted. An Identity address in the received packet is reported as a privacy mismatch. Default Value: 0
0	VALID_ENTRY	Indicates if the index is valid Default Value: 0

22.1.173 BLE_BLELL_WL_CONNECTION_STATUS

whitelist valid entry bit

Address: 0x403C1FA0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	WL_ENTRY_CONNECTED [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	WL_ENTRY_CONNECTED [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	WL_ENTRY_CONNECT-ED	Stores the connection status of each of the sixteen device address stored in the whitelist. 1 - White list entry is already in a connection 0 - White list entry is not in a connection Default Value: 0

22.1.174 BLE_BLELL_CONN_RXMEM_BASE_ADDR_DLE

DLE Connection RX memory base address

Address: 0x403C2800

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CONN_RX_MEM_BASE_ADDR_DLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CONN_RX_MEM_BASE_ADDR_DLE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	CONN_RX_MEM_BASE_ADDR_DLE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	CONN_RX_MEM_BASE_ADDR_DLE [31:24]							

Bits	Name	Description
31 : 0	CONN_RX-_MEM_BASE_ADDR_-DLE	Data from Rx memory are read as 32-bit wide data. This memory is valid only if DLE is set. Default Value: 0

22.1.175 BLE_BLELL_CONN_TXMEM_BASE_ADDR_DLE

DLE Connection TX memory base address

Address: 0x403C3800

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CONN_TX_MEM_BASE_ADDR_DLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CONN_TX_MEM_BASE_ADDR_DLE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	CONN_TX_MEM_BASE_ADDR_DLE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	CONN_TX_MEM_BASE_ADDR_DLE [31:24]							

Bits	Name	Description
31 : 0	CONN_TX-_MEM_BASE_ADDR_-DLE	Data to Tx memory are written as 32-bit wide data. This memory is valid only if DLE is set. Default Value: 0

22.1.176 BLE_BLELL_CONN_1_PARAM_MEM_BASE_ADDR

Connection Parameter memory base address for connection 1

Address: 0x403D3800

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CONN_1_PARAM [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CONN_1_PARAM [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description

22.1.176 BLE_BLELL_CONN_1_PARAM_MEM_BASE_ADDR (continued)

15 : 0	CONN_1_PARAM	Data values are written as 16-bit wide data. This memory is valid only if MMMS is enabled. The layout is as follows 00- AA[15:0] 04 - AA[31:16] 08 - CRC_init[15:0] 0C - WINDOW_SIZE[7:0],CRC_init[23:16] 10 - TX_WINDOW_OFFSET 14 - CI[15:0] 18 - SLV_LATENCY[15:0] 1C - SUPERVISORY_TIMEOUT_VAL[15:0] 20 - CHAN_MAP[15:0] 24 - CHAN_MAP[31:16] 28 - SCA[2:0],CHAN_HOP_INCR[4:0],CHAN_MAP[39:32] 2C - Reserved[1:0],RX_DATA_RATE_1M_2M,TX_DATA_RATE_1M_2M,WINDOW_WIDEN_INTERVAL[11:0] 30 - CE_LENGTH[15:0] 34 - NEXT_SUP_TO[15:0] 38 - Reserved[1:0],LAST_UNMAPPED_CHANNEL[5:0],Reserved[3:0],SN,NESN,Reserved[1:0] 3C - ACCU_WINDOW_WIDEN[15:0] 40 - BT_SLOT_CAPTURE[15:0] 44 - Reserved[15:10],US_CAPTURE[9:0] 48 - Next Connection Instant 4C- Reserved[5:0]. US_OFFSET[9:0] Default Value: 0

22.1.177 BLE_BLELL_CONN_2_PARAM_MEM_BASE_ADDR

Connection Parameter memory base address for connection 2

Address: 0x403D3880

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CONN_2_PARAM [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CONN_2_PARAM [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description

22.1.177 BLE_BLELL_CONN_2_PARAM_MEM_BASE_ADDR (continued)

15 : 0	CONN_2_PARAM	Data values are written as 16-bit wide data. This memory is valid only if MMMS is enabled. The layout is as follows 00- AA[15:0] 04 - AA[31:16] 08 - CRC_init[15:0] 0C - WINDOW_SIZE[7:0],CRC_init[23:16] 10 - TX_WINDOW_OFFSET 14 - CI[15:0] 18 - SLV_LATENCY[15:0] 1C - SUPERVISORY_TIMEOUT_VAL[15:0] 20 - CHAN_MAP[15:0] 24 - CHAN_MAP[31:16] 28 - SCA[2:0],CHAN_HOP_INCR[4:0],CHAN_MAP[39:32] 2C - Reserved[1:0],RX_DATA_RATE_1M_2M,TX_DATA_RATE_1M_2M,WINDOW_WIDEN_INTERVAL[11:0] 30 - CE_LENGTH[15:0] 34 - NEXT_SUP_TO[15:0] 38 - Reserved[1:0],LAST_UNMAPPED_CHANNEL[5:0],Reserved[3:0],SN,NESN,Reserved[1:0] 3C - ACCU_WINDOW_WIDEN[15:0] 40 - BT_SLOT_CAPTURE[15:0] 44 - Reserved[15:10],US_CAPTURE[9:0] 48 - Next Connection Instant 4C- Reserved[5:0]. US_OFFSET[9:0] Default Value: 0

22.1.178 BLE_BLELL_CONN_3_PARAM_MEM_BASE_ADDR

Connection Parameter memory base address for connection 3

Address: 0x403D3900

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CONN_3_PARAM [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CONN_3_PARAM [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description

22.1.178 BLE_BLELL_CONN_3_PARAM_MEM_BASE_ADDR (continued)

15 : 0	CONN_3_PARAM	Data values are written as 16-bit wide data. This memory is valid only if MMMS is enabled. The layout is as follows 00- AA[15:0] 04 - AA[31:16] 08 - CRC_init[15:0] 0C - WINDOW_SIZE[7:0],CRC_init[23:16] 10 - TX_WINDOW_OFFSET 14 - CI[15:0] 18 - SLV_LATENCY[15:0] 1C - SUPERVISORY_TIMEOUT_VAL[15:0] 20 - CHAN_MAP[15:0] 24 - CHAN_MAP[31:16] 28 - SCA[2:0],CHAN_HOP_INCR[4:0],CHAN_MAP[39:32] 2C - Reserved[1:0],RX_DATA_RATE_1M_2M,TX_DATA_RATE_1M_2M,WINDOW_WIDEN_INTERVAL[11:0] 30 - CE_LENGTH[15:0] 34 - NEXT_SUP_TO[15:0] 38 - Reserved[1:0],LAST_UNMAPPED_CHANNEL[5:0],Reserved[3:0],SN,NESN,Reserved[1:0] 3C - ACCU_WINDOW_WIDEN[15:0] 40 - BT_SLOT_CAPTURE[15:0] 44 - Reserved[15:10],US_CAPTURE[9:0] 48 - Next Connection Instant 4C- Reserved[5:0]. US_OFFSET[9:0] Default Value: 0

22.1.179 BLE_BLELL_CONN_4_PARAM_MEM_BASE_ADDR

Connection Parameter memory base address for connection 4

Address: 0x403D3980

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CONN_4_PARAM [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CONN_4_PARAM [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description

22.1.179 BLE_BLELL_CONN_4_PARAM_MEM_BASE_ADDR (continued)

15 : 0	CONN_4_PARAM	Data values are written as 16-bit wide data. This memory is valid only if MMMS is enabled. The layout is as follows 00- AA[15:0] 04 - AA[31:16] 08 - CRC_init[15:0] 0C - WINDOW_SIZE[7:0],CRC_init[23:16] 10 - TX_WINDOW_OFFSET 14 - CI[15:0] 18 - SLV_LATENCY[15:0] 1C - SUPERVISORY_TIMEOUT_VAL[15:0] 20 - CHAN_MAP[15:0] 24 - CHAN_MAP[31:16] 28 - SCA[2:0],CHAN_HOP_INCR[4:0],CHAN_MAP[39:32] 2C - Reserved[1:0],RX_DATA_RATE_1M_2M,TX_DATA_RATE_1M_2M,WINDOW_WIDEN_INTERVAL[11:0] 30 - CE_LENGTH[15:0] 34 - NEXT_SUP_TO[15:0] 38 - Reserved[1:0],LAST_UNMAPPED_CHANNEL[5:0],Reserved[3:0],SN,NESN,Reserved[1:0] 3C - ACCU_WINDOW_WIDEN[15:0] 40 - BT_SLOT_CAPTURE[15:0] 44 - Reserved[15:10],US_CAPTURE[9:0] 48 - Next Connection Instant 4C- Reserved[5:0]. US_OFFSET[9:0] Default Value: 0

22.1.180 BLE_BLELL_NI_TIMER

Next Instant Timer

Address: 0x403D5000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	NI_TIMER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	NI_TIMER [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	NI_TIMER	BT Slot at which the next connection has to be serviced, granularity is 625us. The NI timer has to be programmed 1.25ms before the connection event Default Value: 0

22.1.181 BLE_BLELL_US_OFFSET

Micro-second Offset

Address: 0x403D5004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	US_OFFSET_SLOT_BOUNDARY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						US_OFF-SET_SLOT_BOUNDARY [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 0	US_OFF-SET_SLOT_BOUNDARY	Micro Second Offset from the Slot Bounday at which the connection programmed in NEXT_-CONN has to be serviced. This register along with NI_TIMER has to be programmed 1.25ms be-fore the connection event. The granularity is 1us Default Value: 0

22.1.182 BLE_BLELL_NEXT_CONN

Next Connection

Address: 0x403D5008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW1S	RW	RW				
HW Access	None	RW1C	R	R				
Name	None	NI_VALID	NEXT_-CONN_-TYPE	NEXT_CONN_INDEX [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
6	NI_VALID	Flag indication if programmed NI_TIMER is valid. FW sets this bit to indicate that the NI_TIMER is programmed. HW clears this bit on servicing the connection of if NI_TIMER is pointing to past value Default Value: 0
5	NEXT_CONN_TYPE	Connection type 1 - Master Connection 0 - Slave Connection Default Value: 0
4 : 0	NEXT_CONN_INDEX	Connection Index to be serviced. Allowed values are 0,1,2,3. Default Value: 0

22.1.183 BLE_BLELL_NI_ABORT

Abort next scheduled connection

Address: 0x403D500C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1C	RW
HW Access	None						RW1S	RW1C
Name	None [7:2]						ABORT_ACK	NI_ABORT

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	ABORT_ACK	This bit will set if the scheduled NI is aborted Default Value: 0
0	NI_ABORT	Setting this bit clears the schedule NI Default Value: 0

22.1.184 BLE_BLELL_CONN_NI_STATUS

Connection NI Status

Address: 0x403D5020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	CONN_NI [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	CONN_NI [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CONN_NI	HW updates this register with the next Connection Instant for current serviced connection, granularity is 625us. The reset value is 0x0000. After reset deassertion, then the very next clock, the value assigned to the registers is 0xFFFF. Default Value: 65535

22.1.185 BLE_BLELL_NEXT_SUP_TO_STATUS

Next Supervision timeout Status

Address: 0x403D5024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	NEXT_SUP_TO [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	NEXT_SUP_TO [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	NEXT_SUP_TO	HW updates this register for the SuperVision timeout next instant, granularity is 625us Default Value: 0

22.1.186 BLE_BLELL_MMMS_CONN_STATUS

Connection Status

Address: 0x403D5028

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R				
HW Access	RW	RW	RW	RW				
Name	NESN_CURR	SN_CURR	CURR_-CONN_-TYPE	CURR_CONN_INDEX [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	R	R	R					
HW Access	RW	RW	RW					
Name	AN-CHOR_PT_STATE	PKT_MISS	LAST_UNMAPPED_CHANNEL [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15	ANCHOR_PT_STATE	Anchor Point State 0 - Anchor point missed 1 - Anchor point established Default Value: 0
14	PKT_MISS	1 - Packet Missed 0 - Connection exchanged packets Default Value: 0
13 : 8	LAST_UN-MAPPED_CHANNEL	Last Unmapped Channel Default Value: 0
7	NESN_CURR	Next Sequence Number Default Value: 0
6	SN_CURR	Sequence Number of Packets exchanged Default Value: 0

22.1.186 BLE_BLELL_MMMS_CONN_STATUS (continued)

5	CURR_CONN_TYPE	Connection type 1 - Master Connection 0 - Slave Connection Default Value: 0
4 : 0	CURR_CONN_INDEX	Connection Index that was serviced. Legal values are 0,1,2,3. Default Value: 0

22.1.187 BLE_BLELL_BT_SLOT_CAPT_STATUS

BT Slot Captured Status

Address: 0x403D502C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	BT_SLOT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	BT_SLOT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	BT_SLOT	During slave connection event, HW updates this register with the captured BT_SLOT at anchor point, granularity is 625us Default Value: 0

22.1.188 BLE_BLELL_US_CAPT_STATUS

Micro-second Capture Status

Address: 0x403D5030

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	US_CAPT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						R	
HW Access	None						RW	
Name	None [15:10]						US_CAPT [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 0	US_CAPT	During slave connection event, HW updates this register with the captured microsecond at anchor point, granularity is 1us Default Value: 0

22.1.189 BLE_BLELL_US_OFFSET_STATUS

Micro-second Offset Status

Address: 0x403D5034

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	US_OFFSET [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	US_OFFSET [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	US_OFFSET	During slave connection event, HW updates this register with the calculated us_offset at anchor point, granularity is 1us. The reset value is 0x0000. After reset deassertion, then the very next clock, the value assigned to the registers is 0x00D5. Default Value: 213

22.1.190 BLE_BLELL_ACCU_WINDOW_WIDEN_STATUS

Accumulated Window Widen Status

Address: 0x403D5038

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	ACCU_WINDOW_WIDEN [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	ACCU_WINDOW_WIDEN [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	ACCU_WINDOW_WIDEN	Accumulated Window Widen Value. HW updates this register at the close of slave connection event Default Value: 0

22.1.191 BLE_BLELL_EARLY_INTR_STATUS

Status when early interrupt is raised

Address: 0x403D503C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		R	R				
HW Access	RW		RW	RW				
Name	US_FOR_EARLY_INTR [7:6]		CONN_-TYPE_-FOR_EARLY_INTR	CONN_INDEX_FOR_EARLY_INTR [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	US_FOR_EARLY_INTR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 6	US_FOR_EARLY_INTR	US offset when early interrupt is raised Default Value: 0
5	CONN_TYPE_FOR_EAR-LY_INTR	Connection type for which early interrupt is raised. Default Value: 0
4 : 0	CONN_INDEX_-FOR_EARLY_INTR	Connection Index for which early interrupt is raised Default Value: 0

22.1.192 BLE_BLELL_MMMS_CONFIG

Multi-Master Multi-Slave Config

Address: 0x403D5040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW	RW	RW	RW
HW Access	R				R	R	R	R
Name	ADV_CONN_INDEX [7:4]				CON-N_PARAM_FROM_REG	DISABLE_-CON-N_PARAM_MEM_WR	DISABLE_-CON-N_REQ_PARAM_IN_MEM	MMMS_EN-ABLE

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW1S	RW	RW
HW Access	None					RW1C	R	R
Name	None [15:11]					RE-SET_RX-_FIFO_PTR	CE_LEN_IMMEDI-ATE_EX-PIRE	ADV_CON-N_INDEX

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10	RESET_RX_FIFO_PTR	Setting this bit resets the receive FIFO pointers Default Value: 0
9	CE_LEN_IMMEDIATE_-EXPIRE	Enable for CE length immediate expiry Default Value: 0
8 : 4	ADV_CONN_INDEX	This field specifies the connection index for which ADV is enabled Default Value: 0
3	CONN_PARAM_-FROM_REG	By default the parameters for the connection are picked up from the connection parameters memory. Setting this bit disables this and the parameters are picked up from registers 0 - HW loads the parameters from connection memory 1 - Firmware should program the paramters for the connection event This bit is intended as a fail-safe. Should not be changed dynamically during runtime Default Value: 0

22.1.192 BLE_BLELL_MMMS_CONFIG (continued)

2	DISABLE_CON-N_PARAM_MEM_WR	By default on end_ce, the connection parameters memory is loaded with the updated connection parameters. Setting this bit prevent's this update. This bit is intended as a fail-safe. Should not be changed dynamically during runtime Default Value: 0
1	DISABLE_CON-N_REQ_PARAM_IN_MEM	If set to 1'b1 and MMMS enabled, then the parameters received in connection request are not stored in CONN_REQ_PARAM memory. By default this bit is 1'b0 and the connection request parameters are stored in connection memory. This bit is intended as a fail-safe. Should not be changed dynamically during runtime Default Value: 0
0	MMMS_ENABLE	Configuration bit to enable MMMS functionality Default Value: 0

22.1.193 BLE_BLELL_US_COUNTER

Running US of the current BT Slot

Address: 0x403D5044

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	US_COUNTER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						R	
HW Access	None						RW	
Name	None [15:10]						US_COUNTER [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 0	US_COUNTER	Current value of the US Counter Default Value: 0

22.1.194 BLE_BLELL_US_CAPT_PREV

Previous captured US of the BT Slot

Address: 0x403D5048

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	US_CAPT_LOAD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						RW	
Name	None [15:10]						US_CAPT_LOAD [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 0	US_CAPT_LOAD	HW uses this register to load the us_offset from connection parameter memory. This can be used by firmware as a fail safe option if the HW load from memory is disabled. In alll other conditions firmware should not use this register. Default Value: 0

22.1.195 BLE_BLELL_EARLY_INTR_NI

NI at early interrupt

Address: 0x403D504C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	EARLY_INTR_NI [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	EARLY_INTR_NI [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	EARLY_INTR_NI	Connection Next instant when the early interrupt is triggered Default Value: 0

22.1.196 BLE_BLELL_MMMS_MASTER_CREATE_BT_CAPT

BT slot capture for master connection creation

Address: 0x403D5080

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	BT_SLOT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	BT_SLOT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	BT_SLOT	This register captures the BT_SLOT when master connection is created, granularity is 625us Default Value: 0

22.1.197 BLE_BLELL_MMMS_SLAVE_CREATE_BT_CAPT

BT slot capture for slave connection creation

Address: 0x403D5084

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	US_CAPT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						R	
HW Access	None						RW	
Name	None [15:10]						US_CAPT [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 0	US_CAPT	This register captures the BT_SLOT when slave connection is created, granularity is 625us Default Value: 0

22.1.198 BLE_BLELL_MMMS_SLAVE_CREATE_US_CAPT

Micro second capture for slave connection creation

Address: 0x403D5088

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	US_OFFSET_SLAVE_CREATED [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	US_OFFSET_SLAVE_CREATED [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	US_OFF-SET_SLAVE_CREATED	This register captures the us when slave connection is created, granularity is 1us Default Value: 0

22.1.199 BLE_BLELL_MMMS_DATA_MEM_DESCRIPTOR0

Data buffer descriptor 0 to 15

Address: 0x403D5100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW						RW	
HW Access	R						R	
Name	DATA_LENGTH_C1 [7:2]						LLID_C1 [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						DATA_LENGTH_C1 [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 2	DATA_LENGTH_C1	This field indicates the length of the data packet. Bits [9:7] are valid only if DLE is set. Range 0x00 to 0xFF. Default Value: 0
1 : 0	LLID_C1	The LLID indicates whether the packet is an LL Data PDU or an LL Control PDU. 00b= Reserved. 01b=LL Data PDU: Continuation fragment of an L2CAP message or an Empty PDU. 10b=LL Data PDU: Start of an L@CAP message or a complete L2CAP message with no fragmentation. 11b=LL Control PDU. Default Value: 0

22.1.200 BLE_BLELL_CONN_1_DATA_LIST_SENT

data list sent update and status for connection 1

Address: 0x403D5200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W	None			RW			
HW Access	RW	None			RW			
Name	SET_-CLEAR_C1	None [6:4]			LIST_INDEX__TX_SENT_3_0_C1 [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				RW			
Name	None [15:12]				BUFFER_NUM_TX_SENT_3_0_C1 [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11 : 8	BUFFER_NUM_TX-_SENT_3_0_C1	Write: Indicates the buffer number for which SENT bit is updated by firmware. This is the mapping of the list index to the physical transmit buffer. The total number of transmit buffers is 16, can be shared with up to 8 connections Default Value: 0
7	SET_CLEAR_C1	Write: Used to set the SENT bit in hardware for the selected packet buffer. 1 packet queued When firmware has a packet to send, firmware first loads the next available packet buffer. Then the hardware SENT bit is set by writing 1 to this bit field along with the list_index field that identified the buffer index. This indicates that a packet has been queued in the data buffer for sending. This packet is now ready to be transmitted. The SENT bit in hardware is cleared by hardware only when it has received an acknowledgement from the remote device. Firmware typically does not clear the bit. However, It only clears the bit on its own if it needs to flush a packet from the buffer, without waiting to receive acknowledgement from the remote device, firmware clears BIT7 along with the list_index specified. Default Value: 0

22.1.200 BLE_BLELL_CONN_1_DATA_LIST_SENT (continued)

3 : 0	LIST_INDEX__TX-_SENT_3_0_C1	Write:Indicates the buffer index for which the SENT bit is being updated by firmware. The default number of buffers in the IP is 5. The index range is 0-3. Read: Reads TX_SENT[3:0]. The bits in this field indicate the status of the SENT bit in the hard-ware for each packet buffer. The bit values are 1 queued 0 no packet / packet ack received by hardware Example1: If the read value is : 0x03, then packets in buffer 0 and buffer 1 are in the queue to be transmitted. All the other FIFOs are empty or hardware has cleared them after receiving ac-knowledgement. Default Value: 0

22.1.201 BLE_BLELL_CONN_1_DATA_LIST_ACK

data list ack update and status for connection 1

Address: 0x403D5204

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W	None			RW			
HW Access	RW	None			RW			
Name	SET_-CLEAR_C1	None [6:4]			LIST_INDEX__TX_ACK_3_0_C1 [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	SET_CLEAR_C1	Write: Firmware uses the field to clear and ACK bit in the hardware to indicate that the acknowl-edgement for the transmit packet has been received and processed by firmware. Firmware clears the ACK bit in the hardware by writing in this register only after the acknowl-edgement is processed successfully by firmware. For clearing ack for a packet transmitted in fifo-index : 3, firm-ware will write 3 in the list-index field and set this bit (BIT7) to 0. This is the indication that the corresponding packet buffer identi-fied by List-Index is cleared of previous transmission and can be re-used for another packet from now on. The ACK bit in hardware is set by hardware when it has success-fully transmitted a packet. Default Value: 0

22.1.201 BLE_BLELL_CONN_1_DATA_LIST_ACK (continued)

3 : 0	LIST_INDEX__TX-_ACK_3_0_C1	Write: Indicates the buffer index for which the ACK bit is being updated by firmware. The default number of buffers in the IP is 5. The index range is 0-3. Read: Reads TX_ACK[3:0] If a particular bit is set, then the packet in the selected buffer has been transmitted (at least once) by the hardware and hardware is waiting for acknowledgement. Example1 : If the read value is : 0x03, then packets in FIFO-0 and FIFO-1 are acknowledged by the remote device. These acknowledgements are pending to be processed by firmware. Example2 : If the read value is : 0x02, then packet FIFO-1 is acknowledged by the remote device. This acknowledgement is pending to be processed by firmware. Default Value: 0

22.1.202 BLE_BLELL_CONN_1_CE_DATA_LIST_CFG

Connection specific pause resume for connection 1

Address: 0x403D5208

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW1S	RW			
HW Access	R	R	R	RW1C	R			
Name	MD_BIT_-CLEAR_C1	MD_C1	SLV_MD_-CON-FIG_C1	DATA_LIST_HEAD_UP_C1	DATA_LIST_INDEX_LAST_ACK_INDEX_C1 [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	R				RW1C	RW	RW	RW
HW Access	RW				RW	RW1C	RW1C	R
Name	CURRENT_PDU_INDEX_C1 [15:12]				EMPTYP-DU_SENT	KILL_CON-N_AFTER_TX	KILL_-CONN	PAUSE_-DATA_C1

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 12	CURRENT_PDU_INDEX-_C1	The index of the transmit packet buffer that is currently in transmission/waiting for transmission. Default Value: 0
11	EMPTYPDU_SENT	This bit indicates if EMPTYPDU has been sent. IF ACK is received this bit will be cleared by HW Default Value: 0
10	KILL_CONN_AFTER_TX	Kills the connection when the connection event is active and a TX is completed Default Value: 0
9	KILL_CONN	Kills the connection immediately when the connection event is active Default Value: 0
8	PAUSE_DATA_C1	Pause data. 1 - pause data, 0 - do not pause. The current_pdu_index in hardware does not move to next in-dex until pause_data is cleared. But if the SENT bit is set for the current_pdu_index as which pause is set, data will be sent out Default Value: 0

22.1.202 BLE_BLELL_CONN_1_CE_DATA_LIST_CFG (continued)

7	MD_BIT_CLEAR_C1	This register field indicates whether the MD (More Data) bit needs to be controlled by software or, hardware and software logic combined 1 - MD bit is exclusively controlled by software, based on status of bit [6]. 0 - MD Bit in the transmitted PDU is controlled by software and hardware logic. MD bit is set in transmitted packet, only if the software has set the MD in bit [6] and either of the following conditions is true, a) If there are packets queued for transmission. b) If there is an acknowledgement awaited from the remote side for the packet transmitted. Default Value: 0
6	MD_C1	MD bit set to 1 indicates device has more data to be sent. Default Value: 0
5	SLV_MD_CONFIG_C1	This bit is set to configure the MD bit control when the design is in slave mode. 1 - MD bit will be decided on packet pending status 0 - MD bit will be decided on packet queued in next buffer status This bit has valid only when MD_BIT_CLEAR bit is not set Default Value: 0
4	DATA_LIST_-HEAD_UP_C1	Update the first packet buffer index ready for transmis-sion to start/resume data transfer after a pause. The bit must be set every time the firmware needs to indicate the start/resume. Default Value: 0
3 : 0	DATA_LIST_INDEX-_LAST_ACK_INDEX_C1	Data list index for start/resume. This field must be valid along with data_list_head_up and indicate the transmit packet buffer index at which the data is loaded. The default number of buffers in the IP is 5,but may be customized for a customer. The buffers are in-dexed 0 to 4. Hardware will start the next data transmission from the index indicated by this field. Default Value: 0

22.1.203 BLE_BLELL_CONN_2_DATA_LIST_SENT

data list sent update and status for connection 2

Address: 0x403D5210

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W	None			RW			
HW Access	RW	None			RW			
Name	SET_-CLEAR_C1	None [6:4]			LIST_INDEX__TX_SENT_3_0_C1 [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				RW			
Name	None [15:12]				BUFFER_NUM_TX_SENT_3_0_C1 [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11 : 8	BUFFER_NUM_TX-_SENT_3_0_C1	Write: Indicates the buffer number for which SENT bit is updated by firmware. This is the mapping of the list index to the physical transmit buffer. The total number of transmit buffers is 16, can be shared with up to 8 connections Default Value: 0
7	SET_CLEAR_C1	Write: Used to set the SENT bit in hardware for the selected packet buffer. 1 packet queued When firmware has a packet to send, firmware first loads the next available packet buffer. Then the hardware SENT bit is set by writing 1 to this bit field along with the list_index field that identified the buffer index. This indicates that a packet has been queued in the data buffer for sending. This packet is now ready to be transmitted. The SENT bit in hardware is cleared by hardware only when it has received an acknowledgement from the remote device. Firmware typically does not clear the bit. However, It only clears the bit on its own if it needs to flush a packet from the buffer, without waiting to receive acknowledgement from the remote device, firmware clears BIT7 along with the list_index specified. Default Value: 0

22.1.203 BLE_BLELL_CONN_2_DATA_LIST_SENT (continued)

3 : 0	LIST_INDEX__TX-_SENT_3_0_C1	Write:Indicates the buffer index for which the SENT bit is being updated by firmware. The default number of buffers in the IP is 5. The index range is 0-3. Read: Reads TX_SENT[3:0]. The bits in this field indicate the status of the SENT bit in the hard-ware for each packet buffer. The bit values are 1 queued 0 no packet / packet ack received by hardware Example1: If the read value is : 0x03, then packets in buffer 0 and buffer 1 are in the queue to be transmitted. All the other FIFOs are empty or hardware has cleared them after receiving ac-knowledgement. Default Value: 0

22.1.204 BLE_BLELL_CONN_2_DATA_LIST_ACK

data list ack update and status for connection 2

Address: 0x403D5214

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W	None			RW			
HW Access	RW	None			RW			
Name	SET_-CLEAR_C1	None [6:4]			LIST_INDEX__TX_ACK_3_0_C1 [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	SET_CLEAR_C1	Write: Firmware uses the field to clear and ACK bit in the hardware to indicate that the acknowledgement for the transmit packet has been received and processed by firmware. Firmware clears the ACK bit in the hardware by writing in this register only after the acknowledgement is processed successfully by firmware. For clearing ack for a packet transmitted in fifo-index : 3, firm-ware will write 3 in the list-index field and set this bit (BIT7) to 0. This is the indication that the corresponding packet buffer identi-fied by List-Index is cleared of previous transmission and can be re-used for another packet from now on. The ACK bit in hardware is set by hardware when it has success-fully transmitted a packet. Default Value: 0

22.1.204 BLE_BLELL_CONN_2_DATA_LIST_ACK (continued)

3 : 0	LIST_INDEX__TX-_ACK_3_0_C1	Write: Indicates the buffer index for which the ACK bit is being updated by firmware. The default number of buffers in the IP is 5. The index range is 0-3. Read: Reads TX_ACK[3:0] If a particular bit is set, then the packet in the selected buffer has been transmitted (at least once) by the hardware and hardware is waiting for acknowledgement. Example1 : If the read value is : 0x03, then packets in FIFO-0 and FIFO-1 are acknowledged by the remote device. These acknowledgements are pending to be processed by firmware. Example2 : If the read value is : 0x02, then packet FIFO-1 is acknowledged by the remote device. This acknowledgement is pending to be processed by firmware. Default Value: 0

22.1.205 BLE_BLELL_CONN_2_CE_DATA_LIST_CFG

Connection specific pause resume for connection 2

Address: 0x403D5218

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW1S	RW			
HW Access	R	R	R	RW1C	R			
Name	MD_BIT_-CLEAR_C1	MD_C1	SLV_MD_-CON-FIG_C1	DATA_LIST_HEAD_UP_C1	DATA_LIST_INDEX_LAST_ACK_INDEX_C1 [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	R				RW1C	RW	RW	RW
HW Access	RW				RW	RW1C	RW1C	R
Name	CURRENT_PDU_INDEX_C1 [15:12]				EMPTYP-DU_SENT	KILL_CON-N_AFTER_TX	KILL_-CONN	PAUSE_-DATA_C1

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 12	CURRENT_PDU_INDEX-_C1	The index of the transmit packet buffer that is currently in transmission/waiting for transmission. Default Value: 0
11	EMPTYPDU_SENT	This bit indicates if EMPTYPDU has been sent. IF ACK is received this bit will be cleared by HW Default Value: 0
10	KILL_CONN_AFTER_TX	Kills the connection when the connection event is active and a TX is completed Default Value: 0
9	KILL_CONN	Kills the connection immediately when the connection event is active Default Value: 0
8	PAUSE_DATA_C1	Pause data. 1 - pause data, 0 - do not pause. The current_pdu_index in hardware does not move to next in-dex until pause_data is cleared. But if the SENT bit is set for the current_pdu_index as which pause is set, data will be sent out Default Value: 0

22.1.205 BLE_BLELL_CONN_2_CE_DATA_LIST_CFG (continued)

7	MD_BIT_CLEAR_C1	This register field indicates whether the MD (More Data) bit needs to be controlled by software or, hardware and software logic combined 1 - MD bit is exclusively controlled by software, based on status of bit [6]. 0 - MD Bit in the transmitted PDU is controlled by software and hardware logic. MD bit is set in transmitted packet, only if the software has set the MD in bit [6] and either of the following conditions is true, a) If there are packets queued for transmission. b) If there is an acknowledgement awaited from the remote side for the packet transmitted. Default Value: 0
6	MD_C1	MD bit set to 1 indicates device has more data to be sent. Default Value: 0
5	SLV_MD_CONFIG_C1	This bit is set to configure the MD bit control when the design is in slave mode. 1 - MD bit will be decided on packet pending status 0 - MD bit will be decided on packet queued in next buffer status This bit has valid only when MD_BIT_CLEAR bit is not set Default Value: 0
4	DATA_LIST_- HEAD_UP_C1	Update the first packet buffer index ready for transmis-sion to start/resume data transfer after a pause. The bit must be set every time the firmware needs to indicate the start/resume. Default Value: 0
3 : 0	DATA_LIST_INDEX- _LAST_ACK_INDEX_C1	Data list index for start/resume. This field must be valid along with data_list_head_up and indicate the transmit packet buffer index at which the data is loaded. The default number of buffers in the IP is 5,but may be customized for a customer. The buffers are in-dexed 0 to 4. Hardware will start the next data transmission from the index indicated by this field. Default Value: 0

22.1.206 BLE_BLELL_CONN_3_DATA_LIST_SENT

data list sent update and status for connection 3

Address: 0x403D5220

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W	None			RW			
HW Access	RW	None			RW			
Name	SET_-CLEAR_C1	None [6:4]			LIST_INDEX__TX_SENT_3_0_C1 [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				RW			
Name	None [15:12]				BUFFER_NUM_TX_SENT_3_0_C1 [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11 : 8	BUFFER_NUM_TX-_SENT_3_0_C1	Write: Indicates the buffer number for which SENT bit is updated by firmware. This is the mapping of the list index to the physical transmit buffer. The total number of transmit buffers is 16, can be shared with up to 8 connections Default Value: 0
7	SET_CLEAR_C1	Write: Used to set the SENT bit in hardware for the selected packet buffer. 1 packet queued When firmware has a packet to send, firmware first loads the next available packet buffer. Then the hardware SENT bit is set by writing 1 to this bit field along with the list_index field that identified the buffer index. This indicates that a packet has been queued in the data buffer for sending. This packet is now ready to be transmitted. The SENT bit in hardware is cleared by hardware only when it has received an acknowledgement from the remote device. Firmware typically does not clear the bit. However, It only clears the bit on its own if it needs to flush a packet from the buffer, without waiting to receive acknowledgement from the remote device, firmware clears BIT7 along with the list_index specified. Default Value: 0

22.1.206 BLE_BLELL_CONN_3_DATA_LIST_SENT (continued)

3 : 0	LIST_INDEX__TX-_SENT_3_0_C1	Write:Indicates the buffer index for which the SENT bit is being updated by firmware. The default number of buffers in the IP is 5. The index range is 0-3. Read: Reads TX_SENT[3:0]. The bits in this field indicate the status of the SENT bit in the hard-ware for each packet buffer. The bit values are 1 queued 0 no packet / packet ack received by hardware Example1: If the read value is : 0x03, then packets in buffer 0 and buffer 1 are in the queue to be transmitted. All the other FIFOs are empty or hardware has cleared them after receiving ac-knowledgement. Default Value: 0

22.1.207 BLE_BLELL_CONN_3_DATA_LIST_ACK

data list ack update and status for connection 3

Address: 0x403D5224

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W	None			RW			
HW Access	RW	None			RW			
Name	SET_-CLEAR_C1	None [6:4]			LIST_INDEX__TX_ACK_3_0_C1 [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	SET_CLEAR_C1	Write: Firmware uses the field to clear and ACK bit in the hardware to indicate that the acknowledgement for the transmit packet has been received and processed by firmware. Firmware clears the ACK bit in the hardware by writing in this register only after the acknowledgement is processed successfully by firmware. For clearing ack for a packet transmitted in fifo-index : 3, firm-ware will write 3 in the list-index field and set this bit (BIT7) to 0. This is the indication that the corresponding packet buffer identi-fied by List-Index is cleared of previous transmission and can be re-used for another packet from now on. The ACK bit in hardware is set by hardware when it has success-fully transmitted a packet. Default Value: 0

22.1.207 BLE_BLELL_CONN_3_DATA_LIST_ACK (continued)

3 : 0	LIST_INDEX__TX-_ACK_3_0_C1	Write: Indicates the buffer index for which the ACK bit is being updated by firmware. The default number of buffers in the IP is 5. The index range is 0-3. Read: Reads TX_ACK[3:0] If a particular bit is set, then the packet in the selected buffer has been transmitted (at least once) by the hardware and hardware is waiting for acknowledgement. Example1 : If the read value is : 0x03, then packets in FIFO-0 and FIFO-1 are acknowledged by the remote device. These acknowledgements are pending to be processed by firmware. Example2 : If the read value is : 0x02, then packet FIFO-1 is acknowledged by the remote device. This acknowledgement is pending to be processed by firmware. Default Value: 0

22.1.208 BLE_BLELL_CONN_3_CE_DATA_LIST_CFG

Connection specific pause resume for connection 3

Address: 0x403D5228

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW1S	RW			
HW Access	R	R	R	RW1C	R			
Name	MD_BIT_-CLEAR_C1	MD_C1	SLV_MD_-CON-FIG_C1	DATA_LIST_HEAD_UP_C1	DATA_LIST_INDEX_LAST_ACK_INDEX_C1 [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	R				RW1C	RW	RW	RW
HW Access	RW				RW	RW1C	RW1C	R
Name	CURRENT_PDU_INDEX_C1 [15:12]				EMPTYP-DU_SENT	KILL_CON-N_AFTER_TX	KILL_-CONN	PAUSE_-DATA_C1

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 12	CURRENT_PDU_INDEX-_C1	The index of the transmit packet buffer that is currently in transmission/waiting for transmission. Default Value: 0
11	EMPTYPDU_SENT	This bit indicates if EMPTYPDU has been sent. IF ACK is received this bit will be cleared by HW Default Value: 0
10	KILL_CONN_AFTER_TX	Kills the connection when the connection event is active and a TX is completed Default Value: 0
9	KILL_CONN	Kills the connection immediately when the connection event is active Default Value: 0
8	PAUSE_DATA_C1	Pause data. 1 - pause data, 0 - do not pause. The current_pdu_index in hardware does not move to next in-dex until pause_data is cleared. But if the SENT bit is set for the current_pdu_index as which pause is set, data will be sent out Default Value: 0

22.1.208 BLE_BLELL_CONN_3_CE_DATA_LIST_CFG (continued)

7	MD_BIT_CLEAR_C1	This register field indicates whether the MD (More Data) bit needs to be controlled by software or, hardware and software logic combined 1 - MD bit is exclusively controlled by software, based on status of bit [6]. 0 - MD Bit in the transmitted PDU is controlled by software and hardware logic. MD bit is set in transmitted packet, only if the software has set the MD in bit [6] and either of the following conditions is true, a) If there are packets queued for transmission. b) If there is an acknowledgement awaited from the remote side for the packet transmitted. Default Value: 0
6	MD_C1	MD bit set to 1 indicates device has more data to be sent. Default Value: 0
5	SLV_MD_CONFIG_C1	This bit is set to configure the MD bit control when the design is in slave mode. 1 - MD bit will be decided on packet pending status 0 - MD bit will be decided on packet queued in next buffer status This bit has valid only when MD_BIT_CLEAR bit is not set Default Value: 0
4	DATA_LIST_- HEAD_UP_C1	Update the first packet buffer index ready for transmis-sion to start/resume data transfer after a pause. The bit must be set every time the firmware needs to indicate the start/resume. Default Value: 0
3 : 0	DATA_LIST_INDEX- _LAST_ACK_INDEX_C1	Data list index for start/resume. This field must be valid along with data_list_head_up and indicate the transmit packet buffer index at which the data is loaded. The default number of buffers in the IP is 5,but may be customized for a customer. The buffers are in-dexed 0 to 4. Hardware will start the next data transmission from the index indicated by this field. Default Value: 0

22.1.209 BLE_BLELL_CONN_4_DATA_LIST_SENT

data list sent update and status for connection 4

Address: 0x403D5230

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W	None			RW			
HW Access	RW	None			RW			
Name	SET_-CLEAR_C1	None [6:4]			LIST_INDEX__TX_SENT_3_0_C1 [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				RW			
Name	None [15:12]				BUFFER_NUM_TX_SENT_3_0_C1 [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11 : 8	BUFFER_NUM_TX-_SENT_3_0_C1	Write: Indicates the buffer number for which SENT bit is updated by firmware. This is the mapping of the list index to the physical transmit buffer. The total number of transmit buffers is 16, can be shared with up to 8 connections Default Value: 0
7	SET_CLEAR_C1	Write: Used to set the SENT bit in hardware for the selected packet buffer. 1 packet queued When firmware has a packet to send, firmware first loads the next available packet buffer. Then the hardware SENT bit is set by writing 1 to this bit field along with the list_index field that identified the buffer index. This indicates that a packet has been queued in the data buffer for sending. This packet is now ready to be transmitted. The SENT bit in hardware is cleared by hardware only when it has received an acknowledgement from the remote device. Firmware typically does not clear the bit. However, It only clears the bit on its own if it needs to flush a packet from the buffer, without waiting to receive acknowledgement from the remote device, firmware clears BIT7 along with the list_index specified. Default Value: 0

22.1.209 BLE_BLELL_CONN_4_DATA_LIST_SENT (continued)

3 : 0	LIST_INDEX__TX-_SENT_3_0_C1	Write:Indicates the buffer index for which the SENT bit is being updated by firmware. The default number of buffers in the IP is 5. The index range is 0-3. Read: Reads TX_SENT[3:0]. The bits in this field indicate the status of the SENT bit in the hard-ware for each packet buffer. The bit values are 1 queued 0 no packet / packet ack received by hardware Example1: If the read value is : 0x03, then packets in buffer 0 and buffer 1 are in the queue to be transmitted. All the other FIFOs are empty or hardware has cleared them after receiving ac-knowledgement. Default Value: 0

22.1.210 BLE_BLELL_CONN_4_DATA_LIST_ACK

data list ack update and status for connection 4

Address: 0x403D5234

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W	None			RW			
HW Access	RW	None			RW			
Name	SET_-CLEAR_C1	None [6:4]			LIST_INDEX__TX_ACK_3_0_C1 [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	SET_CLEAR_C1	Write: Firmware uses the field to clear and ACK bit in the hardware to indicate that the acknowledgement for the transmit packet has been received and processed by firmware. Firmware clears the ACK bit in the hardware by writing in this register only after the acknowledgement is processed successfully by firmware. For clearing ack for a packet transmitted in fifo-index : 3, firm-ware will write 3 in the list-index field and set this bit (BIT7) to 0. This is the indication that the corresponding packet buffer identi-fied by List-Index is cleared of previous transmission and can be re-used for another packet from now on. The ACK bit in hardware is set by hardware when it has success-fully transmitted a packet. Default Value: 0

22.1.210 BLE_BLELL_CONN_4_DATA_LIST_ACK (continued)

3 : 0	LIST_INDEX__TX-_ACK_3_0_C1	Write: Indicates the buffer index for which the ACK bit is being updated by firmware. The default number of buffers in the IP is 5. The index range is 0-3. Read: Reads TX_ACK[3:0] If a particular bit is set, then the packet in the selected buffer has been transmitted (at least once) by the hardware and hardware is waiting for acknowledgement. Example1 : If the read value is : 0x03, then packets in FIFO-0 and FIFO-1 are acknowledged by the remote device. These acknowledgements are pending to be processed by firmware. Example2 : If the read value is : 0x02, then packet FIFO-1 is acknowledged by the remote device. This acknowledgement is pending to be processed by firmware. Default Value: 0

22.1.211 BLE_BLELL_CONN_4_CE_DATA_LIST_CFG

Connection specific pause resume for connection 4

Address: 0x403D5238

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW1S	RW			
HW Access	R	R	R	RW1C	R			
Name	MD_BIT_-CLEAR_C1	MD_C1	SLV_MD_-CON-FIG_C1	DATA_LIST_HEAD_UP_C1	DATA_LIST_INDEX_LAST_ACK_INDEX_C1 [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	R				RW1C	RW	RW	RW
HW Access	RW				RW	RW1C	RW1C	R
Name	CURRENT_PDU_INDEX_C1 [15:12]				EMPTYP-DU_SENT	KILL_CON-N_AFTER_TX	KILL_-CONN	PAUSE_-DATA_C1

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 12	CURRENT_PDU_INDEX-_C1	The index of the transmit packet buffer that is currently in transmission/waiting for transmission. Default Value: 0
11	EMPTYPDU_SENT	This bit indicates if EMPTYPDU has been sent. IF ACK is received this bit will be cleared by HW Default Value: 0
10	KILL_CONN_AFTER_TX	Kills the connection when the connection event is active and a TX is completed Default Value: 0
9	KILL_CONN	Kills the connection immediately when the connection event is active Default Value: 0
8	PAUSE_DATA_C1	Pause data. 1 - pause data, 0 - do not pause. The current_pdu_index in hardware does not move to next in-dex until pause_data is cleared. But if the SENT bit is set for the current_pdu_index as which pause is set, data will be sent out Default Value: 0

22.1.211 BLE_BLELL_CONN_4_CE_DATA_LIST_CFG (continued)

7	MD_BIT_CLEAR_C1	This register field indicates whether the MD (More Data) bit needs to be controlled by software or, hardware and software logic combined 1 - MD bit is exclusively controlled by software, based on status of bit [6]. 0 - MD Bit in the transmitted PDU is controlled by software and hardware logic. MD bit is set in transmitted packet, only if the software has set the MD in bit [6] and either of the following conditions is true, a) If there are packets queued for transmission. b) If there is an acknowledgement awaited from the remote side for the packet transmitted. Default Value: 0
6	MD_C1	MD bit set to 1 indicates device has more data to be sent. Default Value: 0
5	SLV_MD_CONFIG_C1	This bit is set to configure the MD bit control when the design is in slave mode. 1 - MD bit will be decided on packet pending status 0 - MD bit will be decided on packet queued in next buffer status This bit has valid only when MD_BIT_CLEAR bit is not set Default Value: 0
4	DATA_LIST_-HEAD_UP_C1	Update the first packet buffer index ready for transmis-sion to start/resume data transfer after a pause. The bit must be set every time the firmware needs to indicate the start/resume. Default Value: 0
3 : 0	DATA_LIST_INDEX-_LAST_ACK_INDEX_C1	Data list index for start/resume. This field must be valid along with data_list_head_up and indicate the transmit packet buffer index at which the data is loaded. The default number of buffers in the IP is 5,but may be customized for a customer. The buffers are in-dexed 0 to 4. Hardware will start the next data transmission from the index indicated by this field. Default Value: 0

22.1.212 BLE_BLELL_MMMS_ADVCH_NI_ENABLE

Enable bits for ADV_NI, SCAN_NI and INIT_NI

Address: 0x403D5400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [7:3]					INIT_NI_ENABLE	SCAN_NI_ENABLE	ADV_NI_ENABLE

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	INIT_NI_ENABLE	This bit is used to enable the INIT NI timer and is valid when MMMS_ENABLE=1. 0 - INIT_NI timer is disabled 1 - INIT_NI timer is enabled In this mode, the init engine next instant is scheduled by firmware Default Value: 0
1	SCAN_NI_ENABLE	This bit is used to enable the SCAN NI timer and is valid when MMMS_ENABLE=1. 0 - SCAN_NI timer is disabled 1 - SCAN_NI timer is enabled In this mode, the scan engine next instant is scheduled by firmware Default Value: 0
0	ADV_NI_ENABLE	This bit is used to enable the Advertisement NI timer and is valid when MMMS_ENABLE=1. 0 - ADV_NI timer is disabled 1 - ADV_NI timer is enabled In this mode, the adv engine next instant is scheduled by firmware Default Value: 0

22.1.213 BLE_BLELL_MMMS_ADVCH_NI_VALID

Next instant valid for ADV, SCAN, INIT

Address: 0x403D5404

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW1S	RW1S	RW1S
HW Access	None					RW1C	RW1C	RW1C
Name	None [7:3]					INIT_NI_VALID	SCAN_NI_VALID	ADV_NI_VALID

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	INIT_NI_VALID	This bit indicates if the programmed initiator NI_TIMER is valid. FW sets this bit to indicate that the NI_TIMER is programmed. HW clears this bit on servicing the initiator event 0 - INIT_NI timer is not valid 1 - INIT_NI timer is valid Default Value: 0
1	SCAN_NI_VALID	This bit indicates if the programmed scan NI_TIMER is valid. FW sets this bit to indicate that the NI_TIMER is programmed. HW clears this bit on servicing the scanner event 0 - SCAN_NI timer is not valid 1 - SCAN_NI timer is valid Default Value: 0
0	ADV_NI_VALID	This bit indicates if the programmed advertisement NI_TIMER is valid. FW sets this bit to indicate that the NI_TIMER is programmed. HW clears this bit on servicing the advertisment event 0 - ADV_NI timer is not valid 1 - ADV_NI timer is valid Default Value: 0

22.1.214 BLE_BLELL_MMMS_ADVCH_NI_ABORT

Abort the next instant of ADV, SCAN, INIT

Address: 0x403D5408

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1C	W
HW Access	None						RW1S	RW1C
Name	None [7:2]						AD-VCH_ABORT_STATUS	AD-VCH_NI_ABORT

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	ADVCH_ABORT_STA-TUS	The link layer hardware logic will set this bit when the NI_TIMER is aborted. Firmware to clear this by writing 1'b1 to this register bit Default Value: 0
0	ADVCH_NI_ABORT	FW can use this bit to clear an unserviced NI_VALID for Advertisement or scanner or initiator. HW will clear NI_VALID for ADV/SCAN/INIT if the event has not yet started Default Value: 0

22.1.215 BLE_BLELL_CONN_PARAM_NEXT_SUP_TO

Register to configure the supervision timeout for next scheduled connection

Address: 0x403D5410

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	NEXT_SUP_TO_LOAD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	NEXT_SUP_TO_LOAD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	NEXT_SUP_TO_LOAD	HW uses this register to load the Supervision timeout Next instant from the connection memory. This can be used by firmware as a failsafe option when the hardware load is disabled. In all other conditions, this register should not be updated by firmware. Default Value: 0

22.1.216 BLE_BLELL_CONN_PARAM_ACC_WIN_WIDEN

Register to configure Accumulated window widening for next scheduled connection

Address: 0x403D5414

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	ACC_WINDOW_WIDEN [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						ACC_WINDOW_WIDEN [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 0	ACC_WINDOW_WIDEN	HW uses this register to load the accumulated window windeing value from the connection memory. This can be used by firmware as a failsafe option when the hardware load is disabled. In all other conditions, this register should not be updated by firmware. Default Value: 0

22.1.217 BLE_BLELL_HW_LOAD_OFFSET

Register to configure offset from connection anchor point at which connection parameter memory should be read

Address: 0x403D5420

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			R				
Name	None [7:5]			LOAD_OFFSET [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4 : 0	LOAD_OFFSET	Load Offset in us before connection event at which the connection parameters are loaded from memory, granularity is in 1us Default Value: 4

22.1.218 BLE_BLELL_ADV_RAND

Random number generated by Hardware for ADV NI calculation

Address: 0x403D5424

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R			
HW Access	None				RW			
Name	None [7:4]				ADV_RAND [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	ADV_RAND	Random ADV delay, to be used for ADV next instant calculation. The granularity is in BT slot Default Value: 7

22.1.219 BLE_BLELL_MMMS_RX_PKT_CNTR

Packet Counter of packets in RX FIFO in MMMS mode

Address: 0x403D5428

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R					
HW Access	None		RW					
Name	None [7:6]		MMMS_RX_PKT_CNT [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	MMMS_RX_PKT_CNT	Count of all packets in the RX FIFO in MMMS mode Default Value: 0

22.1.220 BLE_BLELL_CONN_RX_PKT_CNTR0

Packet Counter for Individual connection index

Address: 0x403D5430

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R					
HW Access	None		RW					
Name	None [7:6]		RX_PKT_CNT [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	RX_PKT_CNT	Number of packets received for the connection. Incremented when the packet is received during the connection event and decremented when firmware has processed the packet. The register field FW_PKT_RCV_CONN_INDEX should be programmed before firmware issues the packet received command Default Value: 0

22.1.221 BLE_BLELL_WHITELIST_BASE_ADDR

Whitelist base address

Address: 0x403D5800

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	WL_BASE_ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	WL_BASE_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	WL_BASE_ADDR	Device address values written to white list memory are written as 16-bit wide address. Default Value: 0

22.1.222 BLE_BLELL_RSLV_LIST_PEER_IDNTT_BASE_ADDR

Resolving list base address for storing Peer Identity address

Address: 0x403D58C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	RSLV_LIST_PEER_IDNTT_BASE_ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	RSLV_LIST_PEER_IDNTT_BASE_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	RSLV_LIST_PEER_ID-NTT_BASE_ADDR	Device address values written to the list are written as 16-bit wide address. Default Value: 0

22.1.223 BLE_BLELL_RSLV_LIST_PEER_RPA_BASE_ADDR

Resolving list base address for storing resolved Peer RPA address

Address: 0x403D5980

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	RSLV_LIST_PEER_RPA_BASE_ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	RSLV_LIST_PEER_RPA_BASE_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	RSLV_LIST_PEER_R-PA_BASE_ADDR	Device address values written to the list are written as 16-bit wide address. Default Value: 0

22.1.224 BLE_BLELL_RSLV_LIST_RCVD_INIT_RPA_BASE_ADDR

Resolving list base address for storing Resolved received INITA RPA

Address: 0x403D5A40

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	RSLV_LIST_RCVD_INIT_RPA_BASE_ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	RSLV_LIST_RCVD_INIT_RPA_BASE_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	RSLV_LIST_RCVD_INIT_RPA_BASE_ADDR	Device address values written to the list are written as 16-bit wide address. Default Value: 0

22.1.225 BLE_BLELL_RSLV_LIST_TX_INIT_RPA_BASE_ADDR

Resolving list base address for storing generated TX INITA RPA

Address: 0x403D5B00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	RSLV_LIST_TX_INIT_RPA_BASE_ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	RSLV_LIST_TX_INIT_RPA_BASE_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	RSLV_LIST_TX_INIT_R-PA_BASE_ADDR	Device address values written to the list are written as 16-bit wide address. Default Value: 0

22.1.226 BLE_BLESS_XTAL_CLK_DIV_CONFIG

Crystal clock divider configuration register

Address: 0x403DF064

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW		RW	
HW Access	None				R		R	
Name	None [7:4]				LLCLK_DIV [3:2]		SYSCLK_DIV [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 2	LLCLK_DIV	Link Layer clock pre-divider value. The 24 MHz crystal clock is divided to generate the Link Layer clock. 0: NO_DIV: LLCLK= XTALCLK/1 1: DIV_BY_2: LLCLK= XTALCLK/2 2: DIV_BY_4: LLCLK= XTALCLK/4 3: DIV_BY_8: LLCLK= XTALCLK/8 Default Value: 0
1 : 0	SYSCLK_DIV	System clock pre-divider value. The 24 MHz crystal clock is divided to generate the system clock. 0: NO_DIV: SYSCLK= XTALCLK/1 1: DIV_BY_2: SYSCLK= XTALCLK/2 2: DIV_BY_4: SYSCLK= XTALCLK/4 3: DIV_BY_8: SYSCLK= XTALCLK/8 Default Value: 0

22.1.227 BLE_BLESS_INTR_STAT

Link Layer interrupt status register

Address: 0x403DF068

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	R	R	RW1C	R	RW1C	RW1C
HW Access	RW1S	RW1S	RW	RW	RW1S	RW	RW1S	RW1S
Name	EFUSE_INTR	GPIO_INTR	LL_INTR	RCB_INTR	BLERD_ACTIVE_INTR	RCBLL_DONE_INTR	DSM_EXITED_INTR	DSM_ENTERED_INTR

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW1C	RW1C	R	RW1C
HW Access	None				RW1S	RW1S	RW	RW1S
Name	None [15:12]				HVLDO_LV_DETECT_NEG	HVLDO_LV_DETECT_POS	ENC_INTR	XTAL_ON_INTR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	HVLDO_LV_DETECT_NEG	This interrupt is set on HVLDO LV Detector Fall edge. There is a 1cycle AHB clock glitch filter on the HVLDO LV Detector output Default Value: 0
10	HVLDO_LV_DETECT_POS	This interrupt is set on HVLDO LV Detector Rise edge. There is a 1cycle AHB clock glitch filter on the HVLDO LV Detector output Default Value: 0
9	ENC_INTR	Encryption Interrupt Triggered Default Value: 0
8	XTAL_ON_INTR	enabled crystal stable signal rising edge interrupt. The interrupt can be cleared by writing one into this location. Default Value: 0
7	EFUSE_INTR	This bit when set by efuse controller logic when the efuse read/write is completed Default Value: 0

22.1.227 BLE_BLESS_INTR_STAT (continued)

6	GPIO_INTR	GPIO interrupt Default Value: 0
5	LL_INTR	LL controller interrupt - Refer to EVENT_INTR register Default Value: 0
4	RCB_INTR	RCB controller Interrupt - Refer to RCB_INTR_STAT register Default Value: 0
3	BLERD_ACTIVE_INTR	CYBLERD55 is in active mode. RF is active Default Value: 0
2	RCBLL_DONE_INTR	RCB transaction Complete Default Value: 0
1	DSM_EXITED_INTR	On a firmware request to LL to exit from Deep Sleep Mode, working on LF clock, LL transitions from Deep Sleep Mode and asserts this interrupt when the Deep Sleep clock gater is turned ON. The interrupt can be cleared by writing one into this location. Default Value: 0
0	DSM_ENTERED_INTR	On a firmware request to LL to enter into state machine, working on LF clock, LL transitions into Deep Sleep Mode and asserts this interrupt. The interrupt can be cleared by writing one into this location. Default Value: 0

22.1.228 BLE_BLESS_INTR_MASK

Link Layer interrupt mask register

Address: 0x403DF06C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	RW1C
Name	LL_INTR_MASK	RCB_INTR_MASK	BLERD_ACTIVE_INTR_MASK	RCBLL_INTR_MASK	XTAL_ON_INTR_MASK	DSM_EXITED_INTR_MASK	DSM_ENTERED_INTR_MASK	DSM_EXIT

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [15:13]			HVLDO_LV_DETECT_NEG_MASK	HVLDO_LV_DETECT_POS_MASK	ENC_INTR_MASK	EFUSE_INTR_MASK	GPIO_INTR_MASK

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
12	HVLDO_LV_DETECT_NEG_MASK	Mask for HVLDO LV Detector Fall edge interrupt Default Value: 0
11	HVLDO_LV_DETECT_POS_MASK	Mask for HVLDO LV Detector Rise edge interrupt Default Value: 0
10	ENC_INTR_MASK	Mask for Encryption interrupt Default Value: 0
9	EFUSE_INTR_MASK	This bit enables the efuse interrupt to firmware Default Value: 0
8	GPIO_INTR_MASK	Mask for GPIO interrupt Default Value: 0
7	LL_INTR_MASK	Mask for LL interrupt Default Value: 0

22.1.228 BLE_BLESS_INTR_MASK (continued)

6	RCB_INTR_MASK	Mask for RCB interrupt Default Value: 0
5	BLERD_ACTIVE_IN-TR_MASK	Mask for CYBLERD55 Active Interrupt Default Value: 0
4	RCBLL_INTR_MASK	Mask for RCBLL interrupt Default Value: 0
3	XTAL_ON_INTR_MASK	Masks the Crystal Stable Interrupt, when disabled. Default Value: 0
2	DSM_EXITED_IN-TR_MASK	Masks the DSM Exited Interrupt, when disabled. Default Value: 0
1	DSM_ENTERED_IN-TR_MASK	Masks the DSM Entered Interrupt, when disabled. Default Value: 0
0	DSM_EXIT	When the Link Layer is in Deep Sleep Mode, firmware can set this bit to wake the Link Layer. Default Value: 0

22.1.229 BLE_BLESS_LL_CLK_EN

Link Layer primary clock enable

Address: 0x403DF070

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		R	R	R	R	R	R
Name	None [7:6]		DPS-LP_HWRC-B_EN	BLESS_RE-SET	SEL_RCB_-CLK	MX-D_IF_OP-TION	CY_COR-REL_EN	CLK_EN

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	DPSLP_HWRCB_EN	Controls the DPSLP entry and exit writes to RD and controls the active domain reset and clock. 1 - LL HW controls the RD active domain reset and clock. 0 - The RD active domain reset and clock. Must be controlled by the FW Default Value: 1
4	BLESS_RESET	0: No Soft Reset 1: Initiate Soft Reset Setting this bit will reset entire BLESS_VER3 Default Value: 0
3	SEL_RCB_CLK	0: AHB clock (clk_sys) is used as the clock for RCB access 1: LL clock (clk_eco) is used as the clock for RCB access Default Value: 0
2	MXD_IF_OPTION	1: MXD IF option 0: CYBLERD55 correlates Access Code 0: MXD IF option 1: LL correlates Access Code Default Value: 1

22.1.229 BLE_BLESS_LL_CLK_EN (continued)

1	CY_CORREL_EN	If MXD_IF option is 1, this bit needs to be set to enable configuring the correlator through BLELL.DPLL_CONFIG register Default Value: 1
0	CLK_EN	Set this bit 1 to enable the clock to Link Layer. Default Value: 0

22.1.230 BLE_BLESS_LF_CLK_CTRL

BLESS LF clock control and BLESS revision ID indicator

Address: 0x403DF074

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						EN-ABLE_ENC_CLK	DIS-ABLE_LF_-CLK

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R			None				
HW Access	R			None				
Name	RESERVED [31:29]			None [28:24]				

Bits	Name	Description
31 : 29	RESERVED	Reserved Default Value: 2
1	ENABLE_ENC_CLK	This bit is used to enable the clock to the encryption engine 0 - Disable the clock to ENC engine 1 - Enable the clock to ENC engine Default Value: 0
0	DISABLE_LF_CLK	When set to 1, gates the LF clock input to the Link Layer. Ths is done for extended DSM mode where the DSM state machine needs to be forzen to prevent a default auto exit. Default Value: 0

22.1.231 BLE_BLESS_EXT_PA_LNA_CTRL

External TX PA and RX LNA control

Address: 0x403DF078

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	RW	RW	RW	None
HW Access	None		R	R	R	R	R	None
Name	None [7:6]		OUT-_EN_DRIVE_VAL	LNA_C-TRL_POL	PA_C-TRL_POL	CHIP_EN_POL	EN-ABLE_EX-T_PA_LNA	None

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	OUT_EN_DRIVE_VAL	Configures the drive value on the output enables of PA, LNA and CHI_EN signals 0 - drive 0 on the output enable signals 1 - drive 1 on the output enable signals Default Value: 0
4	LNA_CTRL_POL	Controls the polarity of the LNA control signal 0 - High enable, low disable 1 - Low enable, High disable Default Value: 0
3	PA_CTRL_POL	Controls the polarity of the PA control signal 0 - High enable, low disable 1 - Low enable, High disable Default Value: 0
2	CHIP_EN_POL	Controls the polarity of the chip enable control signal 0 - High enable, low disable 1 - Low enable, High disable Default Value: 0

22.1.231 BLE_BLESS_EXT_PA_LNA_CTRL (continued)

1	ENABLE_EXT_PA_LNA	When set to 1, enables the external PA & LNA Default Value: 0

22.1.232 BLE_BLESS_LL_PKT_RSSI_CH_ENERGY

Link Layer Last Received packet RSSI/Channel energy and channel number

Address: 0x403DF080

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	RSSI [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	RSSI [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None	R	R					
HW Access	None	W	W					
Name	None	PKT_RSSI_OR_CH_ENERGY	RX_CHANNEL [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
22	PKT_RSSI_OR_CH_ENERGY	This field indicates if the captured RSSI is for a received packet or is the channel energy Default Value: 0
21 : 16	RX_CHANNEL	This field indicates the last channel for which the RSSI is captured Default Value: 0
15 : 0	RSSI	This field captures the RSSI of the packet when a packet reception is complete or gives the Channel energy when a Receive cycle is over without packet reception. Default Value: 0

22.1.233 BLE_BLESS_BT_CLOCK_CAPT

BT clock captured on an LL DSM exit

Address: 0x403DF084

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	BT_CLOCK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	BT_CLOCK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	BT_CLOCK	This field captures the LF BT clock captured on an LL DSM exit. This register is valid only when MT_STATUS.LL_CLK_STATE is set. This value may be used to manage the low power entry. Default Value: 0

22.1.234 BLE_BLESS_MT_CFG

MT Configuration Register

Address: 0x403DF0A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW1S	RW	RW
HW Access	R	R	R	R	R	RW1C	R	R
Name	ACT_REG-ULA-TOR_EN	OVER-RIDE_ACT_REGULA-TOR	HVLDO_BYPASS	OVER-RIDE_H-VLDO_BYPASS	ACT_LDO_NOT_BUCK	DEEPS-LEEP_EX-ITED	DEEPS-LEEP_EX-IT_CFG	EN-ABLE_BLE-RD

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	LL_-CLK_EN	OVER-RIDE_LL_-CLK_EN	ISOLATE_N	OVER-RIDE_ISO-LATE	RET_SWITCH	OVER-RIDE_RET_SWITCH	DIG_REG-ULA-TOR_EN	OVER-RIDE_DIG_REGULA-TOR

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	OVER-RIDE_-CLK_EN	XTAL_EN	OVER-RIDE_X-TAL_EN	RESET_N	OVER-RIDE_RE-SET_N	DPS-LP_ECO_ON	HVLDO_EN	OVER-RIDE_H-VLDO_EN

Bits	31	30	29	28	27	26	25	24
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [31:28]				HVLDO_POR_HV	RET_LDO_OL	OVER-RIDE_RET_LDO_OL	BLERD_-CLK_EN

Bits	Name	Description
27	HVLDO_POR_HV	Reset for HVLDO 1'b1 - HVLDO Disabled 1'b0 - HVLDO Enabled Default Value: 1
26	RET_LDO_OL	Overrie value for CYBLERD55 RET_LDO_OL_HV Default Value: 0
25	OVER-RIDE_RET_LDO_OL	This register should be set to override the HW generated RET_LDO_OL_HV to CYBLERD55. When set CLK_EN is used. Default Value: 0

22.1.234 BLE_BLESS_MT_CFG (continued)

24	BLERD_CLK_EN	Overrie value for CYBLERD55 CLK_EN Default Value: 0
23	OVERRIDE_CLK_EN	This register should be set to override the HW generated CLK_EN to CYBLERD55. When set CLK_EN is used. Default Value: 0
22	XTAL_EN	Overrie value for CYBLERD55 XTAL_EN Default Value: 0
21	OVERRIDE_XTAL_EN	This register should be set to override the HW generated XTAL_EN to CYBLERD55. When set XTAL_EN is used. Default Value: 0
20	RESET_N	Overrie value for CYBLERD55 RESET_N Default Value: 1
19	OVERRIDE_RESET_N	This register should be set to override the HW generated reset to CYBLERD55. When set RE-SET_N is used. Default Value: 0
18	DPSLP_ECO_ON	This bit when set indicates that ECO clock should be kept on even in BLESS DPSLP. This bit must be toggled only when the Link Layer is active. Default Value: 0
17	HVLDO_EN	Overrie value for HVLDO enable 1'b1: switch to Active LDO 1'b0: switch to standby LDO Default Value: 0
16	OVERRIDE_HVLDO_EN	This register should be set to override the HW generated enable to HVLSO. When set HVLDO_EN is used. Default Value: 0
15	LL_CLK_EN	Override value for LL Clock gate Default Value: 0
14	OVERRIDE_LL_CLK_EN	This register should be set to override the HW generated ECO Clock gate. When set LL_-CLK_EN is used to gate the clock Default Value: 0
13	ISOLATE_N	Override value for isolation to CYBLERD55 Default Value: 0
12	OVERRIDE_ISOLATE	This register should be set to override the HW generated isolation signal to CYBLERD55. When set ISOLATE_N is driven to the IP Default Value: 0
11	RET_SWITCH	Override value for RET_SWITCH Default Value: 0
10	OVER-RIDE_RET_SWITCH	This register should be set to override the HW generated signal to the retention switch of CY-BLERD55. When set OVERRIDE_RET_SWITCH is driven to the IP Default Value: 0
9	DIG_REGULATOR_EN	Override value for digital regulator of CYBLERD55 Default Value: 0
8	OVERRIDE_DIG_REGU-LATOR	This register should be set to override the HW generated signal to Digital regulator of CYBLE-RD55. When set DIG_REGULATOR_EN is driven to CYBLERD55 Default Value: 0
7	ACT_REGULATOR_EN	Override value for ACT_LDO_EN/BUCK_EN Default Value: 0

22.1.234 BLE_BLESS_MT_CFG (continued)

6	OVERRIDE_ACT_REGU-LATOR	This register should be set to override the HW generated signal to enable ACTIVE_LDO/BUCK. When set ACT_REGULATOR_EN is driven to CYBLERD55 Default Value: 0
5	HVLDO_BYPASS	Override value for HVLDO BYPASS 1'b0: bypass the HVLDO 1'b1: Do not bypass the HVLDO Default Value: 0
4	OVERRIDE_HVLDO_BY-PASS	This register should be set to override the HW generated signal to HVLDO. When set HVLDO_BYPASS is driven to the IP Default Value: 0
3	ACT_LDO_NOT_BUCK	This register bit specifies whether the Active LDO or BUCK in CYBLERD55 is used in active mode Default Value: 0
2	DEEPSLEEP_EXITED	This register bit is used by FW to indicate that PSoC is out of DeepSleep 1'b0 - PSoC in DeepSleep 1'b1 - PSoC out of DeepSleep This bit is cleared by HW on exit from DPSLP Default Value: 0
1	DEEPSLEEP_EXIT_CFG	This register bit indicates the source for PSoC DeepSleep exit to BLESS 1'b0 - act_power_good from SRSS indicates PSoC DeepSleep exit 1'b1 - MT_CFG.DEEPSLEEP_EXITED indicates PSoC DeepSleep exit Default Value: 0
0	ENABLE_BLERD	This register bit needs to be set to enable CYBLERD55 1'b1 - CYBLERD55 enabled 1'b0 - CYBLERD55 disabled On power up this bit needs to be set to make CYBLERD55 active. Default Value: 0

22.1.235 BLE_BLESS_MT_DELAY_CFG

MT Delay configuration for state transitions

Address: 0x403DF0A4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HVLDO_STARTUP_DELAY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	ISOLATE_DEASSERT_DELAY [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	ACT_TO_SWITCH_DELAY [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	HVLDO_DISABLE_DELAY [31:24]							

Bits	Name	Description
31 : 24	HVLDO_DISABLE_DE-LAY	This register specifies the time from disabling XTAL to switching of the HVLDO. Default Value: 0
23 : 16	ACT_TO_SWITCH_DE-LAY	This register specifies the time from assertion of ISOLATE_N to switching the CYBLERD55 logic to Retention LDO Default Value: 0
15 : 8	ISOLATE_DEAS-SERT_DELAY	This register specifies the time from switching the CYBLERD55 logic to Active regulator to re-moval of ISOLATE_N Default Value: 0
7 : 0	HVLDO_STARTUP_DE-LAY	This register specifies the startup delay for the HVLDO interms of number of LF Clock cycles. FW has to program this register based on the selected LF clock frequency Default Value: 0

22.1.236 BLE_BLESS_MT_DELAY_CFG2

MT Delay configuration for state transitions

Address: 0x403DF0A8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	OSC_STARTUP_DELAY_LF [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DSM_OFFSET_TO_WAKEUP_INSTANT_LF [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	ACT_STARTUP_DELAY [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	DIG_LDO_STARTUP_DELAY [31:24]							

Bits	Name	Description
31 : 24	DIG_LDO_STARTUP_DELAY	This register specifes the Digital LDO startup time in CYBLERD55.The delay is in terms of LF Clock cycles. FW has to program this register based on the selected LF clock frequency. The logic in CYBLERD55 is switched to Active mode Regulator after this (ACT_STARTUP_DELAY + DIG_LDO_STARTUP_DELAY) Default Value: 0
23 : 16	ACT_STARTUP_DELAY	This register specifes the Active Regulator startup time in CYBLERD55. The delay is in terms of LF Clock cycles. FW has to program this register based on the selected LF clock frequency. The digital LDO will be turned on after this time elapses Default Value: 0
15 : 8	DSM_OFFSET_TO_WAKEUP_INSTANT_LF	This register specifies the pre-processing time required in Link Layer. This is esentially the time from CLK_EN (ungating clock in CYBLERD55) to the time when logic in CYBLERD55 is switched to Active mode Regulator.The delay is in terms of LF Clock cycles. FW has to program this register based on the selected LF clock frequency. This is equivalent to Link Layer register WAKEUP_CONFIG.DSM_OFFSET_TO_WAKEUP_INSTANT_LF, but is specified in LF cycles. Default Value: 0

22.1.236 BLE_BLESS_MT_DELAY_CFG2 (continued)

7 : 0	OSC_STARTUP_DE-LAY_LF	This register specifies the time for OSC Startup. After this delay, clock is enabled to the link layer. Clock is enabled after OSC_STARTUP_DELAY + 1 LF clock cycles. If PSoC was in DPSLP when XTAL is enabled, then the wakeup delay will be OSC_STARTUP_DELAY + 1 + PSoC Wakeup time. Minimum value to be programmed in 1. This is equivalent to Link Layer register WAKEUP_CONFIG.OSC_STARTUP_DELAY, but is specified in LF cycles Default Value: 0

22.1.237 BLE_BLESS_MT_DELAY_CFG3

MT Delay configuration for state transitions

Address: 0x403DF0AC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	XTAL_DISABLE_DELAY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DIG_LDO_DISABLE_DELAY [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VDDR_STABLE_DELAY [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	VDDR_STABLE_DELAY	This field holds the delay after HVLDO Startup to VDDR Stable. Refer to memo AKK-410 Default Value: 0
15 : 8	DIG_LDO_DISABLE_DE-LAY	This field holds the delay from the time of diabling Digital LDO to the time at which ACTIVE reg-ulator is disabled Default Value: 0
7 : 0	XTAL_DISABLE_DELAY	This register specifies the time from switching of logic to Retention LDO in CYBLERD55 to XTAL Disable. This should include the post processing time The delay is in terms of LF Clock cycles. FW has to program this register based on the selected LF clock frequency. At the minimum XTAL_DISABLE_DELAY should be the sum of DIG_LDO_DISABLE_DELAY and the powerdown time of ACTIVE_LDO Default Value: 0

22.1.238 BLE_BLESS_MT_VIO_CTRL

MT Configuration Register to control VIO switches

Address: 0x403DF0B0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						SRSS_SWITCH_EN_DLY	SRSS_SWITCH_EN

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	SRSS_SWITCH_EN_DLY	Enable to turn on HVLDO (All legs). This must be enabled 64us after enabling SRSS_SWITCH_EN 1'b0 - Switch is turned off 1'b1 - Switch is turned on Default Value: 0
0	SRSS_SWITCH_EN	Enable to turn on HVLDO (One leg) 1'b0 - Switch is turned off 1'b1 - Switch is turned on Default Value: 0

22.1.239 BLE_BLESS_MT_STATUS

MT Status Register

Address: 0x403DF0B4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R			R				R
HW Access	RW			RW				RW
Name	HVLDO_STARTUP_CURR_STATE [7:5]			MT_CURR_STATE [4:1]				BLESS-_STATE

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							RW
Name	None [15:9]							LL_-CLK_STATE

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	LL_CLK_STATE	This bit indicates when the Link Layer registers are accessible upon a DSM exit. This bit should not be used after a DSM entry command has been issued. 1'b0 - Link Layer clock is not available 1'b1 - Link Layer clock is active Default Value: 0
7 : 5	HVLDO_STARTUP_CUR-R_STATE	This register reflects the current state of the HVLDO Startup FSM 3'h0 - HVLDO_OFF 3'h1 - HVLDO_WAIT 3'h2 - HVLDO_SAMPLE 3'h3 - HVLDO_ENABLED 3'h4 - HVLDO_SET_BYPASS Default Value: 0

22.1.239 BLE_BLESS_MT_STATUS (continued)

4 : 1	MT_CURR_STATE	This register reflects the current state of the MT FSM 4'h0 - IDLE 4'h1 - BLERD_DEEPSLEEP 4'h2 - HVLDO_STARTUP 4'h3 - WAIT_CLK 4'h4 - BLERD_IDLE 4'h5 - SWITCH_EN 4'h6 - ACTIVE 4'h7 - ISOLATE 4'h8 - WAIT_IDLE 4'h9 - XTAL_DISABLE 4'hA - HVLDO_DISABLE Default Value: 0
0	BLESS_STATE	1'b0 - BLESS in DPSLP state 1'b1 - BLESS in ACTIVE state Default Value: 0

22.1.240 BLE_BLESS_PWR_CTRL_SM_ST

Link Layer Power Control FSM Status Register

Address: 0x403DF0B8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R			
HW Access	None				RW			
Name	None [7:4]				PWR_CTRL_SM_CURR_STATE [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	PWR_CTRL_SM_CUR-R_STATE	This register reflects the current state of the LL Power Control FSM 4'h0 - IDLE 4'h1 - SLEEP 4'h2 - DEEP_SLEEP 4'h4 - WAIT_OSC_STABLE 4'h5 - INTR_GEN 4'h6 - ACTIVE 4'h7 - REQ_RF_OFF Default Value: 0

22.1.241 BLE_BLESS_HVLDO_CTRL

HVLDO Configuration register

Address: 0x403DF0C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	None	RW				RW
HW Access	None	R	None	R				R
Name	None	VREF_EXT_EN	None	ADFT_CTRL [4:1]				ADFT_EN

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	RW	None						
Name	STATUS	None [30:24]						

Bits	Name	Description
31	STATUS	hvldo LV detect status Default Value: 0
6	VREF_EXT_EN	Vref ext input enable. Default Value: 0
4 : 1	ADFT_CTRL	ADFT select Default Value: 0
0	ADFT_EN	ADFT enable Default Value: 0

22.1.242 BLE_BLESS_MISC_EN_CTRL

Radio Buck and Active regulator enable control

Address: 0x403DF0C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [7:5]			LPM_EN-TRY_C-TRL_MODE	LP-M_DRIFT_-MULTI	LP-M_DRIFT_EN	ACT_REG_EN_CTRL	BUCK_EN_CTRL

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4	LPM_ENTRY_CTRL_-MODE	Controls the LPM entry control mode 1 - LPM can be entered in the same slot as the previous LPM exit 0 - LPM must not be entered in the same slot or the subsequent slot as the last LPM exit Default Value: 0
3	LPM_DRIFT_MULTI	Controls the LPM drift multi level compensation. 1 - Enables the LPM drift multi comp 0 - Disables the LPM drift multi comp Default Value: 1
2	LPM_DRIFT_EN	Controls the LPM drift calculation. 1 - Enables the LPM drift mod 0 - Disables the LPM drift mod Default Value: 0
1	ACT_REG_EN_CTRL	Active regulator enable control. This must be programmed before enabling the Radio. 1'b0 - Active regulator enable output to radio is tied to 0 1'b1 - Active regulator enable output to radio is controlled from Mode transition FSM Default Value: 0

22.1.242 BLE_BLESS_MISC_EN_CTRL (continued)

0	BUCK_EN_CTRL	Buck enable control. This must be programmed before enabling the Radio. 1'b1 - Buck enable output to radio is tied to 0 1'b0 - Buck enable output to radio is controlled from Mode transition FSM Default Value: 0

22.1.243 BLE_BLESS_EFUSE_CONFIG

EFUSE mode configuration register

Address: 0x403DF0D0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW1S	RW1S	RW
HW Access	None					RW1C	RW1C	R
Name	None [7:3]					EFUSE_WRITE	EFUSE_READ	EFUSE_MODE

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	EFUSE_WRITE	This bit when set by firmware enables the write to EFUSE macro. It is cleared when the efuse write is completed Default Value: 0
1	EFUSE_READ	This bit when set by firmware enables the read from EFUSE macro. It is cleared when the efuse read is completed Default Value: 0
0	EFUSE_MODE	This register enables the efuse mode Default Value: 0

22.1.244 BLE_BLESS_EFUSE_TIM_CTRL1

EFUSE timing control register (common for Program and Read modes)

Address: 0x403DF0D4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SCLK_HIGH [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	SCLK_LOW [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW			
HW Access	R				R			
Name	CS_SCLK_HOLD_TIME [23:20]				CS_SCLK_SETUP_TIME [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	R				R			
Name	RW_CS_HOLD_TIME [31:28]				RW_CS_SETUP_TIME [27:24]			

Bits	Name	Description
31 : 28	RW_CS_HOLD_TIME	This field decides hold time between RW & CS (THR_RW: in read mode) or RW & AVDD (THP_RW: in Program mode). THR_RW: RW to CS hold time out of Read mode THP_RW: RW to AVDD hold time out of program mode Default Value: 1
27 : 24	RW_CS_SETUP_TIME	This field decides setup time between RW & CS (TSR_RW: in read mode) or RW & AVDD (TSP_RW: in Program mode). TSR_RW: RW to CS setup time into Read mode TSP_RW: RW to AVDD setup time into program mode Default Value: 1
23 : 20	CS_SCLK_HOLD_TIME	This register specifies the hold time between CS and SCLK (THR_CLK) Default Value: 1
19 : 16	CS_SCLK_SETUP_TIME	This register specifies the setup time between CS and SCLK (TSR_CLK) Default Value: 2
15 : 8	SCLK_LOW	Duration of SCLK LOW (TCLKP_R) or TCKLP_P Default Value: 1

22.1.244 BLE_BLESS_EFUSE_TIM_CTRL1 (continued)

7 : 0	SCLK_HIGH	Decides the duration of TPGM (in Program mode) or TCKHP (in Read mode) TPGM: Burning Time TCKHP : SCLK high Period Default Value: 192

22.1.245 BLE_BLESS_EFUSE_TIM_CTRL2

EFUSE timing control Register (for Read)

Address: 0x403DF0D8

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA_SAMPLE_TIME [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				DOUT_CS_HOLD_TIME [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11 : 8	DOUT_CS_HOLD_TIME	Wait time DOUT to CS hold time out of read mode (TDQH) Default Value: 1
7 : 0	DATA_SAMPLE_TIME	This register specifies the time for data sampling from SCLK HIGH (TCKDQ_H) Default Value: 2

22.1.246 BLE_BLESS_EFUSE_TIM_CTRL3

EFUSE timing control Register (for Program)

Address: 0x403DF0DC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PGM_SCLK_HOLD_TIME [7:4]				PGM_SCLK_SETUP_TIME [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	AVDD_CS_SETUP_TIME [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	AVDD_CS_HOLD_TIME [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	AVDD_CS_HOLD_TIME	AVDD to CS hold time out of program mode (THP_AVDD_CS) Default Value: 58
15 : 8	AVDD_CS_SETUP_TIME	AVDD to CS setup time into program mode (TSP_AVDD_CS) Default Value: 58
7 : 4	PGM_SCLK_HOLD_TIME	PGM to SCLK hold time (TH_PGM) Default Value: 1
3 : 0	PGM_SCLK_SETUP_-TIME	PGM to SCLK setup time (TS_PGM) PGM_SCLK_SETUP_TIME _SCLK_SETUP_TIME Default Value: 1

22.1.247 BLE_BLESS_EFUSE_RDATA_L

EFUSE Lower read data

Address: 0x403DF0E0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	This register has the read value from the Efuse macro, fuse bits[31:0] Default Value: 0

22.1.248 BLE_BLESS_EFUSE_RDATA_H

EFUSE higher read data

Address: 0x403DF0E4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	This register has the read value from the Efuse macro, fuse bits[63:32] Default Value: 0

22.1.249 BLE_BLESS_EFUSE_WDATA_L

EFUSE lower write word

Address: 0x403DF0E8

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	This register has the write value to the Efuse macro, fuse bits[31:0] Default Value: 0

22.1.250 BLE_BLESS_EFUSE_WDATA_H

EFUSE higher write word

Address: 0x403DF0EC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	This register has the write value to the Efuse macro, fuse bits[63:32] Default Value: 0

22.1.251 BLE_BLESS_DIV_BY_625_CFG

Divide by 625 for FW Use

Address: 0x403DF0F0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	None
HW Access	None						R	None
Name	None [7:2]						ENABLE	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DIVIDEND [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DIVIDEND [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 8	DIVIDEND	This field holds the dividend Default Value: 0
1	ENABLE	This bit enables the divider for use by FW 1'b0 - divider used by LL 1'b1 - divider can be used by FW This divider can only be used in MMMS mode. Do not enable for legacy operation Default Value: 0

22.1.252 BLE_BLESS_DIV_BY_625_STS

Output of divide by 625 divider

Address: 0x403DF0F4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R					
HW Access	None		RW					
Name	None [7:6]		QUOTIENT [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	REMAINDER [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						R	
HW Access	None						RW	
Name	None [23:18]						REMAINDER [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
17 : 8	REMAINDER	Remainder value from the divider. Available 1 cycle after dividend is programmed. Default Value: 1
5 : 0	QUOTIENT	Quotient value from the divider. Available 1 cycle after dividend is programmed. Default Value: 0

22.1.253 BLE_BLESS_PACKET_COUNTER0

Packet counter 0

Address: 0x403DF100

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	PACKET_COUNTER_LOWER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	PACKET_COUNTER_LOWER [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	PACKET_COUNTER_LOWER [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	PACKET_COUNTER_LOWER [31:24]							

Bits	Name	Description
31 : 0	PACKET_COUNTER_LOWER	Lower 32-bits of the packet counter value passed as part of Nonce for the packet to be encrypted. Default Value: 0

22.1.254 BLE_BLESS_PACKET_COUNTER2

Packet counter 2

Address: 0x403DF104

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	PACKET_COUNTER_UPPER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	PACKET_COUNTER_UPPER	Upper 8 bits of the packet counter value passed as part of Nonce for the packet to be encrypted. Default Value: 0

22.1.255 BLE_BLESS_IV_MASTER0

Master Initialization Vector 0

Address: 0x403DF108

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	IV_MASTER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	IV_MASTER [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	IV_MASTER [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	IV_MASTER [31:24]							

Bits	Name	Description
31 : 0	IV_MASTER	This is the IVm field, which contains the masters portion of the initialization vector. Default Value: 0

22.1.256 BLE_BLESS_IV_SLAVE0

Slave Initialization Vector 0

Address: 0x403DF10C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	IV_SLAVE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	IV_SLAVE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	IV_SLAVE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	IV_SLAVE [31:24]							

Bits	Name	Description
31 : 0	IV_SLAVE	This is the IVs field, which contains the slaves portion of the initialization vector. Default Value: 0

22.1.257 BLE_BLESS_ENC_KEY0

Encryption Key register 0-3

Address: 0x403DF110

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	ENC_KEY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	ENC_KEY [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	W							
HW Access	R							
Name	ENC_KEY [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	W							
HW Access	R							
Name	ENC_KEY [31:24]							

Bits	Name	Description
31 : 0	ENC_KEY	The encryption key / session key which is used in ECB encryption, CCM encryption and CCM decryption. Default Value: 0

22.1.258 BLE_BLESS_MIC_IN0

MIC input register

Address: 0x403DF120

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	MIC_IN [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	MIC_IN [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	MIC_IN [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	MIC_IN [31:24]							

Bits	Name	Description
31 : 0	MIC_IN	This is the MIC field used for CCM decryption. Default Value: 0

22.1.259 BLE_BLESS_MIC_OUT0

MIC output register

Address: 0x403DF124

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	MIC_OUT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	MIC_OUT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	MIC_OUT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	MIC_OUT [31:24]							

Bits	Name	Description
31 : 0	MIC_OUT	This is the MIC generated during CCM encryption. Default Value: 0

22.1.260 BLE_BLESS_ENC_PARAMS

Encryption Parameter register

Address: 0x403DF128

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW					RW	
HW Access	R	R					R	
Name	DIRECTION	PAYLOAD_LENGTH_LSB [6:2]					DATA_PDU_HEADER [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	RW		
HW Access	None				R	R		
Name	None [15:12]				MEM_LATENCY_HIDE	PAYLOAD_LENGTH_LSB_EXT [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	MEM_LATENCY_HIDE	Controls the encryption memory access mode. Valid only when DLE is enabled. 0 - The AES is idle while memory fetch/store in progress. 1- The AES is pipelined while memory fetch/store in progress. Default Value: 0
10 : 8	PAYLOAD_LENGTH_LSB_EXT	3 Most significant bits of the LS byte of the length of the input data. Valid only when DLE is enabled. When DLE is enabled total ENC payload length = {PAYLOAD_LENGTH_LSB_EXT, PAYLOAD_LENGTH_LSB} Default Value: 0
7	DIRECTION	The directionBit shall be set to 1 for Data Channel PDUs sent by the master and set to 0 for Data Channel PDUs sent by the slave. Default Value: 0
6 : 2	PAYLOAD_LENGTH_LSB	Length of the input data. Default Value: 0
1 : 0	DATA_PDU_HEADER	LLID of the packet. Default Value: 0

22.1.261 BLE_BLESS_ENC_CONFIG

Encryption Configuration

Address: 0x403DF12C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [7:3]					DEC_ENC	ECB_CCM	START_PROC

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	PAYLOAD_LENGTH_MSB [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	B0_FLAGS [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							RW
HW Access	None							R
Name	None [31:25]							AES_B0_DATA_OVERRIDE

Bits	Name	Description
24	AES_B0_DATA_OVERRIDE	Configuration to use B0 DATA provided by FW for CCM computation Default Value: 0
23 : 16	B0_FLAGS	LS byte of the input data when B0 needs to be completely configurable. Valid only when AES_B0_DATA_OVERRIDE is enabled. Default Value: 0
15 : 8	PAYLOAD_LENGTH_MSB	MS byte of the length of the input data when B0 needs to be completely configurable. Valid only when AES_B0_DATA_OVERRIDE is enabled. When AES_B0_DATA_OVERRIDE is enabled total ENC payload length = {PAYLOAD_LENGTH_MSB, PAYLOAD_LENGTH_MSB, PAYLOAD_LENGTH} Default Value: 0
2	DEC_ENC	Decryption/Encryption 0 - Encrypt 1 - Decrypt Default Value: 0

22.1.261 BLE_BLESS_ENC_CONFIG (continued)

1	ECB_CCM	0 - CCM 1 - ECB Default Value: 0
0	START_PROC	1 Start the AES processing Default Value: 0

22.1.262 BLE_BLESS_ENC_INTR_EN

Encryption Interrupt enable

Address: 0x403DF130

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [7:3]					CCM_PROC_IN-TR_EN	EC-B_PROC_INTR_EN	AUTH_-PASS_IN-TR_EN

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	CCM_PROC_INTR_EN	CCM processed interupt enable 0 - Disable 1 - Enable Default Value: 0
1	ECB_PROC_INTR_EN	ECB processed interrupt enable 0 - Disable 1 - Enable Default Value: 0
0	AUTH_PASS_INTR_EN	Authentication interrupt enable 0 - Disable 1 - Enable Default Value: 0

22.1.263 BLE_BLESS_ENC_INTR

Encryption Interrupt status and clear register

Address: 0x403DF134

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1S	RW1C	RW1C	RW1C
HW Access	None				RW1C	RW1S	RW1S	RW1S
Name	None [7:4]				IN_DATA_-CLEAR	CCM_PROC_INTR	EC-B_PROC_INTR	AUTH_-PASS_INTR

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	IN_DATA_CLEAR	Clears the input data. Used for Zero padding of encryption for less than block sized data. Default Value: 0
2	CCM_PROC_INTR	CCM processed interrupt. Writing 1 to this register clears the interrupt Default Value: 0
1	ECB_PROC_INTR	ECB processed interrupt. Writing 1 to this register clears the interrupt. Default Value: 0
0	AUTH_PASS_INTR	Authentication interrupt. 0x1- indicates MIC matched 0x0 indicated MIC mismatched Writing 1 to this register clears the interrupt. Default Value: 0

22.1.264 BLE_BLESS_B1_DATA_REG0

Programmable B1 Data register (0-3)

Address: 0x403DF140

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	B1_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	B1_DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	B1_DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	B1_DATA [31:24]							

Bits	Name	Description
31 : 0	B1_DATA	Programmable B1 Data register Default Value: 0

22.1.265 BLE_BLESS_ENC_MEM_BASE_ADDR

Encryption memory base address

Address: 0x403DF150

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ENC_MEM [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ENC_MEM [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ENC_MEM [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ENC_MEM [31:24]							

Bits	Name	Description
31 : 0	ENC_MEM	Data values written to Enc memory are written as 16-bit wide data. This memory is valid only if DLE is set. Default Value: 0

22.1.266 BLE_BLESS_TRIM_LDO_0

LDO Trim register 0

Address: 0x403DFF00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	ACT_LDO_ITAIL [7:4]				ACT_LDO_VREG [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	ACT_LDO_ITAIL	To trim the bias currents for all the active mode blocks Default Value: 5
3 : 0	ACT_LDO_VREG	To trim the regulated voltage in steps of 25mV typically Default Value: 8

22.1.267 BLE_BLESS_TRIM_LDO_1

LDO Trim register 1

Address: 0x403DFF04

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	SB_BGRES [7:4]				ACT_REF_BGR [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	SB_BGRES	To trim standby regulator reference voltage Default Value: 0
3 : 0	ACT_REF_BGR	To trim active regulator reference voltage Default Value: 8

22.1.268 BLE_BLESS_TRIM_LDO_2

LDO Trim register 2

Address: 0x403DFF08

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW		RW				
HW Access	None	R		R				
Name	None	SB_BMULT_NBIAS [6:5]		SB_BMULT_RES [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
6 : 5	SB_BMULT_NBIAS	To trim standby regulator beta-multiplier current Default Value: 3
4 : 0	SB_BMULT_RES	To trim standby regulator beta-multiplier current Default Value: 0

22.1.269 BLE_BLESS_TRIM_LDO_3

LDO Trim register 3

Address: 0x403DFF0C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW		RW				
HW Access	None	R		R				
Name	None	SLOPE_SB_BMULT [6:5]		LVDET [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
6 : 5	SLOPE_SB_BMULT	To trim standby regulator beta-multiplier temp-co slope Default Value: 0
4 : 0	LVDET	To trim the trip points of the LV-Detect block Default Value: 16

22.1.270 BLE_BLESS_TRIM_MXD0

MXD die Trim registers

Address: 0x403DFF10

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	MXD_TRIM_BITS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	MXD_TRIM_BITS	MXD trim bits Default Value: 0

22.1.271 BLE_BLESS_TRIM_LDO_4

LDO Trim register 4

Address: 0x403DFF30

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	T_LDO [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	T_LDO	To debug post layout or post silicon Default Value: 0

22.1.272 BLE_BLESS_TRIM_LDO_5

LDO Trim register 5

Address: 0x403DFF34

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	RESERVED [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	RESERVED	Default Value: 0

23 USB Registers

This section discusses the USB registers. It lists all the registers in mapping tables, in address order.

23.1 Register Details

Register	Address	Description
USBFS0_USBDEV_EP0_DR0	0x403F0000	Control End point EP0 Data Register
USBFS0_USBDEV_EP0_DR1	0x403F0004	Control End point EP0 Data Register. See USBFS0_USBDEV_EP0_DR0 for the details of bit fields.
USBFS0_USBDEV_EP0_DR2	0x403F0008	Control End point EP0 Data Register. See USBFS0_USBDEV_EP0_DR0 for the details of bit fields.
USBFS0_USBDEV_EP0_DR3	0x403F000C	Control End point EP0 Data Register. See USBFS0_USBDEV_EP0_DR0 for the details of bit fields.
USBFS0_USBDEV_EP0_DR4	0x403F0010	Control End point EP0 Data Register. See USBFS0_USBDEV_EP0_DR0 for the details of bit fields.
USBFS0_USBDEV_EP0_DR5	0x403F0014	Control End point EP0 Data Register. See USBFS0_USBDEV_EP0_DR0 for the details of bit fields.
USBFS0_USBDEV_EP0_DR6	0x403F0018	Control End point EP0 Data Register. See USBFS0_USBDEV_EP0_DR0 for the details of bit fields.
USBFS0_USBDEV_EP0_DR7	0x403F001C	Control End point EP0 Data Register. See USBFS0_USBDEV_EP0_DR0 for the details of bit fields.
USBFS0_USBDEV_CR0	0x403F0020	USB control 0 Register
USBFS0_USBDEV_CR1	0x403F0024	USB control 1 Register
USBFS0_USBDEV_SIE_EP_INT_EN	0x403F0028	USB SIE Data Endpoints Interrupt Enable Register
USBFS0_USBDEV_SIE_EP_INT_SR	0x403F002C	USB SIE Data Endpoint Interrupt Status
USBFS0_USBDEV_SIE_EP1_CNT0	0x403F0030	Non-control endpoint count register
USBFS0_USBDEV_SIE_EP1_CNT1	0x403F0034	Non-control endpoint count register
USBFS0_USBDEV_SIE_EP1_CR0	0x403F0038	Non-control endpoint's control Register
USBFS0_USBDEV_USBIO_CR0	0x403F0040	USBIO Control 0 Register
USBFS0_USBDEV_USBIO_CR2	0x403F0044	USBIO control 2 Register
USBFS0_USBDEV_USBIO_CR1	0x403F0048	USBIO control 1 Register
USBFS0_USBDEV_DYN_RECONFIG	0x403F0050	USB Dynamic reconfiguration register
USBFS0_USBDEV_SOF0	0x403F0060	Start Of Frame Register
USBFS0_USBDEV_SOF1	0x403F0064	Start Of Frame Register
USBFS0_USBDEV_SIE_EP2_CNT0	0x403F0070	Non-control endpoint count register. See USBFS0_USBDEV_SIE_EP1_CNT0 for the details of bit fields.
USBFS0_USBDEV_SIE_EP2_CNT1	0x403F0074	Non-control endpoint count register. See USBFS0_USBDEV_SIE_EP1_CNT1 for the details of bit fields.

Register	Address	Description
USBFS0_USBDEV_SIE_EP2_CR0	0x403F0078	Non-control endpoint's control Register. See USBFS0_USBDEV_SIE_EP1_CR0 for the details of bit fields.
USBFS0_USBDEV_OSCLK_DR0	0x403F0080	Oscillator lock data register 0
USBFS0_USBDEV_OSCLK_DR1	0x403F0084	Oscillator lock data register 1
USBFS0_USBDEV_EP0_CR	0x403F00A0	Endpoint0 control Register
USBFS0_USBDEV_EP0_CNT	0x403F00A4	Endpoint0 count Register
USBFS0_USBDEV_SIE_EP3_CNT0	0x403F00B0	Non-control endpoint count register. See USBFS0_USBDEV_SIE_EP1_CNT0 for the details of bit fields.
USBFS0_USBDEV_SIE_EP3_CNT1	0x403F00B4	Non-control endpoint count register. See USBFS0_USBDEV_SIE_EP1_CNT1 for the details of bit fields.
USBFS0_USBDEV_SIE_EP3_CR0	0x403F00B8	Non-control endpoint's control Register. See USBFS0_USBDEV_SIE_EP1_CR0 for the details of bit fields.
USBFS0_USBDEV_SIE_EP4_CNT0	0x403F00F0	Non-control endpoint count register. See USBFS0_USBDEV_SIE_EP1_CNT0 for the details of bit fields.
USBFS0_USBDEV_SIE_EP4_CNT1	0x403F00F4	Non-control endpoint count register. See USBFS0_USBDEV_SIE_EP1_CNT1 for the details of bit fields.
USBFS0_USBDEV_SIE_EP4_CR0	0x403F00F8	Non-control endpoint's control Register. See USBFS0_USBDEV_SIE_EP1_CR0 for the details of bit fields.
USBFS0_USBDEV_SIE_EP5_CNT0	0x403F0130	Non-control endpoint count register. See USBFS0_USBDEV_SIE_EP1_CNT0 for the details of bit fields.
USBFS0_USBDEV_SIE_EP5_CNT1	0x403F0134	Non-control endpoint count register. See USBFS0_USBDEV_SIE_EP1_CNT1 for the details of bit fields.
USBFS0_USBDEV_SIE_EP5_CR0	0x403F0138	Non-control endpoint's control Register. See USBFS0_USBDEV_SIE_EP1_CR0 for the details of bit fields.
USBFS0_USBDEV_SIE_EP6_CNT0	0x403F0170	Non-control endpoint count register. See USBFS0_USBDEV_SIE_EP1_CNT0 for the details of bit fields.
USBFS0_USBDEV_SIE_EP6_CNT1	0x403F0174	Non-control endpoint count register. See USBFS0_USBDEV_SIE_EP1_CNT1 for the details of bit fields.
USBFS0_USBDEV_SIE_EP6_CR0	0x403F0178	Non-control endpoint's control Register. See USBFS0_USBDEV_SIE_EP1_CR0 for the details of bit fields.
USBFS0_USBDEV_SIE_EP7_CNT0	0x403F01B0	Non-control endpoint count register. See USBFS0_USBDEV_SIE_EP1_CNT0 for the details of bit fields.
USBFS0_USBDEV_SIE_EP7_CNT1	0x403F01B4	Non-control endpoint count register. See USBFS0_USBDEV_SIE_EP1_CNT1 for the details of bit fields.
USBFS0_USBDEV_SIE_EP7_CR0	0x403F01B8	Non-control endpoint's control Register. See USBFS0_USBDEV_SIE_EP1_CR0 for the details of bit fields.
USBFS0_USBDEV_SIE_EP8_CNT0	0x403F01F0	Non-control endpoint count register. See USBFS0_USBDEV_SIE_EP1_CNT0 for the details of bit fields.
USBFS0_USBDEV_SIE_EP8_CNT1	0x403F01F4	Non-control endpoint count register. See USBFS0_USBDEV_SIE_EP1_CNT1 for the details of bit fields.
USBFS0_USBDEV_SIE_EP8_CR0	0x403F01F8	Non-control endpoint's control Register. See USBFS0_USBDEV_SIE_EP1_CR0 for the details of bit fields.
USBFS0_USBDEV_ARB_EP1_CFG	0x403F0200	Endpoint Configuration Register *1
USBFS0_USBDEV_ARB_EP1_INT_EN	0x403F0204	Endpoint Interrupt Enable Register *1
USBFS0_USBDEV_ARB_EP1_SR	0x403F0208	Endpoint Interrupt Enable Register *1
USBFS0_USBDEV_ARB_RW1_WA	0x403F0210	Endpoint Write Address value *1, *2
USBFS0_USBDEV_ARB_RW1_WA_MSB	0x403F0214	Endpoint Write Address value *1, *2
USBFS0_USBDEV_ARB_RW1_RA	0x403F0218	Endpoint Read Address value *1, *2
USBFS0_USBDEV_ARB_RW1_RA_MSB	0x403F021C	Endpoint Read Address value *1, *2

Register	Address	Description
USBFS0_USBDEV_ARB_RW1_DR	0x403F0220	Endpoint Data Register
USBFS0_USBDEV_BUF_SIZE	0x403F0230	Dedicated Endpoint Buffer Size Register *1
USBFS0_USBDEV_EP_ACTIVE	0x403F0238	Endpoint Active Indication Register *1
USBFS0_USBDEV_EP_TYPE	0x403F023C	Endpoint Type (IN/OUT) Indication *1
USBFS0_USBDEV_ARB_EP2_CFG	0x403F0240	Endpoint Configuration Register *1. See USBFS0_USBDEV_ARB_EP1_CFG for the details of bit fields.
USBFS0_USBDEV_ARB_EP2_INT_EN	0x403F0244	Endpoint Interrupt Enable Register *1. See USBFS0_USBDEV_ARB_EP1_INT_EN for the details of bit fields.
USBFS0_USBDEV_ARB_EP2_SR	0x403F0248	Endpoint Interrupt Enable Register *1. See USBFS0_USBDEV_ARB_EP1_SR for the details of bit fields.
USBFS0_USBDEV_ARB_RW2_WA	0x403F0250	Endpoint Write Address value *1, *2. See USBFS0_USBDEV_ARB_RW1_WA for the details of bit fields.
USBFS0_USBDEV_ARB_RW2_WA_MSB	0x403F0254	Endpoint Write Address value *1, *2. See USBFS0_USBDEV_ARB_RW1_WA_MSB for the details of bit fields.
USBFS0_USBDEV_ARB_RW2_RA	0x403F0258	Endpoint Read Address value *1, *2. See USBFS0_USBDEV_ARB_RW1_RA for the details of bit fields.
USBFS0_USBDEV_ARB_RW2_RA_MSB	0x403F025C	Endpoint Read Address value *1, *2. See USBFS0_USBDEV_ARB_RW1_RA_MSB for the details of bit fields.
USBFS0_USBDEV_ARB_RW2_DR	0x403F0260	Endpoint Data Register. See USBFS0_USBDEV_ARB_RW1_DR for the details of bit fields.
USBFS0_USBDEV_ARB_CFG	0x403F0270	Arbiter Configuration Register *1
USBFS0_USBDEV_USB_CLK_EN	0x403F0274	USB Block Clock Enable Register
USBFS0_USBDEV_ARB_INT_EN	0x403F0278	Arbiter Interrupt Enable *1
USBFS0_USBDEV_ARB_INT_SR	0x403F027C	Arbiter Interrupt Status *1
USBFS0_USBDEV_ARB_EP3_CFG	0x403F0280	Endpoint Configuration Register *1. See USBFS0_USBDEV_ARB_EP1_CFG for the details of bit fields.
USBFS0_USBDEV_ARB_EP3_INT_EN	0x403F0284	Endpoint Interrupt Enable Register *1. See USBFS0_USBDEV_ARB_EP1_INT_EN for the details of bit fields.
USBFS0_USBDEV_ARB_EP3_SR	0x403F0288	Endpoint Interrupt Enable Register *1. See USBFS0_USBDEV_ARB_EP1_SR for the details of bit fields.
USBFS0_USBDEV_ARB_RW3_WA	0x403F0290	Endpoint Write Address value *1, *2. See USBFS0_USBDEV_ARB_RW1_WA for the details of bit fields.
USBFS0_USBDEV_ARB_RW3_WA_MSB	0x403F0294	Endpoint Write Address value *1, *2. See USBFS0_USBDEV_ARB_RW1_WA_MSB for the details of bit fields.
USBFS0_USBDEV_ARB_RW3_RA	0x403F0298	Endpoint Read Address value *1, *2. See USBFS0_USBDEV_ARB_RW1_RA for the details of bit fields.
USBFS0_USBDEV_ARB_RW3_RA_MSB	0x403F029C	Endpoint Read Address value *1, *2. See USBFS0_USBDEV_ARB_RW1_RA_MSB for the details of bit fields.
USBFS0_USBDEV_ARB_RW3_DR	0x403F02A0	Endpoint Data Register. See USBFS0_USBDEV_ARB_RW1_DR for the details of bit fields.
USBFS0_USBDEV_CWA	0x403F02B0	Common Area Write Address *1
USBFS0_USBDEV_CWA_MSB	0x403F02B4	Endpoint Read Address value *1
USBFS0_USBDEV_ARB_EP4_CFG	0x403F02C0	Endpoint Configuration Register *1. See USBFS0_USBDEV_ARB_EP1_CFG for the details of bit fields.
USBFS0_USBDEV_ARB_EP4_INT_EN	0x403F02C4	Endpoint Interrupt Enable Register *1. See USBFS0_USBDEV_ARB_EP1_INT_EN for the details of bit fields.
USBFS0_USBDEV_ARB_EP4_SR	0x403F02C8	Endpoint Interrupt Enable Register *1. See USBFS0_USBDEV_ARB_EP1_SR for the details of bit fields.

Register	Address	Description
USBFS0_USBDEV_ARB_RW4_WA	0x403F02D0	Endpoint Write Address value *1, *2. See USBFS0_USBDEV_ARB_RW1_WA for the details of bit fields.
USBFS0_USBDEV_ARB_RW4_WA_MSB	0x403F02D4	Endpoint Write Address value *1, *2. See USBFS0_USBDEV_ARB_RW1_WA_MSB for the details of bit fields.
USBFS0_USBDEV_ARB_RW4_RA	0x403F02D8	Endpoint Read Address value *1, *2. See USBFS0_USBDEV_ARB_RW1_RA for the details of bit fields.
USBFS0_USBDEV_ARB_RW4_RA_MSB	0x403F02DC	Endpoint Read Address value *1, *2. See USBFS0_USBDEV_ARB_RW1_RA_MSB for the details of bit fields.
USBFS0_USBDEV_ARB_RW4_DR	0x403F02E0	Endpoint Data Register. See USBFS0_USBDEV_ARB_RW1_DR for the details of bit fields.
USBFS0_USBDEV_DMA_THRES	0x403F02F0	DMA Burst / Threshold Configuration
USBFS0_USBDEV_DMA_THRES_MSB	0x403F02F4	DMA Burst / Threshold Configuration
USBFS0_USBDEV_ARB_EP5_CFG	0x403F0300	Endpoint Configuration Register *1. See USBFS0_USBDEV_ARB_EP1_CFG for the details of bit fields.
USBFS0_USBDEV_ARB_EP5_INT_EN	0x403F0304	Endpoint Interrupt Enable Register *1. See USBFS0_USBDEV_ARB_EP1_INT_EN for the details of bit fields.
USBFS0_USBDEV_ARB_EP5_SR	0x403F0308	Endpoint Interrupt Enable Register *1. See USBFS0_USBDEV_ARB_EP1_SR for the details of bit fields.
USBFS0_USBDEV_ARB_RW5_WA	0x403F0310	Endpoint Write Address value *1, *2. See USBFS0_USBDEV_ARB_RW1_WA for the details of bit fields.
USBFS0_USBDEV_ARB_RW5_WA_MSB	0x403F0314	Endpoint Write Address value *1, *2. See USBFS0_USBDEV_ARB_RW1_WA_MSB for the details of bit fields.
USBFS0_USBDEV_ARB_RW5_RA	0x403F0318	Endpoint Read Address value *1, *2. See USBFS0_USBDEV_ARB_RW1_RA for the details of bit fields.
USBFS0_USBDEV_ARB_RW5_RA_MSB	0x403F031C	Endpoint Read Address value *1, *2. See USBFS0_USBDEV_ARB_RW1_RA_MSB for the details of bit fields.
USBFS0_USBDEV_ARB_RW5_DR	0x403F0320	Endpoint Data Register. See USBFS0_USBDEV_ARB_RW1_DR for the details of bit fields.
USBFS0_USBDEV_BUS_RST_CNT	0x403F0330	Bus Reset Count Register
USBFS0_USBDEV_ARB_EP6_CFG	0x403F0340	Endpoint Configuration Register *1. See USBFS0_USBDEV_ARB_EP1_CFG for the details of bit fields.
USBFS0_USBDEV_ARB_EP6_INT_EN	0x403F0344	Endpoint Interrupt Enable Register *1. See USBFS0_USBDEV_ARB_EP1_INT_EN for the details of bit fields.
USBFS0_USBDEV_ARB_EP6_SR	0x403F0348	Endpoint Interrupt Enable Register *1. See USBFS0_USBDEV_ARB_EP1_SR for the details of bit fields.
USBFS0_USBDEV_ARB_RW6_WA	0x403F0350	Endpoint Write Address value *1, *2. See USBFS0_USBDEV_ARB_RW1_WA for the details of bit fields.
USBFS0_USBDEV_ARB_RW6_WA_MSB	0x403F0354	Endpoint Write Address value *1, *2. See USBFS0_USBDEV_ARB_RW1_WA_MSBfor the details of bit fields.
USBFS0_USBDEV_ARB_RW6_RA	0x403F0358	Endpoint Read Address value *1, *2. See USBFS0_USBDEV_ARB_RW1_RA for the details of bit fields.
USBFS0_USBDEV_ARB_RW6_RA_MSB	0x403F035C	Endpoint Read Address value *1, *2. See USBFS0_USBDEV_ARB_RW1_RA_MSB for the details of bit fields.
USBFS0_USBDEV_ARB_RW6_DR	0x403F0360	Endpoint Data Register. See USBFS0_USBDEV_ARB_RW1_DR for the details of bit fields.
USBFS0_USBDEV_ARB_EP7_CFG	0x403F0380	Endpoint Configuration Register *1. See USBFS0_USBDEV_ARB_EP1_CFG for the details of bit fields.
USBFS0_USBDEV_ARB_EP7_INT_EN	0x403F0384	Endpoint Interrupt Enable Register *1. See USBFS0_USBDEV_ARB_EP1_INT_EN for the details of bit fields.
USBFS0_USBDEV_ARB_EP7_SR	0x403F0388	Endpoint Interrupt Enable Register *1. See USBFS0_USBDEV_ARB_EP1_SR for the details of bit fields.
USBFS0_USBDEV_ARB_RW7_WA	0x403F0390	Endpoint Write Address value *1, *2. See USBFS0_USBDEV_ARB_RW1_WA for the details of bit fields.
USBFS0_USBDEV_ARB_RW7_WA_MSB	0x403F0394	Endpoint Write Address value *1, *2. See USBFS0_USBDEV_ARB_RW1_WA_MSB for the details of bit fields.

Register	Address	Description
USBFS0_USBDEV_ARB_RW7_RA	0x403F0398	Endpoint Read Address value *1, *2. See USBFS0_USBDEV_ARB_RW1_RA for the details of bit fields.
USBFS0_USBDEV_ARB_RW7_RA_MSB	0x403F039C	Endpoint Read Address value *1, *2. See USBFS0_USBDEV_ARB_RW1_RA_MSB for the details of bit fields.
USBFS0_USBDEV_ARB_RW7_DR	0x403F03A0	Endpoint Data Register. See USBFS0_USBDEV_ARB_RW1_DR for the details of bit fields.
USBFS0_USBDEV_ARB_EP8_CFG	0x403F03C0	Endpoint Configuration Register *1. See USBFS0_USBDEV_ARB_EP1_CFG for the details of bit fields.
USBFS0_USBDEV_ARB_EP8_INT_EN	0x403F03C4	Endpoint Interrupt Enable Register *1. See USBFS0_USBDEV_ARB_EP1_INT_EN for the details of bit fields.
USBFS0_USBDEV_ARB_EP8_SR	0x403F03C8	Endpoint Interrupt Enable Register *1. See USBFS0_USBDEV_ARB_EP1_SR for the details of bit fields.
USBFS0_USBDEV_ARB_RW8_WA	0x403F03D0	Endpoint Write Address value *1, *2. See USBFS0_USBDEV_ARB_RW1_WA for the details of bit fields.
USBFS0_USBDEV_ARB_RW8_WA_MSB	0x403F03D4	Endpoint Write Address value *1, *2. See USBFS0_USBDEV_ARB_RW1_WA_MSB for the details of bit fields.
USBFS0_USBDEV_ARB_RW8_RA	0x403F03D8	Endpoint Read Address value *1, *2. See USBFS0_USBDEV_ARB_RW1_RA for the details of bit fields.
USBFS0_USBDEV_ARB_RW8_RA_MSB	0x403F03DC	Endpoint Read Address value *1, *2. See USBFS0_USBDEV_ARB_RW1_RA_MSB for the details of bit fields.
USBFS0_USBDEV_ARB_RW8_DR	0x403F03E0	Endpoint Data Register. See USBFS0_USBDEV_ARB_RW1_DR for the details of bit fields.
USBFS0_USBDEV_MEM_DATA0	0x403F0400	DATA. This is the starting address of a register bank containing 512 registers (USBFS0_USBDEV_MEM_DATA0 to USBFS0_USBDEV_MEM_DATA511)
USBFS0_USBDEV_SOF16	0x403F1060	Start Of Frame Register
USBFS0_USBDEV_OSCLK_DR16	0x403F1080	Oscillator lock data register
USBFS0_USBDEV_ARB_RW1_WA16	0x403F1210	Endpoint Write Address value *3
USBFS0_USBDEV_ARB_RW1_RA16	0x403F1218	Endpoint Read Address value *3
USBFS0_USBDEV_ARB_RW1_DR16	0x403F1220	Endpoint Data Register
USBFS0_USBDEV_ARB_RW2_WA16	0x403F1250	Endpoint Write Address value *3. See USBFS0_USBDEV_ARB_RW1_WA16 for the details of bit fields.
USBFS0_USBDEV_ARB_RW2_RA16	0x403F1258	Endpoint Read Address value *3. See USBFS0_USBDEV_ARB_RW1_RA16 for the details of bit fields.
USBFS0_USBDEV_ARB_RW2_DR16	0x403F1260	Endpoint Data Register. See USBFS0_USBDEV_ARB_RW1_DR16 for the details of bit fields.
USBFS0_USBDEV_ARB_RW3_WA16	0x403F1290	Endpoint Write Address value *3. See USBFS0_USBDEV_ARB_RW1_WA16 for the details of bit fields.
USBFS0_USBDEV_ARB_RW3_RA16	0x403F1298	Endpoint Read Address value *3. See USBFS0_USBDEV_ARB_RW1_RA16 for the details of bit fields.
USBFS0_USBDEV_ARB_RW3_DR16	0x403F12A0	Endpoint Data Register. See USBFS0_USBDEV_ARB_RW1_DR16 for the details of bit fields.
USBFS0_USBDEV_CWA16	0x403F12B0	Common Area Write Address
USBFS0_USBDEV_ARB_RW4_WA16	0x403F12D0	Endpoint Write Address value *3. See USBFS0_USBDEV_ARB_RW1_WA16 for the details of bit fields.
USBFS0_USBDEV_ARB_RW4_RA16	0x403F12D8	Endpoint Read Address value *3. See USBFS0_USBDEV_ARB_RW1_RA16 for the details of bit fields.
USBFS0_USBDEV_ARB_RW4_DR16	0x403F12E0	Endpoint Data Register. See USBFS0_USBDEV_ARB_RW1_DR16 for the details of bit fields.
USBFS0_USBDEV_DMA_THRES16	0x403F12F0	DMA Burst / Threshold Configuration
USBFS0_USBDEV_ARB_RW5_WA16	0x403F1310	Endpoint Write Address value *3. See USBFS0_USBDEV_ARB_RW1_WA16 for the details of bit fields.

Register	Address	Description
USBFS0_USBDEV_ARB_RW5_RA16	0x403F1318	Endpoint Read Address value *3. See USBFS0_USBDEV_ARB_RW1_RA16 for the details of bit fields.
USBFS0_USBDEV_ARB_RW5_DR16	0x403F1320	Endpoint Data Register. See USBFS0_USBDEV_ARB_RW1_DR16 for the details of bit fields.
USBFS0_USBDEV_ARB_RW6_WA16	0x403F1350	Endpoint Write Address value *3. See USBFS0_USBDEV_ARB_RW1_WA16 for the details of bit fields.
USBFS0_USBDEV_ARB_RW6_RA16	0x403F1358	Endpoint Read Address value *3. See USBFS0_USBDEV_ARB_RW1_RA16 for the details of bit fields.
USBFS0_USBDEV_ARB_RW6_DR16	0x403F1360	Endpoint Data Register. See USBFS0_USBDEV_ARB_RW1_DR16 for the details of bit fields.
USBFS0_USBDEV_ARB_RW7_WA16	0x403F1390	Endpoint Write Address value *3. See USBFS0_USBDEV_ARB_RW1_WA16 for the details of bit fields.
USBFS0_USBDEV_ARB_RW7_RA16	0x403F1398	Endpoint Read Address value *3. See USBFS0_USBDEV_ARB_RW1_RA16 for the details of bit fields.
USBFS0_USBDEV_ARB_RW7_DR16	0x403F13A0	Endpoint Data Register. See USBFS0_USBDEV_ARB_RW1_DR16 for the details of bit fields.
USBFS0_USBDEV_ARB_RW8_WA16	0x403F13D0	Endpoint Write Address value *3. See USBFS0_USBDEV_ARB_RW1_WA16 for the details of bit fields.
USBFS0_USBDEV_ARB_RW8_RA16	0x403F13D8	Endpoint Read Address value *3. See USBFS0_USBDEV_ARB_RW1_RA16 for the details of bit fields.
USBFS0_USBDEV_ARB_RW8_DR16	0x403F13E0	Endpoint Data Register. See USBFS0_USBDEV_ARB_RW1_DR16 for the details of bit fields.
USBFS0_USBLPM_POWER_CTL	0x403F2000	Power Control Register
USBFS0_USBLPM_USBIO_CTL	0x403F2008	USB IO Control Register
USBFS0_USBLPM_FLOW_CTL	0x403F200C	Flow Control Register
USBFS0_USBLPM_LPM_CTL	0x403F2010	LPM Control Register
USBFS0_USBLPM_LPM_STAT	0x403F2014	LPM Status register
USBFS0_USBLPM_INTR_SIE	0x403F2020	USB SOF, BUS RESET and EP0 Interrupt Status
USBFS0_USBLPM_INTR_SIE_SET	0x403F2024	USB SOF, BUS RESET and EP0 Interrupt Set
USBFS0_USBLPM_INTR_SIE_MASK	0x403F2028	USB SOF, BUS RESET and EP0 Interrupt Mask
USBFS0_USBLPM_INTR_SIE_MASKED	0x403F202C	USB SOF, BUS RESET and EP0 Interrupt Masked
USBFS0_USBLPM_INTR_LVL_SEL	0x403F2030	Select interrupt level for each interrupt source
USBFS0_USBLPM_INTR_CAUSE_HI	0x403F2034	High priority interrupt Cause register
USBFS0_USBLPM_INTR_CAUSE_MED	0x403F2038	Medium priority interrupt Cause register
USBFS0_USBLPM_INTR_CAUSE_LO	0x403F203C	Low priority interrupt Cause register
USBFS0_USBLPM_DFT_CTL	0x403F2070	DFT control
USBFS0_USBHOST_HOST_CTL0	0x403F4000	Host Control 0 Register.
USBFS0_USBHOST_HOST_CTL1	0x403F4010	Host Control 1 Register.
USBFS0_USBHOST_HOST_CTL2	0x403F4100	Host Control 2 Register.
USBFS0_USBHOST_HOST_ERR	0x403F4104	Host Error Status Register.

Register	Address	Description
USBFS0_USBHOST_HOST_STATUS	0x403F4108	Host Status Register.
USBFS0_USBHOST_HOST_FCOMP	0x403F410C	Host SOF Interrupt Frame Compare Register
USBFS0_USBHOST_HOST_RTIMER	0x403F4110	Host Retry Timer Setup Register
USBFS0_USBHOST_HOST_ADDR	0x403F4114	Host Address Register
USBFS0_USBHOST_HOST_EOF	0x403F4118	Host EOF Setup Register
USBFS0_USBHOST_HOST_FRAME	0x403F411C	Host Frame Setup Register
USBFS0_USBHOST_HOST_TOKEN	0x403F4120	Host Token Endpoint Register
USBFS0_USBHOST_HOST_EP1_CTL	0x403F4400	Host Endpoint 1 Control Register
USBFS0_USBHOST_HOST_EP1_STATUS	0x403F4404	Host Endpoint 1 Status Register
USBFS0_USBHOST_HOST_EP1_RW1_DR	0x403F4408	Host Endpoint 1 Data 1-Byte Register
USBFS0_USBHOST_HOST_EP1_RW2_DR	0x403F440C	Host Endpoint 1 Data 2-Byte Register
USBFS0_USBHOST_HOST_EP2_CTL	0x403F4500	Host Endpoint 2 Control Register
USBFS0_USBHOST_HOST_EP2_STATUS	0x403F4504	Host Endpoint 2 Status Register
USBFS0_USBHOST_HOST_EP2_RW1_DR	0x403F4508	Host Endpoint 2 Data 1-Byte Register
USBFS0_USBHOST_HOST_EP2_RW2_DR	0x403F450C	Host Endpoint 2 Data 2-Byte Register
USBFS0_USBHOST_HOST_LVL1_SEL	0x403F4800	Host Interrupt Level 1 Selection Register
USBFS0_USBHOST_HOST_LVL2_SEL	0x403F4804	Host Interrupt Level 2 Selection Register
USBFS0_USBHOST_INTR_USBHOST_-CAUSE_HI	0x403F4900	Interrupt USB Host Cause High Register
USBFS0_USBHOST_INTR_USBHOST_-CAUSE_MED	0x403F4904	Interrupt USB Host Cause Medium Register
USBFS0_USBHOST_INTR_USBHOST_-CAUSE_LO	0x403F4908	Interrupt USB Host Cause Low Register
USBFS0_USBHOST_INTR_HOST_EP_-CAUSE_HI	0x403F4920	Interrupt USB Host Endpoint Cause High Register
USBFS0_USBHOST_INTR_HOST_EP_-CAUSE_MED	0x403F4924	Interrupt USB Host Endpoint Cause Medium Register
USBFS0_USBHOST_INTR_HOST_EP_-CAUSE_LO	0x403F4928	Interrupt USB Host Endpoint Cause Low Register
USBFS0_USBHOST_INTR_USBHOST	0x403F4940	Interrupt USB Host Register
USBFS0_USBHOST_INTR_USBHOST_SET	0x403F4944	Interrupt USB Host Set Register
USBFS0_USBHOST_INTR_USBHOST_MASK	0x403F4948	Interrupt USB Host Mask Register
USBFS0_USBHOST_INTR_USB-HOST_MASKED	0x403F494C	Interrupt USB Host Masked Register
USBFS0_USBHOST_INTR_HOST_EP	0x403F4A00	Interrupt USB Host Endpoint Register
USBFS0_USBHOST_INTR_HOST_EP_SET	0x403F4A04	Interrupt USB Host Endpoint Set Register

Register	Address	Description
USBFS0_USBHOST_INTR_HOST_EP_MASK	0x403F4A08	Interrupt USB Host Endpoint Mask Register
USBFS0_USBHOST_IN-TR_HOST_EP_MASKED	0x403F4A0C	Interrupt USB Host Endpoint Masked Register
USBFS0_USBHOST_HOST_DMA_ENBL	0x403F4B00	Host DMA Enable Register
USBFS0_USBHOST_HOST_EP1_BLK	0x403F4B20	Host Endpoint 1 Block Register
USBFS0_USBHOST_HOST_EP2_BLK	0x403F4B30	Host Endpoint 2 Block Register

23.1.1 USBFS0_USBDEV_EP0_DR0

Control End point EP0 Data Register

Address: 0x403F0000

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA_BYTE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA_BYTE	This register is shared for both transmit and receive. The count in the EP0_CNT register determines the number of bytes received or to be transferred. Default Value: 0

23.1.2 USBFS0_USBDEV_CR0

USB control 0 Register

Address: 0x403F0020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW						
HW Access	RW	RW						
Name	USB_EN-ABLE	DEVICE_ADDRESS [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	USB_ENABLE	This bit enables the device to respond to USB traffic. If USB bus reset is detected, this bit is cleared. Note: When USB PHY is GPIO mode(USBIO_CR1.IOMODE=0), USB bus reset is detected. Therefore, when USB PHY is GPIO mode, this bit is cleared even if this bit is set to 1. If this bit is set to 1, write this bit upon USB bus reset interrupt, and do not write to this bit during initialization steps. Default Value: 0
6 : 0	DEVICE_ADDRESS	These bits specify the USB device address to which the SIE will respond. This address must be set by firmware and is specified by the USB Host with a SET ADDRESS command during USB enumeration. This value must be programmed by firmware when assigned during enumeration. It is not set automatically by the hardware. If USB bus reset is detected, these bits are initialized. Default Value: 0

23.1.3 USBFS0_USBDEV_CR1

USB control 1 Register

Address: 0x403F0024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW0C	RW	RW
HW Access	None				R	RW1S	R	R
Name	None [7:4]				RE-SERVED_3	BUS_AC-TIVITY	EN-ABLE_LOCK	REG_EN-ABLE

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	RESERVED_3	Reserved Default Value: 0
2	BUS_ACTIVITY	The Bus Activity bit is a stickybit that detects any non-idle USB event that has occurred on the USB bus. Once set to High by the SIE to indicate the bus activity this bit retains its logical High value until firmware clears it. Default Value: 0
1	ENABLE_LOCK	This bit is set to turn on the automatic frequency locking of the internal oscillator to USB traffic. Unless an external clock is being provided this bit should remain set for proper USB operation. Default Value: 0
0	REG_ENABLE	This bit controls the operation of the internal USB regulator. For applications with supply voltages in the 5V range this bit is set high to enable the internal regulator. For device supply voltage in the 3.3V range this bit is cleared to connect the transceiver directly to the supply. Default Value: 0

23.1.4 USBFS0_USBDEV_SIE_EP_INT_EN

USB SIE Data Endpoints Interrupt Enable Register

Address: 0x403F0028

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	EP8_IN-TR_EN	EP7_IN-TR_EN	EP6_IN-TR_EN	EP5_IN-TR_EN	EP4_IN-TR_EN	EP3_IN-TR_EN	EP2_IN-TR_EN	EP1_IN-TR_EN

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	EP8_INTR_EN	Enables interrupt for EP8 Default Value: 0
6	EP7_INTR_EN	Enables interrupt for EP7 Default Value: 0
5	EP6_INTR_EN	Enables interrupt for EP6 Default Value: 0
4	EP5_INTR_EN	Enables interrupt for EP5 Default Value: 0
3	EP4_INTR_EN	Enables interrupt for EP4 Default Value: 0
2	EP3_INTR_EN	Enables interrupt for EP3 Default Value: 0
1	EP2_INTR_EN	Enables interrupt for EP2 Default Value: 0

23.1.4 USBFS0_USBDEV_SIE_EP_INT_EN (continued)

0	EP1_INTR_EN	Enables interrupt for EP1 Default Value: 0

23.1.5 USBFS0_USBDEV_SIE_EP_INT_SR

USB SIE Data Endpoint Interrupt Status

Address: 0x403F002C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
Name	EP8_INTR	EP7_INTR	EP6_INTR	EP5_INTR	EP4_INTR	EP3_INTR	EP2_INTR	EP1_INTR

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	EP8_INTR	Interrupt status for EP8 Default Value: 0
6	EP7_INTR	Interrupt status for EP7 Default Value: 0
5	EP6_INTR	Interrupt status for EP6 Default Value: 0
4	EP5_INTR	Interrupt status for EP5 Default Value: 0
3	EP4_INTR	Interrupt status for EP4 Default Value: 0
2	EP3_INTR	Interrupt status for EP3 Default Value: 0
1	EP2_INTR	Interrupt status for EP2 Default Value: 0
0	EP1_INTR	Interrupt status for EP1 Default Value: 0

23.1.6 USBFS0_USBDEV_SIE_EP1_CNT0

Non-control endpoint count register

Address: 0x403F0030

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW0C	None			RW		
HW Access	RW	RW1S	None			RW		
Name	DATA_-TOGGLE	DATA_VAL-ID	None [5:3]			DATA_COUNT_MSB [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	DATA_TOGGLE	This bit selects the DATA packet's toggle state. For IN transactions firmware must set this bit to the expected state. For OUT transactions the hardware sets this bit to the state of the received Data Toggle bit. Default Value: 0
6	DATA_VALID	This bit is used for OUT transactions only and is read only. It is cleared to '0' if CRC bit stuffing errors or PID errors occur. This bit does not update for some endpoint mode settings. Default Value: 0 **0x0: DATA_ERROR :** No ACK'd transactions since bit was last cleared. **0x1: DATA_VALID :** Indicates a transaction ended with an ACK.
2 : 0	DATA_COUNT_MSB	These bits are the 3 MSb bits of an 11-bit counter. The LSb are the Data Count[7:0] bits of the CNT1 register. Refer to the CNT1 register for more information. Default Value: 0

23.1.7 USBFS0_USBDEV_SIE_EP1_CNT1

Non-control endpoint count register

Address: 0x403F0034

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA_COUNT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA_COUNT	These bits are the 8 LSb of a 11-bit counter. The 3 MSb bits are in the CNT0 register. The 11-bit count indicates the number of data bytes in a transaction. Default Value: 0

23.1.8 USBFS0_USBDEV_SIE_EP1_CR0

Non-control endpoint's control Register

Address: 0x403F0038

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RWC	RW	RWC	RW			
HW Access	R	RW1S	R	RW1S	RW			
Name	STALL	ER-R_IN_TXN	NA-K_INT_EN	ACKED_TXN	MODE [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	STALL	When this bit is set the SIE stalls an OUT packet if the Mode bits are set to ACK-OUT. The SIE stalls an IN packet if the mode bits are set to ACK-IN. This bit must be clear for all other modes. Default Value: 0
6	ERR_IN_TXN	The Error in transaction bit is set whenever an error is detected. For an IN transaction, this indicates a no response from HOST scenario. For an OUT transaction, this represents an RxErr (PID error/ CRC error/ bit-stuff error scenario). This bit is cleared by any writes to the register. Default Value: 0
5	NAK_INT_EN	When set this bit causes an endpoint interrupt to be generated even when a transfer completes with a NAK. Default Value: 0
4	ACKED_TXN	The ACK'd transaction bit is set whenever the SIE engages in a transaction to the register's endpoint that completes with an ACK packet. This bit is cleared by any writes to the register. Default Value: 0 **0x0: ACKED_NO :** No ACK'd transactions since bit was last cleared.

23.1.8 USBFS0_USBDEV_SIE_EP1_CR0 (continued)

		0x1: ACKED_YES : Indicates a transaction ended with an ACK.
3 : 0	MODE	The mode controls how the USB SIE responds to traffic and how the USB SIE changes the mode of that endpoint as a result of host packets to the endpoint. Default Value: 0 **0x0: DISABLE :** Ignore all USB traffic to this endpoint **0x1: NAK_INOUT :** SETUP: Accept IN: NAK OUT: NAK **0x2: STATUS_OUT_ONLY :** SETUP: Accept IN: STALL OUT: ACK 0B tokens, NAK others **0x3: STALL_INOUT :** SETUP: Accept IN: STALL OUT: STALL **0x5: ISO_OUT :** SETUP: Ignore IN: Ignore OUT: Accept Isochronous OUT token **0x6: STATUS_IN_ONLY :** SETUP: Accept IN: Respond with 0B data OUT: Stall **0x7: ISO_IN :** SETUP: Ignore IN: Accept Isochronous IN token OUT: Ignore **0x8: NAK_OUT :** SETUP: Ignore IN: Ignore OUT: NAK

23.1.8 USBFS0_USBDEV_SIE_EP1_CR0 (continued)

0x9: ACK_OUT :

SETUP: Ignore
IN: Ignore
OUT: Accept data and ACK if STALL=0, STALL otherwise.
Change to MODE=8 after one succesfull OUT token.

0xb: ACK_OUT_STATUS_IN :

SETUP: Accept
IN: Respond with 0B data
OUT: Accept data

0xc: NAK_IN :

SETUP: Ignore
IN: NAK
OUT: Ignore

0xd: ACK_IN :

SETUP: Ignore
IN: Respond to IN with data if STALL=0, STALL otherwise
OUT: Ignore

0xf: ACK_IN_STATUS_OUT :

SETUP: Accept
IN: Respond to IN with data
OUT: ACK 0B tokens, NAK others

23.1.9 USBFS0_USBDEV_USBIO_CR0

USBIO Control 0 Register

Address: 0x403F0040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	None				R
HW Access	R	R	R	None				W
Name	TEN	TSE0	TD	None [4:1]				RD

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	TEN	USB Transmit Enable. This is used to manually transmit on the D+ and D- pins. Normally this bit should be cleared to allow the internal SIE to drive the pins. The most common reason for man-ually transmitting is to force a resume state on the bus. Default Value: 0
6	TSE0	Transmit Single-Ended Zero. SE0: both D+ and D- low. No effect if TEN=0. Default Value: 0
5	TD	Transmit Data. Transmit a USB J or K state on the USB bus. No effect if TEN=0 or TSE0=1. Default Value: 0 **0x0: DIFF_K :** Force USB K state (D+ is low D- is high). **0x1: DIFF_J :** Force USB J state (D+ is high D- is low).

23.1.9 USBFS0_USBDEV_USBIO_CR0 (continued)

0	RD	Received Data. This read only bit gives the state of the USB differential receiver when IOMODE bit is '0' and USB doesn't transmit. This bit is valid if USB Device. If D+=D- (SE0), this value is undefined. Default Value: X **0x0: DIFF_LOW :** D+ < D- (K state) **0x1: DIFF_HIGH :** D+ > D- (J state)

23.1.10 USBFS0_USBDEV_USBIO_CR2

USBIO control 2 Register

Address: 0x403F0044

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	R					
HW Access	R	R	R					
Name	RE-SERVED_7	TEST_PKT	RESERVED_5_0 [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	RESERVED_7	Reserved Default Value: 0
6	TEST_PKT	This bit enables the device to transmit a packet in response to an internally generated IN packet. When set, one packet will be generated. Default Value: 0
5 : 0	RESERVED_5_0	Reserved Default Value: 0

23.1.11 USBFS0_USBDEV_USBIO_CR1

USBIO control 1 Register

Address: 0x403F0048

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	None		RW	R	R
HW Access	None		R	None		W	W	W
Name	None [7:6]		IOMODE	None [4:3]		RE-SERVED_2	DPO	DMO

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	IOMODE	This bit allows the D+ and D- pins to be configured for either USB mode or bit-banged modes. If this bit is set the DMI and DPI bits are used to drive the D- and D+ pins. Default Value: 1
2	RESERVED_2	Reserved Default Value: X
1	DPO	This read only bit gives the state of the D+ pin when IOMODE bit is '0' and USB doesn't transmit. This bit displays the output value of D+ pin when USB transmits SE0 or data. This bit is valid if USB Device. Default Value: X
0	DMO	This read only bit gives the state of the D- pin when IOMODE bit is '0' and USB doesn't transmit. This bit is '0' when USB transmits SE0, and this bit is '1' when USB transmits other than SE0. This bit is valid if USB Device. Default Value: X

23.1.12 USBFS0_USBDEV_DYN_RECONFIG

USB Dynamic reconfiguration register

Address: 0x403F0050

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			R	RW			RW
HW Access	None			W	R			R
Name	None [7:5]			DYN_RE-CON-FIG_RDY_STS	DYN_RECONFIG_EPNO [3:1]			DYN_CON-FIG_EN

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4	DYN_RECON-FIG_RDY_STS	This bit indicates the ready status for the dynamic reconfiguration, when set to 1, indicates the block is ready for reconfiguration. Default Value: 0
3 : 1	DYN_RECONFIG_EPNO	These bits indicates the EP number for which reconfiguration is required when dyn_config_en bit is set to 1. Default Value: 0
0	DYN_CONFIG_EN	This bit is used to enable the dynamic re-configuration for the selected EP. If set to 1, indicates the reconfiguration required for selected EP. Use 0 for EP1, 1 for EP2, etc. Default Value: 0

23.1.13 USBFS0_USBDEV_SOF0

Start Of Frame Register

Address: 0x403F0060

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	FRAME_NUMBER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	FRAME_NUMBER	It has the lower 8 bits [7:0] of the SOF frame number. Default Value: 0

23.1.14 USBFS0_USBDEV_SOF1

Start Of Frame Register

Address: 0x403F0064

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					R		
HW Access	None					RW		
Name	None [7:3]					FRAME_NUMBER_MSB [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2 : 0	FRAME_NUMBER_MSB	It has the upper 3 bits [10:8] of the SOF frame number. Default Value: 0

23.1.15 USBFS0_USBDEV_OSCLK_DR0

Oscillator lock data register 0

Address: 0x403F0080

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	ADDER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	ADDER	These bits return the lower 8 bits of the oscillator locking circuits adder output. Default Value: X

23.1.16 USBFS0_USBDEV_OSCLK_DR1

Oscillator lock data register 1

Address: 0x403F0084

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	R						
HW Access	None	W						
Name	None	ADDER_MSB [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
6 : 0	ADDER_MSB	These bits return the upper 7 bits of the oscillator locking circuits adder output. Default Value: X

23.1.17 USBFS0_USBDEV_EP0_CR

Endpoint0 control Register

Address: 0x403F00A0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RWC	RWC	RWC	RWC	RW			
HW Access	RW1S	RW1S	RW1S	RW1S	RW			
Name	SET-UP_RCVD	IN_RCVD	OUT_RCVD	ACKED_TXN	MODE [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	SETUP_RCVD	When set this bit indicates a valid SETUP packet was received and ACKed. This bit is forced HIGH from the start of the data packet phase of the SETUP transaction until the start of the ACK packet returned by the SIE. The CPU is prevented from clearing this bit during this interval. After this interval the bit will remain set until cleared by firmware. While this bit is set to '1' the CPU cannot write to the EP0_DRx registers. This prevents firmware from overwriting an incoming SETUP transaction before firmware has a chance to read the SETUP data. This bit is cleared by any non-locked writes to the register. Default Value: 0
6	IN_RCVD	When set this bit indicates a valid IN packet has been received. This bit is updated to '1' after the host acknowledges an IN data packet. When clear this bit indicates either no IN has been re-ceived or that the host did not acknowledge the IN data by sending ACK handshake. It is cleared by any writes to the register. Default Value: 0
5	OUT_RCVD	When set this bit indicates a valid OUT packet has been received and ACKed. This bit is updated to '1' after the last received packet in an OUT transaction. When clear this bit indicates no OUT received. It is cleared by any writes to the register. Default Value: 0

23.1.17 USBFS0_USBDEV_EP0_CR (continued)

4	ACKED_TXN	The ACK'd transaction bit is set whenever the SIE engages in a transaction to the register's end-point that completes with an ACK packet. This bit is cleared by any writes to the register. Default Value: 0 **0x0: ACKED_NO :** No ACK'd transactions since bit was last cleared. **0x1: ACKED_YES :** Indicates a transaction ended with an ACK.
3 : 0	MODE	The mode controls how the USB SIE responds to traffic and how the USB SIE changes the mode of that endpoint as a result of host packets to the endpoint. Default Value: 0 **0x0: DISABLE :** Ignore all USB traffic to this endpoint **0x1: NAK_INOUT :** SETUP: Accept IN: NAK OUT: NAK **0x2: STATUS_OUT_ONLY :** SETUP: Accept IN: STALL OUT: ACK 0B tokens, NAK others **0x3: STALL_INOUT :** SETUP: Accept IN: STALL OUT: STALL **0x5: ISO_OUT :** SETUP: Ignore IN: Ignore OUT: Accept Isochronous OUT token **0x6: STATUS_IN_ONLY :** SETUP: Accept IN: Respond with 0B data OUT: Stall

23.1.17 USBFS0_USBDEV_EP0_CR (continued)

0x7: ISO_IN :

SETUP: Ignore
IN: Accept Isochronous IN token
OUT: Ignore

0x8: NAK_OUT :

SETUP: Ignore
IN: Ignore
OUT: NAK

0x9: ACK_OUT :

SETUP: Ignore
IN: Ignore
OUT: Accept data and ACK if STALL=0, STALL otherwise.
Change to MODE=8 after one succesfull OUT token.

0xb: ACK_OUT_STATUS_IN :

SETUP: Accept
IN: Respond with 0B data
OUT: Accept data

0xc: NAK_IN :

SETUP: Ignore
IN: NAK
OUT: Ignore

0xd: ACK_IN :

SETUP: Ignore
IN: Respond to IN with data if STALL=0, STALL otherwise
OUT: Ignore

0xf: ACK_IN_STATUS_OUT :

SETUP: Accept
IN: Respond to IN with data
OUT: ACK 0B tokens, NAK others

23.1.18 USBFS0_USBDEV_EP0_CNT

Endpoint0 count Register

Address: 0x403F00A4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW0C	None		RW			
HW Access	RW	RW1S	None		RW			
Name	DATA_-TOGGLE	DATA_VAL-ID	None [5:4]		BYTE_COUNT [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	DATA_TOGGLE	This bit selects the DATA packet's toggle state. For IN transactions firmware must set this bit to the expected state. For OUT transactions the hardware sets this bit to the state of the received Data Toggle bit. Default Value: 0
6	DATA_VALID	This bit is used for OUT/SETUP transactions only and is read only. It is cleared to '0' if CRC bit stuffing errors or PID errors occur. This bit does not update for some endpoint mode settings. Default Value: 0 **0x0: DATA_ERROR :** No ACK'd transactions since bit was last cleared. **0x1: DATA_VALID :** Indicates a transaction ended with an ACK.

23.1.18 USBFS0_USBDEV_EP0_CNT (continued)

3 : 0	BYTE_COUNT	These bits indicate the number of data bytes in a transaction. For IN transactions firmware loads the count with the number of bytes to be transmitted to the host from the endpoint FIFO. Valid values are 0 to 8. For OUT or SETUP transactions the count is updated by hardware to the number of data bytes received plus two for the CRC bytes. Valid values are 2 to 10. Default Value: 0

23.1.19 USBFS0_USBDEV_ARB_EP1_CFG

Endpoint Configuration Register *1

Address: 0x403F0200

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [7:4]				RE-SET_PTR	CRC_BY-PASS	DMA_REQ	IN_-DATA_RDY

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	RESET_PTR	Configuration Setting to Reset the RA and WA Pointers to their start values at the End of Packet transaction. Default Value: 0 **0x0: RESET_KRYPTON :** Do not Reset Pointer; Krypton Backward compatibility mode **0x1: RESET_NORMAL :** Reset Pointer; recommended value for reduction of CPU Configuration Writes.
2	CRC_BYPASS	Configuration Setting to prevent CRC bytes from being written to memory and being read by firm-ware Default Value: 0

23.1.19 USBFS0_USBDEV_ARB_EP1_CFG (continued)

		0x0: CRC_NORMAL : No CRC bypass; CRC bytes will be written to memory and Termin will be generated for the CRC byte/s **0x1: CRC_BYPASS :** CRC Bypass Set; CRC bytes will not be written into memory and Termin will be generated for the last data byte/s
1	DMA_REQ	Manual DMA Request for a particular (1 to 8) endpoint; changing this field from 0 to 1 causes a DMA request to be generated. Default Value: 0
0	IN_DATA_RDY	Indication that Endpoint Packet Data is Ready in Main memory Default Value: 0

23.1.20 USBFS0_USBDEV_ARB_EP1_INT_EN

Endpoint Interrupt Enable Register *1

Address: 0x403F0204

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		R	R	R	R	R	R
Name	None [7:6]		DMA_TERMIN_EN	ERR_INT_EN	BUF_UNDER_EN	BUF_OVER_EN	DMA_GNT_EN	IN_BUF_FULL_EN

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	DMA_TERMIN_EN	Endpoint DMA Terminated Enable Default Value: 0
4	ERR_INT_EN	Endpoint Error in Transaction Interrupt Enable Default Value: 0
3	BUF_UNDER_EN	Endpoint Buffer Underflow Enable Default Value: 0
2	BUF_OVER_EN	Endpoint Buffer Overflow Enable Default Value: 0
1	DMA_GNT_EN	Endpoint DMA Grant Enable Default Value: 0
0	IN_BUF_FULL_EN	IN Endpoint Local Buffer Full Enable Default Value: 0

23.1.21 USBFS0_USBDEV_ARB_EP1_SR

Endpoint Interrupt Enable Register *1

Address: 0x403F0208

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW1C	None	RW1C	RW1C	RW1C	RW1C
HW Access	None		RW1S	None	RW1S	RW1S	RW1S	RW1S
Name	None [7:6]		DMA_TER-MIN	None	BUF_UNDER	BUF_OVER	DMA_GNT	IN_BUF_-FULL

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	DMA_TERMIN	Endpoint DMA Terminated Interrupt Default Value: 0
3	BUF_UNDER	Endpoint Buffer Underflow Interrupt Default Value: 0
2	BUF_OVER	Endpoint Buffer Overflow Interrupt Default Value: 0
1	DMA_GNT	Endpoint DMA Grant Interrupt Default Value: 0
0	IN_BUF_FULL	IN Endpoint Local Buffer Full Interrupt Default Value: 0

23.1.22 USBFS0_USBDEV_ARB_RW1_WA

Endpoint Write Address value *1, *2

Address: 0x403F0210

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	WA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	WA	Write Address for EP Default Value: 0

23.1.23 USBFS0_USBDEV_ARB_RW1_WA_MSB

Endpoint Write Address value *1, *2

Address: 0x403F0214

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							RW
Name	None [7:1]							WA_MSB

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	WA_MSB	Write Address for EP Default Value: 0

23.1.24 USBFS0_USBDEV_ARB_RW1_RA

Endpoint Read Address value *1, *2

Address: 0x403F0218

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	RA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	RA	Read Address for EP Default Value: 0

23.1.25 USBFS0_USBDEV_ARB_RW1_RA_MSB

Endpoint Read Address value *1, *2

Address: 0x403F021C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							RW
Name	None [7:1]							RA_MSB

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	RA_MSB	Read Address for EP Default Value: 0

23.1.26 USBFS0_USBDEV_ARB_RW1_DR

Endpoint Data Register

Address: 0x403F0220

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DR	Data Register for EP ; This register is linked to the memory, hence reset value is undefined Default Value: X

23.1.27 USBFS0_USBDEV_BUF_SIZE

Dedicated Endpoint Buffer Size Register *1

Address: 0x403F0230

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	OUT_BUF [7:4]				IN_BUF [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	OUT_BUF	Buffer size for OUT Endpoints. Default Value: 0
3 : 0	IN_BUF	Buffer size for IN Endpoints. Default Value: 0

23.1.28 USBFS0_USBDEV_EP_ACTIVE

Endpoint Active Indication Register *1

Address: 0x403F0238

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	EP8_ACT	EP7_ACT	EP6_ACT	EP5_ACT	EP4_ACT	EP3_ACT	EP2_ACT	EP1_ACT

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	EP8_ACT	Indicates that Endpoint is currently active. Default Value: 0
6	EP7_ACT	Indicates that Endpoint is currently active. Default Value: 0
5	EP6_ACT	Indicates that Endpoint is currently active. Default Value: 0
4	EP5_ACT	Indicates that Endpoint is currently active. Default Value: 0
3	EP4_ACT	Indicates that Endpoint is currently active. Default Value: 0
2	EP3_ACT	Indicates that Endpoint is currently active. Default Value: 0
1	EP2_ACT	Indicates that Endpoint is currently active. Default Value: 0
0	EP1_ACT	Indicates that Endpoint is currently active. Default Value: 0

23.1.29 USBFS0_USBDEV_EP_TYPE

Endpoint Type (IN/OUT) Indication *1

Address: 0x403F023C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	EP8_TYP	EP7_TYP	EP6_TYP	EP5_TYP	EP4_TYP	EP3_TYP	EP2_TYP	EP1_TYP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	EP8_TYP	Endpoint Type Indication. Default Value: 0 **0x0: EP_IN :** IN outpoint **0x1: EP_OUT :** OUT outpoint
6	EP7_TYP	Endpoint Type Indication. Default Value: 0 **0x0: EP_IN :** IN outpoint

23.1.29 USBFS0_USBDEV_EP_TYPE (continued)

		0x1: EP_OUT : OUT outpoint
5	EP6_TYP	Endpoint Type Indication. Default Value: 0 **0x0: EP_IN :** IN outpoint **0x1: EP_OUT :** OUT outpoint
4	EP5_TYP	Endpoint Type Indication. Default Value: 0 **0x0: EP_IN :** IN outpoint **0x1: EP_OUT :** OUT outpoint
3	EP4_TYP	Endpoint Type Indication. Default Value: 0 **0x0: EP_IN :** IN outpoint **0x1: EP_OUT :** OUT outpoint
2	EP3_TYP	Endpoint Type Indication. Default Value: 0 **0x0: EP_IN :** IN outpoint **0x1: EP_OUT :** OUT outpoint
1	EP2_TYP	Endpoint Type Indication. Default Value: 0 **0x0: EP_IN :** IN outpoint

23.1.29 USBFS0_USBDEV_EP_TYPE (continued)

		0x1: EP_OUT : OUT outpoint
0	EP1_TYP	Endpoint Type Indication. Default Value: 0 **0x0: EP_IN :** IN outpoint **0x1: EP_OUT :** OUT outpoint

23.1.30 USBFS0_USBDEV_ARB_CFG

Arbiter Configuration Register *1

Address: 0x403F0270

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW		RW	None			
HW Access	R	R		R	None			
Name	CFG_CMP	DMA_CFG [6:5]		AU-TO_MEM	None			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	CFG_CMP	Register Configuration Complete Indication. Posedge is detected on this bit. Hence a 0 to 1 transition is required. Default Value: 0
6 : 5	DMA_CFG	DMA Access Configuration. Default Value: 0 **0x0: DMA_NONE :** No DMA **0x1: DMA_MANUAL :** Manual DMA **0x2: DMA_AUTO :** Auto DMA

23.1.30 USBFS0_USBDEV_ARB_CFG (continued)

4	AUTO_MEM	Enables Auto Memory Configuration. Manual memory configuration by default. Default Value: 0

23.1.31 USBFS0_USBDEV_USB_CLK_EN

USB Block Clock Enable Register

Address: 0x403F0274

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							CSR_-CLK_EN

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	CSR_CLK_EN	Clock Enable for Core Logic clocked by AHB bus clock Default Value: 0

23.1.32 USBFS0_USBDEV_ARB_INT_EN

Arbiter Interrupt Enable *1

Address: 0x403F0278

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	EP8_IN-TR_EN	EP7_IN-TR_EN	EP6_IN-TR_EN	EP5_IN-TR_EN	EP4_IN-TR_EN	EP3_IN-TR_EN	EP2_IN-TR_EN	EP1_IN-TR_EN

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	EP8_INTR_EN	Enables interrupt for EP8 Default Value: 0
6	EP7_INTR_EN	Enables interrupt for EP7 Default Value: 0
5	EP6_INTR_EN	Enables interrupt for EP6 Default Value: 0
4	EP5_INTR_EN	Enables interrupt for EP5 Default Value: 0
3	EP4_INTR_EN	Enables interrupt for EP4 Default Value: 0
2	EP3_INTR_EN	Enables interrupt for EP3 Default Value: 0
1	EP2_INTR_EN	Enables interrupt for EP2 Default Value: 0

23.1.32 USBFS0_USBDEV_ARB_INT_EN (continued)

0	EP1_INTR_EN	Enables interrupt for EP1 Default Value: 0

23.1.33 USBFS0_USBDEV_ARB_INT_SR

Arbiter Interrupt Status *1

Address: 0x403F027C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
Name	EP8_INTR	EP7_INTR	EP6_INTR	EP5_INTR	EP4_INTR	EP3_INTR	EP2_INTR	EP1_INTR

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	EP8_INTR	Interrupt status for EP8 Default Value: 0
6	EP7_INTR	Interrupt status for EP7 Default Value: 0
5	EP6_INTR	Interrupt status for EP6 Default Value: 0
4	EP5_INTR	Interrupt status for EP5 Default Value: 0
3	EP4_INTR	Interrupt status for EP4 Default Value: 0
2	EP3_INTR	Interrupt status for EP3 Default Value: 0
1	EP2_INTR	Interrupt status for EP2 Default Value: 0
0	EP1_INTR	Interrupt status for EP1 Default Value: 0

23.1.34 USBFS0_USBDEV_CWA

Common Area Write Address *1

Address: 0x403F02B0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CWA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	CWA	Write Address for Common Area Default Value: 0

23.1.35 USBFS0_USBDEV_CWA_MSB

Endpoint Read Address value *1

Address: 0x403F02B4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							RW
Name	None [7:1]							CWA_MSB

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	CWA_MSB	Write Address for Common Area Default Value: 0

23.1.36 USBFS0_USBDEV_DMA_THRES

DMA Burst / Threshold Configuration

Address: 0x403F02F0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DMA_THS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DMA_THS	DMA Threshold count Default Value: 0

23.1.37 USBFS0_USBDEV_DMA_THRES_MSB

DMA Burst / Threshold Configuration

Address: 0x403F02F4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							RW
Name	None [7:1]							DMA_THS_MSB

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	DMA_THS_MSB	DMA Threshold count Default Value: 0

23.1.38 USBFS0_USBDEV_BUS_RST_CNT

Bus Reset Count Register

Address: 0x403F0330

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				bus_rst_cnt [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	bus_rst_cnt	Bus Reset Count Length Default Value: 10

23.1.39 USBFS0_USBDEV_MEM_DATA0

DATA

Address: 0x403F0400

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DR	Data Register for EP ; This register is linked to the memory, hence reset value is undefined Default Value: X

23.1.40 USBFS0_USBDEV_SOF16

Start Of Frame Register

Address: 0x403F1060

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	FRAME_NUMBER16 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None					R		
HW Access	None					RW		
Name	None [15:11]					FRAME_NUMBER16 [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10 : 0	FRAME_NUMBER16	The frame number (11b) Default Value: 0

23.1.41 USBFS0_USBDEV_OSCLK_DR16

Oscillator lock data register

Address: 0x403F1080

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	ADDER16 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None	R						
HW Access	None	W						
Name	None	ADDER16 [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
14 : 0	ADDER16	These bits return the oscillator locking circuits adder output. Default Value: X

23.1.42 USBFS0_USBDEV_ARB_RW1_WA16

Endpoint Write Address value *3

Address: 0x403F1210

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	WA16 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							RW
Name	None [15:9]							WA16

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8 : 0	WA16	Write Address for EP Default Value: 0

23.1.43 USBFS0_USBDEV_ARB_RW1_RA16

Endpoint Read Address value *3

Address: 0x403F1218

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	RA16 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							RW
Name	None [15:9]							RA16

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8 : 0	RA16	Read Address for EP Default Value: 0

23.1.44 USBFS0_USBDEV_ARB_RW1_DR16

Endpoint Data Register

Address: 0x403F1220

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DR16 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DR16 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DR16	Data Register for EP ; This register is linked to the memory, hence reset value is undefined Default Value: X

23.1.45 USBFS0_USBDEV_CWA16

Common Area Write Address

Address: 0x403F12B0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CWA16 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							RW
Name	None [15:9]							CWA16

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8 : 0	CWA16	Write Address for Common Area Default Value: 0

23.1.46 USBFS0_USBDEV_DMA_THRES16

DMA Burst / Threshold Configuration

Address: 0x403F12F0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DMA_THS16 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							RW
Name	None [15:9]							DMA_THS16

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8 : 0	DMA_THS16	DMA Threshold count Default Value: 0

23.1.47 USBFS0_USBLPM_POWER_CTL

Power Control Register

Address: 0x403F2000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW	None	
HW Access	None					R	None	
Name	None [7:3]					SUSPEND	None	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		R	R	R	R	R	R
Name	None [23:22]		DM_DOWN_EN	DM_BIG	DM_UP_EN	DP_DOWN_EN	DP_BIG	DP_UP_EN

Bits	31	30	29	28	27	26	25	24
SW Access	None		RW	RW	None			
HW Access	None		R	R	None			
Name	None [31:30]		ENABLE_DMO	ENABLE_DPO	None [27:24]			

Bits	Name	Description
29	ENABLE_DMO	Enables the signle ended receiver on D-. Default Value: 0
28	ENABLE_DPO	Enables the single ended receiver on D+. Default Value: 0
21	DM_DOWN_EN	Enables the ~15k pull down on the DP. Default Value: 0
20	DM_BIG	Select the resister value if POWER_CTL.DM_EN='1'. This bit is valid in GPIO. '0' : The resister value is from 900 to1575Ohmpull up on the DM. '1' : The resister value is from 1425 to 3090Ohmpull up on the DM Default Value: 0
19	DM_UP_EN	Enables the pull up on the DM. The bit is valid in GPIO. The pull up resistor is disabled in not GPIO. '0' : Disable. '1' : Enable. Default Value: 0

23.1.47 USBFS0_USBLPM_POWER_CTL (continued)

18	DP_DOWN_EN	Enables the ~15k pull down on the DP. Default Value: 0
17	DP_BIG	Select the resister value if POWER_CTL.DP_EN='1'. This bit is valid in GPIO. '0' : The resister value is from 900 to1575Ohmpull up on the DP. '1' : The resister value is from 1425 to 3090Ohmpull up on the DP Default Value: 0
16	DP_UP_EN	Enables the pull up on the DP. '0' : Disable. '1' : Enable. Default Value: 0
2	SUSPEND	Put PHY into Suspend mode. If the PHY is enabled, this bit MUST be set before entering a low power mode (DeepSleep). Note: - This bit is invalid if the HOST bit of the Host Control 0 Register (HOST_CTL0) is '1'. Default Value: 0

23.1.48 USBFS0_USBLPM_USBIO_CTL

USB IO Control Register

Address: 0x403F2008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW			RW		
HW Access	None		R			R		
Name	None [7:6]		DM_M [5:3]			DM_P [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 3	DM_M	The GPIO Drive Mode for DM IO pad. Default Value: 0
2 : 0	DM_P	The GPIO Drive Mode for DP IO pad. This field only applies if USBIO_CR1.IOMODE =1. Data comes from the corresponding GPIO.DR register. Default Value: 0 **0x0: OFF :** Mode 0: Output buffer off (high Z). Input buffer off. **0x1: INPUT :** Mode 1: Output buffer off (high Z). Input buffer on. Other values, not supported.

23.1.49 USBFS0_USBLPM_FLOW_CTL

Flow Control Register

Address: 0x403F200C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	EP8_ER-R_RESP	EP7_ER-R_RESP	EP6_ER-R_RESP	EP5_ER-R_RESP	EP4_ER-R_RESP	EP3_ER-R_RESP	EP2_ER-R_RESP	EP1_ER-R_RESP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	EP8_ERR_RESP	End Point 8 error response Default Value: 0
6	EP7_ERR_RESP	End Point 7 error response Default Value: 0
5	EP6_ERR_RESP	End Point 6 error response Default Value: 0
4	EP5_ERR_RESP	End Point 5 error response Default Value: 0
3	EP4_ERR_RESP	End Point 4 error response Default Value: 0
2	EP3_ERR_RESP	End Point 3 error response Default Value: 0
1	EP2_ERR_RESP	End Point 2 error response Default Value: 0

23.1.49 USBFS0_USBLPM_FLOW_CTL (continued)

0	EP1_ERR_RESP	End Point 1 error response 0: do nothing (backward compatibility mode) 1: if this is an IN EP and an underflow occurs then cause a CRC error, if this is an OUT EP and an overflow occurs then send a NAK Default Value: 0

23.1.50 USBFS0_USBLPM_LPM_CTL

LPM Control Register

Address: 0x403F2010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	None	RW	RW	RW
HW Access	None			R	None	R	R	R
Name	None [7:5]			SUB_RESP	None	NYET_EN	LP-M_ACK_RESP	LPM_EN

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4	SUB_RESP	Enable a STALL response for all undefined SubPIDs, i.e. other than LPM (0011b). If not enabled then there will be no response (Error) for the undefined SubPIDs. Default Value: 0
2	NYET_EN	Allow firmware to choose which response to use for an LPM token (LPM_EN=1) when the device is NOT ready to go to the requested low power mode (LPM_ACK_RESP=0). 0: a LPM token will get an NAK response (indicating a CRC error), the host is expected to repeat the LPM token. 1: a LPM token will get a NYET response Default Value: 0
1	LPM_ACK_RESP	LPM ACK response enable (if LPM_EN=1), to allow firmware to refuse a low power request 0: a LPM token will get a NYET or NAK (depending on NYET_EN bit below) response and the device will NOT go to a low power mode 1: a LPM token will get an ACK response and the device will go to the requested low power mode Default Value: 0

23.1.50 USBFS0_USBLPM_LPM_CTL (continued)

0	LPM_EN	LPM enable 0: Disabled, LPM token will not get a response (backward compatibility mode) 1: Enable, LPM token will get a handshake response (ACK, STALL, NYET or NAK) A STALL will be sent if the bLinkState is not 0001b A NYET, NAK or ACK response will be sent depending on the NYET_EN and LPM_ACK_RESP bits below Default Value: 0

23.1.51 USBFS0_USBLPM_LPM_STAT

LPM Status register

Address: 0x403F2014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			R	R			
HW Access	None			RW	RW			
Name	None [7:5]			LPM_RE-MOTEWAKE	LPM_BESL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4	LPM_REMOTEWAKE	0: Device is prohibited from initiating a remote wake 1: Device is allow to wake the host Default Value: 0
3 : 0	LPM_BESL	Best Effort Service Latency This value should match either the Baseline (DeepSleep) or Deep (Hibernate) BESL in the BOS descriptor. Default Value: 0

23.1.52 USBFS0_USBLPM_INTR_SIE

USB SOF, BUS RESET and EP0 Interrupt Status

Address: 0x403F2020

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	None			RW1S	RW1S	RW1S	RW1S	RW1S
Name	None [7:5]			RE-SUME_IN-TR	LPM_INTR	EP0_INTR	BUS_RE-SET_INTR	SOF_INTR

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4	RESUME_INTR	Interrupt status for Resume Default Value: 0
3	LPM_INTR	Interrupt status for LPM (Link Power Management, L1 entry) Default Value: 0
2	EP0_INTR	Interrupt status for EP0 Default Value: 0
1	BUS_RESET_INTR	Interrupt status for BUS RESET Default Value: 0
0	SOF_INTR	Interrupt status for USB SOF Default Value: 0

23.1.53 USBFS0_USBLPM_INTR_SIE_SET

USB SOF, BUS RESET and EP0 Interrupt Set

Address: 0x403F2024

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	None			A	A	A	A	A
Name	None [7:5]			RE-SUME_IN-TR_SET	LPM_IN-TR_SET	EP0_IN-TR_SET	BUS_RE-SET_IN-TR_SET	SOF_IN-TR_SET

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4	RESUME_INTR_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
3	LPM_INTR_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
2	EP0_INTR_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
1	BUS_RESET_INTR_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	SOF_INTR_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

23.1.54 USBFS0_USBLPM_INTR_SIE_MASK

USB SOF, BUS RESET and EP0 Interrupt Mask

Address: 0x403F2028

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [7:5]			RE-SUME_IN-TR_MASK	LPM_IN-TR_MASK	EP0_IN-TR_MASK	BUS_RE-SET_IN-TR_MASK	SOF_IN-TR_MASK

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4	RESUME_INTR_MASK	Set to 1 to enable interrupt corresponding to interrupt request register Default Value: 0
3	LPM_INTR_MASK	Set to 1 to enable interrupt corresponding to interrupt request register Default Value: 0
2	EP0_INTR_MASK	Set to 1 to enable interrupt corresponding to interrupt request register Default Value: 0
1	BUS_RESET_IN-TR_MASK	Set to 1 to enable interrupt corresponding to interrupt request register Default Value: 0
0	SOF_INTR_MASK	Set to 1 to enable interrupt corresponding to interrupt request register Default Value: 0

23.1.55 USBFS0_USBLPM_INTR_SIE_MASKED

USB SOF, BUS RESET and EP0 Interrupt Masked

Address: 0x403F202C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			R	R	R	R	R
HW Access	None			W	W	W	W	W
Name	None [7:5]			RESUME_INTR_MASKED	LPM_INTR_MASKED	EP0_INTR_MASKED	BUS_RESET_INTR_MASKED	SOF_INTR_MASKED

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4	RESUME_INTR_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
3	LPM_INTR_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
2	EP0_INTR_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
1	BUS_RESET_INTR_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
0	SOF_INTR_MASKED	Logical and of corresponding request and mask bits. Default Value: 0

23.1.56 USBFS0_USBLPM_INTR_LVL_SEL

Select interrupt level for each interrupt source

Address: 0x403F2030

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	LPM_LVL_SEL [7:6]		EP0_LVL_SEL [5:4]		BUS_RESET_LVL_SEL [3:2]		SOF_LVL_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW		None				RW	
HW Access	R		None				R	
Name	ARB_EP_LVL_SEL [15:14]		None [13:10]				RESUME_LVL_SEL [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	EP4_LVL_SEL [23:22]		EP3_LVL_SEL [21:20]		EP2_LVL_SEL [19:18]		EP1_LVL_SEL [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	EP8_LVL_SEL [31:30]		EP7_LVL_SEL [29:28]		EP6_LVL_SEL [27:26]		EP5_LVL_SEL [25:24]	

Bits	Name	Description
31 : 30	EP8_LVL_SEL	EP8 Interrupt level select Default Value: 0
29 : 28	EP7_LVL_SEL	EP7 Interrupt level select Default Value: 0
27 : 26	EP6_LVL_SEL	EP6 Interrupt level select Default Value: 0
25 : 24	EP5_LVL_SEL	EP5 Interrupt level select Default Value: 0
23 : 22	EP4_LVL_SEL	EP4 Interrupt level select Default Value: 0
21 : 20	EP3_LVL_SEL	EP3 Interrupt level select Default Value: 0
19 : 18	EP2_LVL_SEL	EP2 Interrupt level select Default Value: 0

23.1.56 USBFS0_USBLPM_INTR_LVL_SEL (continued)

17 : 16	EP1_LVL_SEL	EP1 Interrupt level select Default Value: 0
15 : 14	ARB_EP_LVL_SEL	Arbiter Endpoint Interrupt level select Default Value: 0
9 : 8	RESUME_LVL_SEL	Resume Interrupt level select Default Value: 0
7 : 6	LPM_LVL_SEL	LPM Interrupt level select Default Value: 0
5 : 4	EP0_LVL_SEL	EP0 Interrupt level select Default Value: 0
3 : 2	BUS_RESET_LVL_SEL	BUS RESET Interrupt level select Default Value: 0
1 : 0	SOF_LVL_SEL	USB SOF Interrupt level select Default Value: 0 **0x0: HI :** High priority interrupt **0x1: MED :** Medium priority interrupt **0x2: LO :** Low priority interrupt **0x3: RESERVED :** illegal

23.1.57 USBFS0_USBLPM_INTR_CAUSE_HI

High priority interrupt Cause register

Address: 0x403F2034

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	None		R	R	R	R	R
HW Access	RW	None		RW	RW	RW	RW	RW
Name	AR-B_EP_INTR	None [6:5]		RE-SUME_IN-TR	LPM_INTR	EP0_INTR	BUS_RE-SET_INTR	SOF_INTR

Bits	15	14	13	12	11	10	9	8
SW Access	R	R	R	R	R	R	R	R
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	EP8_INTR	EP7_INTR	EP6_INTR	EP5_INTR	EP4_INTR	EP3_INTR	EP2_INTR	EP1_INTR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15	EP8_INTR	EP8 Interrupt Default Value: 0
14	EP7_INTR	EP7 Interrupt Default Value: 0
13	EP6_INTR	EP6 Interrupt Default Value: 0
12	EP5_INTR	EP5 Interrupt Default Value: 0
11	EP4_INTR	EP4 Interrupt Default Value: 0
10	EP3_INTR	EP3 Interrupt Default Value: 0
9	EP2_INTR	EP2 Interrupt Default Value: 0

23.1.57 USBFS0_USBLPM_INTR_CAUSE_HI (continued)

8	EP1_INTR	EP1 Interrupt Default Value: 0
7	ARB_EP_INTR	Arbiter Endpoint Interrupt Default Value: 0
4	RESUME_INTR	Resume Interrupt Default Value: 0
3	LPM_INTR	LPM Interrupt Default Value: 0
2	EP0_INTR	EP0 Interrupt Default Value: 0
1	BUS_RESET_INTR	BUS RESET Interrupt Default Value: 0
0	SOF_INTR	USB SOF Interrupt Default Value: 0

23.1.58 USBFS0_USBLPM_INTR_CAUSE_MED

Medium priority interrupt Cause register

Address: 0x403F2038

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	None		R	R	R	R	R
HW Access	RW	None		RW	RW	RW	RW	RW
Name	AR-B_EP_INTR	None [6:5]		RE-SUME_IN-TR	LPM_INTR	EP0_INTR	BUS_RE-SET_INTR	SOF_INTR

Bits	15	14	13	12	11	10	9	8
SW Access	R	R	R	R	R	R	R	R
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	EP8_INTR	EP7_INTR	EP6_INTR	EP5_INTR	EP4_INTR	EP3_INTR	EP2_INTR	EP1_INTR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15	EP8_INTR	EP8 Interrupt Default Value: 0
14	EP7_INTR	EP7 Interrupt Default Value: 0
13	EP6_INTR	EP6 Interrupt Default Value: 0
12	EP5_INTR	EP5 Interrupt Default Value: 0
11	EP4_INTR	EP4 Interrupt Default Value: 0
10	EP3_INTR	EP3 Interrupt Default Value: 0
9	EP2_INTR	EP2 Interrupt Default Value: 0

23.1.58 USBFS0_USBLPM_INTR_CAUSE_MED (continued)

8	EP1_INTR	EP1 Interrupt Default Value: 0
7	ARB_EP_INTR	Arbiter Endpoint Interrupt Default Value: 0
4	RESUME_INTR	Resume Interrupt Default Value: 0
3	LPM_INTR	LPM Interrupt Default Value: 0
2	EP0_INTR	EP0 Interrupt Default Value: 0
1	BUS_RESET_INTR	BUS RESET Interrupt Default Value: 0
0	SOF_INTR	USB SOF Interrupt Default Value: 0

23.1.59 USBFS0_USBLPM_INTR_CAUSE_LO

Low priority interrupt Cause register

Address: 0x403F203C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	None		R	R	R	R	R
HW Access	RW	None		RW	RW	RW	RW	RW
Name	ARB_EP_INTR	None [6:5]		RESUME_INTR	LPM_INTR	EP0_INTR	BUS_RESET_INTR	SOF_INTR

Bits	15	14	13	12	11	10	9	8
SW Access	R	R	R	R	R	R	R	R
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	EP8_INTR	EP7_INTR	EP6_INTR	EP5_INTR	EP4_INTR	EP3_INTR	EP2_INTR	EP1_INTR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15	EP8_INTR	EP8 Interrupt Default Value: 0
14	EP7_INTR	EP7 Interrupt Default Value: 0
13	EP6_INTR	EP6 Interrupt Default Value: 0
12	EP5_INTR	EP5 Interrupt Default Value: 0
11	EP4_INTR	EP4 Interrupt Default Value: 0
10	EP3_INTR	EP3 Interrupt Default Value: 0
9	EP2_INTR	EP2 Interrupt Default Value: 0

23.1.59 USBFS0_USBLPM_INTR_CAUSE_LO (continued)

8	EP1_INTR	EP1 Interrupt Default Value: 0
7	ARB_EP_INTR	Arbiter Endpoint Interrupt Default Value: 0
4	RESUME_INTR	Resume Interrupt Default Value: 0
3	LPM_INTR	LPM Interrupt Default Value: 0
2	EP0_INTR	EP0 Interrupt Default Value: 0
1	BUS_RESET_INTR	BUS RESET Interrupt Default Value: 0
0	SOF_INTR	USB SOF Interrupt Default Value: 0

23.1.60 USBFS0_USBLPM_DFT_CTL

DFT control

Address: 0x403F2070

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW		RW		
HW Access	None			R		R		
Name	None [7:5]			DDFT_IN_SEL [4:3]		DDFT_OUT_SEL [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4 : 3	DDFT_IN_SEL	DDFT input select signal Default Value: 0 **0x0: OFF :** Nothing connected, output 0 **0x1: GPIO_DP_IN :** GPIO input of DP **0x2: GPIO_DM_IN :** GPIO input of DM
2 : 0	DDFT_OUT_SEL	DDFT output select signal Default Value: 0

23.1.60 USBFS0_USBLPM_DFT_CTL (continued)

0x0: OFF :

Nothing connected, output 0

0x1: DP_SE :

Single Ended output of DP

0x2: DM_SE :

Single Ended output of DM

0x3: TXOE :

Output Enable

0x4: RCV_DF :

Differential Receiver output

0x5: GPIO_DP_OUT :

GPIO output of DP

0x6: GPIO_DM_OUT :

GPIO output of DM

23.1.61 USBFS0_USBHOST_HOST_CTL0

Host Control 0 Register.

Address: 0x403F4000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							RW
Name	None [7:1]							HOST

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	ENABLE	None [30:24]						

Bits	Name	Description
31	ENABLE	This bit enables the operation of this IP. '0' : Disable USB Host '1' : Enable USB Host Note: - This bit doesn't affect the USB Device. Default Value: 0
0	HOST	This bit selects an operating mode of this IP. '0' : USB Device '1' : USB Host Notes: - The mode of operation mode does not transition immediately after setting this bit. Read this bit to confirm that the operation mode has changed. - This bit is reset to '0' if the ENABLE bit in this register changes from '1' to '0'. - Before changing from the USB Host to the USB Device, check that the following conditions are satisfied and also set the RST bit of the Host Control 1 Register (HOST_CTL1). to '1'. * The SOFBUSY bit of the Host Status Register (HOST_STATUS) is set to '0'. * The TKNEN bits of the Host Token Endpoint Register (HOST_TOKEN) is set to '000'. * The SUSP bit of the Host Status Register (HOST_STATUS) is set to '0'. Default Value: 0

23.1.62 USBFS0_USBHOST_HOST_CTL1

Host Control 1 Register.

Address: 0x403F4010

Retention: Retained

Bits	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SW Access	RW	None					RW	RW
HW Access	R	None					R	R
Name	RST	None [6:2]					USTP	CLKSEL

Bits	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	**Name**	**Description**
7	RST	This bit resets the USB Host. '0' : Normal operating mode. '1' : USB Host is reset. Notes: - This bit is to it's default value '1' if the ENABLE bit of the Host Control 0 Register (HOST_CTL0) changes from '1' to '0'. - If this bit is set to '1', both the BFINI bits of the Host Endpoint 1 Control Register (HOST_EP1_CTL) and Host Endpoint 2 Control Register (HOST_EP2_CTL) are set to '1'. Default Value: 1
1	USTP	This bit stops the clock for the USB Host operating unit. When this bit is '1', power consumption can be reduced by configuring this bit. '0' : Normal operating mode. '1' : Stops the clock for the USB Host operating unit. Notes: - If this bit is set to '1', the function of USB Host can't be used because internal clock is stopped. - This bit is initialized if ENABLE bit of the Host Control 0 Register (HOST_CTL0) changes from '1' to '0'. Default Value: 1

23.1.62 USBFS0_USBHOST_HOST_CTL1 (continued)

0	CLKSEL	This bit selects the operating clock of USB Host. '0' : Low-speed clock '1' : Full-speed clock Notes: - This bit is set to it's default vaulue '1' if the ENABLE bit of the Host Control 0 Register (HOST_CTL0) changes from '1' to '0'. - This bit must always be set to '1' in the USB Device mode. Default Value: 1

23.1.63 USBFS0_USBHOST_HOST_CTL2

Host Control 2 Register.

Address: 0x403F4100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW	RW	RW	RW	RW	RW
HW Access	R		R	R	R	R	R	R
Name	TTEST [7:6]		RE-SERVED_5	RE-SERVED_4	ALIVE	SOFSTEP	CANCEL	RETRY

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	TTEST	Reserved. Keep this bitfield at the default value. Default Value: 0
5	RESERVED_5	Reserved. Keep this bitfield at the default value. Default Value: 0
4	RESERVED_4	Reserved. Keep this bitfield at the default value. Default Value: 0
3	ALIVE	This bit is used to specify the keep-alive function in the low-speed mode. If this bit it set to '1' while the CLKSEL bit of the Host Control 1 Register (HOST_CTL1) is '0', SE0 is output instead of SOF. This bit is only effective when the CLKSEL bit is '0'. If the CLKSEL bit is '1' (Full-Speed mode), SOF is output regardless of the setting of the ALIVE bit. '0' : SOF output. '1' : SE0 output (Keep alive) Default Value: 0

23.1.63 USBFS0_USBHOST_HOST_CTL2 (continued)

2	SOFSTEP	If this bit is set to '1', the SOF interrupt flag (INTR_USBHOST.SOFIRQ) is set to '1' each time SOF is sent. If this bit is set to '0', the set value of the Host SOF Interrupt Frame Compare Register (HOST_F-COMP) is compared with the low-order eight bits of the SOF frame number. If they match, the SOF interrupt flag (INTR_USBHOST.SOFIRQ) is set to '1'. '0' : An interrupt occurred due to the HOST_HFCOMP setting. '1' : An interrupt occurred. Notes: - If a SOF token (TKNEN='001') is sent by the setting of the Host Token Endpoint Register (HOST_TOKEN), the SOF interrupt flag (INTR_USBHOST.SOFIRQ) is not set to '1' regardless of the setting of this bit. Default Value: 0
1	CANCEL	When this bit is set to '1', if the target token is written to the Host Token Endpoint Register (HOST_TOKEN) in the EOF area (specified in the Host EOF Setup Register), its sending is canceled. When this bit is set to '0', token sending is not canceled even if the target token is written to the register. The cancellation of token sending is detected by reading the TCAN bit of the Interrupt USB Host Register (INTR_USBHOST). '0' : Continues a token. '1' : Cancels a token. Default Value: 0
0	RETRY	If this bit is set to '1', the target token is retried if a NAK or error* occurs. Retry processing is performed after the time that is specified in the Host Retry Timer Setup Register (HOST_RTIMER). * : HOST_ERR.RERR='1', HOST_ERR.TOUT='1', HOST_ERR.CRC='1', HOST_ERR.TGERR='1', HOST_ERR.STUFF='1' '0' : Doesn't retry token sending. '1' : Retries token sending Note: - This bit isn't initialized even if the RST bit of the Host Control 1 Register (HOST_CTL1) is set to '1'. Default Value: 1

23.1.64 USBFS0_USBHOST_HOST_ERR

Host Error Status Register.

Address: 0x403F4104

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1S	
HW Access	W1S	W1S	W1S	W1S	W1S	W1S	W	
Name	LSTSOF	RERR	TOUT	CRC	TGERR	STUFF	HS [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	LSTSOF	If this bit is set to '1', it means that the SOF token can't be sent in the USB Host because other token is in process. When this bit is '0', it means that SOF token was sent with no error. Write '1' to clear, a write of '0' is ignored. '0' : SOF sent without error. '1' : SOF error detected. Note: - This bit is set to the default value when the RST bit of the Host Control 1 Register (HOST_CTL1) is set to '1'. Default Value: 0
6	RERR	When this bit is set to '1', it means that the received data exceeds the specified maximum number of packets in the USB Host. If a receive error is detected, bit5 (TOUT) of this register is also set to '1'. When this bit is '0', it means that no error is detected. Write '1' to clear, a write of '0' is ignored. '0' : No receive error. '1' : Maximum packet receive error detected. - This bit is set to the default value when the RST bit of the Host Control 1 Register (HOST_CTL1) is set to '1'. Default Value: 0

23.1.64 USBFS0_USBHOST_HOST_ERR (continued)

5	TOUT	If this bit is set to '1', it means that no response is returned from the device within the specified time after a token has been sent in the USB Host. When this bit is '0', it means that no timeout is detected. Write '1' to clear, a write of '0' is ignored. '0' : No timeout. '1' : Timeout has detected. Note: - This bit is set to the default value when the RST bit of the Host Control 1 Register (HOST_CTL1) is set to '1'. Default Value: 0
4	CRC	If this bit is set to '1', it means that a CRC error is detected in the USB Host. When this bit is '0', it means that no error is detected. If a CRC error is detected, bit5 (TOUT) of this register is also set to '1'. Write '1' to clear, a write of '0' is ignored. '0' : No CRC error. '1' : CRC error detected. Note: - This bit is set to the default value when the RST bit of the Host Control 1 Register (HOST_CTL1) is set to '1'. Default Value: 0
3	TGERR	If this bit is set to '1', it means that the data does not match the TGGL data. When this bit is '0', it means that no error is detected. Write '1' to clear, a write of '0' is ignored. '0' : No toggle error. '1' : Toggle error detected. Note: - This bit is set to the default value when the RST bit of the Host Control 1 Register (HOST_CTL1) is set to '1'. Default Value: 0
2	STUFF	If this bit is set to '1', it means that a bit stuffing error has been detected. When this bit is '0', it means that no error is detected. If a stuffing error is detected, bit5 (TOUT) of this register is also set to '1'. Write '1' to clear, a write of '0' is ignored. '0' : No stuffing error. '1' : Stuffing error detected. Note: - This bit is set to the default value when the RST bit of the Host Control 1 Register (HOST_CTL1) is set to '1'. Default Value: 0
1 : 0	HS	These flags indicate the status of a handshake packet to be sent or received. These flags are set to 'NULL' when no handshake occurs due to an error or when a SOF token has been ended with the TKNEN bit of the Host Token Endpoint Register (HOST_TOKEN). These bits are updated when sending or receiving has been ended. Write '11' to set the status back to 'NULL", all other write values are ignored. Note: This bit is set to the default value when the RST bit of the Host Control 1 Register (HOST_CTL1) is set to '1'. Default Value: 3 **0x0: ACK :** Acknowledge Packet **0x1: NAK :** Non-Acknowledge Packet

23.1.64 USBFS0_USBHOST_HOST_ERR (continued)

0x2: STALL :

Stall Packet

0x3: NULL :

Null Packet

23.1.65 USBFS0_USBHOST_HOST_STATUS

Host Status Register.

Address: 0x403F4108

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	RW1S	RW0C	RW	R	R
HW Access	RW	RW	RW	RW0C	RW	RW	RW	RW
Name	CLK-SEL_ST	RSTBUSY	RE-SERVED_5	URST	SOFBUSY	SUSP	TMODE	CSTAT

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							RW
Name	None [15:9]							HOST_ST

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	HOST_ST	This bit shows whether the device is in USB Host mode. If the HOST bit of the Host Control Register (HOST_CTL0) is set to '1', this bit is set to '1'. '0' : USB Device '1' : USB Host Notes: - If this bit is different from the HOST bit, The execution of a token must wait these bits match. - This bit takes time to be initialized by the RST bit of the Host Control 1 Resgiter (HOST_CTL1). Read this bit to confirm the operation is complete. Default Value: 0
7	CLKSEL_ST	This bit shows whether it is full-speed or not. If the CLKSEL bit of the Host Control 1 Register (HOST_CTL1) is set to '1', this bit is set to '1'. '0' : Low speed '1' : Full speed Note: - If this bit is different from the CLKSEL bit, The execution of the token and bus reset must wait these bits match. - This bit takes time to be initialized by the RST bit of the Host Control 1 Resgiter (HOST_CTL1). Read this bit to confirm the operation is complete. Default Value: 1

23.1.65 USBFS0_USBHOST_HOST_STATUS (continued)

6	RSTBUSY	This bit shows that USB Host is being reset internally. If the RST bit of the Host Control 1 Register (HOST_CTL1) is set to '1', this bit is set to '1'. If the RST bit of Host Control 1 Register (HOST_CTL1) is set to '0', this bit is set to '0'. '0' : USB Host isn't being reset. '1' : USB Host is being reset. Notes: - If this bit is '1', the a token must not be executed. - This bit isn't set to '0' or '1' immediately even if the RST bit of Host Control 1 Register (HOST_CTL1) is set to '0' or '1'. Read this bit to confirm the operation is complete. Default Value: 1
5	RESERVED_5	Reserved. Keep this bitfield at the default value. Default Value: 0
4	URST	When this bit is set to '1', the USB bus is reset. This bit remains a '1' during USB bus resetting, and changes to '0' when USB bus resetting is ended. If this bit is set to '0', the USB bus reset is complete Default Value: 0
3	SOFBUSY	When a SOF token is sent using the Host Token Endpoint Register (HOST_TOKEN), this bit is set to '1', which means that the SOF timer is active. When this bit is '0', it means that the SOF timer is under suspension. To stop the active SOF timer, write '0' to this bit. However, if this bit is written with '1', its value is ignored. '0' : The SOF timer is stopped. '1' : The SOF timer is active. Notes: - This bit is set to the initial value when the RST bit of the Host Control 1 Register (HOST_CTL1) is set to '1'. - This bit takes time to be initialized by the RST bit of the Host Control 1 Resgiter (HOST_CTL1). - The SOF timer does not stop immediately after this bit has been set to '0' to stop the SOF timer. To check whether or not the SOF timer is stopped, read this bit. Default Value: 0
2	SUSP	If this bit is set to '1', the USB Host is placed into the suspend state. If this bit is set to '0' while it is '1' or the USB bus is placed into the k-state mode, then suspend state is released, and the RWIRQ bit of the Interrupt USB Host Register (INTR_USBHOST) is set to '1'. Set to '1' : Suspend. Set '0' when this bit is '1' : Resume. Other conditions : Holds the status. Notes: - This bit is set to the default value when the RST bit of the Host Control 1 Register (HOST_CTL1) is set to '1'. - The transition to disconnected on RST isn't immediate. Read this bit to confirm the transition is complete. - If this bit is set to '1', this bit must not be set to '1' until the RWIRQ bit of the Interrupt USB Host Register (INTR_USBHOST) is set to '1'. - Do not set this bit to '1' while the USB is active (during USB bus resetting, data transfer, or SOF timer running). - If the value of this bit is changed, it is not immediately reflected on the state of the USB bus. To check whether or not the state is updated, read this bit. Default Value: 0

23.1.65 USBFS0_USBHOST_HOST_STATUS (continued)

1	TMODE	If this bit is '1', it means that the device is connected in the full-speed mode. When this bit is '0', it means that the device is connected in the low-speed mode. This bit is valid when the CSTAT bit of the Host Status Register (HOST_STATUS) is '1'. '0' : Low-speed. '1' : Full-speed. Notes: - This bit is set to the default value if the RST bit of the Host Control 1 Register (HOST_CTL1) is set to '1'. - The transition to disconnected on RST isn't immediate. Read this bit to confirm the transition is complete. Default Value: 1
0	CSTAT	When this bit is '1', it means that the device is connected. When this bit is '0', it means that the device is disconnected. '0' : Device is disconnected. '1' : Device is connected. Notes: - This bit is set to the default value if the RST bit of the Host Control 1 Register (Host_CTL1) is set to '1'. - The transition to disconnected on RST isn't immediate. Read this bit to confirm the transition is complete. Default Value: 0

23.1.66 USBFS0_USBHOST_HOST_FCOMP

Host SOF Interrupt Frame Compare Register

Address: 0x403F410C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	FRAMECOMP [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	FRAMECOMP	These bits are used to specify the data to be compared with the low-order eight bits of a frame number when sending a SOF token. If the SOFSTEP bit of Host Control 2 Register (HOST_CTL2) is '0', the frame number of SOF is compared with the value of this register when sending a SOF token. If they match, the SOFIRQ bit of the Interrupt USB Host Register (INTR_USBHOST) is set to '1'. The setting of this register is invalid when the SOFSTEP bit of Host Control 2 Register (HOST_CTL2) is '1'. Note: - This bit is not reset to default even if the RST bit of the Host Control 1 Register (HOST_CTL1) is set to '1'. Default Value: 0

23.1.67 USBFS0_USBHOST_HOST_RTIMER

Host Retry Timer Setup Register

Address: 0x403F4110

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	RTIMER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	RTIMER [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	
HW Access	None						R	
Name	None [23:18]						RTIMER [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
17 : 0	RTIMER	These bits are used to specify the retry time in this register. The retry timer is activated when token sending starts while the RETRY bit of Host Control 2 Register (HOST_CTL2) is '1'. The retry time is then decremented by one when a 1-bit transfer clock (12 MHz in the full-speed mode) is output. When the retry timer reaches 0, the target token is sent, and processing ends. If a token retry occurs in the EOF area, the retry timer is stopped until SOF sending is ended. After SOF sending has been completed, the retry timer restarts with the value that is set when the timer stopped. Default Value: 0

23.1.68 USBFS0_USBHOST_HOST_ADDR

Host Address Register

Address: 0x403F4114

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW						
HW Access	None	R						
Name	None	ADDRESS [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
6 : 0	ADDRESS	These bits are used to specify a token address. Note: - This bit is reset to default even if the RST bit of the Host Control 1 Register (HOST_CTL1) is set to '1'. Default Value: 0

23.1.69 USBFS0_USBHOST_HOST_EOF

Host EOF Setup Register

Address: 0x403F4118

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	EOF [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW					
HW Access	None		R					
Name	None [15:14]		EOF [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
13 : 0	EOF	These bits are used to specify the time to disable token sending before transferring SOF. Specify the time with a margin, which is longer than the one-packet length. The time unit is the 1-bit transfer time. Setting example: MAXPKT = 64 bytes, full-speed mode (Token_length + packet_length + header + CRC)*7/6 + Turn_around_time =(34 bit + 546 bit)*7/6 + 36 bit = 712.7 bit Therefore, set 0x2C9. Note: - This bit is not reset to default even if the RST bit of the Host Control 1 Register (HOST_CTL1) is set to '1'. Default Value: 0

23.1.70 USBFS0_USBHOST_HOST_FRAME

Host Frame Setup Register

Address: 0x403F411C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	FRAME [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW		
HW Access	None					RW		
Name	None [15:11]					FRAME [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10 : 0	FRAME	These bits are used to specify a frame number of SOF. Notes: - This bit isn't reset to default even if the RST bit of the Host Control 1 Register (HOST_CTL1) is set to '1'. - Specify a frame number in this register before setting SOF in the TKNEN bit of the Host Token Endpoint Register (HOST_TOKEN). - This register cannot be written while the SOFBUSY bit of the Host Status Register (HOST_STATUS) is '1' and a SOF token is in process. Default Value: 0

23.1.71 USBFS0_USBHOST_HOST_TOKEN

Host Token Endpoint Register

Address: 0x403F4120

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			RW			
HW Access	None	RW0C			R			
Name	None	TKNEN [6:4]			ENDPT [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							TGGL

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	TGGL	This bit is used to set toggle data. Toggle data is sent depending on the setting of this bit. When receiving toggle data, received toggle data is compared with the toggle data of this bit to verify whether or not an error occurs. '0' : DATA0 '1' : DATA1 Notes: - This bit isn't reset to the default value even if the RST bit of the Host Control 1 Register (HOST_CTL1) is set to '1'. - Set this bit when the TKNEN bit of the Host Token Endpoint Register (HOST_TOKEN) is '000'. Default Value: 0

23.1.71 USBFS0_USBHOST_HOST_TOKEN (continued)

6 : 4	TKNEN	These bits send a token according to the current settings. After operation is complete, the TKNEN bit is set to '000', and the CMPIRQ bit of the Interrupt USB Host Register (INTR_USB-HOST) is set to '1'. The settings of the TGGL and ENDPT bits are ignored when sending a SOF token. Notes: - This bit is set to the default value when the RST bit of the Host Control 1 Register (HOST_CTL1) is set to '1'. - The PRE packet isn't supported. - Do not set '100' to the TKNEN bit when the SOFBUSY bit of the Host Status Register (HOST_STATUS) is '1' - Mode should be USB Host before writing data to this bit. - When issuing a token again after the token interrupt flag (CMPIRQ) has been set to '1', wait for 3 cycles or more after a USB transfer clock (12 MHz in the full-speed mode, 1.5 MHz in the low-speed mode) was output, then write data to this bit. - Read the value of TKNEN bit if a new value is written in it .Continue writing in this bit until a retrieved value equals a new value written in. During this checking process, it is needed to pre-vent any interrupt. - Take the following steps when CMPIRQ bit of Interrupt USB Host Register (INTR_USBHOST) is set to '1' by finishing IN token or Isochronous IN token. 1. Read HS bit of Host Error Status Register (HOST_ERR), then set CMPIRQ bit to '0'. 2. Set EPn bit of Host DMA Enable Register (HOST_DMA_ENBL) (n=1 or 2) to '1' if HS bit of Host Error Status Register (HOST_ERR) is equal to '00' and wait until EPn bit of Host DMA Data Request Register (HOST_DMA_DREQ) changes to '1'. Finish the IN token processing if HS bit is not equal to '00'. 3. Read the received data if EPn bit of Host DMA Data Requet (HOST_DMA_DREQ) (n=1 or 2) changes to '1'. Default Value: 0 **0x0: NONE :** Sends no data. **0x1: SETUP :** Sends SETUP token. **0x2: IN :** Sends IN token. **0x3: OUT :** Sends OUT token. **0x4: SOF :** Sends SOF token. **0x5: ISO_IN :** Sends Isochronous IN.

23.1.71 USBFS0_USBHOST_HOST_TOKEN (continued)

		0x6: ISO_OUT : Sends Isochronous OUT. **0x7: RSV :** Reserved.
3 : 0	ENDPT	These bits are used to specify an endpoint to send or receive data to or from the device. Note: - This bit isn't reset to default even if the RST bit of the Host Control 1 Register (HOST_CTL1) is set to '1'. Default Value: 0

23.1.72 USBFS0_USBHOST_HOST_EP1_CTL

Host Endpoint 1 Control Register

Address: 0x403F4400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	PKS1 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW	None		RW	RW	RW	None	RW
HW Access	RW1S	None		R	R	R	None	R
Name	BFINI	None [14:13]		DIR	DMAE	NULLE	None	PKS1

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15	BFINI	This bit initializes the send/receive buffer of transfer data. The BFINI bit is also automatically set by setting the RST bit of the HOST Control 1 Register (HOST_CTL1). If the RST bit was used for resetting, therefore, set the RST bit to "0" before clearing the BFINI bit. '0' : Clears the initialization. '1' : Initializes the send/receive buffer Note : - The EP1 buffer has a double-buffer configuration. The BFINI bit initialization initializes the double buffers concurrently and also initializes the EP1DRQ and EP1SPK bits. Default Value: 1
12	DIR	This bit specifies the transfer direction the Endpoint support. '0' : IN Endpoint. '1' : OUT Endpoint Note: - This bit must be changed when INI_ST bit of the Host Endpoint 1 Status Register (HOST_EP1_STATUS) is '1'. Default Value: 0

23.1.72 USBFS0_USBHOST_HOST_EP1_CTL (continued)

11	DMAE	This bit sets a mode that uses DMA for writing or reading transfer data to/from send/receive buffer, and automatically transfers the send/receive data synchronized with an data request in the IN or OUT direction. Until the data size set in the DMA is reached, the data is transferred. '0' : Releases the packet transfer mode. '1' : Sets the packet transfer mode. Note : - The CPU must not access the send/receive buffer while the DMAE bit is set to '1'. For data transfer in the IN direction, set the DMA transfer size to the multiples of that set in PKS1 bits of the Host EP1 Control Register (HOST_EP1_CTL) and Host EP2 Control Register (HOST_EP2_CTR). Default Value: 0
10	NULLE	When a data transfer request in OUT the direction is transmitted while automatic buffer transfer mode is set (DMAE = 1), this bit sets a mode that transfers 0-byte data automatically upon the detection of the last packet transfer. '0' : Releases the NULL automatic transfer mode. '1' : Sets the NULL automatic transfer mode. Note : - For data transfer in the IN direction or when automatic buffer transfer mode is not set, the NULL bit configuration does not affect communication. Default Value: 0
8 : 0	PKS1	This bit specifies the maximum size transferred by one packet. The configurable range is from 0x001 to 0x100. - If automatic buffer transfer mode (DMAE='1') is used, Endpoint 0,1, or 2 cannot be used, Default Value: 256

23.1.73 USBFS0_USBHOST_HOST_EP1_STATUS

Host Endpoint 1 Status Register

Address: 0x403F4404

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	SIZE1 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							RW
Name	None [15:9]							SIZE1

Bits	23	22	21	20	19	18	17	16
SW Access	None					R	R	R
HW Access	None					RW	RW	RW
Name	None [23:19]					RE-SERVED_18	INI_ST	VAL_DATA

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
18	RESERVED_18	Reserved. Keep this bitfield at the default value. Default Value: 1
17	INI_ST	This bit shows that EP1 is initialized. If the init bit of the Host Endpoint 1 Control Register (HOST_EP1_CTL) is set to '1' and EP1 is initialized, this bit is to '1'. '0' : Not initiatialized '1' : Initialized Note: - This bit isn't set to '0' or '1' immediately even if BFINI bit of the Host Endpoint 1 Control Register (HOST_EP1_CTL) is set to '0' or '1'. Read this bit to confirm the transition. Default Value: 1
16	VAL_DATA	This bit shows that there is valid data in the EP1 buffer. '0' : Invalid data in the buffer '1' : Valid data in the buffer Default Value: 0

23.1.73 USBFS0_USBHOST_HOST_EP1_STATUS (continued)

8 : 0	SIZE1	These bits indicate the number of data bytes written to the receive buffer when IN packet transfer of EP1 has finished. The indication range is from 0x000 to 0x100. Note : - These bits are set to the data size transferred in the IN direction and written to the buffer. Therefore, a value read during transfer in the OUT direction has no effect. Default Value: X

23.1.74 USBFS0_USBHOST_HOST_EP1_RW1_DR

Host Endpoint 1 Data 1-Byte Register

Address: 0x403F4408

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	BFDT8 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	BFDT8	Data Register for EP1 for 1-byte data Default Value: 0

23.1.75 USBFS0_USBHOST_HOST_EP1_RW2_DR

Host Endpoint 1 Data 2-Byte Register

Address: 0x403F440C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	BFDT16 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	BFDT16 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	BFDT16	Data Register for EP1 for 2-byte data Default Value: 0

23.1.76 USBFS0_USBHOST_HOST_EP2_CTL

Host Endpoint 2 Control Register

Address: 0x403F4500

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW						
HW Access	None	R						
Name	None	PKS2 [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	RW	None		RW	RW	RW	None	
HW Access	RW1S	None		R	R	R	None	
Name	BFINI	None [14:13]		DIR	DMAE	NULLE	None [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15	BFINI	This bit initializes the send/receive buffer of transfer data. The BFINI bit is also automatically set by setting the RST bit of the HOST Control 1 Register (HOST_CTL1). If the RST bit was used for resetting, therefore, set the RST bit to '0' before clearing the BFINI bit. '0' : Clears the initialization. '1' : Initializes the send/receive buffer Note : - The EP2 buffer has a double-buffer configuration. The BFINI bit initialization initializes the double buffers concurrently and also initializes the EP2DRQ and EP2SPK bits. Default Value: 1
12	DIR	This bit specifies the transfer direction the Endpoint support. '0' : IN Endpoint. '1' : OUT Endpoint Note: - This bit must be changed when INI_ST bit of the Host Endpoint 2 Status Register (HOST_EP2_STATUS) is '1'. Default Value: 0

23.1.76 USBFS0_USBHOST_HOST_EP2_CTL (continued)

11	DMAE	This bit sets a mode that uses DMA for writing or reading transfer data to/from send/receive buffer, and automatically transfers the send/receive data synchronized with an data request in the IN or OUT direction. Until the data size set in the DMA is reached, the data is transferred. '0' : Releases the automatic buffer transfer mode. '1' : Sets the automatic buffer transfer mode. Note : - The CPU must not access the send/receive buffer while the DMAE bit is set to '1'. For data transfer in the IN direction, set the DMA transfer size to the multiples of that set in PKS bits of the Host EP1 Control Register (HOST_EP1_CTL) and Host EP2 Control Register (HOST_EP2_CTR). Default Value: 0
10	NULLE	When a data transfer request in the OUT direction transmitted while packet transfer mode is set (DMAE = 1), this bit sets a mode that transfers 0-byte data automatically upon the detection of the last packet transfer. '0' : Releases the NULL automatic transfer mode. '1' : Sets the NULL automatic transfer mode. Note : - For data transfer in the IN direction or when automatic buffer transfer mode is not set, the NULL bit configuration does not affect communication. Default Value: 0
6 : 0	PKS2	This bit specifies the maximum size transferred by one packet. The configurable range is from 0x001 to 0x40. - If automatic buffer transfer mode (DMAE='1') is used, this Endpoint must not set from 0 to 2. Default Value: 64

23.1.77 USBFS0_USBHOST_HOST_EP2_STATUS

Host Endpoint 2 Status Register

Address: 0x403F4504

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	R						
HW Access	None	RW						
Name	None	SIZE2 [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None					R	R	R
HW Access	None					RW	RW	RW
Name	None [23:19]					RE-SERVED_18	INI_ST	VAL_DATA

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
18	RESERVED_18	Reserved. Keep this bitfield at the default value. Default Value: 1
17	INI_ST	This bit shows that EP2 is initialized. If the BFINI bit of the Host Endpoint 2 Control Register (HOST_EP2_CTL) is set to '1' and EP2 is initialized, this bit is to '1'. '0' : Not Initialized '1' : Initialized Note: - This bit isn't set to '0' or '1' immediately evne if BFINI bit of the Host Endpoint 2 Control Register (HOST_EP2_CTL) is set to '0' or '1'. Default Value: 1
16	VAL_DATA	This bit shows that there is valid data in the EP2 buffer. '0' : Invalid data in the buffer '1' : Valid data in the buffer Default Value: 0

23.1.77 USBFS0_USBHOST_HOST_EP2_STATUS (continued)

6 : 0	SIZE2	These bits indicate the number of data bytes written to the receive buffer when IN packet transfer of EP2 has finished. The indication range is from 0x000 to 0x40. Note : - These bits are set to the data size transferred in the IN direction and written to the buffer. Therefore, a value read during transfer in the OUT direction has no effect. Default Value: X

23.1.78 USBFS0_USBHOST_HOST_EP2_RW1_DR

Host Endpoint 2 Data 1-Byte Register

Address: 0x403F4508

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	BFDT8 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	BFDT8	Data Register for EP2 for 1-byte data. Default Value: 0

23.1.79 USBFS0_USBHOST_HOST_EP2_RW2_DR

Host Endpoint 2 Data 2-Byte Register

Address: 0x403F450C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	BFDT16 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	BFDT16 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	BFDT16	Data Register for EP2 for 2 byte data. Default Value: 0

23.1.80 USBFS0_USBHOST_HOST_LVL1_SEL

Host Interrupt Level 1 Selection Register

Address: 0x403F4800

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	CMPIRQ_SEL [7:6]		CNNIRQ_SEL [5:4]		DIRQ_SEL [3:2]		SOFIRQ_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	TCAN_SEL [15:14]		RESERVED_13_12 [13:12]		RWKIRQ_SEL [11:10]		URIRQ_SEL [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 14	TCAN_SEL	These bits assign TCAN interrupt flag to selected interrupt signals. Default Value: 0
13 : 12	RESERVED_13_12	Reserved. Keep this bitfield at the default value. Default Value: 0
11 : 10	RWKIRQ_SEL	These bits assign RWKIRQ interrupt flag to selected interrupt signals. Default Value: 0
9 : 8	URIRQ_SEL	These bits assign URIRQ interrupt flag to selected interrupt signals. Default Value: 0
7 : 6	CMPIRQ_SEL	These bits assign URIRQ interrupt flag to selected interrupt signals. Default Value: 0
5 : 4	CNNIRQ_SEL	These bits assign CNNIRQ interrupt flag to selected interrupt signals. Default Value: 0
3 : 2	DIRQ_SEL	These bits assign DIRQ interrupt flag to selected interrupt signals. Default Value: 0
1 : 0	SOFIRQ_SEL	These bits assign SOFIRQ interrupt flag to selected interrupt signals. Default Value: 0

23.1.80 USBFS0_USBHOST_HOST_LVL1_SEL (continued)

0x0: HI :

High priority interrupt

0x1: MED :

Medium priority interrupt

0x2: LO :

Low priority interrupt

0x3: RESERVED :

Reserved.

23.1.81 USBFS0_USBHOST_HOST_LVL2_SEL

Host Interrupt Level 2 Selection Register

Address: 0x403F4804

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		None			
HW Access	R		R		None			
Name	EP1_SPK_SEL [7:6]		EP1_DRQ_SEL [5:4]		None [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW		RW	
HW Access	None				R		R	
Name	None [15:12]				EP2_SPK_SEL [11:10]		EP2_DRQ_SEL [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11 : 10	EP2_SPK_SEL	These bits assign EP2_SPK interrupt flag to selected interrupt signals. Default Value: 0
9 : 8	EP2_DRQ_SEL	These bits assign EP2_DRQ interrupt flag to selected interrupt signals. Default Value: 0
7 : 6	EP1_SPK_SEL	These bits assign EP1_SPK interrupt flag to selected interrupt signals. Default Value: 0
5 : 4	EP1_DRQ_SEL	These bits assign EP1_DRQ interrupt flag to selected interrupt signals. Default Value: 0 **0x0: HI :** High priority interrupt **0x1: MED :** Medium priority interrupt

23.1.81 USBFS0_USBHOST_HOST_LVL2_SEL (continued)

0x2: LO :

Low priority interrupt

0x3: RESERVED :

Reserved.

23.1.82 USBFS0_USBHOST_INTR_USBHOST_CAUSE_HI

Interrupt USB Host Cause High Register

Address: 0x403F4900

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	TCAN_INT	RE-SERVED_6	RWKIRQ_INT	URIRQ_INT	CM-PIRQ_INT	CN-NIRQ_INT	DIRQ_INT	SO-FIRQ_INT

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	TCAN_INT	TCAN interrupt Default Value: 0
6	RESERVED_6	Reserved. Default Value: 0
5	RWKIRQ_INT	RWKIRQ interrupt Default Value: 0
4	URIRQ_INT	URIRQ interrupt Default Value: 0
3	CMPIRQ_INT	CMPIRQ interrupt Default Value: 0
2	CNNIRQ_INT	CNNIRQ interrupt Default Value: 0
1	DIRQ_INT	DIRQ interrupt Default Value: 0

23.1.82 USBFS0_USBHOST_INTR_USBHOST_CAUSE_HI (continued)

0	SOFIRQ_INT	SOFIRQ interrupt Default Value: 0

23.1.83 USBFS0_USBHOST_INTR_USBHOST_CAUSE_MED

Interrupt USB Host Cause Medium Register

Address: 0x403F4904

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	TCAN_INT	RE-SERVED_6	RWKIRQ_INT	URIRQ_INT	CM-PIRQ_INT	CN-NIRQ_INT	DIRQ_INT	SO-FIRQ_INT

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	TCAN_INT	TCAN interrupt Default Value: 0
6	RESERVED_6	Reserved. Default Value: 0
5	RWKIRQ_INT	RWKIRQ interrupt Default Value: 0
4	URIRQ_INT	URIRQ interrupt Default Value: 0
3	CMPIRQ_INT	CMPIRQ interrupt Default Value: 0
2	CNNIRQ_INT	CNNIRQ interrupt Default Value: 0
1	DIRQ_INT	DIRQ interrupt Default Value: 0

23.1.83 USBFS0_USBHOST_INTR_USBHOST_CAUSE_MED (continued)

0	SOFIRQ_INT	SOFIRQ interrupt Default Value: 0

23.1.84 USBFS0_USBHOST_INTR_USBHOST_CAUSE_LO

Interrupt USB Host Cause Low Register

Address: 0x403F4908

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	TCAN_INT	RE-SERVED_6	RWKIRQ_INT	URIRQ_INT	CM-PIRQ_INT	CN-NIRQ_INT	DIRQ_INT	SO-FIRQ_INT

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	TCAN_INT	TCAN interrupt Default Value: 0
6	RESERVED_6	Reserved. Default Value: 0
5	RWKIRQ_INT	RWKIRQ interrupt Default Value: 0
4	URIRQ_INT	URIRQ interrupt Default Value: 0
3	CMPIRQ_INT	CMPIRQ interrupt Default Value: 0
2	CNNIRQ_INT	CNNIRQ interrupt Default Value: 0
1	DIRQ_INT	DIRQ interrupt Default Value: 0

23.1.84 USBFS0_USBHOST_INTR_USBHOST_CAUSE_LO (continued)

0	SOFIRQ_INT	SOFIRQ interrupt Default Value: 0

23.1.85 USBFS0_USBHOST_INTR_HOST_EP_CAUSE_HI

Interrupt USB Host Endpoint Cause High Register

Address: 0x403F4920

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R	R	R	R	None	
HW Access	None		W	W	W	W	None	
Name	None [7:6]		EP2SP-K_INT	EP2DRQ_INT	EP1SP-K_INT	EP1DRQ_INT	None	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	EP2SPK_INT	EP2SPK interrupt Default Value: 0
4	EP2DRQ_INT	EP2DRQ interrupt Default Value: 0
3	EP1SPK_INT	EP1SPK interrupt Default Value: 0
2	EP1DRQ_INT	EP1DRQ interrupt Default Value: 0

23.1.86 USBFS0_USBHOST_INTR_HOST_EP_CAUSE_MED

Interrupt USB Host Endpoint Cause Medium Register

Address: 0x403F4924

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R	R	R	R	None	
HW Access	None		W	W	W	W	None	
Name	None [7:6]		EP2SP-K_INT	EP2DRQ_INT	EP1SP-K_INT	EP1DRQ_INT	None	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	EP2SPK_INT	EP2SPK interrupt Default Value: 0
4	EP2DRQ_INT	EP2DRQ interrupt Default Value: 0
3	EP1SPK_INT	EP1SPK interrupt Default Value: 0
2	EP1DRQ_INT	EP1DRQ interrupt Default Value: 0

23.1.87 USBFS0_USBHOST_INTR_HOST_EP_CAUSE_LO

Interrupt USB Host Endpoint Cause Low Register

Address: 0x403F4928

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R	R	R	R	None	
HW Access	None		W	W	W	W	None	
Name	None [7:6]		EP2SP-K_INT	EP2DRQ_INT	EP1SP-K_INT	EP1DRQ_INT	None	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	EP2SPK_INT	EP2SPK interrupt Default Value: 0
4	EP2DRQ_INT	EP2DRQ interrupt Default Value: 0
3	EP1SPK_INT	EP1SPK interrupt Default Value: 0
2	EP1DRQ_INT	EP1DRQ interrupt Default Value: 0

23.1.88 USBFS0_USBHOST_INTR_USBHOST

Interrupt USB Host Register

Address: 0x403F4940

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	W1S	W1S	W1S	W1S	W1S	W1S	W1S	W1S
Name	TCAN	RESERVED_6	RWKIRQ	URIRQ	CMPIRQ	CNNIRQ	DIRQ	SOFIRQ

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	TCAN	If this bit is set to '1', it means that token sending is canceled based on the setting of the CANCEL bit of Host Control 2 Register (HOST_CTL2). When this bit is '0', it means that token sending is not canceled. Write '1' to clear, a write of '0' is ignored. '0' : Does not cancel token sending. '1' : Cancels token sending. Note : - This bit is set to the default value when the RST bit of the Host Control 1 Register (HOST_CTL1) is set to '1'. Default Value: 0
6	RESERVED_6	Reserved. Default Value: 0

23.1.88 USBFS0_USBHOST_INTR_USBHOST (continued)

5	RWKIRQ	If this bit is set to '1', it means that remote Wake-up is ended. When this bit is '0', it has no meaning. Write '1' to clear, a write of '0' is ignored. '0' : Issues no interrupt request by restart. '1' : Issues an interrupt request by restart. Note : - This bit is set to the default value when the RST bit of the Host Control 1 Register (HOST_CTL1) is set to '1'. Default Value: 0
4	URIRQ	If this bit is set to '1', it means that USB bus resetting is ended. When this bit is '0', it has no meaning. If this bit is written with '1', it is set to '0'. However, if this bit is written with '0', its value is ignored. '0' : Issues no interrupt request by USB bus resetting. '1' : Issues an interrupt request by USB bus resetting. Note : - This bit is set to the initial value when the RST bit of the Host Control 1 Register (HOST_CTL1) is set to '1'. Default Value: 0
3	CMPIRQ	If this bit is set to '1', it means that a token is completed. When this bit is '0', it has no meaning. Write '1' to clear, a write of '0' is ignored. '0' : Issues no interrupt request by token completion. '1' : Issues an interrupt request by token completion. Note : - This bit is set to the initial value when the RST bit of the Host Control 1 Register (HOST_CTL1) is set to '1'. - This bit is not set to '1' even if the TCAN bit of the Interrupt USBHost Register (INTR_USBHOST) changes to '1'. - Take the following steps when this bit is set to '1' by finishing IN token or Isochronous IN token. 1. Read HS bit of Host Error Status Register (HOST_ERR), then set CMPIRQ bit to '0'. 2. Set EPn bit of Host DMA Enable Register (HOST_DMA_ENBL) (n=1 or 2) to '1' if HS bit of Host Error Status Register (HOST_ERR) is equal to '00' and wait until EPn bit of Host DMA Data Request Register (HOST_DMA_DREQ) changes to '1'. Finish the IN token processing if HS bit is not equal to '00'. 3. Read the received data if EPn bit of Host DMA Data Requet (HOST_DMA_DREQ) (n=1 or 2) changes to '1'. Default Value: 0
2	CNNIRQ	If this bit is set to '1', it means that a device connection is detected. When this bit is '0', it has no meaning. Write '1' to clear, a write of '0' is ignored. '0' : Issues no interrupt request by detecting a device connection. '1' : Issues an interrupt request by detecting a device connection. Note : - This bit is set to the default value when the RST bit of the Host Control 1 Register (HOST_CTL1) is set to '1'. Default Value: 0
1	DIRQ	If this bit is set to '1', it means that a device disconnection is detected. When this bit is '0', it has no meaning. Write '1' to clear, a write of '0' is ignored. '0' : Issues no interrupt request by detecting a device disconnection. '1' : Issues an interrupt request by detecting a device disconnection. Note : - This bit is set to the default value when the RST bit of the Host Control 1 Register (HOST_CTL1) is set to '1'. Default Value: 0

23.1.88 USBFS0_USBHOST_INTR_USBHOST (continued)

0	SOFIRQ	If this bit is set to '1', it means that SOF token sending is started. When this bit is '0', it has no meaning. Write '1' to clear, a write of '0' is ignored. '0' : Does not issue an interrupt request by starting a SOF token. '1' : Issues an interrupt request by starting a SOF token. Note : - This bit is set to the default value when the RST bit of the Host Control 1 Register (HOST_CTL1) is set to '1'. Default Value: 0

23.1.89 USBFS0_USBHOST_INTR_USBHOST_SET

Interrupt USB Host Set Register

Address: 0x403F4944

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	A	A	A	A	A	A	A	A
Name	TCANS	RE-SERVED_6	RWKIRQS	URIRQS	CMPIRQS	CNNIRQS	DIRQS	SOFIRQS

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	TCANS	This bit sets TCAN bit. If this bit is written to '1', TCAN is set to '1'. However, if this bit is written with '0', its value is ignored. Default Value: 0
6	RESERVED_6	Reserved. Keep this bitfield at the default value. Default Value: 0
5	RWKIRQS	This bit sets RWKIRQ bit. If this bit is written to '1', RWKIRQ is set to '1'. However, if this bit is written with '0', its value is ignored. Default Value: 0
4	URIRQS	This bit sets URIRQ bit. If this bit is written to '1', URIRQ is set to '1'. However, if this bit is written with '0', its value is ignored. Default Value: 0
3	CMPIRQS	This bit sets CMPIRQ bit. If this bit is written to '1', CMPIRQ is set to '1'. However, if this bit is written with '0', its value is ignored. Default Value: 0
2	CNNIRQS	This bit sets CNNIRQ bit. If this bit is written to '1', CNNIRQ is set to '1'. However, if this bit is written with '0', its value is ignored. Default Value: 0

23.1.89 USBFS0_USBHOST_INTR_USBHOST_SET (continued)

1	DIRQS	This bit sets DIRQ bit. If this bit is written to '1', DIRQ is set to '1'. However, if this bit is written with '0', its value is ignored. Default Value: 0
0	SOFIRQS	This bit sets SOFIRQ bit. If this bit is written to '1', SOFIRQ is set to '1'. However, if this bit is written with '0', its value is ignored. Default Value: 0

23.1.90 USBFS0_USBHOST_INTR_USBHOST_MASK

Interrupt USB Host Mask Register

Address: 0x403F4948

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	TCANM	RE-SERVED_6	RWKIRQM	URIRQM	CMPIRQM	CNNIRQM	DIRQM	SOFIRQM

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	TCANM	This bit masks the interrupt by TCAN flag. '0' : Disables '1' : Enables Default Value: 0
6	RESERVED_6	Reserved. Keep this bitfield at the default value. Default Value: 0
5	RWKIRQM	This bit masks the interrupt by RWKIRQ flag. '0' : Disables '1' : Enables Default Value: 0
4	URIRQM	This bit masks the interrupt by URIRQ flag. '0' : Disables '1' : Enables Default Value: 0

23.1.90 USBFS0_USBHOST_INTR_USBHOST_MASK (continued)

3	CMPIRQM	This bit masks the interrupt by CMPIRQ flag. '0' : Disables '1' : Enables Default Value: 0
2	CNNIRQM	This bit masks the interrupt by CNNIRQ flag. '0' : Disables '1' : Enables Default Value: 0
1	DIRQM	This bit masks the interrupt by DIRQ flag. '0' : Disables '1' : Enables Default Value: 0
0	SOFIRQM	This bit masks the interrupt by SOF flag. '0' : Disables '1' : Enables Default Value: 0

23.1.91 USBFS0_USBHOST_INTR_USBHOST_MASKED

Interrupt USB Host Masked Register

Address: 0x403F494C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	TCANED	RE-SERVED_6	RWKIRQED	URIRQED	CMPIRQED	CNNIRQED	DIRQED	SOFIRQED

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	TCANED	This bit indicates the interrupt by TCAN flag. '0' : Doesn't request the interrupt by TCAN '1' : Request the interrupt by TCAN Default Value: 0
6	RESERVED_6	Reserved. Default Value: 0
5	RWKIRQED	This bit indicates the interrupt by RWKIRQ flag. '0' : Doesn't request the interrupt by RWKIRQ '1' : Request the interrupt by RWKIRQ Default Value: 0
4	URIRQED	This bit indicates the interrupt by URIRQ flag. '0' : Doesn't request the interrupt by URIRQ '1' : Request the interrupt by URIRQ Default Value: 0

23.1.91 USBFS0_USBHOST_INTR_USBHOST_MASKED (continued)

3	CMPIRQED	This bit indicates the interrupt by CMPIRQ flag. '0' : Doesn't request the interrupt by CMPIRQ '1' : Request the interrupt by CMPIRQ Default Value: 0
2	CNNIRQED	This bit indicates the interrupt by CNNIRQ flag. '0' : Doesn't request the interrupt by CNNIRQ '1' : Request the interrupt by CNNIRQ Default Value: 0
1	DIRQED	This bit indicates the interrupt by DIRQ flag. '0' : Doesn't request the interrupt by DIRQ '1' : Request the interrupt by DIRQ Default Value: 0
0	SOFIRQED	This bit indicates the interrupt by SOF flag. '0' : Doesn't request the interrupt by SOF '1' : Request the interrupt by SOF Default Value: 0

23.1.92 USBFS0_USBHOST_INTR_HOST_EP

Interrupt USB Host Endpoint Register

Address: 0x403F4A00

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW1C	RW1C	RW1C	RW1C	None	
HW Access	None		W1S	W1S	W1S	W1S	None	
Name	None [7:6]		EP2SPK	EP2DRQ	EP1SPK	EP1DRQ	None	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	EP2SPK	This bit indicates that the data size transferred from the host does not satisfy the maximum packet size (including 0-byte) set by PKS1 in the Host Endpoint 2 Control Register (HOST_EP2_CTL) when the data has been received successfully. This bit is an interrupt cause, and writing '0' is ignored. Clear it by writing '1'. '0' : Received data size satisfies the maximum packet size '1' : Received data size does not satisfy the maximum packet size Note : - The SPK bit is not set during data transfer in the OUT direction. Default Value: 0

23.1.92 USBFS0_USBHOST_INTR_HOST_EP (continued)

4	EP2DRQ	This bit indicates that the EP2 packet transfer has normally ended, and processing of the data is required. The DRQ bit is an interrupt cause, and writing '0' is ignored. Clear the DRQ bit by writing '1'. '0' : Clears the interrupt cause '1' : Packet transfer normally ended Note : - If packet transfer mode (DMAE = '1') is not used, '1' must be written to the DRQ bit after data has been written or read to/from the send/receive buffer. Switch the access buffers once the DRQ bit is cleared. That DRQ = '0' may not be read after the DRQ bit is cleared. If the transfer direction is set to OUT, and the DRQ bit is cleared without writing buffer data while the DRQ bit is '1', it implies that 0-byte data is set. If DIR of the Host Endpoint 2 Control Register (HOST_EP2_CTL) is set to '1' at initial settings, the DRQ bit of corresponding Endpoint is set at the same time. Also while the DRQ bit is not set, '1' must not be written. Default Value: 0
3	EP1SPK	This bit indicates that the data size transferred from the host does not satisfy the maximum packet size (including 0-byte) set by PKS in the Host Endpoint 1 Control Register (HOST_EP1_CTL) when the data has been received successfully. This bit is an interrupt cause, and writing '0' is ignored. Clear it by writing '1'. '0' : Received data size satisfies the maximum packet size '1' : Received data size does not satisfy the maximum packet size Note : - The EP1SPK bit is not set during data transfer in the OUT direction. Default Value: 0
2	EP1DRQ	This bit indicates that the EP1 packet transfer has normally ended, and processing of the data is required. The DRQ bit is an interrupt cause, and writing '0' is ignored. Clear the DRQ bit by writing '1'. '0' : Clears the interrupt cause '1' : Packet transfer normally ended Note : - If automatic buffer transfer mode (DMAE = '1') is not used, '1' must be written to the DRQ bit after data has been written or read to/from the send/receive buffer. Switch the access buffers once the DRQ bit is cleared. That DRQ = '0' may not be read after the DRQ bit is cleared. If the transfer direction is set to OUT, and the DRQ bit is cleared without writing buffer data while the DRQ bit is '1', it implies that 0-byte data is set. If DIR of the Host Endpoint 1 Control Register (HOST_EP1_CTL) is set to '1' at initial settings, the DRQ bit of corresponding Endpoint is set at the same time. Also while the DRQ bit is not set, '1' must not be written. Default Value: 0

23.1.93 USBFS0_USBHOST_INTR_HOST_EP_SET

Interrupt USB Host Endpoint Set Register

Address: 0x403F4A04

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW1S	RW1S	RW1S	RW1S	None	
HW Access	None		A	A	A	A	None	
Name	None [7:6]		EP2SPKS	EP2DRQS	EP1SPKS	EP1DRQS	None	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	EP2SPKS	This bit sets EP2SPK bit. If this bit is written to '1', EP2SPK is set to '1'. However, if this bit is written with '0', its value is ignored. Note: If BFINI bit of the Host Endpoint 2 Control Register (HOST_EP2_CTL) is '1', EP2SPK can't be set to '1'. Default Value: 0
4	EP2DRQS	This bit sets EP2DRQ bit. If this bit is written to '1', EP2DRQ is set to '1'. However, if this bit is written with '0', its value is ignored. Note: If BFINI bit of the Host Endpoint 2 Control Register (HOST_EP2_CTL) is '1', EP2DRQ can't be set to '1'. Default Value: 0
3	EP1SPKS	This bit sets EP1SPK bit. If this bit is written to '1', EP1SPK is set to '1'. However, if this bit is written with '0', its value is ignored. Note: If BFINI bit of the Host Endpoint 1 Control Register (HOST_EP1_CTL) is '1', EP1SPK can't be set to '1'. Default Value: 0

23.1.93 USBFS0_USBHOST_INTR_HOST_EP_SET (continued)

2	EP1DRQS	This bit sets EP1DRQ bit. If this bit is written to '1', EP1DRQ is set to '1'. However, if this bit is written with '0', its value is ignored. Note: If BFINI bit of the Host Endpoint 1 Control Register (HOST_EP1_CTL) is '1', EP1DRQ can't be set to '1'. Default Value: 0

23.1.94 USBFS0_USBHOST_INTR_HOST_EP_MASK

Interrupt USB Host Endpoint Mask Register

Address: 0x403F4A08

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	RW	RW	None	
HW Access	None		R	R	R	R	None	
Name	None [7:6]		EP2SPKM	EP2DRQM	EP1SPKM	EP1DRQM	None	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	EP2SPKM	This bit masks the interrupt by EP2SPK flag. '0' : Disables '1' : Enables Default Value: 0
4	EP2DRQM	This bit masks the interrupt by EP2DRQ flag. '0' : Disables '1' : Enables Default Value: 0
3	EP1SPKM	This bit masks the interrupt by EP1SPK flag. '0' : Disables '1' : Enables Default Value: 0
2	EP1DRQM	This bit masks the interrupt by EP1DRQ flag. '0' : Disables '1' : Enables Default Value: 0

23.1.95 USBFS0_USBHOST_INTR_HOST_EP_MASKED

Interrupt USB Host Endpoint Masked Register

Address: 0x403F4A0C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R	R	R	R	None	
HW Access	None		RW	RW	RW	RW	None	
Name	None [7:6]		EP2SPKED	EP2DRQED	EP1SPKED	EP1DRQED	None	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	EP2SPKED	This bit indicates the interrupt by EP2SPK flag. '0' : Doesn't request the interrupt by EP2SPK '1' : Request the interrupt by EP2SPK Default Value: 0
4	EP2DRQED	This bit indicates the interrupt by EP2DRQ flag. '0' : Doesn't request the interrupt by EP2DRQ '1' : Request the interrupt by EP2DRQ Default Value: 0
3	EP1SPKED	This bit indicates the interrupt by EP1SPK flag. '0' : Doesn't request the interrupt by EP1SPK '1' : Request the interrupt by EP1SPK Default Value: 0
2	EP1DRQED	This bit indicates the interrupt by EP1DRQ flag. '0' : Doesn't request the interrupt by EP1DRQ '1' : Request the interrupt by EP1DRQ Default Value: 0

23.1.96 USBFS0_USBHOST_HOST_DMA_ENBL

Host DMA Enable Register

Address: 0x403F4B00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	None	
HW Access	None				R	R	None	
Name	None [7:4]				DM_EP2DRQE	DM_EP1DRQE	None	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	DM_EP2DRQE	This bit enables DMA Request by EP2DRQ. '0' : Disable '1' : Enable Default Value: 0
2	DM_EP1DRQE	This bit enables DMA Request by EP1DRQ. '0' : Disable '1' : Enable Default Value: 0

23.1.97 USBFS0_USBHOST_HOST_EP1_BLK

Host Endpoint 1 Block Register

Address: 0x403F4B20

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	BLK_NUM [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	BLK_NUM [31:24]							

Bits	Name	Description
31 : 16	BLK_NUM	Set the total byte number for DMA transfer. If HOST_EP1_RW1_DR or HOST_EP1_RW2_DR is written, the block number counter is decremented when DMAE='1'. - Set this bits before DMA transfer is enabled (HOST_DMA_ENBL.DM_DP1DRQE='1') Default Value: 0

23.1.98 USBFS0_USBHOST_HOST_EP2_BLK

Host Endpoint 2 Block Register

Address: 0x403F4B30

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	BLK_NUM [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	BLK_NUM [31:24]							

Bits	Name	Description
31 : 16	BLK_NUM	Set the total byte number for DMA transfer. If HOST_EP2_RW1_DR or HOST_EP2_RW2_DR is written, the block number counter is decremented when DMAE='1'. - Set this bits before DMA transfer is enabled (HOST_DMA_ENBL.DM_DP2DRQE='1') Default Value: 0

Section F: Peripheral Group 4

This section encompasses the following chapter:

24 Serial Memory Interface (SMIF) Registers

This section discusses the Serial Memory Interface (SMIF) registers. It lists all the registers in mapping tables, in address order.

24.1 Register Details

Register	Address	Description
SMIF0_CTL	0x40420000	Control
SMIF0_STATUS	0x40420004	Status
SMIF0_TX_CMD_FIFO_STATUS	0x40420044	Transmitter command FIFO status
SMIF0_TX_CMD_FIFO_WR	0x40420050	Transmitter command FIFO write
SMIF0_TX_DATA_FIFO_CTL	0x40420080	Transmitter data FIFO control
SMIF0_TX_DATA_FIFO_STATUS	0x40420084	Transmitter data FIFO status
SMIF0_TX_DATA_FIFO_WR1	0x40420090	Transmitter data FIFO write
SMIF0_TX_DATA_FIFO_WR2	0x40420094	Transmitter data FIFO write
SMIF0_TX_DATA_FIFO_WR4	0x40420098	Transmitter data FIFO write
SMIF0_RX_DATA_FIFO_CTL	0x404200C0	Receiver data FIFO control
SMIF0_RX_DATA_FIFO_STATUS	0x404200C4	Receiver data FIFO status
SMIF0_RX_DATA_FIFO_RD1	0x404200D0	Receiver data FIFO read
SMIF0_RX_DATA_FIFO_RD2	0x404200D4	Receiver data FIFO read
SMIF0_RX_DATA_FIFO_RD4	0x404200D8	Receiver data FIFO read
SMIF0_RX_DATA_FIFO_RD1_SILENT	0x404200E0	Receiver data FIFO silent read
SMIF0_SLOW_CA_CTL	0x40420100	Slow cache control
SMIF0_SLOW_CA_CMD	0x40420108	Slow cache command
SMIF0_FAST_CA_CTL	0x40420180	Fast cache control
SMIF0_FAST_CA_CMD	0x40420188	Fast cache command
SMIF0_CRYPTO_CMD	0x40420200	Cryptography Command
SMIF0_CRYPTO_INPUT0	0x40420220	Cryptography input 0
SMIF0_CRYPTO_INPUT1	0x40420224	Cryptography input 1
SMIF0_CRYPTO_INPUT2	0x40420228	Cryptography input 2
SMIF0_CRYPTO_INPUT3	0x4042022C	Cryptography input 3
SMIF0_CRYPTO_KEY0	0x40420240	Cryptography key 0
SMIF0_CRYPTO_KEY1	0x40420244	Cryptography key 1

Register	Address	Description
SMIF0_CRYPTO_KEY2	0x40420248	Cryptography key 2
SMIF0_CRYPTO_KEY3	0x4042024C	Cryptography key 3
SMIF0_CRYPTO_OUTPUT0	0x40420260	Cryptography output 0
SMIF0_CRYPTO_OUTPUT1	0x40420264	Cryptography output 1
SMIF0_CRYPTO_OUTPUT2	0x40420268	Cryptography output 2
SMIF0_CRYPTO_OUTPUT3	0x4042026C	Cryptography output 3
SMIF0_INTR	0x404207C0	Interrupt register
SMIF0_INTR_SET	0x404207C4	Interrupt set register
SMIF0_INTR_MASK	0x404207C8	Interrupt mask register
SMIF0_INTR_MASKED	0x404207CC	Interrupt masked register
SMIF0_DEVICE0_CTL	0x40420800	Control
SMIF0_DEVICE0_ADDR	0x40420808	Device region base address
SMIF0_DEVICE0_MASK	0x4042080C	Device region mask
SMIF0_DEVICE0_ADDR_CTL	0x40420820	Address control
SMIF0_DEVICE0_RD_CMD_CTL	0x40420840	Read command control
SMIF0_DEVICE0_RD_ADDR_CTL	0x40420844	Read address control
SMIF0_DEVICE0_RD_MODE_CTL	0x40420848	Read mode control
SMIF0_DEVICE0_RD_DUMMY_CTL	0x4042084C	Read dummy control
SMIF0_DEVICE0_RD_DATA_CTL	0x40420850	Read data control
SMIF0_DEVICE0_WR_CMD_CTL	0x40420860	Write command control
SMIF0_DEVICE0_WR_ADDR_CTL	0x40420864	Write address control
SMIF0_DEVICE0_WR_MODE_CTL	0x40420868	Write mode control
SMIF0_DEVICE0_WR_DUMMY_CTL	0x4042086C	Write dummy control
SMIF0_DEVICE0_WR_DATA_CTL	0x40420870	Write data control
SMIF0_DEVICE1_CTL	0x40420880	Control. See SMIF0_DEVICE0_CTL for the details of bit fields.
SMIF0_DEVICE1_ADDR	0x40420888	Device region base address. See SMIF0_DEVICE0_ADDR for the details of bit fields.
SMIF0_DEVICE1_MASK	0x4042088C	Device region mask. See SMIF0_DEVICE0_MASK for the details of bit fields.
SMIF0_DEVICE1_ADDR_CTL	0x404208A0	Address control. See SMIF0_DEVICE0_ADDR_CTL for the details of bit fields.
SMIF0_DEVICE1_RD_CMD_CTL	0x404208C0	Read command control. See SMIF0_DEVICE0_RD_CMD_CTL for the details of bit fields.
SMIF0_DEVICE1_RD_ADDR_CTL	0x404208C4	Read address control. See SMIF0_DEVICE0_RD_ADDR_CTL for the details of bit fields.
SMIF0_DEVICE1_RD_MODE_CTL	0x404208C8	Read mode control. See SMIF0_DEVICE0_RD_MODE_CTL for the details of bit fields.
SMIF0_DEVICE1_RD_DUMMY_CTL	0x404208CC	Read dummy control. See SMIF0_DEVICE0_RD_DUMMY_CTL for the details of bit fields.
SMIF0_DEVICE1_RD_DATA_CTL	0x404208D0	Read data control. See SMIF0_DEVICE0_RD_DATA_CTL for the details of bit fields.
SMIF0_DEVICE1_WR_CMD_CTL	0x404208E0	Write command control. See SMIF0_DEVICE0_WR_CMD_CTL for the details of bit fields.
SMIF0_DEVICE1_WR_ADDR_CTL	0x404208E4	Write address control. See SMIF0_DEVICE0_WR_ADDR_CTL for the details of bit fields.
SMIF0_DEVICE1_WR_MODE_CTL	0x404208E8	Write mode control. See SMIF0_DEVICE0_WR_MODE_CTL for the details of bit fields.
SMIF0_DEVICE1_WR_DUMMY_CTL	0x404208EC	Write dummy control. See SMIF0_DEVICE0_WR_DUMMY_CTL for the details of bit fields.

Register	Address	Description
SMIF0_DEVICE1_WR_DATA_CTL	0x404208F0	Write data control. See SMIF0_DEVICE0_WR_DATA_CTL for the details of bit fields.
SMIF0_DEVICE2_CTL	0x40420900	Control. See SMIF0_DEVICE0_CTLfor the details of bit fields.
SMIF0_DEVICE2_ADDR	0x40420908	Device region base address. See SMIF0_DEVICE0_ADDR for the details of bit fields.
SMIF0_DEVICE2_MASK	0x4042090C	Device region mask. See SMIF0_DEVICE0_MASK for the details of bit fields.
SMIF0_DEVICE2_ADDR_CTL	0x40420920	Address control. See SMIF0_DEVICE0_ADDR_CTL for the details of bit fields.
SMIF0_DEVICE2_RD_CMD_CTL	0x40420940	Read command control. See SMIF0_DEVICE0_RD_CMD_CTL for the details of bit fields.
SMIF0_DEVICE2_RD_ADDR_CTL	0x40420944	Read address control. See SMIF0_DEVICE0_RD_ADDR_CTL for the details of bit fields.
SMIF0_DEVICE2_RD_MODE_CTL	0x40420948	Read mode control. See SMIF0_DEVICE0_RD_MODE_CTL for the details of bit fields.
SMIF0_DEVICE2_RD_DUMMY_CTL	0x4042094C	Read dummy control. See SMIF0_DEVICE0_RD_DUMMY_CTL for the details of bit fields.
SMIF0_DEVICE2_RD_DATA_CTL	0x40420950	Read data control. See SMIF0_DEVICE0_RD_DATA_CTL for the details of bit fields.
SMIF0_DEVICE2_WR_CMD_CTL	0x40420960	Write command control. See SMIF0_DEVICE0_WR_CMD_CTL for the details of bit fields.
SMIF0_DEVICE2_WR_ADDR_CTL	0x40420964	Write address control. See SMIF0_DEVICE0_WR_ADDR_CTL for the details of bit fields.
SMIF0_DEVICE2_WR_MODE_CTL	0x40420968	Write mode control. See SMIF0_DEVICE0_WR_MODE_CTL for the details of bit fields.
SMIF0_DEVICE2_WR_DUMMY_CTL	0x4042096C	Write dummy control. See SMIF0_DEVICE0_WR_DUMMY_CTL for the details of bit fields.
SMIF0_DEVICE2_WR_DATA_CTL	0x40420970	Write data control. See SMIF0_DEVICE0_WR_DATA_CTL for the details of bit fields.
SMIF0_DEVICE3_CTL	0x40420980	Control. See SMIF0_DEVICE0_CTL for the details of bit fields.
SMIF0_DEVICE3_ADDR	0x40420988	Device region base address. See SMIF0_DEVICE0_ADDR for the details of bit fields.
SMIF0_DEVICE3_MASK	0x4042098C	Device region mask. See SMIF0_DEVICE0_MASK for the details of bit fields.
SMIF0_DEVICE3_ADDR_CTL	0x404209A0	Address control. See SMIF0_DEVICE0_ADDR_CTL for the details of bit fields.
SMIF0_DEVICE3_RD_CMD_CTL	0x404209C0	Read command control. See SMIF0_DEVICE0_RD_CMD_CTL for the details of bit fields.
SMIF0_DEVICE3_RD_ADDR_CTL	0x404209C4	Read address control. See SMIF0_DEVICE0_RD_ADDR_CTL for the details of bit fields.
SMIF0_DEVICE3_RD_MODE_CTL	0x404209C8	Read mode control. See SMIF0_DEVICE0_RD_MODE_CTL for the details of bit fields.
SMIF0_DEVICE3_RD_DUMMY_CTL	0x404209CC	Read dummy control. See SMIF0_DEVICE0_RD_DUMMY_CTL for the details of bit fields.
SMIF0_DEVICE3_RD_DATA_CTL	0x404209D0	Read data control. See SMIF0_DEVICE0_RD_DATA_CTL for the details of bit fields.
SMIF0_DEVICE3_WR_CMD_CTL	0x404209E0	Write command control. See SMIF0_DEVICE0_WR_CMD_CTL for the details of bit fields.
SMIF0_DEVICE3_WR_ADDR_CTL	0x404209E4	Write address control. See SMIF0_DEVICE0_WR_ADDR_CTL for the details of bit fields.
SMIF0_DEVICE3_WR_MODE_CTL	0x404209E8	Write mode control. See SMIF0_DEVICE0_WR_MODE_CTL for the details of bit fields.
SMIF0_DEVICE3_WR_DUMMY_CTL	0x404209EC	Write dummy control. See SMIF0_DEVICE0_WR_DUMMY_CTL for the details of bit fields.
SMIF0_DEVICE3_WR_DATA_CTL	0x404209F0	Write data control. See SMIF0_DEVICE0_WR_DATA_CTL for the details of bit fields.

24.1.1 SMIF0_CTL

Control

Address: 0x40420000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							XIP_MODE

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW		None			
HW Access	None		R		None			
Name	None [15:14]		CLOCK_IF_RX_SEL [13:12]		None [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None					RW		
HW Access	None					R		
Name	None [23:19]					DESELECT_DELAY [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						RW
HW Access	R	None						R
Name	ENABLED	None [30:25]						BLOCK

Bits	Name	Description
31	ENABLED	IP enable: '0': Disabled. All non-retention registers are reset to their default value when the IP is disabled. When the IP is disabled, the XIP accesses produce AHB-Lite bus errors. '1': Enabled. Note: Before disabling the IP, SW should ensure that the IP is NOT busy (STATUS.BUSY is '0'), otherwise illegal interface transfers may occur. Default Value: 0 **0x0: DISABLED :** **0x1: ENABLED :**
24	BLOCK	Specifies what happens for MMIO interface read accesses to an empty RX data FIFO or to a full TX format/data FIFO. Note: the FIFOs can only be accessed in MMIO_MODE. This field is not used for test controller accesses. Default Value: 0

24.1.1 SMIF0_CTL (continued)

		0x0: BUS_ERROR : 0': Generate an AHB-Lite bus error. This option is useful when SW decides to use polling on STATUS.TR_BUSY to determine if a interface transfer is no longer busy (transfer is completed). This option adds SW complexity, but limits the number of AHB-Lite wait states (and limits ISR latency). **0x1: WAIT_STATES :** 1': Introduce wait states. This setting potentially locks up the AHB-Lite infrastructure and may increase the CPU interrupt latency.This option is useful when SW performs TX/RX data FIFO accesses immediately after a command is setup using the TX format FIFO. This option has low SW complexity, but may result in a significant number of AHB-Lite wait states (and may increase ISR latency).
18 : 16	DESELECT_DELAY	Specifies the minimum duration of SPI deselection ("spi_select_out[]" is high/'1') in between SPI transfers: "0": 1 interface clock cycle. "1": 2 interface clock cycles. "2": 3 interface clock cycles. "3": 4 interface clock cycles. "4": 5 interface clock cycles. "5": 6 interface clock cycles. "6": 7 interface clock cycles. "7": 8 interface clock cycles. During SPI deselection, "spi_select_out[]" are '1'/inactive, "spi_data_out[]" are '1' and "spi_clk_out" is '0'/inactive. Default Value: 0
13 : 12	CLOCK_IF_RX_SEL	Specifies device interface receiver clock "clk_if_rx" source. MISO data is captured on the rising edge of "clk_if_rx". "0": "spi_clk_out" (internal clock) "1": !"spi_clk_out" (internal clock) "2": "spi_clk_in" (feedback clock) "3": !"spi_clk_in" (feedback clock) Note: the device interface transmitter clock "clk_if_tx" is fixed and is "spi_clk_out" MOSI data is driven on the falling edge of "clk_if_tx". Default Value: 3
0	XIP_MODE	Mode of operation. Note: this field should only be changed when the IP is disabled or when STATUS.BUSY is '0' and SW should not be executing from the XIP interface or MMIO interface. Default Value: 0 **0x0: MMIO_MODE :** '0': MMIO mode. Individual MMIO accesses to TX and RX FIFOs are used to generate a sequence of SPI transfers. This mode of operation allows for large flexibility in terms of the SPI transfers that can be generated. **0x1: XIP_MODE :** 1': XIP mode. eXecute-In-Place mode: incoming read and write transfers over the AHB-Lite bus infrastructure are automatically translated in SPI transfers to read data from and write data to a device. This mode of operation allow for efficient device read and write operations. This mode is only supported in SPI_MODE.

24.1.2 SMIF0_STATUS

Status

Address: 0x40420004

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	BUSY	None						

Bits	Name	Description
31	BUSY	Cache, cryptography, XIP, device interface or any other logic busy in the IP: '0': not busy '1': busy When BUSY is '0', the IP can be safely disabled without: - the potential loss of transient write data. - the potential risk of aborting an inflight SPI device interface transfer. When BUSY is '0', the mode of operation (XIP_MODE or MMIO_MODE) can be safely changed. Default Value: 0

24.1.3 SMIF0_TX_CMD_FIFO_STATUS

Transmitter command FIFO status

Address: 0x40420044

Retention: Not Retained

Bits	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SW Access	None					R		
HW Access	None					W		
Name	None [7:3]					USED3 [2:0]		

Bits	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	**Name**	**Description**
2 : 0	USED3	Number of entries that are used in the TX command FIFO (available in both XIP_MODE and MMIO_MODE). Legal range: [0, 4]. Default Value: 0

24.1.4 SMIF0_TX_CMD_FIFO_WR

Transmitter command FIFO write

Address: 0x40420050

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	DATA20 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	DATA20 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None				W			
HW Access	None				R			
Name	None [23:20]				DATA20 [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description

24.1.4 SMIF0_TX_CMD_FIFO_WR (continued)

19 : 0	DATA20	Command data. The higher two bits DATA[19:18] specify the specific command "0"/TX: A SPI transfer always start with a TX command FIFO entry of the TX format. - DATA[17:16] specifies the width of the data transfer: - "0": 1 bit/cycle (single data transfer). - "1": 2 bits/cycle (dual data transfer). - "2": 4 bits/cycle (quad data transfer). - "3": 8 bits/cycle (octal data transfer). - DATA[15]: specifies whether this is the last TX Byte; i.e. whether the spi_select_out[3:0] IO output signals are de-activated after the transfer. - DATA[11:8] specifies which of the four devices are selected. DATA[11:8] are directly mapped to "spi_select_out[3:0]". Two devices can be selected at the same time in dual-quad mode. - '0': device deselected - '1': device selected - DATA[7:0] specifies the transmitted Byte. "1"/TX_COUNT: The TX_COUNT command relies on the TX data FIFO to provide the transmitted bytes. The "TX_COUNT" command is ALWAYS considered to be the last command of a SPI data transfers. - DATA[17:16] specifies the width of the transfer. - DATA[15:0] specifies the number of to be transmitted Bytes (minus 1) from the TX data FIFO. "2"/RX_COUNT: The RX_COUNT command relies on the RX data FIFO to accept the received bytes. The "RX_COUNT" command is ALWAYS considered to be the last command of a SPI data transfers. - DATA[17:16] specifies the width of the transfer. - DATA[15:0] specifies the number of to be transmitted Bytes (minus 1) to the RX data FIFO. "3"/DUMMY_COUNT: The "DUMMY_COUNT" command conveys dummy cycles. Dummy cycles are used to implement a Turn-Around time in which the SPI master changes from a transmitter driving the data lines to a receiver receiving on the same data lines. The "DUMMY_COUNT" command is ALWAYS considered to be NOT the last command of a SPI data transfers; i.e. it needs to be followed by another command. - DATA[15:0] specifies the number of dummy cycles (minus 1). In dummy cycles, the data lines are not driven. Default Value: 0

24.1.5 SMIF0_TX_DATA_FIFO_CTL

Transmitter data FIFO control

Address: 0x40420080

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW		
HW Access	None					R		
Name	None [7:3]					TRIGGER_LEVEL [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2 : 0	TRIGGER_LEVEL	Determines when the TX data FIFO "tr_tx_req" trigger is activated (trigger activation requires MMIO_MODE, the trigger is NOT activated in XIP_MODE): - Trigger is active when TX_DATA_FIFO_STATUS.USED <= TRIGGER_LEVEL. Default Value: 0

24.1.6 SMIF0_TX_DATA_FIFO_STATUS

Transmitter data FIFO status

Address: 0x40420084

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R			
HW Access	None				W			
Name	None [7:4]				USED4 [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	USED4	Number of entries that are used in the TX data FIFO (available in both XIP_MODE and MMIO_-MODE). Legal range: [0, 8]. Default Value: 0

24.1.7 SMIF0_TX_DATA_FIFO_WR1

Transmitter data FIFO write

Address: 0x40420090

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	DATA0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA0	TX data (written to TX data FIFO). Default Value: 0

24.1.8 SMIF0_TX_DATA_FIFO_WR2

Transmitter data FIFO write

Address: 0x40420094

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	DATA0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	DATA1 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 8	DATA1	TX data (written to TX data FIFO, second byte). Default Value: 0
7 : 0	DATA0	TX data (written to TX data FIFO, first byte). Default Value: 0

24.1.9 SMIF0_TX_DATA_FIFO_WR4

Transmitter data FIFO write

Address: 0x40420098

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	DATA0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	DATA1 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	W							
HW Access	R							
Name	DATA2 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	W							
HW Access	R							
Name	DATA3 [31:24]							

Bits	Name	Description
31 : 24	DATA3	TX data (written to TX data FIFO, fourth byte). Default Value: 0
23 : 16	DATA2	TX data (written to TX data FIFO, third byte). Default Value: 0
15 : 8	DATA1	TX data (written to TX data FIFO, second byte). Default Value: 0
7 : 0	DATA0	TX data (written to TX data FIFO, first byte). Default Value: 0

24.1.10 SMIF0_RX_DATA_FIFO_CTL

Receiver data FIFO control

Address: 0x404200C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW		
HW Access	None					R		
Name	None [7:3]					TRIGGER_LEVEL [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2 : 0	TRIGGER_LEVEL	Determines when RX data FIFO "tr_rx_req" trigger is activated (trigger activation requires MMIO_MODE, the trigger is NOT activated in XIP_MODE): - Trigger is active when RX_DATA_FIFO_STATUS.USED > TRIGGER_LEVEL. Default Value: 0

24.1.11 SMIF0_RX_DATA_FIFO_STATUS

Receiver data FIFO status

Address: 0x404200C4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R			
HW Access	None				W			
Name	None [7:4]				USED4 [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	USED4	Number of entries that are used in the RX data FIFO (available in both XIP_MODE and MMIO_-MODE). Legal range: [0, 8]. Default Value: 0

24.1.12 SMIF0_RX_DATA_FIFO_RD1

Receiver data FIFO read

Address: 0x404200D0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA0	RX data (read from RX data FIFO). Default Value: 0

24.1.13 SMIF0_RX_DATA_FIFO_RD2

Receiver data FIFO read

Address: 0x404200D4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA1 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 8	DATA1	RX data (read from RX data FIFO, second byte). Default Value: 0
7 : 0	DATA0	RX data (read from RX data FIFO, first byte). Default Value: 0

24.1.14 SMIF0_RX_DATA_FIFO_RD4

Receiver data FIFO read

Address: 0x404200D8

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA1 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	DATA2 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	DATA3 [31:24]							

Bits	Name	Description
31 : 24	DATA3	RX data (read from RX data FIFO, fourth byte). Default Value: 0
23 : 16	DATA2	RX data (read from RX data FIFO, third byte). Default Value: 0
15 : 8	DATA1	RX data (read from RX data FIFO, second byte). Default Value: 0
7 : 0	DATA0	RX data (read from RX data FIFO, first byte). Default Value: 0

24.1.15 SMIF0_RX_DATA_FIFO_RD1_SILENT

Receiver data FIFO silent read

Address: 0x404200E0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA0	RX data (read from RX data FIFO). Default Value: 0

24.1.16 SMIF0_SLOW_CA_CTL

Slow cache control

Address: 0x40420100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	
HW Access	None						R	
Name	None [23:18]						WAY [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None				RW	
HW Access	R	R	None				R	
Name	ENABLED	PREF_EN	None [29:26]				SET_ADDR [25:24]	

Bits	Name	Description
31	ENABLED	Cache enable: '0': Disabled. '1': Enabled. Default Value: 1
30	PREF_EN	Prefetch enable: '0': Disabled. '1': Enabled. Prefetching requires the cache to be enabled; i.e. ENABLED is '1'. Default Value: 1
25 : 24	SET_ADDR	Specifies the cache set for which cache information is provided in SLOW_CA_STATUS0/1/2. Default Value: 0
17 : 16	WAY	Specifies the cache way for which cache information is provided in SLOW_CA_STATUS0/1/2. Default Value: 0

24.1.17 SMIF0_SLOW_CA_CMD

Slow cache command

Address: 0x40420108

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1S
HW Access	None							RW1C
Name	None [7:1]							INV

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	INV	Cache and prefetch buffer invalidation. SW writes a '1' to clear the cache and prefetch buffer. The cache's LRU structure is also reset to its default state. Note, A write access will invalidate the prefetch buffer automatically in hardware. A write access should invalidate both fast and slow caches, by firmware. Note, firmware should invalidate the cache and prefetch buffer only when STATUS.BUSY is '0'. Default Value: 0

24.1.18 SMIF0_FAST_CA_CTL

Fast cache control

Address: 0x40420180

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	
HW Access	None						R	
Name	None [23:18]						WAY [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None				RW	
HW Access	R	R	None				R	
Name	ENABLED	PREF_EN	None [29:26]				SET_ADDR [25:24]	

Bits	Name	Description
31	ENABLED	See SLOW_CA_CTL.ENABLED. Default Value: 1
30	PREF_EN	See SLOW_CA_CTL.PREF_EN. Default Value: 1
25 : 24	SET_ADDR	See SLOW_CA_CTL.SET_ADDR. Default Value: 0
17 : 16	WAY	See SLOW_CA_CTL.WAY. Default Value: 0

24.1.19 SMIF0_FAST_CA_CMD

Fast cache command

Address: 0x40420188

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1S
HW Access	None							RW1C
Name	None [7:1]							INV

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	INV	See SLOW_CA_CMD.INV. Default Value: 0

24.1.20 SMIF0_CRYPTO_CMD

Cryptography Command

Address: 0x40420200

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1S
HW Access	None							RW1C
Name	None [7:1]							START

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	START	SW sets this field to '1' to start a AES-128 forward block cipher operation (on the address in CRYPTO_ADDR). HW sets this field to '0' to indicate that the operation has completed. Once completed, the result of the operation can be read from CRYPTO_RESULT0, ..., CRYPTO_RE-SULT3. The operation takes roughly 13 clk_hf clock cycles. Note: An operation can only be started in MMIO_MODE. Default Value: 0

24.1.21 SMIF0_CRYPTO_INPUT0

Cryptography input 0

Address: 0x40420220

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	INPUT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INPUT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INPUT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	INPUT [31:24]							

Bits	Name	Description
31 : 0	INPUT	Four Bytes of the plaintext PT[31:0] = CRYPTO_INPUT0.INPUT[31:0]. Default Value: Undefined

24.1.22 SMIF0_CRYPTO_INPUT1

Cryptography input 1

Address: 0x40420224

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	INPUT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INPUT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INPUT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	INPUT [31:24]							

Bits	Name	Description
31 : 0	INPUT	Four Bytes of the plaintext PT[63:32] = CRYPTO_INPUT1.INPUT[31:0]. Default Value: Undefined

24.1.23 SMIF0_CRYPTO_INPUT2

Cryptography input 2

Address: 0x40420228

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	INPUT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INPUT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INPUT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	INPUT [31:24]							

Bits	Name	Description
31 : 0	INPUT	Four Bytes of the plaintext PT[95:64] = CRYPTO_INPUT2.INPUT[31:0]. Default Value: Undefined

24.1.24 SMIF0_CRYPTO_INPUT3

Cryptography input 3

Address: 0x4042022C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	INPUT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INPUT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INPUT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	INPUT [31:24]							

Bits	Name	Description
31 : 0	INPUT	Four Bytes of the plaintext PT[127:96] = CRYPTO_INPUT3.INPUT[31:0]. Default Value: Undefined

24.1.25 SMIF0_CRYPTO_KEY0

Cryptography key 0

Address: 0x40420240

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	KEY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	KEY [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	W							
HW Access	R							
Name	KEY [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	W							
HW Access	R							
Name	KEY [31:24]							

Bits	Name	Description
31 : 0	KEY	Four Bytes of the key KEY[31:0] = CRYPTO_KEY0.KEY[31:0]. Default Value: Undefined

24.1.26 SMIF0_CRYPTO_KEY1

Cryptography key 1

Address: 0x40420244

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	KEY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	KEY [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	W							
HW Access	R							
Name	KEY [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	W							
HW Access	R							
Name	KEY [31:24]							

Bits	Name	Description
31 : 0	KEY	Four Bytes of the key KEY[63:32] = CRYPTO_KEY1.KEY[31:0]. Default Value: Undefined

24.1.27 SMIF0_CRYPTO_KEY2

Cryptography key 2

Address: 0x40420248

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	KEY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	KEY [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	W							
HW Access	R							
Name	KEY [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	W							
HW Access	R							
Name	KEY [31:24]							

Bits	Name	Description
31 : 0	KEY	Four Bytes of the key KEY[95:64] = CRYPTO_KEY2.KEY[31:0]. Default Value: Undefined

24.1.28 SMIF0_CRYPTO_KEY3

Cryptography key 3

Address: 0x4042024C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	KEY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	KEY [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	W							
HW Access	R							
Name	KEY [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	W							
HW Access	R							
Name	KEY [31:24]							

Bits	Name	Description
31 : 0	KEY	Four Bytes of the key KEY[127:96] = CRYPTO_KEY3.KEY[31:0]. Default Value: Undefined

24.1.29 SMIF0_CRYPTO_OUTPUT0

Cryptography output 0

Address: 0x40420260

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	OUTPUT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	OUTPUT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	A							
Name	OUTPUT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	A							
Name	OUTPUT [31:24]							

Bits	Name	Description
31 : 0	OUTPUT	Four Bytes of the ciphertext CT[31:0] = CRYPTO_OUTPUT0.OUTPUT[31:0]. Default Value: Undefined

24.1.30 SMIF0_CRYPTO_OUTPUT1

Cryptography output 1

Address: 0x40420264

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	OUTPUT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	OUTPUT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	A							
Name	OUTPUT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	A							
Name	OUTPUT [31:24]							

Bits	Name	Description
31 : 0	OUTPUT	Four Bytes of the ciphertext CT[63:32] = CRYPTO_OUTPUT1.OUTPUT[31:0]. Default Value: Undefined

24.1.31 SMIF0_CRYPTO_OUTPUT2

Cryptography output 2

Address: 0x40420268

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	OUTPUT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	OUTPUT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	A							
Name	OUTPUT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	A							
Name	OUTPUT [31:24]							

Bits	Name	Description
31 : 0	OUTPUT	Four Bytes of the ciphertext CT[95:64] = CRYPTO_OUTPUT2.OUTPUT[31:0]. Default Value: Undefined

24.1.32 SMIF0_CRYPTO_OUTPUT3

Cryptography output 3

Address: 0x4042026C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	OUTPUT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	OUTPUT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	A							
Name	OUTPUT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	A							
Name	OUTPUT [31:24]							

Bits	Name	Description
31 : 0	OUTPUT	Four Bytes of the ciphertext CT[127:96] = CRYPTO_OUTPUT3.OUTPUT[31:0]. Default Value: Undefined

24.1.33 SMIF0_INTR

Interrupt register

Address: 0x404207C0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	None		RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
Name	None [7:6]		RX_-DATA_FI-FO_UNDERFLOW	TX_-DATA_FI-FO_OVERFLOW	TX_CM-D_FI-FO_OVERFLOW	XIP_ALIGN-MENT_ER-ROR	TR_RX-_REQ	TR_TX-_REQ

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	RX_DATA_FIFO_UNDER-FLOW	Activated in MMIO mode, on an AHB-Lite read transfer from the RX data FIFO (RX_DATA_FI-FO_RD1, RX_DATA_FIFO_RD2, RX_DATA_FIFO_RD4) with not enough entries available. Only activated for NON test bus controller transfers. Default Value: 0
4	TX_DATA_FIFO_OVER-FLOW	Activated in MMIO mode, on an AHB-Lite write transfer to the TX data FIFO (TX_DATA_FI-FO_WR1, TX_DATA_FIFO_WR2, TX_DATA_FIFO_WR4) with not enough free entries avail-able. Default Value: 0
3	TX_CMD_FIFO_OVER-FLOW	Activated in MMIO mode, on an AHB-Lite write transfer to the TX command FIFO (TX_CMD_FI-FO_WR) with not enough free entries available. Default Value: 0

24.1.33 SMIF0_INTR (continued)

2	XIP_ALIGNMENT_ERROR	Activated in XIP mode, if: - The selected device's ADDR_CTL.DIV2 is '1' and the AHB-Lite bus transfer address is not a multiple of 2. - The selected device's ADDR_CTL.DIV2 is '1' and the XIP transfer request is NOT for a multiple of 2 Bytes. Note: In dual-quad SPI mode (ADDR_CTL.DIV is '1'), each memory device contributes a 4-bit nibble for read data or write data. This is only possible if the request address is a multiple of 2 and the number of requested Bytes is a multiple of 2. Default Value: 0
1	TR_RX_REQ	Activated in MMIO mode, when a RX data FIFO trigger "tr_rx_req" is activated. Default Value: 0
0	TR_TX_REQ	Activated in MMIO mode, when a TX data FIFO trigger "tr_tx_req" is activated. Default Value: 0

24.1.34 SMIF0_INTR_SET

Interrupt set register

Address: 0x404207C4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	None		A	A	A	A	A	A
Name	None [7:6]		RX_-DATA_FI-FO_UNDERFLOW	TX_-DATA_FI-FO_OVERFLOW	TX_CM-D_FI-FO_OVERFLOW	XIP_ALIGN-MENT_ER-ROR	TR_RX-_REQ	TR_TX-_REQ

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	RX_DATA_FIFO_UNDER-FLOW	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
4	TX_DATA_FIFO_OVER-FLOW	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
3	TX_CMD_FIFO_OVER-FLOW	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
2	XIP_ALIGNMENT_ER-ROR	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
1	TR_RX_REQ	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	TR_TX_REQ	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

24.1.35 SMIF0_INTR_MASK

Interrupt mask register

Address: 0x404207C8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		R	R	R	R	R	R
Name	None [7:6]		RX_-DATA_FI-FO_UNDERFLOW	TX_-DATA_FI-FO_OVERFLOW	TX_CM-D_FI-FO_OVERFLOW	XIP_ALIGN-MENT_ER-ROR	TR_RX-_REQ	TR_TX-_REQ

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	RX_DATA_FIFO_UNDER-FLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
4	TX_DATA_FIFO_OVER-FLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
3	TX_CMD_FIFO_OVER-FLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	XIP_ALIGNMENT_ER-ROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	TR_RX_REQ	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	TR_TX_REQ	Mask bit for corresponding bit in interrupt request register. Default Value: 0

24.1.36 SMIF0_INTR_MASKED

Interrupt masked register

Address: 0x404207CC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R	R	R	R	R	R
HW Access	None		W	W	W	W	W	W
Name	None [7:6]		RX_-DATA_FI-FO_UNDERFLOW	TX_-DATA_FI-FO_OVERFLOW	TX_CM-D_FI-FO_OVERFLOW	XIP_ALIGN-MENT_ER-ROR	TR_RX-_REQ	TR_TX-_REQ

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	RX_DATA_FIFO_UNDER-FLOW	Logical and of corresponding request and mask bits. Default Value: 0
4	TX_DATA_FIFO_OVER-FLOW	Logical and of corresponding request and mask bits. Default Value: 0
3	TX_CMD_FIFO_OVER-FLOW	Logical and of corresponding request and mask bits. Default Value: 0
2	XIP_ALIGNMENT_ER-ROR	Logical and of corresponding request and mask bits. Default Value: 0
1	TR_RX_REQ	Logical and of corresponding request and mask bits. Default Value: 0
0	TR_TX_REQ	Logical and of corresponding request and mask bits. Default Value: 0

24.1.37 SMIF0_DEVICE0_CTL

Control

Address: 0x40420800

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							WR_EN

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							CRYPTO_EN

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	
HW Access	None						R	
Name	None [23:18]						DATA_SEL [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	ENABLED	None [30:24]						

Bits	Name	Description
31	ENABLED	Device enable: '0': Disabled. '1': Enabled. Default Value: 0
17 : 16	DATA_SEL	Specifies the connection of the IP's data lines (spi_data[0], , spi_data[7]) to the device's data lines (SI/IO0, SO/IO1, IO2, IO3, IO4, IO5, IO6, IO7): "0": spi_data[0] = IO0, spi_data[1] = IO1, , spi_data[7] = IO7. This value is allowed for single, dual, quad, dual quad and octal SPI modes. This value must be used for the first device in dual quad SPI mode. This value must be used for octal SPI mode. "1": spi_data[2] = IO0, spi_data[3] = IO1. This value is only allowed for single and dual SPI modes. "2": spi_data[4] = IO0, spi_data[5] = IO1, , spi_data[7] = IO3. This value is only allowed for single, dual, quad and dual quad SPI modes. In dual quad SPI mode, this value must be used for the second device. "3": spi_data[6] = IO0, spi_data[7] = IO1. This value is only allowed for single and dual SPI modes. Default Value: 0

24.1.37 SMIF0_DEVICE0_CTL (continued)

8	CRYPTO_EN	Cryptography on read/write accesses: '0': disabled. '1': enabled. Default Value: 0
0	WR_EN	Write enable: '0': write transfers are not allowed to this device. An attempt to write to this device results in an AHB-Lite bus error. '1': write transfers are allowed to this device. Default Value: 0

24.1.38 SMIF0_DEVICE0_ADDR

Device region base address

Address: 0x40420808

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	A							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	A							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 8	ADDR	Specifies the base address of the device region. If the device region is 2^m Bytes, ADDR MUST be a multiple of 2^m. In dual quad SPI data transfer, the two devices should have the same ADDR and MASK register settings. The device control information (ADDR_CTL, RD_CMD_CTL, etc.) are provided by the MMIO control registers of the device with the lowest index. The most significant bit fields are constants and set based on the SMIF_XIP_ADDR parameter. The most significant bits are identified on the SMIF_XIP_MASK parameter. E.g., if SMIF_X-IP_MASK is 0xff00:0000 (16 MB XIP memory region), ADDR[31:24] = SMIF_XIP_ADDR[31:24]. Default Value: Undefined

24.1.39 SMIF0_DEVICE0_MASK

Device region mask

Address: 0x4042080C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	MASK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	A							
Name	MASK [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	A							
Name	MASK [31:24]							

Bits	Name	Description
31 : 8	MASK	Specifies the size of the device region. All '1' bits are used to compare the incoming transfer request address A[31:0] with the address as specified in ADDR.ADDR: Address A is in the device when (A[31:8] & MASK[31:8]) == ADDR.ADDR[31:8]. The most significant bit fields are constants and set to'1'. The most significant bits are identified on the SMIF_XIP_MASK parameter. E.g., if SMIF_XIP_MASK is 0xff00:0000 (16 MB XIP memory region), MASK[31:24] = 0xff. Note: a transfer request that is not in any device region results in an AHB-Lite bus error. Default Value: Undefined

24.1.40 SMIF0_DEVICE0_ADDR_CTL

Address control

Address: 0x40420820

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	
HW Access	None						R	
Name	None [7:2]						SIZE2 [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							DIV2

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	DIV2	Specifies if the AHB-Lite bus transfer address is divided by 2 or not: '0': No divide by 2. '1': Divide by 2. This functionality is used for read and write operation in XIP, dual quad SPI mode; i.e. this DIV2 must be set to '1' in dual quad SPI mode. If the transfer request address is NOT a multiple of 2 or the requested number of Bytes is not a multiple of 2, the XIP_ALIGNMENT_ERROR interrupt cause is activated. Default Value: 0
1 : 0	SIZE2	Specifies the size of the XIP device address in Bytes: "0": 1 Byte address. "1": 2 Byte address. "2": 3 Byte address. "3": 4 Byte address. The lower significant address Bytes of the transfer request are used as XIP address to the external device. Note that for dual quad SPI data transfer, the transfer request address is divided by 2. Therefore, the transfer request address needs to be a multiple of 2. If the trasnfer requestaddress is NOT a multiple of 2, the XIP_ALIGNMENT_ERROR interrupt cause is activated. Default Value: 0

24.1.41 SMIF0_DEVICE0_RD_CMD_CTL

Read command control

Address: 0x40420840

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CODE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	
HW Access	None						R	
Name	None [23:18]						WIDTH [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	PRESENT	None [30:24]						

Bits	Name	Description
31	PRESENT	Presence of command field: '0': not present '1': present Default Value: 0
17 : 16	WIDTH	Width of data transfer: "0": 1 bit/cycle (single data transfer). "1": 2 bits/cycle (dual data transfer). "2": 4 bits/cycle (quad data transfer). "3": 8 bits/cycle (octal data transfer). Default Value: 0
7 : 0	CODE	Command byte code. Default Value: 0

24.1.42 SMIF0_DEVICE0_RD_ADDR_CTL

Read address control

Address: 0x40420844

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	
HW Access	None						R	
Name	None [23:18]						WIDTH [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
17 : 16	WIDTH	Width of transfer. Default Value: 0

24.1.43 SMIF0_DEVICE0_RD_MODE_CTL

Read mode control

Address: 0x40420848

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CODE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	
HW Access	None						R	
Name	None [23:18]						WIDTH [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	PRESENT	None [30:24]						

Bits	Name	Description
31	PRESENT	Presence of mode field: '0': not present '1': present Default Value: 0
17 : 16	WIDTH	Width of transfer. Default Value: 0
7 : 0	CODE	Mode byte code. Default Value: 0

24.1.44 SMIF0_DEVICE0_RD_DUMMY_CTL

Read dummy control

Address: 0x4042084C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			R				
Name	None [7:5]			SIZE5 [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	PRESENT	None [30:24]						

Bits	Name	Description
31	PRESENT	Presence of dummy cycles: '0': not present '1': present Default Value: 0
4 : 0	SIZE5	Number of dummy cycles (minus 1): "0": 1 cycles ... "31": 32 cycles. Note: this field specifies dummy cycles, not dummy Bytes! Default Value: 0

24.1.45 SMIF0_DEVICE0_RD_DATA_CTL

Read data control

Address: 0x40420850

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	
HW Access	None						R	
Name	None [23:18]						WIDTH [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
17 : 16	WIDTH	Width of transfer. Default Value: 0

24.1.46 SMIF0_DEVICE0_WR_CMD_CTL

Write command control

Address: 0x40420860

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CODE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	
HW Access	None						R	
Name	None [23:18]						WIDTH [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	PRESENT	None [30:24]						

Bits	Name	Description
31	PRESENT	Presence of command field: '0': not present '1': present Default Value: 0
17 : 16	WIDTH	Width of transfer. Default Value: 0
7 : 0	CODE	Command byte code. Default Value: 0

24.1.47 SMIF0_DEVICE0_WR_ADDR_CTL

Write address control

Address: 0x40420864

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	
HW Access	None						R	
Name	None [23:18]						WIDTH [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
17 : 16	WIDTH	Width of transfer. Default Value: 0

24.1.48 SMIF0_DEVICE0_WR_MODE_CTL

Write mode control

Address: 0x40420868

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CODE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	
HW Access	None						R	
Name	None [23:18]						WIDTH [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	PRESENT	None [30:24]						

Bits	Name	Description
31	PRESENT	Presence of mode field: '0': not present '1': present Default Value: 0
17 : 16	WIDTH	Width of transfer. Default Value: 0
7 : 0	CODE	Mode byte code. Default Value: 0

24.1.49 SMIF0_DEVICE0_WR_DUMMY_CTL

Write dummy control

Address: 0x4042086C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			R				
Name	None [7:5]			SIZE5 [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	PRESENT	None [30:24]						

Bits	Name	Description
31	PRESENT	Presence of dummy cycles: '0': not present '1': present Default Value: 0
4 : 0	SIZE5	Number of dummy cycles (minus 1): "0": 1 cycles ... "31": 32 cycles. Default Value: 0

24.1.50 SMIF0_DEVICE0_WR_DATA_CTL

Write data control

Address: 0x40420870

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	
HW Access	None						R	
Name	None [23:18]						WIDTH [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
17 : 16	WIDTH	Width of transfer. Default Value: 0

Section G: Peripheral Group 6

This section encompasses the following chapters:

25 Serial Communication Block (SCB) Registers

This section discusses the Serial Communications Block (SCB) registers. It lists all the registers in mapping tables, in address order

25.1 Register Details

Register	Address	Description
SCB0_CTRL	0x40610000	Generic control
SCB0_SPI_CTRL	0x40610020	SPI control
SCB0_SPI_STATUS	0x40610024	SPI status
SCB0_UART_CTRL	0x40610040	UART control
SCB0_UART_TX_CTRL	0x40610044	UART transmitter control
SCB0_UART_RX_CTRL	0x40610048	UART receiver control
SCB0_UART_RX_STATUS	0x4061004C	UART receiver status
SCB0_UART_FLOW_CTRL	0x40610050	UART flow control
SCB0_I2C_CTRL	0x40610060	I2C control
SCB0_I2C_STATUS	0x40610064	I2C status
SCB0_I2C_M_CMD	0x40610068	I2C master command
SCB0_I2C_S_CMD	0x4061006C	I2C slave command
SCB0_I2C_CFG	0x40610070	I2C configuration
SCB0_TX_CTRL	0x40610200	Transmitter control
SCB0_TX_FIFO_CTRL	0x40610204	Transmitter FIFO control
SCB0_TX_FIFO_STATUS	0x40610208	Transmitter FIFO status
SCB0_TX_FIFO_WR	0x40610240	Transmitter FIFO write
SCB0_RX_CTRL	0x40610300	Receiver control
SCB0_RX_FIFO_CTRL	0x40610304	Receiver FIFO control
SCB0_RX_FIFO_STATUS	0x40610308	Receiver FIFO status
SCB0_RX_MATCH	0x40610310	Slave address and mask
SCB0_RX_FIFO_RD	0x40610340	Receiver FIFO read
SCB0_RX_FIFO_RD_SILENT	0x40610344	Receiver FIFO read silent
SCB0_EZ_DATA0	0x40610400	Memory buffer. This is the starting address of a register bank containing 256 registers (SCB0_EZ_DATA0 to SCB0_EZ_DATA255)
SCB0_INTR_CAUSE	0x40610E00	Active clocked interrupt signal
SCB0_INTR_M	0x40610F00	Master interrupt request

Register	Address	Description
SCB0_INTR_M_SET	0x40610F04	Master interrupt set request
SCB0_INTR_M_MASK	0x40610F08	Master interrupt mask
SCB0_INTR_M_MASKED	0x40610F0C	Master interrupt masked request
SCB0_INTR_S	0x40610F40	Slave interrupt request
SCB0_INTR_S_SET	0x40610F44	Slave interrupt set request
SCB0_INTR_S_MASK	0x40610F48	Slave interrupt mask
SCB0_INTR_S_MASKED	0x40610F4C	Slave interrupt masked request
SCB0_INTR_TX	0x40610F80	Transmitter interrupt request
SCB0_INTR_TX_SET	0x40610F84	Transmitter interrupt set request
SCB0_INTR_TX_MASK	0x40610F88	Transmitter interrupt mask
SCB0_INTR_TX_MASKED	0x40610F8C	Transmitter interrupt masked request
SCB0_INTR_RX	0x40610FC0	Receiver interrupt request
SCB0_INTR_RX_SET	0x40610FC4	Receiver interrupt set request
SCB0_INTR_RX_MASK	0x40610FC8	Receiver interrupt mask
SCB0_INTR_RX_MASKED	0x40610FCC	Receiver interrupt masked request
SCB1_CTRL	0x40620000	Generic control. See SCB0_CTRL for the details of bit fields.
SCB1_SPI_CTRL	0x40620020	SPI control. See SCB0_SPI_CTRL for the details of bit fields.
SCB1_SPI_STATUS	0x40620024	SPI status. See SCB0_SPI_STATUS for the details of bit fields.
SCB1_UART_CTRL	0x40620040	UART control. See SCB0_UART_CTRL for the details of bit fields.
SCB1_UART_TX_CTRL	0x40620044	UART transmitter control. See SCB0_UART_TX_CTRL for the details of bit fields.
SCB1_UART_RX_CTRL	0x40620048	UART receiver control. See SCB0_UART_RX_CTRL for the details of bit fields.
SCB1_UART_RX_STATUS	0x4062004C	UART receiver status. See SCB0_UART_RX_STATUS for the details of bit fields.
SCB1_UART_FLOW_CTRL	0x40620050	UART flow control. See SCB0_UART_FLOW_CTRL for the details of bit fields.
SCB1_I2C_CTRL	0x40620060	I2C control. See SCB0_I2C_CTRL for the details of bit fields.
SCB1_I2C_STATUS	0x40620064	I2C status. See SCB0_I2C_STATUS for the details of bit fields.
SCB1_I2C_M_CMD	0x40620068	I2C master command. See SCB0_I2C_M_CMD for the details of bit fields.
SCB1_I2C_S_CMD	0x4062006C	I2C slave command. See SCB0_I2C_S_CMD for the details of bit fields.
SCB1_I2C_CFG	0x40620070	I2C configuration. See SCB0_I2C_CFG for the details of bit fields.
SCB1_TX_CTRL	0x40620200	Transmitter control. See SCB0_TX_CTRL for the details of bit fields.
SCB1_TX_FIFO_CTRL	0x40620204	Transmitter FIFO control. See SCB0_TX_FIFO_CTRL for the details of bit fields.
SCB1_TX_FIFO_STATUS	0x40620208	Transmitter FIFO status. See SCB0_TX_FIFO_STATUS for the details of bit fields.
SCB1_TX_FIFO_WR	0x40620240	Transmitter FIFO write. See SCB0_TX_FIFO_WR for the details of bit fields.
SCB1_RX_CTRL	0x40620300	Receiver control. See SCB0_RX_CTRL for the details of bit fields.
SCB1_RX_FIFO_CTRL	0x40620304	Receiver FIFO control. See SCB0_RX_FIFO_CTRL for the details of bit fields.
SCB1_RX_FIFO_STATUS	0x40620308	Receiver FIFO status. See SCB0_RX_FIFO_STATUS for the details of bit fields.
SCB1_RX_MATCH	0x40620310	Slave address and mask. See SCB0_RX_MATCH for the details of bit fields.
SCB1_RX_FIFO_RD	0x40620340	Receiver FIFO read. See SCB0_RX_FIFO_RDfor the details of bit fields.
SCB1_RX_FIFO_RD_SILENT	0x40620344	Receiver FIFO read silent. See SCB0_RX_FIFO_RD_SILENT for the details of bit fields.
SCB1_EZ_DATA0	0x40620400	Memory buffer. This is the starting address of a register bank containing 256 registers (SCB1_EZ_DATA0 to SCB1_EZ_DATA255). See SCB0_EZ_DATA0 for the details of bit fields.
SCB1_INTR_CAUSE	0x40620E00	Active clocked interrupt signal. See SCB0_INTR_CAUSEfor the details of bit fields.
SCB1_INTR_M	0x40620F00	Master interrupt request. See SCB0_INTR_Mfor the details of bit fields.
SCB1_INTR_M_SET	0x40620F04	Master interrupt set request. See SCB0_INTR_M_SETfor the details of bit fields.

Register	Address	Description
SCB1_INTR_M_MASK	0x40620F08	Master interrupt mask. See SCB0_INTR_M_MASKfor the details of bit fields.
SCB1_INTR_M_MASKED	0x40620F0C	Master interrupt masked request. See SCB0_INTR_M_MASKEDfor the details of bit fields.
SCB1_INTR_S	0x40620F40	Slave interrupt request. See SCB0_INTR_Sfor the details of bit fields.
SCB1_INTR_S_SET	0x40620F44	Slave interrupt set request. See SCB0_INTR_S_SETfor the details of bit fields.
SCB1_INTR_S_MASK	0x40620F48	Slave interrupt mask. See SCB0_INTR_S_MASKfor the details of bit fields.
SCB1_INTR_S_MASKED	0x40620F4C	Slave interrupt masked request. See SCB0_INTR_S_MASKEDfor the details of bit fields.
SCB1_INTR_TX	0x40620F80	Transmitter interrupt request. See SCB0_INTR_TXfor the details of bit fields.
SCB1_INTR_TX_SET	0x40620F84	Transmitter interrupt set request. See SCB0_INTR_TX_SETfor the details of bit fields.
SCB1_INTR_TX_MASK	0x40620F88	Transmitter interrupt mask. See SCB0_INTR_TX_MASKfor the details of bit fields.
SCB1_INTR_TX_MASKED	0x40620F8C	Transmitter interrupt masked request. See SCB0_INTR_TX_MASKEDfor the details of bit fields.
SCB1_INTR_RX	0x40620FC0	Receiver interrupt request. See SCB0_INTR_RXfor the details of bit fields.
SCB1_INTR_RX_SET	0x40620FC4	Receiver interrupt set request. See SCB0_INTR_RX_SETfor the details of bit fields.
SCB1_INTR_RX_MASK	0x40620FC8	Receiver interrupt mask. See SCB0_INTR_RX_MASKfor the details of bit fields.
SCB1_INTR_RX_MASKED	0x40620FCC	Receiver interrupt masked request. See SCB0_INTR_RX_MASKEDfor the details of bit fields.
SCB2_CTRL	0x40630000	Generic control. See SCB0_CTRL for the details of bit fields.
SCB2_SPI_CTRL	0x40630020	SPI control. See SCB0_SPI_CTRL for the details of bit fields.
SCB2_SPI_STATUS	0x40630024	SPI status. See SCB0_SPI_STATUS for the details of bit fields.
SCB2_UART_CTRL	0x40630040	UART control. See SCB0_UART_CTRL for the details of bit fields.
SCB2_UART_TX_CTRL	0x40630044	UART transmitter control. See SCB0_UART_TX_CTRL for the details of bit fields.
SCB2_UART_RX_CTRL	0x40630048	UART receiver control. See SCB0_UART_RX_CTRL for the details of bit fields.
SCB2_UART_RX_STATUS	0x4063004C	UART receiver status. See SCB0_UART_RX_STATUS for the details of bit fields.
SCB2_UART_FLOW_CTRL	0x40630050	UART flow control. See SCB0_UART_FLOW_CTRL for the details of bit fields.
SCB2_I2C_CTRL	0x40630060	I2C control. See SCB0_I2C_CTRL for the details of bit fields.
SCB2_I2C_STATUS	0x40630064	I2C status. See SCB0_I2C_STATUS for the details of bit fields.
SCB2_I2C_M_CMD	0x40630068	I2C master command. See SCB0_I2C_M_CMD for the details of bit fields.
SCB2_I2C_S_CMD	0x4063006C	I2C slave command. See SCB0_I2C_S_CMD for the details of bit fields.
SCB2_I2C_CFG	0x40630070	I2C configuration. See SCB0_I2C_CFG for the details of bit fields.
SCB2_TX_CTRL	0x40630200	Transmitter control. See SCB0_TX_CTRL for the details of bit fields.
SCB2_TX_FIFO_CTRL	0x40630204	Transmitter FIFO control. See SCB0_TX_FIFO_CTRL for the details of bit fields.
SCB2_TX_FIFO_STATUS	0x40630208	Transmitter FIFO status. See SCB0_TX_FIFO_STATUS for the details of bit fields.
SCB2_TX_FIFO_WR	0x40630240	Transmitter FIFO write. See SCB0_TX_FIFO_WR for the details of bit fields.
SCB2_RX_CTRL	0x40630300	Receiver control. See SCB0_RX_CTRL for the details of bit fields.
SCB2_RX_FIFO_CTRL	0x40630304	Receiver FIFO control. See SCB0_RX_FIFO_CTRL for the details of bit fields.
SCB2_RX_FIFO_STATUS	0x40630308	Receiver FIFO status. See SCB0_RX_FIFO_STATUS for the details of bit fields.
SCB2_RX_MATCH	0x40630310	Slave address and mask. See SCB0_RX_MATCH for the details of bit fields.
SCB2_RX_FIFO_RD	0x40630340	Receiver FIFO read. See SCB0_RX_FIFO_RDfor the details of bit fields.
SCB2_RX_FIFO_RD_SILENT	0x40630344	Receiver FIFO read silent. See SCB0_RX_FIFO_RD_SILENT for the details of bit fields.
SCB2_EZ_DATA0	0x40630400	Memory buffer. This is the starting address of a register bank containing 256 registers(SCB2_EZ_DATA0 to SCB2_EZ_DATA255) . See SCB0_EZ_DATA0 for the details of bit fields.
SCB2_INTR_CAUSE	0x40630E00	Active clocked interrupt signal. See SCB0_INTR_CAUSEfor the details of bit fields.
SCB2_INTR_M	0x40630F00	Master interrupt request. See SCB0_INTR_Mfor the details of bit fields.
SCB2_INTR_M_SET	0x40630F04	Master interrupt set request. See SCB0_INTR_M_SETfor the details of bit fields.

Register	Address	Description
SCB2_INTR_M_MASK	0x40630F08	Master interrupt mask. See SCB0_INTR_M_MASKfor the details of bit fields.
SCB2_INTR_M_MASKED	0x40630F0C	Master interrupt masked request. See SCB0_INTR_M_MASKEDfor the details of bit fields.
SCB2_INTR_S	0x40630F40	Slave interrupt request. See SCB0_INTR_Sfor the details of bit fields.
SCB2_INTR_S_SET	0x40630F44	Slave interrupt set request. See SCB0_INTR_S_SETfor the details of bit fields.
SCB2_INTR_S_MASK	0x40630F48	Slave interrupt mask. See SCB0_INTR_S_MASKfor the details of bit fields.
SCB2_INTR_S_MASKED	0x40630F4C	Slave interrupt masked request. See SCB0_INTR_S_MASKEDfor the details of bit fields.
SCB2_INTR_TX	0x40630F80	Transmitter interrupt request. See SCB0_INTR_TXfor the details of bit fields.
SCB2_INTR_TX_SET	0x40630F84	Transmitter interrupt set request. See SCB0_INTR_TX_SETfor the details of bit fields.
SCB2_INTR_TX_MASK	0x40630F88	Transmitter interrupt mask. See SCB0_INTR_TX_MASKfor the details of bit fields.
SCB2_INTR_TX_MASKED	0x40630F8C	Transmitter interrupt masked request. See SCB0_INTR_TX_MASKEDfor the details of bit fields.
SCB2_INTR_RX	0x40630FC0	Receiver interrupt request. See SCB0_INTR_RXfor the details of bit fields.
SCB2_INTR_RX_SET	0x40630FC4	Receiver interrupt set request. See SCB0_INTR_RX_SETfor the details of bit fields.
SCB2_INTR_RX_MASK	0x40630FC8	Receiver interrupt mask. See SCB0_INTR_RX_MASKfor the details of bit fields.
SCB2_INTR_RX_MASKED	0x40630FCC	Receiver interrupt masked request. See SCB0_INTR_RX_MASKEDfor the details of bit fields.
SCB3_CTRL	0x40640000	Generic control. See SCB0_CTRL for the details of bit fields.
SCB3_SPI_CTRL	0x40640020	SPI control. See SCB0_SPI_CTRL for the details of bit fields.
SCB3_SPI_STATUS	0x40640024	SPI status. See SCB0_SPI_STATUS for the details of bit fields.
SCB3_UART_CTRL	0x40640040	UART control. See SCB0_UART_CTRL for the details of bit fields.
SCB3_UART_TX_CTRL	0x40640044	UART transmitter control. See SCB0_UART_TX_CTRL for the details of bit fields.
SCB3_UART_RX_CTRL	0x40640048	UART receiver control. See SCB0_UART_RX_CTRL for the details of bit fields.
SCB3_UART_RX_STATUS	0x4064004C	UART receiver status. See SCB0_UART_RX_STATUS for the details of bit fields.
SCB3_UART_FLOW_CTRL	0x40640050	UART flow control. See SCB0_UART_FLOW_CTRL for the details of bit fields.
SCB3_I2C_CTRL	0x40640060	I2C control. See SCB0_I2C_CTRL for the details of bit fields.
SCB3_I2C_STATUS	0x40640064	I2C status. See SCB0_I2C_STATUS for the details of bit fields.
SCB3_I2C_M_CMD	0x40640068	I2C master command. See SCB0_I2C_M_CMD for the details of bit fields.
SCB3_I2C_S_CMD	0x4064006C	I2C slave command. See SCB0_I2C_S_CMD for the details of bit fields.
SCB3_I2C_CFG	0x40640070	I2C configuration. See SCB0_I2C_CFG for the details of bit fields.
SCB3_TX_CTRL	0x40640200	Transmitter control. See SCB0_TX_CTRL for the details of bit fields.
SCB3_TX_FIFO_CTRL	0x40640204	Transmitter FIFO control. See SCB0_TX_FIFO_CTRL for the details of bit fields.
SCB3_TX_FIFO_STATUS	0x40640208	Transmitter FIFO status. See SCB0_TX_FIFO_STATUS for the details of bit fields.
SCB3_TX_FIFO_WR	0x40640240	Transmitter FIFO write. See SCB0_TX_FIFO_WR for the details of bit fields.
SCB3_RX_CTRL	0x40640300	Receiver control. See SCB0_RX_CTRL for the details of bit fields.
SCB3_RX_FIFO_CTRL	0x40640304	Receiver FIFO control. See SCB0_RX_FIFO_CTRL for the details of bit fields.
SCB3_RX_FIFO_STATUS	0x40640308	Receiver FIFO status. See SCB0_RX_FIFO_STATUS for the details of bit fields.
SCB3_RX_MATCH	0x40640310	Slave address and mask. See SCB0_RX_MATCH for the details of bit fields.
SCB3_RX_FIFO_RD	0x40640340	Receiver FIFO read. See SCB0_RX_FIFO_RDfor the details of bit fields.
SCB3_RX_FIFO_RD_SILENT	0x40640344	Receiver FIFO read silent. See SCB0_RX_FIFO_RD_SILENT for the details of bit fields.
SCB3_EZ_DATA0	0x40640400	Memory buffer. This is the starting address of a register bank containing 256 registers(SCB3_EZ_DATA0 to SCB3_EZ_DATA255) . See SCB0_EZ_DATA0 for the details of bit fields.
SCB3_INTR_CAUSE	0x40640E00	Active clocked interrupt signal. See SCB0_INTR_CAUSEfor the details of bit fields.
SCB3_INTR_M	0x40640F00	Master interrupt request. See SCB0_INTR_Mfor the details of bit fields.
SCB3_INTR_M_SET	0x40640F04	Master interrupt set request. See SCB0_INTR_M_SETfor the details of bit fields.

Register	Address	Description
SCB3_INTR_M_MASK	0x40640F08	Master interrupt mask. See SCB0_INTR_M_MASKfor the details of bit fields.
SCB3_INTR_M_MASKED	0x40640F0C	Master interrupt masked request. See SCB0_INTR_M_MASKEDfor the details of bit fields.
SCB3_INTR_S	0x40640F40	Slave interrupt request. See SCB0_INTR_Sfor the details of bit fields.
SCB3_INTR_S_SET	0x40640F44	Slave interrupt set request. See SCB0_INTR_S_SETfor the details of bit fields.
SCB3_INTR_S_MASK	0x40640F48	Slave interrupt mask. See SCB0_INTR_S_MASKfor the details of bit fields.
SCB3_INTR_S_MASKED	0x40640F4C	Slave interrupt masked request. See SCB0_INTR_S_MASKEDfor the details of bit fields.
SCB3_INTR_TX	0x40640F80	Transmitter interrupt request. See SCB0_INTR_TXfor the details of bit fields.
SCB3_INTR_TX_SET	0x40640F84	Transmitter interrupt set request. See SCB0_INTR_TX_SETfor the details of bit fields.
SCB3_INTR_TX_MASK	0x40640F88	Transmitter interrupt mask. See SCB0_INTR_TX_MASKfor the details of bit fields.
SCB3_INTR_TX_MASKED	0x40640F8C	Transmitter interrupt masked request. See SCB0_INTR_TX_MASKEDfor the details of bit fields.
SCB3_INTR_RX	0x40640FC0	Receiver interrupt request. See SCB0_INTR_RXfor the details of bit fields.
SCB3_INTR_RX_SET	0x40640FC4	Receiver interrupt set request. See SCB0_INTR_RX_SETfor the details of bit fields.
SCB3_INTR_RX_MASK	0x40640FC8	Receiver interrupt mask. See SCB0_INTR_RX_MASKfor the details of bit fields.
SCB3_INTR_RX_MASKED	0x40640FCC	Receiver interrupt masked request. See SCB0_INTR_RX_MASKEDfor the details of bit fields.
SCB4_CTRL	0x40650000	Generic control. See SCB0_CTRL for the details of bit fields.
SCB4_SPI_CTRL	0x40650020	SPI control. See SCB0_SPI_CTRL for the details of bit fields.
SCB4_SPI_STATUS	0x40650024	SPI status. See SCB0_SPI_STATUS for the details of bit fields.
SCB4_UART_CTRL	0x40650040	UART control. See SCB0_UART_CTRL for the details of bit fields.
SCB4_UART_TX_CTRL	0x40650044	UART transmitter control. See SCB0_UART_TX_CTRL for the details of bit fields.
SCB4_UART_RX_CTRL	0x40650048	UART receiver control. See SCB0_UART_RX_CTRL for the details of bit fields.
SCB4_UART_RX_STATUS	0x4065004C	UART receiver status. See SCB0_UART_RX_STATUS for the details of bit fields.
SCB4_UART_FLOW_CTRL	0x40650050	UART flow control. See SCB0_UART_FLOW_CTRL for the details of bit fields.
SCB4_I2C_CTRL	0x40650060	I2C control. See SCB0_I2C_CTRL for the details of bit fields.
SCB4_I2C_STATUS	0x40650064	I2C status. See SCB0_I2C_STATUS for the details of bit fields.
SCB4_I2C_M_CMD	0x40650068	I2C master command. See SCB0_I2C_M_CMD for the details of bit fields.
SCB4_I2C_S_CMD	0x4065006C	I2C slave command. See SCB0_I2C_S_CMD for the details of bit fields.
SCB4_I2C_CFG	0x40650070	I2C configuration. See SCB0_I2C_CFG for the details of bit fields.
SCB4_TX_CTRL	0x40650200	Transmitter control. See SCB0_TX_CTRL for the details of bit fields.
SCB4_TX_FIFO_CTRL	0x40650204	Transmitter FIFO control. See SCB0_TX_FIFO_CTRL for the details of bit fields.
SCB4_TX_FIFO_STATUS	0x40650208	Transmitter FIFO status. See SCB0_TX_FIFO_STATUS for the details of bit fields.
SCB4_TX_FIFO_WR	0x40650240	Transmitter FIFO write. See SCB0_TX_FIFO_WR for the details of bit fields.
SCB4_RX_CTRL	0x40650300	Receiver control. See SCB0_RX_CTRL for the details of bit fields.
SCB4_RX_FIFO_CTRL	0x40650304	Receiver FIFO control. See SCB0_RX_FIFO_CTRL for the details of bit fields.
SCB4_RX_FIFO_STATUS	0x40650308	Receiver FIFO status. See SCB0_RX_FIFO_STATUS for the details of bit fields.
SCB4_RX_MATCH	0x40650310	Slave address and mask. See SCB0_RX_MATCH for the details of bit fields.
SCB4_RX_FIFO_RD	0x40650340	Receiver FIFO read. See SCB0_RX_FIFO_RDfor the details of bit fields.
SCB4_RX_FIFO_RD_SILENT	0x40650344	Receiver FIFO read silent. See SCB0_RX_FIFO_RD_SILENT for the details of bit fields.
SCB4_EZ_DATA0	0x40650400	Memory buffer. This is the starting address of a register bank containing 256 registers (SCB4_EZ_DATA1 to SCB4_EZ_DATA255) . See SCB0_EZ_DATA0 for the details of bit fields.
SCB4_INTR_CAUSE	0x40650E00	Active clocked interrupt signal. See SCB0_INTR_CAUSEfor the details of bit fields.
SCB4_INTR_M	0x40650F00	Master interrupt request. See SCB0_INTR_M for the details of bit fields.
SCB4_INTR_M_SET	0x40650F04	Master interrupt set request. See SCB0_INTR_M_SET for the details of bit fields.
SCB4_INTR_M_MASK	0x40650F08	Master interrupt mask. See SCB0_INTR_M_MASK for the details of bit fields.

Register	Address	Description
SCB4_INTR_M_MASKED	0x40650F0C	Master interrupt masked request. See SCB0_INTR_M_MASKED for the details of bit fields.
SCB4_INTR_S	0x40650F40	Slave interrupt request. See SCB0_INTR_S for the details of bit fields.
SCB4_INTR_S_SET	0x40650F44	Slave interrupt set request. See SCB0_INTR_S_SET for the details of bit fields.
SCB4_INTR_S_MASK	0x40650F48	Slave interrupt mask. See SCB0_INTR_S_MASK for the details of bit fields.
SCB4_INTR_S_MASKED	0x40650F4C	Slave interrupt masked request. See SCB0_INTR_S_MASKED for the details of bit fields.
SCB4_INTR_TX	0x40650F80	Transmitter interrupt request. See SCB0_INTR_TX for the details of bit fields.
SCB4_INTR_TX_SET	0x40650F84	Transmitter interrupt set request. See SCB0_INTR_TX_SETfor the details of bit fields.
SCB4_INTR_TX_MASK	0x40650F88	Transmitter interrupt mask. See SCB0_INTR_TX_MASK for the details of bit fields.
SCB4_INTR_TX_MASKED	0x40650F8C	Transmitter interrupt masked request. See SCB0_INTR_TX_MASKED for the details of bit fields.
SCB4_INTR_RX	0x40650FC0	Receiver interrupt request. See SCB0_INTR_RX for the details of bit fields.
SCB4_INTR_RX_SET	0x40650FC4	Receiver interrupt set request. See SCB0_INTR_RX_SETfor the details of bit fields.
SCB4_INTR_RX_MASK	0x40650FC8	Receiver interrupt mask. See SCB0_INTR_RX_MASK for the details of bit fields.
SCB4_INTR_RX_MASKED	0x40650FCC	Receiver interrupt masked request. See SCB0_INTR_RX_MASKEDfor the details of bit fields.
SCB5_CTRL	0x40660000	Generic control. See SCB0_CTRL for the details of bit fields.
SCB5_SPI_CTRL	0x40660020	SPI control. See SCB0_SPI_CTRL for the details of bit fields.
SCB5_SPI_STATUS	0x40660024	SPI status. See SCB0_SPI_STATUS for the details of bit fields.
SCB5_UART_CTRL	0x40660040	UART control. See SCB0_UART_CTRL for the details of bit fields.
SCB5_UART_TX_CTRL	0x40660044	UART transmitter control. See SCB0_UART_TX_CTRL for the details of bit fields.
SCB5_UART_RX_CTRL	0x40660048	UART receiver control. See SCB0_UART_RX_CTRL for the details of bit fields.
SCB5_UART_RX_STATUS	0x4066004C	UART receiver status. See SCB0_UART_RX_STATUS for the details of bit fields.
SCB5_UART_FLOW_CTRL	0x40660050	UART flow control. See SCB0_UART_FLOW_CTRL for the details of bit fields.
SCB5_I2C_CTRL	0x40660060	I2C control. See SCB0_I2C_CTRL for the details of bit fields.
SCB5_I2C_STATUS	0x40660064	I2C status. See SCB0_I2C_STATUS for the details of bit fields.
SCB5_I2C_M_CMD	0x40660068	I2C master command. See SCB0_I2C_M_CMD for the details of bit fields.
SCB5_I2C_S_CMD	0x4066006C	I2C slave command. See SCB0_I2C_S_CMD for the details of bit fields.
SCB5_I2C_CFG	0x40660070	I2C configuration. See SCB0_I2C_CFG for the details of bit fields.
SCB5_TX_CTRL	0x40660200	Transmitter control. See SCB0_TX_CTRL for the details of bit fields.
SCB5_TX_FIFO_CTRL	0x40660204	Transmitter FIFO control. See SCB0_TX_FIFO_CTRL for the details of bit fields.
SCB5_TX_FIFO_STATUS	0x40660208	Transmitter FIFO status. See SCB0_TX_FIFO_STATUS for the details of bit fields.
SCB5_TX_FIFO_WR	0x40660240	Transmitter FIFO write. See SCB0_TX_FIFO_WR for the details of bit fields.
SCB5_RX_CTRL	0x40660300	Receiver control. See SCB0_RX_CTRL for the details of bit fields.
SCB5_RX_FIFO_CTRL	0x40660304	Receiver FIFO control. See SCB0_RX_FIFO_CTRL for the details of bit fields.
SCB5_RX_FIFO_STATUS	0x40660308	Receiver FIFO status. See SCB0_RX_FIFO_STATUS for the details of bit fields.
SCB5_RX_MATCH	0x40660310	Slave address and mask. See SCB0_RX_MATCH for the details of bit fields.
SCB5_RX_FIFO_RD	0x40660340	Receiver FIFO read. See SCB0_RX_FIFO_RDfor the details of bit fields.
SCB5_RX_FIFO_RD_SILENT	0x40660344	Receiver FIFO read silent. See SCB0_RX_FIFO_RD_SILENT for the details of bit fields.
SCB5_EZ_DATA0	0x40660400	Memory buffer. This is the starting address of a register bank containing 256 registers (SCB5_EZ_DATA0 to SCB5_EZ_DATA255) . See SCB0_EZ_DATA0 for the details of bit fields.
SCB5_INTR_CAUSE	0x40660E00	Active clocked interrupt signal. See SCB0_INTR_CAUSEfor the details of bit fields.
SCB5_INTR_M	0x40660F00	Master interrupt request. See SCB0_INTR_M for the details of bit fields.
SCB5_INTR_M_SET	0x40660F04	Master interrupt set request. See SCB0_INTR_M_SET for the details of bit fields.
SCB5_INTR_M_MASK	0x40660F08	Master interrupt mask. See SCB0_INTR_M_MASK for the details of bit fields.
SCB5_INTR_M_MASKED	0x40660F0C	Master interrupt masked request. See SCB0_INTR_M_MASKEDfor the details of bit fields.

Register	Address	Description
SCB5_INTR_S	0x40660F40	Slave interrupt request. See SCB0_INTR_Sfor the details of bit fields.
SCB5_INTR_S_SET	0x40660F44	Slave interrupt set request. See SCB0_INTR_S_SET for the details of bit fields.
SCB5_INTR_S_MASK	0x40660F48	Slave interrupt mask. See SCB0_INTR_S_MASK for the details of bit fields.
SCB5_INTR_S_MASKED	0x40660F4C	Slave interrupt masked request. See SCB0_INTR_S_MASKED for the details of bit fields.
SCB5_INTR_TX	0x40660F80	Transmitter interrupt request. See SCB0_INTR_TX for the details of bit fields.
SCB5_INTR_TX_SET	0x40660F84	Transmitter interrupt set request. See SCB0_INTR_TX_SET for the details of bit fields.
SCB5_INTR_TX_MASK	0x40660F88	Transmitter interrupt mask. See SCB0_INTR_TX_MASK for the details of bit fields.
SCB5_INTR_TX_MASKED	0x40660F8C	Transmitter interrupt masked request. See SCB0_INTR_TX_MASKED for the details of bit fields.
SCB5_INTR_RX	0x40660FC0	Receiver interrupt request. See SCB0_INTR_RX for the details of bit fields.
SCB5_INTR_RX_SET	0x40660FC4	Receiver interrupt set request. See SCB0_INTR_RX_SET for the details of bit fields.
SCB5_INTR_RX_MASK	0x40660FC8	Receiver interrupt mask. See SCB0_INTR_RX_MASK for the details of bit fields.
SCB5_INTR_RX_MASKED	0x40660FCC	Receiver interrupt masked request. See SCB0_INTR_RX_MASKED for the details of bit fields.
SCB6_CTRL	0x40670000	Generic control. See SCB0_CTRL for the details of bit fields.
SCB6_SPI_CTRL	0x40670020	SPI control. See SCB0_SPI_CTRL for the details of bit fields.
SCB6_SPI_STATUS	0x40670024	SPI status. See SCB0_SPI_STATUS for the details of bit fields.
SCB6_UART_CTRL	0x40670040	UART control. See SCB0_UART_CTRL for the details of bit fields.
SCB6_UART_TX_CTRL	0x40670044	UART transmitter control. See SCB0_UART_TX_CTRL for the details of bit fields.
SCB6_UART_RX_CTRL	0x40670048	UART receiver control. See SCB0_UART_RX_CTRL for the details of bit fields.
SCB6_UART_RX_STATUS	0x4067004C	UART receiver status. See SCB0_UART_RX_STATUS for the details of bit fields.
SCB6_UART_FLOW_CTRL	0x40670050	UART flow control. See SCB0_UART_FLOW_CTRL for the details of bit fields.
SCB6_I2C_CTRL	0x40670060	I2C control. See SCB0_I2C_CTRL for the details of bit fields.
SCB6_I2C_STATUS	0x40670064	I2C status. See SCB0_I2C_STATUS for the details of bit fields.
SCB6_I2C_M_CMD	0x40670068	I2C master command. See SCB0_I2C_M_CMD for the details of bit fields.
SCB6_I2C_S_CMD	0x4067006C	I2C slave command. See SCB0_I2C_S_CMD for the details of bit fields.
SCB6_I2C_CFG	0x40670070	I2C configuration. See SCB0_I2C_CFG for the details of bit fields.
SCB6_TX_CTRL	0x40670200	Transmitter control. See SCB0_TX_CTRL for the details of bit fields.
SCB6_TX_FIFO_CTRL	0x40670204	Transmitter FIFO control. See SCB0_TX_FIFO_CTRL for the details of bit fields.
SCB6_TX_FIFO_STATUS	0x40670208	Transmitter FIFO status. See SCB0_TX_FIFO_STATUS for the details of bit fields.
SCB6_TX_FIFO_WR	0x40670240	Transmitter FIFO write. See SCB0_TX_FIFO_WR for the details of bit fields.
SCB6_RX_CTRL	0x40670300	Receiver control. See SCB0_RX_CTRL for the details of bit fields.
SCB6_RX_FIFO_CTRL	0x40670304	Receiver FIFO control. See SCB0_RX_FIFO_CTRL for the details of bit fields.
SCB6_RX_FIFO_STATUS	0x40670308	Receiver FIFO status. See SCB0_RX_FIFO_STATUS for the details of bit fields.
SCB6_RX_MATCH	0x40670310	Slave address and mask. See SCB0_RX_MATCH for the details of bit fields.
SCB6_RX_FIFO_RD	0x40670340	Receiver FIFO read. See SCB0_RX_FIFO_RDfor the details of bit fields.
SCB6_RX_FIFO_RD_SILENT	0x40670344	Receiver FIFO read silent. See SCB0_RX_FIFO_RD_SILENT for the details of bit fields.
SCB6_EZ_DATA0	0x40670400	Memory buffer. This is the starting address of a register bank containing 256 registers (SCB6_EZ_DATA0 to SCB6_EZ_DATA255). See SCB0_EZ_DATA0 for the details of bit fields.
SCB6_INTR_CAUSE	0x40670E00	Active clocked interrupt signal. See SCB0_INTR_CAUSE for the details of bit fields.
SCB6_INTR_M	0x40670F00	Master interrupt request. See SCB0_INTR_M for the details of bit fields.
SCB6_INTR_M_SET	0x40670F04	Master interrupt set request. See SCB0_INTR_M_SET for the details of bit fields.
SCB6_INTR_M_MASK	0x40670F08	Master interrupt mask. See SCB0_INTR_M_MASK for the details of bit fields.
SCB6_INTR_M_MASKED	0x40670F0C	Master interrupt masked request. See SCB0_INTR_M_MASKED for the details of bit fields.
SCB6_INTR_S	0x40670F40	Slave interrupt request. See SCB0_INTR_S for the details of bit fields.

Register	Address	Description
SCB6_INTR_S_SET	0x40670F44	Slave interrupt set request. See SCB0_INTR_S_SETfor the details of bit fields.
SCB6_INTR_S_MASK	0x40670F48	Slave interrupt mask. See SCB0_INTR_S_MASK for the details of bit fields.
SCB6_INTR_S_MASKED	0x40670F4C	Slave interrupt masked request. See SCB0_INTR_S_MASKED for the details of bit fields.
SCB6_INTR_TX	0x40670F80	Transmitter interrupt request. See SCB0_INTR_TX for the details of bit fields.
SCB6_INTR_TX_SET	0x40670F84	Transmitter interrupt set request. See SCB0_INTR_TX_SET for the details of bit fields.
SCB6_INTR_TX_MASK	0x40670F88	Transmitter interrupt mask. See SCB0_INTR_TX_MASK for the details of bit fields.
SCB6_INTR_TX_MASKED	0x40670F8C	Transmitter interrupt masked request. See SCB0_INTR_TX_MASKED for the details of bit fields.
SCB6_INTR_RX	0x40670FC0	Receiver interrupt request. See SCB0_INTR_RX for the details of bit fields.
SCB6_INTR_RX_SET	0x40670FC4	Receiver interrupt set request. See SCB0_INTR_RX_SET for the details of bit fields.
SCB6_INTR_RX_MASK	0x40670FC8	Receiver interrupt mask. See SCB0_INTR_RX_MASK for the details of bit fields.
SCB6_INTR_RX_MASKED	0x40670FCC	Receiver interrupt masked request. See SCB0_INTR_RX_MASKED for the details of bit fields.
SCB7_CTRL	0x40680000	Generic control. See SCB0_CTRL for the details of bit fields.
SCB7_SPI_CTRL	0x40680020	SPI control. See SCB0_SPI_CTRL for the details of bit fields.
SCB7_SPI_STATUS	0x40680024	SPI status. See SCB0_SPI_STATUS for the details of bit fields.
SCB7_UART_CTRL	0x40680040	UART control. See SCB0_UART_CTRL for the details of bit fields.
SCB7_UART_TX_CTRL	0x40680044	UART transmitter control. See SCB0_UART_TX_CTRL for the details of bit fields.
SCB7_UART_RX_CTRL	0x40680048	UART receiver control. See SCB0_UART_RX_CTRL for the details of bit fields.
SCB7_UART_RX_STATUS	0x4068004C	UART receiver status. See SCB0_UART_RX_STATUS for the details of bit fields.
SCB7_UART_FLOW_CTRL	0x40680050	UART flow control. See SCB0_UART_FLOW_CTRL for the details of bit fields.
SCB7_I2C_CTRL	0x40680060	I2C control. See SCB0_I2C_CTRL for the details of bit fields.
SCB7_I2C_STATUS	0x40680064	I2C status. See SCB0_I2C_STATUS for the details of bit fields.
SCB7_I2C_M_CMD	0x40680068	I2C master command. See SCB0_I2C_M_CMD for the details of bit fields.
SCB7_I2C_S_CMD	0x4068006C	I2C slave command. See SCB0_I2C_S_CMD for the details of bit fields.
SCB7_I2C_CFG	0x40680070	I2C configuration. See SCB0_I2C_CFG for the details of bit fields.
SCB7_TX_CTRL	0x40680200	Transmitter control. See SCB0_TX_CTRL for the details of bit fields.
SCB7_TX_FIFO_CTRL	0x40680204	Transmitter FIFO control. See SCB0_TX_FIFO_CTRL for the details of bit fields.
SCB7_TX_FIFO_STATUS	0x40680208	Transmitter FIFO status. See SCB0_TX_FIFO_STATUS for the details of bit fields.
SCB7_TX_FIFO_WR	0x40680240	Transmitter FIFO write. See SCB0_TX_FIFO_WR for the details of bit fields.
SCB7_RX_CTRL	0x40680300	Receiver control. See SCB0_RX_CTRL for the details of bit fields.
SCB7_RX_FIFO_CTRL	0x40680304	Receiver FIFO control. See SCB0_RX_FIFO_CTRL for the details of bit fields.
SCB7_RX_FIFO_STATUS	0x40680308	Receiver FIFO status. See SCB0_RX_FIFO_STATUS for the details of bit fields.
SCB7_RX_MATCH	0x40680310	Slave address and mask. See SCB0_RX_MATCH for the details of bit fields.
SCB7_RX_FIFO_RD	0x40680340	Receiver FIFO read. See SCB0_RX_FIFO_RDfor the details of bit fields.
SCB7_RX_FIFO_RD_SILENT	0x40680344	Receiver FIFO read silent. See SCB0_RX_FIFO_RD_SILENT for the details of bit fields.
SCB7_EZ_DATA0	0x40680400	Memory buffer. This is the starting address of a register bank containing 256 registers (SCB7_EZ_DATA0 to SCB7_EZ_DATA255) .See SCB0_EZ_DATA0 for the details of bit fields.
SCB7_INTR_CAUSE	0x40680E00	Active clocked interrupt signal. See SCB0_INTR_CAUSEfor the details of bit fields.
SCB7_INTR_M	0x40680F00	Master interrupt request. See SCB0_INTR_M for the details of bit fields.
SCB7_INTR_M_SET	0x40680F04	Master interrupt set request. See SCB0_INTR_M_SET for the details of bit fields.
SCB7_INTR_M_MASK	0x40680F08	Master interrupt mask. See SCB0_INTR_M_MASK for the details of bit fields.
SCB7_INTR_M_MASKED	0x40680F0C	Master interrupt masked request. See SCB0_INTR_M_MASKED for the details of bit fields.
SCB7_INTR_S	0x40680F40	Slave interrupt request. See SCB0_INTR_S for the details of bit fields.
SCB7_INTR_S_SET	0x40680F44	Slave interrupt set request. See SCB0_INTR_S_SET for the details of bit fields.

Register	Address	Description
SCB7_INTR_S_MASK	0x40680F48	Slave interrupt mask. See SCB0_INTR_S_MASKfor the details of bit fields.
SCB7_INTR_S_MASKED	0x40680F4C	Slave interrupt masked request. See SCB0_INTR_S_MASKEDfor the details of bit fields.
SCB7_INTR_TX	0x40680F80	Transmitter interrupt request. See SCB0_INTR_TX for the details of bit fields.
SCB7_INTR_TX_SET	0x40680F84	Transmitter interrupt set request. See SCB0_INTR_TX_SETfor the details of bit fields.
SCB7_INTR_TX_MASK	0x40680F88	Transmitter interrupt mask. See SCB0_INTR_TX_MASK for the details of bit fields.
SCB7_INTR_TX_MASKED	0x40680F8C	Transmitter interrupt masked request. See SCB0_INTR_TX_MASKED for the details of bit fields.
SCB7_INTR_RX	0x40680FC0	Receiver interrupt request. See SCB0_INTR_RX for the details of bit fields.
SCB7_INTR_RX_SET	0x40680FC4	Receiver interrupt set request. See SCB0_INTR_RX_SET for the details of bit fields.
SCB7_INTR_RX_MASK	0x40680FC8	Receiver interrupt mask. See SCB0_INTR_RX_MASK for the details of bit fields.
SCB7_INTR_RX_MASKED	0x40680FCC	Receiver interrupt masked request. See SCB0_INTR_RX_MASKED for the details of bit fields.
SCB8_CTRL	0x40690000	Generic control
SCB8_STATUS	0x40690004	Generic status
SCB8_CMD_RESP_CTRL	0x40690008	Command/response control
SCB8_CMD_RESP_STATUS	0x4069000C	Command/response status
SCB8_SPI_CTRL	0x40690020	SPI control
SCB8_SPI_STATUS	0x40690024	SPI status
SCB8_I2C_CTRL	0x40690060	I2C control
SCB8_I2C_STATUS	0x40690064	I2C status
SCB8_I2C_S_CMD	0x4069006C	I2C slave command. See SCB0_I2C_S_CMD for the details of bit fields.
SCB8_I2C_CFG	0x40690070	I2C configuration. See SCB0_I2C_CFG for the details of bit fields.
SCB8_TX_CTRL	0x40690200	Transmitter control. See SCB0_TX_CTRL for the details of bit fields.
SCB8_TX_FIFO_CTRL	0x40690204	Transmitter FIFO control. See SCB0_TX_FIFO_CTRL for the details of bit fields.
SCB8_TX_FIFO_STATUS	0x40690208	Transmitter FIFO status. See SCB0_TX_FIFO_STATUS for the details of bit fields.
SCB8_TX_FIFO_WR	0x40690240	Transmitter FIFO write. See SCB0_TX_FIFO_WR for the details of bit fields.
SCB8_RX_CTRL	0x40690300	Receiver control. See SCB0_RX_CTRL for the details of bit fields.
SCB8_RX_FIFO_CTRL	0x40690304	Receiver FIFO control. See SCB0_RX_FIFO_CTRL for the details of bit fields.
SCB8_RX_FIFO_STATUS	0x40690308	Receiver FIFO status. See SCB0_RX_FIFO_STATUS for the details of bit fields.
SCB8_RX_MATCH	0x40690310	Slave address and mask. See SCB0_RX_MATCH for the details of bit fields.
SCB8_RX_FIFO_RD	0x40690340	Receiver FIFO read. See SCB0_RX_FIFO_RDfor the details of bit fields.
SCB8_RX_FIFO_RD_SILENT	0x40690344	Receiver FIFO read silent. See SCB0_RX_FIFO_RD_SILENT for the details of bit fields.
SCB8_EZ_DATA0	0x40690400	Memory buffer. This is the starting address of a register bank containing 256 registers (SCB_EZ_DATA0 to SCB8_EZ_DATA255).See SCB0_EZ_DATA0 for the details of bit fields.
SCB8_INTR_CAUSE	0x40690E00	Active clocked interrupt signal
SCB8_INTR_I2C_EC	0x40690E80	Externally clocked I2C interrupt request
SCB8_INTR_I2C_EC_MASK	0x40690E88	Externally clocked I2C interrupt mask
SCB8_INTR_I2C_EC_MASKED	0x40690E8C	Externally clocked I2C interrupt masked
SCB8_INTR_SPI_EC	0x40690EC0	Externally clocked SPI interrupt request
SCB8_INTR_SPI_EC_MASK	0x40690EC8	Externally clocked SPI interrupt mask
SCB8_INTR_SPI_EC_MASKED	0x40690ECC	Externally clocked SPI interrupt masked
SCB8_INTR_S	0x40690F40	Slave interrupt request. See SCB0_INTR_Sfor the details of bit fields.
SCB8_INTR_S_SET	0x40690F44	Slave interrupt set request. See SCB0_INTR_S_SET for the details of bit fields.
SCB8_INTR_S_MASK	0x40690F48	Slave interrupt mask. See SCB0_INTR_S_MASK for the details of bit fields.
SCB8_INTR_S_MASKED	0x40690F4C	Slave interrupt masked request. See SCB0_INTR_S_MASKED for the details of bit fields.

Register	Address	Description
SCB8_INTR_TX	0x40690F80	Transmitter interrupt request
SCB8_INTR_TX_SET	0x40690F84	Transmitter interrupt set request
SCB8_INTR_TX_MASK	0x40690F88	Transmitter interrupt mask
SCB8_INTR_TX_MASKED	0x40690F8C	Transmitter interrupt masked request
SCB8_INTR_RX	0x40690FC0	Receiver interrupt request
SCB8_INTR_RX_SET	0x40690FC4	Receiver interrupt set request
SCB8_INTR_RX_MASK	0x40690FC8	Receiver interrupt mask
SCB8_INTR_RX_MASKED	0x40690FCC	Receiver interrupt masked request

25.1.1 SCB0_CTRL

Generic control

Address: 0x40610000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				OVS [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	None		
HW Access	None				R	None		
Name	None [15:12]				BYTE_-MODE	None [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							ADDR_AC-CEPT

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None					RW	
HW Access	R	None					R	
Name	ENABLED	None [30:26]					MODE [25:24]	

Bits	Name	Description
31	ENABLED	0': Block Disabled '1': Block Enabled The proper order in which to initialize the SCB is as follows: - Program protocol specific information using SPI_CTRL, UART_CTRL (and UART_TX_CTRL and UART_RX_CTRL) or I2C_CTRL. This includes selection of a submode, master/slave functionality and transmitter/receiver functionality when applicable. - Program generic transmitter (TX_CTRL) and receiver (RX_CTRL) information. This includes enabling of the transmitter and receiver functionality. - Program transmitter FIFO (TX_FIFO_CTRL) and receiver FIFO (RX_FIFO_CTRL) information. - Program CTRL to enable SCB, select the specific operation mode and oversampling factor. When the SCB is enabled, no control information should be changed. Changes must be made AFTER disabling the SCB, e.g. to modify the operation mode (from I2C to SPI) or to go from externally to internally clocked. The change takes effect after the SCB is re-enabled. Note that disabling the SCB will cause re-initialization of the design and associated state is lost (e.g. FIFO content). Default Value: 0
25 : 24	MODE	Mode of operation (3: Reserved) Default Value: 3

25.1.1 SCB0_CTRL (continued)

		0x0: I2C : Inter-Integrated Circuits (I2C) mode. **0x1: SPI :** Serial Peripheral Interface (SPI) mode. **0x2: UART :** Universal Asynchronous Receiver/Transmitter (UART) mode.
16	ADDR_ACCEPT	Determines whether a received matching address is accepted in the RX FIFO:. '0': Matching address does not go in RX FIFO '1': Match address does go in RX FIFO In I2C mode, this field is used to allow the slave to put the received slave address or general call address in the RX FIFO. Note that a received matching address is put in the RX FIFO when this bit is '1' for both I2C read and write transfers. In multi-processor UART receiver mode, this field is used to allow the receiver to put the received address in the RX FIFO. Note: non-matching addresses are never put in the RX FIFO. In SPI mode this field must be '0' Default Value: 0
11	BYTE_MODE	Determines the number of bits per FIFO data element: '0': 16-bit FIFO data elements. '1': 8-bit FIFO data elements. This mode doubles the amount of FIFO entries, but TX_C-TRL.DATA_WIDTH and RX_CTRL.DATA_WIDTH are restricted to [0, 7]. Default Value: 0

25.1.1 SCB0_CTRL (continued)

3 : 0	OVS	Serial interface bit period oversampling factor expressed in clk_scb cycles. clk_scb is the peripheral clock divider connected to the SCB. Used for SPI Master and UART functionality. This field is NOT used in externally clocked mode. This filed is NOT used for SPI slave or I2C mode. OVS + 1 clk_scb cycles constitute a single serial interface clock/bit cycle. If OVS is odd, the oversampling factor is even and the low and high phase of the interface clock period are the same. If OVS is even, the oversampling factor is odd and the low and high phase can differ by 1 SCB clock period. In SPI master mode, the valid range is [3, 15]. The frequency of the SPI Clock is (frequency of clk_scb) / (OVS + 1). For example, is clk_scb is 50 MHz and OVS is 9, then the frequency of SPI Clock is 50 MHz / (9+1) = 5 MHz. If the MISO signal is not used for SPI master the valid range changes to [1,15] In SPI slave mode, the OVS field is NOT used. Refer to the architecture TRM for information on how to configure clk_scb for SPI Slave. Generally, it is recommended that clk_scb be as fast as possible for the slave. In UART standard sub mode (including LIN and Smartcard), the valid range is [7, 15]. In UART IrDA sub mode this field indirectly specifies the oversampling. The oversampling determines the interface clock/bit cycle and the width of the pulse. For normal transmission mode, the pulse is roughly 3/16 of the bit period (for all bit rates). There is only one valid OVS value: - 0: 16 times oversampling. clk_scb frequency = 16*115.2 KHz for 115.2 Kbps. clk_scb frequency = 16*57.6 KHz for 57.6 Kbps. clk_scb frequency = 16*38.4 KHz for 38.4 Kbps. clk_scb frequency = 16*19.2 KHz for 19.2 Kbps. clk_scb frequency = 16*9.6 KHz for 9.6 Kbps. clk_scb frequency = 16*2.4 KHz for 2.4 Kbps. clk_scb frequency = 16*1.2 KHz for 1.2 Kbps. - all other values are not used in normal mode. RX_CTRL.MEDIAN must be set to '1' for IrDA receiver functionality. UART IrDA RX Low power mode, OVS field values (with the required clk_scb frequency): - 0: 16 times oversampling. clk_scb frequency = 16*115.2 KHz for 115.2 Kbps. - 1: 32 times oversampling. clk_scb frequency = 32*57.6 KHz for 57.6 Kbps. - 2: 48 times oversampling. clk_scb frequency = 48*38.4 KHz for 38.4 Kbps. - 3: 96 times oversampling. clk_scb frequency = 96*19.2 KHz for 19.2 Kbps. - 4: 192 times oversampling. clk_scb frequency = 192*9.6 KHz for 9.6 Kbps. - 5: 768 times oversampling. clk_scb frequency = 768*2.4 KHz for 2.4 Kbps. - 6: 1536 times oversampling. clk_scb frequency = 1536*1.2 KHz for 1.2 Kbps. - all other values are not used in low power mode. In low power transmission mode, this pulse is potentially smaller (down to 1.62 us typical and 1.41 us minimal) than 3/16 of the bit period (for < 115.2 Kbps bitrates). Pulse widths greater or equal than two SCB clock cycles are guaranteed to be detected by the receiver. Pulse widths less than two SCB clock cycles and greater or equal than one SCB clock cycle may be detected by the receiver. Pulse widths less than one SCB clock cycle will not be detected by the receiver. Default Value: 15

25.1.2 SCB0_SPI_CTRL

SPI control

Address: 0x40610020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		R	R	R	R	R	R
Name	None [7:6]		SCLK_-CONTINU-OUS	LATE_MISO_SAMPLE	CPOL	CPHA	SE-LECT_PRE-CEDE	SSEL_-CONTINU-OUS

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [15:12]				SSEL_PO-LARITY3	SSEL_PO-LARITY2	SSEL_PO-LARITY1	SSEL_PO-LARITY0

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							LOOPBACK

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None			RW		RW	
HW Access	R	None			R		R	
Name	MASTER_-MODE	None [30:28]			SSEL [27:26]		MODE [25:24]	

Bits	Name	Description
31	MASTER_MODE	Master ('1') or slave ('0') mode. In master mode, transmission will commence on availability of data frames in the TX FIFO. In slave mode, when selected and there is no data frame in the TX FIFO, the slave will transmit all '1's. In both master and slave modes, received data frames will be lost if the RX FIFO is full. Default Value: 0
27 : 26	SSEL	Selects one of the four incoming/outgoing SPI slave select signals: - 0: Slave 0, SSEL[0]. - 1: Slave 1, SSEL[1]. - 2: Slave 2, SSEL[2]. - 3: Slave 3, SSEL[3]. The SCB should be disabled when changes are made to this field. Default Value: 0
25 : 24	MODE	Submode of SPI operation (3: Reserved). Default Value: 3

25.1.2 SCB0_SPI_CTRL (continued)

Bits	Name	Description
		0x0: SPI_MOTOROLA : SPI Motorola submode. **0x1: SPI_TI :** SPI Texas Instruments submode. **0x2: SPI_NS :** SPI National Semiconducturs submode.
16	LOOPBACK	Local loopback control (does NOT affect the information on the pins). Only used in master mode. Not used in National Semiconductors submode. '0': No local loopback '1': the SPI master MISO line is connected to the SPI master MOSI line. In other words, in loop-back mode the SPI master receives on MISO what it transmits on MOSI. Default Value: 0
11	SSEL_POLARITY3	Slave select polarity. Default Value: 0
10	SSEL_POLARITY2	Slave select polarity. Default Value: 0
9	SSEL_POLARITY1	Slave select polarity. Default Value: 0
8	SSEL_POLARITY0	Slave select polarity. SSEL_POLARITY0 applies to the outgoing SPI slave select signal 0 (mas-ter mode) and to the incoming SPI slave select signal (slave mode). For Motorola and National Semiconductors submodes: '0': slave select is low/'0' active. '1': slave select is high/'1' active. For Texas Instruments submode: '0': high/'1' active precede/coincide pulse. '1': low/'0' active precede/coincide pulse. Default Value: 0
5	SCLK_CONTINUOUS	Only applicable in master mode. '0': SCLK is generated, when the SPI master is enabled and data is transmitted. '1': SCLK is generated, when the SPI master is enabled. This mode is useful for slave devices that use SCLK for functional operation other than just SPI functionality. Default Value: 0
4	LATE_MISO_SAMPLE	Changes the SCLK edge on which MISO is captured. Only used in master mode. When '0', the default applies (for Motorola as determined by CPOL and CPHA, for Texas Instruments on the falling edge of SCLK and for National Semiconductors on the rising edge of SCLK). When '1', the alternate clock edge is used (which comes half a SPI SCLK period later). Late sam-pling addresses the round trip delay associated with transmitting SCLK from the master to the slave and transmitting MISO from the slave to the master. Default Value: 0
3	CPOL	Indicates the clock polarity. This field, together with the CPHA field, indicates when MOSI data is driven and MISO data is captured: - CPOL is 0: SCLK is 0 when not transmitting data. - CPOL is 1: SCLK is 1 when not transmitting data. Default Value: 0

25.1.2 SCB0_SPI_CTRL (continued)

2	CPHA	Indicates the clock phase. This field, together with the CPOL field, indicates when MOSI data is driven and MISO data is captured: - Motorola mode 0. CPOL is 0, CPHA is 0: MOSI is driven on a falling edge of SCLK. MISO is captured on a rising edge of SCLK. - Motorola mode 1. CPOL is 0, CPHA is 1: MOSI is driven on a rising edge of SCLK. MISO is captured on a falling edge of SCLK. - Motorola mode 2. CPOL is 1, CPHA is 0: MOSI is driven on a rising edge of SCLK. MISO is captured on a falling edge of SCLK. - Motorola mode 3. CPOL is 1, CPHA is 1: MOSI is driven on a falling edge of SCLK. MISO is captured on a rising edge of SCLK. In SPI Motorola submode, all four CPOL/CPHA modes are valid. in SPI NS submode, only CPOL=0 CPHA=0 mode is valid. in SPI TI submode, only CPOL=0 CPHA=1 mode is valid. Default Value: 0
1	SELECT_PRECEDE	Only used in SPI Texas Instruments' submode. When '1', the data frame start indication is a pulse on the Slave SELECT line that precedes the transfer of the first data frame bit. When '0', the data frame start indication is a pulse on the Slave SELECT line that coincides with the transfer of the first data frame bit. Default Value: 0
0	SSEL_CONTINUOUS	Continuous SPI data transfers enabled ('1') or not ('0'). This field is used in master mode. In slave mode, both continuous and non-continuous SPI data transfers are supported independent of this field. When continuous transfers are enabled indiviual data transfers are NOT seperated by slave select deselection as long as there is data in the TX FIFO. If the TX FIFO becomes empty then the slave select will be deselected. When continuous transfers are not enabled individual data frame transfers are always seperated by slave select deselection: independent of the availability of TX FIFO data frames. Default Value: 0

25.1.3 SCB0_SPI_STATUS

SPI status

Address: 0x40610024

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							W
Name	None [7:1]							BUS_BUSY

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	BUS_BUSY	SPI bus is busy. The bus is considered busy ('1') during an ongoing transaction. For Motorola and National submodes, the busy bit is '1', when the slave selection is activated. For TI submode, the busy bit is '1' from the time the preceding/coinciding slave select is activated for the first transmitted data frame, till the last MOSI/MISO bit of the last data frame is transmitted. Default Value: Undefined

25.1.4 SCB0_UART_CTRL

UART control

Address: 0x40610040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							LOOPBACK

Bits	31	30	29	28	27	26	25	24
SW Access	None						RW	
HW Access	None						R	
Name	None [31:26]						MODE [25:24]	

Bits	Name	Description
25 : 24	MODE	Submode of UART operation (3: Reserved) Default Value: 3 **0x0: UART_STD :** Standard UART submode. **0x1: UART_SMARTCARD :** SmartCard (ISO7816) submode. Support for negative acknowledgement (NACK) on the receiver side and retransmission on the transmitter side. **0x2: UART_IRDA :** Infrared Data Association (IrDA) submode. Return to Zero modulation scheme.
16	LOOPBACK	Local loopback control (does NOT affect the information on the pins). 0: Loopback is not enabled 1: UART_TX is connected to UART_RX. UART_RTS is connected to UART_CTS. This allows a SCB UART transmitter to communicate with its receiver counterpart. Default Value: 0

25.1.5 SCB0_UART_TX_CTRL

UART transmitter control

Address: 0x40610044

Retention: Retained

<table>
<tr><th>Bits</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td>SW Access</td><td colspan="2">None</td><td>RW</td><td>RW</td><td>None</td><td colspan="3">RW</td></tr>
<tr><td>HW Access</td><td colspan="2">None</td><td>R</td><td>R</td><td>None</td><td colspan="3">R</td></tr>
<tr><td>Name</td><td colspan="2">None [7:6]</td><td>PARI-
TY_EN-
ABLED</td><td>PARITY</td><td>None</td><td colspan="3">STOP_BITS [2:0]</td></tr>
</table>

<table>
<tr><th>Bits</th><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th></tr>
<tr><td>SW Access</td><td colspan="7">None</td><td>RW</td></tr>
<tr><td>HW Access</td><td colspan="7">None</td><td>R</td></tr>
<tr><td>Name</td><td colspan="7">None [15:9]</td><td>RE-
TRY_ON_N
ACK</td></tr>
</table>

<table>
<tr><th>Bits</th><th>23</th><th>22</th><th>21</th><th>20</th><th>19</th><th>18</th><th>17</th><th>16</th></tr>
<tr><td>SW Access</td><td colspan="8">None</td></tr>
<tr><td>HW Access</td><td colspan="8">None</td></tr>
<tr><td>Name</td><td colspan="8">None [23:16]</td></tr>
</table>

<table>
<tr><th>Bits</th><th>31</th><th>30</th><th>29</th><th>28</th><th>27</th><th>26</th><th>25</th><th>24</th></tr>
<tr><td>SW Access</td><td colspan="8">None</td></tr>
<tr><td>HW Access</td><td colspan="8">None</td></tr>
<tr><td>Name</td><td colspan="8">None [31:24]</td></tr>
</table>

Bits	Name	Description
8	RETRY_ON_NACK	When '1', a data frame is retransmitted when a negative acknowledgement is received. Only applicable to the SmartCard submode. Default Value: 0
5	PARITY_ENABLED	Parity generation enabled ('1') or not ('0'). Only applicable in standard UART submodes. In SmartCard submode, parity generation is always enabled through hardware. In IrDA submode, parity generation is always disabled through hardware Default Value: 0
4	PARITY	Parity bit. When '0', the transmitter generates an even parity. When '1', the transmitter generates an odd parity. Only applicable in standard UART and SmartCard submodes. Default Value: 0
2 : 0	STOP_BITS	Stop bits. STOP_BITS + 1 is the duration of the stop period in terms of haf bit periods. Valid range is [1, 7]; i.e. a stop period should last at least one bit period. Default Value: 2

25.1.6 SCB0_UART_RX_CTRL

UART receiver control

Address: 0x40610048

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	RW	RW	None	RW		
HW Access	None	R	R	R	None	R		
Name	None	POLARITY	PARI-TY_EN-ABLED	PARITY	None	STOP_BITS [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW	RW	None	RW	RW	RW
HW Access	None		R	R	None	R	R	R
Name	None [15:14]		SKIP_START	LIN_MODE	None	MP_MODE	DROP_ON_FRAME_ERROR	DROP_ON_PARI-TY_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				BREAK_WIDTH [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	BREAK_WIDTH	Break width. BREAK_WIDTH + 1 is the minimum width in bit periods of a break. During a break the transmitted/received line value is '0'. This feature is useful for standard UART submode and LIN submode ("break field" detection). Once, the break is detected, the INTR_RX.BREAK_DETECT bit is set to '1'. Note for LIN the break detection precedes baud rate detection, which is used to synchronize/refine the receiver clock to the transmitter clock. As a result, break detection operates with an unsynchronized/unrefined receiver clock. Therefore, the receiver's definition of a bit period is imprecise and the setting of this field should take this imprecision into account. The LIN standard also accounts for this imprecision: a LIN start bit followed by 8 data bits allows for up to 9 consecutive '0' bit periods during regular transmission, whereas the LIN break detection should be at least 13 consecutive '0' bit periods. This provides for a margin of 4 bit periods. Therefore, the default value of this field is set to 10, representing a minimal break field with of 10+1 = 11 bit periods; a value in between the 9 consecutive bit periods of a regular transmission and the 13 consecutive bit periods of a break field. This provides for slight imprecisions of the receiver clock wrt. the transmitter clock. There should not be a need to program this field to any value other than its default value. Default Value: 10

25.1.6 SCB0_UART_RX_CTRL (continued)

13	SKIP_START	Only applicable in standard UART submode. When '1', the receiver skips start bit detection for the first received data frame. Instead, it synchronizes on the first received data frame bit, which should be a '1'. This functionality is intended for wake up from DeepSleep when receiving a data frame. The transition from idle ('1') to START ('0') on the RX line is used to wake up the CPU. The transition detection (and the associated wake up functionality) is performed by the GPIO. The woken up CPU will enable the SCB's UART receiver functionality. Once enabled, it is assumed that the START bit is ongoing (the CPU wakeup and SCB enable time should be less than the START bit period). The SCB will then synchronize to a '0' to '1' transition, which indicates the first data frame bit is received (first data frame bit should be '1'). After synchronization to the first data frame bit, the SCB will resume normal UART functionality: subsequent data frames will be synchronized on the receipt of a START bit. Default Value: 0
12	LIN_MODE	Only applicable in standard UART submode. When '1', the receiver performs break detection and baud rate detection on the incoming data. First, break detection counts the amount of bit periods that have a line value of '0'. BREAK_WIDTH specifies the minum required amount of bit periods. Successful break detection sets the INTR_RX.BREAK_DETECT interrupt cause to '1'. Second, baud rate detection counts the amount of peripheral clock periods that are use to receive the synchronization byte (0x55; least significant bit first). The count is available through UART_RX_STATUS.BR_COUNTER. Successful baud rate detection sets the INTR_RX.BAUD_DETECT interrupt cause to '1' (BR_COUNTER is reliable). This functionality is used to synchronize/refine the receiver clock to the transmitter clock. The receiver software can use the BR_COUNTER value to set the right clk_scb to guarantee successful receipt of the first LIN data frame (Protected Identifier Field) after the synchronization byte. Default Value: 0
10	MP_MODE	Multi-processor mode. When '1', multi-processor mode is enabled. In this mode, RX_CTRL.DATA_WIDTH must be 9 bits. In multi-processor mode, the 9th received bit of a data frame seperates addresses (bit is '1') from data (bit is '0'). A received address is matched with RX_MATCH.DATA and RX_MATCH.MASK. In the case of a match, subsequent received data is sent to the RX FIFO. In the case of NO match, subsequent received data is dropped. Default Value: 0
9	DROP_ON_FRAME_ERROR	Behaviour when an error is detected in a start or stop period. When '0', received data is sent to the RX FIFO. When '1', received data is dropped and lost. Default Value: 0
8	DROP_ON_PARITY_ERROR	Behavior when a parity check fails. When '0', received data is send to the RX FIFO. When '1', received data is dropped and lost. Only applicable in standard UART and SmartCard submodes (negatively acknowledged SmartCard data frames may be dropped with this field). Default Value: 0
6	POLARITY	Inverts incoming RX line signal "uart_rx_in". Inversion is after local loopback. This functionality only works for IrDA receiver functionality. Default Value: 0
5	PARITY_ENABLED	Parity checking enabled ('1') or not ('0'). Only applicable in standard UART submode. In SmartCard submode, parity checking is always enabled through hardware. In IrDA submode, parity checking is always disabled through hardware. Default Value: 0
4	PARITY	Parity bit. When '0', the receiver expects an even parity. When '1', the receiver expects an odd parity. Only applicable in standard UART and SmartCard submodes. Default Value: 0

25.1.6 SCB0_UART_RX_CTRL (continued)

2 : 0	STOP_BITS	Stop bits. STOP_BITS + 1 is the duration of the stop period in terms of haf bit periods. Valid range is [1, 7]; i.e. a stop period should last at least one bit period. If STOP_BITS is '1', stop bits error detection is NOT performed. If STOP_BITS is in [2, 7], stop bits error detection is performed and the associated interrupt cause INTR_RX.FRAME_ERROR is set to '1' if an error is detected. In other words, the receiver supports data frames with a 1 bit period stop bit sequence, but requires at least 1.5 bit period stop bit sequences to detect errors. Note that in case of a stop bits error, the successive data frames may get lost as the receiver needs to resynchronize its start bit detection. The amount of lost data frames depends on both the amount of stop bits, the idle time between data frames and the data frame value. Default Value: 2

25.1.7 SCB0_UART_RX_STATUS

UART receiver status

Address: 0x4061004C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	BR_COUNTER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None				R			
HW Access	None				W			
Name	None [15:12]				BR_COUNTER [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11 : 0	BR_COUNTER	For LIN: Amount of clk_scb periods that constitute the transmission of a 0x55 data frame (sent least signficant bit first) as determined by the receiver. BR_COUNTER / 8 is the amount of clk_scb periods that constitute a bit period. This field has valid data when INTR_RX.BAUD_DE-TECT is set to '1'. Default Value: Undefined

25.1.8 SCB0_UART_FLOW_CTRL

UART flow control

Address: 0x40610050

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW						
HW Access	None	R						
Name	None	TRIGGER_LEVEL [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							RTS_POLARITY

Bits	31	30	29	28	27	26	25	24
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [31:26]						CTS_ENABLED	CTS_POLARITY

Bits	Name	Description
25	CTS_ENABLED	Enable use of CTS input signal by the UART transmitter: '0': Disabled. The UART transmitter ignores the CTS input signal and transmits when a data frame is available for transmission in the TX FIFO or the TX shift register. '1': Enabled. The UART transmitter uses CTS input signal to qualify the transmission of data. It transmits when CTS input signal is active and a data frame is available for transmission in the TX FIFO or the TX shift register. If UART_CTRL.LOOPBACK is '1', the CTS input signal is driven by the RTS output signal locally in SCB (both signals are subjected to signal polarity changes are indicated by RTS_POLARITY and CTS_POLARITY). Default Value: 0
24	CTS_POLARITY	Polarity of the CTS input signal '0': CTS is active low ; '1': CTS is active high; Default Value: 0

25.1.8 SCB0_UART_FLOW_CTRL (continued)

16	RTS_POLARITY	Polarity of the RTS output signal: '0': RTS is active low; '1': RTS is active high; During SCB reset (Hibernate system power mode), RTS output signal is '1'. This represents an inactive state assuming an active low polarity. Default Value: 0
6 : 0	TRIGGER_LEVEL	Trigger level. When the receiver FIFO has less entries than the amount of this field, a Ready To Send (RTS) output signal is activated. By setting this field to "0", flow control is disabled Default Value: 0

25.1.9 SCB0_I2C_CTRL

I2C control

Address: 0x40610060

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	LOW_PHASE_OVS [7:4]				HIGH_PHASE_OVS [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	None	RW	RW
HW Access	R	R	R	R	R	None	R	R
Name	S_NOT_READY_DATA_NACK	S_NOT_READY_ADDR_NACK	S_READY_DATA_ACK	S_READY_ADDR_ACK	S_GENERAL_IGNORE	None	M_NOT_READY_DATA_NACK	M_READY_DATA_ACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							LOOPBACK

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None					
HW Access	R	R	None					
Name	MASTER_MODE	SLAVE_MODE	None [29:24]					

Bits	Name	Description
31	MASTER_MODE	Master mode enabled ('1') or not ('0'). Note that both master and slave modes can be enabled at the same time. This allows the SCB to address itself. Default Value: 0
30	SLAVE_MODE	Slave mode enabled ('1') or not ('0'). Default Value: 0
16	LOOPBACK	Local loopback control (does NOT affect the information on the pins). Only applicable in master/slave mode. When '0', no loopback When '1', loopback is enabled internally in the peripheral, and as a result unaffected by other I2C devices. This allows a SCB I2C peripheral to address itself. Default Value: 0

25.1.9 SCB0_I2C_CTRL (continued)

15	S_NOT_READY_-DATA_NACK	Only used for FIFO mode, NOT EZ or CMD_RESP mode. Functionality is as follows: - 1: a received data element byte the slave is immediately NACK'd when the receiver FIFO is full. - 0: clock stretching is performed (till the receiver FIFO is no longer full). Default Value: 1
14	S_NOT_READY_AD-DR_NACK	Only used for FIFO mode, NOT EZ or CMD_RESP mode. Functionality is as follows: - 1: In Active/Sleep mode a received (matching) slave address is immediately NACK'd when the RX FIFO is full In DeepSleep power mode when EC_AM = '1' and EC_OP = '0' clk_scb is not avaliable, so the incoming address will be NACK'd until the clock is avaliable. Once clk_scb is avaliable the address ACK will follow S_READY_ADDR_ACK - 0: in Active/Sleep mode clock stretching is performed when the RX FIFO is full, the strech is released when the RX FIFO is no longer full. In DeepSleep power mode when EC_AM = '1' and EC_OP = '0' clk_scb is not avaliable, so the clocked will be streched on an incoming address until clk_scb is avaliable. After clk_scb is avalaible the address ACK will follow S_READY_ADDR_ACK Default Value: 1
13	S_READY_DATA_ACK	When '1', a received data element by the slave is immediately ACK'd when the RX FIFO is not full. In EZ and CMD_RESP mode, this field should be set to '1'. When '0' the data must be ACK/NACK'd by the CPU using I2C_S_CMD.S_ACK or I2C_S_CMD.S_NACK Default Value: 1
12	S_READY_ADDR_ACK	When '1', a received (matching) slave address is immediately ACK'd when the RX FIFO is not full. In EZ and CMD_RESP mode, this field should be set to '1'. When '0' the address must be ACK/NACK'd by the CPU using I2C_S_CMD.S_ACK or I2C_S_CMD.S_NACK Default Value: 1
11	S_GENERAL_IGNORE	When '1', a received general call slave address is immediately NACK'd (no ACK or clock stretching) and treated as a non matching slave address. This is useful for slaves that do not need any data supplied within the general call structure. When '0' the general call address is accepted and follows S_READY_ADDR_ACK and S_NOT_READY_ADDR_NACK Default Value: 1
9	M_NOT_READY_-DATA_NACK	When '1', a received data element by the master is immediately NACK'd when the RX FIFO is full. When '0', clock stretching is used instead (till the RX FIFO is no longer full). Default Value: 1
8	M_READY_DATA_ACK	When '1', a received data element by the master is immediately ACK'd when the RX FIFO is not full. When '0' the CPU is responsible for ACK/NACKing the received data frame using I2C_M_CMD.M_ACK or I2C_M_CMD.M_NACK Default Value: 1
7 : 4	LOW_PHASE_OVS	Serial I2C interface low phase oversampling factor. (LOW_PHASE_OVS + 1) * clk_scb constitutes the low phase of a bit period. The valid range is [7, 15] with input signal median filtering and [6, 15] without input signal median filtering. The field is only used in master mode. In slave mode, the field is NOT used. See architecture TRM for information on slave data rate requirments. Default Value: 8
3 : 0	HIGH_PHASE_OVS	Serial I2C interface high phase oversampling factor. (HIGH_PHASE_OVS + 1) * clk_scb constitutes the high phase of a bit period. The valid range is [5, 15] with input signal median filtering and [4, 15] without input signal median filtering. The field is only used in master mode. In slave mode, the field is NOT used. See architecture TRM for information on slave data rate requirments. Default Value: 8

25.1.10 SCB0_I2C_STATUS

I2C status

Address: 0x40610064

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R	R	None			R
HW Access	None		W	W	None			W
Name	None [7:6]		M_READ	S_READ	None [3:1]			BUS_BUSY

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	M_READ	I2C master read transfer ('1') or I2C master write transfer ('0'). When the I2C master is inactive/ idle or transmitting START, REPEATED START, STOP or an address, this field is '0". Default Value: 0
4	S_READ	I2C slave read transfer ('1') or I2C slave write transfer ('0'). When the I2C slave is inactive/idle or receiving START, REPEATED START, STOP or an address, this field is '0". Default Value: 0
0	BUS_BUSY	I2C bus is busy. The bus is considered busy ('1'), from the time a START is detected or from the time the SCL line is '0'. The bus is considered idle ('0'), from the time a STOP is detected. If the SCB is disabled, BUS_BUSY is '0'. After enabling the SCB, it takes time for the BUS_BUSY to detect a busy bus. This time is the maximum high time of the SCL line. For a 100 kHz interface frequency, this maximum high time may last roughly 5 us (half a bit period). For single master systems, BUS_BUSY does not have to be used to detect an idle bus before a master starts a transfer using I2C_M_CMD.M_START (no bus collisions). For multi-master systems, BUS_BUSY can be used to detect an idle bus before a master starts a transfer using I2C_M_CMD.M_START_ON_IDLE (to prevent bus collisions). Default Value: 0

25.1.11 SCB0_I2C_M_CMD

I2C master command

Address: 0x40610068

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			RW1C	RW1C	RW1C	RW1C	RW1C
Name	None [7:5]			M_STOP	M_NACK	M_ACK	M_START_ON_IDLE	M_START

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4	M_STOP	When '1', attempt to transmit a STOP. When this action is performed, the hardware sets this field to '0'. I2C_M_CMD.M_START has a higher priority than this command: in situations where both a STOP and a REPEATED START could be transmitted, M_START takes precedence over M_STOP. Default Value: 0
3	M_NACK	When '1', attempt to transmit a negative acknowledgement (NACK). When this action is performed, the hardware sets this field to '0'. Default Value: 0
2	M_ACK	When '1', attempt to transmit an acknowledgement (ACK). When this action is performed, the hardware sets this field to '0'. Default Value: 0

25.1.11 SCB0_I2C_M_CMD (continued)

1	M_START_ON_IDLE	When '1', transmit a START as soon as the bus is idle (I2C_STATUS.BUS_BUSY is '0', note that BUSY has a default value of '0'). For bus idle detection the hardware relies on STOP detection. As a result, bus idle detection is only functional after at least one I2C bus transfer has been detected on the bus (default/reset value of BUSY is '0') . A START is only transmitted when the master state machine is in the default state. When this action is performed, the hardware sets this field to '0'. Default Value: 0
0	M_START	When '1', transmit a START or REPEATED START. Whether a START or REPEATED START is transmitted depends on the state of the master state machine. A START is only transmitted when the master state machine is in the default state. A REPEATED START is transmitted when the master state machine is not in the default state, but is working on an ongoing transaction. The REPEATED START can only be transmitted after a NACK or ACK has been received for a transmitted data element or after a NACK has been transmitted for a received data element. When this action is performed, the hardware sets this field to '0'. Default Value: 0

25.1.12 SCB0_I2C_S_CMD

I2C slave command

Address: 0x4061006C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						RW1C	RW1C
Name	None [7:2]						S_NACK	S_ACK

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	S_NACK	When '1', attempt to transmit a negative acknowledgement (NACK). When this action is performed, the hardware sets this field to '0'. In EZ and CMD_RESP mode, this field should be set to '0' (it is only to be used in FIFO mode). This command has a higher priority than I2C_S_CMD.S_ACK, I2C_CTRL.S_READY_ADDR_ACK or I2C_CTRL.S_READY_DATA_ACK. Default Value: 0
0	S_ACK	When '1', attempt to transmit an acknowledgement (ACK). When this action is performed, the hardware sets this field to '0'. In EZ and CMD_RESP mode, this field should be set to '0' (it is only to be used in FIFO mode). Default Value: 0

25.1.13 SCB0_I2C_CFG

I2C configuration

Address: 0x40610070

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	None		RW	
HW Access	None			R	None		R	
Name	None [7:5]			SDA_IN_-FILT_SEL	None [3:2]		SDA_IN_FILT_TRIM [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	None		RW	
HW Access	None			R	None		R	
Name	None [15:13]			SCL_IN_-FILT_SEL	None [11:10]		SCL_IN_FILT_TRIM [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW		RW		RW	
HW Access	None		R		R		R	
Name	None [23:22]		SDA_OUT_FILT2_TRIM [21:20]		SDA_OUT_FILT1_TRIM [19:18]		SDA_OUT_FILT0_TRIM [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None		RW		None			
HW Access	None		R		None			
Name	None [31:30]		SDA_OUT_FILT_SEL [29:28]		None [27:24]			

Bits	Name	Description
29 : 28	SDA_OUT_FILT_SEL	Selection of cumulative "i2c_sda_out" filter delay: "0": 0 ns. "1": 50 ns (filter 0 enabled). "2": 100 ns (filters 0 and 1 enabled). "3": 150 ns (filters 0, 1 and 2 enabled). Default Value: 0
21 : 20	SDA_OUT_FILT2_TRIM	Trim bits for "i2c_sda_out" 50 ns filter 2. Not to be modified by the user Default Value: 2
19 : 18	SDA_OUT_FILT1_TRIM	Trim bits for "i2c_sda_out" 50 ns filter 1. Not to be modified by the user Default Value: 2
17 : 16	SDA_OUT_FILT0_TRIM	Trim bits for "i2c_sda_out" 50 ns filter 0. Not to be modified by the user Default Value: 2

25.1.13 SCB0_I2C_CFG (continued)

12	SCL_IN_FILT_SEL	Selection of "i2c_scl_in" filter delay: '0': 0 ns. '1: 50 ns (filter enabled). Default Value: 1
9 : 8	SCL_IN_FILT_TRIM	Trim bits for "i2c_scl_in" 50 ns filter. Not to be modified by the user Default Value: 0
4	SDA_IN_FILT_SEL	Selection of "i2c_sda_in" filter delay: '0': 0 ns. '1: 50 ns (filter enabled). Default Value: 1
1 : 0	SDA_IN_FILT_TRIM	Trim bits for "i2c_sda_in" 50 ns filter. SDA_IN_FILT_TRIM[1] is used to enable I2CS_EC or SPIS_EC access to internal EZ memory. 1: enable clk_scb 0: disable clk_scb Before going to deepsleep this field should be set to 0. It should be re-enabled once the device is awoken and clk_hf[0] is at the desired frequency. Default Value: 3

25.1.14 SCB0_TX_CTRL

Transmitter control

Address: 0x40610200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				DATA_WIDTH [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							MSB_-FIRST

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							OPEN_DRAIN

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
16	OPEN_DRAIN	Each IO cell "xxx" has two associated SCB output signals "xxx_out_en" and "xxx_out". This field determines how the SCB controls those two signals. Consult the GPIO chapter in the architecture TRM to understand how the pin drive modes behave when connected to SCBs. '0': Normal operation mode. In this operation mode "xxx_out_en" output enable signal is typically constant '1' the "xxx_out" output is the outputted value. In other words, in normal operation mode, the "xxx_out" output is used to control the IO cell output value: "xxx_out" is '0' to drive an IO cell output value of '0' and "xxx_out" is '1' to drive an IO cell output value of '1'. '1': Open drain operation mode. In this operation mode "xxx_out_en" output controls the outputted value. Typically the "xxx_out" signal is a constant "0". Thus when "xxx_out_en" is "1" the line is driven low, but when "xxx_out_en" is "0" the output is not driven. This requires that the line is driven high by an external device or pull-up resistor The open drain mode is supported for: - I2C mode this field must be set. - UART mode use this mode when a pull-up resistor is used on the TX line. - SPI mode this field must be set if there are multiple slaves driving MISO. Default Value: 0

25.1.14 SCB0_TX_CTRL (continued)

8	MSB_FIRST	Least significant bit first ('0') or most significant bit first ('1'). For I2C, this field should be '1'. For EZ and CMD_RESP this field must be set to "1" Default Value: 1
3 : 0	DATA_WIDTH	Dataframe width. DATA_WIDTH + 1 is the amount of bits in a transmitted data frame. This number does not include start, parity and stop bits. For UART mode, the valid range is [3, 8]. For SPI, the valid range is [3, 15]. For I2C the only valid value is 7. In EZ and CMD_RESP mode (for both SPI and I2C), the only valid value is 7. Default Value: 7

25.1.15 SCB0_TX_FIFO_CTRL

Transmitter FIFO control

Address: 0x40610204

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW						
HW Access	None	R						
Name	None	TRIGGER_LEVEL [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [23:18]						FREEZE	CLEAR

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
17	FREEZE	When '1', hardware reads from the transmitter FIFO do not remove FIFO entries. Freeze will not advance the TX FIFO read pointer. Default Value: 0
16	CLEAR	When '1', the transmitter FIFO and transmitter shift register are cleared/invalidated. Invalidation will last for as long as this field is '1'. If a quick clear/invalidation is required, the field should be set to '1' and be followed by a set to '0'. If a clear/invalidation is required for an extended time period, the field should be set to '1' during the complete time period. Default Value: 0
6 : 0	TRIGGER_LEVEL	Trigger level. When the transmitter FIFO has less entries than the number of this field, a transmitter trigger event is generated. Default Value: 0

25.1.16 SCB0_TX_FIFO_STATUS

Transmitter FIFO status

Address: 0x40610208

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	USED [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R	None						
HW Access	W	None						
Name	SR_VALID	None [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	None	R						
HW Access	None	W						
Name	None	RD_PTR [22:16]						

Bits	31	30	29	28	27	26	25	24
SW Access	None	R						
HW Access	None	W						
Name	None	WR_PTR [30:24]						

Bits	Name	Description
30 : 24	WR_PTR	FIFO write pointer: FIFO location at which a new data frame is written. Default Value: 0
22 : 16	RD_PTR	FIFO read pointer: FIFO location from which a data frame is read by the hardware. Default Value: 0
15	SR_VALID	Indicates whether the TX shift registers holds a valid data frame ('1') or not ('0'). The shift register can be considered the top of the TX FIFO (the data frame is not included in the USED field of the TX FIFO). The shift register is a working register and holds the data frame that is currently transmitted (when the protocol state machine is transmitting a data frame) or the data frame that is transmitted next (when the protocol state machine is not transmitting a data frame). Default Value: 0
7 : 0	USED	Amount of entries in the transmitter FIFO. The value of this field ranges from 0 to FF_DATA_NR. Default Value: 0

25.1.17 SCB0_TX_FIFO_WR

Transmitter FIFO write

Address: 0x40610240

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATA	Data frame written into the transmitter FIFO. Behavior is similar to that of a PUSH operation. Note that when CTRL.BYTE_MODE is '1', only DATA[7:0] are used. A write to a full TX FIFO sets INTR_TX.OVERFLOW to '1'. Default Value: 0

25.1.18 SCB0_RX_CTRL

Receiver control

Address: 0x40610300

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				DATA_WIDTH [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [15:10]						MEDIAN	MSB_-FIRST

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	MEDIAN	Median filter. When '1', a digital 3 taps median filter is performed on input interface lines. This filter should reduce the susceptibility to errors. However, its requires higher oversampling values. For UART IrDA submode, this field should always be '1'. Default Value: 0
8	MSB_FIRST	Least significant bit first ('0') or most significant bit first ('1'). For I2C, this field should be '1'. For EZ and CMD_RESP this field must be set to "1" Default Value: 1
3 : 0	DATA_WIDTH	Dataframe width. DATA_WIDTH + 1 is the expected amount of bits in received data frame. This number does not include start, parity and stop bits. For UART mode, the valid range is [3, 8]. For SPI, the valid range is [3, 15]. For I2C the only valid value is 7. In EZ mode (for both SPI and I2C), the only valid value is 7. Default Value: 7

25.1.19 SCB0_RX_FIFO_CTRL

Receiver FIFO control

Address: 0x40610304

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW						
HW Access	None	R						
Name	None	TRIGGER_LEVEL [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [23:18]						FREEZE	CLEAR

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
17	FREEZE	When '1', hardware writes to the receiver FIFO have no effect. Freeze will not advance the RX FIFO write pointer. Default Value: 0
16	CLEAR	When '1', the receiver FIFO and receiver shift register are cleared/invalidated. Invalidation will last for as long as this field is '1'. If a quick clear/invalidation is required, the field should be set to '1' and be followed by a set to '0'. If a clear/invalidation is required for an extended time period, the field should be set to '1' during the complete time period. Default Value: 0
6 : 0	TRIGGER_LEVEL	Trigger level. When the receiver FIFO has more entries than the number of this field, a receiver trigger event is generated. Default Value: 0

25.1.20 SCB0_RX_FIFO_STATUS

Receiver FIFO status

Address: 0x40610308

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	USED [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R	None						
HW Access	W	None						
Name	SR_VALID	None [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	None	R						
HW Access	None	W						
Name	None	RD_PTR [22:16]						

Bits	31	30	29	28	27	26	25	24
SW Access	None	R						
HW Access	None	W						
Name	None	WR_PTR [30:24]						

Bits	Name	Description
30 : 24	WR_PTR	FIFO write pointer: FIFO location at which a new data frame is written by the hardware. Default Value: 0
22 : 16	RD_PTR	FIFO read pointer: FIFO location from which a data frame is read. Default Value: 0
15	SR_VALID	Indicates whether the RX shift registers holds a (partial) valid data frame ('1') or not ('0'). The shift register can be considered the bottom of the RX FIFO (the data frame is not included in the USED field of the RX FIFO). The shift register is a working register and holds the data frame that is currently being received (when the protocol state machine is receiving a data frame). Default Value: 0
7 : 0	USED	Amount of entries in the receiver FIFO. The value of this field ranges from 0 to FF_DATA_NR. Default Value: 0

25.1.21 SCB0_RX_MATCH

Slave address and mask

Address: 0x40610310

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	MASK [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	MASK	Slave device address mask. This field is a mask that specifies which of the ADDR field bits in the ADDR field take part in the matching of the slave address: MATCH = ((ADDR & MASK) == ("slave address" & MASK)). Default Value: 0
7 : 0	ADDR	Slave device address. In UART multi-processor mode, all 8 bits are used. In I2C slave mode, only bits 7 down to 1 are used. This reflects the organization of the first transmitted byte in a I2C transfer: the first 7 bits represent the address of the addressed slave, and the last 1 bit is a read/write indicator ('0': write, '1': read). Default Value: 0

25.1.22 SCB0_RX_FIFO_RD

Receiver FIFO read

Address: 0x40610340

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATA	Data read from the receiver FIFO. Reading a data frame will remove the data frame from the FIFO; i.e. behavior is similar to that of a POP operation. Note that when CTRL.BYTE_MODE is '1', only DATA[7:0] are used. When in debug mode a read from this register behaves as a read from the SCB_RX_FIFO_RD_-SILENT register. That is data will not be removed from the FIFO A read from an empty RX FIFO sets INTR_RX.UNDERFLOW to '1'. Default Value: Undefined

25.1.23 SCB0_RX_FIFO_RD_SILENT

Receiver FIFO read silent

Address: 0x40610344

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATA	Data read from the receiver FIFO. Reading a data frame will NOT remove the data frame from the FIFO; i.e. behavior is similar to that of a PEEK operation. Note that when CTRL.BYTE_-MODE is '1', only DATA[7:0] are used. A read from an empty RX FIFO sets INTR_RX.UNDERFLOW to '1'. Default Value: Undefined

25.1.24 SCB0_EZ_DATA0

Memory buffer

Address: 0x40610400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be de-tected by reading back the written value, or checking the field BLOCKED of the INTR_TX and INTR_RX registers Default Value: Undefined

25.1.25 SCB0_INTR_CAUSE

Active clocked interrupt signal

Address: 0x40610E00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R	R	R	R
HW Access	None				W	W	W	W
Name	None [7:4]				RX	TX	S	M

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	RX	Receiver interrupt active ("interrupt_rx"): INTR_RX_MASKED != 0. Default Value: 0
2	TX	Transmitter interrupt active ("interrupt_tx"): INTR_TX_MASKED != 0. Default Value: 0
1	S	Slave interrupt active ("interrupt_slave"): INTR_S_MASKED != 0. Default Value: 0
0	M	Master interrupt active ("interrupt_master"): INTR_M_MASKED != 0. Default Value: 0

25.1.26 SCB0_INTR_M

Master interrupt request

Address: 0x40610F00

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW1C	None	RW1C	RW1C	RW1C
HW Access	None			RW1S	None	RW1S	RW1S	RW1S
Name	None [7:5]			I2C_STOP	None	I2C_ACK	I2C_NACK	I2C_AR-B_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW1C	RW1C
HW Access	None						RW1S	RW1S
Name	None [15:10]						SPI_DONE	I2C_BUS_E RROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

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Bits	Name	Description
9	SPI_DONE	SPI master transfer done event: all data frames in the transmit FIFO are sent, the transmit FIFO is empty (both TX FIFO and transmit shifter register are empty), and SPI select output pin is de-selected. Default Value: 0
8	I2C_BUS_ERROR	I2C master bus error (unexpected detection of START or STOP condition). Default Value: 0
4	I2C_STOP	I2C master STOP. Set to '1', when the master has transmitted a STOP. Default Value: 0
2	I2C_ACK	I2C master acknowledgement. Set to '1', when the master receives a ACK (typically after the master transmitted the slave address or TX data). Default Value: 0
1	I2C_NACK	I2C master negative acknowledgement. Set to '1', when the master receives a NACK (typically after the master transmitted the slave address or TX data). Default Value: 0

25.1.26 SCB0_INTR_M (continued)

0	I2C_ARB_LOST	I2C master lost arbitration: the value driven by the master on the SDA line is not the same as the value observed on the SDA line. Default Value: 0

25.1.27 SCB0_INTR_M_SET

Master interrupt set request

Address: 0x40610F04

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW1S	None	RW1S	RW1S	RW1S
HW Access	None			A	None	A	A	A
Name	None [7:5]			I2C_STOP	None	I2C_ACK	I2C_NACK	I2C_AR-B_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW1S	RW1S
HW Access	None						A	A
Name	None [15:10]						SPI_DONE	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	SPI_DONE	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
8	I2C_BUS_ERROR	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
4	I2C_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
2	I2C_ACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
1	I2C_NACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	I2C_ARB_LOST	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

25.1.28 SCB0_INTR_M_MASK

Master interrupt mask

Address: 0x40610F08

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	None	RW	RW	RW
HW Access	None			R	None	R	R	R
Name	None [7:5]			I2C_STOP	None	I2C_ACK	I2C_NACK	I2C_AR-B_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [15:10]						SPI_DONE	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	SPI_DONE	Mask bit for corresponding bit in interrupt request register. Default Value: 0
8	I2C_BUS_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
4	I2C_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	I2C_ACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	I2C_NACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	I2C_ARB_LOST	Mask bit for corresponding bit in interrupt request register. Default Value: 0

25.1.29 SCB0_INTR_M_MASKED

Master interrupt masked request

Address: 0x40610F0C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			R	None	R	R	R
HW Access	None			W	None	W	W	W
Name	None [7:5]			I2C_STOP	None	I2C_ACK	I2C_NACK	I2C_AR-B_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None						R	R
HW Access	None						W	W
Name	None [15:10]						SPI_DONE	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	SPI_DONE	Logical and of corresponding request and mask bits. Default Value: 0
8	I2C_BUS_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
4	I2C_STOP	Logical and of corresponding request and mask bits. Default Value: 0
2	I2C_ACK	Logical and of corresponding request and mask bits. Default Value: 0
1	I2C_NACK	Logical and of corresponding request and mask bits. Default Value: 0
0	I2C_ARB_LOST	Logical and of corresponding request and mask bits. Default Value: 0

25.1.30 SCB0_INTR_S

Slave interrupt request

Address: 0x40610F40

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
Name	I2C_GEN-ERAL	I2C_AD-DR_MATCH	I2C_START	I2C_STOP	I2C_WRITE_STOP	I2C_ACK	I2C_NACK	I2C_AR-B_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW1C	RW1C	RW1C	RW1C
HW Access	None				RW1S	RW1S	RW1S	RW1S
Name	None [15:12]				SPI_BUS_ERROR	SPI_EZ_STOP	SPI_EZ_WRITE_STOP	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	SPI_BUS_ERROR	SPI slave deselected at an unexpected time in the SPI transfer. Firmware may decide to clear the TX and RX FIFOs in case of this error. Default Value: 0
10	SPI_EZ_STOP	SPI slave deselected after any EZ SPI transfer occurred. Default Value: 0
9	SPI_EZ_WRITE_STOP	SPI slave deselected after a write EZ SPI transfer occurred. Default Value: 0
8	I2C_BUS_ERROR	I2C slave bus error (unexpected detection of START or STOP condition). This should not occur, it represents erroneous I2C bus behavior. In case of a bus error, the I2C slave state machine abort the ongoing transfer. Firmware may decide to clear the TX and RX FIFOs in case of this error. Default Value: 0

25.1.30 SCB0_INTR_S (continued)

7	I2C_GENERAL	I2C slave general call address received. If CTRL.ADDR_ACCEPT is set the received address 0x00 (including the R/W bit) is available in the RX FIFO. In the case of externally clocked address matching (CTRL.EC_AM_MODE is '1') and internally clocked operation (CTRL.EC_OP_MODE is '0'), this field is set when the event is detected. Default Value: 0
6	I2C_ADDR_MATCH	I2C slave matching address received. If CTRL.ADDR_ACCEPT, the received address (including the R/W bit) is available in the RX FIFO. In the case of externally clocked address matching (CTRL.EC_AM_MODE is '1') and internally clocked operation (CTRL.EC_OP_MODE is '0'), this field is set when the event is detected. Default Value: 0
5	I2C_START	I2C slave START received. Set to '1', when START or REPEATED START event is detected. In the case of externally clocked address matching (CTRL.EC_AM_MODE is '1') AND clock stretching is performed (till the internally clocked logic takes over) (I2C_CTRL.S_NOT_READY_ADDR_NACK is '0'), this field is NOT set. Firmware should use INTR_S_EC.WAKE_UP, INTR_S.I2C_ADDR_MATCH and INTR_S.I2C_GENERAL. Default Value: 0
4	I2C_STOP	I2C STOP event for I2C (read or write) transfer intended for this slave (address matching is performed). Set to '1', when STOP or REPEATED START event is detected. The REPEATED START event is included in this interrupt cause such that the I2C transfers separated by a REPEATED START can be distinguished and potentially treated separately by the Firmware. Note that the second I2C transfer (after a REPEATED START) may be to a different slave address. The event is detected on any I2C transfer intended for this slave. Note that a I2C address intended for the slave (address is matching) will result in a I2C_STOP event independent of whether the I2C address is ACK'd or NACK'd. Default Value: 0
3	I2C_WRITE_STOP	I2C STOP event for I2C write transfer intended for this slave (address matching is performed). Set to '1', when STOP or REPEATED START event is detected. The REPEATED START event is included in this interrupt cause such that the I2C transfers separated by a REPEATED START can be distinguished and potentially treated separately by the firmware. Note that the second I2C transfer (after a REPEATED START) may be to a different slave address. Note that a I2C write address intended for the slave (address is matching and a it is a write transfer) will result in a I2C_WRITE_STOP event independent of whether the I2C address is ACK'd or NACK'd. In EZ mode, the event is detected only on I2C write transfers that have EZ data written to the memory structure (an I2C write transfer that only communicates an I2C address and EZ base address, will not result in this event being detected). Default Value: 0
2	I2C_ACK	I2C slave acknowledgement received. Set to '1', when the slave receives a ACK (typically after the slave transmitted TX data). Default Value: 0
1	I2C_NACK	I2C slave negative acknowledgement received. Set to '1', when the slave receives a NACK (typically after the slave transmitted TX data). Default Value: 0
0	I2C_ARB_LOST	I2C slave lost arbitration: the value driven on the SDA line is not the same as the value observed on the SDA line (while the SCL line is '1'). This should not occur, it represents erroneous I2C bus behavior. In case of lost arbitration, the I2C slave state machine aborts the ongoing transfer. SW may decide to clear the TX and RX FIFOs in case of this error. Default Value: 0

25.1.31 SCB0_INTR_S_SET

Slave interrupt set request

Address: 0x40610F44

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	A	A	A	A	A	A	A	A
Name	I2C_GEN-ERAL	I2C_AD-DR_MATCH	I2C_START	I2C_STOP	I2C_WRITE_STOP	I2C_ACK	I2C_NACK	I2C_AR-B_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW1S	RW1S	RW1S	RW1S
HW Access	None				A	A	A	A
Name	None [15:12]				SPI_BUS_ERROR	SPI_EZ_STOP	SPI_EZ_WRITE_STOP	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	SPI_BUS_ERROR	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
10	SPI_EZ_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
9	SPI_EZ_WRITE_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
8	I2C_BUS_ERROR	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
7	I2C_GENERAL	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
6	I2C_ADDR_MATCH	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
5	I2C_START	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

25.1.31 SCB0_INTR_S_SET (continued)

4	I2C_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
3	I2C_WRITE_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
2	I2C_ACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
1	I2C_NACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	I2C_ARB_LOST	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

25.1.32 SCB0_INTR_S_MASK

Slave interrupt mask

Address: 0x40610F48

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	I2C_GEN-ERAL	I2C_AD-DR_MATCH	I2C_START	I2C_STOP	I2C_WRITE_STOP	I2C_ACK	I2C_NACK	I2C_AR-B_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [15:12]				SPI_BUS_ERROR	SPI_EZ_STOP	SPI_EZ_WRITE_STOP	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	SPI_BUS_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
10	SPI_EZ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
9	SPI_EZ_WRITE_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
8	I2C_BUS_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
7	I2C_GENERAL	Mask bit for corresponding bit in interrupt request register. Default Value: 0
6	I2C_ADDR_MATCH	Mask bit for corresponding bit in interrupt request register. Default Value: 0
5	I2C_START	Mask bit for corresponding bit in interrupt request register. Default Value: 0

25.1.32 SCB0_INTR_S_MASK (continued)

4	I2C_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
3	I2C_WRITE_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	I2C_ACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	I2C_NACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	I2C_ARB_LOST	Mask bit for corresponding bit in interrupt request register. Default Value: 0

25.1.33 SCB0_INTR_S_MASKED

Slave interrupt masked request

Address: 0x40610F4C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	I2C_GEN-ERAL	I2C_AD-DR_MATCH	I2C_START	I2C_STOP	I2C_WRITE_STOP	I2C_ACK	I2C_NACK	I2C_AR-B_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None				R	R	R	R
HW Access	None				W	W	W	W
Name	None [15:12]				SPI_BUS_ERROR	SPI_EZ_STOP	SPI_EZ_WRITE_STOP	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	SPI_BUS_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
10	SPI_EZ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
9	SPI_EZ_WRITE_STOP	Logical and of corresponding request and mask bits. Default Value: 0
8	I2C_BUS_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
7	I2C_GENERAL	Logical and of corresponding request and mask bits. Default Value: 0
6	I2C_ADDR_MATCH	Logical and of corresponding request and mask bits. Default Value: 0
5	I2C_START	Logical and of corresponding request and mask bits. Default Value: 0

25.1.33 SCB0_INTR_S_MASKED (continued)

4	I2C_STOP	Logical and of corresponding request and mask bits. Default Value: 0
3	I2C_WRITE_STOP	Logical and of corresponding request and mask bits. Default Value: 0
2	I2C_ACK	Logical and of corresponding request and mask bits. Default Value: 0
1	I2C_NACK	Logical and of corresponding request and mask bits. Default Value: 0
0	I2C_ARB_LOST	Logical and of corresponding request and mask bits. Default Value: 0

25.1.34 SCB0_INTR_TX

Transmitter interrupt request

Address: 0x40610F80

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW1C	RW1C	RW1C	None		RW1C	RW1C
HW Access	None	RW1S	RW1S	RW1S	None		RW1S	RW1S
Name	None	UNDER-FLOW	OVER-FLOW	EMPTY	None [3:2]		NOT_FULL	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW1C	RW1C	RW1C
HW Access	None					RW1S	RW1S	RW1S
Name	None [15:11]					UART_AR-B_LOST	UART_-DONE	UART_NAC K

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10	UART_ARB_LOST	UART lost arbitration: the value driven on the TX line is not the same as the value observed on the RX line. This condition event is usefull when transmitter and receiver share a TX/RX line. This is the case in LIN or SmartCard modes. Default Value: 0
9	UART_DONE	UART transmitter done event. This happens when the SCB is done transferring all data in the TX FIFO, and the last stop field is transmitted (both TX FIFO and transmit shifter register are empty). Default Value: 0
8	UART_NACK	UART transmitter received a negative acknowledgement in SmartCard mode. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
6	UNDERFLOW	Attempt to read from an empty TX FIFO. This happens when the SCB is ready to transfer data and EMPTY is '1'. Only used in FIFO mode. Default Value: 0

25.1.34 SCB0_INTR_TX (continued)

5	OVERFLOW	Attempt to write to a full TX FIFO. Only used in FIFO mode. Default Value: 0
4	EMPTY	TX FIFO is empty; i.e. it has 0 entries. Only used in FIFO mode. Default Value: 0
1	NOT_FULL	TX FIFO is not full. Dependent on CTRL.BYTE_MODE: BYTE_MODE is '0': # entries != FF_DATA_NR/2. BYTE_MODE is '1': # entries != FF_DATA_NR. Only used in FIFO mode. Default Value: 0
0	TRIGGER	Less entries in the TX FIFO than the value specified by TX_FIFO_CTRL. Only used in FIFO mode. Default Value: 0

25.1.35 SCB0_INTR_TX_SET

Transmitter interrupt set request

Address: 0x40610F84

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW1S	RW1S	RW1S	None		RW1S	RW1S
HW Access	None	A	A	A	None		A	A
Name	None	UNDER-FLOW	OVER-FLOW	EMPTY	None [3:2]		NOT_FULL	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW1S	RW1S	RW1S
HW Access	None					A	A	A
Name	None [15:11]					UART_AR-B_LOST	UART_-DONE	UART_NAC K

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10	UART_ARB_LOST	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
9	UART_DONE	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
8	UART_NACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
6	UNDERFLOW	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
5	OVERFLOW	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
4	EMPTY	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
1	NOT_FULL	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

25.1.35 SCB0_INTR_TX_SET (continued)

0	TRIGGER	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

25.1.36 SCB0_INTR_TX_MASK

Transmitter interrupt mask

Address: 0x40610F88

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	RW	RW	None		RW	RW
HW Access	None	R	R	R	None		R	R
Name	None	UNDER-FLOW	OVER-FLOW	EMPTY	None [3:2]		NOT_FULL	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [15:11]					UART_AR-B_LOST	UART_-DONE	UART_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10	UART_ARB_LOST	Mask bit for corresponding bit in interrupt request register. Default Value: 0
9	UART_DONE	Mask bit for corresponding bit in interrupt request register. Default Value: 0
8	UART_NACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
6	UNDERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
5	OVERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
4	EMPTY	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	NOT_FULL	Mask bit for corresponding bit in interrupt request register. Default Value: 0

25.1.36 SCB0_INTR_TX_MASK (continued)

0	TRIGGER	Mask bit for corresponding bit in interrupt request register. Default Value: 0

25.1.37 SCB0_INTR_TX_MASKED

Transmitter interrupt masked request

Address: 0x40610F8C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	R	R	R	None		R	R
HW Access	None	W	W	W	None		W	W
Name	None	UNDER-FLOW	OVER-FLOW	EMPTY	None [3:2]		NOT_FULL	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None					R	R	R
HW Access	None					W	W	W
Name	None [15:11]					UART_AR-B_LOST	UART_-DONE	UART_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10	UART_ARB_LOST	Logical and of corresponding request and mask bits. Default Value: 0
9	UART_DONE	Logical and of corresponding request and mask bits. Default Value: 0
8	UART_NACK	Logical and of corresponding request and mask bits. Default Value: 0
6	UNDERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
5	OVERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
4	EMPTY	Logical and of corresponding request and mask bits. Default Value: 0
1	NOT_FULL	Logical and of corresponding request and mask bits. Default Value: 0

25.1.37 SCB0_INTR_TX_MASKED (continued)

0	TRIGGER	Logical and of corresponding request and mask bits. Default Value: 0

25.1.38 SCB0_INTR_RX

Receiver interrupt request

Address: 0x40610FC0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW1C	RW1C	None	RW1C	RW1C	None	RW1C
HW Access	None	RW1S	RW1S	None	RW1S	RW1S	None	RW1S
Name	None	UNDER-FLOW	OVER-FLOW	None	FULL	NOT_EMP-TY	None	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW1C	RW1C	RW1C	RW1C
HW Access	None				RW1S	RW1S	RW1S	RW1S
Name	None [15:12]				BREAK_-DETECT	BAUD_DE-TECT	PARI-TY_ERROR	FRAME_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	BREAK_DETECT	Break detection is successful: the line is '0' for UART_RX_CTRL.BREAK_WIDTH + 1 bit period. Can occur at any time to address unanticipated break fields; i.e. "break-in-data" is supported. This feature is supported for the UART standard and LIN submodes. For the UART standard submodes, ongoing receipt of data frames is NOT affected; i.e. Firmware is expected to take the proper action. For the LIN submode, possible ongoing receipt of a data frame is stopped and the (partially) received data frame is dropped and baud rate detection is started. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
10	BAUD_DETECT	LIN baudrate detection is completed. The receiver software uses the UART_RX_STA-TUS.BR_COUNTER value to set the clk_scb to guarantee successful receipt of the first LIN data frame (Protected Identifier Field) after the synchronization byte. Default Value: 0

25.1.38 SCB0_INTR_RX (continued)

9	PARITY_ERROR	UART Parity error in received data frame. If UART_RX_CTL.DROP_ON_PARITY_ERROR is '1', the received frame is dropped. If UART_RX_CTL.DROP_ON_PARITY_ERROR is '0', the re-ceived frame is send to the RX FIFO. In SmartCard submode, negatively acknowledged data frames generate a parity error. Note that Firmware can only identify the erroneous data frame in the RX FIFO if it is fast enough to read the data frame before the hardware writes a next data frame into the RX FIFO. Default Value: 0
8	FRAME_ERROR	UART Frame error in received data frame. This can be either a start or stop bit(s) error: Start bit error: after the detection of the beginning of a start bit period (RX line changes from '1' to '0'), the middle of the start bit period is sampled erroneously (RX line is '1'). Note: a start bit error is detected BEFORE a data frame is received. Stop bit error: the RX line is sampled as '0', but a '1' was expected. Note: a stop bit error may result in failure to receive successive data frame(s). Note: a stop bit error is detected AFTER a data frame is received. A stop bit error is detected after a data frame is received, and the UART_RX_CTL.DROP_ON_-FRAME_ERROR field specifies whether the received frame is dropped or send to the RX FIFO. If UART_RX_CTL.DROP_ON_FRAME_ERROR is '1', the received data frame is dropped. If UART_RX_CTL.DROP_ON_FRAME_ERROR is '0', the received data frame is send to the RX FIFO. Note that Firmware can only identify the erroneous data frame in the RX FIFO if it is fast enough to read the data frame before the hardware writes a next data frame into the RX FIFO; i.e. the RX FIFO does not have error flags to tag erroneous data frames. Default Value: 0
6	UNDERFLOW	Attempt to read from an empty RX FIFO. Only used in FIFO mode. Default Value: 0
5	OVERFLOW	Attempt to write to a full RX FIFO. Note: in I2C mode, the OVERFLOW is set when a data frame is received and the RX FIFO is full, independent of whether it is ACK'd or NACK'd. Only used in FIFO mode. Default Value: 0
3	FULL	RX FIFO is full. Note that received data frames are lost when the RX FIFO is full. Dependent on CTRL.BYTE_MODET: BYTE_MODE is '0': # entries == FF_DATA_NR/2. BYTE_MODE is '1': # entries == FF_DATA_NR. Only used in FIFO mode. Default Value: 0
2	NOT_EMPTY	RX FIFO is not empty. Only used in FIFO mode. Default Value: 0
0	TRIGGER	More entries in the RX FIFO than the value specified by TRIGGER_LEVEL in SCB_RX_FI-FO_CTL. Only used in FIFO mode. Default Value: 0

25.1.39 SCB0_INTR_RX_SET

Receiver interrupt set request

Address: 0x40610FC4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW1S	RW1S	None	RW1S	RW1S	None	RW1S
HW Access	None	A	A	None	A	A	None	A
Name	None	UNDER-FLOW	OVER-FLOW	None	FULL	NOT_EMP-TY	None	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW1S	RW1S	RW1S	RW1S
HW Access	None				A	A	A	A
Name	None [15:12]				BREAK_-DETECT	BAUD_DE-TECT	PARI-TY_ERROR	FRAME_ER ROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	BREAK_DETECT	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
10	BAUD_DETECT	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
9	PARITY_ERROR	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
8	FRAME_ERROR	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
6	UNDERFLOW	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
5	OVERFLOW	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
3	FULL	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0

25.1.39 SCB0_INTR_RX_SET (continued)

2	NOT_EMPTY	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
0	TRIGGER	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

25.1.40 SCB0_INTR_RX_MASK

Receiver interrupt mask

Address: 0x40610FC8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	RW	None	RW	RW	None	RW
HW Access	None	R	R	None	R	R	None	R
Name	None	UNDER-FLOW	OVER-FLOW	None	FULL	NOT_EMP-TY	None	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [15:12]				BREAK_-DETECT	BAUD_DE-TECT	PARI-TY_ERROR	FRAME_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	BREAK_DETECT	Mask bit for corresponding bit in interrupt request register. Default Value: 0
10	BAUD_DETECT	Mask bit for corresponding bit in interrupt request register. Default Value: 0
9	PARITY_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
8	FRAME_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
6	UNDERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
5	OVERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
3	FULL	Mask bit for corresponding bit in interrupt request register. Default Value: 0

25.1.40 SCB0_INTR_RX_MASK (continued)

2	NOT_EMPTY	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	TRIGGER	Mask bit for corresponding bit in interrupt request register. Default Value: 0

25.1.41 SCB0_INTR_RX_MASKED

Receiver interrupt masked request

Address: 0x40610FCC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	R	R	None	R	R	None	R
HW Access	None	W	W	None	W	W	None	W
Name	None	UNDER-FLOW	OVER-FLOW	None	FULL	NOT_EMP-TY	None	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None				R	R	R	R
HW Access	None				W	W	W	W
Name	None [15:12]				BREAK_-DETECT	BAUD_DE-TECT	PARI-TY_ERROR	FRAME_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	BREAK_DETECT	Logical and of corresponding request and mask bits. Default Value: 0
10	BAUD_DETECT	Logical and of corresponding request and mask bits. Default Value: 0
9	PARITY_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
8	FRAME_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
6	UNDERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
5	OVERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
3	FULL	Logical and of corresponding request and mask bits. Default Value: 0

25.1.41 SCB0_INTR_RX_MASKED (continued)

2	NOT_EMPTY	Logical and of corresponding request and mask bits. Default Value: 0
0	TRIGGER	Logical and of corresponding request and mask bits. Default Value: 0

25.1.42 SCB8_CTRL

Generic control

Address: 0x40690000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				OVS [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [15:13]			CMD_RE-SP_MODE	BYTE_-MODE	EZ_MODE	EC_OP_-MODE	EC_AM_-MODE

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [23:18]						BLOCK	ADDR_AC-CEPT

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None					RW	
HW Access	R	None					R	
Name	ENABLED	None [30:26]					MODE [25:24]	

Bits	Name	Description
31	ENABLED	0': Block Disabled '1': Block Enabled The proper order in which to initialize the SCB is as follows: - Program protocol specific information using SPI_CTRL, UART_CTRL (and UART_TX_CTRL and UART_RX_CTRL) or I2C_CTRL. This includes selection of a submode, master/slave functionality and transmitter/receiver functionality when applicable. - Program generic transmitter (TX_CTRL) and receiver (RX_CTRL) information. This includes enabling of the transmitter and receiver functionality. - Program transmitter FIFO (TX_FIFO_CTRL) and receiver FIFO (RX_FIFO_CTRL) information. - Program CTRL to enable SCB, select the specific operation mode and oversampling factor. When the SCB is enabled, no control information should be changed. Changes must be made AFTER disabling the SCB, e.g. to modify the operation mode (from I2C to SPI) or to go from externally to internally clocked. The change takes effect after the SCB is re-enabled. Note that disabling the SCB will cause re-initialization of the design and associated state is lost (e.g. FIFO content). Default Value: 0
25 : 24	MODE	Mode of operation (3: Reserved) Default Value: 3

25.1.42 SCB8_CTRL (continued)

		0x0: I2C : Inter-Integrated Circuits (I2C) mode. **0x1: SPI :** Serial Peripheral Interface (SPI) mode. **0x2: UART :** Universal Asynchronous Receiver/Transmitter (UART) mode.
17	BLOCK	Only used in externally clocked mode. If the externally clocked logic and the CPU access the EZ memory at the same time this bit determines whether a CPU access should block and result in bus wait states '0': Do not block, but ingore a write and return 0xffff:ffff for a read '1': Block, resulting in CPU wait states. If BLOCK is 0 and the accesses collide, CPU read operations return 0xffff:ffff and CPU write operations are ignored. Colliding accesses are registered as interrupt causes: field BLOCKED of the INTR_TX and INTR_RX registers. Default Value: 0
16	ADDR_ACCEPT	Determines whether a received matching address is accepted in the RX FIFO:. '0': Matching address does not go in RX FIFO '1': Match address does go in RX FIFO In I2C mode, this field is used to allow the slave to put the received slave address or general call address in the RX FIFO. Note that a received matching address is put in the RX FIFO when this bit is '1' for both I2C read and write transfers. In multi-processor UART receiver mode, this field is used to allow the receiver to put the received address in the RX FIFO. Note: non-matching addresses are never put in the RX FIFO. In SPI mode this field must be '0' Default Value: 0
12	CMD_RESP_MODE	Determines CMD_RESP mode of operation: '0': CMD_RESP mode disabled. '1': CMD_RESP mode enabled (also requires EC_AM_MODE and EC_OP_MODE to be set to '1'). In CMD_RESP mode, a meta protocol is applied to the serial interface protocol. This meta protocol adds meaning to the data frames transferred by the serial interface protocol: a data frame can represent a write memory data element or a read memory data element. The difference from EZ mode is that the address is written by the CPU, not the interface master. CMD_RESP mode can only be used for synchronous serial interface protocols (SPI and I2C) in slave mode. In SPI mode, only Motorola submode (all Motorola modes: 0, 1, 2, 3) is supported. The external master should use continuous data frames; i.e. data frames not seperated by slave deselection. In CMD_RESP mode, data frames should 8-bit in size and should be transmitted and received with the Most Significant Bit (MSB) first. In UART mode this field must be '0'. Default Value: 0
11	BYTE_MODE	Determines the number of bits per FIFO data element: '0': 16-bit FIFO data elements. '1': 8-bit FIFO data elements. This mode doubles the amount of FIFO entries, but TX_CTRL.DATA_WIDTH and RX_CTRL.DATA_WIDTH are restricted to [0, 7]. Default Value: 0

25.1.42 SCB8_CTRL (continued)

10	EZ_MODE	This field determines if EZ mode is enabled or disabled for the SCB block '0': EZ Mode Disabled '1': EZ Mode Enabled In EZ mode, a meta protocol is applied to the serial interface protocol. This meta protocol adds meaning to the data frames transferred by the serial interface protocol: a data frame can represent a memory address, a write memory data element or a read memory data element. EZ mode can only be used for synchronous serial interface protocols (SPI and I2C) in slave mode. In SPI mode, only Motorola submode (all Motorola modes: 0, 1, 2, 3) is supported. The external master should use continuous data frames; i.e. data frames not seperated by slave deselection. In EZ mode, data frames should 8-bit in size and should be transmitted and received with the Most Significant Bit (MSB) first. In UART mode this field must be '0'. Default Value: 0
9	EC_OP_MODE	This field specifies the clocking for the SCB block after the address phase '0': Internally clocked mode '1': externally clocked mode In internally clocked mode, the serial interface protocols run off the clk_scb. In externally clocked mode, the serial interface protocols run off the clock as provided by the serial interface. Externally clocked operation mode is only used for synchronous serial interface protocols (SPI and I2C) in slave mode. In SPI mode, only Motorola submode (all Motorola modes: 0, 1, 2, 3) is supported. In UART mode this field must be '0'. Default Value: 0
8	EC_AM_MODE	This field specifies the clocking for the address matching (I2C slave) or slave selection detection logic (SPI slave) '0': Internally clocked mode '1': Externally clocked mode In internally clocked mode the address detection(and slave selection detection) is done by clk_scb, and thus won't be done in deep sleep power mode as clk_scb isn't active. In externally clocked mode the address detection is done by the I2C/SPI interface clock. This allows for the device to be awoken on I2C salve address match and SPI slave select assertion. The clocking for the rest of the logic is determined by CTRL.EC_OP_MODE. Externally clocked mode is only used for synchronous serial interface protocols (SPI and I2C) in slave mode. In SPI mode, only Motorola submode (all Motorola modes: 0, 1, 2, 3) is supported. In UART mode this field must be '0'. Default Value: 0

25.1.42 SCB8_CTRL (continued)

3 : 0	OVS	Serial interface bit period oversampling factor expressed in clk_scb cycles. clk_scb is the peripheral clock divider connected to the SCB. Used for SPI Master and UART functionality. This field is NOT used in externally clocked mode. This filed is NOT used for SPI slave or I2C mode. OVS + 1 clk_scb cycles constitute a single serial interface clock/bit cycle. If OVS is odd, the oversampling factor is even and the low and high phase of the interface clock period are the same. If OVS is even, the oversampling factor is odd and the low and high phase can differ by 1 SCB clock period. In SPI master mode, the valid range is [3, 15]. The frequency of the SPI Clock is (frequency of clk_scb) / (OVS + 1). For example, is clk_scb is 50 MHz and OVS is 9, then the frequency of SPI Clock is 50 MHz / (9+1) = 5 MHz. If the MISO signal is not used for SPI master the valid range changes to [1,15] In SPI slave mode, the OVS field is NOT used. Refer to the architecture TRM for information on how to configure clk_scb for SPI Slave. Generally, it is recommended that clk_scb be as fast as possible for the slave. In UART standard sub mode (including LIN and Smartcard), the valid range is [7, 15]. In UART IrDA sub mode this field indirectly specifies the oversampling. The oversampling determines the interface clock/bit cycle and the width of the pulse. For normal transmission mode, the pulse is roughly 3/16 of the bit period (for all bit rates). There is only one valid OVS value: - 0: 16 times oversampling. clk_scb frequency = 16*115.2 KHz for 115.2 Kbps. clk_scb frequency = 16*57.6 KHz for 57.6 Kbps. clk_scb frequency = 16*38.4 KHz for 38.4 Kbps. clk_scb frequency = 16*19.2 KHz for 19.2 Kbps. clk_scb frequency = 16*9.6 KHz for 9.6 Kbps. clk_scb frequency = 16*2.4 KHz for 2.4 Kbps. clk_scb frequency = 16*1.2 KHz for 1.2 Kbps. - all other values are not used in normal mode. RX_CTRL.MEDIAN must be set to '1' for IrDA receiver functionality. UART IrDA RX Low power mode, OVS field values (with the required clk_scb frequency): - 0: 16 times oversampling. clk_scb frequency = 16*115.2 KHz for 115.2 Kbps. - 1: 32 times oversampling. clk_scb frequency = 32*57.6 KHz for 57.6 Kbps. - 2: 48 times oversampling. clk_scb frequency = 48*38.4 KHz for 38.4 Kbps. - 3: 96 times oversampling. clk_scb frequency = 96*19.2 KHz for 19.2 Kbps. - 4: 192 times oversampling. clk_scb frequency = 192*9.6 KHz for 9.6 Kbps. - 5: 768 times oversampling. clk_scb frequency = 768*2.4 KHz for 2.4 Kbps. - 6: 1536 times oversampling. clk_scb frequency = 1536*1.2 KHz for 1.2 Kbps. - all other values are not used in low power mode. In low power transmission mode, this pulse is potentially smaller (down to 1.62 us typical and 1.41 us minimal) than 3/16 of the bit period (for < 115.2 Kbps bitrates). Pulse widths greater or equal than two SCB clock cycles are guaranteed to be detected by the receiver. Pulse widths less than two SCB clock cycles and greater or equal than one SCB clock cycle may be detected by the receiver. Pulse widths less than one SCB clock cycle will not be detected by the receiver. Default Value: 15

25.1.43 SCB8_STATUS

Generic status

Address: 0x40690004

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							W
Name	None [7:1]							EC_BUSY

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	EC_BUSY	Inidicates whether the externally clocked logic is potentially accessing the EZ memory (this is only possible in EZ and CMD_RESP mode). This bit can be used by SW to determine whether it is safe for the CPU to access the EZ memory (without bus wait states (a blocked CPU access) or bus errors being generated). Note that the INTR_TX.BLOCKED and INTR_RX.BLOCKED interrupt causes are used to indicate whether CPU access was actually blocked by externally clocked logic. Default Value: Undefined

25.1.44 SCB8_CMD_RESP_CTRL

Command/response control

Address: 0x40690008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	BASE_RD_ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	BASE_WR_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	BASE_WR_ADDR	I2C/SPI write base address for CMD_RESP mode. At the start of a write transfer this BASE_WR_ADDR is copied to CMD_RESP_STATUS.CURR_WR_ADDR. This field should not be modified during ongoing bus transfers. Default Value: 0
7 : 0	BASE_RD_ADDR	I2C/SPI write base address for CMD_RESP mode. At the start of a write transfer this BASE_WR_ADDR is copied to CMD_RESP_STATUS.CURR_WR_ADDR. This field should not be modified during ongoing bus transfers. Default Value: 0

25.1.45 SCB8_CMD_RESP_STATUS

Command/response status

Address: 0x4069000C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	CURR_RD_ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	CURR_WR_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	None					
HW Access	W	W	None					
Name	CMD_RE-SP_EC_BUSY	CMD_RE-SP_EC_BUS_BUSY	None [29:24]					

Bits	Name	Description
31	CMD_RESP_EC_BUSY	Indicates whether the CURR_RD_ADDR and CURR_WR_ADDR fields in this register are reliable (when CMD_RESP_EC_BUSY is '0') or not reliable (when CMD_RESP_EC_BUSY is '1'). Note: - When there is no ongoing bus transfer, CMD_RESP_EC_BUSY is '0' (reliable). - When there is a ongoing bus transfer, CMD_RESP_EC_BUSY is '0' (reliable), when the CURR_RD_ADDR and CURR_WR_ADDR are not being updated by the HW. - When there is a ongoing bus transfer, CMD_RESP_EC_BUSY is '1' (not reliable), when the CURR_RD_ADDR or CURR_WR_ADDR are being updated by the HW. Note that this update lasts one I2C clock cycle, or two SPI clock cycles. Default Value: Undefined
30	CMD_RE-SP_EC_BUS_BUSY	Indicates whether there is an ongoing bus transfer to the SCB. '0': no ongoing bus transfer. '1': ongoing bus transfer. For SPI, the field is '1' when slave mode is selected. For I2C, the field is set to '1' at a I2C START/RESTART. In case of an address match, the field is set to '0' on a I2C STOP. In case of NO address match, the field is set to '0' after the failing address match. Default Value: Undefined

25.1.45 SCB8_CMD_RESP_STATUS (continued)

23 : 16	CURR_WR_ADDR	I2C/SPI write current address for CMD_RESP mode. HW increments the field after a write access to the memory buffer. However, when the last memory buffer address is reached, the address is NOT incremented (but remains at the maximim memory buffer address). The field is used to determine how many bytes have been written (# bytes = CURR_WR_ADDR - CMD_RESP_CTRL.BASE_WR_ADDR). This field is reliable when there is no bus transfer. This field is potentially unreliable when there is a ongoing bus transfer, i.e when CMD_RESP_EC_BUSY is '0', the field is reliable. Default Value: Undefined
7 : 0	CURR_RD_ADDR	I2C/SPI read current address for CMD_RESP mode. HW increments the field after a read access to the memory buffer. However, when the last memory buffer address is reached, the address is NOT incremented (but remains at the maximim memory buffer address). The field is used to determine how many bytes have been read (# bytes = CURR_RD_ADDR - CMD_RESP_CTRL.BASE_RD_ADDR). This field is reliable when there is no bus transfer. This field is potentially unreliable when there is a ongoing bus transfer, i.e. when CMD_RESP_EC_BUSY is '0', the field is reliable. Default Value: Undefined

25.1.46 SCB8_SPI_CTRL

SPI control

Address: 0x40690020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	None
HW Access	None				R	R	R	None
Name	None [7:4]				CPOL	CPHA	SE-LECT_PRE-CEDE	None

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [15:12]				SSEL_PO-LARITY3	SSEL_PO-LARITY2	SSEL_PO-LARITY1	SSEL_PO-LARITY0

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None				RW		RW	
HW Access	None				R		R	
Name	None [31:28]				SSEL [27:26]		MODE [25:24]	

Bits	Name	Description
27 : 26	SSEL	Selects one of the four incoming/outgoing SPI slave select signals: - 0: Slave 0, SSEL[0]. - 1: Slave 1, SSEL[1]. - 2: Slave 2, SSEL[2]. - 3: Slave 3, SSEL[3]. The SCB should be disabled when changes are made to this field. Default Value: 0
25 : 24	MODE	Submode of SPI operation (3: Reserved). Default Value: 3 **0x0: SPI_MOTOROLA :** SPI Motorola submode.

25.1.46 SCB8_SPI_CTRL (continued)

		0x1: SPI_TI : SPI Texas Instruments submode. **0x2: SPI_NS :** SPI National Semiconducturs submode.
11	SSEL_POLARITY3	Slave select polarity. Default Value: 0
10	SSEL_POLARITY2	Slave select polarity. Default Value: 0
9	SSEL_POLARITY1	Slave select polarity. Default Value: 0
8	SSEL_POLARITY0	Slave select polarity. SSEL_POLARITY0 applies to the outgoing SPI slave select signal 0 (master mode) and to the incoming SPI slave select signal (slave mode). For Motorola and National Semiconductors submodes: '0': slave select is low/'0' active. '1': slave select is high/'1' active. For Texas Instruments submode: '0': high/'1' active precede/coincide pulse. '1': low/'0' active precede/coincide pulse. Default Value: 0
3	CPOL	Indicates the clock polarity. This field, together with the CPHA field, indicates when MOSI data is driven and MISO data is captured: - CPOL is 0: SCLK is 0 when not transmitting data. - CPOL is 1: SCLK is 1 when not transmitting data. Default Value: 0
2	CPHA	Indicates the clock phase. This field, together with the CPOL field, indicates when MOSI data is driven and MISO data is captured: - Motorola mode 0. CPOL is 0, CPHA is 0: MOSI is driven on a falling edge of SCLK. MISO is captured on a rising edge of SCLK. - Motorola mode 1. CPOL is 0, CPHA is 1: MOSI is driven on a rising edge of SCLK. MISO is captured on a falling edge of SCLK. - Motorola mode 2. CPOL is 1, CPHA is 0: MOSI is driven on a rising edge of SCLK. MISO is captured on a falling edge of SCLK. - Motorola mode 3. CPOL is 1, CPHA is 1: MOSI is driven on a falling edge of SCLK. MISO is captured on a rising edge of SCLK. In SPI Motorola submode, all four CPOL/CPHA modes are valid. in SPI NS submode, only CPOL=0 CPHA=0 mode is valid. in SPI TI submode, only CPOL=0 CPHA=1 mode is valid. Default Value: 0
1	SELECT_PRECEDE	Only used in SPI Texas Instruments' submode. When '1', the data frame start indication is a pulse on the Slave SELECT line that precedes the transfer of the first data frame bit. When '0', the data frame start indication is a pulse on the Slave SELECT line that coincides with the transfer of the first data frame bit. Default Value: 0

25.1.47 SCB8_SPI_STATUS

SPI status

Address: 0x40690024

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						W	W
Name	None [7:2]						SPI_EC_BUSY	BUS_BUSY

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	CURR_EZ_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	BASE_EZ_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	BASE_EZ_ADDR	SPI base EZ address. Address as provided by a SPI write transfer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable. Default Value: Undefined
15 : 8	CURR_EZ_ADDR	SPI current EZ address. Current address pointer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable (during an ongoing transfer when SPI_EC_BUSY is '1'). Default Value: Undefined
1	SPI_EC_BUSY	Inidicates whether the externally clocked logic is potentially accessing the EZ memory and/or updating BASE_ADDR or CURR_ADDR (this is only possible in EZ and CMD_RESP mode). This bit can be used by the CPU to determine whether BASE_ADDR and CURR_ADDR are reliable. Default Value: Undefined
0	BUS_BUSY	SPI bus is busy. The bus is considered busy ('1') during an ongoing transaction. For Motorola and National submodes, the busy bit is '1', when the slave selection is activated. For TI submode, the busy bit is '1' from the time the preceding/coinciding slave select is activated for the first transmitted data frame, till the last MOSI/MISO bit of the last data frame is transmitted. Default Value: Undefined

25.1.48 SCB8_I2C_CTRL

I2C control

Address: 0x40690060

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	None		
HW Access	R	R	R	R	R	None		
Name	S_NOT_READY_-DATA_NACK	S_NOT_READY_ADDR_NACK	S_READY_DATA_ACK	S_READY_ADDR_ACK	S_GENER-AL_IGNORE	None		

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None	RW	None					
HW Access	None	R	None					
Name	None	SLAVE_-MODE	None [29:24]					

Bits	Name	Description
30	SLAVE_MODE	Slave mode enabled ('1') or not ('0'). Default Value: 0
15	S_NOT_READY_-DATA_NACK	Only used for FIFO mode, NOT EZ or CMD_RESP mode. Functionality is as follows: - 1: a received data element byte the slave is immediately NACK'd when the receiver FIFO is full. - 0: clock stretching is performed (till the receiver FIFO is no longer full). Default Value: 1

25.1.48 SCB8_I2C_CTRL (continued)

14	S_NOT_READY_ADDR_NACK	Only used for FIFO mode, NOT EZ or CMD_RESP mode. Functionality is as follows: - 1: In Active/Sleep mode a received (matching) slave address is immediately NACK'd when the RX FIFO is full In DeepSleep power mode when EC_AM = '1' and EC_OP = '0' clk_scb is not avaliable, so the incoming address will be NACK'd until the clock is avaliable. Once clk_scb is avaliable the address ACK will follow S_READY_ADDR_ACK - 0: in Active/Sleep mode clock stretching is performed when the RX FIFO is full, the strech is released when the RX FIFO is no longer full. In DeepSleep power mode when EC_AM = '1' and EC_OP = '0' clk_scb is not avaliable, so the clocked will be streched on an incoming address until clk_scb is avaliable. After clk_scb is avalaible the address ACK will follow S_READY_ADDR_ACK Default Value: 1
13	S_READY_DATA_ACK	When '1', a received data element by the slave is immediately ACK'd when the RX FIFO is not full. In EZ and CMD_RESP mode, this field should be set to '1'. When '0' the data must be ACK/NACK'd by the CPU using I2C_S_CMD.S_ACK or I2C_S_CMD.S_NACK Default Value: 1
12	S_READY_ADDR_ACK	When '1', a received (matching) slave address is immediately ACK'd when the RX FIFO is not full. In EZ and CMD_RESP mode, this field should be set to '1'. When '0' the address must be ACK/NACK'd by the CPU using I2C_S_CMD.S_ACK or I2C_S_CMD.S_NACK Default Value: 1
11	S_GENERAL_IGNORE	When '1', a received general call slave address is immediately NACK'd (no ACK or clock stretching) and treated as a non matching slave address. This is useful for slaves that do not need any data supplied within the general call structure. When '0' the general call address is accepted and follows S_READY_ADDR_ACK and S_NOT_READY_ADDR_NACK Default Value: 1

25.1.49 SCB8_I2C_STATUS

I2C status

Address: 0x40690064

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			R	None		R	R
HW Access	None			W	None		W	W
Name	None [7:5]			S_READ	None [3:2]		I2C_EC_BUSY	BUS_BUSY

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	CURR_EZ_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	BASE_EZ_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	BASE_EZ_ADDR	I2C slave base EZ address. Address as provided by an I2C write transfer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable. Default Value: Undefined
15 : 8	CURR_EZ_ADDR	I2C slave current EZ address. Current address pointer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable (during an ongoing transfer when I2C_EC_BUSY is '1'). Default Value: Undefined
4	S_READ	I2C slave read transfer ('1') or I2C slave write transfer ('0'). When the I2C slave is inactive/idle or receiving START, REPEATED START, STOP or an address, this field is '0''. Default Value: 0
1	I2C_EC_BUSY	Inidicates whether the externally clocked logic is potentially accessing the EZ memory and/or updating BASE_ADDR or CURR_ADDR (this is only possible in EZ and CMD_RESP mode). This bit can be used by the CPU to determine whether BASE_ADDR and CURR_ADDR are reliable. Default Value: Undefined

0	BUS_BUSY	I2C bus is busy. The bus is considered busy ('1'), from the time a START is detected or from the time the SCL line is '0'. The bus is considered idle ('0'), from the time a STOP is detected. If the SCB is disabled, BUS_BUSY is '0'. After enabling the SCB, it takes time for the BUS_BUSY to detect a busy bus. This time is the maximum high time of the SCL line. For a 100 kHz interface frequency, this maximum high time may last roughly 5 us (half a bit period). For single master systems, BUS_BUSY does not have to be used to detect an idle bus before a master starts a transfer using I2C_M_CMD.M_START (no bus collisions). For multi-master systems, BUS_BUSY can be used to detect an idle bus before a master starts a transfer using I2C_M_CMD.M_START_ON_IDLE (to prevent bus collisions). Default Value: 0

25.1.50 SCB8_INTR_CAUSE

Active clocked interrupt signal

Address: 0x40690E00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R	R	R	R	R	R
HW Access	None		W	W	W	W	W	W
Name	None [7:6]		SPI_EC	I2C_EC	RX	TX	S	M

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	SPI_EC	Externally clocked SPI interrupt active ("interrupt_spi_ec"): INTR_SPI_EC_MASKED != 0. Default Value: 0
4	I2C_EC	Externally clock I2C interrupt active ("interrupt_i2c_ec"): INTR_I2C_EC_MASKED != 0. Default Value: 0
3	RX	Receiver interrupt active ("interrupt_rx"): INTR_RX_MASKED != 0. Default Value: 0
2	TX	Transmitter interrupt active ("interrupt_tx"): INTR_TX_MASKED != 0. Default Value: 0
1	S	Slave interrupt active ("interrupt_slave"): INTR_S_MASKED != 0. Default Value: 0
0	M	Master interrupt active ("interrupt_master"): INTR_M_MASKED != 0. Default Value: 0

25.1.51 SCB8_INTR_I2C_EC

Externally clocked I2C interrupt request

Address: 0x40690E80

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1C	RW1C	RW1C	RW1C
HW Access	None				A	A	A	A
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	STOP detection after a read transfer occurred. Activated on the end of a read transfer (I2C STOP). This event is an indication that a buffer memory location has been read from. Only set for a slave request with an address match, in EZ and CMD_RESP modes, when EC_OP is '1'. Default Value: 0
2	EZ_WRITE_STOP	STOP detection after a write transfer occurred. Activated on the end of a write transfer (I2C STOP). This event is an indication that a buffer memory location has been written to. For EZ mode: a transfer that only writes the base address does NOT activate this event. Only set for a slave request with an address match, in EZ and CMD_RESP modes, when EC_OP is '1'. Default Value: 0
1	EZ_STOP	STOP detection. Activated on the end of a every transfer (I2C STOP). Only set for a slave request with an address match, in EZ and CMD_RESP modes, when EC_OP is '1'. Default Value: 0
0	WAKE_UP	Wake up request. Active on incoming slave request (with address match). Only set when EC_AM is '1'. Default Value: 0

25.1.52 SCB8_INTR_I2C_EC_MASK

Externally clocked I2C interrupt mask

Address: 0x40690E88

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	EZ_WRITE_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	EZ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	WAKE_UP	Mask bit for corresponding bit in interrupt request register. Default Value: 0

25.1.53 SCB8_INTR_I2C_EC_MASKED

Externally clocked I2C interrupt masked

Address: 0x40690E8C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R	R	R	R
HW Access	None				W	W	W	W
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
2	EZ_WRITE_STOP	Logical and of corresponding request and mask bits. Default Value: 0
1	EZ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
0	WAKE_UP	Logical and of corresponding request and mask bits. Default Value: 0

25.1.54 SCB8_INTR_SPI_EC

Externally clocked SPI interrupt request

Address: 0x40690EC0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1C	RW1C	RW1C	RW1C
HW Access	None				A	A	A	A
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	STOP detection after a read transfer occurred. Activated on the end of a read transfer (SPI deselection). This event is an indication that a buffer memory location has been read from. Only set in EZ and CMD_RESP modes and when EC_OP is '1'. Default Value: 0
2	EZ_WRITE_STOP	STOP detection after a write transfer occurred. Activated on the end of a write transfer (SPI deselection). This event is an indication that a buffer memory location has been written to. For EZ mode: a transfer that only writes the base address does NOT activate this event. Only set in EZ and CMD_RESP modes and when EC_OP is '1'. Default Value: 0
1	EZ_STOP	STOP detection. Activated on the end of a every transfer (SPI deselection). Only set in EZ and CMD_RESP mode and when EC_OP is '1'. Default Value: 0
0	WAKE_UP	Wake up request. Active on incoming slave request. Only set when EC_AM is '1'. Default Value: 0

25.1.55 SCB8_INTR_SPI_EC_MASK

Externally clocked SPI interrupt mask

Address: 0x40690EC8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	EZ_WRITE_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	EZ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	WAKE_UP	Mask bit for corresponding bit in interrupt request register. Default Value: 0

25.1.56 SCB8_INTR_SPI_EC_MASKED

Externally clocked SPI interrupt masked

Address: 0x40690ECC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R	R	R	R
HW Access	None				W	W	W	W
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
2	EZ_WRITE_STOP	Logical and of corresponding request and mask bits. Default Value: 0
1	EZ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
0	WAKE_UP	Logical and of corresponding request and mask bits. Default Value: 0

25.1.57 SCB8_INTR_TX

Transmitter interrupt request

Address: 0x40690F80

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	None		RW1C	RW1C
HW Access	RW1S	RW1S	RW1S	RW1S	None		RW1S	RW1S
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	EMPTY	None [3:2]		NOT_FULL	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	BLOCKED	CPU write can not get access to the EZ memory (EZ data access), due to an externally clocked EZ access. Default Value: 0
6	UNDERFLOW	Attempt to read from an empty TX FIFO. This happens when the SCB is ready to transfer data and EMPTY is '1'. Only used in FIFO mode. Default Value: 0
5	OVERFLOW	Attempt to write to a full TX FIFO. Only used in FIFO mode. Default Value: 0
4	EMPTY	TX FIFO is empty; i.e. it has 0 entries. Only used in FIFO mode. Default Value: 0

1	NOT_FULL	TX FIFO is not full. Dependent on CTRL.BYTE_MODE: BYTE_MODE is '0': # entries != FF_DATA_NR/2. BYTE_MODE is '1': # entries != FF_DATA_NR. Only used in FIFO mode. Default Value: 0
0	TRIGGER	Less entries in the TX FIFO than the value specified by TX_FIFO_CTRL. Only used in FIFO mode. Default Value: 0

25.1.58 SCB8_INTR_TX_SET

Transmitter interrupt set request

Address: 0x40690F84

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	RW1S	None		RW1S	RW1S
HW Access	A	A	A	A	None		A	A
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	EMPTY	None [3:2]		NOT_FULL	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	BLOCKED	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
6	UNDERFLOW	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
5	OVERFLOW	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
4	EMPTY	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
1	NOT_FULL	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	TRIGGER	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

25.1.59 SCB8_INTR_TX_MASK

Transmitter interrupt mask

Address: 0x40690F88

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	None		RW	RW
HW Access	R	R	R	R	None		R	R
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	EMPTY	None [3:2]		NOT_FULL	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	BLOCKED	Mask bit for corresponding bit in interrupt request register. Default Value: 0
6	UNDERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
5	OVERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
4	EMPTY	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	NOT_FULL	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	TRIGGER	Mask bit for corresponding bit in interrupt request register. Default Value: 0

25.1.60 SCB8_INTR_TX_MASKED

Transmitter interrupt masked request

Address: 0x40690F8C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	None		R	R
HW Access	W	W	W	W	None		W	W
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	EMPTY	None [3:2]		NOT_FULL	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	BLOCKED	Logical and of corresponding request and mask bits. Default Value: 0
6	UNDERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
5	OVERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
4	EMPTY	Logical and of corresponding request and mask bits. Default Value: 0
1	NOT_FULL	Logical and of corresponding request and mask bits. Default Value: 0
0	TRIGGER	Logical and of corresponding request and mask bits. Default Value: 0

25.1.61 SCB8_INTR_RX

Receiver interrupt request

Address: 0x40690FC0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	None	RW1C	RW1C	None	RW1C
HW Access	RW1S	RW1S	RW1S	None	RW1S	RW1S	None	RW1S
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	None	FULL	NOT_EMP-TY	None	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	BLOCKED	CPU read transfer can not get access to the EZ memory (EZ_DATA accesses), due to an externally clocked EZ access. Default Value: 0
6	UNDERFLOW	Attempt to read from an empty RX FIFO. Only used in FIFO mode. Default Value: 0
5	OVERFLOW	Attempt to write to a full RX FIFO. Note: in I2C mode, the OVERFLOW is set when a data frame is received and the RX FIFO is full, independent of whether it is ACK'd or NACK'd. Only used in FIFO mode. Default Value: 0
3	FULL	RX FIFO is full. Note that received data frames are lost when the RX FIFO is full. Dependent on CTRL.BYTE_MODET: BYTE_MODE is '0': # entries == FF_DATA_NR/2. BYTE_MODE is '1': # entries == FF_DATA_NR. Only used in FIFO mode. Default Value: 0

2	NOT_EMPTY	RX FIFO is not empty. Only used in FIFO mode. Default Value: 0
0	TRIGGER	More entries in the RX FIFO than the value specified by TRIGGER_LEVEL in SCB_RX_FI-FO_CTL. Only used in FIFO mode. Default Value: 0

25.1.62 SCB8_INTR_RX_SET

Receiver interrupt set request

Address: 0x40690FC4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	None	RW1S	RW1S	None	RW1S
HW Access	A	A	A	None	A	A	None	A
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	None	FULL	NOT_EMP-TY	None	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	BLOCKED	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
6	UNDERFLOW	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
5	OVERFLOW	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
3	FULL	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
2	NOT_EMPTY	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
0	TRIGGER	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

25.1.63 SCB8_INTR_RX_MASK

Receiver interrupt mask

Address: 0x40690FC8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	None	RW	RW	None	RW
HW Access	R	R	R	None	R	R	None	R
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	None	FULL	NOT_EMP-TY	None	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	BLOCKED	Mask bit for corresponding bit in interrupt request register. Default Value: 0
6	UNDERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
5	OVERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
3	FULL	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	NOT_EMPTY	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	TRIGGER	Mask bit for corresponding bit in interrupt request register. Default Value: 0

25.1.64 SCB8_INTR_RX_MASKED

Receiver interrupt masked request

Address: 0x40690FCC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	None	R	R	None	R
HW Access	W	W	W	None	W	W	None	W
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	None	FULL	NOT_EMP-TY	None	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	BLOCKED	Logical and of corresponding request and mask bits. Default Value: 0
6	UNDERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
5	OVERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
3	FULL	Logical and of corresponding request and mask bits. Default Value: 0
2	NOT_EMPTY	Logical and of corresponding request and mask bits. Default Value: 0
0	TRIGGER	Logical and of corresponding request and mask bits. Default Value: 0

Section H: Peripheral Group 9

This section encompasses the following chapters:

26 Analog Reference Block (AREF) Registers

This section discusses the Analog Reference Block (AREF) registers. It lists all the registers in mapping tables, in address order.

26.1 Register Details

Register	Address	Description
PASS_AREF_AREF_CTRL	0x411F0E00	Global AREF control

26.1.1 PASS_AREF_AREF_CTRL

Global AREF control

Address: 0x411F0E00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW			RW		None	RW
HW Access	R	R			R		None	R
Name	CTB_IP-TAT_S-CALE	AREF_RMB [6:4]			AREF_BIAS_SCALE [3:2]		None	AREF_-MODE

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CTB_IPTAT_REDIRECT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW		RW	None		RW
HW Access	None		R		R	None		R
Name	None [23:22]		VREF_SEL [21:20]		CLOCK_PUMP_PERI_-SEL	None [18:17]		IZTAT_SEL

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW		None			
HW Access	R	R	R		None			
Name	ENABLED	DEEPS-LEEP_ON	DEEPSLEEP_MODE [29:28]		None [27:24]			

Bits	Name	Description
31	ENABLED	Disable AREF Default Value: 0
30	DEEPSLEEP_ON	- 0: AREF IP disabled/off during DeepSleep power mode - 1: AREF IP remains enabled during DeepSleep power mode (if ENABLED=1) Default Value: 0
29 : 28	DEEPSLEEP_MODE	AREF DeepSleep Operation Modes (only applies if DEEPSLEEP_ON = 1) Default Value: 0 **0x0: OFF :** All blocks "OFF" in DeepSleep **0x1: IPTAT :** IPTAT bias generator "ON" in DeepSleep (used for fast AREF wakeup only: IPTAT outputs not available)

26.1.1 PASS_AREF_AREF_CTRL (continued)

		0x2: IPTAT_IZTAT : IPTAT bias generator and outputs "ON" in DeepSleep (used for biasing the CTBm with a PTAT current only in deep sleep) *Note that this mode also requires that the CTB_IPTAT_REDIRECT be set if the CTBm opamp is to operate in DeepSleep **0x3: IPTAT_IZTAT_VREF :** IPTAT, VREF, and IZTAT generators "ON" in DeepSleep. This mode provides identical AREF functionality in DeepSleep as in the Active mode.
21 : 20	VREF_SEL	bandgap voltage select control Default Value: 0 **0x0: SRSS :** Use 0.8V Vref from SRSS **0x1: LOCAL :** Use locally generated Vref **0x2: EXTERNAL :** Use externally supplied Vref (aref_ext_vref)
19	CLOCK_PUMP_PERI_-SEL	CTBm charge pump clock source select. This field has nothing to do with the AREF. 0: Use the dedicated pump clock from SRSS (default) 1: Use one of the CLK_PERI dividers Default Value: 0
16	IZTAT_SEL	iztat current select control Default Value: 0 **0x0: SRSS :** Use 250nA IZTAT from SRSS **0x1: LOCAL :** Use locally generated 250nA
15 : 8	CTB_IPTAT_REDIRECT	Re-direct the CTB IPTAT output current. This can be used to reduce amplifier bias glitches during power mode transitions (for PSoC4A/B DSAB backwards compatibility). 0: Opamp.IPTAT = AREF.IPTAT and Opamp.IZTAT= AREF.IZTAT 1: Opamp.IPTAT = HiZ and Opamp.IZTAT= AREF.IPTAT *Note that in Deep Sleep, the AREF IZTAT and/or IPTAT currents can be disabled and therefore the corresponding Opamp.IZTAT/IPTAT will be HiZ. Default Value: 0
7	CTB_IPTAT_SCALE	CTB IPTAT current scaler. This bit must be set in order to operate the CTB amplifiers in the lowest power mode. This bit is chip-wide (controls all CTB amplifiers). 0: 1uA 1: 100nA Default Value: 0
6 : 4	AREF_RMB	AREF control signals (RMB). Bit 0: Manual VBG startup circuit enable 0: normal VBG startup circuit operation 1: VBG startup circuit is forced "always on" Bit 1: Manual disable of IPTAT2 DAC 0: normal IPTAT2 DAC operation 1: PTAT2 DAC is disabled while VBG startup is active Bit 2: Manual enable of VBG offset correction DAC 0: normal VBG offset correction DAC operation 1: VBG offset correction DAC is enabled while VBG startup is active Default Value: 0

26.1.1 PASS_AREF_AREF_CTRL (continued)

3 : 2	AREF_BIAS_SCALE	BIAS Current Control for all AREF Amplifiers. (These are risk mitigation bits that should not be touched by the customer: the impact on IDDA/noise/startup still needs to be characterized) 0: 125nA (reduced bias: reduction in total AREF IDDA, higher noise and longer startup times) 1: 250nA ("default" setting to meet bandgap performance (noise/startup) and IDDA specifications) 2: 375nA (increased bias: increase in total AREF IDDA, lower noise and shorter startup times) 3: 500nA (further increased bias: increase in total AREF IDDA, lower noise and shorter startup times) Default Value: 0
0	AREF_MODE	Control bit to trade off AREF settling and noise performance Default Value: 0 **0x0: NORMAL :** Nominal noise normal startup mode (meets normal mode settling and noise specifications) **0x1: FAST_START :** High noise fast startup mode (meets fast mode settling and noise specifications)

27 Continuous-Time Block Mini Registers

This section discusses the Continuous-Time Block Mini (CTBm) registers. It lists all the registers in mapping tables, in address order.

27.1 Register Details

Register	Address	Description
CTBM0_CTB_CTRL	0x41100000	global CTB and power control
CTBM0_OA_RES0_CTRL	0x41100004	Opamp0 and resistor0 control
CTBM0_OA_RES1_CTRL	0x41100008	Opamp1 and resistor1 control
CTBM0_COMP_STAT	0x4110000C	Comparator status
CTBM0_INTR	0x41100020	Interrupt request register
CTBM0_INTR_SET	0x41100024	Interrupt request set register
CTBM0_INTR_MASK	0x41100028	Interrupt request mask
CTBM0_INTR_MASKED	0x4110002C	Interrupt request masked
CTBM0_OA0_SW	0x41100080	Opamp0 switch control
CTBM0_OA0_SW_CLEAR	0x41100084	Opamp0 switch control clear
CTBM0_OA1_SW	0x41100088	Opamp1 switch control
CTBM0_OA1_SW_CLEAR	0x4110008C	Opamp1 switch control clear
CTBM0_CTD_SW	0x411000A0	CTDAC connection switch control
CTBM0_CTD_SW_CLEAR	0x411000A4	CTDAC connection switch control clear
CTBM0_CTB_SW_DS_CTRL	0x411000C0	CTB bus switch control
CTBM0_CTB_SW_SQ_CTRL	0x411000C4	CTB bus switch Sar Sequencer control
CTBM0_CTB_SW_STATUS	0x411000C8	CTB bus switch control status
CTBM0_OA0_OFFSET_TRIM	0x41100F00	Opamp0 trim control
CTBM0_OA0_SLOPE_OFFSET_TRIM	0x41100F04	Opamp0 trim control
CTBM0_OA0_COMP_TRIM	0x41100F08	Opamp0 trim control
CTBM0_OA1_OFFSET_TRIM	0x41100F0C	Opamp1 trim control
CTBM0_OA1_SLOPE_OFFSET_TRIM	0x41100F10	Opamp1 trim control
CTBM0_OA1_COMP_TRIM	0x41100F14	Opamp1 trim control
PASS_INTR_CAUSE	0x411F0000	Interrupt cause register

27.1.1 CTBM0_CTB_CTRL

global CTB and power control

Address: 0x41100000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None					
HW Access	R	R	None					
Name	ENABLED	DEEPS-LEEP_ON	None					

Bits	Name	Description
31	ENABLED	- 0: CTB IP disabled (put analog in power down, open all switches) - 1: CTB IP enabled Default Value: 0
30	DEEPSLEEP_ON	- 0: CTB IP disabled off during DeepSleep power mode - 1: CTB IP remains enabled during DeepSleep power mode (if ENABLED=1) Default Value: 0

27.1.2 CTBM0_OA_RES0_CTRL

Opamp0 and resistor0 control

Address: 0x41100004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW		
HW Access	R	R	R	R	R	R		
Name	OA0_DSI_LEVEL	OA0_BY-PASS_DSI_SYNC	OA0_HYST_EN	OA0_COM-P_EN	OA0_DRIVE_STR_-SEL	OA0_PWR_MODE [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	RW	None	RW	
HW Access	None			R	R	None	R	
Name	None [15:13]			OA0_-BOOST_EN	OA0_PUMP_EN	None	OA0_COMPINT [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
12	OA0_BOOST_EN	Reserved. Keep this bit at the default value. Default Value: 0
11	OA0_PUMP_EN	Opamp0 pump enable Default Value: 0
9 : 8	OA0_COMPINT	Opamp0 comparator edge detect for interrupt and pulse mode of DSI (trigger) Default Value: 0 **0x0: DISABLE :** Disabled, no interrupts will be detected **0x1: RISING :** Rising edge **0x2: FALLING :** Falling edge **0x3: BOTH :** Both rising and falling edges

27.1.2 CTBM0_OA_RES0_CTRL (continued)

7	OA0_DSI_LEVEL	Opamp0 comparator DSI (trigger) out level : 0=pulse, each time an edge is detected (see OA0_COMPINT) a pulse is sent out on DSI 1=level, DSI output is a synchronized version of the comparator output Default Value: 0
6	OA0_BY-PASS_DSI_SYNC	Opamp0 bypass comparator output synchronization for DSI (trigger) output: 0=synchronize (level or pulse), 1=bypass (output async) Default Value: 0
5	OA0_HYST_EN	Opamp0 hysteresis enable (10mV) Default Value: 0
4	OA0_COMP_EN	Opamp0 comparator enable Default Value: 0
3	OA0_DRIVE_STR_SEL	Opamp0 output strength select 0=1x, 1=10x This setting sets specific requirements for OA0_BOOST_EN and OA0_COMP_TRIM Default Value: 0
2 : 0	OA0_PWR_MODE	Opamp0 power level, assumes Cload=15pF for the (internal only) 1x driver or 50pF for the (external) 10x driver Default Value: 0 **0x0: OFF :** Off **0x1: LOW :** Low power mode (IDD: 350uA, GBW: 1MHz for both 1x/10x) **0x2: MEDIUM :** Medium power mode (IDD: 600uA, GBW: 3MHz for 1x & 2.5MHz for 10x) **0x3: HIGH :** High power mode for highest GBW (IDD: 1500uA, GBW: 8MHz for 1x & 6MHz for 10x) **0x4: RESERVED :** Reserved **0x5: PS_LOW :** Power Saver Low power mode (IDD: ~20uA with 1uA bias from AREF, GBW: ~100kHz for 1x/10x, offset correcting IDAC is disabled) **0x6: PS_MEDIUM :** Power Saver Medium power mode (IDD: ~40uA with 1uA bias from AREF, GBW: ~100kHz for 1x/10x, offset correcting IDAC is enabled) **0x7: PS_HIGH :** Power Saver Medium power mode (IDD: ~60uA with 1uA bias from AREF, GBW: ~200kHz for 1x/10x, offset correcting IDAC is enabled)

27.1.3 CTBM0_OA_RES1_CTRL (continued)

27.1.3 CTBM0_OA_RES1_CTRL

Opamp1 and resistor1 control

Address: 0x41100008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW		
HW Access	R	R	R	R	R	R		
Name	OA1_DSI_LEVEL	OA1_BY-PASS_DSI_SYNC	OA1_HYST_EN	OA1_COM-P_EN	OA1_DRIVE_STR_-SEL	OA1_PWR_MODE [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	RW	None	RW	
HW Access	None			R	R	None	R	
Name	None [15:13]			OA1_-BOOST_EN	OA1_PUMP_EN	None	OA1_COMPINT [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
12	OA1_BOOST_EN	Reserved. Keep this bit at the default value. Default Value: 0
11	OA1_PUMP_EN	Opamp1 pump enable Default Value: 0
9 : 8	OA1_COMPINT	Opamp1 comparator edge detect for interrupt and pulse mode of DSI (trigger) Default Value: 0 **0x0: DISABLE :** Disabled, no interrupts will be detected **0x1: RISING :** Rising edge **0x2: FALLING :** Falling edge

		0x3: BOTH : Both rising and falling edges
7	OA1_DSI_LEVEL	Opamp1 comparator DSI (trigger) out level : 0=pulse, each time an edge is detected (see OA1_COMPINT) a pulse is sent out on DSI 1=level, DSI output is a synchronized version of the comparator output Default Value: 0
6	OA1_BY-PASS_DSI_SYNC	Opamp1 bypass comparator output synchronization for DSI output: 0=synchronize, 1=bypass Default Value: 0
5	OA1_HYST_EN	Opamp1 hysteresis enable (10mV) Default Value: 0
4	OA1_COMP_EN	Opamp1 comparator enable Default Value: 0
3	OA1_DRIVE_STR_SEL	Opamp1 output strength select 0=1x, 1=10x This setting sets specific requirements for OA1_BOOST_EN and OA1_COMP_TRIM Default Value: 0
2 : 0	OA1_PWR_MODE	Opamp1 power level: see description of OA0_PWR_MODE Default Value: 0

27.1.4 CTBM0_COMP_STAT

Comparator status

Address: 0x4110000C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							W
Name	None [7:1]							OA0_-COMP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							R
HW Access	None							W
Name	None [23:17]							OA1_-COMP

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
16	OA1_COMP	Opamp1 current comparator status Default Value: 0
0	OA0_COMP	Opamp0 current comparator status Default Value: 0

27.1.5 CTBM0_INTR

Interrupt request register

Address: 0x41100020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1C	RW1C
HW Access	None						RW1S	RW1S
Name	None [7:2]						COMP1	COMP0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	COMP1	Comparator 1 Interrupt: hardware sets this interrupt when comparator 1 triggers. Write with '1' to clear bit. Default Value: 0
0	COMP0	Comparator 0 Interrupt: hardware sets this interrupt when comparator 0 triggers. Write with '1' to clear bit. Default Value: 0

27.1.6 CTBM0_INTR_SET

Interrupt request set register

Address: 0x41100024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1S	RW1S
HW Access	None						A	A
Name	None [7:2]						COMP1_SET	COMP0_SET

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	COMP1_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	COMP0_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

27.1.7 CTBM0_INTR_MASK

Interrupt request mask

Address: 0x41100028

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						COMP1_MASK	COMP0_MASK

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	COMP1_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	COMP0_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0

27.1.8 CTBM0_INTR_MASKED

Interrupt request masked

Address: 0x4110002C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						W	W
Name	None [7:2]						COMP1_MASKED	COMP0_MASKED

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	COMP1_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
0	COMP0_MASKED	Logical and of corresponding request and mask bits. Default Value: 0

27.1.9 CTBM0_OA0_SW

Opamp0 switch control

Address: 0x41100080

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1S	RW1S	None	RW1S
HW Access	None				RW1C	RW1C	None	RW1C
Name	None [7:4]				OA0P_A30	OA0P_A20	None	OA0P_A00

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW1S	None					RW1S
HW Access	None	RW1C	None					RW1C
Name	None	OA0M_A81	None [13:9]					OA0M_A11

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW1S	None		RW1S	None	
HW Access	None		RW1C	None		RW1C	None	
Name	None [23:22]		OA0O_D81	None [20:19]		OA0O_D51	None [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
21	OA0O_D81	Opamp0 output switch to short 1x with 10x drive Default Value: 0
18	OA0O_D51	Opamp0 output sarbus0 (ctbbus2 in CTB) Default Value: 0
14	OA0M_A81	Opamp0 negative terminal Opamp0 output Default Value: 0
8	OA0M_A11	Opamp0 negative terminal P1 Default Value: 0
3	OA0P_A30	Opamp0 positive terminal ctbbus0 Default Value: 0
2	OA0P_A20	Opamp0 positive terminal P0 Default Value: 0
0	OA0P_A00	Opamp0 positive terminal amuxbusa Default Value: 0

27.1.10 CTBM0_OA0_SW_CLEAR

Opamp0 switch control clear

Address: 0x41100084

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1C	RW1C	None	RW1C
HW Access	None				A	A	None	A
Name	None [7:4]				OA0P_A30	OA0P_A20	None	OA0P_A00

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW1C	None					RW1C
HW Access	None	A	None					A
Name	None	OA0M_A81	None [13:9]					OA0M_A11

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW1C	None		RW1C	None	
HW Access	None		A	None		A	None	
Name	None [23:22]		OA0O_D81	None [20:19]		OA0O_D51	None [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
21	OA0O_D81	see corresponding bit in OA0_SW Default Value: 0
18	OA0O_D51	see corresponding bit in OA0_SW Default Value: 0
14	OA0M_A81	see corresponding bit in OA0_SW Default Value: 0
8	OA0M_A11	see corresponding bit in OA0_SW Default Value: 0
3	OA0P_A30	see corresponding bit in OA0_SW Default Value: 0
2	OA0P_A20	see corresponding bit in OA0_SW Default Value: 0
0	OA0P_A00	see corresponding bit in OA0_SW Default Value: 0

27.1.11 CTBM0_OA1_SW

Opamp1 switch control

Address: 0x41100088

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	None		RW1S	None		RW1S	RW1S
HW Access	RW1C	None		RW1C	None		RW1C	RW1C
Name	OA1P_A73	None [6:5]		OA1P_A43	None [3:2]		OA1P_A13	OA1P_A03

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW1S	None					RW1S
HW Access	None	RW1C	None					RW1C
Name	None	OA1M_A82	None [13:9]					OA1M_A22

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW1S	None	RW1S	RW1S	None	
HW Access	None		RW1C	None	RW1C	RW1C	None	
Name	None [23:22]		OA1O_D82	None	OA1O_D62	OA1O_D52	None [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
21	OA1O_D82	Opamp1 output switch to short 1x with 10x drive Default Value: 0
19	OA1O_D62	Opamp1 output sarbus1 (ctbbus3 in CTB) Default Value: 0
18	OA1O_D52	Opamp1 output sarbus0 (ctbbus2 in CTB) Default Value: 0
14	OA1M_A82	Opamp1 negative terminal Opamp1 output Default Value: 0
8	OA1M_A22	Opamp1 negative terminal P4 Default Value: 0
7	OA1P_A73	Opamp1 positive terminal to vref1 Default Value: 0
4	OA1P_A43	Opamp1 positive terminal ctbbus1 Default Value: 0
1	OA1P_A13	Opamp1 positive terminal P5 Default Value: 0

0	OA1P_A03	Opamp1 positive terminal amuxbusb Default Value: 0

27.1.12 CTBM0_OA1_SW_CLEAR (continued)

27.1.12 CTBM0_OA1_SW_CLEAR

Opamp1 switch control clear

Address: 0x4110008C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	None		RW1C	None		RW1C	RW1C
HW Access	A	None		A	None		A	A
Name	OA1P_A73	None [6:5]		OA1P_A43	None [3:2]		OA1P_A13	OA1P_A03

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW1C	None					RW1C
HW Access	None	A	None					A
Name	None	OA1M_A82	None [13:9]					OA1M_A22

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW1C	None	RW1C	RW1C	None	
HW Access	None		A	None	A	A	None	
Name	None [23:22]		OA1O_D82	None	OA1O_D62	OA1O_D52	None [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
21	OA1O_D82	see corresponding bit in OA1_SW Default Value: 0
19	OA1O_D62	see corresponding bit in OA1_SW Default Value: 0
18	OA1O_D52	see corresponding bit in OA1_SW Default Value: 0
14	OA1M_A82	see corresponding bit in OA1_SW Default Value: 0
8	OA1M_A22	see corresponding bit in OA1_SW Default Value: 0
7	OA1P_A73	see corresponding bit in OA1_SW Default Value: 0
4	OA1P_A43	see corresponding bit in OA1_SW Default Value: 0

1	OA1P_A13	see corresponding bit in OA1_SW Default Value: 0
0	OA1P_A03	see corresponding bit in OA1_SW Default Value: 0

27.1.13 CTBM0_CTD_SW (continued)

27.1.13 CTBM0_CTD_SW

CTDAC connection switch control

Address: 0x411000A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW1S	RW1S	None		RW1S	None
HW Access	None		RW1C	RW1C	None		RW1C	None
Name	None [7:6]		CTDS_COR	CTDS_CRS	None [3:2]		CTDD_CRD	None

Bits	15	14	13	12	11	10	9	8
SW Access	RW1S	RW1S	RW1S	RW1S	None	RW1S	RW1S	RW1S
HW Access	RW1C	RW1C	RW1C	RW1C	None	RW1C	RW1C	RW1C
Name	CTDH_ILR	CTDH_CIS	CTDH_CA0	CTDH_CHD	None	CTDH_COB	CTDO_-COS	CTDO_C6H

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15	CTDH_ILR	Hold capacitor leakage reduction (drive other side of CIS to capacitor voltage) Default Value: 0
14	CTDH_CIS	Hold capacitor isolation (from all the other switches) Default Value: 0
13	CTDH_CA0	Hold capacitor to opamp input Default Value: 0
12	CTDH_CHD	Hold capacitor connect Default Value: 0
10	CTDH_COB	Drive the CTDAC output with CTBM 1x output during hold mode in Sample and Hold operation Default Value: 0
9	CTDO_COS	ctdvout to Hold capacitor (Sample switch). Note this switch will temporarily be opened for deglitching if CTDAC.DEGLITCH_COS is set Default Value: 0

8	CTDO_C6H	P6 pin to Hold capacitor Default Value: 0
5	CTDS_COR	ctdvout to opamp input Default Value: 0
4	CTDS_CRS	ctdrefsense to opamp input Default Value: 0
1	CTDD_CRD	CTDAC Reference opamp output to ctdrefdrive Default Value: 0

27.1.14 CTBM0_CTD_SW_CLEAR (continued)

27.1.14 CTBM0_CTD_SW_CLEAR

CTDAC connection switch control clear

Address: 0x411000A4

Retention: Retained

Bits	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SW Access	None		RW1C	RW1C	None		RW1C	None
HW Access	None		A	A	None		A	None
Name	None [7:6]		CTDS_COR	CTDS_CRS	None [3:2]		CTDD_CRD	None

Bits	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SW Access	RW1C	RW1C	RW1C	RW1C	None	RW1C	RW1C	RW1C
HW Access	A	A	A	A	None	A	A	A
Name	CTDH_ILR	CTDH_CIS	CTDH_CA0	CTDH_CHD	None	CTDH_COB	CTDO_-COS	CTDO_C6H

Bits	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	**31**	**30**	**29**	**28**	**27**	**26**	**25**	**24**
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	**Name**	**Description**
15	CTDH_ILR	see corresponding bit in CTD_SW Default Value: 0
14	CTDH_CIS	see corresponding bit in CTD_SW Default Value: 0
13	CTDH_CA0	see corresponding bit in CTD_SW Default Value: 0
12	CTDH_CHD	see corresponding bit in CTD_SW Default Value: 0
10	CTDH_COB	see corresponding bit in CTD_SW Default Value: 0
9	CTDO_COS	see corresponding bit in CTD_SW Default Value: 0
8	CTDO_C6H	see corresponding bit in CTD_SW Default Value: 0

5	CTDS_COR	see corresponding bit in CTD_SW Default Value: 0
4	CTDS_CRS	see corresponding bit in CTD_SW Default Value: 0
1	CTDD_CRD	see corresponding bit in CTD_SW Default Value: 0

27.1.15 CTBM0_CTB_SW_DS_CTRL (continued)

27.1.15 CTBM0_CTB_SW_DS_CTRL

CTB bus switch control

Address: 0x411000C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	RW	None	
HW Access	None				R	R	None	
Name	None [15:12]				P3_DS_C-TRL23	P2_DS_C-TRL23	None	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	CT-D_COS_DS_CTRL	None [30:24]						

Bits	Name	Description
31	CTD_COS_DS_CTRL	Hold capacitor Sample switch (COS) Default Value: 0
11	P3_DS_CTRL23	for P33, D52, D62 (dsi_out[3]) Default Value: 0
10	P2_DS_CTRL23	for P22, D51 (dsi_out[2]) Default Value: 0

27.1.16 CTBM0_CTB_SW_SQ_CTRL

CTB bus switch Sar Sequencer control

Address: 0x411000C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	RW	None	
HW Access	None				R	R	None	
Name	None [15:12]				P3_SQ_C-TRL23	P2_SQ_C-TRL23	None	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	P3_SQ_CTRL23	for D52, D62 Default Value: 0
10	P2_SQ_CTRL23	for D51 Default Value: 0

27.1.17 CTBM0_CTB_SW_STATUS

CTB bus switch control status

Address: 0x411000C8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	R	R	None			
HW Access	W	W	W	W	None			
Name	CT-D_COS_STAT	OA1O_D62_STAT	OA1O_D52_STAT	OA0O_D51_STAT	None			

Bits	Name	Description
31	CTD_COS_STAT	see COS bit in CTD_SW Default Value: 0
30	OA1O_D62_STAT	see OA1O_D62 bit in OA1_SW Default Value: 0
29	OA1O_D52_STAT	see OA1O_D52 bit in OA1_SW Default Value: 0
28	OA0O_D51_STAT	see OA0O_D51 bit in OA0_SW Default Value: 0

27.1.18 CTBM0_OA0_OFFSET_TRIM

Opamp0 trim control

Address: 0x41100F00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		OA0_OFFSET_TRIM [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	OA0_OFFSET_TRIM	Opamp0 offset trim Default Value: 0

27.1.19 CTBM0_OA0_SLOPE_OFFSET_TRIM

Opamp0 trim control

Address: 0x41100F04

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		OA0_SLOPE_OFFSET_TRIM [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	OA0_SLOPE_OFF-SET_TRIM	Opamp0 slope offset drift trim Default Value: 0

27.1.20 CTBM0_OA0_COMP_TRIM

Opamp0 trim control

Address: 0x41100F08

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	
HW Access	None						R	
Name	None [7:2]						OA0_COMP_TRIM [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1 : 0	OA0_COMP_TRIM	Opamp0 Compensation Capacitor Trim. Value depends on the drive strength setting - 1x mode: set to 01; 10x mode: set to 11 Default Value: 0

27.1.21 CTBM0_OA1_OFFSET_TRIM

Opamp1 trim control

Address: 0x41100F0C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		OA1_OFFSET_TRIM [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	OA1_OFFSET_TRIM	Opamp1 offset trim Default Value: 0

27.1.22 CTBM0_OA1_SLOPE_OFFSET_TRIM

Opamp1 trim control

Address: 0x41100F10

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		OA1_SLOPE_OFFSET_TRIM [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	OA1_SLOPE_OFF-SET_TRIM	Opamp1 slope offset drift trim Default Value: 0

27.1.23 CTBM0_OA1_COMP_TRIM

Opamp1 trim control

Address: 0x41100F14

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	
HW Access	None						R	
Name	None [7:2]						OA1_COMP_TRIM [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1 : 0	OA1_COMP_TRIM	Opamp1 Compensation Capacitor Trim. Value depends on the drive strength setting - 1x mode: set to 01; 10x mode: set to 11 Default Value: 0

27.1.24 PASS_INTR_CAUSE

Interrupt cause register

Address: 0x411F0000

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			R	None			R
HW Access	None			W	None			W
Name	None [7:5]			CT-DAC0_INT	None [3:1]			CTB0_INT

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4	CTDAC0_INT	CTDAC0 interrupt pending Default Value: 0
0	CTB0_INT	CTB0 interrupt pending Default Value: 0

28 Continuous-Time DAC Registers

This section discusses the Continuous-Time DAC registers. It lists all the registers in mapping tables, in address order.

28.1 Register Details

Register	Address	Description
CTDAC0_CTDAC_CTRL	0x41140000	Global CTDAC control
CTDAC0_INTR	0x41140020	Interrupt request register
CTDAC0_INTR_SET	0x41140024	Interrupt request set register
CTDAC0_INTR_MASK	0x41140028	Interrupt request mask
CTDAC0_INTR_MASKED	0x4114002C	Interrupt request masked
CTDAC0_CTDAC_SW	0x411400B0	CTDAC switch control
CTDAC0_CTDAC_SW_CLEAR	0x411400B4	CTDAC switch control clear
CTDAC0_CTDAC_VAL	0x41140100	DAC Value
CTDAC0_CTDAC_VAL_NXT	0x41140104	Next DAC value (double buffering)

28.1.1 CTDAC0_CTDAC_CTRL

Global CTDAC control

Address: 0x41140000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		DEGLITCH_CNT [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [15:10]						DEGLITCH_COS	DEGLITCH_CO6

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	None					
HW Access	R	R	None					
Name	CTDAC_RANGE	OUT_EN	None [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	None	RW	
HW Access	R	R	R	R	R	None	R	
Name	ENABLED	DEEPSLEEP_ON	DSI_STROBE_LEVEL	DSI_STROBE_EN	DISABLED_MODE	None	CTDAC_MODE [25:24]	

Bits	Name	Description
31	ENABLED	0: CTDAC IP disabled (put analog in power down, open all switches) 1: CTDAC IP enabled Default Value: 0
30	DEEPSLEEP_ON	- 0: CTDAC IP disabled off during DeepSleep power mode - 1: CTDAC IP remains enabled during DeepSleep power mode (if ENABLED=1) Default Value: 0
29	DSI_STROBE_LEVEL	Select level or edge detect for DSI strobe - 0: DSI strobe signal is a pulse input, after a positive edge is detected on the DSI strobe signal the next DAC value update is done on the next CTDAC clock - 1: DSI strobe signal is a level input, as long as the DSI strobe signal remains high the CTDAC will do a next DAC value update on each CTDAC clock. Default Value: 0

28.1.1 CTDAC0_CTDAC_CTRL (continued)

28	DSI_STROBE_EN	DSI strobe input Enable. This enables CTDAC updates to be further throttled by DSI. 0: Ignore DSI strobe input 1: Only do a CTDAC update if allowed by the DSI strobe (throttle), see below for level or edge Default Value: 0
27	DISABLED_MODE	Select the output value when the output is disabled (OUT_EN=0) (for risk mitigation) 0: Tri-state CTDAC output when disabled 1: output Vssa or Vref when disabled (see OUT_EN description) Default Value: 0
25 : 24	CTDAC_MODE	DAC mode, this determines the Value decoding Default Value: 0 **0x0: UNSIGNED12 :** Unsigned 12-bit VDAC, i.e. no value decoding. **0x1: VIRT_SIGNED12 :** Virtual signed 12-bits' VDAC. Value decoding: add 0x800 to the 12-bit Value (=invert MSB), to convert the lowest signed number 0x800 to the lowest unsigned number 0x000. This is the same as the SAR handles 12-bit 'virtual' signed numbers. **0x2: RESERVED2 :** Reserved **0x3: RESERVED3 :** Reserved
23	CTDAC_RANGE	By closing the bottom switch in the R2R network the output is lifted by one LSB, effectively adding 1 0: Range is [0, 4095] * Vref / 4096 1: Range is [1, 4096] * Vref / 4096 Default Value: 0
22	OUT_EN	Output enable, intended to be used during the Hold phase of the Sample and Hold when power cycling : 0: output disabled, the output is either: - Tri-state (DISABLED_MODE=0) - or Vssa (DISABLED_MODE=1 && CTDAC_RANGE=0) - or Vref (DISABLED_MODE=1 && CTDAC_RANGE=1) 1: output enabled, CTDAC output drives the programmed VALUE Default Value: 0
9	DEGLITCH_COS	Force CTB.COS switch open after each VALUE change for the set number of clock cycles. Default Value: 0
8	DEGLITCH_CO6	Force CTDAC.CO6 switch open after each VALUE change for the set number of clock cycles. Default Value: 0
5 : 0	DEGLITCH_CNT	To prevent glitches after VALUE changes from propagating the output switch can be opened for DEGLITCH_CNT+1 clk_peri clock cycles. Default Value: 0

28.1.2 CTDAC0_INTR

Interrupt request register

Address: 0x41140020

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1C
HW Access	None							RW1S
Name	None [7:1]							VDAC_EMPTY

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	VDAC_EMPTY	VDAC Interrupt: hardware sets this interrupt when VDAC next value field is empty, i.e. was copied to the current VALUE. Write with '1' to clear bit. Default Value: 0

28.1.3 CTDAC0_INTR_SET

Interrupt request set register

Address: 0x41140024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1S
HW Access	None							A
Name	None [7:1]							VDAC_EMPTY_SET

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	VDAC_EMPTY_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

28.1.4 CTDAC0_INTR_MASK

Interrupt request mask

Address: 0x41140028

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							VDAC_EMPTY_MASK

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	VDAC_EMPTY_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0

28.1.5 CTDAC0_INTR_MASKED

Interrupt request masked

Address: 0x4114002C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							W
Name	None [7:1]							VDAC_EMPTY_MASKED

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	VDAC_EMPTY_MASKED	Logical and of corresponding request and mask bits. Default Value: 0

28.1.6 CTDAC0_CTDAC_SW

CTDAC switch control

Address: 0x411400B0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1S
HW Access	None							RW1C
Name	None [7:1]							CTDD_CVD

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1S
HW Access	None							RW1C
Name	None [15:9]							CTDO_CO6

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	CTDO_CO6	ctdvout to P6 pin. Note this switch will temporarily be opened for deglitching if DEGLITCH_CO6 is set Default Value: 0
0	CTDD_CVD	VDDA supply to ctdrefdrive Default Value: 0

28.1.7 CTDAC0_CTDAC_SW_CLEAR

CTDAC switch control clear

Address: 0x411400B4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1C
HW Access	None							A
Name	None [7:1]							CTDD_CVD

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1C
HW Access	None							A
Name	None [15:9]							CTDO_CO6

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	CTDO_CO6	see corresponding bit in CTD_SW Default Value: 0
0	CTDD_CVD	see corresponding bit in CTD_SW Default Value: 0

28.1.8 CTDAC0_CTDAC_VAL

DAC Value

Address: 0x41140100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				RW			
Name	None [15:12]				VALUE [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11 : 0	VALUE	Value, in CTDAC_MODE 1 this value is decoded Default Value: 0

28.1.9 CTDAC0_CTDAC_VAL_NXT

Next DAC value (double buffering)

Address: 0x41140104

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				VALUE [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11 : 0	VALUE	Next value for CTDAC_VAL.VALUE Default Value: 0

29 SAR ADC Registers

This section discusses the SAR ADC registers. It lists all the registers in mapping tables, in address order.

29.1 Register Details

Register	Address	Description
SAR_CTRL	0x411D0000	Analog control register.
SAR_SAMPLE_CTRL	0x411D0004	Sample control register.
SAR_SAMPLE_TIME01	0x411D0010	Sample time specification ST0 and ST1
SAR_SAMPLE_TIME23	0x411D0014	Sample time specification ST2 and ST3
SAR_RANGE_THRES	0x411D0018	Global range detect threshold register.
SAR_RANGE_COND	0x411D001C	Global range detect mode register.
SAR_CHAN_EN	0x411D0020	Enable bits for the channels
SAR_START_CTRL	0x411D0024	Start control register (firmware trigger).
SAR_CHAN_CONFIG0	0x411D0080	Channel configuration register.
SAR_CHAN_CONFIG1	0x411D0084	Channel configuration register. See SAR_CHAN_CONFIG0 for the details of bit fields.
SAR_CHAN_CONFIG2	0x411D0088	Channel configuration register. See SAR_CHAN_CONFIG0 for the details of bit fields.
SAR_CHAN_CONFIG3	0x411D008C	Channel configuration register. See SAR_CHAN_CONFIG0 for the details of bit fields.
SAR_CHAN_CONFIG4	0x411D0090	Channel configuration register. See SAR_CHAN_CONFIG0 for the details of bit fields.
SAR_CHAN_CONFIG5	0x411D0094	Channel configuration register. See SAR_CHAN_CONFIG0 for the details of bit fields.
SAR_CHAN_CONFIG6	0x411D0098	Channel configuration register. See SAR_CHAN_CONFIG0 for the details of bit fields.
SAR_CHAN_CONFIG7	0x411D009C	Channel configuration register. See SAR_CHAN_CONFIG0 for the details of bit fields.
SAR_CHAN_CONFIG8	0x411D00A0	Channel configuration register. See SAR_CHAN_CONFIG0 for the details of bit fields.
SAR_CHAN_CONFIG9	0x411D00A4	Channel configuration register. See SAR_CHAN_CONFIG0 for the details of bit fields.
SAR_CHAN_CONFIG10	0x411D00A8	Channel configuration register. See SAR_CHAN_CONFIG0 for the details of bit fields.
SAR_CHAN_CONFIG11	0x411D00AC	Channel configuration register. See SAR_CHAN_CONFIG0 for the details of bit fields.
SAR_CHAN_CONFIG12	0x411D00B0	Channel configuration register. See SAR_CHAN_CONFIG0 for the details of bit fields.
SAR_CHAN_CONFIG13	0x411D00B4	Channel configuration register. See SAR_CHAN_CONFIG0 for the details of bit fields.
SAR_CHAN_CONFIG14	0x411D00B8	Channel configuration register. See SAR_CHAN_CONFIG0 for the details of bit fields.
SAR_CHAN_CONFIG15	0x411D00BC	Channel configuration register. See SAR_CHAN_CONFIG0 for the details of bit fields.
SAR_CHAN_WORK0	0x411D0100	Channel working data register
SAR_CHAN_WORK1	0x411D0104	Channel working data register. See SAR_CHAN_WORK0 for the details of bit fields.
SAR_CHAN_WORK2	0x411D0108	Channel working data register. See SAR_CHAN_WORK0 for the details of bit fields.

Register	Address	Description
SAR_CHAN_WORK3	0x411D010C	Channel working data register. See SAR_CHAN_WORK0 for the details of bit fields.
SAR_CHAN_WORK4	0x411D0110	Channel working data register. See SAR_CHAN_WORK0 for the details of bit fields.
SAR_CHAN_WORK5	0x411D0114	Channel working data register. See SAR_CHAN_WORK0 for the details of bit fields.
SAR_CHAN_WORK6	0x411D0118	Channel working data register. See SAR_CHAN_WORK0 for the details of bit fields.
SAR_CHAN_WORK7	0x411D011C	Channel working data register. See SAR_CHAN_WORK0 for the details of bit fields.
SAR_CHAN_WORK8	0x411D0120	Channel working data register. See SAR_CHAN_WORK0 for the details of bit fields.
SAR_CHAN_WORK9	0x411D0124	Channel working data register. See SAR_CHAN_WORK0 for the details of bit fields.
SAR_CHAN_WORK10	0x411D0128	Channel working data register. See SAR_CHAN_WORK0 for the details of bit fields.
SAR_CHAN_WORK11	0x411D012C	Channel working data register. See SAR_CHAN_WORK0 for the details of bit fields.
SAR_CHAN_WORK12	0x411D0130	Channel working data register. See SAR_CHAN_WORK0 for the details of bit fields.
SAR_CHAN_WORK13	0x411D0134	Channel working data register. See SAR_CHAN_WORK0 for the details of bit fields.
SAR_CHAN_WORK14	0x411D0138	Channel working data register. See SAR_CHAN_WORK0 for the details of bit fields.
SAR_CHAN_WORK15	0x411D013C	Channel working data register. See SAR_CHAN_WORK0 for the details of bit fields.
SAR_CHAN_RESULT0	0x411D0180	Channel result data register
SAR_CHAN_RESULT1	0x411D0184	Channel result data register. See SAR_CHAN_RESULT0 for the details of bit fields.
SAR_CHAN_RESULT2	0x411D0188	Channel result data register. See SAR_CHAN_RESULT0 for the details of bit fields.
SAR_CHAN_RESULT3	0x411D018C	Channel result data register. See SAR_CHAN_RESULT0 for the details of bit fields.
SAR_CHAN_RESULT4	0x411D0190	Channel result data register. See SAR_CHAN_RESULT0 for the details of bit fields.
SAR_CHAN_RESULT5	0x411D0194	Channel result data register. See SAR_CHAN_RESULT0 for the details of bit fields.
SAR_CHAN_RESULT6	0x411D0198	Channel result data register. See SAR_CHAN_RESULT0 for the details of bit fields.
SAR_CHAN_RESULT7	0x411D019C	Channel result data register. See SAR_CHAN_RESULT0 for the details of bit fields.
SAR_CHAN_RESULT8	0x411D01A0	Channel result data register. See SAR_CHAN_RESULT0 for the details of bit fields.
SAR_CHAN_RESULT9	0x411D01A4	Channel result data register. See SAR_CHAN_RESULT0 for the details of bit fields.
SAR_CHAN_RESULT10	0x411D01A8	Channel result data register. See SAR_CHAN_RESULT0 for the details of bit fields.
SAR_CHAN_RESULT11	0x411D01AC	Channel result data register. See SAR_CHAN_RESULT0 for the details of bit fields.
SAR_CHAN_RESULT12	0x411D01B0	Channel result data register. See SAR_CHAN_RESULT0 for the details of bit fields.
SAR_CHAN_RESULT13	0x411D01B4	Channel result data register. See SAR_CHAN_RESULT0 for the details of bit fields.
SAR_CHAN_RESULT14	0x411D01B8	Channel result data register. See SAR_CHAN_RESULT0 for the details of bit fields.
SAR_CHAN_RESULT15	0x411D01BC	Channel result data register. See SAR_CHAN_RESULT0 for the details of bit fields.
SAR_CHAN_WORK_UPDATED	0x411D0200	Channel working data register 'updated' bits
SAR_CHAN_RESULT_UPDATED	0x411D0204	Channel result data register 'updated' bits
SAR_INTR	0x411D0210	Interrupt request register.
SAR_INTR_SET	0x411D0214	Interrupt set request register
SAR_INTR_MASK	0x411D0218	Interrupt mask register.
SAR_INTR_MASKED	0x411D021C	Interrupt masked request register
SAR_SATURATE_INTR	0x411D0220	Saturate interrupt request register.
SAR_SATURATE_INTR_SET	0x411D0224	Saturate interrupt set request register
SAR_SATURATE_INTR_MASK	0x411D0228	Saturate interrupt mask register.
SAR_SATURATE_INTR_MASKED	0x411D022C	Saturate interrupt masked request register
SAR_RANGE_INTR	0x411D0230	Range detect interrupt request register.
SAR_RANGE_INTR_SET	0x411D0234	Range detect interrupt set request register
SAR_RANGE_INTR_MASK	0x411D0238	Range detect interrupt mask register.

Register	Address	Description
SAR_RANGE_INTR_MASKED	0x411D023C	Range interrupt masked request register
SAR_INTR_CAUSE	0x411D0240	Interrupt cause register
SAR_INJ_CHAN_CONFIG	0x411D0280	Injection channel configuration register.
SAR_INJ_RESULT	0x411D0290	Injection channel result register
SAR_STATUS	0x411D02A0	Current status of internal SAR registers (mostly for debug)
SAR_AVG_STAT	0x411D02A4	Current averaging status (for debug)
SAR_MUX_SWITCH0	0x411D0300	SARMUX Firmware switch controls
SAR_MUX_SWITCH_CLEAR0	0x411D0304	SARMUX Firmware switch control clear
SAR_MUX_SWITCH_DS_CTRL	0x411D0340	SARMUX switch DSI control
SAR_MUX_SWITCH_SQ_CTRL	0x411D0344	SARMUX switch SAR Sequencer control
SAR_MUX_SWITCH_STATUS	0x411D0348	SARMUX switch status

29.1.1 SAR_CTRL

Analog control register.

Address: 0x411D0000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW			None	RW		
HW Access	R	R			None	R		
Name	VREF_BY-P_CAP_EN	VREF_SEL [6:4]			None	PWR_CTRL_VREF [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW	None	RW			None
HW Access	R		R	None	R			None
Name	COMP_DLY [15:14]		SAR_HW_CTRL_NEGVREF	None	NEG_SEL [11:9]			None

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW	RW	RW			
HW Access	None		R	R	R			
Name	None [23:22]		REF-BUF_EN	BOOST-PUMP_EN	SPARE [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW		
HW Access	R	R	R	R	R	R		
Name	ENABLED	SWITCH_-DISABLE	DSI_MODE	DSI_SYN-C_CONFIG	DEEPS-LEEP_ON	COMP_PWR [26:24]		

Bits	Name	Description
31	ENABLED	- 0: SAR disabled (put analog in power down and stop clocks), also can clear FW_TRIGGER and INJ_START_EN (if not tailgaiting) on write. - 1: SAR enabled. Default Value: 0 Default Value: 0
30	SWITCH_DISABLE	Disable SAR sequencer from enabling routing switches (note DSI and firmware can always close switches independent of this control) - 0: Normal mode, SAR sequencer changes switches according to pin address in channel configurations - 1: Switches disabled, SAR sequencer does not enable any switches, it is the responsibility of the firmware or UDBs (through DSI) to set the switches to route the signal to be converted through the SARMUX Default Value: 0

29.1.1 SAR_CTRL (continued)

29	DSI_MODE	SAR sequencer takes configuration from DSI signals (note this also has the same effect as SWITCH_DISABLE==1) - 0: Normal mode, SAR sequencer operates according to CHAN_EN enables and CHAN_CONFIG channel configurations - 1: CHAN_EN, INJ_START_EN and channel configurations in CHAN_CONFIG and INJ_CHAN_CONFIG are ignored Default Value: 0
28	DSI_SYNC_CONFIG	- 0: bypass clock domain synchronization of the DSI config signals. - 1: synchronize the DSI config signals to peripheral clock domain. Default Value: 1
27	DEEPSLEEP_ON	- 0: SARMUX IP disabled off during DeepSleep power mode - 1: SARMUX IP remains enabled during DeepSleep power mode (if ENABLED=1) Default Value: 0
26 : 24	COMP_PWR	Comparator power mode. Default Value: 0 **0x0: P100 :** Reserved **0x1: P80 :** Reserved **0x2: P60 :** Reserved **0x3: P50 :** Power = 50%, use this for 500-1000Ksps **0x4: P40 :** Power = 40%, use this for 250-500Ksps **0x5: P30 :** Power = 30%, use this for 100-250Ksps **0x6: P20 :** Power = 20%, use this for 100-250Ksps **0x7: P10 :** Power = 10%, use this for <100Ksps
21	REFBUF_EN	For normal ADC operation this bit must be set, for all reference choices - internal, external or vdda based reference. Setting this bit is critical to proper function of switches inside SARREF block. Default Value: 0
20	BOOSTPUMP_EN	Reserved, keep this bit at default value Default Value: 0
19 : 16	SPARE	Reserved, keep this bit at default value Default Value: 0
15 : 14	COMP_DLY	Set the comparator latch delay in accordance with SAR conversion rate Default Value: 0 **0x0: D2P5 :** Reserved **0x1: D4 :** Reserved **0x2: D10 :** Reserved

29.1.1 SAR_CTRL (continued)

		0x3: D12 : Select this option for all operating modes
13	SAR_HW_C-TRL_NEGVREF	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for VREF to NEG switch. Default Value: 0
11 : 9	NEG_SEL	SARADC internal NEG selection for Single ended conversion Default Value: 0 **0x0: VSSA_KELVIN :** NEG input of SARADC is connected to "vssa_kelvin", gives more precision around zero. Note this opens both SARADC internal switches, therefore use this value to insert a break-before-make cycle on those switches when SWITCH_DISABLE is high. **0x1: ART_VSSA :** Reserved **0x2: P1 :** NEG input of SARADC is connected to P1 pin of SARMUX **0x3: P3 :** NEG input of SARADC is connected to P3 pin of SARMUX **0x4: P5 :** NEG input of SARADC is connected to P5 pin of SARMUX **0x5: P7 :** NEG input of SARADC is connected to P7 pin of SARMUX **0x6: ACORE :** Reserved **0x7: VREF :** NEG input of SARADC is shorted with VREF input of SARADC.
7	VREF_BYP_CAP_EN	VREF bypass cap enable for when VREF buffer is on Default Value: 0
6 : 4	VREF_SEL	SARADC internal VREF selection. Default Value: 0 **0x0: VREF0 :** Reserved **0x1: VREF1 :** Reserved **0x2: VREF2 :** Reserved **0x3: VREF_AROUTE :** Reserved **0x4: VBGR :** 1.2V from BandGap (VREF buffer on) **0x5: VREF_EXT :** External precision Vref direct from a pin (low impedance path). **0x6: VDDA_DIV_2 :** Vdda/2 (VREF buffer on) **0x7: VDDA :** Vdda.

29.1.1 SAR_CTRL (continued)

2 : 0	PWR_CTRL_VREF	VREF buffer low power mode. Default Value: 0 **0x0: PWR_100 :** full power (100%) (default), bypass cap, max clk_sar is 18MHz. **0x1: PWR_80 :** 80% power **0x2: PWR_60 :** 60% power **0x3: PWR_50 :** 50% power **0x4: PWR_40 :** 40% power **0x5: PWR_30 :** 30% power **0x6: PWR_20 :** 20% power **0x7: PWR_10 :** 10% power

29.1.2 SAR_SAMPLE_CTRL

Sample control register.

Address: 0x411D0004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW			RW	RW	RW	None
HW Access	R	R			R	R	R	None
Name	AVG_SHIFT	AVG_CNT [6:4]			DIFFEREN-TIAL_-SIGNED	SIN-GLE_END-ED_SIGNED	LEFT_ALIGN	None

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							AVG_-MODE

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [23:20]				DSI_SYN-C_TRIG-GER	DSI_TRIG-GER_LEV-EL	DSI_TRIG-GER_EN	CONTINU-OUS

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	EO-S_DSI_OUT_EN	None [30:24]						

Bits	Name	Description
31	EOS_DSI_OUT_EN	Enable to output EOS_INTR to DSI. When enabled each time EOS_INTR is set by the hardware also a trigger pulse is send on the tr_sar_out signal. Default Value: 0
19	DSI_SYNC_TRIGGER	- 0: bypass clock domain synchronization of the trigger signal. - 1: synchronize the trigger signal to the SAR clock domain, if needed an edge detect is done in the peripheral clock domain. Default Value: 1

29.1.2 SAR_SAMPLE_CTRL (continued)

18	DSI_TRIGGER_LEVEL	- 0: trigger signal is a pulse input, a positive edge detected on the trigger signal triggers a new scan. - 1: trigger signal is a level input, as long as the trigger signal remains high the SAR will do continuous scans. Default Value: 0
17	DSI_TRIGGER_EN	- 0: firmware trigger only: disable hardware trigger tr_sar_in. - 1: enable hardware trigger tr_sar_in (e.g. from TCPWM, GPIO or UDB). Default Value: 0
16	CONTINUOUS	- 0: Wait for next FW_TRIGGER (one shot) or hardware trigger (e.g. from TPWM for periodic triggering) before scanning enabled channels. - 1: Continuously scan enabled channels, ignore triggers. Default Value: 0
8	AVG_MODE	Averaging mode, in DSI mode this bit is ignored and only AccuNDump mode is available. Default Value: 0 **0x0: ACCUNDUMP :** Accumulate and Dump (1st order accumulate and dump filter): a channel will be sampled back to back and averaged **0x1: INTERLEAVED :** Interleaved: Each scan (trigger) one sample is taken per channel and averaged over several scans.
7	AVG_SHIFT	Averaging shifting: after averaging the result is shifted right to fit in 12 bits. Default Value: 0
6 : 4	AVG_CNT	Averaging Count for channels that have averaging enabled (AVG_EN). A channel will be sampled (1<<(AVG_CNT+1)) = [2..256] times. - In ACCUNDUMP mode (1st order accumulate and dump filter) a channel will be sampled back to back, the average result is calculated and stored and then the next enabled channel is sampled. If shifting is not enabled (AVG_SHIFT=0) then the result is forced to shift right so that is fits in 16 bits, so right shift is done by max(0,AVG_CNT-3). - In INTERLEAVED mode one sample is taken per triggered scan, only in the scan where the final averaging count is reached a valid average is calculated and stored in the RESULT register (by definition the same scan for all the channels that have averaging enabled). In all other scans the RESULT register for averaged channels will have an invalid result and the intermediate accumulated value is stored in the 16-bit WORK register. In this mode make sure that the averaging count is low enough to ensure that the intermediate value does not exceed 16-bits otherwise the MSBs will be lost. So for a 12-bit resolution the averaging count should be set to 16 or less (AVG_CNT=<3). Default Value: 0
3	DIFFERENTIAL_SIGNED	Output data from a differential conversion as a signed value when DIFFERENTIAL_EN or NEG_ADDR_EN is set to 1 Default Value: 1 **0x0: UNSIGNED :** result data is unsigned (zero extended if needed) **0x1: SIGNED :** Default: result data is signed (sign extended if needed)
2	SINGLE_ENDED_- SIGNED	Output data from a single ended conversion as a signed value Default Value: 0 **0x0: UNSIGNED :** Default: result data is unsigned (zero extended if needed) **0x1: SIGNED :** result data is signed (sign extended if needed)

29.1.2 SAR_SAMPLE_CTRL (continued)

1	LEFT_ALIGN	Left align data in data[15:0], default data is right aligned in data[11:0], with sign extension to 16 bits if the channel is differential. Default Value: 0

29.1.3 SAR_SAMPLE_TIME01

Sample time specification ST0 and ST1

Address: 0x411D0010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SAMPLE_TIME0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						SAMPLE_TIME0 [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	SAMPLE_TIME1 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None						RW	
HW Access	None						R	
Name	None [31:26]						SAMPLE_TIME1 [25:24]	

Bits	Name	Description
25 : 16	SAMPLE_TIME1	Sample time1 Default Value: 3
9 : 0	SAMPLE_TIME0	Sample time0 (aperture) in ADC clock cycles. Note that actual sample time is one clock less than specified here. The minimum sample time is 167ns, which is 3.0 cycles (4 in this field) with an 18MHz clock. Minimum legal value in this register is 2. Default Value: 3

29.1.4 SAR_SAMPLE_TIME23

Sample time specification ST2 and ST3

Address: 0x411D0014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SAMPLE_TIME2 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						SAMPLE_TIME2 [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	SAMPLE_TIME3 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None						RW	
HW Access	None						R	
Name	None [31:26]						SAMPLE_TIME3 [25:24]	

Bits	Name	Description
25 : 16	SAMPLE_TIME3	Sample time3 Default Value: 3
9 : 0	SAMPLE_TIME2	Sample time2 Default Value: 3

29.1.5 SAR_RANGE_THRES

Global range detect threshold register.

Address: 0x411D0018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	RANGE_LOW [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	RANGE_LOW [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	RANGE_HIGH [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	RANGE_HIGH [31:24]							

Bits	Name	Description
31 : 16	RANGE_HIGH	High threshold for range detect. Default Value: 0
15 : 0	RANGE_LOW	Low threshold for range detect. Default Value: 0

29.1.6 SAR_RANGE_COND

Global range detect mode register.

Address: 0x411D001C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None					
HW Access	R		None					
Name	RANGE_COND [31:30]		None [29:24]					

Bits	Name	Description
31 : 30	RANGE_COND	Range condition select. Default Value: 0 **0x0: BELOW :** result < RANGE_LOW **0x1: INSIDE :** RANGE_LOW <= result < RANGE_HIGH **0x2: ABOVE :** RANGE_HIGH <= result **0x3: OUTSIDE :** result < RANGE_LOW || RANGE_HIGH <= result

29.1.7 SAR_CHAN_EN

Enable bits for the channels

Address: 0x411D0020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CHAN_EN [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CHAN_EN [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CHAN_EN	Channel enable. - 0: the corresponding channel is disabled. - 1: the corresponding channel is enabled, it will be included in the next scan. Default Value: 0

29.1.8 SAR_START_CTRL

Start control register (firmware trigger).

Address: 0x411D0024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1S
HW Access	None							RW1C
Name	None [7:1]							FW_TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	FW_TRIGGER	When firmware writes a 1 here it will trigger the next scan of enabled channels, hardware clears this bit when the scan started with this trigger is completed. If scanning continuously the trigger is ignored and hardware clears this bit after the next scan is done. This bit is also cleared when the SAR is disabled. Default Value: 0

29.1.9 SAR_CHAN_CONFIG0

Channel configuration register.

Address: 0x411D0080

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	POS_PORT_ADDR [6:4]			None	POS_PIN_ADDR [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW		None	RW	None	RW
HW Access	None		R		None	R	None	R
Name	None [15:14]		SAMPLE_TIME_SEL [13:12]		None	AVG_EN	None	DIFFEREN-TIAL_EN

Bits	23	22	21	20	19	18	17	16
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	NEG_PORT_ADDR [22:20]			None	NEG_PIN_ADDR [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						RW
HW Access	R	None						R
Name	DSI_OUT_EN	None [30:25]						NEG_AD-DR_EN

Bits	Name	Description
31	DSI_OUT_EN	DSI data output enable for this channel. - 0: the conversion result for this channel is only stored in the channel data register and the corresponding CHAN_DATA_VALID bit is set. - 1: the conversion result for this channel is stored in the channel data register and the corresponding CHAN_DATA_VALID bit is set. The same data (same formatting), together with the channel number, is sent out on the DSI communication channel for processing in UDBs. Default Value: 0
24	NEG_ADDR_EN	1 - The NEG_PIN_ADDR and NEG_PORT_ADDR determines what drives the Vminus pin. This is a variation of differential mode with no even-odd pair limitation 0 - The NEG_SEL determines what drives the Vminus pin. Default Value: 0
22 : 20	NEG_PORT_ADDR	Address of the neg port that contains the pin to be sampled by this channel. Default Value: 0 **0x0: SARMUX :** SARMUX pins.

29.1.9 SAR_CHAN_CONFIG0 (continued)

		0x5: AROUTE_VIRT2 : Reserved
		0x6: AROUTE_VIRT1 : Reserved
		0x7: SARMUX_VIRT : SARMUX virtual port (VPORT0)
18 : 16	NEG_PIN_ADDR	Address of the neg pin to be sampled by this channel. Default Value: 0
13 : 12	SAMPLE_TIME_SEL	Sample time select: select which of the 4 global sample times to use for this channel Default Value: 0
10	AVG_EN	Averaging enable for this channel. If set the AVG_CNT and AVG_SHIFT settings are used for sampling the addressed pin(s) Default Value: 0
8	DIFFERENTIAL_EN	Differential enable for this channel. If NEG_ADDR_EN=0 and this bit is 1 then POS_PIN_ADDR[0] is ignored and considered to be 0, i.e. POS_PIN_ADDR points to the even pin of a pin pair. In that case the even pin of the pair is connected to Vplus and the odd pin of the pair is connected to Vminus. POS_PORT_ADDR is used to identify the port that contains the pins. - 0: The voltage on the addressed pin is measured (Single-ended) and the resulting value is stored in the corresponding data register. - 1: The differential voltage on the addressed pin pair is measured and the resulting value is stored in the corresponding data register. (if NEG_ADDR_EN=0 then POS_PIN_ADDR[0] is ignored). Default Value: 0
6 : 4	POS_PORT_ADDR	Address of the port that contains the pin to be sampled by this channel (connected to Vplus) Default Value: 0
		0x0: SARMUX : SARMUX pins.
		0x1: CTB0 : CTB0
		0x2: CTB1 : CTB1
		0x3: CTB2 : Reserved
		0x4: CTB3 : Reserved
		0x5: AROUTE_VIRT2 : Reserved
		0x6: AROUTE_VIRT1 : Reserved
		0x7: SARMUX_VIRT : SARMUX virtual port (VPORT0)
2 : 0	POS_PIN_ADDR	Address of the pin to be sampled by this channel (connected to Vplus) Default Value: 0

29.1.10 SAR_CHAN_WORK0

Channel working data register

Address: 0x411D0100

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	WORK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	WORK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	CHAN_WORK_UPDATED_MIR	None [30:24]						

Bits	Name	Description
31	CHAN_WORK_UPDATED_MIR	mirror bit of corresponding bit in SAR_CHAN_WORK_UPDATED register Default Value: 0
15 : 0	WORK	SAR conversion working data of the channel. The data is written here right after sampling this channel. Default Value: Undefined

29.1.11 SAR_CHAN_RESULT0

Channel result data register

Address: 0x411D0180

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	RESULT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	RESULT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	R	None				
HW Access	W	W	W	None				
Name	CHAN_RE-SULT_UP-DATED_MIR	RANGE_IN-TR_MIR	SATU-RATE_IN-TR_MIR	None [28:24]				

Bits	Name	Description
31	CHAN_RESULT_UPDAT-ED_MIR	mirror bit of corresponding bit in SAR_CHAN_RESULT_UPDATED register Default Value: 0
30	RANGE_INTR_MIR	mirror bit of corresponding bit in SAR_RANGE_INTR register Default Value: 0
29	SATURATE_INTR_MIR	mirror bit of corresponding bit in SAR_SATURATE_INTR register Default Value: 0
15 : 0	RESULT	SAR conversion result of the channel. The data is copied here from the WORK field after all enabled channels in this scan have been sampled. Default Value: Undefined

29.1.12 SAR_CHAN_WORK_UPDATED

Channel working data register 'updated' bits

Address: 0x411D0200

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	CHAN_WORK_UPDATED [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	CHAN_WORK_UPDATED [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CHAN_WORK_UPDATED	If set the corresponding WORK register was updated, i.e. was already sampled during the current scan and, in case of Interleaved averaging, reached the averaging count. If this bit is low then either the channel is not enabled or the averaging count is not yet reached for Interleaved averaging. Default Value: 0

29.1.13 SAR_CHAN_RESULT_UPDATED

Channel result data register 'updated' bits

Address: 0x411D0204

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	CHAN_RESULT_UPDATED [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	CHAN_RESULT_UPDATED [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CHAN_RESULT_UPDAT-ED	If set the corresponding RESULT register was updated, i.e. was sampled during the previous scan and, in case of Interleaved averaging, reached the averaging count. If this bit is low then either the channel is not enabled or the averaging count is not yet reached for Interleaved aver-aging. Default Value: 0

29.1.14 SAR_INTR

Interrupt request register.

Address: 0x411D0210

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
Name	INJ_COLLI-SION_INTR	IN-J_RANGE_INTR	INJ_SATU-RATE_INTR	IN-J_EOC_IN-TR	DSI_COLLI-SION_INTR	FW_COLLI-SION_INTR	OVER-FLOW_IN-TR	EOS_INTR

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	INJ_COLLISION_INTR	Injection Collision Interrupt: hardware sets this interrupt when the injection trigger signal is asserted (INJ_START_EN==1 && INJ_TAILGATING==0) while the SAR is BUSY. Raising this interrupt is delayed to when the sampling of the injection channel has been completed, i.e. not when the preceding scan with which this trigger collided is completed. When this interrupt is set it implies that the injection channel was sampled later than was intended. Write with '1' to clear bit. Default Value: 0
6	INJ_RANGE_INTR	Injection Range detect Interrupt: hardware sets this interrupt if the injection conversion result (after averaging) met the condition specified by the SAR_RANGE registers. Write with '1' to clear bit. Default Value: 0
5	INJ_SATURATE_INTR	Injection Saturation Interrupt: hardware sets this interrupt if an injection conversion result (before averaging) is either 0x000 or 0xFFF, this is an indication that the ADC likely saturated. Write with '1' to clear bit. Default Value: 0

29.1.14 SAR_INTR (continued)

4	INJ_EOC_INTR	Injection End of Conversion Interrupt: hardware sets this interrupt after completing the conversion for the injection channel (irrespective of if tailgating was used). Write with '1' to clear bit. Default Value: 0
3	DSI_COLLISION_INTR	DSI Collision Interrupt: hardware sets this interrupt when the DSI trigger signal is asserted while the SAR is BUSY. Raising this interrupt is delayed to when the scan caused by the DSI trigger has been completed, i.e. not when the preceding scan with which this trigger collided is completed. When this interrupt is set it implies that the channels were sampled later than was intended (jitter). Write with '1' to clear bit. Default Value: 0
2	FW_COLLISION_INTR	Firmware Collision Interrupt: hardware sets this interrupt when FW_TRIGGER is asserted while the SAR is BUSY. Raising this interrupt is delayed to when the scan caused by the FW_TRIGGER has been completed, i.e. not when the preceding scan with which this trigger collided is completed. When this interrupt is set it implies that the channels were sampled later than was intended (jitter). Write with '1' to clear bit. Default Value: 0
1	OVERFLOW_INTR	Overflow Interrupt: hardware sets this interrupt when it sets a new EOS_INTR while that bit was not yet cleared by the firmware. Write with '1' to clear bit. Default Value: 0
0	EOS_INTR	End Of Scan Interrupt: hardware sets this interrupt after completing a scan of all the enabled channels. Write with '1' to clear bit. Default Value: 0

29.1.15 SAR_INTR_SET

Interrupt set request register

Address: 0x411D0214

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	A	A	A	A	A	A	A	A
Name	INJ_COLLI-SION_SET	IN-J_RANGE_SET	INJ_SATU-RATE_SET	IN-J_EOC_SET	DSI_COLLI-SION_SET	FW_COLLI-SION_SET	OVER-FLOW_SET	EOS_SET

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	INJ_COLLISION_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
6	INJ_RANGE_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
5	INJ_SATURATE_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
4	INJ_EOC_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
3	DSI_COLLISION_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
2	FW_COLLISION_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
1	OVERFLOW_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

29.1.15 SAR_INTR_SET (continued)

0	EOS_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

29.1.16 SAR_INTR_MASK

Interrupt mask register.

Address: 0x411D0218

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	INJ_COLLISION_MASK	INJ_RANGE_MASK	INJ_SATURATE_MASK	INJ_EOC_MASK	DSI_COLLISION_MASK	FW_COLLISION_MASK	OVERFLOW_MASK	EOS_MASK

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	INJ_COLLISION_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
6	INJ_RANGE_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
5	INJ_SATURATE_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
4	INJ_EOC_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
3	DSI_COLLISION_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	FW_COLLISION_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	OVERFLOW_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0

29.1.16 SAR_INTR_MASK (continued)

0	EOS_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0

29.1.17 SAR_INTR_MASKED

Interrupt masked request register

Address: 0x411D021C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	INJ_COLLI-SION_MASKED	IN-J_RANGE_MASKED	INJ_SATU-RATE_MASKED	IN-J_EOC_MASKED	DSI_COLLI-SION_MASKED	FW_COLLI-SION_MASKED	OVER-FLOW_MASKED	EO-S_MASKED

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	INJ_COLLI-SION_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
6	INJ_RANGE_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
5	INJ_SATU-RATE_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
4	INJ_EOC_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
3	DSI_COLLI-SION_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
2	FW_COLLI-SION_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
1	OVERFLOW_MASKED	Logical and of corresponding request and mask bits. Default Value: 0

29.1.17 SAR_INTR_MASKED (continued)

0	EOS_MASKED	Logical and of corresponding request and mask bits. Default Value: 0

29.1.18 SAR_SATURATE_INTR

Saturate interrupt request register.

Address: 0x411D0220

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C							
HW Access	RW1S							
Name	SATURATE_INTR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1C							
HW Access	RW1S							
Name	SATURATE_INTR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	SATURATE_INTR	Saturate Interrupt: hardware sets this interrupt for each channel if a conversion result (before averaging) of that channel is either 0x000 or 0xFFF, this is an indication that the ADC likely saturated. Write with '1' to clear bit. Default Value: 0

29.1.19 SAR_SATURATE_INTR_SET

Saturate interrupt set request register

Address: 0x411D0224

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S							
HW Access	A							
Name	SATURATE_SET [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1S							
HW Access	A							
Name	SATURATE_SET [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	SATURATE_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

29.1.20 SAR_SATURATE_INTR_MASK

Saturate interrupt mask register.

Address: 0x411D0228

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SATURATE_MASK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	SATURATE_MASK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	SATURATE_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0

29.1.21 SAR_SATURATE_INTR_MASKED

Saturate interrupt masked request register

Address: 0x411D022C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	SATURATE_MASKED [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	SATURATE_MASKED [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	SATURATE_MASKED	Logical and of corresponding request and mask bits. Default Value: 0

29.1.22 SAR_RANGE_INTR

Range detect interrupt request register.

Address: 0x411D0230

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C							
HW Access	RW1S							
Name	RANGE_INTR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1C							
HW Access	RW1S							
Name	RANGE_INTR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	RANGE_INTR	Range detect Interrupt: hardware sets this interrupt for each channel if the conversion result (after averaging) of that channel met the condition specified by the SAR_RANGE registers. Write with '1' to clear bit. Default Value: 0

29.1.23 SAR_RANGE_INTR_SET

Range detect interrupt set request register

Address: 0x411D0234

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S							
HW Access	A							
Name	RANGE_SET [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1S							
HW Access	A							
Name	RANGE_SET [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	RANGE_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

29.1.24 SAR_RANGE_INTR_MASK

Range detect interrupt mask register.

Address: 0x411D0238

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	RANGE_MASK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	RANGE_MASK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	RANGE_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0

29.1.25 SAR_RANGE_INTR_MASKED

Range interrupt masked request register

Address: 0x411D023C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	RANGE_MASKED [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	RANGE_MASKED [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	RANGE_MASKED	Logical and of corresponding request and mask bits. Default Value: 0

29.1.26 SAR_INTR_CAUSE

Interrupt cause register

Address: 0x411D0240

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	INJ_COLLI-SION_MASKED_MIR	IN-J_RANGE_MASKED_MIR	INJ_SATU-RATE_MASKED_MIR	IN-J_EOC_MASKED_MIR	DSI_COLLI-SION_MASKED_MIR	FW_COLLI-SION_MASKED_MIR	OVER-FLOW_MASKED_MIR	EO-S_MASKED_MIR

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	None					
HW Access	W	W	None					
Name	RANGE_MASKED_RED	SATU-RATE_MASKED_RED	None [29:24]					

Bits	Name	Description
31	RANGE_MASKED_RED	Reduction OR of all SAR_RANGE_INTR_MASKED bits Default Value: 0
30	SATU-RATE_MASKED_RED	Reduction OR of all SAR_SATURATION_INTR_MASKED bits Default Value: 0
7	INJ_COLLI-SION_MASKED_MIR	Mirror copy of corresponding bit in SAR_INTR_MASKED Default Value: 0
6	IN-J_RANGE_MASKED_MIR	Mirror copy of corresponding bit in SAR_INTR_MASKED Default Value: 0
5	INJ_SATU-RATE_MASKED_MIR	Mirror copy of corresponding bit in SAR_INTR_MASKED Default Value: 0
4	INJ_EOC_MASKED_MIR	Mirror copy of corresponding bit in SAR_INTR_MASKED Default Value: 0

29.1.26 SAR_INTR_CAUSE (continued)

3	DSI_COLLI-SION_MASKED_MIR	Mirror copy of corresponding bit in SAR_INTR_MASKED Default Value: 0
2	FW_COLLI-SION_MASKED_MIR	Mirror copy of corresponding bit in SAR_INTR_MASKED Default Value: 0
1	OVER-FLOW_MASKED_MIR	Mirror copy of corresponding bit in SAR_INTR_MASKED Default Value: 0
0	EOS_MASKED_MIR	Mirror copy of corresponding bit in SAR_INTR_MASKED Default Value: 0

29.1.27 SAR_INJ_CHAN_CONFIG

Injection channel configuration register.

Address: 0x411D0280

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	INJ_PORT_ADDR [6:4]			None	INJ_PIN_ADDR [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW		None	RW	None	RW
HW Access	None		R		None	R	None	R
Name	None [15:14]		INJ_SAMPLE_TIME_SEL [13:12]		None	IN-J_AVG_EN	None	INJ_DIF-FEREN-TIAL_EN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1S	RW	None					
HW Access	RW1C	R	None					
Name	IN-J_START_E N	INJ_TAIL-GATING	None [29:24]					

Bits	Name	Description
31	INJ_START_EN	Set by firmware to enable the injection channel. If INJ_TAILGATING is not set this bit also functions as trigger for this channel. Cleared by hardware after this channel has been sampled (i.e. this channel is always one shot even if CONTINUOUS is set). Also cleared if the SAR is disabled. Default Value: 0
30	INJ_TAILGATING	Injection channel tailgating. - 0: no tailgating for this channel, SAR is immediately triggered when the INJ_START_EN bit is set. - 1: injection channel tailgating. The addressed pin is sampled after the next trigger and after all enabled channels have been scanned. Default Value: 0
13 : 12	INJ_SAMPLE_TIME_SEL	Injection sample time select: select which of the 4 global sample times to use for this channel Default Value: 0
10	INJ_AVG_EN	Averaging enable for this channel. If set the AVG_CNT and AVG_SHIFT settings are used for sampling the addressed pin(s) Default Value: 0

29.1.27 SAR_INJ_CHAN_CONFIG (continued)

8	INJ_DIFFERENTIAL_EN	Differential enable for this channel. - 0: The voltage on the addressed pin is measured (Single-ended) and the resulting value is stored in the corresponding data register. - 1: The differential voltage on the addressed pin pair is measured and the resulting value is stored in the corresponding data register. (INJ_PIN_ADDR[0] is ignored). Default Value: 0
6 : 4	INJ_PORT_ADDR	Address of the port that contains the pin to be sampled by this channel. Default Value: 0 **0x0: SARMUX :** SARMUX pins. **0x1: CTB0 :** CTB0 **0x2: CTB1 :** CTB1 **0x3: CTB2 :** Reserved **0x4: CTB3 :** Reserved **0x6: AROUTE_VIRT :** Reserved **0x7: SARMUX_VIRT :** SARMUX virtual port
2 : 0	INJ_PIN_ADDR	Address of the pin to be sampled by this injection channel. If differential is enabled then INJ_PIN_ADDR[0] is ignored and considered to be 0, i.e. INJ_PIN_ADDR points to the even pin of a pin pair. Default Value: 0

29.1.28 SAR_INJ_RESULT

Injection channel result register

Address: 0x411D0290

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	INJ_RESULT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	INJ_RESULT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	R	R	None			
HW Access	W	W	W	W	None			
Name	INJ_EOC_INTR_MIR	INJ_RANGE_INTR_MIR	INJ_SATURATE_INTR_MIR	INJ_COLLISION_INTR_MIR	None [27:24]			

Bits	Name	Description
31	INJ_EOC_INTR_MIR	mirror bit of corresponding bit in SAR_INTR register Default Value: 0
30	INJ_RANGE_INTR_MIR	mirror bit of corresponding bit in SAR_INTR register Default Value: 0
29	INJ_SATURATE_INTR_MIR	mirror bit of corresponding bit in SAR_INTR register Default Value: 0
28	INJ_COLLISION_INTR_MIR	mirror bit of corresponding bit in SAR_INTR register Default Value: 0
15 : 0	INJ_RESULT	SAR conversion result of the channel. Default Value: Undefined

29.1.29 SAR_STATUS

Current status of internal SAR registers (mostly for debug)

Address: 0x411D02A0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			R				
HW Access	None			W				
Name	None [7:5]			CUR_CHAN [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	None					
HW Access	W	W	None					
Name	BUSY	SW_VREF_NEG	None [29:24]					

Bits	Name	Description
31	BUSY	If high then the SAR is busy with a conversion. This bit is always high when CONTINUOUS is set. Firmware should wait for this bit to be low before putting the SAR in power down. Default Value: 0
30	SW_VREF_NEG	the current switch status, including DSI and sequencer controls, of the switch in the SARADC that shorts NEG with VREF input (see NEG_SEL). Default Value: 0
4 : 0	CUR_CHAN	current channel being sampled (channel 16 indicates the injection channel), only valid if BUSY. Default Value: 0

29.1.30 SAR_AVG_STAT

Current averaging status (for debug)

Address: 0x411D02A4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	CUR_AVG_ACCU [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	CUR_AVG_ACCU [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R	None			R			
HW Access	W	None			W			
Name	IN-TRLV_BUSY	None [22:20]			CUR_AVG_ACCU [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	CUR_AVG_CNT [31:24]							

Bits	Name	Description
31 : 24	CUR_AVG_CNT	the current value of the averaging counter. Note that the value shown is updated after the sampling time and therefore runs ahead of the accumulator update. Default Value: 0
23	INTRLV_BUSY	If high then the SAR is in the middle of Interleaved averaging spanning several scans. While this bit is high the Firmware should not make any changes to the configuration registers otherwise some results may be incorrect. Note that the CUR_AVG_CNT status register below gives an indication how many more scans need to be done to complete the Interleaved averaging. This bit can be cleared by changing the averaging mode to ACCUNDUMP or by disabling the SAR. Default Value: 0
19 : 0	CUR_AVG_ACCU	the current value of the averaging accumulator Default Value: 0

29.1.31 SAR_MUX_SWITCH0

SARMUX Firmware switch controls

Address: 0x411D0300

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
Name	MUX_F-W_P7_VPLUS	MUX_F-W_P6_VPLUS	MUX_F-W_P5_VPLUS	MUX_F-W_P4_VPLUS	MUX_F-W_P3_VPLUS	MUX_F-W_P2_VPLUS	MUX_F-W_P1_VPLUS	MUX_F-W_P0_VPLUS

Bits	15	14	13	12	11	10	9	8
SW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
Name	MUX_F-W_P7_VMI-NUS	MUX_F-W_P6_VMI-NUS	MUX_F-W_P5_VMI-NUS	MUX_F-W_P4_VMI-NUS	MUX_F-W_P3_VMI-NUS	MUX_F-W_P2_VMI-NUS	MUX_F-W_P1_VMI-NUS	MUX_F-W_P0_VMI-NUS

Bits	23	22	21	20	19	18	17	16
SW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
Name	MUX_F-W_SAR-BUS1_VPLUS	MUX_F-W_SAR-BUS0_VPLUS	MUX_F-W_AMUX-BUSB_VMINUS	MUX_F-W_AMUX-BUSA_VMINUS	MUX_F-W_AMUX-BUSB_VPLUS	MUX_F-W_AMUX-BUSA_VPLUS	MUX_FW_-TEMP_VPLUS	MUX_F-W_VS-SA_VMINUS

Bits	31	30	29	28	27	26	25	24
SW Access	None		RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	None		RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
Name	None [31:30]		MUX_F-W_P7_COREIO3	MUX_F-W_P6_COREIO2	MUX_F-W_P5_COREIO1	MUX_F-W_P4_COREIO0	MUX_F-W_SAR-BUS1_VMINUS	MUX_F-W_SAR-BUS0_VMINUS

Bits	Name	Description
29	MUX_FW_P7_COREIO3	Firmware control: 0=open, 1=close switch between P7 and coreio3 signal. Write with '1' to set bit. Default Value: 0
28	MUX_FW_P6_COREIO2	Firmware control: 0=open, 1=close switch between P6 and coreio2 signal. Write with '1' to set bit. Default Value: 0
27	MUX_FW_P5_COREIO1	Firmware control: 0=open, 1=close switch between P5 and coreio1 signal. Write with '1' to set bit. Default Value: 0
26	MUX_FW_P4_COREIO0	Firmware control: 0=open, 1=close switch between P4 and coreio0 signal. Write with '1' to set bit. Default Value: 0

29.1.31 SAR_MUX_SWITCH0 (continued)

25	MUX_FW_SAR-BUS1_VMINUS	Firmware control: 0=open, 1=close switch between sarbus1 and vminus signal. Write with '1' to set bit. Default Value: 0
24	MUX_FW_SAR-BUS0_VMINUS	Firmware control: 0=open, 1=close switch between sarbus0 and vminus signal. Write with '1' to set bit. Default Value: 0
23	MUX_FW_SAR-BUS1_VPLUS	Firmware control: 0=open, 1=close switch between sarbus1 and vplus signal. Write with '1' to set bit. Default Value: 0
22	MUX_FW_SAR-BUS0_VPLUS	Firmware control: 0=open, 1=close switch between sarbus0 and vplus signal. Write with '1' to set bit. Default Value: 0
21	MUX_FW_AMUXBUS-B_VMINUS	Firmware control: 0=open, 1=close switch between amuxbusb and vminus signal. Write with '1' to set bit. Default Value: 0
20	MUX_FW_AMUX-BUSA_VMINUS	Firmware control: 0=open, 1=close switch between amuxbusa and vminus signal. Write with '1' to set bit. Default Value: 0
19	MUX_FW_AMUXBUS-B_VPLUS	Firmware control: 0=open, 1=close switch between amuxbusb and vplus signal. Write with '1' to set bit. Default Value: 0
18	MUX_FW_AMUX-BUSA_VPLUS	Firmware control: 0=open, 1=close switch between amuxbusa and vplus signal. Write with '1' to set bit. Default Value: 0
17	MUX_FW_TEMP_VPLUS	Firmware control: 0=open, 1=close switch between temperature sensor and vplus signal, also powers on the temperature sensor. Write with '1' to set bit. Default Value: 0
16	MUX_FW_VSSA_VMI-NUS	Firmware control: 0=open, 1=close switch between vssa_kelvin and vminus signal. Write with '1' to set bit. Default Value: 0
15	MUX_FW_P7_VMINUS	Firmware control: 0=open, 1=close switch between pin P7 and vminus signal. Write with '1' to set bit. Default Value: 0
14	MUX_FW_P6_VMINUS	Firmware control: 0=open, 1=close switch between pin P6 and vminus signal. Write with '1' to set bit. Default Value: 0
13	MUX_FW_P5_VMINUS	Firmware control: 0=open, 1=close switch between pin P5 and vminus signal. Write with '1' to set bit. Default Value: 0
12	MUX_FW_P4_VMINUS	Firmware control: 0=open, 1=close switch between pin P4 and vminus signal. Write with '1' to set bit. Default Value: 0
11	MUX_FW_P3_VMINUS	Firmware control: 0=open, 1=close switch between pin P3 and vminus signal. Write with '1' to set bit. Default Value: 0
10	MUX_FW_P2_VMINUS	Firmware control: 0=open, 1=close switch between pin P2 and vminus signal. Write with '1' to set bit. Default Value: 0

29.1.31 SAR_MUX_SWITCH0 (continued)

9	MUX_FW_P1_VMINUS	Firmware control: 0=open, 1=close switch between pin P1 and vminus signal. Write with '1' to set bit. Default Value: 0
8	MUX_FW_P0_VMINUS	Firmware control: 0=open, 1=close switch between pin P0 and vminus signal. Write with '1' to set bit. Default Value: 0
7	MUX_FW_P7_VPLUS	Firmware control: 0=open, 1=close switch between pin P7 and vplus signal. Write with '1' to set bit. Default Value: 0
6	MUX_FW_P6_VPLUS	Firmware control: 0=open, 1=close switch between pin P6 and vplus signal. Write with '1' to set bit. Default Value: 0
5	MUX_FW_P5_VPLUS	Firmware control: 0=open, 1=close switch between pin P5 and vplus signal. Write with '1' to set bit. Default Value: 0
4	MUX_FW_P4_VPLUS	Firmware control: 0=open, 1=close switch between pin P4 and vplus signal. Write with '1' to set bit. Default Value: 0
3	MUX_FW_P3_VPLUS	Firmware control: 0=open, 1=close switch between pin P3 and vplus signal. Write with '1' to set bit. Default Value: 0
2	MUX_FW_P2_VPLUS	Firmware control: 0=open, 1=close switch between pin P2 and vplus signal. Write with '1' to set bit. Default Value: 0
1	MUX_FW_P1_VPLUS	Firmware control: 0=open, 1=close switch between pin P1 and vplus signal. Write with '1' to set bit. Default Value: 0
0	MUX_FW_P0_VPLUS	Firmware control: 0=open, 1=close switch between pin P0 and vplus signal. Write with '1' to set bit. Default Value: 0

29.1.32 SAR_MUX_SWITCH_CLEAR0

SARMUX Firmware switch control clear

Address: 0x411D0304

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	A	A	A	A	A	A	A	A
Name	MUX_F-W_P7_VPLUS	MUX_F-W_P6_VPLUS	MUX_F-W_P5_VPLUS	MUX_F-W_P4_VPLUS	MUX_F-W_P3_VPLUS	MUX_F-W_P2_VPLUS	MUX_F-W_P1_VPLUS	MUX_F-W_P0_VPLUS

Bits	15	14	13	12	11	10	9	8
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	A	A	A	A	A	A	A	A
Name	MUX_F-W_P7_VMI-NUS	MUX_F-W_P6_VMI-NUS	MUX_F-W_P5_VMI-NUS	MUX_F-W_P4_VMI-NUS	MUX_F-W_P3_VMI-NUS	MUX_F-W_P2_VMI-NUS	MUX_F-W_P1_VMI-NUS	MUX_F-W_P0_VMI-NUS

Bits	23	22	21	20	19	18	17	16
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	A	A	A	A	A	A	A	A
Name	MUX_F-W_SAR-BUS1_VPLUS	MUX_F-W_SAR-BUS0_VPLUS	MUX_F-W_AMUX-BUSB_VMINUS	MUX_F-W_AMUX-BUSA_VMINUS	MUX_F-W_AMUX-BUSB_VPLUS	MUX_F-W_AMUX-BUSA_VPLUS	MUX_FW_-TEMP_VPLUS	MUX_F-W_VS-SA_VMINUS

Bits	31	30	29	28	27	26	25	24
SW Access	None		RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	None		A	A	A	A	A	A
Name	None [31:30]		MUX_F-W_P7_COREIO3	MUX_F-W_P6_COREIO2	MUX_F-W_P5_COREIO1	MUX_F-W_P4_COREIO0	MUX_F-W_SAR-BUS1_VMINUS	MUX_F-W_SAR-BUS0_VMINUS

Bits	Name	Description
29	MUX_FW_P7_COREIO3	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
28	MUX_FW_P6_COREIO2	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
27	MUX_FW_P5_COREIO1	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
26	MUX_FW_P4_COREIO0	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0

29.1.32 SAR_MUX_SWITCH_CLEAR0 (continued)

25	MUX_FW_SAR-BUS1_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
24	MUX_FW_SAR-BUS0_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
23	MUX_FW_SAR-BUS1_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
22	MUX_FW_SAR-BUS0_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
21	MUX_FW_AMUXBUS-B_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
20	MUX_FW_AMUX-BUSA_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
19	MUX_FW_AMUXBUS-B_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
18	MUX_FW_AMUX-BUSA_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
17	MUX_FW_TEMP_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
16	MUX_FW_VSSA_VMI-NUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
15	MUX_FW_P7_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
14	MUX_FW_P6_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
13	MUX_FW_P5_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
12	MUX_FW_P4_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
11	MUX_FW_P3_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
10	MUX_FW_P2_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
9	MUX_FW_P1_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
8	MUX_FW_P0_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
7	MUX_FW_P7_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
6	MUX_FW_P6_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
5	MUX_FW_P5_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
4	MUX_FW_P4_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0

3	MUX_FW_P3_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
2	MUX_FW_P2_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
1	MUX_FW_P1_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
0	MUX_FW_P0_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0

29.1.33 SAR_MUX_SWITCH_DS_CTRL

SARMUX switch DSI control

Address: 0x411D0340

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	MUX-_DS_C-TRL_P7	MUX-_DS_C-TRL_P6	MUX-_DS_C-TRL_P5	MUX-_DS_C-TRL_P4	MUX-_DS_C-TRL_P3	MUX-_DS_C-TRL_P2	MUX-_DS_C-TRL_P1	MUX-_DS_C-TRL_P0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	None		RW	RW	RW	RW
HW Access	R	R	None		R	R	R	R
Name	MUX-_DS_C-TRL_SARBUS1	MUX-_DS_C-TRL_SARBUS0	None [21:20]		MUX-_DS_C-TRL_AMUXBUSB	MUX-_DS_C-TRL_AMUXBUSA	MUX-_DS_C-TRL_TEMP	MUX-_DS_C-TRL_VSSA

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23	MUX_DS_CTRL_SAR-BUS1	for sarbus1 switch Default Value: 0
22	MUX_DS_CTRL_SAR-BUS0	for sarbus0 switch Default Value: 0
19	MUX_DS_CTRL_AMUX-BUSB	for amuxbusb switches Default Value: 0
18	MUX_DS_CTRL_AMUX-BUSA	for amuxbusa switch Default Value: 0
17	MUX_DS_CTRL_TEMP	for temp switch Default Value: 0

29.1.33 SAR_MUX_SWITCH_DS_CTRL (continued)

16	MUX_DS_CTRL_VSSA	for vssa switch Default Value: 0
7	MUX_DS_CTRL_P7	for P7 switches Default Value: 0
6	MUX_DS_CTRL_P6	for P6 switches Default Value: 0
5	MUX_DS_CTRL_P5	for P5 switches Default Value: 0
4	MUX_DS_CTRL_P4	for P4 switches Default Value: 0
3	MUX_DS_CTRL_P3	for P3 switches Default Value: 0
2	MUX_DS_CTRL_P2	for P2 switches Default Value: 0
1	MUX_DS_CTRL_P1	for P1 switches Default Value: 0
0	MUX_DS_CTRL_P0	for P0 switches Default Value: 0

29.1.34 SAR_MUX_SWITCH_SQ_CTRL

SARMUX switch Sar Sequencer control

Address: 0x411D0344

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	MUX-_SQ_C-TRL_P7	MUX-_SQ_C-TRL_P6	MUX-_SQ_C-TRL_P5	MUX-_SQ_C-TRL_P4	MUX-_SQ_C-TRL_P3	MUX-_SQ_C-TRL_P2	MUX-_SQ_C-TRL_P1	MUX-_SQ_C-TRL_P0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	None		RW	RW	RW	RW
HW Access	R	R	None		R	R	R	R
Name	MUX-_SQ_C-TRL_SARBUS1	MUX-_SQ_C-TRL_SARBUS0	None [21:20]		MUX-_SQ_C-TRL_AMUXBUSB	MUX-_SQ_C-TRL_AMUXBUSA	MUX-_SQ_C-TRL_TEMP	MUX-_SQ_C-TRL_VSSA

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23	MUX_SQ_CTRL_SAR-BUS1	for sarbus1 switch Default Value: 0
22	MUX_SQ_CTRL_SAR-BUS0	for sarbus0 switch Default Value: 0
19	MUX_SQ_CTRL_AMUX-BUSB	for amuxbusb switches Default Value: 0
18	MUX_SQ_CTRL_AMUX-BUSA	for amuxbusa switch Default Value: 0
17	MUX_SQ_CTRL_TEMP	for temp switch Default Value: 0
16	MUX_SQ_CTRL_VSSA	for vssa switch Default Value: 0

29.1.34 SAR_MUX_SWITCH_SQ_CTRL (continued)

7	MUX_SQ_CTRL_P7	for P7 switches Default Value: 0
6	MUX_SQ_CTRL_P6	for P6 switches Default Value: 0
5	MUX_SQ_CTRL_P5	for P5 switches Default Value: 0
4	MUX_SQ_CTRL_P4	for P4 switches Default Value: 0
3	MUX_SQ_CTRL_P3	for P3 switches Default Value: 0
2	MUX_SQ_CTRL_P2	for P2 switches Default Value: 0
1	MUX_SQ_CTRL_P1	for P1 switches Default Value: 0
0	MUX_SQ_CTRL_P0	for P0 switches Default Value: 0

29.1.35 SAR_MUX_SWITCH_STATUS

SARMUX switch status

Address: 0x411D0348

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	MUX_F-W_P7_VPLUS	MUX_F-W_P6_VPLUS	MUX_F-W_P5_VPLUS	MUX_F-W_P4_VPLUS	MUX_F-W_P3_VPLUS	MUX_F-W_P2_VPLUS	MUX_F-W_P1_VPLUS	MUX_F-W_P0_VPLUS

Bits	15	14	13	12	11	10	9	8
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	MUX_F-W_P7_VMI-NUS	MUX_F-W_P6_VMI-NUS	MUX_F-W_P5_VMI-NUS	MUX_F-W_P4_VMI-NUS	MUX_F-W_P3_VMI-NUS	MUX_F-W_P2_VMI-NUS	MUX_F-W_P1_VMI-NUS	MUX_F-W_P0_VMI-NUS

Bits	23	22	21	20	19	18	17	16
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	MUX_F-W_SAR-BUS1_VPLUS	MUX_F-W_SAR-BUS0_VPLUS	MUX_F-W_AMUX-BUSB_VMINUS	MUX_F-W_AMUX-BUSA_VMINUS	MUX_F-W_AMUX-BUSB_VPLUS	MUX_F-W_AMUX-BUSA_VPLUS	MUX_FW_-TEMP_VPLUS	MUX_F-W_VS-SA_VMINUS

Bits	31	30	29	28	27	26	25	24
SW Access	None						R	R
HW Access	None						W	W
Name	None [31:26]						MUX_F-W_SAR-BUS1_VMINUS	MUX_F-W_SAR-BUS0_VMINUS

Bits	Name	Description
25	MUX_FW_SAR-BUS1_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
24	MUX_FW_SAR-BUS0_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
23	MUX_FW_SAR-BUS1_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
22	MUX_FW_SAR-BUS0_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0

29.1.35 SAR_MUX_SWITCH_STATUS (continued)

21	MUX_FW_AMUXBUS-B_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
20	MUX_FW_AMUX-BUSA_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
19	MUX_FW_AMUXBUS-B_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
18	MUX_FW_AMUX-BUSA_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
17	MUX_FW_TEMP_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
16	MUX_FW_VSSA_VMI-NUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
15	MUX_FW_P7_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
14	MUX_FW_P6_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
13	MUX_FW_P5_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
12	MUX_FW_P4_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
11	MUX_FW_P3_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
10	MUX_FW_P2_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
9	MUX_FW_P1_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
8	MUX_FW_P0_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
7	MUX_FW_P7_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
6	MUX_FW_P6_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
5	MUX_FW_P5_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
4	MUX_FW_P4_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
3	MUX_FW_P3_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
2	MUX_FW_P2_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
1	MUX_FW_P1_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
0	MUX_FW_P0_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0

Section I: Peripheral Group 10

This section encompasses the following chapters:

30 Pulse Density Modulation (PDM) Registers

This section discusses the Pulse Density Modulation (PDM) block registers. It lists all the registers in mapping tables, in address order.

30.1 Register Details

Register	Address	Description
PDM0_CTL	0x42A20000	Control
PDM0_CLOCK_CTL	0x42A20010	Clock control
PDM0_MODE_CTL	0x42A20014	Mode control
PDM0_DATA_CTL	0x42A20018	Data control
PDM0_CMD	0x42A20020	Command
PDM0_TR_CTL	0x42A20040	Trigger control
PDM0_RX_FIFO_CTL	0x42A20300	RX FIFO control
PDM0_RX_FIFO_STATUS	0x42A20304	RX FIFO status
PDM0_RX_FIFO_RD	0x42A20308	RX FIFO read
PDM0_RX_FIFO_RD_SILENT	0x42A2030C	RX FIFO silent read
PDM0_INTR	0x42A20F00	Interrupt register
PDM0_INTR_SET	0x42A20F04	Interrupt set register
PDM0_INTR_MASK	0x42A20F08	Interrupt mask register
PDM0_INTR_MASKED	0x42A20F0C	Interrupt masked register

30.1.1 PDM0_CTL

Control

Address: 0x42A20000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				PGA_R [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				PGA_L [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [23:18]						STEP_SEL	SOFT-_MUTE

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	ENABLED	None [30:24]						

Bits	Name	Description
31	ENABLED	Enables the PDM component: '0': Disabled. '1': Enabled. Default Value: 0
17	STEP_SEL	Set fine gain step for smooth PGA or Soft-Mute attenuation transition. '0': 0.13dB '1': 0.26dB (Note: This bit is connected to AR36U12.PDM_CORE2_CFG.SEL_STEP) Default Value: 1
16	SOFT_MUTE	Soft mute function to mute the volume smoothly '0': Disabled. '1': Enabled. (Note: This bit is connected to AR36U12.PDM_CORE_CFG.SOFT_MUTE) Default Value: 0

30.1.1 PDM0_CTL (continued)

11 : 8	PGA_L	Left channel PGA gain: +1.5dB/step, -12dB ~ +10.5dB "0": -12 dB "1": -10.5 dB "15": +10.5 dB (Note: These bits are connected to AR36U12.PDM_CORE_CFG.PGA_L) Default Value: 8
3 : 0	PGA_R	Right channel PGA gain: +1.5dB/step, -12dB ~ +10.5dB "0": -12 dB "1": -10.5 dB "15" +10.5 dB (Note: These bits are connected to AR36U12.PDM_CORE_CFG.PGA_R) Default Value: 8

30.1.2 PDM0_CLOCK_CTL

Clock control

Address: 0x42A20010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW		None		RW	
HW Access	None		R		None		R	
Name	None [7:6]		MCLKQ_CLOCK_DIV [5:4]		None [3:2]		CLK_CLOCK_DIV [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				CKO_CLOCK_DIV [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None	RW						
HW Access	None	R						
Name	None	SINC_RATE [22:16]						

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
22 : 16	SINC_RATE	SINC Decimation Rate. For details, see the data sheet provided by Archband. Oversampling Ratio = Decimation Rate = 2 X SINC_RATE (Note: These bits are connected to AR36U12.PDM_CORE_CFG.SINC_RATE) Default Value: 32
11 : 8	CKO_CLOCK_DIV	PDM CKO (FPDM_CKO) clock divider (3rd divider): FPDM_CKO = MCLKQ / (CKO_CLOCK_DIV + 1) Note: To configure "0" to this field is prohibited. (Note: PDM_CKO is configured by MCLKQ_CLOCK_DIV, CLK_CLOCK_DIV and CKO_-CLOCK_DIV.) (Note: These bits are connected to AR36U12.PDM_CORE_CFG.MCLKDIV) Default Value: 3
5 : 4	MCLKQ_CLOCK_DIV	MCLKQ divider (2nd divider) (Note: These bits are connected to AR36U12.PDM_CORE2_CFG.DIV_MCLKQ) Default Value: 1 **0x0: DIVBY1 :** Divide by 1

30.1.2 PDM0_CLOCK_CTL (continued)

		0x1: DIVBY2 : Divide by 2 (no 50% duty cycle)
		0x2: DIVBY3 : Divide by 3 (no 50% duty cycle)
		0x3: DIVBY4 : Divide by 4 (no 50% duty cycle)
1 : 0	CLK_CLOCK_DIV	PDM CLK (FPDM_CLK) (1st divider): This configures a frequency of PDM CLK. The configured frequency is used to operate PDM core. I.e. the frequency is input to MCLKQ_CLOCK_DIV register. Note: configure a frequency of PDM CLK as lower than or equal 50MHz with this divider. Default Value: 0
		0x0: DIVBY1 : Divide by 1
		0x1: DIVBY2 : Divide by 2 (no 50% duty cycle)
		0x2: DIVBY3 : Divide by 3 (no 50% duty cycle)
		0x3: DIVBY4 : Divide by 4 (no 50% duty cycle)

30.1.3 PDM0_MODE_CTL

Mode control

Address: 0x42A20014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW	RW	
HW Access	None					R	R	
Name	None [7:3]					SWAP_LR	PCM_CH_SET [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW		
HW Access	None					R		
Name	None [15:11]					S_CYCLES [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	None					RW		
HW Access	None					R		
Name	None [23:19]					CKO_DELAY [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	None			RW	RW			
HW Access	None			R	R			
Name	None [31:29]			HPF_EN_N	HPF_GAIN [27:24]			

Bits	Name	Description
28	HPF_EN_N	Enable high pass filter (active low) '1': Disabled. '0': Enabled. (Note: This bit is connected to AR36U12.PDM_CORE_CFG.ADCHPD) Default Value: 1
27 : 24	HPF_GAIN	Adjust high pass filter coefficients. H(Z) = (1 Z-1) / [1 (1- 2 HPF_GAIN) Z-1] (Note: These bits are connected to AR36U12.PDM_CORE_CFG.HPGAIN) Default Value: 11
18 : 16	CKO_DELAY	Phase difference from the rising edge of internal sampler clock (CLK_IS) to that of PDM_CKO clock: (Note: These bits are connected to AR36U12.PDM_CORE2_CFG.PDMCKO_DLY) Default Value: 0 **0x0: ADV3 :** CLK_IS is 3*PDM_CLK period early **0x1: ADV2 :** CLK_IS is 2*PDM_CLK period early

30.1.3 PDM0_MODE_CTL (continued)

		0x2: ADV1 : CLK_IS is 1*PDM_CLK period early
		0x3: NO_DELAY : CLK_IS is the same as PDM_CKO
		0x4: DLY1 : CLK_IS is 1*PDM_CLK period late
		0x5: DLY2 : CLK_IS is 2*PDM_CLK period late
		0x6: DLY3 : CLK_IS is 3*PDM_CLK period late
		0x7: DLY4 : CLK_IS is 4*PDM_CLK period late
10 : 8	S_CYCLES	Set time step for gain change during PGA or soft mute operation in number of 1/a sampling rate. (Note: These bits are connected to AR36U12.PDM_CORE_CFG.S_CYCLES) Default Value: 1
		0x0: STEP_NUM64 : 64steps
		0x1: STEP_NUM96 : 96steps
		0x2: STEP_NUM128 : 128steps
		0x3: STEP_NUM160 : 160steps
		0x4: STEP_NUM192 : 192steps
		0x5: STEP_NUM256 : 256steps
		0x6: STEP_NUM384 : 384steps
		0x7: STEP_NUM512 : 512steps
2	SWAP_LR	Input data L/R channel swap: '1': Right/Left channel recording swap '0': No Swap (Note: This bit is connected to AR36U12.PDM_CORE_CFG.LRSWAP) Default Value: 0
1 : 0	PCM_CH_SET	Specifies PCM output channels as mono or stereo: (Note: These bits are connected to AR36U12.PDM_CORE2_CFG.PCM_CHSET) Default Value: 3
		0x0: DISABLED : Channel disabled
		0x1: MONO_L : Mono left channel enable
		0x2: MONO_R : Mono right channel enable

30.1.3 PDM0_MODE_CTL (continued)

0x3: STEREO :
Stereo channel enable

30.1.4 PDM0_DATA_CTL

Data control

Address: 0x42A20018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	
HW Access	None						R	
Name	None [7:2]						WORD_LEN [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							BIT_EX-TENSION

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	BIT_EXTENSION	When reception word length is shorter than the word length of RX_FIFO_RD, extension mode of upper bit should be set. '0': Extended by '0' '1': Extended by sign bit (if MSB word is "1", then it is extended by "1", if MSB is "0" then it is extended by "0") Default Value: 0
1 : 0	WORD_LEN	PCM Word Length in number of bits: (Note: These bits are connected to AR36U12.PDM_CORE2_CFG.PCM_IWL) Default Value: 0 **0x0: BIT_LEN16 :** 16-bit **0x1: BIT_LEN18 :** 18-bit **0x2: BIT_LEN20 :** 20-bit **0x3: BIT_LEN24 :** 24-bit

30.1.5 PDM0_CMD

Command

Address: 0x42A20020

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							STREAM_EN

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	STREAM_EN	Enable data streaming flow: '0': Disabled. '1': Enabled. (Note: This bit is connected to AR36U12.PDM_CORE_CFG.PDMA_EN) Default Value: 0

30.1.6 PDM0_TR_CTL

Trigger control

Address: 0x42A20040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							RX-_REQ_EN

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
16	RX_REQ_EN	Trigger output ("tr_pdm_rx_req") enable for requests of DMA transfer '0': Disabled. '1': Enabled. Default Value: 0

30.1.7 PDM0_RX_FIFO_CTL

RX FIFO control

Address: 0x42A20300

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	TRIGGER_LEVEL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [23:18]						FREEZE	CLEAR

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
17	FREEZE	When '1', hardware writes to the RX FIFO have no effect. Freeze will not advance the RX FIFO write pointer.This field is used only for debugging purposes. Default Value: 0
16	CLEAR	When '1', the RX FIFO and RX_BUF are cleared/invalidated. Invalidation will last for as long as this field is '1'. If a quick clear/invalidation is required, the field should be set to '1' and be followed by a set to '0'. If a clear/invalidation is required for an extended time period, the field should be set to '1' during the complete time period. Default Value: 0
7 : 0	TRIGGER_LEVEL	Trigger level. When the RX FIFO has more entries than the number of this field, a receiver trigger event is generated. Note: software can configure up to 254 in Mono channel enabled (MODE_CTL.PCM_CH_SET = "1" or "2"), up to 253 in Stereo channel enabled (MODE_CTL.PCM_CH_SET = "3"). Default Value: 0

30.1.8 PDM0_RX_FIFO_STATUS

RX FIFO status

Address: 0x42A20304

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	USED [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	RD_PTR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	WR_PTR [31:24]							

Bits	Name	Description
31 : 24	WR_PTR	RX FIFO write pointer: RX FIFO location at which a new data frame is written by the hardware.This field is used only for debugging purposes. Default Value: 0
23 : 16	RD_PTR	RX FIFO read pointer: RX FIFO location from which a data frame is read by the host.This field is used only for debugging purposes. Default Value: 0
7 : 0	USED	Number of entries in the RX FIFO. The field value is in the range [0, 255]. When this is zero, the RX FIFO is empty. Default Value: 0

30.1.9 PDM0_RX_FIFO_RD

RX FIFO read

Address: 0x42A20308

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data read from the RX FIFO. Reading a data frame will remove the data frame from the FIFO; i.e. behavior is similar to that of a POP operation. Note: Don't access to this bit while RX_FIFO_CTL.CLEAR is '1'. Default Value: 0

30.1.10 PDM0_RX_FIFO_RD_SILENT

RX FIFO silent read

Address: 0x42A2030C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data read from the RX FIFO. Reading a data frame will NOT remove the data frame from the RX FIFO; i.e. behavior is similar to that of a PEEK operation. This field is used only for debugging purposes. Note: Don't access to this bit while RX_FIFO_CTL.CLEAR is '1'. Default Value: 0

30.1.11 PDM0_INTR

Interrupt register

Address: 0x42A20F00

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None	RW1C	RW1C	None		RW1C	None	RW1C
HW Access	None	RW1S	RW1S	None		RW1S	None	RW1S
Name	None	RX_UN-DERFLOW	RX_OVER-FLOW	None [20:19]		RX-_NOT_EMPTY	None	RX_TRIG-GER

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
22	RX_UNDERFLOW	Attempt to read from an empty RX FIFO Default Value: 0
21	RX_OVERFLOW	Attempt to write to a full RX FIFO Default Value: 0
18	RX_NOT_EMPTY	RX FIFO is not empty. Default Value: 0
16	RX_TRIGGER	More entries in the RX FIFO than the value specified by TRIGGER_LEVEL in RX_FIFO_CTL. Default Value: 0

30.1.12 PDM0_INTR_SET

Interrupt set register

Address: 0x42A20F04

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None	RW1S	RW1S	None		RW1S	None	RW1S
HW Access	None	A	A	None		A	None	A
Name	None	RX_UN-DERFLOW	RX_OVER-FLOW	None [20:19]		RX-_NOT_EMPTY	None	RX_TRIG-GER

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
22	RX_UNDERFLOW	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
21	RX_OVERFLOW	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
18	RX_NOT_EMPTY	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
16	RX_TRIGGER	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

30.1.13 PDM0_INTR_MASK

Interrupt mask register

Address: 0x42A20F08

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None	RW	RW	None		RW	None	RW
HW Access	None	R	R	None		R	None	R
Name	None	RX_UN-DERFLOW	RX_OVER-FLOW	None [20:19]		RX-_NOT_EMPTY	None	RX_TRIG-GER

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
22	RX_UNDERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
21	RX_OVERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
18	RX_NOT_EMPTY	Mask bit for corresponding bit in interrupt request register. Default Value: 0
16	RX_TRIGGER	Mask bit for corresponding bit in interrupt request register. Default Value: 0

30.1.14 PDM0_INTR_MASKED

Interrupt masked register

Address: 0x42A20F0C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None	R	R	None		R	None	R
HW Access	None	W	W	None		W	None	W
Name	None	RX_UN-DERFLOW	RX_OVER-FLOW	None [20:19]		RX-_NOT_EMPTY	None	RX_TRIG-GER

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
22	RX_UNDERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
21	RX_OVERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
18	RX_NOT_EMPTY	Logical and of corresponding request and mask bits. Default Value: 0
16	RX_TRIGGER	Logical and of corresponding request and mask bits. Default Value: 0

31 Inter IC Sound (I2S) Registers

This section discusses the Inter IC Sound (I2S) registers. It lists all the registers in mapping tables, in address order.

31.1 Register Details

Register	Address	Description
I2S0_CTL	0x42A10000	Control
I2S0_CLOCK_CTL	0x42A10010	Clock control
I2S0_CMD	0x42A10020	Command
I2S0_TR_CTL	0x42A10040	Trigger control
I2S0_TX_CTL	0x42A10080	Transmitter control
I2S0_TX_WATCHDOG	0x42A10084	Transmitter watchdog
I2S0_RX_CTL	0x42A100A0	Receiver control
I2S0_RX_WATCHDOG	0x42A100A4	Receiver watchdog
I2S0_TX_FIFO_CTL	0x42A10200	TX FIFO control
I2S0_TX_FIFO_STATUS	0x42A10204	TX FIFO status
I2S0_TX_FIFO_WR	0x42A10208	TX FIFO write
I2S0_RX_FIFO_CTL	0x42A10300	RX FIFO control
I2S0_RX_FIFO_STATUS	0x42A10304	RX FIFO status
I2S0_RX_FIFO_RD	0x42A10308	RX FIFO read
I2S0_RX_FIFO_RD_SILENT	0x42A1030C	RX FIFO silent read
I2S0_INTR	0x42A10F00	Interrupt register
I2S0_INTR_SET	0x42A10F04	Interrupt set register
I2S0_INTR_MASK	0x42A10F08	Interrupt mask register
I2S0_INTR_MASKED	0x42A10F0C	Interrupt masked register

31.1.1 I2S0_CTL

Control

Address: 0x42A10000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None					
HW Access	R	R	None					
Name	RX_EN-ABLED	TX_EN-ABLED	None					

Bits	Name	Description
31	RX_ENABLED	Enables the I2S RX component: '0': Disabled. '1': Enabled. Default Value: 0
30	TX_ENABLED	Enables the I2S TX component: '0': Disabled. '1': Enabled. Default Value: 0

31.1.2 I2S0_CLOCK_CTL

Clock control

Address: 0x42A10010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		CLOCK_DIV [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							CLOCK_-SEL

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	CLOCK_SEL	Selects clock to be used by I2S: '0': Internal clock ("clk_audio_i2s") '1': External clock ("clk_i2s_if") Default Value: 0
5 : 0	CLOCK_DIV	Frequency divisor for generating I2S clock frequency. The selected clock with CLOCK_SEL is divided by this. "0": Bypass "1": 2 x "2": 3 x "3": 4 x ... "62": 63 x "63": 64 x Default Value: 0

31.1.3 I2S0_CMD

Command

Address: 0x42A10020

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							TX_START

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							TX_PAUSE

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							RX_START

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
16	RX_START	Receiver enable: '0': Disabled. '1': Enabled. Default Value: 0
8	TX_PAUSE	Pause enable: '0': Disabled (TX FIFO data is sent over I2S). '1': Enabled ("0" data is sent over I2S, instead of TX FIFO data). Default Value: 0
0	TX_START	Transmitter enable: '0': Disabled. '1': Enabled. Default Value: 0

31.1.4 I2S0_TR_CTL

Trigger control

Address: 0x42A10040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							TX-_REQ_EN

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							RX-_REQ_EN

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
16	RX_REQ_EN	Trigger output ("tr_i2s_rx_req") enable for requests of DMA transfer in reception '0': Disabled. '1': Enabled. Default Value: 0
0	TX_REQ_EN	Trigger output ("tr_i2s_tx_req") enable for requests of DMA transfer in transmission '0': Disabled. '1': Enabled. Default Value: 0

31.1.5 I2S0_TX_CTL

Transmitter control

Address: 0x42A10080

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW			RW	None		
HW Access	R	R			R	None		
Name	MS	CH_NR [6:4]			B_-CLOCK_-INV	None		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW	RW	None	RW	RW	
HW Access	None		R	R	None	R	R	
Name	None [15:14]		WD_EN	OVHDATA	None	WS_PULSE	I2S_MODE [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	WORD_LEN [22:20]			None	CH_LEN [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [31:26]						SCKI_POL	SCKO_POL

Bits	Name	Description
25	SCKI_POL	TX slave bit clock polarity. When this bit is 1, the incoming tx_sck signal is inverted before it is received by the I2S transceiver core. This bit does not affect the internal serial data transmission timing. The word sync (TX_WS) signal is not affected by this bit setting. See TX_CTL.B_CLOCK_INV for more details. Default Value: 0
24	SCKO_POL	TX master bit clock polarity. When this bit is 1, the outgoing tx_sck signal is inverted after it has been transmitted from the I2S transceiver core. This bit does not affect the internal serial data transmission timing. The word sync (TX_WS) signal is not affected by this bit setting. '0': When transmitter is in master mode, serial data is transmitted from the falling bit clock edge '1': When transmitter is in master mode, serial data is transmitted from the rising bit clock edge Default Value: 0

31.1.5 I2S0_TX_CTL (continued)

22 : 20	WORD_LEN	Word length in number of bits: Note: - When this field is configured to "6" or "7", the length is set to 32-bit (same as "5"). - Don't configure this field as beyond Channel length. (Note: These bits are connected to AR38U12.TX_CFG.TX_IWL) Default Value: 4 **0x0: BIT_LEN8 :** 8-bit **0x1: BIT_LEN16 :** 16-bit **0x2: BIT_LEN18 :** 18-bit **0x3: BIT_LEN20 :** 20-bit **0x4: BIT_LEN24 :** 24-bit **0x5: BIT_LEN32 :** 32-bit
18 : 16	CH_LEN	Channel length in number of bits: Note: - When this field is configured to "6" or "7", the length is set to 32-bit (same as "5"). - When TDM mode, must be 32-bit length to this field. (Note: These bits are connected to AR38U12.TX_CFG.TX_CHLEN) Default Value: 4 **0x0: BIT_LEN8 :** 8-bit **0x1: BIT_LEN16 :** 16-bit **0x2: BIT_LEN18 :** 18-bit **0x3: BIT_LEN20 :** 20-bit **0x4: BIT_LEN24 :** 24-bit **0x5: BIT_LEN32 :** 32-bit
13	WD_EN	Set watchdog for "tx_ws_in": '0': Disabled. '1': Enabled. Default Value: 0
12	OVHDATA	Set overhead value: '0': Set to '0' '1': Set to '1' (Note: This bit is connected to AR38U12.TX_CFG.TX_OVHDATA) Default Value: 0

31.1.5 I2S0_TX_CTL (continued)

10	WS_PULSE	Set WS pulse width in TDM mode: (Note: This bit is connected to AR38U12.TX_CFG.TX_WS_PULSE) Note: When not TDM mode, must be "1". Default Value: 1 **0x0: SCK_PERIOD :** Pulse width is 1 SCK period **0x1: CH_LENGTH :** Pulse width is 1 channel length
9 : 8	I2S_MODE	Select I2S, left-justified or TDM: (Note: These bits are connected to AR38U12.TX_CFG.TX_I2S_MODE) Default Value: 1 **0x0: LEFT_JUSTIFIED :** Left Justified **0x1: I2S :** I2S mode **0x2: TDM_A :** TDM mode A, the 1st Channel align to WSO Rising Edge **0x3: TDM_B :** TDM mode B, the 1st Channel align to WSO Rising edge with1 SCK Delay
7	MS	Set interface in master or slave mode: (Note: This bit is connected to AR38U12.TX_CFG.TX_MS) Default Value: 0 **0x0: SLAVE :** Slave **0x1: MASTER :** Master
6 : 4	CH_NR	Specifies number of channels per frame: Note: only "2channels" is supported during Left Justfied or I2S mode. Hence software must set "1" to this field in the modes. (Note: These bits are connected to AR38U12.TX_CFG.TX_CHSET) Default Value: 1 **0x0: CH_NUM1 :** 1 channel **0x1: CH_NUM2 :** 2 channels **0x2: CH_NUM3 :** 3 channels **0x3: CH_NUM4 :** 4 channels **0x4: CH_NUM5 :** 5 channels **0x5: CH_NUM6 :** 6 channels **0x6: CH_NUM7 :** 7 channels **0x7: CH_NUM8 :** 8 channels

31.1.5 I2S0_TX_CTL (continued)

3	B_CLOCK_INV	Serial data transmission is advanced by 0.5 SCK cycles. This bit is valid only in TX slave mode. When set to "1", the serial data will be transmitted 0.5 SCK cycles earlier than when set to "0". 1) TX_CTL.SCKI_POL=0 and TX_CTL.B_CLOCK_INV=0: Serial data will be transmitted off the SCK falling edge 2) TX_CTL.SCKI_POL=0 and TX_CTL.B_CLOCK_INV=1: Serial data will be transmitted off the SCK rising edge that is 0.5 SCK cycles before the SCK falling edge in 1) 3) TX_CTL.SCKI_POL=1 and TX_CTL.B_CLOCK_INV=0: Serial data will be transmitted off the SCK rising edge 4) TX_CTL.SCKI_POL=1 and TX_CTL.B_CLOCK_INV=1: Serial data will be transmitted off the SCK falling edge that is 0.5 SCK cycles before the SCK rising edge in 3) (Note that this is only the appearance w.r.t. SCK edge, the actual timing is generated by an internal clock that runs 8x the SCK frequency). The word sync (TX_WS) signal is not affected by this bit setting. Note: When Master mode, must be "0". (Note: This bit is connected to AR38U12.TX_CFG.TX_BCLKINV) Default Value: 0 **0x0: FALLING_EDGE_TX :** SDO transmitted at SCK falling edge when TX_CTL.SCKI_POL=0 **0x1: RISING_EDGE_TX :** SDO transmitted at SCK rising edge when TX_CTL.SCKI_POL=0

31.1.6 I2S0_TX_WATCHDOG

Transmitter watchdog

Address: 0x42A10084

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	WD_COUNTER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	WD_COUNTER [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	WD_COUNTER [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	WD_COUNTER [31:24]							

Bits	Name	Description
31 : 0	WD_COUNTER	Start value of the TX watchdog. With the reset value of 0x0000:0000 the counter is disabled. This is clocked by the AHB-Lite system clock "clk_sys". Default Value: 0

31.1.7 I2S0_RX_CTL

Receiver control

Address: 0x42A100A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW			RW	None		
HW Access	R	R			R	None		
Name	MS	CH_NR [6:4]			B_-CLOCK_-INV	None		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW	None		RW	RW	
HW Access	None		R	None		R	R	
Name	None [15:14]		WD_EN	None [12:11]		WS_PULSE	I2S_MODE [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW			None	RW		
HW Access	R	R			None	R		
Name	BIT_EX-TENSION	WORD_LEN [22:20]			None	CH_LEN [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [31:26]						SCKI_POL	SCKO_POL

Bits	Name	Description
25	SCKI_POL	RX slave bit clock polarity. When this bit is 1, the incoming rx_sck signal is inverted before it is received by the I2S receiver core. This bit does not affect the internal serial data capture timing. The word sync (RX_WS) signal is not affected by this bit setting. '0': When receiver is in slave mode, serial data is sampled on the rising bit clock edge '1': When receiver is in slave mode, serial data is sampled on the falling bit clock edge Default Value: 0
24	SCKO_POL	RX master bit clock polarity. When this bit is 1, the outgoing rx_sck signal is inverted after it has been transmitted from the I2S receiver core. This bit does not affect the internal serial data capture timing. The word sync (RX_WS) signal is not affected by this bit setting.See RX_CTL.B_CLOCK_INV for more details. Default Value: 0

31.1.7 I2S0_RX_CTL (continued)

23	BIT_EXTENSION	When reception word length is shorter than the word length of RX_FIFO_RD, extension mode of upper bit should be set. '0': Extended by "0" '1': Extended by sign bit (if MSB word is '1', then it is extended by '1', if MSB is '0' then it is extended by '0') Default Value: 0
22 : 20	WORD_LEN	Word length in number of bits: Note: - When this field is configured to "6" or "7", the length is set to 32-bit (same as "5"). - Don't configure this field as beyond Channel length. (Note: These bits are connected to AR38U12.RX_CFG.RX_IWL) Default Value: 4 **0x0: BIT_LEN8 :** 8-bit **0x1: BIT_LEN16 :** 16-bit **0x2: BIT_LEN18 :** 18-bit **0x3: BIT_LEN20 :** 20-bit **0x4: BIT_LEN24 :** 24-bit **0x5: BIT_LEN32 :** 32-bit
18 : 16	CH_LEN	Channel length in number of bits: Note: - When this field is configured to "6" or "7", the length is set to 32-bit (same as "5"). - When TDM mode, must be 32-bit length to this field. (Note: These bits are connected to AR38U12.RX_CFG.RX_CHLEN) Default Value: 4 **0x0: BIT_LEN8 :** 8-bit **0x1: BIT_LEN16 :** 16-bit **0x2: BIT_LEN18 :** 18-bit **0x3: BIT_LEN20 :** 20-bit **0x4: BIT_LEN24 :** 24-bit **0x5: BIT_LEN32 :** 32-bit
13	WD_EN	Set watchdog for "rx_ws_in" '0': Disabled. '1': Enabled. Default Value: 0

31.1.7 I2S0_RX_CTL (continued)

10	WS_PULSE	Set WS pulse width in TDM mode: (Note: This bit is connected to AR38U12.RX_CFG.RX_WS_PULSE) Note: When not TDM mode, must be "1". Default Value: 1 **0x0: SCK_PERIOD :** Pulse width is 1 SCK period **0x1: CH_LENGTH :** Pulse width is 1 channel length
9 : 8	I2S_MODE	Select I2S, left-justified or TDM: (Note: These bits are connected to AR38U12.RX_CFG.RX_I2S_MODE) Default Value: 1 **0x0: LEFT_JUSTIFIED :** Left Justified **0x1: I2S :** I2S mode **0x2: TDM_A :** TDM mode A, the 1st Channel align to WSO Rising Edge **0x3: TDM_B :** TDM mode B, the 1st Channel align to WSO Rising edge with1 SCK Delay
7	MS	Set interface in master or slave mode: (Note: This bit is connected to AR38U12.TX_CFG.RX_MS) Default Value: 0 **0x0: SLAVE :** Slave **0x1: MASTER :** Master
6 : 4	CH_NR	Specifies number of channels per frame: Note: only "2channels" is supported during Left Justfied or I2S mode. Hence software must set "1" to this field in the modes. (Note: These bits are connected to AR38U12.RX_CFG.RX_CHSET) Default Value: 1 **0x0: CH_NUM1 :** 1 channel **0x1: CH_NUM2 :** 2 channels **0x2: CH_NUM3 :** 3 channels **0x3: CH_NUM4 :** 4 channels **0x4: CH_NUM5 :** 5 channels **0x5: CH_NUM6 :** 6 channels **0x6: CH_NUM7 :** 7 channels

31.1.7 I2S0_RX_CTL (continued)

		0x7: CH_NUM8 : 8 channels
3	B_CLOCK_INV	Serial data capture is delayed by 0.5 SCK cycles. This bit is valid only in RX master mode. When set to "1", the serial data will be captured 0.5 SCK cycles later than when set to "0". 1) RX_CTL.SCKO_POL=0 and RX_CTL.B_CLOCK_INV=0: Serial data will be captured by the SCK rising edge 2) RX_CTL.SCKO_POL=0 and RX_CTL.B_CLOCK_INV=1: Serial data will be captured by the SCK falling edge that is 0.5 SCK cycles after the SCK rising edge in 1) 3) RX_CTL.SCKO_POL=1 and RX_CTL.B_CLOCK_INV=0: Serial data will be captured by the SCK falling edge 4) RX_CTL.SCKO_POL=1 and RX_CTL.B_CLOCK_INV=1: Serial data will be captured by the SCK rising edge that is 0.5 SCK cycles after the SCK falling edge in 3) (Note that this is only the appearance w.r.t. SCK edge, the actual capture timing is derived from an internal clock that runs 8x the SCK frequency). The word sync (RX_WS) signal is not affected by this bit setting. Note: When Slave mode, must be "0". (Note: This bit is connected to AR38U12.TX_CFG.RX_BCLKINV) Default Value: 0
		0x0: RISING_EDGE_RX : SDI received at SCK rising edge when RX_CTL.SCKO_POL=0
		0x1: FALLING_EDGE_RX : SDI received at SCK falling edge when RX_CTL.SCKO_POL=0

31.1.8 I2S0_RX_WATCHDOG

Receiver watchdog

Address: 0x42A100A4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	WD_COUNTER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	WD_COUNTER [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	WD_COUNTER [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	WD_COUNTER [31:24]							

Bits	Name	Description
31 : 0	WD_COUNTER	Start value of the RX watchdog. With the reset value of 0x0000:0000 the counter is disabled. This is clocked by the AHB-Lite system clock "clk_sys". Default Value: 0

31.1.9 I2S0_TX_FIFO_CTL

TX FIFO control

Address: 0x42A10200

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	TRIGGER_LEVEL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [23:18]						FREEZE	CLEAR

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
17	FREEZE	When '1', hardware reads from the TX FIFO do not remove FIFO entries. Freeze will not advance the TX FIFO read pointer. This field is used only for debugging purposes. Default Value: 0
16	CLEAR	When '1', the TX FIFO and TX_BUF are cleared/invalidated. Invalidation will last for as long as this field is '1'. If a quick clear/invalidation is required, the field should be set to '1' and be followed by a set to '0'. If a clear/invalidation is required for an extended time period, the field should be set to '1' during the complete time period. Default Value: 0
7 : 0	TRIGGER_LEVEL	Trigger level. When the TX FIFO has less entries than the number of this field, a transmitter trigger event is generated. Default Value: 0

31.1.10 I2S0_TX_FIFO_STATUS

TX FIFO status

Address: 0x42A10204

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	USED [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							USED

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	RD_PTR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	WR_PTR [31:24]							

Bits	Name	Description
31 : 24	WR_PTR	TX FIFO write pointer: FIFO location at which a new data frame is written by the host. This field is used only for debugging purposes. Default Value: 0
23 : 16	RD_PTR	TX FIFO read pointer: FIFO location from which a data frame is read by the hardware.This field is used only for debugging purposes. Default Value: 0
8 : 0	USED	Number of entries in the TX FIFO. The field value is in the range [0, 256]. Default Value: 0

31.1.11 I2S0_TX_FIFO_WR

TX FIFO write

Address: 0x42A10208

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	W							
HW Access	R							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	W							
HW Access	R							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data written into the TX FIFO. Behavior is similar to that of a PUSH operation. Note: Don't access to this register while TX_FIFO_CTL.CLEAR is '1'. Default Value: 0

31.1.12 I2S0_RX_FIFO_CTL

RX FIFO control

Address: 0x42A10300

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	TRIGGER_LEVEL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [23:18]						FREEZE	CLEAR

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
17	FREEZE	When '1', hardware writes to the RX FIFO have no effect. Freeze will not advance the RX FIFO write pointer. This field is used only for debugging purposee. Default Value: 0
16	CLEAR	When '1', the RX FIFO and RX_BUF are cleared/invalidated. Invalidation will last for as long as this field is '1'. If a quick clear/invalidation is required, the field should be set to '1' and be followed by a set to '0'. If a clear/invalidation is required for an extended time period, the field should be set to '1' during the complete time period. Default Value: 0
7 : 0	TRIGGER_LEVEL	Trigger level. When the RX FIFO has more entries than the number of this field, a receiver trigger event is generated. Note: software can configure up to 253 in I2S mode or Left Justified (RX_CTL.I2S_MODE = "0" or "1"). In TDM mode (RX_CTL.I2S_MODE = "2" or "3"), it can configure up to [256 - (RX-_CTL.CH_NR+2)]. Default Value: 0

31.1.13 I2S0_RX_FIFO_STATUS

RX FIFO status

Address: 0x42A10304

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	USED [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							USED

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	RD_PTR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	WR_PTR [31:24]							

Bits	Name	Description
31 : 24	WR_PTR	RX FIFO write pointer: FIFO location at which a new data frame is written by the hardware. This field is used only for debugging purposes. Default Value: 0
23 : 16	RD_PTR	RX FIFO read pointer: FIFO location from which a data frame is read by the host. This field is used only for debugging purposes. Default Value: 0
8 : 0	USED	Number of entries in the RX FIFO. The field value is in the range [0, 256]. Default Value: 0

31.1.14 I2S0_RX_FIFO_RD

RX FIFO read

Address: 0x42A10308

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data read from the RX FIFO. Reading a data frame will remove the data frame from the RX FIFO; i.e. behavior is similar to that of a POP operation. Notes: - Don't access to this register while RX_FIFO_CTL.CLEAR is '1'. - Two stored data may be not valid after CMD.RX_START is set '1'. Therefore we recommend software discard those data. Default Value: 0

31.1.15 I2S0_RX_FIFO_RD_SILENT

RX FIFO silent read

Address: 0x42A1030C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data read from the RX FIFO. Reading a data frame will NOT remove the data frame from the RX FIFO; i.e. behavior is similar to that of a PEEK operation. This field is used only for debugging purposes. Notes: - Don't access to this register while RX_FIFO_CTL.CLEAR is '1'. - Two stored data may be not valid after CMD.RX_START is set '1'. Therefore we recommend software discard those data. Default Value: 0

31.1.16 I2S0_INTR

Interrupt register

Address: 0x42A10F00

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW1C	RW1C	RW1C	None		RW1C	RW1C
HW Access	None	RW1S	RW1S	RW1S	None		RW1S	RW1S
Name	None	TX_UN-DERFLOW	TX_OVER-FLOW	TX_EMPTY	None [3:2]		TX_NOT_-FULL	TX_TRIG-GER

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1C
HW Access	None							RW1S
Name	None [15:9]							TX_WD

Bits	23	22	21	20	19	18	17	16
SW Access	None	RW1C	RW1C	None	RW1C	RW1C	None	RW1C
HW Access	None	RW1S	RW1S	None	RW1S	RW1S	None	RW1S
Name	None	RX_UN-DERFLOW	RX_OVER-FLOW	None	RX_FULL	RX-_NOT_EMPTY	None	RX_TRIG-GER

Bits	31	30	29	28	27	26	25	24
SW Access	None							RW1C
HW Access	None							RW1S
Name	None [31:25]							RX_WD

Bits	Name	Description
24	RX_WD	Triggers (sets to '1') when the Rx watchdog event occurs. Default Value: 0
22	RX_UNDERFLOW	Attempt to read from an empty RX FIFO. Default Value: 0
21	RX_OVERFLOW	Attempt to write to a full RX FIFO. Default Value: 0
19	RX_FULL	RX FIFO is full. Default Value: 0
18	RX_NOT_EMPTY	RX FIFO is not empty. Default Value: 0
16	RX_TRIGGER	More entries in the RX FIFO than the value specified by TRIGGER_LEVEL in RX_FIFO_CTRL. Default Value: 0
8	TX_WD	Triggers (sets to '1') when the Tx watchdog event occurs. Default Value: 0

31.1.16 I2S0_INTR (continued)

6	TX_UNDERFLOW	Attempt to read from an empty TX FIFO. This happens when the IP is ready to transfer data and TX_EMPTY is '1'. Default Value: 0
5	TX_OVERFLOW	Attempt to write to a full TX FIFO. Default Value: 0
4	TX_EMPTY	TX FIFO is empty; i.e. it has 0 entries. Default Value: 0
1	TX_NOT_FULL	TX FIFO is not full. Default Value: 0
0	TX_TRIGGER	Less entries in the TX FIFO than the value specified by TRIGGER_LEVEL in TX_FIFO_CTRL. Default Value: 0

31.1.17 I2S0_INTR_SET

Interrupt set register

Address: 0x42A10F04

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW1S	RW1S	RW1S	None		RW1S	RW1S
HW Access	None	A	A	A	None		A	A
Name	None	TX_UN-DERFLOW	TX_OVER-FLOW	TX_EMPTY	None [3:2]		TX_NOT_-FULL	TX_TRIG-GER

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1S
HW Access	None							A
Name	None [15:9]							TX_WD

Bits	23	22	21	20	19	18	17	16
SW Access	None	RW1S	RW1S	None	RW1S	RW1S	None	RW1S
HW Access	None	A	A	None	A	A	None	A
Name	None	RX_UN-DERFLOW	RX_OVER-FLOW	None	RX_FULL	RX-_NOT_EMPTY	None	RX_TRIG-GER

Bits	31	30	29	28	27	26	25	24
SW Access	None							RW1S
HW Access	None							A
Name	None [31:25]							RX_WD

Bits	Name	Description
24	RX_WD	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
22	RX_UNDERFLOW	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
21	RX_OVERFLOW	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
19	RX_FULL	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
18	RX_NOT_EMPTY	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
16	RX_TRIGGER	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
8	TX_WD	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

31.1.17 I2S0_INTR_SET (continued)

6	TX_UNDERFLOW	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
5	TX_OVERFLOW	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
4	TX_EMPTY	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
1	TX_NOT_FULL	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	TX_TRIGGER	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

31.1.18 I2S0_INTR_MASK

Interrupt mask register

Address: 0x42A10F08

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	RW	RW	None		RW	RW
HW Access	None	R	R	R	None		R	R
Name	None	TX_UN-DERFLOW	TX_OVER-FLOW	TX_EMPTY	None [3:2]		TX_NOT_-FULL	TX_TRIG-GER

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							TX_WD

Bits	23	22	21	20	19	18	17	16
SW Access	None	RW	RW	None	RW	RW	None	RW
HW Access	None	R	R	None	R	R	None	R
Name	None	RX_UN-DERFLOW	RX_OVER-FLOW	None	RX_FULL	RX-_NOT_EMPTY	None	RX_TRIG-GER

Bits	31	30	29	28	27	26	25	24
SW Access	None							RW
HW Access	None							R
Name	None [31:25]							RX_WD

Bits	Name	Description
24	RX_WD	Mask bit for corresponding bit in interrupt request register. Default Value: 0
22	RX_UNDERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
21	RX_OVERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
19	RX_FULL	Mask bit for corresponding bit in interrupt request register. Default Value: 0
18	RX_NOT_EMPTY	Mask bit for corresponding bit in interrupt request register. Default Value: 0
16	RX_TRIGGER	Mask bit for corresponding bit in interrupt request register. Default Value: 0
8	TX_WD	Mask bit for corresponding bit in interrupt request register. Default Value: 0

31.1.18 I2S0_INTR_MASK (continued)

6	TX_UNDERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
5	TX_OVERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
4	TX_EMPTY	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	TX_NOT_FULL	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	TX_TRIGGER	Mask bit for corresponding bit in interrupt request register. Default Value: 0

31.1.19 I2S0_INTR_MASKED

Interrupt masked register

Address: 0x42A10F0C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	R	R	R	None		R	R
HW Access	None	W	W	W	None		W	W
Name	None	TX_UN-DERFLOW	TX_OVER-FLOW	TX_EMPTY	None [3:2]		TX_NOT_-FULL	TX_TRIG-GER

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							TX_WD

Bits	23	22	21	20	19	18	17	16
SW Access	None	R	R	None	R	R	None	R
HW Access	None	W	W	None	W	W	None	W
Name	None	RX_UN-DERFLOW	RX_OVER-FLOW	None	RX_FULL	RX-_NOT_EMPTY	None	RX_TRIG-GER

Bits	31	30	29	28	27	26	25	24
SW Access	None							R
HW Access	None							W
Name	None [31:25]							RX_WD

Bits	Name	Description
24	RX_WD	Logical and of corresponding request and mask bits. Default Value: 0
22	RX_UNDERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
21	RX_OVERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
19	RX_FULL	Logical and of corresponding request and mask bits. Default Value: 0
18	RX_NOT_EMPTY	Logical and of corresponding request and mask bits. Default Value: 0
16	RX_TRIGGER	Logical and of corresponding request and mask bits. Default Value: 0
8	TX_WD	Logical and of corresponding request and mask bits. Default Value: 0

31.1.19 I2S0_INTR_MASKED (continued)

6	TX_UNDERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
5	TX_OVERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
4	TX_EMPTY	Logical and of corresponding request and mask bits. Default Value: 0
1	TX_NOT_FULL	Logical and of corresponding request and mask bits. Default Value: 0
0	TX_TRIGGER	Logical and of corresponding request and mask bits. Default Value: 0

Section J: System Registers

See the following documentation available at Arm® website for the details of Cortex®- M4 and Cortex®-M0+ system registers.

- Cortex®-M4 Technical Reference Manual
- Cortex®-M0+ Technical Reference Manual

Revision History

Revision History

Document Title: PSoC 6 MCU: CY8C63x6, CY8C63x7 Registers Technical Reference Manual (TRM) Document Number: 002-18270			
Revision	**ECN#**	**Issue Date**	**Description of Change**
**	5563478	12/27/2016	Specification for new silicon
*A	5653974	03/08/2017	Updated Template
*B	5803716	07/13/2017	Updated all registers
*C	5855453	08/16/2017	Updated all registers
*D	6032757	01/31/2018	Updated all registers
*E	6155258	05/03/2018	Approximately 50% size reduced. The registers TRM is consolidated into a single document instead of three separate documents.
*F	6406758	12/21/2018	Document size reduction.
*G	6657179	08/21/2019	Updated title Updated Peripheral Registers
*H	6683263	09/26/2019	Renamed Energy Profiler Registers to Profiler Registers Updated title
*I	6917234	07/28/2020	Added CRYPTO chapter. Updated SRSS, MCWDT, GPIO, LPCOMP, FLASH and USB chapters.