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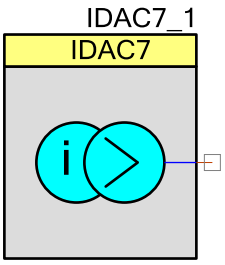
PSoC 4 Current Digital to Analog Converter (IDAC7)

1.10



Features

- Six current ranges (4.76 uA to 609 uA)
- Sink or Source current
- 7-bit resolution
- Two IDACs can be put in parallel to form an 8-bit IDAC
- Add external resistor for VDAC functionality

General Description

The IDAC7 component provides a programmable current with a resolution of 7 bits. The seven overlapping ranges are from 4.76 uA to 609 uA, to allow sufficient resolution for most applications.

When to Use a IDAC7

- Resistance measurements
- Current sink or source
- Capacitance measurements other than CapSense
- Sensor current
- Temperature measurement (diode sensor)

Input/Output Connections

This section describes the various input and output connections for the IDAC7 component.

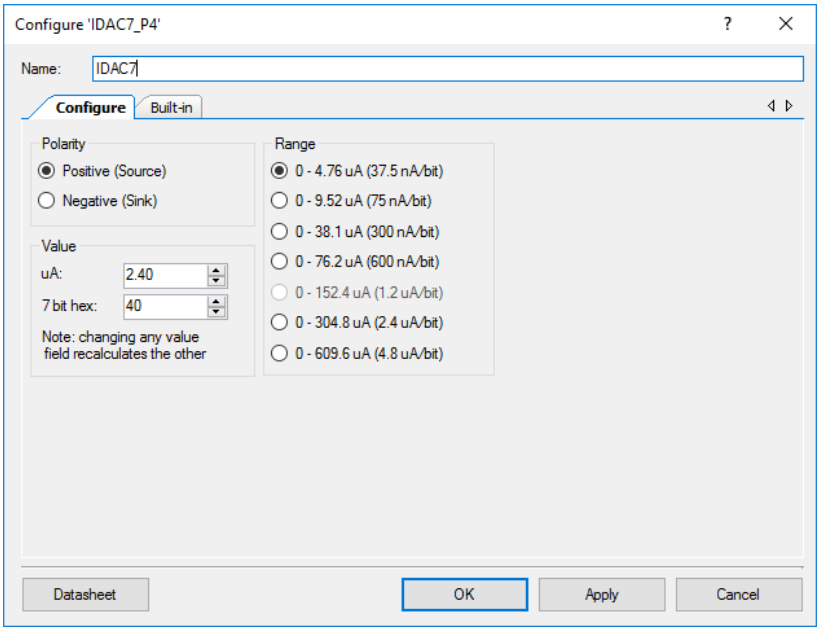
Iout – Analog

The connection to the DAC's current source/sink.

Component Parameters

Drag an IDAC7 component onto your design and double-click it to open the Configure dialog. This dialog has the following tabs with different parameters.

Configure Tab



Parameter Name	Description
Polarity	Selects either a current sink or source initial configuration. **Parameter Options:** • Positive (Source) (default) • Negative (Sink)
Range	Selects one of seven overlapping current ranges. **Parameter Options:** • 0-4.76uA (37.5nA/bit) (default) • 0-9.52uA (75 nA/bit) • 0-38.1uA (300nA/bit) • 0-76.2uA (600nA/bit) • 0-152.4uA (1.2uA/bit) • 0-304.8uA (2.4uA/bit) • 0-609.6uA (4.8uA/bit)

Parameter Name	Description
Value	Selects the initial value of the current sink or source. **Parameter Options:** • 0 to 7F (default 40)

Application Programming Interface

Application Programming Interface (API) routines allow you to configure the component using software. The following sections list and describe each function and dependencies.

By default, PSoC Creator assigns the instance name **IDAC7** to the first instance of a component in a given design. You can rename it to any unique value that follows the syntactic rules for identifiers. The instance name becomes the prefix of every global function name, variable, and constant symbol. For readability, the instance name used in the following table is **IDAC7**.

General APIs

Description

General APIs are used for run-time configuration of the component during active power mode. These include, initializing, starting, stopping, reading from registers and writing to registers.

Functions

- void IDAC7_Init (void)
- void IDAC7_Enable (void)
- void IDAC7_Start (void)
- void IDAC7_Stop (void)
- void IDAC7_SetValue (uint32 current)
- void IDAC7_SetPolarity (uint32 polarity)
- void IDAC7_SetRange (uint32 range)

Function Documentation

void IDAC7_Init (void)

Initializes all initial parameters and operating modes.

void IDAC7_Enable (void)

Enables the IDAC for operation.

void IDAC7_Start (void)

Initializes all the parameters required to setup the component as defined in the customizer.

void IDAC7_Stop (void)

The Stop is not required.

void IDAC7_SetValue (uint32 current)

Sets the IDAC current to the new value.

Parameters:

uint32	current: The current value Valid range : [0 - 127]

void IDAC7_SetPolarity (uint32 polarity)

Sets polarity to either sink or source.

Parameters:

uint32	polarity: Current polarity • IDAC7_POL_SOURCE : Source polarity • IDAC7_POL_SINK : Sink polarity

void IDAC7_SetRange (uint32 range)

Sets the IDAC range to one of the six ranges.

Parameters:

uint32	range: Current range • IDAC7_RNG_4_76UA : 37.5 nA/bit current range • IDAC7_RNG_9_52UA : 75 nA/bit current range • IDAC7_RNG_38_1UA : 300 nA/bit current range • IDAC7_RNG_76_2UA : 600 nA/bit current range • IDAC7_RNG_152_4UA: 1.2 uA/bit current range • IDAC7_RNG_304_8UA : 2.4 uA/bit current range • IDAC7_RNG_609_6UA : 4.8 uA/bit current range

Power Management APIs

Description

Power management APIs perform the necessary configurations to the components to prepare it for entering low power modes.

These APIs must be used if the intent is to put the chip to sleep, and then to continue component operation when it comes back to active power mode.

This component does not stop the CSD IP block. One possible way to turn off the entire CSD block before sleep is to use a specific define (IDAC7_CSD_CONFIG_ENABLE) for the m0s8csdv2 IP block control register (IDAC7_CSD_CONTROL_REG):

```
IDAC7_CSD_CONTROL_REG &= ~IDAC7_CSD_CONFIG_ENABLE
```

Functions

- void IDAC7_Sleep (void)
- void IDAC7_Wakeup (void)

Function Documentation

void IDAC7_Sleep (void)

Stores all volatile settings and powers down the IDAC7.

void IDAC7_Wakeup (void)

Restores settings and power saved by the Sleep function after wakeup.

Global Variables

The following global variables are used in the component.

- uint32 IDAC7_initVar – This variable is used to indicate the initial configuration of this component. The variable is initialized to zero and set to 1 the first time IDAC7_Start() is called. This allows the component initialization without re-initialization in all subsequent calls to the IDAC7_Start() routine.

Code Examples and Application Notes

This section lists the projects that demonstrate the use of the component.

Code Examples

PSoC Creator provides access to code examples in the Code Example dialog. For component-specific examples, open the dialog from the Component Catalog or an instance of the component in a schematic. For general examples, open the dialog from the Start Page or **File** menu. As needed, use the **Filter Options** in the dialog to narrow the list of projects available to select.

Refer to the "Code Example" topic in the PSoC Creator Help for more information.

There are also numerous code examples that include schematics and example code available online at the Cypress Code Examples web page. Examples that use this component include:

- CE204022 - IDAC7_Sawtooth.

API Memory Usage

Shows the Flash, SRAM and stack usage of the component.

The component memory usage varies significantly depending on the compiler, device, number of APIs used and component configuration. The following table provides the memory usage for all APIs available in the given component configuration.

The measurements have been done with an associated compiler configured in Release mode with optimization set for Size. For a specific design, the map file generated by the compiler can be analyzed to determine the memory usage.

PSoC 4 (GCC)

Configuration	PSoC 4000S / PSoC 4100S / PSoC Analog Coprocessor	
	Flash Bytes	SRAM Bytes
All	226	4

Functional Description

The 7-bit current DAC (IDAC7) is based on the CapSense block (CSDV2).

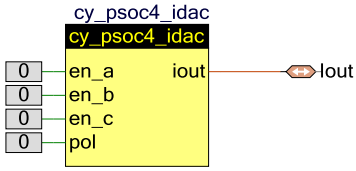
Note Some PSoC 4100S devices have an enhanced version of the CapSense block, which includes an additional 1.2 uA/bit current range and improved performance on the VDDA voltage below 2 V.

Definitions

- DAC – Digital to Analog Converter
- IDAC – Current Digital to Analog Converter
- VDAC – Voltage Digital to Analog Converter
- CSDV2 – Capacitive Sigma Delta version 2

Block Diagram and Configuration

The following is a simplified diagram of the IDAC7 hardware:



The IDAC7 component uses cy_psoc4_idac primitive. It is configured using the CSDV2 block configuration registers only.

DMA Support

The DMA Component can be used to transfer data from the component registers to RAM or another component. Use the DMA Wizard to configure DMA operation as follows:

Name of DMA Source/ Destination in the DMA Wizard	Length	Direction	DMA Req Signal	DMA Req Type	Description
IDAC7_IDAC_CONTROL_PTR	32 bit	Source/ Destination	N/A	N/A	This register is intended to control the IDAC settings. See the device Technical Reference Manual (TRM) for details.

Note DMA support in the IDAC7 component is limited due to the following reasons:

- The IDAC7_IDAC_CONTROL register is common for the IDAC setting and IDAC current value.

Before using the DMA channel with the IDAC7 component, review the description of this register in the device registers Technical Reference Manual (TRM).

Placement

The PSoC 4 IDACs are part of the CapSense CSDV2 hardware block. Two of the 7-bit IDACs are available.

Note The IDAC Component cannot be placed on the schematic if both AMUXA and AMUXB buses are used by the other blocks (for example, the CapSense Component with the enabled Shield electrode).

MISRA Compliance

This section describes the MISRA-C:2004 compliance and deviations for the component. There are two types of deviations defined:

- project deviations – deviations that are applicable for all PSoC Creator components
- specific deviations – deviations that are applicable only for this component

This section provides information on component-specific deviations. Project deviations are described in the MISRA Compliance section of the *System Reference Guide* along with information on the MISRA compliance verification environment.

The IDAC7 component does not have any specific deviations.

Registers

For fixed-function blocks, refer to the device *Technical Reference Manual (TRM)* for more information about the registers.

Component Debug Window

PSoC Creator allows you to view debug information about components in your design. Each component window lists the memory and registers for the instance. For detailed hardware registers descriptions, refer to the appropriate device technical reference manual.

To open the Component Debug window:

1. Make sure the debugger is running or in break mode.
2. Choose **Windows > Components…** from the **Debug** menu.
3. In the Component Window Selector dialog, select the component instances to view and click **OK**.

The selected Component Debug window(s) will open within the debugger framework. Refer to the "Component Debug Window" topic in the PSoC Creator Help for more information.

Resources

The IDAC7 uses the following device resources:

- CSDV2 IDAC block

DC and AC Electrical Characteristics

Specifications are valid for -40° C <= TA <= 85° C and TJ <= 100° C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

Note Final characterization data for the PSoC Analog Coprocessor device is not available at this time. Once the data is available, the component datasheet will be updated on the Cypress web site.

Parameter	Description	Min	Typ	Max	Units	Details / Conditions
VDD_RIPPLE	Max allowed ripple on power supply, DC to 10 MHz	–	–	±50	mV	V_{DD} > 2 V (with ripple), 25 °C T_A, Sensitivity = 0.1 pF
VDD_RIPPLE_1.8	Max allowed ripple on power supply, DC to 10 MHz	–	–	±25	mV	V_{DD} > 1.75V (with ripple), 25 °C T_A, Parasitic Capacitance (C_P) < 20 pF, Sensitivity ≥ 0.4 pF
ICSD	Maximum block current	–	–	4000	µA	Maximum block current for both IDACs in dynamic (switching) mode including comparators, buffer, and reference generator.
V_{REF}	Voltage reference for CSD and Comparator	0.6	1.2	V_{DDA} - 0.6	V	V_{DDA} - 0.6 or 4.4, whichever is lower
VREF_EXT	External Voltage reference for CSD and Comparator	0.6		V_{DDA} - 0.6	V	V_{DDA} - 0.6 or 4.4, whichever is lower
IDAC1IDD	IDAC1 (7-bits) block current	–	–	1750	µA	
IDAC2IDD	IDAC2 (7-bits) block current	–	–	1750	µA	
VCSD	Voltage range of operation	1.71	–	5.5	V	1.8 V ±5% or 1.8 V to 5.5 V
VCOMPIDAC [1]	Voltage compliance range of IDAC	0.6	–	V_{DDA} –0.6	V	V_{DDA} - 0.6 or 4.4, whichever is lower
IDAC1DNL	DNL	–1	–	1	LSB	
IDAC1INL	INL	–2	–	2	LSB	INL is ±5.5 LSB for V_{DDA} < 2 V

1. The min value of the VCOMPIDAC defines the maximum IDAC load impedance for the Negative (Sink) polarity. The max value of the VCOMPIDAC defines the maximum IDAC load impedance for the Positive (Source) polarity.

Parameter	Description	Min	Typ	Max	Units	Details / Conditions
IDAC2DNL	DNL	–1	–	1	LSB	
IDAC2INL	INL	–2	–	2	LSB	INL is ±5.5 LSB for V_{DDA} < 2 V
SNR	Ratio of counts of finger to noise. Guaranteed by characterization	5	–	–	Ratio	Capacitance range of 5 to 35 pF, 0.1-pF sensitivity. All use cases. V_{DDA} > 2 V.
IDAC1CRT1	Output current of IDAC1 (7 bits) in low range	4.2	–	5.4	µA	LSB = 37.5-nA typ.
IDAC1CRT2	Output current of IDAC1(7 bits) in medium range	34	–	41	µA	LSB = 300-nA typ.
IDAC1CRT3	Output current of IDAC1(7 bits) in high range	275	–	330	µA	LSB = 2.4-µA typ.
IDAC1CRT12	Output current of IDAC1 (7 bits) in low range, 2X mode	8	–	10.5	µA	LSB = 75-nA typ.
IDAC1CRT22	Output current of IDAC1(7 bits) in medium range, 2X mode	69	–	82	µA	LSB = 600-nA typ.
IDAC1CRT32	Output current of IDAC1(7 bits) in high range, 2X mode	540	–	660	µA	LSB = 4.8-µA typ.
IDAC2CRT1	Output current of IDAC2 (7 bits) in low range	4.2	–	5.4	µA	LSB = 37.5-nA typ.
IDAC2CRT2	Output current of IDAC2 (7 bits) in medium range	34	–	41	µA	LSB = 300-nA typ.
IDAC2CRT3	Output current of IDAC2 (7 bits) in high range	275	–	330	µA	LSB = 2.4-µA typ.
IDAC2CRT12	Output current of IDAC2 (7 bits) in low range, 2X mode	8	–	10.5	µA	LSB = 75-nA typ.
IDAC2CRT22	Output current of IDAC2(7 bits) in medium range, 2X mode	69	–	82	µA	LSB = 600-nA typ.
IDAC2CRT32	Output current of IDAC2(7 bits) in high range, 2X mode	540	–	660	µA	LSB = 4.8-µA typ.
IDAC3CRT13	Output current of IDAC in 8-bit mode in low range	8	–	10.5	µA	LSB = 37.5-nA typ.
IDAC3CRT23	Output current of IDAC in 8-bit mode in medium range	69	–	82	µA	LSB = 300-nA typ.
IDAC3CRT33	Output current of IDAC in 8-bit mode in high range	540	–	660	µA	LSB = 2.4-µA typ.
IDACOFFSET	All zeroes input	–	–	1	LSB	Polarity set by Source or Sink. Offset is 2 LSBs for 37.5 nA/LSB mode
IDACGAIN	Full-scale error less offset	–	–	±10	%	

Parameter	Description	Min	Typ	Max	Units	Details / Conditions
IDACMISMATCH1	Mismatch between IDAC1 and IDAC2 in Low mode	–	–	9.2	LSB	LSB = 37.5-nA typ.
IDACMISMATCH2	Mismatch between IDAC1 and IDAC2 in Medium mode	–	–	5.6	LSB	LSB = 300-nA typ.
IDACMISMATCH3	Mismatch between IDAC1 and IDAC2 in High mode	–	–	6.8	LSB	LSB = 2.4-µA typ.
IDACSET8	Settling time to 0.5 LSB for 8-bit IDAC	–	–	10	µs	Full-scale transition. No external load.
IDACSET7	Settling time to 0.5 LSB for 7-bit IDAC	–	–	10	µs	Full-scale transition. No external load.
CMOD	External modulator capacitor.	–	2.2	–	nF	5-V rating, X7R or NP0 cap.

Component Changes

This section lists the major changes in the component from the previous version.

Version	Description of Changes	Reason for Changes / Impact
1.10.a	Edited the datasheet.	Added a note that the IDAC Component cannot be placed on the schematic if both AMUXA and AMUXB buses are used by the other blocks.
1.10	Added 0-152.4uA (1.2uA/bit) range for PSoC 4100S devices, which have an enhancement version of the CapSense block.	Updated device support.
1.0.c	Edited datasheet.	Added final characterization data for PSoC 4100S device.
1.0.b	Edited datasheet.	Added final characterization data for PSoC 4000S device
1.0.a	Edited datasheet.	Final characterization data for PSoC 4000S, PSoC 4100S and PSoC Analog Coprocessor devices is not available at this time. Once the data is available, the component datasheet will be updated on the Cypress web site.
1.0	Initial release	

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