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PSoC 4100-BL/4200-BL Family

PSoC® 4 BLE Registers Technical Reference Manual (TRM)

Document No. 001-92739 Rev. *E August 31, 2017

Book 2 of 2

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Contents

11. DMA Descriptor Registers 666

Register Mapping

The Register Mapping section discusses the registers and lists all the registers in mapping tables, in address order.

Register General Conventions

The register conventions specific to this section and the Register Reference chapter are listed in this table.

Convention	Example	Description
'x' in a register name	ACBxxCR1	Multiple instances/address ranges of the same register
R	R : 00	Read register or bit(s)
W	W : 00	Write register or bit(s)
WOC	WOC:0	Write one to clear
WZC	WZC:0	Write zero to clear
RC	RC:0	Read to clear
WC	WC:0	Write to clear
NA	NA:000	Reserved
U	R:U	Undefined
00	RW : 00	Reset value is 0x00
XX	RW : XX	Register is not reset

1 UDB Array Bank Control (BCTL) Registers

This section discusses the BCTL registers. It lists all the registers in mapping tables, in address order.

1.1 Register Details

Register Name	Address
UDB_BCTL0_DRV	0x400F6000
UDB_BCTL0_MDCLK_EN	0x400F6001
UDB_BCTL0_MBCLK_EN	0x400F6002
UDB_BCTL0_BOTSEL_L	0x400F6008
UDB_BCTL0_BOTSEL_U	0x400F6009
UDB_BCTL0_TOPSEL_L	0x400F600A
UDB_BCTL0_TOPSEL_U	0x400F600B
UDB_BCTL0_QCLK_EN0	0x400F6010
UDB_BCTL0_QCLK_EN1	0x400F6012
UDB_BCTL0_QCLK_EN2	0x400F6014
UDB_BCTL0_QCLK_EN3	0x400F6016

1.1.1 UDB_BCTL0_DRV

Master Digital Clock Drive Register

Address: 0x400F6000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DRV [7:0]							

Bits	Name	Description
7 : 0	DRV	Master digital clock drive enable for the digital clock that matches the index. Default Value: 0 **0x0: DISABLE:** Enabled drive from array bottom, top drive disabled. **0x1: ENABLE:** Disabled drive from array bottom, top drive enabled.

1.1.2 UDB_BCTL0_MDCLK_EN

Master Digital Clock Enable Register

Address: 0x400F6001

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DCEN [7:0]							

Bits	Name	Description
7 : 0	DCEN	Master digital clock enable for the digital clock that matches the index. Default Value: 0 **0x0: DISABLE:** Disabled **0x1: ENABLE:** Enabled

1.1.3 UDB_BCTL0_MBCLK_EN

Master Bus Clock Enable Register

Address: 0x400F6002

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							BCEN

Bits	Name	Description
0	BCEN	Bank Clock Enable Control Default Value: 0 **0x0: DISABLE:** Disabled **0x1: ENABLE:** Enabled

1.1.4 UDB_BCTL0_BOTSEL_L

Lower Nibble Bottom Digital Clock Select Register

Address: 0x400F6008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	CLK_SEL3 [7:6]		CLK_SEL2 [5:4]		CLK_SEL1 [3:2]		CLK_SEL0 [1:0]	

Bits	Name	Description
7 : 6	CLK_SEL3	Clock selection control for digital clock Default Value: 0 **0x0: EDGE_ENABLES:** clock generated from edge enables from clock distribution block **0x1: PORT_INPUT:** Port input **0x2: DSI_OUTPUT:** DSI output **0x3: SYNC_DSI_OUTPUT:** synchronized DSI output
5 : 4	CLK_SEL2	Clock selection control for digital clock Default Value: 0 **0x0: EDGE_ENABLES:** clock generated from edge enables from clock distribution block **0x1: PORT_INPUT:** Port input **0x2: DSI_OUTPUT:** DSI output **0x3: SYNC_DSI_OUTPUT:** synchronized DSI output
3 : 2	CLK_SEL1	Clock selection control for digital clock Default Value: 0 **0x0: EDGE_ENABLES:** clock generated from edge enables from clock distribution block **0x1: PORT_INPUT:** Port input **0x2: DSI_OUTPUT:** DSI output **0x3: SYNC_DSI_OUTPUT:** synchronized DSI output
1 : 0	CLK_SEL0	Clock selection control for digital clock Default Value: 0

(continued)

0x0: EDGE_ENABLES:
clock generated from edge enables from clock distribution block

0x1: PORT_INPUT:
Port input

0x2: DSI_OUTPUT:
DSI output

0x3: SYNC_DSI_OUTPUT:
synchronized DSI output

1.1.5 UDB_BCTL0_BOTSEL_U

Upper Nibble Bottom Digital Clock Select Register

Address: 0x400F6009

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	CLK_SEL7 [7:6]		CLK_SEL6 [5:4]		CLK_SEL5 [3:2]		CLK_SEL4 [1:0]	

Bits	Name	Description
7 : 6	CLK_SEL7	Clock selection control for digital clock Default Value: 0 **0x0: EDGE_ENABLES:** clock generated from edge enables from clock distribution block **0x1: PORT_INPUT:** Port input **0x2: DSI_OUTPUT:** DSI output **0x3: SYNC_DSI_OUTPUT:** synchronized DSI output
5 : 4	CLK_SEL6	Clock selection control for digital clock Default Value: 0 **0x0: EDGE_ENABLES:** clock generated from edge enables from clock distribution block **0x1: PORT_INPUT:** Port input **0x2: DSI_OUTPUT:** DSI output **0x3: SYNC_DSI_OUTPUT:** synchronized DSI output
3 : 2	CLK_SEL5	Clock selection control for digital clock Default Value: 0 **0x0: EDGE_ENABLES:** clock generated from edge enables from clock distribution block **0x1: PORT_INPUT:** Port input **0x2: DSI_OUTPUT:** DSI output **0x3: SYNC_DSI_OUTPUT:** synchronized DSI output
1 : 0	CLK_SEL4	Clock selection control for digital clock Default Value: 0

(continued)

0x0: EDGE_ENABLES:
clock generated from edge enables from clock distribution block

0x1: PORT_INPUT:
Port input

0x2: DSI_OUTPUT:
DSI output

0x3: SYNC_DSI_OUTPUT:
synchronized DSI output

1.1.6 UDB_BCTL0_TOPSEL_L

Lower Nibble Top Digital Clock Select Register

Address: 0x400F600A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	CLK_SEL3 [7:6]		CLK_SEL2 [5:4]		CLK_SEL1 [3:2]		CLK_SEL0 [1:0]	

Bits	Name	Description
7 : 6	CLK_SEL3	Clock selection control for digital clock Default Value: 0 **0x0: EDGE_ENABLES:** clock generated from edge enables from clock distribution block **0x1: PORT_INPUT:** Port input **0x2: DSI_OUTPUT:** DSI output **0x3: SYNC_DSI_OUTPUT:** synchronized DSI output
5 : 4	CLK_SEL2	Clock selection control for digital clock Default Value: 0 **0x0: EDGE_ENABLES:** clock generated from edge enables from clock distribution block **0x1: PORT_INPUT:** Port input **0x2: DSI_OUTPUT:** DSI output **0x3: SYNC_DSI_OUTPUT:** synchronized DSI output
3 : 2	CLK_SEL1	Clock selection control for digital clock Default Value: 0 **0x0: EDGE_ENABLES:** clock generated from edge enables from clock distribution block **0x1: PORT_INPUT:** Port input **0x2: DSI_OUTPUT:** DSI output **0x3: SYNC_DSI_OUTPUT:** synchronized DSI output
1 : 0	CLK_SEL0	Clock selection control for digital clock Default Value: 0

(continued)

0x0: EDGE_ENABLES:
clock generated from edge enables from clock distribution block

0x1: PORT_INPUT:
Port input

0x2: DSI_OUTPUT:
DSI output

0x3: SYNC_DSI_OUTPUT:
synchronized DSI output

1.1.7 UDB_BCTL0_TOPSEL_U

Upper Nibble Top Digital Clock Select Register

Address: 0x400F600B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	CLK_SEL7 [7:6]		CLK_SEL6 [5:4]		CLK_SEL5 [3:2]		CLK_SEL4 [1:0]	

Bits	Name	Description
7 : 6	CLK_SEL7	Clock selection control for digital clock Default Value: 0 **0x0: EDGE_ENABLES:** clock generated from edge enables from clock distribution block **0x1: PORT_INPUT:** Port input **0x2: DSI_OUTPUT:** DSI output **0x3: SYNC_DSI_OUTPUT:** synchronized DSI output
5 : 4	CLK_SEL6	Clock selection control for digital clock Default Value: 0 **0x0: EDGE_ENABLES:** clock generated from edge enables from clock distribution block **0x1: PORT_INPUT:** Port input **0x2: DSI_OUTPUT:** DSI output **0x3: SYNC_DSI_OUTPUT:** synchronized DSI output
3 : 2	CLK_SEL5	Clock selection control for digital clock Default Value: 0 **0x0: EDGE_ENABLES:** clock generated from edge enables from clock distribution block **0x1: PORT_INPUT:** Port input **0x2: DSI_OUTPUT:** DSI output **0x3: SYNC_DSI_OUTPUT:** synchronized DSI output
1 : 0	CLK_SEL4	Clock selection control for digital clock Default Value: 0

(continued)

0x0: EDGE_ENABLES:
clock generated from edge enables from clock distribution block

0x1: PORT_INPUT:
Port input

0x2: DSI_OUTPUT:
DSI output

0x3: SYNC_DSI_OUTPUT:
synchronized DSI output

1.1.8 UDB_BCTL0_QCLK_EN0

Quadrant Digital Clock Enable Registers

Address: 0x400F6010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DCEN_Q [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	SLEEP_TEST	NC0	WR_CFG_OPT	GLB_DSI_WR	DISABLE_ROUTE	GCH_WR_HI	GCH_WR_LO	BCEN_Q

Bits	Name	Description
15	SLEEP_TEST	Assertion of this bit drives sleep into the UDB array for internal UDB test purposes. Assertion does not affect the power switches. This signal drives pulldowns on the write strobes for all configuration memory, inhibiting writes when set. Sleep or sleep_test does not inhibit writes to this bit, allowing it to be cleared once it has been set. Control is split top and bottom. BCTL0_QCLK_EN0[15:8] controls Bank 0 UDB pairs 0-3 and lower half DSI blocks. BCTL0_QCLK_EN3[15:8] controls Bank 0 UDB pairs 4-7 and upper half DSI blocks. The SLEEP_TEST bits in the other BCTLx_QCLK_ENy registers are not used. Sleep assertion drives bus_rdata to zero so bus read transactions will not return data during assertion of certain sleep_test bits. This is only true for assertion of sleep_test in BCTL0_QCLK_EN0 for Bank 0. Default Value: 0 **0x0: DISABLE:** sleep_test is not asserted. **0x1: ENABLE:** sleep_test is asserted.
14	NC0	Spare register bit Default Value: 0
13	WR_CFG_OPT	Select 1/2 clock cycle or full clock cycle generation for bus_last_strobe used in generating write strobes for latches within the UDB. Only one QCLK_ENx register per bank has an active bit. BCTL0_QCLK_EN0[15:8] controls this bit for Bank 0. The WR_CFG_OPT bits in the other BCTLx_QCLK_ENy[15:8] registers are not used. Default Value: 0 **0x0: FULL_CYCLE_STB:** bus_last_strobe is generated for the full final bus_clk cycle of a bus transaction. **0x1: HALF_CYCLE_STB:** bus_last_strobe is generated during the last 1/2 clock cycle of a bus transaction on the negative edge of bus_clk.

(continued)

12	GLB_DSI_WR	Enable global write operation for the DSI routing channels. When this bit is set, the DSI ID select decoding is bypassed and therefore multiple channels can be written to simultaneously. This is designed to support test modes. Control is split top and bottom. BCTL0_QCLK_EN0[15:8] controls lower half DSI blocks. BCTL0_QCLK_EN3[15:8] controls upper half DSI blocks. The GLB_DSI_WR bits in the other BCTLx_QCLK_ENy[15:8] registers are not used. Default Value: 0 **0x0: DISABLE:** Global DSI channel configuration write is disabled. **0x1: ENABLE:** Global DSI channel configuration write is enabled.
11	DISABLE_ROUTE	By default, when this bit is set to '0', the quadrant routing (for 2 channels in the quadrant) are enabled when the global route enable for the bank is set. However, when this bit is set to '1', the routing in the associated quadrant is disabled and is not enabled by the global route enable bit. The routing will remain in a benign state until it is subsequently configured and then enabled by clearing this bit. Default Value: 0 **0x0: DISABLE:** The routing in this quadrant can be enabled with the bank route enable bit. (default) **0x1: ENABLE:** The routing in this quadrant is disabled and held in a benign state.
10	GCH_WR_HI	Enable global write operation for the routing channel with the higher address in the associated quadrant. When enabled, the UDB ID select decoding is bypassed and therefore multiple channels can be written to simultaneously. This is designed to support test modes. Default Value: 0 **0x0: DISABLE:** Global UDB channel configuration write for higher order address is disabled. **0x1: ENABLE:** Global UDB channel configuration write for higher order address is enabled.
9	GCH_WR_LO	Enable global write operation for the routing channel with the lower address in the associated quadrant. When enabled, the UDB ID select decoding is bypassed and therefore multiple channels can be written to simultaneously. This is designed to support test modes. Default Value: 0 **0x0: DISABLE:** Global UDB channel configuration write for lower order address is disabled. **0x1: ENABLE:** Global UDB channel configuration write for lower order address is enabled.
8	BCEN_Q	Bank Clock Enable Control Default Value: 0 **0x0: DISABLE:** Digital Global clock is disabled. **0x1: ENABLE:** Digital Global clock is enabled.
7 : 0	DCEN_Q	Digital clock enable for indexed digital clock for the associated quadrant. Default Value: 0 **0x0: DISABLE:** Disabled **0x1: ENABLE:** Enabled

1.1.9 UDB_BCTL0_QCLK_EN1

Quadrant Digital Clock Enable Registers

Address: 0x400F6012

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DCEN_Q [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	SLEEP_TEST	NC0	WR_CFG_OPT	GLB_DSI_WR	DISABLE_ROUTE	GCH_WR_HI	GCH_WR_LO	BCEN_Q

Bits	Name	Description
15	SLEEP_TEST	Assertion of this bit drives sleep into the UDB array for internal UDB test purposes. Assertion does not affect the power switches. This signal drives pulldowns on the write strobes for all configuration memory, inhibiting writes when set. Sleep or sleep_test does not inhibit writes to this bit, allowing it to be cleared once it has been set. Control is split top and bottom. BCTL0_QCLK_EN0[15:8] controls Bank 0 UDB pairs 0-3 and lower half DSI blocks. BCTL0_QCLK_EN3[15:8] controls Bank 0 UDB pairs 4-7 and upper half DSI blocks. The SLEEP_TEST bits in the other BCTLx_QCLK_ENy registers are not used. Sleep assertion drives bus_rdata to zero so bus read transactions will not return data during assertion of certain sleep_test bits. This is only true for assertion of sleep_test in BCTL0_QCLK_EN0 for Bank 0. Default Value: 0 **0x0: DISABLE:** sleep_test is not asserted. **0x1: ENABLE:** sleep_test is asserted.
14	NC0	Spare register bit Default Value: 0
13	WR_CFG_OPT	Select 1/2 clock cycle or full clock cycle generation for bus_last_strobe used in generating write strobes for latches within the UDB. Only one QCLK_ENx register per bank has an active bit. BCTL0_QCLK_EN0[15:8] controls this bit for Bank 0. The WR_CFG_OPT bits in the other BCTLx_QCLK_ENy[15:8] registers are not used. Default Value: 0 **0x0: FULL_CYCLE_STB:** bus_last_strobe is generated for the full final bus_clk cycle of a bus transaction. **0x1: HALF_CYCLE_STB:** bus_last_strobe is generated during the last 1/2 clock cycle of a bus transaction on the negative edge of bus_clk.

(continued)

12	GLB_DSI_WR	Enable global write operation for the DSI routing channels. When this bit is set, the DSI ID select decoding is bypassed and therefore multiple channels can be written to simultaneously. This is designed to support test modes. Control is split top and bottom. BCTL0_QCLK_EN0[15:8] controls lower half DSI blocks. BCTL0_QCLK_EN3[15:8] controls upper half DSI blocks. The GLB_DSI_WR bits in the other BCTLx_QCLK_ENy[15:8] registers are not used. Default Value: 0 **0x0: DISABLE:** Global DSI channel configuration write is disabled. **0x1: ENABLE:** Global DSI channel configuration write is enabled.
11	DISABLE_ROUTE	By default, when this bit is set to '0', the quadrant routing (for 2 channels in the quadrant) are enabled when the global route enable for the bank is set. However, when this bit is set to '1', the routing in the associated quadrant is disabled and is not enabled by the global route enable bit. The routing will remain in a benign state until it is subsequently configured and then enabled by clearing this bit. Default Value: 0 **0x0: DISABLE:** The routing in this quadrant can be enabled with the bank route enable bit. (default) **0x1: ENABLE:** The routing in this quadrant is disabled and held in a benign state.
10	GCH_WR_HI	Enable global write operation for the routing channel with the higher address in the associated quadrant. When enabled, the UDB ID select decoding is bypassed and therefore multiple channels can be written to simultaneously. This is designed to support test modes. Default Value: 0 **0x0: DISABLE:** Global UDB channel configuration write for higher order address is disabled. **0x1: ENABLE:** Global UDB channel configuration write for higher order address is enabled.
9	GCH_WR_LO	Enable global write operation for the routing channel with the lower address in the associated quadrant. When enabled, the UDB ID select decoding is bypassed and therefore multiple channels can be written to simultaneously. This is designed to support test modes. Default Value: 0 **0x0: DISABLE:** Global UDB channel configuration write for lower order address is disabled. **0x1: ENABLE:** Global UDB channel configuration write for lower order address is enabled.
8	BCEN_Q	Bank Clock Enable Control Default Value: 0 **0x0: DISABLE:** Digital Global clock is disabled. **0x1: ENABLE:** Digital Global clock is enabled.
7 : 0	DCEN_Q	Digital clock enable for indexed digital clock for the associated quadrant. Default Value: 0 **0x0: DISABLE:** Disabled **0x1: ENABLE:** Enabled

1.1.10 UDB_BCTL0_QCLK_EN2

Quadrant Digital Clock Enable Registers

Address: 0x400F6014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DCEN_Q [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	SLEEP_TEST	NC0	WR_CFG_OPT	GLB_DSI_WR	DISABLE_ROUTE	GCH_WR_HI	GCH_WR_LO	BCEN_Q

Bits	Name	Description
15	SLEEP_TEST	Assertion of this bit drives sleep into the UDB array for internal UDB test purposes. Assertion does not affect the power switches. This signal drives pulldowns on the write strobes for all configuration memory, inhibiting writes when set. Sleep or sleep_test does not inhibit writes to this bit, allowing it to be cleared once it has been set. Control is split top and bottom. BCTL0_QCLK_EN0[15:8] controls Bank 0 UDB pairs 0-3 and lower half DSI blocks. BCTL0_QCLK_EN3[15:8] controls Bank 0 UDB pairs 4-7 and upper half DSI blocks. The SLEEP_TEST bits in the other BCTLx_QCLK_ENy registers are not used. Sleep assertion drives bus_rdata to zero so bus read transactions will not return data during assertion of certain sleep_test bits. This is only true for assertion of sleep_test in BCTL0_QCLK_EN0 for Bank 0. Default Value: 0 **0x0: DISABLE:** sleep_test is not asserted. **0x1: ENABLE:** sleep_test is asserted.
14	NC0	Spare register bit Default Value: 0
13	WR_CFG_OPT	Select 1/2 clock cycle or full clock cycle generation for bus_last_strobe used in generating write strobes for latches within the UDB. Only one QCLK_ENx register per bank has an active bit. BCTL0_QCLK_EN0[15:8] controls this bit for Bank 0. The WR_CFG_OPT bits in the other BCTLx_QCLK_ENy[15:8] registers are not used. Default Value: 0 **0x0: FULL_CYCLE_STB:** bus_last_strobe is generated for the full final bus_clk cycle of a bus transaction. **0x1: HALF_CYCLE_STB:** bus_last_strobe is generated during the last 1/2 clock cycle of a bus transaction on the negative edge of bus_clk.

(continued)

12	GLB_DSI_WR	Enable global write operation for the DSI routing channels. When this bit is set, the DSI ID select decoding is bypassed and therefore multiple channels can be written to simultaneously. This is designed to support test modes. Control is split top and bottom. BCTL0_QCLK_EN0[15:8] controls lower half DSI blocks. BCTL0_QCLK_EN3[15:8] controls upper half DSI blocks. The GLB_DSI_WR bits in the other BCTLx_QCLK_ENy[15:8] registers are not used. Default Value: 0 **0x0: DISABLE:** Global DSI channel configuration write is disabled. **0x1: ENABLE:** Global DSI channel configuration write is enabled.
11	DISABLE_ROUTE	By default, when this bit is set to '0', the quadrant routing (for 2 channels in the quadrant) are enabled when the global route enable for the bank is set. However, when this bit is set to '1', the routing in the associated quadrant is disabled and is not enabled by the global route enable bit. The routing will remain in a benign state until it is subsequently configured and then enabled by clearing this bit. Default Value: 0 **0x0: DISABLE:** The routing in this quadrant can be enabled with the bank route enable bit. (default) **0x1: ENABLE:** The routing in this quadrant is disabled and held in a benign state.
10	GCH_WR_HI	Enable global write operation for the routing channel with the higher address in the associated quadrant. When enabled, the UDB ID select decoding is bypassed and therefore multiple channels can be written to simultaneously. This is designed to support test modes. Default Value: 0 **0x0: DISABLE:** Global UDB channel configuration write for higher order address is disabled. **0x1: ENABLE:** Global UDB channel configuration write for higher order address is enabled.
9	GCH_WR_LO	Enable global write operation for the routing channel with the lower address in the associated quadrant. When enabled, the UDB ID select decoding is bypassed and therefore multiple channels can be written to simultaneously. This is designed to support test modes. Default Value: 0 **0x0: DISABLE:** Global UDB channel configuration write for lower order address is disabled. **0x1: ENABLE:** Global UDB channel configuration write for lower order address is enabled.
8	BCEN_Q	Bank Clock Enable Control Default Value: 0 **0x0: DISABLE:** Digital Global clock is disabled. **0x1: ENABLE:** Digital Global clock is enabled.
7 : 0	DCEN_Q	Digital clock enable for indexed digital clock for the associated quadrant. Default Value: 0 **0x0: DISABLE:** Disabled **0x1: ENABLE:** Enabled

1.1.11 UDB_BCTL0_QCLK_EN3

Quadrant Digital Clock Enable Registers

Address: 0x400F6016

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DCEN_Q [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	SLEEP_TEST	NC0	WR_CFG_OPT	GLB_DSI_WR	DISABLE_ROUTE	GCH_WR_HI	GCH_WR_LO	BCEN_Q

Bits	Name	Description
15	SLEEP_TEST	Assertion of this bit drives sleep into the UDB array for internal UDB test purposes. Assertion does not affect the power switches. This signal drives pulldowns on the write strobes for all configuration memory, inhibiting writes when set. Sleep or sleep_test does not inhibit writes to this bit, allowing it to be cleared once it has been set. Control is split top and bottom. BCTL0_QCLK_EN0[15:8] controls Bank 0 UDB pairs 0-3 and lower half DSI blocks. BCTL0_QCLK_EN3[15:8] controls Bank 0 UDB pairs 4-7 and upper half DSI blocks. The SLEEP_TEST bits in the other BCTLx_QCLK_ENy registers are not used. Sleep assertion drives bus_rdata to zero so bus read transactions will not return data during assertion of certain sleep_test bits. This is only true for assertion of sleep_test in BCTL0_QCLK_EN0 for Bank 0. Default Value: 0 **0x0: DISABLE:** sleep_test is not asserted. **0x1: ENABLE:** sleep_test is asserted.
14	NC0	Spare register bit Default Value: 0
13	WR_CFG_OPT	Select 1/2 clock cycle or full clock cycle generation for bus_last_strobe used in generating write strobes for latches within the UDB. Only one QCLK_ENx register per bank has an active bit. BCTL0_QCLK_EN0[15:8] controls this bit for Bank 0. The WR_CFG_OPT bits in the other BCTLx_QCLK_ENy[15:8] registers are not used. Default Value: 0 **0x0: FULL_CYCLE_STB:** bus_last_strobe is generated for the full final bus_clk cycle of a bus transaction. **0x1: HALF_CYCLE_STB:** bus_last_strobe is generated during the last 1/2 clock cycle of a bus transaction on the negative edge of bus_clk.

(continued)

12	GLB_DSI_WR	Enable global write operation for the DSI routing channels. When this bit is set, the DSI ID select decoding is bypassed and therefore multiple channels can be written to simultaneously. This is designed to support test modes. Control is split top and bottom. BCTL0_QCLK_EN0[15:8] controls lower half DSI blocks. BCTL0_QCLK_EN3[15:8] controls upper half DSI blocks. The GLB_DSI_WR bits in the other BCTLx_QCLK_ENy[15:8] registers are not used. Default Value: 0 **0x0: DISABLE:** Global DSI channel configuration write is disabled. **0x1: ENABLE:** Global DSI channel configuration write is enabled.
11	DISABLE_ROUTE	By default, when this bit is set to '0', the quadrant routing (for 2 channels in the quadrant) are enabled when the global route enable for the bank is set. However, when this bit is set to '1', the routing in the associated quadrant is disabled and is not enabled by the global route enable bit. The routing will remain in a benign state until it is subsequently configured and then enabled by clearing this bit. Default Value: 0 **0x0: DISABLE:** The routing in this quadrant can be enabled with the bank route enable bit. (default) **0x1: ENABLE:** The routing in this quadrant is disabled and held in a benign state.
10	GCH_WR_HI	Enable global write operation for the routing channel with the higher address in the associated quadrant. When enabled, the UDB ID select decoding is bypassed and therefore multiple channels can be written to simultaneously. This is designed to support test modes. Default Value: 0 **0x0: DISABLE:** Global UDB channel configuration write for higher order address is disabled. **0x1: ENABLE:** Global UDB channel configuration write for higher order address is enabled.
9	GCH_WR_LO	Enable global write operation for the routing channel with the lower address in the associated quadrant. When enabled, the UDB ID select decoding is bypassed and therefore multiple channels can be written to simultaneously. This is designed to support test modes. Default Value: 0 **0x0: DISABLE:** Global UDB channel configuration write for lower order address is disabled. **0x1: ENABLE:** Global UDB channel configuration write for lower order address is enabled.
8	BCEN_Q	Bank Clock Enable Control Default Value: 0 **0x0: DISABLE:** Digital Global clock is disabled. **0x1: ENABLE:** Digital Global clock is enabled.
7 : 0	DCEN_Q	Digital clock enable for indexed digital clock for the associated quadrant. Default Value: 0 **0x0: DISABLE:** Disabled **0x1: ENABLE:** Enabled

2 BLE Link Layer (BLELL) Registers

This section discusses the BLELL registers. It lists all the registers in mapping tables, in address order.

2.1 Register Details

Register Name	Address
BLE_BLELL_COMMAND_REGISTER	0x402E1000
BLE_BLELL_EVENT_INTR	0x402E1008
BLE_BLELL_EVENT_ENABLE	0x402E1010
BLE_BLELL_ADV_PARAMS	0x402E1018
BLE_BLELL_ADV_INTERVAL_TIMEOUT	0x402E101C
BLE_BLELL_ADV_INTR	0x402E1020
BLE_BLELL_ADV_NEXT_INSTANT	0x402E1024
BLE_BLELL_SCAN_INTERVAL	0x402E1028
BLE_BLELL_SCAN_WINDOW	0x402E102C
BLE_BLELL_SCAN_PARAM	0x402E1030
BLE_BLELL_SCAN_INTR	0x402E1038
BLE_BLELL_SCAN_NEXT_INSTANT	0x402E103C
BLE_BLELL_INIT_INTERVAL	0x402E1040
BLE_BLELL_INIT_WINDOW	0x402E1044
BLE_BLELL_INIT_PARAM	0x402E1048
BLE_BLELL_INIT_INTR	0x402E1050
BLE_BLELL_INIT_NEXT_INSTANT	0x402E1054
BLE_BLELL_DEVICE_RAND_ADDR_L	0x402E1058
BLE_BLELL_DEVICE_RAND_ADDR_M	0x402E105C
BLE_BLELL_DEVICE_RAND_ADDR_H	0x402E1060
BLE_BLELL_PEER_ADDR_L	0x402E1068
BLE_BLELL_PEER_ADDR_M	0x402E106C
BLE_BLELL_PEER_ADDR_H	0x402E1070
BLE_BLELL_WL_ADDR_TYPE	0x402E1078
BLE_BLELL_WL_ENABLE	0x402E107C
BLE_BLELL_TRANSMIT_WINDOW_OFFSET	0x402E1080
BLE_BLELL_TRANSMIT_WINDOW_SIZE	0x402E1084

Register Name	Address
BLE_BLELL_DATA_CHANNELS_L0	0x402E1088
BLE_BLELL_DATA_CHANNELS_M0	0x402E108C
BLE_BLELL_DATA_CHANNELS_H0	0x402E1090
BLE_BLELL_DATA_CHANNELS_L1	0x402E1098
BLE_BLELL_DATA_CHANNELS_M1	0x402E109C
BLE_BLELL_DATA_CHANNELS_H1	0x402E10A0
BLE_BLELL_CONN_INTR	0x402E10A8
BLE_BLELL_CONN_STATUS	0x402E10AC
BLE_BLELL_CONN_INDEX	0x402E10B0
BLE_BLELL_WAKEUP_CONFIG	0x402E10B8
BLE_BLELL_WAKEUP_CONTROL	0x402E10C0
BLE_BLELL_CLOCK_CONFIG	0x402E10C4
BLE_BLELL_TIM_COUNTER_L	0x402E10C8
BLE_BLELL_POC_REG__TIM_CONTROL	0x402E10D8
BLE_BLELL_ADV_TX_DATA_FIFO	0x402E10E0
BLE_BLELL_ADV_SCN_RSP_TX_FIFO	0x402E10E8
BLE_BLELL_INIT_SCN_ADV_RX_FIFO	0x402E10F8
BLE_BLELL_CONN_INTERVAL	0x402E1100
BLE_BLELL_SUP_TIMEOUT	0x402E1104
BLE_BLELL_SLAVE_LATENCY	0x402E1108
BLE_BLELL_CE_LENGTH	0x402E110C
BLE_BLELL_PDU_ACCESS_ADDR_L_REGISTER	0x402E1110
BLE_BLELL_PDU_ACCESS_ADDR_H_REGISTER	0x402E1114
BLE_BLELL_CONN_CE_INSTANT	0x402E1118
BLE_BLELL_CE_CNFG_STS_REGISTER	0x402E111C
BLE_BLELL_NEXT_CE_INSTANT	0x402E1120
BLE_BLELL_CONN_CE_COUNTER	0x402E1124
BLE_BLELL_DATA_LIST_SENT_UPDATE__STATUS	0x402E1128
BLE_BLELL_DATA_LIST_ACK_UPDATE__STATUS	0x402E112C
BLE_BLELL_DATA_MEM_DESCRIPTOR0	0x402E1140
BLE_BLELL_DATA_MEM_DESCRIPTOR1	0x402E1144
BLE_BLELL_DATA_MEM_DESCRIPTOR2	0x402E1148
BLE_BLELL_DATA_MEM_DESCRIPTOR3	0x402E114C
BLE_BLELL_DATA_MEM_DESCRIPTOR4	0x402E1150
BLE_BLELL_WINDOW_WIDEN_INTVL	0x402E1160
BLE_BLELL_WINDOW_WIDEN_WINOFF	0x402E1164
BLE_BLELL_LE_RF_TEST_MODE	0x402E1170
BLE_BLELL_DTM_RX_PKT_COUNT	0x402E1174
BLE_BLELL_TXRX_HOP	0x402E1188
BLE_BLELL_TX_RX_ON_DELAY	0x402E1190
BLE_BLELL_DEV_PUB_ADDR_L	0x402E11C0
BLE_BLELL_DEV_PUB_ADDR_M	0x402E11C4

Register Name	Address
BLE_BLELL_DEV_PUB_ADDR_H	0x402E11C8
BLE_BLELL_ADV_CH_TX_POWER	0x402E11CC
BLE_BLELL_OFFSET_TO_FIRST_INSTANT	0x402E11D0
BLE_BLELL_ADV_CONFIG	0x402E11D4
BLE_BLELL_SCAN_CONFIG	0x402E11D8
BLE_BLELL_INIT_CONFIG	0x402E11DC
BLE_BLELL_CONN_CONFIG	0x402E11E0
BLE_BLELL_CONN_CH_TX_POWER	0x402E11E4
BLE_BLELL_CONN_PARAM1	0x402E11E8
BLE_BLELL_CONN_PARAM2	0x402E11EC
BLE_BLELL_CONN_INTR_MASK	0x402E11F0
BLE_BLELL_SLAVE_TIMING_CONTROL	0x402E11F4
BLE_BLELL_RECEIVE_TRIG_CTRL	0x402E11F8
BLE_BLELL_DPLL_CONFIG	0x402E1258
BLE_BLELL_WHITELIST_BASE_ADDR	0x402E1340
BLE_BLELL_CONN_UPDATE_NEW_INTERVAL	0x402E13A4
BLE_BLELL_CONN_UPDATE_NEW_LATENCY	0x402E13A8
BLE_BLELL_CONN_UPDATE_NEW_SUP_TO	0x402E13AC
BLE_BLELL_CONN_UPDATE_NEW_SL_INTERVAL	0x402E13B0
BLE_BLELL_CONN_REQ_WORD0	0x402E13C0
BLE_BLELL_CONN_REQ_WORD1	0x402E13C4
BLE_BLELL_CONN_REQ_WORD2	0x402E13C8
BLE_BLELL_CONN_REQ_WORD3	0x402E13CC
BLE_BLELL_CONN_REQ_WORD4	0x402E13D0
BLE_BLELL_CONN_REQ_WORD5	0x402E13D4
BLE_BLELL_CONN_REQ_WORD6	0x402E13D8
BLE_BLELL_CONN_REQ_WORD7	0x402E13DC
BLE_BLELL_CONN_REQ_WORD8	0x402E13E0
BLE_BLELL_CONN_REQ_WORD9	0x402E13E4
BLE_BLELL_CONN_REQ_WORD10	0x402E13E8
BLE_BLELL_CONN_REQ_WORD11	0x402E13EC
BLE_BLELL_PACKET_COUNTER0	0x402E1400
BLE_BLELL_PACKET_COUNTER1	0x402E1404
BLE_BLELL_PACKET_COUNTER2	0x402E1408
BLE_BLELL_IV_MASTER0	0x402E1410
BLE_BLELL_IV_MASTER1	0x402E1414
BLE_BLELL_IV_SLAVE0	0x402E1418
BLE_BLELL_IV_SLAVE1	0x402E141C
BLE_BLELL_ENC_KEY0	0x402E1420
BLE_BLELL_ENC_KEY1	0x402E1424
BLE_BLELL_ENC_KEY2	0x402E1428
BLE_BLELL_ENC_KEY3	0x402E142C

Register Name	Address
BLE_BLELL_ENC_KEY4	0x402E1430
BLE_BLELL_ENC_KEY5	0x402E1434
BLE_BLELL_ENC_KEY6	0x402E1438
BLE_BLELL_ENC_KEY7	0x402E143C
BLE_BLELL_DATA0	0x402E1440
BLE_BLELL_DATA1	0x402E1444
BLE_BLELL_DATA2	0x402E1448
BLE_BLELL_DATA3	0x402E144C
BLE_BLELL_DATA4	0x402E1450
BLE_BLELL_DATA5	0x402E1454
BLE_BLELL_DATA6	0x402E1458
BLE_BLELL_DATA7	0x402E145C
BLE_BLELL_DATA8	0x402E1460
BLE_BLELL_DATA9	0x402E1464
BLE_BLELL_DATA10	0x402E1468
BLE_BLELL_DATA11	0x402E146C
BLE_BLELL_DATA12	0x402E1470
BLE_BLELL_DATA13	0x402E1474
BLE_BLELL_MIC_IN0	0x402E1478
BLE_BLELL_MIC_IN1	0x402E147C
BLE_BLELL_MIC_OUT0	0x402E1480
BLE_BLELL_MIC_OUT1	0x402E1484
BLE_BLELL_ENC_PARAMS	0x402E1488
BLE_BLELL_ENC_CONFIG	0x402E1490
BLE_BLELL_ENC_INTR_EN	0x402E1498
BLE_BLELL_ENC_INTR	0x402E14A0
BLE_BLELL_CONN_TXMEM_BASE_ADDR	0x402E1600
BLE_BLELL_CONN_RXMEM_BASE_ADDR	0x402E1800
BLE_BLELL_PDU_RESP_TIMER	0x402E1A04
BLE_BLELL_NEXT_RESP_TIMER_EXP	0x402E1A08
BLE_BLELL_NEXT_SUP_TO	0x402E1A0C
BLE_BLELL_LLH_FEATURE_CONFIG	0x402E1A10
BLE_BLELL_WIN_MIN_STEP_SIZE	0x402E1A14
BLE_BLELL_SLV_WIN_ADJ	0x402E1A18
BLE_BLELL_SL_CONN_INTERVAL	0x402E1A1C
BLE_BLELL_LE_PING_TIMER_ADDR	0x402E1A20
BLE_BLELL_LE_PING_TIMER_OFFSET	0x402E1A24
BLE_BLELL_LE_PING_TIMER_NEXT_EXP	0x402E1A28
BLE_BLELL_LE_PING_TIMER_WRAP_COUNT	0x402E1A2C
BLE_BLELL_TX_EN_EXT_DELAY	0x402E1E00
BLE_BLELL_TX_RX_SYNTH_DELAY	0x402E1E04

2.1.1 BLE_BLELL_COMMAND_REGISTER

Instruction Register

Address: 0x402E1000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	COMMAND [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description

(continued)

7 : 0	COMMAND	8-bit command from firmware to the link layer controller. See below for the list of instructions and their opcodes. The instruction results in the link layer hardware starting/stopping an operation. Notes on use Few of the commands will require other configuration registers to be set, before the command is written. Refer to the description below for details of the registers to be set before setting these instructions. ---------- Command Opcode Description START_ADV - 0x40: Start Advertiser operation. The associated Advertiser configuration registers are pro-grammed before the command is issued. [refer to llh_set_adv_parameters function in lec_llh/simulation/ llh_driver/ll_hardware_api.c file] STOP_ADV - 0x41: Stop advertiser operation. START_SCAN - 0x42: Start scanner operation. The associated configuration registers must be programmed before the command is issued. [refer to llh_set_scan_parameters function in lec_llh/simulation/llh_driver/ ll_hardware_api.c file] STOP_SCAN - 0x43: Stop the scanner operation. START_INIT - 0x44: Start connection creation operation. The associated configuration registers must be pro-grammed before the command is issued. [refer to create_connection function in lec_llh/simulation/llh_driver/ ll_hardware_api.c file] STOP_INIT - 0x45: Cancel connection creation operation. DTM_TX_START - 0x46: Start Direct Test Mode Transmit Test. The associated configuration registers must be programmed before the command is issued. [refer to dtm_tx_test function in lec_llh/simulation/llh_driver/ ll_hardware_api.c file] DTM_RX_START - 0x47: Start Direct Test Mode Receive Test. The associated configuration registers must be programmed before the command is issued. [refer to dtm_rx_test function in lec_llh/simulation/llh_driver/ ll_hardware_api.c file] DTM_STOP - 0x48: Stop Direct Test Mode. UPDATE_CHAN_MAP - 0x4B: Update channel map for the connection. UPDATE_CONN_PROC - 0x4C: Start connection update procedure for the connection. PACKET_RECEIVED - 0x4D: Indicates a received connection packet is read by firmware from connection receive FIFO. ENTER_DSM - 0x50: Enter deep sleep mode. CORE_CLK_OFF - 0x51: Enter sleep mode. CORE_CLK_ON - 0x52: Exit sleep mode ENC_CLK_ON - 0x53: Turn on clock to encryption block ENC_CLK_OFF - 0x54: Turn off clock to encryption block ADV_CLK_ON - 0x55: Turn on clock to advertiser block in NAP mode. ADV_CLK_OFF - 0x56: Turn off clock to advertiser block in NAP mode. SCAN_CLK_ON - 0x57: Turn on clock to scanner block in NAP mode. SCAN_CLK_OFF - 0x58: Turn off clock to scanner block in NAP mode. INIT_CLK_ON - 0x59: Turn on clock to initiator block in NAP mode. INIT_CLK_OFF - 0x5a: Turn off clock to initiator block in NAP mode. CONN_CLK_ON - 0x5b: Turn on clock to connection block in NAP mode. CONN_CLK_OFF - 0x5c: Turn off clock to connection block in NAP mode. UPDATE_CONN - 0x68: Update connection parameters. Deprecated. KILL_CONN - 0x70: Kill connection immediately. KILL_CONN_AFTER_TX - 0x71: Kill connection after a transmit operation is over. RESP_TIMER_ON - 0x72: Start PDU response timer. The PDU_RESP_TIMER register must be pro-grammed with timeout value before issuing this command. RESP_TIMER_OFF - 0x73: Stop PDU response timer. RESET_READ_PTR - 0x74: Reset the white list memory read pointer to 0. CONN_PING_TIMER_ON - 0x75: Start connection ping timer CONN_PING_TIMER_OFF - 0x076: Stop connection ping timer SOFT_RESET - 0x80: Software reset. Resets all the hardware registers (except a few registers related to radio initializa-tion). RESET_US_COUNTER - 0xC3: Reset microsecond counter Default Value: 0

2.1.2 BLE_BLELL_EVENT_INTR

Event(Interrupt) status and Clear register

Address: 0x402E1008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	R	RW1C	RW1C	R	R	R	R
HW Access	None	RW	RW	RW	RW	RW	RW	RW
Name	None	ENC_INTR	DSM_INTR	SM_INTR	CONN_INTR	INIT_INTR	SCAN_INTR	ADV_INTR

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
6	ENC_INTR	Encryption module interrupt. Default Value: 0
5	DSM_INTR	Read: Deep sleep mode exit interrupt. This bit is set, when link layer hardware exits from deep sleep mode. Write: Clear deep sleep mode exit interrupt. Write to the register with this bit set to 1, clears the interrupt source. Default Value: 0
4	SM_INTR	Read: Sleep-mode-exit interrupt. This bit is set, when link layer hardware exits from sleep mode. Write: Clear sleep-mode-exit interrupt. Write to the register with this bit set to 1, clears the interrupt source. Default Value: 0
3	CONN_INTR	Connection interrupt. If bit is set to 1, it indicates an event occurred in the connection operation. This interrupt is aggregation of interrupts for all the connections. The source of the event for the specific connection, needs to be read from the CONN_INTR register specific to the connection. This bit is cleared, when firmware clears ALL interrupts by writing to the CONN_INTR register. Default Value: 0

(continued)

2	INIT_INTR	Initiator interrupt. If bit is set to 1, it indicates an event occurred in the initiating procedure. The source of the event needs to be read from the INIT_INTR register. This bit is cleared, when firmware clears ALL interrupts by writing to the INIT_INTR register. Default Value: 0
1	SCAN_INTR	Scanner interrupt. If bit is set to 1, it indicates an event occurred in the scanning procedure. The source of the event needs to be read from the SCAN_INTR register. This bit is cleared, when firmware clears ALL interrupts by writing to the SCAN_INTR register. Default Value: 0
0	ADV_INTR	Advertiser interrupt. If bit is set to 1, it indicates an event occurred in the advertising procedure. The source of the event needs to be read from the ADV_INTR register. This bit is cleared, when firmware clears ALL interrupts by writing to the ADV_INTR register. Default Value: 0

2.1.3 BLE_BLELL_EVENT_ENABLE

Event indications enable.

Address: 0x402E1010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	RW	RW	RW	RW	RW	RW
HW Access	None	R	R	R	R	R	R	R
Name	None	ENC_INT_EN	DSM_INT_EN	SM_INT_EN	CONN_INT_EN	INIT_INT_EN	SCN_INT_EN	ADV_INT_EN

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
6	ENC_INT_EN	Encryption module interrupt enable. 1 Enable encryption module interrupt to firmware. 0 disable encryption module interrupt to firmware. Default Value: 0
5	DSM_INT_EN	Deep Sleep-mode-exit interrupt enable. 1 enable deep sleep mode exit event to interrupt the firmware. 0 disable deep sleep mode exit interrupt to firmware. Default Value: 0
4	SM_INT_EN	Sleep-mode-exit interrupt enable. 1 enable sleep mode exit event to interrupt the firmware. 0 disable sleep mode exit interrupt to firmware. Default Value: 0
3	CONN_INT_EN	Connection interrupt enable. 1 enable connection procedure to interrupt the firmware. 0 disable connection procedure interrupt to firmware. Default Value: 0

(continued)

2	INIT_INT_EN	Initiator interrupt enable. 1 enable initiator procedure to interrupt the firmware. 0 disable initiator procedure interrupt to firmware. Default Value: 0
1	SCN_INT_EN	Scanner interrupt enable. 1 enable scan procedure to interrupt the firmware. 0 disable scan procedure interrupt to firmware. Default Value: 0
0	ADV_INT_EN	Advertiser interrupt enable. 1 enable advertiser procedure to interrupt the firmware. 0 disable advertiser procedure interrupt to firmware. Default Value: 0

2.1.4 BLE_BLELL_ADV_PARAMS

Advertising parameters register.

Address: 0x402E1018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW			RW		RW		RW
HW Access	R			R		R		R
Name	ADV_CHANNEL_MAP [7:5]			ADV_FILT_POLICY [4:3]		ADV_TYPE [2:1]		TX_ADDR

Bits	15	14	13	12	11	10	9	8
SW Access	R	None				RW	None	RW
HW Access	RW	None				R	None	R
Name	RCV_TX_ADDR	None [14:11]				ADV_LOW_DUTY_CYCLE	None	RX_ADDR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15	RCV_TX_ADDR	Transmit address field of the received packet extracted from the receive packet. This field is used by firmware to report peer_addr_type parameter in the connection complete event. Default Value: 0
10	ADV_LOW_DUTY_CYCLE	This bit field is used to specify to the Controller the Low Duty Cycle connectable directed advertising variant being used. 1 Low Duty Cycle Connectable Directed Advertising. 0 High Duty Cycle Connectable Directed Advertising. Default Value: 0
8	RX_ADDR	Peer addresses type. This is the Direct_Address_type field programmed, only if ADV_DIRECT_IND type is sent. 1 Rx addr type is random. 0 Rx addr type is public Default Value: 0

(continued)

7 : 5	ADV_CHANNEL_MAP	Advertising channel map indicates the advertising channels used for advertising. By setting the bit, corresponding channel is enabled for use. Atleast one channel bit should be set. 7 - enable channel 39. 6 - enable channel 38. 5 - enable channel 37. Default Value: 7
4 : 3	ADV_FILT_POLICY	Advertising filter policy. The set of devices that the advertising procedure uses for device filtering is called the White List. 0x0 - Allow scan request from any device, allow connect request from any device. 0x1 - Allow scan request from devices in white list only, allow connect request from any device. 0x2 - Allow scan request from any device, allow connect request from devices in white list only. 0x3 - Allow scan request from devices in white list only, allow connect request from devices in white list only. Default Value: 0
2 : 1	ADV_TYPE	The Advertising type is used to determine the packet type that is used for advertising when advertising is enabled. 0x0 - Connectable undirected advertising. (adv_ind) 0x1 - Connectable directed advertising (adv_direct_ind). 0x2 - Discoverable undirected advertising (adv_discover_ind) 0x3 - Non connectable undirected advertising (adv_nonconn_ind). Default Value: 0
0	TX_ADDR	Device own address type. 1 - Address type is random. 0 - Address type is public. Default Value: 0

2.1.5 BLE_BLELL_ADV_INTERVAL_TIMEOUT

Advertising interval register.

Address: 0x402E101C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	ADV_INTERVAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW						
HW Access	None	R						
Name	None	ADV_INTERVAL [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
14 : 0	ADV_INTERVAL	Range: 0x0020 to 0x4000 (For ADV_IND) 0x00A0 to 0x4000 (For ADV_SCAN_IND and NONCONN_IND) Invalid for ADV_DIRECT_IND Time = N * 0.625 msec Time Range: 20 ms to 10.24 sec. For directed advertising, firmware programs the default value of 1.28 seconds. Default Value: 32

2.1.6 BLE_BLELL_ADV_INTR

Advertising interrupt status and Clear register

Address: 0x402E1020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	ADV_TIMEOUT	SLV_CONNECTED	CONN_REQ_RX_INTR	SCAN_REQ_RX_INTR	SCAN_RSP_TX_INTR	ADV_TX_INTR	ADV_CLOSE_INTR	ADV_STRT_INTR

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							RW
Name	None [15:9]							ADV_ON

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	ADV_ON	Advertiser procedure is ON in hardware. Indicates that advertiser procedure is ON in hardware. 1 - ON 0 - OFF Default Value: 0
7	ADV_TIMEOUT	If this bit is set it indicates that the directed advertising event has timed out after 1.28 seconds. Applicable in adv_direct_ind advertising. Write to the register with this bit set to 1, clears the interrupt source. Default Value: 0
6	SLV_CONNECTED	If this bit is set it indicates that connection is created as slave. Write to the register with this bit set to 1, clears the interrupt source. Default Value: 0
5	CONN_REQ_RX_INTR	If this bit is set it indicates connect request packet is received. Write to the register with this bit set to 1, clears the interrupt source. Default Value: 0

(continued)

4	SCAN_REQ_RX_INTR	If this bit is set it indicates scan request packet received. Write to the register with this bit set to 1, clears the interrupt source. Default Value: 0
3	SCAN_RSP_TX_INTR	If this bit is set it indicates scan response packet transmitted in response to previous scan request packet received. Write to the register with this bit set to 1, clears the interrupt source. Default Value: 0
2	ADV_TX_INTR	If this bit is set it indicates ADV packet is transmitted. Write to the register with this bit set to 1, clears the interrupt source. Default Value: 0
1	ADV_CLOSE_INTR	If this bit is set it indicates current advertising event is closed. Write to the register with this bit set to 1, clears the interrupt source. Default Value: 0
0	ADV_STRT_INTR	If this bit is set it indicates a new advertising event started after interval expiry. Write to the register with this bit set to 1, clears the interrupt source. Default Value: 0

2.1.7 BLE_BLELL_ADV_NEXT_INSTANT

Advertising next instant.

Address: 0x402E1024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	ADV_NEXT_INSTANT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	ADV_NEXT_INSTANT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	ADV_NEXT_INSTANT	Shows the next start of advertising event with reference to the internal reference clock. Default Value: 0

2.1.8 BLE_BLELL_SCAN_INTERVAL

Scan Interval Register

Address: 0x402E1028

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SCAN_INTERVAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	SCAN_INTERVAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	SCAN_INTERVAL	Scan interval register. Interval between two consecutive scanning events. Firmware sets the scanning interval value to this register before issuing start scan command. Range: 0x0004 to 0x4000 Default: 0x0010 (10 ms) Time = N * 0.625 msec Time Range: 2.5 msec to 10.24 sec. Default Value: 16

2.1.9 BLE_BLELL_SCAN_WINDOW

Scan window Register

Address: 0x402E102C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SCAN_WINDOW [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	SCAN_WINDOW [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	SCAN_WINDOW	Duration of scan in a scanning event, which should be less than or equal to scan interval value. Firmware sets the scan window value to this register before issuing start scan command. Range: 0x0004 to 0x4000 Default: 0x0010 (10 ms) Time = N * 0.625 msec Time Range: 2.5 msec to 10.24 sec. Default Value: 16

2.1.10 BLE_BLELL_SCAN_PARAM

Scanning parameters register

Address: 0x402E1030

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW		RW		RW
HW Access	None		R	R		R		R
Name	None [7:6]		DUP_FILT_EN	SCAN_FILT_POLICY [4:3]		SCAN_TYPE [2:1]		TX_ADDR

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	DUP_FILT_EN	Filter duplicate packets. 1- Duplicate filtering enabled. 0- Duplicate filtering not enabled. This field is derived from the LE_set_scan_enable command. Default Value: 0
4 : 3	SCAN_FILT_POLICY	The scanner filter policy determines how the scanner processes advertising packets. 0x00 - Accept advertising packets from any device. 0x01 - Accept advertising packets from only devices in the whitelist. 0x10 - RFU 0x11 - RFU Adv_direct_ind packets which are not addressed to this device are ignored. Default Value: 0
2 : 1	SCAN_TYPE	0x00 - passive scanning.(default) 0x01 - active scanning. 0x10 - RFU 0x11 - RFU Default Value: 0

(continued)

0	TX_ADDR	Devices own address type. 1 - addr type is random. 0 - addr type is public. Default Value: 0

2.1.11 BLE_BLELL_SCAN_INTR

Scan interrupt status and Clear register

Address: 0x402E1038

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	None			RW	RW	RW	RW	RW
Name	None [7:5]			SCAN_RSP_RX_INTR	ADV_RX_INTR	SCAN_TX_INTR	SCAN_CLOSE_INTR	SCAN_START_INTR

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							RW
Name	None [15:9]							SCAN_ON

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	SCAN_ON	Scan procedure status. 1 scan procedure is active. 0 scan procedure is not active. Default Value: 0
4	SCAN_RSP_RX_INTR	If this bit is set it indicates SCAN_RSP packet is received. Firmware can read the content of the packet from the INIT_SCN_ADV_RX_FIFO. Write to the register with this bit set to 1, clears the interrupt source. NOTE: This interrupt is generated while active scanning upon receiving scan response packet. Default Value: 0
3	ADV_RX_INTR	If this bit is set it indicates ADV packet received. Firmware can read the content of the packet from the INIT_SCN_ADV_RX_FIFO. Write to the register with this bit set to 1, clears the interrupt source. This interrupt is generated while active/passive scanning upon receiving adv packets. Default Value: 0
2	SCAN_TX_INTR	If this bit is set it indicates scan request packet is transmitted. Write to the register with this bit set to 1, clears the interrupt source. Default Value: 0

(continued)

1	SCAN_CLOSE_INTR	If this bit is set it indicates scan window is closed. Write to the register with this bit set to 1, clears the interrupt source. Default Value: 0
0	SCAN_STRT_INTR	If this bit is set it indicates scan window is opened. Write to the register with this bit set to 1, clears the interrupt source. Default Value: 0

2.1.12 BLE_BLELL_SCAN_NEXT_INSTANT

Advertising next instant.

Address: 0x402E103C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	NEXT_SCAN_INSTANT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	NEXT_SCAN_INSTANT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	NEXT_SCAN_INSTANT	Shows the instant with respect to internal reference clock of resolution 625 us at which next scanning event begins. Default Value: 0

2.1.13 BLE_BLELL_INIT_INTERVAL

Initiator Interval Register

Address: 0x402E1040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	INIT_SCAN_INTERVAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INIT_SCAN_INTERVAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	INIT_SCAN_INTERVAL	Initiator interval register. Firmware sets the initiators scanning interval value to this regis-ter before issuing create connection command. Interval between two consecutive scanning events. Range: 0x0004 to 0x4000 Time = N * 0.625 msec Time Range: 2.5 msec to 10.24 sec. Default Value: 0

2.1.14 BLE_BLELL_INIT_WINDOW

Initiator window Register

Address: 0x402E1044

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	INIT_SCAN_WINDOW [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INIT_SCAN_WINDOW [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	INIT_SCAN_WINDOW	Duration of scan in a scanning event, which should be less than or equal to scan interval value. Firmware sets the scan window value to this register before issuing create connection command. Range: 0x0004 to 0x4000 Time = N * 0.625 msec Time Range: 2.5 msec to 10.24 sec. Default Value: 0

2.1.15 BLE_BLELL_INIT_PARAM

Initiator parameters register

Address: 0x402E1048

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	None	RW	RW
HW Access	None				R	None	R	R
Name	None [7:4]				INIT_FILT_POLICY	None	RX_ADDR__RX_TX_ADDR	TX_ADDR

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	INIT_FILT_POLICY	The Initiator_Filter_Policy is used to determine whether the White List is used or not. 0 - White list is not used to determine which advertiser to connect to. Instead the Peer_Address_Type and Peer Address fields are used to specify the address type and address of the advertising device to connect to. 1 - White list is used to determine the advertising device to connect to. Peer_Address_Type and Peer_Address fields are ignored when whitelist is used. Default Value: 0
1	RX_ADDR__RX_TX_ADDR	Peer address type. The rx_addr field is updated by the receiver with the address type of the received connectable advertising packet. 1 - addr type is random. 0 - addr type is public. Default Value: 0
0	TX_ADDR	Device own address type. 1 - addr type is random. 0 - addr type is public. Default Value: 0

2.1.16 BLE_BLELL_INIT_INTR

Scan interrupt status and Clear register

Address: 0x402E1050

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW1C	None	RW1C	RW1C	RW1C
HW Access	None			RW	None	RW	RW	RW
Name	None [7:5]			MASTER_CONN_CREATED	None	INIT_TX_START_INTR	INIT_CLOSE_WINDOW_INR	INIT_INTERVAL_EXPIRE_INTR

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4	MASTER_CONN_CREATED	If this bit is set it indicates connection is created as master. Write to the register with this bit set to 1, clears the interrupt source. Default Value: 0
2	INIT_TX_START_INTR	If this bit is set it indicates initiator packet (CONREQ) transmission has started. Write to the register with this bit set to 1, clears the interrupt source. Default Value: 0
1	INIT_CLOSE_WINDOW_INR	If this bit is set it indicates initiator scan window has finished. Write to the register with this bit set to 1, clears the interrupt source. Default Value: 0
0	INIT_INTERVAL_EXPIRE_INTR	If this bit is set it indicates initiator scan window has started. Write to the register with this bit set to 1, clears the interrupt source. Default Value: 0

2.1.17 BLE_BLELL_INIT_NEXT_INSTANT

Initiator next instant.

Address: 0x402E1054

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	INIT_NEXT_INSTANT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	INIT_NEXT_INSTANT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	INIT_NEXT_INSTANT	Shows the instant with respect to internal reference clock of resolution 625 us at which next initiator scanning event begins. Default Value: 0

2.1.18 BLE_BLELL_DEVICE_RAND_ADDR_L

Lower 16 bit random address of the device.

Address: 0x402E1058

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DEVICE_RAND_ADDR_L [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DEVICE_RAND_ADDR_L [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DEVICE_RAND_ADDR_L	Lower 16 bit of 48-bit random address of the device. Default Value: 0

2.1.19 BLE_BLELL_DEVICE_RAND_ADDR_M

Middle 16 bit random address of the device.

Address: 0x402E105C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DEVICE_RAND_ADDR_M [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DEVICE_RAND_ADDR_M [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DEVICE_RAND_ADDR_M	Middle 16 bit of 48-bit random address of the device. Default Value: 0

2.1.20 BLE_BLELL_DEVICE_RAND_ADDR_H

Higher 16 bit random address of the device.

Address: 0x402E1060

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DEVICE_RAND_ADDR_H [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DEVICE_RAND_ADDR_H [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DEVICE_RAND_ADDR_H	Higher 16 bit of 48-bit random address of the device. Default Value: 0

2.1.21 BLE_BLELL_PEER_ADDR_L

Lower 16 bit address of the peer device.

Address: 0x402E1068

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	PEER_ADDR_L [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PEER_ADDR_L [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	PEER_ADDR_L	Lower 16 bit of 48-bit address of the peer device. Default Value: 0

2.1.22 BLE_BLELL_PEER_ADDR_M

Middle 16 bit address of the peer device.

Address: 0x402E106C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	PEER_ADDR_M [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PEER_ADDR_M [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	PEER_ADDR_M	Middle 16 bit of 48-bit address of the peer device. Default Value: 0

2.1.23 BLE_BLELL_PEER_ADDR_H

Higher 16 bit address of the peer device.

Address: 0x402E1070

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	PEER_ADDR_H [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PEER_ADDR_H [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	PEER_ADDR_H	Higher 16 bit of 48-bit address of the peer device. The peer address registers are used for multiple purposes. The register is written by firmware to provide the peer address to be used for a hardware procedure. When firmware reads the register, it reads back peer address values updated by hardware. While doing directed Advertising, the firmware writes the peer address of the device specified by the Di-rect_Address parameter of the LE_Set_Advertising_Parameters command. While device is configured as an initiator without white list filtering, the peer address specified in the peer_address field of the create connection command is programmed into this register, which is used by hard-ware procedures. While device is configured as an initiator and white list is enabled, firmware can read this register to get the address of the peer device from which connectable ADV packet was received and to which the connection is created. When a connection is created as a slave, the firmware can read this register to get the address of the peer de-vice to which connection is created. Default Value: 0

2.1.24 BLE_BLELL_WL_ADDR_TYPE

whitelist address type

Address: 0x402E1078

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	WL_ADDR_TYPE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	WL_ADDR_TYPE	8 address type bits corresponding to the device address stored. 1 - Address type is random. 0 - Address type is public. Default Value: 0

2.1.25 BLE_BLELL_WL_ENABLE

whitelist valid entry bit

Address: 0x402E107C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	WL_ENABLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	WL_ENABLE	Stores the valid entry bit corresponding to each of the eight device address stored in the whitelist. 1 - White list entry is Valid 0 - White list entry is Invalid Default Value: 0

2.1.26 BLE_BLELL_TRANSMIT_WINDOW_OFFSET

Transmit window offset

Address: 0x402E1080

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	TX_WINDOW_OFFSET [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	TX_WINDOW_OFFSET [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	TX_WINDOW_OFFSET	This is used to determine the first anchor point for the master transmission, from the time of connection creation. Range: This shall be a multiple of 1.25 ms in the range of 0 ms to connInterval value. Default Value: 0

2.1.27 BLE_BLELL_TRANSMIT_WINDOW_SIZE

Transmit window size

Address: 0x402E1084

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	TX_WINDOW_SIZE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	TX_WINDOW_SIZE	window_size along with the window_offset is used to calculate the first connection point anchor point for the master. This shall be a multiple of 1.25 ms in the range of 1.25 ms to the lesser of 10 ms and (connInterval 1.25 ms). Values range from 0 to 10 ms. Default Value: 0

2.1.28 BLE_BLELL_DATA_CHANNELS_L0

Data channel map 0 (lower word)

Address: 0x402E1088

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA_CHANNELS_L0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA_CHANNELS_L0 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATA_CHANNELS_L0	This register field indicates which of the data channels are in use. This stores the information for the lower 16 (15:0) data channel indices. 1 indicates the corresponding data channel is used and 0 indicates the channel is unused. Default Value: 0

2.1.29 BLE_BLELL_DATA_CHANNELS_M0

Data channel map 0 (middle word)

Address: 0x402E108C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA_CHANNELS_M0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DATA_CHANNELS_M0 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATA_CHANNELS_M0	This register field indicates which of the data channels are in use. This stores the information for the middle 16 (32:16) data channel indices. 1 indicates the corresponding data channel is used and 0 indicates the channel is unused. Default Value: 0

2.1.30 BLE_BLELL_DATA_CHANNELS_H0

Data channel map 0 (upper word)

Address: 0x402E1090

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:5]				DATA_CHANNELS_H0 [4:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4 : 0	DATA_CHANNELS_H0	This register field indicates which of the data channels are in use. This stores the information for the upper 5 (36:32) data channel indices. 1 indicates the corresponding data channel is used and 0 indicates the channel is unused. Note: The Data channel map 0 and data channel map 1 are two sets of channel maps stored, common for all the connections. At any given time, only two maps can be maintained and the connections will use one of the two sets as indicated by the channel map index field in the CE_CNFG_STS registers specific to the link. Firmware must also manage to update this field along with the map. Default Value: 0

2.1.31 BLE_BLELL_DATA_CHANNELS_L1

Data channel map 1 (lower word)

Address: 0x402E1098

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA_CHANNELS_L1 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DATA_CHANNELS_L1 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATA_CHANNELS_L1	This register field indicates which of the data channels are in use. This stores the information for the lower 16 (15:0) data channel indices. 1 indicates the corresponding data channel is used and 0 indicates the channel is unused. Default Value: 0

2.1.32 BLE_BLELL_DATA_CHANNELS_M1

Data channel map 1 (middle word)

Address: 0x402E109C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA_CHANNELS_M1 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DATA_CHANNELS_M1 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATA_CHANNELS_M1	This register field indicates which of the data channels are in use. This stores the information for the middle 16 (32:16) data channel indices. 1 indicates the corresponding data channel is used and 0 indicates the channel is unused. Default Value: 0

2.1.33 BLE_BLELL_DATA_CHANNELS_H1

Data channel map 1 (upper word)

Address: 0x402E10A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:5]				DATA_CHANNELS_H1 [4:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4 : 0	DATA_CHANNELS_H1	This register field indicates which of the data channels are in use. This stores the information for the upper 5 data channel indices. 1 indicates the corresponding data channel is used and 0 indicates the channel is unused. Note: The Data channel map 0 and data channel map 1 are two sets of channel maps stored, common for all the connections. At any given time, only two maps can be maintained and the connections will use one of the two sets as indicated by the channel map index field in the CE_CNFG_STS registers specific to the link. Firmware must also manage to update this field along with the map. Default Value: 0

2.1.34 BLE_BLELL_CONN_INTR

Connection interrupt status and Clear register

Address: 0x402E10A8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	CON_UPDT_DONE	CE_RX	CE_TX_ACK	CLOSE_CE	START_CE	MAP_UPDT_DONE	CONN_ESTB	CONN_CLOSED

Bits	15	14	13	12	11	10	9	8
SW Access	R	R	R			R		
HW Access	RW	RW	RW			RW		
Name	PING_NEARLY_EXPIRD_INTR	PING_TIMER_EXPIRD_INTR	RX_PDU_STATUS [13:11]			DISCON_STATUS [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15	PING_NEARLY_EXPIRD_INTR	If this is set, it indicates that ping timer has nearly expired. Default Value: 0
14	PING_TIMER_EXPIRD_INTR	If this is set, it indicates that ping timer has expired. Default Value: 0
13 : 11	RX_PDU_STATUS	Status of PDU received. This information is valid along with receive interrupt. xx1 Bad Packet (packet with CRC error) 000 empty PDU 010 - new data (non-empty) PDU 110 Duplicate Packet Default Value: 0

(continued)

10 : 8	DISCON_STATUS	Reason for disconnect indicates the reason the link is disconnected by hardware. 001 - connection failed to be established 010 - supervision timeout 011 - kill connection by host 100 - kill connection after ACK transmitted 101 - PDU response timer expired Default Value: 0
7	CON_UPDT_DONE	This bit is set when the last connection event with previous connec-tion parameters is reached. The bit is set immediately after the re-ceive operation at the anchor point of the last connection event. If this bit is written with 1, it clears the connection updated interrupt. Default Value: 0
6	CE_RX	If this bit is set it indicates that a packet is received in the connection event. If this bit is written with 1, it clears the connection event received interrupt. Default Value: 0
5	CE_TX_ACK	If this bit is set it indicates that the connection event transmission acknowledgement is received for the previous non-empty packet transmitted. If this bit is written with 1, it clears the ce transmission acknowledgement interrupt. Default Value: 0
4	CLOSE_CE	If this bit is set it indicates that the connection event closed interrupt has happened. If this bit is written with 1, it clears the connection event closed interrupt. Default Value: 0
3	START_CE	If this bit is set it indicates that the connection event started interrupt has happened. If this bit is written with 1, it clears the connection event started interrupt. Default Value: 0
2	MAP_UPDT_DONE	If this bit is set it indicates that the channel map update is completed at the instant specified by the firmware. If this bit is written with 1, it clears the map update done interrupt. Default Value: 0
1	CONN_ESTB	If this bit is set it indicates that the connection has been established. The bit is also set when a connection update procedure is complet-ed, at the start of the first anchor point with the updated parameters. If this bit is written with 1, it clears the connection established interrupt. Default Value: 0
0	CONN_CLOSED	If this bit is set it indicates that the link is disconnected. If this bit is written with 1, it clears the connection updated interrupt. Default Value: 0

2.1.35 BLE_BLELL_CONN_STATUS

Connection channel status

Address: 0x402E10AC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R				None			
HW Access	RW				None			
Name	RECEIVE_PACKET_COUNT [15:12]				None [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 12	RECEIVE_PACKET_COUNT	This field stores the count for the number of receive packets in the receive FIFO that are still not ready by firmware. The counter value is incremented by hardware for every good packet it stores in the FIFO. After firmware reads a packet, it decrements the counter by issuing the PACKET_RECEIVED command from the commander. Default Value: 0

2.1.36 BLE_BLELL_CONN_INDEX

Connection Index register

Address: 0x402E10B0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CONN_INDEX [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CONN_INDEX [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CONN_INDEX	This field is used to index the multiple connections existing. Range is 0 to maximum number of connections supported. For a single connection device, conn_index is 0. Default Value: 0

2.1.37 BLE_BLELL_WAKEUP_CONFIG

Wakeup configuration

Address: 0x402E10B8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	OSC_STARTUP_DELAY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW						None	
HW Access	R						None	
Name	DSM_OFFSET_TO_WAKEUP_INSTANT [15:10]						None [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 10	DSM_OFFSET_TO_WAKEUP_INSTANT	Number of slots before the wake up instant before which the hardware needs to exit from deep sleep mode. The slot is of 0.625ms period. This is a onetime configuration field, which is used every time hardware does an auto-wakeup before the next wakeup instant. Default Value: 0
7 : 0	OSC_STARTUP_DELAY	Oscillator stabilization/startup delay. This is in X.Y for-mat where X is in terms of number of BT slots (625 us) and Y is in terms of number of clock periods of 16KHz clock input, required for RF oscillator to stabilize the clock output to the controller on its output pin, after oscillator is turned ON. In this period the clock is as-sumed to be unstable, and so the controller does not turn on the clock to internal logic till this period is over. This means, the wake up from deep sleep mode must account for this delay before the wakeup instant. Osc_startup_delay[7:5] is number of slots(625us) Osc_startup_delay[4:0 is number of clock periods of 16KHz clock (Warning: Min. value of Osc_startup_delay [4:0] sup-ported is 1 and Max. value is 9. Therefore programmable range is 1 to 9) Default Value: 0

2.1.38 BLE_BLELL_WAKEUP_CONTROL

Wakeup control

Address: 0x402E10C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	WAKEUP_INSTANT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	WAKEUP_INSTANT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	WAKEUP_INSTANT	Instant, with reference to the internal 16-bit clock reference, at which the hardware must wakeup from deep sleep mode. This is calculated by firmware based on the next closest instant where a controller operation is required (like advertiser/scanner). Firmware reads the next instant of the procedures in the corresponding *_NEXT_INSTANT registers. This value is used only when hardware auto wakeup from deep sleep mode is enabled in the clock control register. Note: it is recommended to program wakeup_instant such a way that the actual instant to wake-up shall be at least two counts (two slots of 625 us) ahead of reference clock when entering DSM. The actual instant to wakeup is wakeup_instant dsm_offset_to_wakeup_instant osc_startup_delay, and it shall be greater than reference clock + 2 Default Value: 0

2.1.39 BLE_BLELL_CLOCK_CONFIG

Clock control

Address: 0x402E10C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	RW	RW	RW	RW	RW	RW	RW
HW Access	RW	R	R	R	R	R	R	R
Name	LLH_IDLE	PHY_CLK_GATE_EN	SYSCLK_GATE_EN	CORECLK_GATE_EN	CONN_CLK_GATE_EN	INIT_CLK_GATE_EN	SCAN_CLK_GATE_EN	ADV_CLK_GATE_EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	None	RW	None	RW	RW	RW
HW Access	R	R	None	R	None	R	R	R
Name	DEEP_SLEEP_MODE_EN	SLEEP_MODE_EN	None	SM_INTR_EN	None	SM_AUTO_WKUP_EN	LPO_SEL_EXTERNAL	LPO_CLK_FREQ_SEL

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15	DEEP_SLEEP_MODE_EN	Enable deep sleep mode. 1 enable, 0 disable. Enables hardware logic related to deep sleep mode to control the deep sleep mode operation. If disabled, the related logic is not executed and hardware cannot enter deep sleep mode. Default Value: 0
14	SLEEP_MODE_EN	Enable sleep mode. 1 enable, 0 disable. Enables hardware to control sleep mode operation. Default Value: 0
12	SM_INTR_EN	Enable SM exit interrupt. 1 enable, 0 disable. Enables hardware to generate an interrupt while exiting sleep mode irrespective of whether it is initiated by hardware or firmware. The interrupt is captured and stored till it gets cleared. Disabling this bit mask the sleep mode exit event from hardware & firmware. Default Value: 0

(continued)

10	SM_AUTO_WKUP_EN	Enable sleep mode auto wakeup enable. 1- enable, 0 disable. Enables hardware to automatically wakeup from sleep mode at the instant = wakeup_instant sm_offset_to_wakeup_instant. The wakeup_insant is the field in the wakeup control register described earlier. The sm_offset_to_wakeup_instant value is the field described in the wakeup configuration register. Default Value: 0
9	LPO_SEL_EXTERNAL	Select external sleep clock. 1 External clock, 0 - inter-nal generated clock. The field is used to select either the low power clock in-put on sleep_clk input pin(of frequency 16.384KHz) di-rectly to run the DSM logic or to use the internal gener-ated reference clock(of 16KHz) for the same. Default Value: 0
8	LPO_CLK_FREQ_SEL	Clock frequency select. 0 32KHz, 1 32.768KHz. Base frequency of the sleep_clk input used for generat-ing the internal reference clock of approximate 16Khz frequency. Default Value: 0
7	LLH_IDLE	Indicates if hardware is doing any transmit/receive operation. This information is used by firmware to decide to program the hardware into deep sleep mode. 1 LL hardware is idle. 0 LL hardware is busy. In this case LL hardware will not enter deep sleep mode, even if firmware gives an enter DSM command. (In this situation hardware generates dsm exit interrupt to inform firmware that DSM entry was not successful). Default Value: 1
6	PHY_CLK_GATE_EN	Digital PHY clock enable. 1- enable, 0-disable. Enable the Digital PHY to shutdown the clock. When 1, it indicates that controller has an upcoming activity so PHY clock must be turned ON. When 0, it indicates inactivity in the controller. Default Value: 0
5	SYSCLK_GATE_EN	Sysclk gate enable. 1- enable, 0 disable. Enables clock gating of system clock input to the link layer. If 1, it enables the DSM logic to control the clock gate for system clock input from pin. If 0, the DSM logic has no control and the system clock is always ON. Default Value: 0
4	CORECLK_GATE_EN	Core clock gate enable. 1 enable, 0 disable. Enables gating of clock to the llh_core module in hard-ware. If 1, the sleep mode/deep sleep mode logic can control the clock gate to shutdown/wakeup the clock to the module. If 0, the logic has no control and clock is always turned ON. Default Value: 0
3	CONN_CLK_GATE_EN	Connection block clock gate enable. 1 enable, 0 disable. Enables gating of clock to the connection module (llh_connch_top) in hardware. If 1, the sleep mode logic can control the clock gate to shutdown/wakeup the clock to the engine. If 0, the logic has no control and clock to the module is always turned ON. Default Value: 0
2	INIT_CLK_GATE_EN	Initiator block clock gate enable. 1 enable, 0 disable. Enables gating of clock to the initiator module (llh_init). If 1, the sleep mode logic can control the clock gate to shutdown/wakeup the clock to the module. If 0, the logic has no control and clock to the module is always turned ON. Default Value: 0
1	SCAN_CLK_GATE_EN	Scan block clock gate enable. 1 enable, 0 disable. Enables gating of clock to the scanner module (llh_scan) in hardware. If 1, the sleep mode logic can control the clock gate to shutdown/wakeup the clock to the module. If 0, the logic has no control and clock to the module is always turned ON. Default Value: 0

(continued)

0	ADV_CLK_GATE_EN	Advertiser block clock gate enable. 1 enable, 0 disable. Enables gating of clock to the advertiser module (llh_adv) in hardware. If 1, the sleep mode logic can control the clock gate to shutdown/wakeup the clock to the module. If 0, the logic has no control and clock to the module is always turned ON. Default Value: 0

2.1.40 BLE_BLELL_TIM_COUNTER_L

Reference Clock

Address: 0x402E10C8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	TIM_REF_CLOCK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	TIM_REF_CLOCK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	TIM_REF_CLOCK	16-bit internal reference clock. The clock is a free run-ning clock, incremented by a 0.625ms periodic pulse. It is used as a reference clock to derive all the timing required as per protocol. Default Value: 0

2.1.41 BLE_BLELL_POC_REG__TIM_CONTROL

BLE Time Control

Address: 0x402E10D8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		
HW Access	RW					None		
Name	BB_CLK_FREQ_MINUS_1 [7:3]					None [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 3	BB_CLK_FREQ_MINUS_1	LLH clock configuration. The clock frequency of the clock input to this design is configured in this register. This is used to derive a 1MHz clock. Default Value: 0

2.1.42 BLE_BLELL_ADV_TX_DATA_FIFO

Advertising data transmit FIFO. Access ADVCH_TX_FIFO.

Address: 0x402E10E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	ADV_TX_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	ADV_TX_DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	ADV_TX_DATA	IO mapped FIFO of depth 16 (2 byte wide), to store ADV data of maximum length 31 bytes for transmitting. Firmware writes consecutive words by writing to the same address location. Note: ADV_TX_DATA_FIFO and ADV_SCN_RSP_TX_FIFO shares same physical FIFO of depth 32. 16 locations for each FIFO are allocated. Default Value: 0

2.1.43 BLE_BLELL_ADV_SCN_RSP_TX_FIFO

Advertising scan response data transmit FIFO. Access ADVCH_TX_FIFO.

Address: 0x402E10E8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	SCAN_RSP_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	SCAN_RSP_DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	SCAN_RSP_DATA	IO mapped FIFO of depth 16 (2 byte wide), to store scan response data of maximum length 31 bytes for transmitting. Firmware writes consecutive words by writing to the same location. Note: ADV_TX_DATA_FIFO and ADV_SCN_RSP_TX_FIFO shares same physical FIFO of depth 32. 16 locations for each FIFO are allocated. Default Value: 0

2.1.44 BLE_BLELL_INIT_SCN_ADV_RX_FIFO

advertising scan response data receive data FIFO. Access ADVRX_FIFO.

Address: 0x402E10F8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	ADV_SCAN_RSP_RX_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	ADV_SCAN_RSP_RX_DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	ADV_SCAN_RSP_RX_DATA	IO mapped FIFO of depth 64, to store ADV and SCAN_RSP header and payload received by the scanner. The RSSI value at the time of reception of this packet is also stored. Firmware reads from the same address to read out consecutive words of data. Note: The 16 bit header is first loaded to the advertise channel data receive FIFO followed by the payload data and then 16 bit RSSI. Default Value: 0

2.1.45 BLE_BLELL_CONN_INTERVAL

Connection Interval

Address: 0x402E1100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CONNECTION_INTERVAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CONNECTION_INTERVAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CONNECTION_INTERVAL	The value configured in this register determines the spacing be-tween the connection events. This shall be a multiple of 1.25 ms in the range of 7.5 ms to 4.0 s. Default Value: 0

2.1.46 BLE_BLELL_SUP_TIMEOUT

Supervision timeout

Address: 0x402E1104

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	SUPERVISION_TIMEOUT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	SUPERVISION_TIMEOUT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	SUPERVISION_TIMEOUT	This field defines the maximum time between two received Data packet PDUs before the connection is considered lost. This shall be a multiple of 10 ms in the range of 100 ms to 32.0 s and it shall be larger than (1+connSlaveLatency)*connInterval. Default Value: 0

2.1.47 BLE_BLELL_SLAVE_LATENCY

Slave Latency

Address: 0x402E1108

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	SLAVE_LATENCY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	SLAVE_LATENCY [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	SLAVE_LATENCY	The value configured in this field defines the number of consecutive connection events that the slave device is not required to listen for master. The value of connSlaveLatency should not cause a Supervision Timeout. This shall be an integer in the range of 0 to ((connSupervision Timeout/connInterval)-1). connSlaveLatency shall also be less than 500. Default Value: 0

2.1.48 BLE_BLELL_CE_LENGTH

Connection event length

Address: 0x402E110C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CONNECTION_EVENT_LENGTH [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CONNECTION_EVENT_LENGTH [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description

(continued)

15 : 0	CONNECTION_EVENT_LENGTH	This field defines the length of Connection event. This value is derived from the CE length HCI parameters received from the host. This determines the number of master transmit slots in a connection event, subject to either of the MD bits being set. If both MD bits are set to 0, this has no effect. Units: 625us Note: The connection event length as specified by the CE_LENGTH shall not exceed CONN_INTERVAL 1.25 ms. The CE-length parameter, according to the Bluetooth specification, is the length of the connection event. Take an example to illustrate this scenario: Assume a connection with interval = 100ms. that the application has put allowed 20ms of CE-length. Here, the CE-length can be upto 100ms (100ms - 150us to be exact). If the connection is maintained for 5 minutes, there could be 10*60*5 = 3000 connection-intervals. The CE-length need not be maintained constant during all the 3000 connection events. Here are the typical cases that determine the value of CE-length: (1) No data packets exchanged. we are just maintaining time and frequency synchronization. In this case, only a packet pair will be exchanged every connection interval. Here, CE-length = 1. (2) Average of 10 packets to be sent per connection event. We can pump data in multiple ways here: 2.1: Send data at uniform rate : In this case, the CE-length will be enough to accommodate 10 packets, which will take about 7ms. As this is less than application enforced limit of 20ms, we can comfortably push all the 10 data packets in this connection interval. So data will be pumped to the other BT device at the same rate as is received from my application. 2.2: Can send data in bursts. Assume that we accumulate data for 1 second and pump out at the end of 1 second(this is not done by our Bluetooth stack, the application needs to buffer the data). So, at 10th connection interval, we have 100 packets accumulated. We are now ready to pump this data. 100 packets take about 70 ms. This is above the application enforced 20ms. So, the hardware can pump data that can fill up 20ms. The remaining data will be deferred to the next connection interval. So, in this case, you would see a CE-length spread over time like this (Per connection interval): 0,0,0,0,0,0,0,0,0,0, 20,20,20,10,0,0,0,0,0,0, 20,20,20,10,0,0,0,0,0,0, 20,20,20,10,0,0,0,0,0,0, and so on. (3) We are receiving data at the same rate as in (2). This case is to honor data sent by the other BT-device by giving it more time in the current connection interval. In (2) and (3) you will see non-empty packets either transmitted or received. We can also utilize the CE-length for different reasons: (4) A transaction is in progress, and we are expecting a response packet very soon. In this case, we may be exchanging only empty packets now, and in the next few packet-pairs. In this case, you will the CE-length to be large, and a non-empty packet may not be exchanged in all the slots. In slave mode, the connection event length (unit of 625us) will close the connection event at programmed time irrespective of MD bit received from the master or the MD bit sent from slave. Default Value: 0

2.1.49 BLE_BLELL_PDU_ACCESS_ADDR_L_REGISTER

Access address (lower)

Address: 0x402E1110

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	PDU_ACCESS_ADDRESS_LOWER_BITS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PDU_ACCESS_ADDRESS_LOWER_BITS [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	PDU_ACCESS_ADDRESS_LOWER_BITS	This field defines the lower 16 bits of the access address for each Link layer connection between any two devices. Default Value: 0

2.1.50 BLE_BLELL_PDU_ACCESS_ADDR_H_REGISTER

Access address (upper)

Address: 0x402E1114

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	PDU_ACCESS_ADDRESS_HIGHER_BITS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PDU_ACCESS_ADDRESS_HIGHER_BITS [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	PDU_ACCESS_ADDRESS_HIGHER_BITS	This field defines the higher 16 bits of the access address for each Link layer connection between any two devices. Default Value: 0

2.1.51 BLE_BLELL_CONN_CE_INSTANT

Connection event instant

Address: 0x402E1118

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CE_INSTANT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CE_INSTANT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CE_INSTANT	This is the value of the free running Connection Event counter when the new parameters of connection update and/or Channel map update will be effective. Range : 0x0000 to 0xFFFF Default Value: 0

2.1.52 BLE_BLELL_CE_CNFG_STS_REGISTER

connection configuration & status register

Address: 0x402E111C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW			
HW Access	RW	R	R	R	R			
Name	MAP_INDEX__CURR_INDEX	MD	MAS_SLV	DATA_LIST_HEAD_UP	DATA_LIST_INDEX_LAST_ACK_INDEX [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	R				None	R	None	RW
HW Access	RW				None	RW	None	R
Name	CURRENT_PDU_INDEX [15:12]				None	CONN_ACTIVE	None	PAUSE_DATA

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 12	CURRENT_PDU_INDEX	The index of the transmit packet buffer that is currently in transmission/waiting for transmission. Default Value: 0
10	CONN_ACTIVE	This bit is 1 whenever the connection is active. Default Value: 0
8	PAUSE_DATA	Pause data. 1 - pause data, 0 - do not pause. Pause the data transfer on the connection. The current_pdu_index in hardware does not move to next in-dex until pause_data is cleared. Default Value: 0
7	MAP_INDEX__CURR_INDEX	Written by firmware to select the map index to be used by hardware for this connection. 1 - use channel map register set 1. 0 - use channel map register set 0. When firmware reads this field, it returns the current map index being used in hardware. Default Value: 0

(continued)

6	MD	MD bit set to 1 indicates device has more data to be sent. Default Value: 0
5	MAS_SLV	mas_slv bit set to 1 indicates that device is confi-gured as a master or a slave. 1 - master, 0 - slave. Default Value: 0
4	DATA_LIST_HEAD_UP	Update the first packet buffer index ready for transmis-sion to start/resume data transfer after a pause. The bit must be toggled every time the firmware needs to indicate the start/resume. This requires a read modify write operation. Default Value: 0
3 : 0	DATA_LIST_INDEX_LAST_ACK_INDEX	Data list index for start/resume. This field must be valid along with data_list_head_up and indi-cate the transmit packet buffer index at which the data is loaded. The default number of buffers in the IP is 5,but may be customized for a customer. The buffers are in-dexed 0 to 4. Hardware will start the next data transmission from the index indicated by this field. Default Value: 0

2.1.53 BLE_BLELL_NEXT_CE_INSTANT

Next connection event instant

Address: 0x402E1120

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	NEXT_CE_INSTANT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	NEXT_CE_INSTANT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	NEXT_CE_INSTANT	16-bit internal reference clock value at which the next connection event will occur on a connection. The connection index register must be programmed with index of the connection, before reading the register. Default Value: 0

2.1.54 BLE_BLELL_CONN_CE_COUNTER

connection event counter

Address: 0x402E1124

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	CONNECTION_EVENT_COUNTER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	CONNECTION_EVENT_COUNTER [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CONNECTION_EVENT_COUNTER	This is the free running counter, connEventCounter as defined by Bluetooth spec. Firmware will read the instantaneous Event counter from this register, during connection update and channel map update procedure. Firmware will use this value to calculate the instant from which the new parameters (for connection update and channel map update) will be effective. Default Value: 0

2.1.55 BLE_BLELL_DATA_LIST_SENT_UPDATE__STATUS

data list sent update and status

Address: 0x402E1128

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W	None		R	RW			
HW Access	RW	None		RW	RW			
Name	SET_CLEAR	None [6:5]		TX_SENT_4	LIST_INDEX__TX_SENT_3_0 [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	SET_CLEAR	Write: Used to set the SENT bit in hardware for the selected packet buffer. 1 packet queued When firmware has a packet to send, firmware first loads the next available packet buffer. Then the hardware SENT bit is set by writing 1 to this bit field along with the list_index field that identified the buffer index. This indicates that a packet has been queued in the data buffer for sending. This packet is now ready to be transmitted. The SENT bit in hardware is cleared by hardware only when it has received an acknowledgement from the remote device. Firmware typically does not clear the bit. However, It only clears the bit on its own if it needs to flush a packet from the buffer, without waiting to receive acknowledgement from the remote device, firmware clears BIT7 along with the list_index specified. Default Value: 0

(continued)

4	TX_SENT_4	Read: Reads TX_SENT[4]. The bits in this field indicate the status of the SENT bit in the hard-ware for each packet buffer. The bit values are 1 queued 0 no packet / packet ack received by hardware Example1: If the read value is : 0x03, then packets in buffer 0 and buffer 1 are in the queue to be transmitted. All the other FIFOs are empty or hardware has cleared them after receiving ac-knowledgement. NOTE: The SENT status bit and ACK status bit have to be taken together to understand the meaning of packet status. The table below describes how the two bits are sequentially updated by either hardware/firmware to complete one data transmission. SENT ACK Description 0 0 Buffer is empty. No packet is queued in the buffer 1 0 Packet is queued by firmware. 1 1 Packet is transmitted by hardware. Hardware is waiting for acknowledgement. 0 1 Hardware has received ACK. Firmware has not yet processed the ACK. 0 0 Firmware has processed the ack. The buffer is again empty. Default Value: 0
3 : 0	LIST_INDEX__TX_SENT_3_0	Write:Indicates the buffer index for which the SENT bit is being updated by firmware. The default number of buffers in the IP is 5. The index range is 0-4. Read: Reads TX_SENT[3:0]. The bits in this field indicate the status of the SENT bit in the hard-ware for each packet buffer. The bit values are 1 queued 0 no packet / packet ack received by hardware Example1: If the read value is : 0x03, then packets in buffer 0 and buffer 1 are in the queue to be transmitted. All the other FIFOs are empty or hardware has cleared them after receiving ac-knowledgement. Default Value: 0

2.1.56 BLE_BLELL_DATA_LIST_ACK_UPDATE__STATUS

data list ack update and status

Address: 0x402E112C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W	None		R	RW			
HW Access	RW	None		RW	RW			
Name	SET_CLEAR	None [6:5]		TX_ACK_4	LIST_INDEX__TX_ACK_3_0 [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	SET_CLEAR	Write: Firmware uses the field to clear and ACK bit in the hardware to indicate that the acknowl-edgement for the transmit packet has been received and processed by firmware. Firmware clears the ACK bit in the hardware by writing in this register only after the acknowl-edgement is processed successfully by firmware. For clearing ack for a packet transmitted in fifo-index : 3, firm-ware will write 3 in the list-index field and set this bit (BIT7) to 0. This is the indication that the corresponding packet buffer identi-fied by List-Index is cleared of previous transmission and can be re-used for another packet from now on. The ACK bit in hardware is set by hardware when it has success-fully transmitted a packet. Default Value: 0

(continued)

4	TX_ACK_4	Reads TX_ACK[4] If a particular bit is set, then the packet in the selected buffer has been transmitted (at least once) by the hardware and hardware is waiting for acknowledgement. Example1 : If the read value is : 0x03, then packets in FIFO-0 and FIFO-1 are acknowledged by the remote device. These acknowledgements are pending to be processed by firmware. Example2 : If the read value is : 0x02, then packet FIFO-1 is acknowledged by the remote device. This acknowledgement is pending to be processed by firmware. NOTE: The SENT status bit and ACK status bit have to be taken together to understand the meaning of packet status. The table below describes how the two bits are sequentially updated by either hardware/firmware to complete one data transmission. SENT ACK Description 0 0 Buffer is empty. No packet is queued in the buffer 1 0 Packet is queued by firmware. 1 1 Packet is transmitted by hardware. Hardware is waiting for acknowledgement. 0 1 Hardware has received ACK. Firmware has not yet processed the ACK. 0 0 Firmware has processed the ack. The buffer is again empty. Default Value: 0
3 : 0	LIST_INDEX__TX_ACK_3_0	Write: Indicates the buffer index for which the ACK bit is being updated by firmware. The default number of buffers in the IP is 5. The index range is 0-4. Read: Reads TX_ACK[3:0] If a particular bit is set, then the packet in the selected buffer has been transmitted (at least once) by the hardware and hardware is waiting for acknowledgement. Example1 : If the read value is : 0x03, then packets in FIFO-0 and FIFO-1 are acknowledged by the remote device. These acknowledgements are pending to be processed by firmware. Example2 : If the read value is : 0x02, then packet FIFO-1 is acknowledged by the remote device. This acknowledgement is pending to be processed by firmware. Default Value: 0

2.1.57 BLE_BLELL_DATA_MEM_DESCRIPTOR0

Data buffer descriptor 0 to 4

Address: 0x402E1140

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW					RW	
HW Access	None	R					R	
Name	None	DATA_LENGTH [6:2]					LLID [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
6 : 2	DATA_LENGTH	This field indicates the length of the data packet. Range 0x0 to 0xF. Default Value: 0
1 : 0	LLID	The LLID indicates whether the packet is an LL Data PDU or an LL Control PDU. 00b= Reserved. 01b=LL Data PDU: Continuation fragment of an L2CAP message or an Empty PDU. 10b=LL Data PDU: Start of an L@CAP message or a complete L2CAP message with no fragmentation. 11b=LL Control PDU. Default Value: 0

2.1.58 BLE_BLELL_DATA_MEM_DESCRIPTOR1

Data buffer descriptor 0 to 4

Address: 0x402E1144

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW					RW	
HW Access	None	R					R	
Name	None	DATA_LENGTH [6:2]					LLID [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
6 : 2	DATA_LENGTH	This field indicates the length of the data packet. Range 0x0 to 0xF. Default Value: 0
1 : 0	LLID	The LLID indicates whether the packet is an LL Data PDU or an LL Control PDU. 00b= Reserved. 01b=LL Data PDU: Continuation fragment of an L2CAP message or an Empty PDU. 10b=LL Data PDU: Start of an L@CAP message or a complete L2CAP message with no fragmentation. 11b=LL Control PDU. Default Value: 0

2.1.59 BLE_BLELL_DATA_MEM_DESCRIPTOR2

Data buffer descriptor 0 to 4

Address: 0x402E1148

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW					RW	
HW Access	None	R					R	
Name	None	DATA_LENGTH [6:2]					LLID [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
6 : 2	DATA_LENGTH	This field indicates the length of the data packet. Range 0x0 to 0xF. Default Value: 0
1 : 0	LLID	The LLID indicates whether the packet is an LL Data PDU or an LL Control PDU. 00b= Reserved. 01b=LL Data PDU: Continuation fragment of an L2CAP message or an Empty PDU. 10b=LL Data PDU: Start of an L@CAP message or a complete L2CAP message with no fragmentation. 11b=LL Control PDU. Default Value: 0

2.1.60 BLE_BLELL_DATA_MEM_DESCRIPTOR3

Data buffer descriptor 0 to 4

Address: 0x402E114C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW					RW	
HW Access	None	R					R	
Name	None	DATA_LENGTH [6:2]					LLID [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
6 : 2	DATA_LENGTH	This field indicates the length of the data packet. Range 0x0 to 0xF. Default Value: 0
1 : 0	LLID	The LLID indicates whether the packet is an LL Data PDU or an LL Control PDU. 00b= Reserved. 01b=LL Data PDU: Continuation fragment of an L2CAP message or an Empty PDU. 10b=LL Data PDU: Start of an L@CAP message or a complete L2CAP message with no fragmentation. 11b=LL Control PDU. Default Value: 0

2.1.61 BLE_BLELL_DATA_MEM_DESCRIPTOR4

Data buffer descriptor 0 to 4

Address: 0x402E1150

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW					RW	
HW Access	None	R					R	
Name	None	DATA_LENGTH [6:2]					LLID [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
6 : 2	DATA_LENGTH	This field indicates the length of the data packet. Range 0x0 to 0xF. Default Value: 0
1 : 0	LLID	The LLID indicates whether the packet is an LL Data PDU or an LL Control PDU. 00b= Reserved. 01b=LL Data PDU: Continuation fragment of an L2CAP message or an Empty PDU. 10b=LL Data PDU: Start of an L@CAP message or a complete L2CAP message with no fragmentation. 11b=LL Control PDU. Default Value: 0

2.1.62 BLE_BLELL_WINDOW_WIDEN_INTVL

Window widen for interval

Address: 0x402E1160

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	WINDOW_WIDEN_INTVL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				WINDOW_WIDEN_INTVL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11 : 0	WINDOW_WIDEN_INTVL	This value defines the increased listening time for the slave. The window widening shall be smaller than ((connInterval/2)-T_IFS us) This value is calculated by firmware based on the drift, the connec-tion interval value. The value is the unit widening value for one con-nection interval duration. In case of slave latency, this val-ue is accu-mulated till the next anchor point at which the slave will listen. Default Value: 10

2.1.63 BLE_BLELL_WINDOW_WIDEN_WINOFF

Window widen for offset

Address: 0x402E1164

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	WINDOW_WIDEN_WINOFF [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				WINDOW_WIDEN_WINOFF [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11 : 0	WINDOW_WIDEN_WINOFF	This field stores the additional number of microseconds the slave must extend its listening window to listen for a master packet. This value is calculated based on the window offset value. This is used at connection setup directly. During connection setup, this value is added with window_widen_intvl register value to calculate the win-dow widening size. Default Value: 10

2.1.64 BLE_BLELL_LE_RF_TEST_MODE

Direct Test Mode control

Address: 0x402E1170

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW					
HW Access	R	RW	R					
Name	PKT_PAYLOAD	TEST_TYPE	TEST_FREQUENCY [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	RW						RW	
HW Access	R						R	
Name	TEST_LENGTH [15:10]						PKT_PAYLOAD [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 10	TEST_LENGTH	0x00-0x25 Length in bytes of payload data in each packet 0x26-0xFF Reserved for future use Default Value: 0
9 : 7	PKT_PAYLOAD	Payload type as per the HCI parameter. 0x00 Pseudo-Random bit sequence 9 0x01 Pattern of alter-nating bits 11110000 0x02 Pattern of alternating bits 10101010 0x03 Pseudo-Random bit sequence 15 0x04 Pat-tern of All 1 bits 0x05 Pattern of All 0 bits 0x06 Pattern of alternating bits 00001111 0x07 Pattern of alternating bits 0101 0x08-0xFF Reserved for future use Default Value: 0
6	TEST_TYPE	1 - DTM test ON 0 - DTM test OFF Default Value: 0

(continued)

5 : 0	TEST_FREQUENCY	N = (F 2402) / 2 Range: 0x00 0x27. Frequency Range : 2402 MHz to 2480 MHz Default Value: 0

2.1.65 BLE_BLELL_DTM_RX_PKT_COUNT

Direct Test Mode receive packet count

Address: 0x402E1174

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	RX_PACKET_COUNT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	RX_PACKET_COUNT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	RX_PACKET_COUNT	Number of packets received in receive test mode. Default Value: 0

2.1.66 BLE_BLELL_TXRX_HOP

Channel Address register

Address: 0x402E1188

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	R						
HW Access	None	RW						
Name	None	HOP_CH_TX [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None	R						
HW Access	None	RW						
Name	None	HOP_CH_RX [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
14 : 8	HOP_CH_RX	Receive channel index. Channel index on which previous packet is received. Default Value: 0
6 : 0	HOP_CH_TX	Transmit channel index. Channel index on which previous packet is transmitted. Default Value: 0

2.1.67 BLE_BLELL_TX_RX_ON_DELAY

Transmit/Receive data delay

Address: 0x402E1190

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	RXON_DELAY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	TXON_DELAY [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 8	TXON_DELAY	Transmit delay Delay from start of transmit to transmission of first bit on air. It is used to control the T_IFS. The delay is in resolution of 1 microsecond. Default Value: 0
7 : 0	RXON_DELAY	Receive delay Delay from start of receive to expected first bit of receive packet at the controller. Used to control the turn on time of radio to optimize on power. The delay is in resolution of 1 microsecond. Default Value: 0

2.1.68 BLE_BLELL_DEV_PUB_ADDR_L

Device public address lower register

Address: 0x402E11C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DEV_PUB_ADDR_L [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DEV_PUB_ADDR_L [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DEV_PUB_ADDR_L	Lower 16 bit of 48-bit public address of the device. Default Value: 13330

2.1.69 BLE_BLELL_DEV_PUB_ADDR_M

Device public address middle register

Address: 0x402E11C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DEV_PUB_ADDR_M [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DEV_PUB_ADDR_M [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DEV_PUB_ADDR_M	Middle 16 bit of 48-bit public address of the device. Default Value: 86

2.1.70 BLE_BLELL_DEV_PUB_ADDR_H

Device public address higher register

Address: 0x402E11C8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DEV_PUB_ADDR_H [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DEV_PUB_ADDR_H [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DEV_PUB_ADDR_H	Higher 16 bit of 48-bit public address of the device. Default Value: 0

2.1.71 BLE_BLELL_ADV_CH_TX_POWER

Advetising channel transmit power

Address: 0x402E11CC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	ADV_TRANSMIT_POWER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	ADV_TRANSMIT_POWER [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	ADV_TRANSMIT_POWER	Size: 1 Octet (signed integer) Range: -20 = N = 10 Units: dBm Accuracy: +/- 4 dBm in general. In implementation this is a radio specific value. Default Value: 34639

2.1.72 BLE_BLELL_OFFSET_TO_FIRST_INSTANT

Offset to first instant

Address: 0x402E11D0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	OFFSET_TO_FIRST_EVENT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	OFFSET_TO_FIRST_EVENT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	OFFSET_TO_FIRST_EVENT	The offset w.r.t the internal reference clock at which instant the first event occurs. This register will give flexibility to the firmware to position the con-nection at a desired point with respect to the internal free running clock. It is optional to be updated by firmware. This is not updated in the current firmware. Default Value: 6

2.1.73 BLE_BLELL_ADV_CONFIG

Advertiser configuration register

Address: 0x402E11D4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	ADV_TIMEOUT_EN	SLV_CONNECTED_EN	ADV_CONN_REQ_RX_EN	ADV_SCN_REQ_RX_EN	SCN_RSP_TX_EN	ADV_TX_EN	ADV_CLS_EN	ADV_STRT_EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW					None		RW
HW Access	R					None		R
Name	ADV_PKT_INTERVAL [15:11]					None [10:9]		ADV_RAND_DISABLE

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 11	ADV_PKT_INTERVAL	Time between the beginning of two consecutive advertising PDUs. Time = N * 0.625 msec Time Range: <=10msec. Default Value: 4
8	ADV_RAND_DISABLE	Disable randomization of adv interval. When disabled, interval is same as programmed in adv_interval register. Default Value: 0
7	ADV_TIMEOUT_EN	Enable adv_timeout interrupt. Applicable in adv_direct_ind advertising. Default Value: 1
6	SLV_CONNECTED_EN	Enable slave connected interrupt. Default Value: 1
5	ADV_CONN_REQ_RX_EN	Enable connect request packet received interrupt. Default Value: 1

(continued)

4	ADV_SCN_REQ_RX_EN	Enable scan request packet received interrupt. Default Value: 1
3	SCN_RSP_TX_EN	Enable scan response packet transmitted interrupt. Default Value: 1
2	ADV_TX_EN	Enable adv packet transmitted interrupt. Default Value: 1
1	ADV_CLS_EN	Enable advertising event stop interrupt. Default Value: 1
0	ADV_STRT_EN	Enable advertising event start interrupt. Default Value: 1

2.1.74 BLE_BLELL_SCAN_CONFIG

Scan configuration register

Address: 0x402E11D8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [7:5]			SCN_RSP_RX_EN	ADV_RX_EN	SCN_TX_EN	SCN_CLOSE_EN	SCN_STRT_EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW			None	RW	None		
HW Access	R			None	R	None		
Name	SCAN_CHANNEL_MAP [15:13]			None	BACKOFF_ENABLE	None [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 13	SCAN_CHANNEL_MAP	Advertising channels that are enabled for scanning operation. Bit 15: setting 1 - enables channel 39 for use. Bit 14: setting 1 - enables channel 38 for use. Bit 13: setting 1 - enables channel 37 for use. Default Value: 7
11	BACKOFF_ENABLE	Enable random backoff feature in scanner. 1 - enable 0 - disable Default Value: 0
4	SCN_RSP_RX_EN	Enable scan_rsp packet received interrupt . Default Value: 1
3	ADV_RX_EN	Enable adv packet received interrupt . Default Value: 1
2	SCN_TX_EN	Enable scan request packet transmitted interrupt. Default Value: 1

(continued)

1	SCN_CLOSE_EN	Enable scan event close interrupt. Default Value: 1
0	SCN_STRT_EN	Enable scan event start interrupt. Default Value: 1

2.1.75 BLE_BLELL_INIT_CONFIG

Initiator configuration register

Address: 0x402E11DC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	None	RW	RW	RW
HW Access	None			R	None	R	R	R
Name	None [7:5]			CONN_CREATED	None	CONN_REQ_TX_EN	INIT_CLOSE_EN	INIT_STRT_EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW			None				
HW Access	R			None				
Name	INIT_CHANNEL_MAP [15:13]			None [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 13	INIT_CHANNEL_MAP	Advertising channels that are enabled for initiator scanning operation. Bit 15: setting 1 - enables channel 39 for use. Bit 14: setting 1 - enables channel 38 for use. Bit 13: setting 1 - enables channel 37 for use. Default Value: 0
4	CONN_CREATED	Enable master connection created interrupt Default Value: 0
2	CONN_REQ_TX_EN	Enables connection request packet transmission start interrupt. Default Value: 0
1	INIT_CLOSE_EN	Enable Initiator event close interrupt. Default Value: 0
0	INIT_STRT_EN	Enable Initiator event start interrupt. Default Value: 0

2.1.76 BLE_BLELL_CONN_CONFIG

Connection configuration register

Address: 0x402E11E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	RX_INTR_THRESHOLD [7:4]				RX_PKT_LIMIT [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	None		RW
HW Access	R	R	R	R	R	None		R
Name	CONN_REQ_1SLOT_EARLY	MASK_SUTO_AT_UPDT	EXTEND_CU_TX_WIN	SLV_MD_CONFIG	DSM_SLOT_VARIANCE	None [10:9]		MD_BIT_CLEAR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15	CONN_REQ_1SLOT_EARLY	This bit is used to enable extension of the Conn Request to arbiter to 1 slot early. When enabled the request length is 2 slots. 1 - Enable 0 - Disable Default Value: 1
14	MASK_SUTO_AT_UPDT	This bit is used to enable/disable masking of internal hardware supervision timeout trigger when switching from old connection parameters to new parameters. 1 - Enable 0 - Disable Default Value: 1
13	EXTEND_CU_TX_WIN	This bit is used to enable/disable extending the additional rx window on slave side during connection update in event of packet miss at the update instant. 1 - Enable 0 - Disable Default Value: 1

(continued)

12	SLV_MD_CONFIG	This bit is set to configure the MD bit control when IUT is in slave role. 1 - MD bit will be decided on packet pending status 0 - MD bit will be decided on packet queued in next buffer status This bit has effect only when CONN_CONFIG.md_bit_ctr bit is not set . Default Value: 0
11	DSM_SLOT_VARIANCE	This bit configures the DSM slot counting mode. 0 - The DSM slot count variance with respect to actual time is less than 1 slot 1 - The DSM slot count variance with respect to actual time is more than 1 slot that 2 slots Default Value: 0
8	MD_BIT_CLEAR	This register field indicates whether the MD (More Data) bit needs to be controlled by software or, hardware and soft-ware logic combined. 1 - MD bit is exclusively controlled by software, ie based on status of CE_CNFG_STS_REGISTER[6] - md bit. 0 - MD Bit in the transmitted pdu is controlled by software and hardware logic. MD bit is set in transmitted packet, only if the software has set the md bit in CE_CNFG_STS_REGISTER[6] and either of the following conditions is true, a) If there are packets queued for transmission. b) If there is an acknowledgement awaited from the remote side for the packet transmitted. Default Value: 1
7 : 4	RX_INTR_THRESHOLD	This register field allows setting a threshold for the packet received interrupt to the firmware. For example if the value programmed is 0x2 then HW will generate interrupt only on receiving the second packet. In any case if the received number of packets in a conn event is less than the threshold or there are still packets (less than threshold) pending in the Rx FIFO, HW will generate the interrupt at the ce_close. Min value possible is 1. Max value depends on the Rx FIFO capacity. Default Value: 1
3 : 0	RX_PKT_LIMIT	Defines a limit for the number of Rx packets that can be re-ceived by the LLH. Default maximum value is 0xF.Minimum value shall be 1 or no packet will be stored in the Rx FIFO. Default Value: 15

2.1.77 BLE_BLELL_CONN_CH_TX_POWER

Connection channel transmit power

Address: 0x402E11E4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CONNCH_TRANSMIT_POWER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CONNCH_TRANSMIT_POWER [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CONNCH_TRANSMIT_POWER	Transmit power to be used for all packets transmitted on the connection channel. Default Value: 0

2.1.78 BLE_BLELL_CONN_PARAM1

Connection parameter 1

Address: 0x402E11E8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW		
HW Access	RW					RW		
Name	HOP_INCREMENT_PARAM [7:3]					SCA_PARAM [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CRC_INIT_L [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 8	CRC_INIT_L	This field defines the lower byte (7:0) of the CRC initialization vector. Default Value: 0
7 : 3	HOP_INCREMENT_PARAM	Hop increment for connection channel. Default Value: 0
2 : 0	SCA_PARAM	Sleep Clock Accuracy Default Value: 0

2.1.79 BLE_BLELL_CONN_PARAM2

Connection parameter 2

Address: 0x402E11EC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CRC_INIT_H [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CRC_INIT_H [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CRC_INIT_H	This field defines the upper two bytes (23:8) of the CRC initialization vector. Default Value: 0

2.1.80 BLE_BLELL_CONN_INTR_MASK

Connection Interrupt mask

Address: 0x402E11F0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	CONN_UPDATE_INTR_EN	CE_RX_INT_EN	CE_TX_ACK_INT_EN	CLOSE_CE_INT_EN	START_CE_INT_EN	MAP_UPDT_INT_EN	CONN_ESTB_INT_EN	CONN_CL_INT_EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	None				RW	RW
HW Access	R	R	None				R	R
Name	PING_NEARLY_EXPIRD_INTR	PING_TIMER_EXPIRD_INTR	None [13:10]				RX_BAD_PDU_INT_EN	RX_GOOD_PDU_INT_EN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15	PING_NEARLY_EXPIRD_INTR	If this bit is set ping timer nearly expired interrupt is enabled Default Value: 0
14	PING_TIMER_EXPIRD_INTR	If this bit is set ping timer expired interrupt is enabled. Default Value: 0
9	RX_BAD_PDU_INT_EN	If this bit is set packet receive bad pdu interrupt is enabled. Effective only when bit 6 is set. Default Value: 0
8	RX_GOOD_PDU_INT_EN	If this bit is set packet receive good pdu interrupt is enabled. Effective only when bit 6 is set. Default Value: 0
7	CONN_UPDATE_INTR_EN	If this bit is set connection update interrupt is enabled. Default Value: 0
6	CE_RX_INT_EN	If this bit is set interrupt is enabled for reception of packet in a connection event. Default Value: 0

(continued)

5	CE_TX_ACK_INT_EN	If this bit is set transmission acknowledgement interrupt is enabled: This interrupt is generated to indicate to the firmware that a non-empty packet transmitted is successfully acknowledged by the remote device. For negative acknowledgements from remote device, this interrupt indication is not generated. Default Value: 0
4	CLOSE_CE_INT_EN	If this bit is set connection event closed interrupt is enabled. Default Value: 0
3	START_CE_INT_EN	If this bit is set connection event start interrupt is enabled Default Value: 0
2	MAP_UPDT_INT_EN	If this bit is set, channel map update interrupt is enabled. Default Value: 0
1	CONN_ESTB_INT_EN	If this bit is set connection establishment interrupt is enabled. Default Value: 0
0	CONN_CL_INT_EN	If this bit is set connection closed interrupt is enabled. Default Value: 0

2.1.81 BLE_BLELL_SLAVE_TIMING_CONTROL

slave timing control

Address: 0x402E11F4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SLAVE_TIME_SET_VAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	SLAVE_TIME_ADJ_VAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 8	SLAVE_TIME_ADJ_VAL	Timing adjust value. The internal micro second counter is adjusted to this value whenever slave receives a good access address match at connection anchor point. This will ensure the slave gets synchronized to master timing. Default Value: 190
7 : 0	SLAVE_TIME_SET_VAL	Programmable adjust value to the clock counter when slave is connected Default Value: 150

2.1.82 BLE_BLELL_RECEIVE_TRIG_CTRL

Receive trigger control

Address: 0x402E11F8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		ACC_TRIGGER_THRESHOLD [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	ACC_TRIGGER_TIMEOUT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 8	ACC_TRIGGER_TIMEOUT	If access address match does not occur then within this time from the start of receive operation, the receive operation times out and stops. An internal counter value of 1usec resolution is continuously compared with the value programmed. Max value :0xFF Default Value: 0
5 : 0	ACC_TRIGGER_THRESHOLD	Access address match threshold value. Number of bits of ac-cess address that should match with the expected access ad-dress to trigger an access code match. Max value : 32 (for 32-bit access address) Lower values may be programmed for bad radios or channels but care must be taken to ensure there are no false matches due to reduced number of bits required to match. Default Value: 0

2.1.83 BLE_BLELL_DPLL_CONFIG

DPLL & CY Correlator configuration register

Address: 0x402E1258

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DPLL_CORREL_CONFIG [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DPLL_CORREL_CONFIG [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DPLL_CORREL_CONFIG	If CY_CORREL_EN is 0: [2:0] Read pointer correction on DPLL overflow. Optimal setting is 0x4. [6:4] Minimum distance from Rd ptr to Wr ptr to start read in DPLL. Optimal setting is 0x6. [11:8] Sets lower water mark for DPLL. Optimal setting is 0x2. [15:12] Sets upper water mark for DPLL. Optimal setting is 0x9. If CY_CORREL_EN is 1: [11:0] CY correl Access address compare mask for LSB 12 bits. Ideal value is 0xFFF [15:12] CY correl maximum number of allowed mismatched bits in access address. Ideal value is 0x0. Default Value: 37600

2.1.84 BLE_BLELL_WHITELIST_BASE_ADDR

Whitelist base address

Address: 0x402E1340

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	WL_BASE_ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	WL_BASE_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	WL_BASE_ADDR	Device address values written to white list memory are written as 16-bit wide address. Default Value: 0

2.1.85 BLE_BLELL_CONN_UPDATE_NEW_INTERVAL

Connection update new interval

Address: 0x402E13A4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CONN_UPDT_INTERVAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CONN_UPDT_INTERVAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CONN_UPDT_INTERVAL	This register will have the new connection interval that the hardware will use after the connection update instant. Before the instant, the connection interval in the register CONN_INTERVAL will be used by hardware. Default Value: 0

2.1.86 BLE_BLELL_CONN_UPDATE_NEW_LATENCY

Connection update new latency

Address: 0x402E13A8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CONN_UPDT_SLV_LATENCY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CONN_UPDT_SLV_LATENCY [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CONN_UPDT_SLV_LATENCY	This register will have the new slave latency parameter that the hardware will use after the connection update instant. Before the instant, the connection interval in the register SLAVE_LATENCY will be used by hardware. Default Value: 0

2.1.87 BLE_BLELL_CONN_UPDATE_NEW_SUP_TO

Connection update new supervision timeout

Address: 0x402E13AC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CONN_UPDT_SUP_TO [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CONN_UPDT_SUP_TO [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CONN_UPDT_SUP_TO	This register will have the new supervision timeout that the hardware will use after the connection update instant. Before the instant, the connection interval in the register SUP_TIMEOUT will be used by hardware. Default Value: 0

2.1.88 BLE_BLELL_CONN_UPDATE_NEW_SL_INTERVAL

Connection update new Slave Latency X Conn interval Value

Address: 0x402E13B0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SL_CONN_INTERVAL_VAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	SL_CONN_INTERVAL_VAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	SL_CONN_INTERVAL_VAL	This register will have the new Slave Latency * Conn Interval value that the hardware will use after the connection update instant. Before the instant, the connection interval in the register SL_CONN_INTERVAL will be used by hardware. Default Value: 0

2.1.89 BLE_BLELL_CONN_REQ_WORD0

Connection request address word 0

Address: 0x402E13C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ACCESS_ADDR_LOWER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ACCESS_ADDR_LOWER [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	ACCESS_ADDR_LOWER	This field defines the lower 16 bits of the access address that is to be sent in the connect request packet of the initiator. Default Value: 0

2.1.90 BLE_BLELL_CONN_REQ_WORD1

Connection request address word 1

Address: 0x402E13C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ACCESS_ADDR_UPPER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ACCESS_ADDR_UPPER [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	ACCESS_ADDR_UPPER	This field defines the upper16 bits of the access address that is to be sent in the connect request packet of the initiator. Default Value: 0

2.1.91 BLE_BLELL_CONN_REQ_WORD2

Connection request address word 2

Address: 0x402E13C8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	TX_WINDOW_SIZE_VAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CRC_INIT_LOWER [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 8	CRC_INIT_LOWER	This field defines the lower byte [7:0] of the CRC initialization value. Default Value: 0
7 : 0	TX_WINDOW_SIZE_VAL	window_size along with the window_offset is used to calculate the first connection point anchor point for the master. This shall be a multiple of 1.25 ms in the range of 1.25 ms to the lesser of 10 ms and (connInterval 1.25 ms). Values range from 0 to 10 ms. Default Value: 0

2.1.92 BLE_BLELL_CONN_REQ_WORD3

Connection request address word 3

Address: 0x402E13CC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CRC_INIT_UPPER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CRC_INIT_UPPER [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CRC_INIT_UPPER	This field defines the upper byte [23:8] of the CRC initialization value that is to be sent in the connect request packet of the initiator. Default Value: 0

2.1.93 BLE_BLELL_CONN_REQ_WORD4

Connection request address word 4

Address: 0x402E13D0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	TX_WINDOW_OFFSET [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	TX_WINDOW_OFFSET [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	TX_WINDOW_OFFSET	This is used to determine the anchor point for the master transmission. Range: This shall be a multiple of 1.25 ms in the range of 0 ms to connInterval value. Default Value: 0

2.1.94 BLE_BLELL_CONN_REQ_WORD5

Connection request address word 5

Address: 0x402E13D4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CONNECTION_INTERVAL_VAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CONNECTION_INTERVAL_VAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CONNECTION_INTERVAL_VAL	The value configured in this register determines the spacing between the connection events. This shall be a multiple of 1.25 ms in the range of 7.5 ms to 4.0 s. Default Value: 0

2.1.95 BLE_BLELL_CONN_REQ_WORD6

Connection request address word 6

Address: 0x402E13D8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	SLAVE_LATENCY_VAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	SLAVE_LATENCY_VAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	SLAVE_LATENCY_VAL	The value configured in this field defines the number of consecutive connection events that the slave device is not required to listen for master. The value of connSlaveLatency should not cause a Supervision Timeout. This shall be an integer in the range of 0 to ((connSupervision Timeout/connInterval)-1). connSlaveLatency shall also be less than 500. Default Value: 0

2.1.96 BLE_BLELL_CONN_REQ_WORD7

Connection request address word 7

Address: 0x402E13DC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	SUPERVISION_TIMEOUT_VAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	SUPERVISION_TIMEOUT_VAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	SUPERVISION_TIMEOUT_VAL	This field defines the maximum time between two received Data packet PDUs before the connection is considered lost. This shall be a multiple of 10 ms in the range of 100 ms to 32.0 s and it shall be larger than (1+connSlaveLatency)*connInterval. Default Value: 0

2.1.97 BLE_BLELL_CONN_REQ_WORD8

Connection request address word 8

Address: 0x402E13E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA_CHANNELS_LOWER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA_CHANNELS_LOWER [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATA_CHANNELS_LOWER	This register field indicates which of the data channels are in use. This stores the information for the lower 16 (15:0) data channel indices. 1 indicates the corresponding data channel is used and 0 indicates the channel is unused. Default Value: 0

2.1.98 BLE_BLELL_CONN_REQ_WORD9

Connection request address word 9

Address: 0x402E13E4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA_CHANNELS_MID [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA_CHANNELS_MID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATA_CHANNELS_MID	This register field indicates which of the data channels are in use. This stores the information for the middle 16 (31:16) data channel indices. 1 indicates the corresponding data channel is used and 0 indicates the channel is unused. Default Value: 0

2.1.99 BLE_BLELL_CONN_REQ_WORD10

Connection request address word 10

Address: 0x402E13E8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				RW			
Name	None [7:5]				DATA_CHANNELS_UPPER [4:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4 : 0	DATA_CHANNELS_UPPER	This register field indicates which of the data channels are in use. This stores the information for the upper 5 (36:32) data channel indices. 1 indicates the corresponding data channel is used and 0 indicates the channel is unused. Default Value: 0

2.1.100 BLE_BLELL_CONN_REQ_WORD11

Connection request address word 11

Address: 0x402E13EC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	RW				RW			
Name	SCA_2 [7:5]				HOP_INCREMENT_2 [4:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 5	SCA_2	This field defines the sleep clock accuracies given in ppm. Default Value: 0
4 : 0	HOP_INCREMENT_2	This field is used for the data channel selection process. Default Value: 0

2.1.101 BLE_BLELL_PACKET_COUNTER0

Packet counter 0

Address: 0x402E1400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	PACKET_COUNTER_LOWER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	PACKET_COUNTER_LOWER [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	PACKET_COUNTER_LOWER	Lower 16-bits of the packet counter value passed as part of Nonce for the packet to be encrypted. Default Value: 0

2.1.102 BLE_BLELL_PACKET_COUNTER1

Packet counter 1

Address: 0x402E1404

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	PACKET_COUNTER_MIDDLE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	PACKET_COUNTER_MIDDLE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	PACKET_COUNTER_MIDDLE	Middle 16-bits of the packet counter value passed as part of Nonce for the packet to be encrypted. Default Value: 0

2.1.103 BLE_BLELL_PACKET_COUNTER2

Packet counter 2

Address: 0x402E1408

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	PACKET_COUNTER_UPPER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	PACKET_COUNTER_UPPER	Upper 8 bits of the packet counter value passed as part of Nonce for the packet to be encrypted. Default Value: 0

2.1.104 BLE_BLELL_IV_MASTER0

Master Initialization Vector 0

Address: 0x402E1410

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	IV_MASTER_LOWER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	IV_MASTER_LOWER [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	IV_MASTER_LOWER	This is the lower 16-bits of the IVm field, which contains the masters portion of the initialization vector. Default Value: 0

2.1.105 BLE_BLELL_IV_MASTER1

Master Initialization Vector 1

Address: 0x402E1414

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	IV_MASTER_UPPER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	IV_MASTER_UPPER [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	IV_MASTER_UPPER	This is the upper 16-bits of the IVm field, which contains the masters portion of the initialization vector. Default Value: 0

2.1.106 BLE_BLELL_IV_SLAVE0

Slave Initialization Vector 0

Address: 0x402E1418

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	IV_SLAVE_LOWER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	IV_SLAVE_LOWER [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	IV_SLAVE_LOWER	This is the lower 16-bits of the IVs field, which contains the slaves portion of the initialization vector. Default Value: 0

2.1.107 BLE_BLELL_IV_SLAVE1

Slave Initialization Vector 1

Address: 0x402E141C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	IV_SLAVE_UPPER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	IV_SLAVE_UPPER [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	IV_SLAVE_UPPER	This is the upper 16-bits of the IVs field, which contains the slaves portion of the initialization vector. Default Value: 0

2.1.108 BLE_BLELL_ENC_KEY0

Encryption Key register 0-7

Address: 0x402E1420

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	ENC_KEY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	ENC_KEY [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	ENC_KEY	The encryption key / session key which is used in ECB encryption, CCM encryption and CCM decryption. Default Value: 0

2.1.109 BLE_BLELL_ENC_KEY1

Encryption Key register 0-7

Address: 0x402E1424

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	ENC_KEY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	ENC_KEY [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	ENC_KEY	The encryption key / session key which is used in ECB encryption, CCM encryption and CCM decryption. Default Value: 0

2.1.110 BLE_BLELL_ENC_KEY2

Encryption Key register 0-7

Address: 0x402E1428

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	ENC_KEY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	ENC_KEY [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	ENC_KEY	The encryption key / session key which is used in ECB encryption, CCM encryption and CCM decryption. Default Value: 0

2.1.111 BLE_BLELL_ENC_KEY3

Encryption Key register 0-7

Address: 0x402E142C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	ENC_KEY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	ENC_KEY [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	ENC_KEY	The encryption key / session key which is used in ECB encryption, CCM encryption and CCM decryption. Default Value: 0

2.1.112 BLE_BLELL_ENC_KEY4

Encryption Key register 0-7

Address: 0x402E1430

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	ENC_KEY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	ENC_KEY [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	ENC_KEY	The encryption key / session key which is used in ECB encryption, CCM encryption and CCM decryption. Default Value: 0

2.1.113 BLE_BLELL_ENC_KEY5

Encryption Key register 0-7

Address: 0x402E1434

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	ENC_KEY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	ENC_KEY [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	ENC_KEY	The encryption key / session key which is used in ECB encryption, CCM encryption and CCM decryption. Default Value: 0

2.1.114 BLE_BLELL_ENC_KEY6

Encryption Key register 0-7

Address: 0x402E1438

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	ENC_KEY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	ENC_KEY [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	ENC_KEY	The encryption key / session key which is used in ECB encryption, CCM encryption and CCM decryption. Default Value: 0

2.1.115 BLE_BLELL_ENC_KEY7

Encryption Key register 0-7

Address: 0x402E143C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	ENC_KEY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	ENC_KEY [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	ENC_KEY	The encryption key / session key which is used in ECB encryption, CCM encryption and CCM decryption. Default Value: 0

2.1.116 BLE_BLELL_DATA0

Input / Output Data register

Address: 0x402E1440

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA0 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATA0	Write: Bytes 1 and 0 of the input plain text to be encrypted. Read: Bytes 1 and 0 of the decrypted plain text/ encrypted text. Default Value: 0

2.1.117 BLE_BLELL_DATA1

Input / Output Data register

Address: 0x402E1444

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA1 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA1 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATA1	Write: Bytes 3 and 2 of the input plain text to be encrypted. Read: Bytes 3 and 2 of the decrypted plain text/ encrypted text. Default Value: 0

2.1.118 BLE_BLELL_DATA2

Input / Output Data register

Address: 0x402E1448

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA2 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA2 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATA2	Write: Bytes 5 and 4 of the input plain text to be encrypted. Read: Bytes 5 and 4 of the decrypted plain text/ encrypted text. Default Value: 0

2.1.119 BLE_BLELL_DATA3

Input / Output Data register

Address: 0x402E144C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA3 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA3 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATA3	Write: Bytes 7 and 6 of the input plain text to be encrypted. Read: Bytes 7 and 6 of the decrypted plain text/ encrypted text. Default Value: 0

2.1.120 BLE_BLELL_DATA4

Input / Output Data register

Address: 0x402E1450

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA4 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA4 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATA4	Write: Bytes 9 and 8 of the input plain text to be encrypted. Read: Bytes 9 and 8 of the decrypted plain text/ encrypted text. Default Value: 0

2.1.121 BLE_BLELL_DATA5

Input / Output Data register

Address: 0x402E1454

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA5 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA5 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATA5	Write: Bytes 11 and 10 of the input plain text to be encrypted. Read: Bytes 11 and 10 of the decrypted plain text/ encrypted text. Default Value: 0

2.1.122 BLE_BLELL_DATA6

Input / Output Data register

Address: 0x402E1458

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA6 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA6 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATA6	Write: Bytes 13 and 12 of the input plain text to be encrypted. Read: Bytes 13 and 12 of the decrypted plain text/ encrypted text. Default Value: 0

2.1.123 BLE_BLELL_DATA7

Input / Output Data register

Address: 0x402E145C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA7 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA7 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATA7	Write: Bytes 15 and 14 of the input plain text to be encrypted. Read: Bytes 15 and 14 of the decrypted plain text/ encrypted text. Default Value: 0

2.1.124 BLE_BLELL_DATA8

Input / Output Data register

Address: 0x402E1460

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA8 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA8 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATA8	Write: Bytes 17 and 16 of the input plain text to be encrypted. Read: Bytes 17 and 16 of the decrypted plain text/ encrypted text. Default Value: 0

2.1.125 BLE_BLELL_DATA9

Input / Output Data register

Address: 0x402E1464

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA9 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA9 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATA9	Write: Bytes 19 and 18 of the input plain text to be encrypted. Read: Bytes 19 and 18 of the decrypted plain text/ encrypted text. Default Value: 0

2.1.126 BLE_BLELL_DATA10

Input / Output Data register

Address: 0x402E1468

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA10 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA10 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATA10	Write: Bytes 21 and 20 of the input plain text to be encrypted. Read: Bytes 21 and 20 of the decrypted plain text/ encrypted text. Default Value: 0

2.1.127 BLE_BLELL_DATA11

Input / Output Data register

Address: 0x402E146C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA11 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA11 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATA11	Write: Bytes 23 and 22 of the input plain text to be encrypted. Read: Bytes 23 and 22 of the decrypted plain text/ encrypted text. Default Value: 0

2.1.128 BLE_BLELL_DATA12

Input / Output Data register

Address: 0x402E1470

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA12 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA12 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATA12	Write: Bytes 25 and 24 of the input plain text to be encrypted. Read: Bytes 25 and 24 of the decrypted plain text/ encrypted text. Default Value: 0

2.1.129 BLE_BLELL_DATA13

Input / Output Data register

Address: 0x402E1474

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA13 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA13	Write: Byte 26 of the input plain text to be encrypted. Read: Byte 26 of the decrypted plain text/ encrypted text. Default Value: 0

2.1.130 BLE_BLELL_MIC_IN0

MIC input register

Address: 0x402E1478

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	MIC_IN_LOWER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	MIC_IN_LOWER [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	MIC_IN_LOWER	This is the lower 16-bits of the MIC field used for CCM decryption. Default Value: 0

2.1.131 BLE_BLELL_MIC_IN1

MIC input register

Address: 0x402E147C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	MIC_IN_UPPER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	MIC_IN_UPPER [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	MIC_IN_UPPER	This is the upper 16-bits of the MIC field used for CCM decryption. Default Value: 0

2.1.132 BLE_BLELL_MIC_OUT0

MIC output register

Address: 0x402E1480

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	MIC_OUT_LOWER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	MIC_OUT_LOWER [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	MIC_OUT_LOWER	This is the lower 16-bits of the MIC generated during CCM encryption. Default Value: 0

2.1.133 BLE_BLELL_MIC_OUT1

MIC output register

Address: 0x402E1484

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	MIC_OUT_UPPER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	MIC_OUT_UPPER [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	MIC_OUT_UPPER	This is the lower 16-bits of the MIC generated during CCM encryption. Default Value: 0

2.1.134 BLE_BLELL_ENC_PARAMS

Encryption Parameter register

Address: 0x402E1488

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW					RW	
HW Access	R	R					R	
Name	DIRECTION	PAYLOAD_LENGTH [6:2]					DATA_PDU_HEADER [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	DIRECTION	The directionBit shall be set to 1 for Data Channel PDUs sent by the master and set to 0 for Data Channel PDUs sent by the slave. Default Value: 0
6 : 2	PAYLOAD_LENGTH	Length of the input data. Default Value: 0
1 : 0	DATA_PDU_HEADER	LLID of the packet. Default Value: 0

2.1.135 BLE_BLELL_ENC_CONFIG

Encryption Configuration

Address: 0x402E1490

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [7:3]					DEC_ENC	ECB_CCM	START_PROC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	DEC_ENC	Decryption/Encryption 0 - Encrypt 1 - Decrypt Default Value: 0
1	ECB_CCM	0 - CCM 1 - ECB Default Value: 0
0	START_PROC	1 Start the AES processing Default Value: 0

2.1.136 BLE_BLELL_ENC_INTR_EN

Encryption Interrupt enable

Address: 0x402E1498

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [7:3]					CCM_PROC_INTR_EN	ECB_PROC_INTR_EN	AUTH_PASS_INTR_EN

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	CCM_PROC_INTR_EN	CCM processed interupt enable 0 - Disable 1 - Enable Default Value: 0
1	ECB_PROC_INTR_EN	ECB processed interrupt enable 0 - Disable 1 - Enable Default Value: 0
0	AUTH_PASS_INTR_EN	Authentication interrupt enable 0 - Disable 1 - Enable Default Value: 0

2.1.137 BLE_BLELL_ENC_INTR

Encryption Interrupt status and clear register

Address: 0x402E14A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				W	RW1C	RW1C	RW1C
HW Access	None				RW	RW	RW	RW
Name	None [7:4]				IN_DATA_CLEAR	CCM_PROC_INTR	ECB_PROC_INTR	AUTH_PASS_INTR

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	IN_DATA_CLEAR	Clears the input data. Used for Zero padding of encryption for less than block sized data. Default Value: 0
2	CCM_PROC_INTR	CCM processed interrupt. Writing 1 to this register clears the interrupt Default Value: 0
1	ECB_PROC_INTR	ECB processed interrupt. Writing 1 to this register clears the interrupt. Default Value: 0
0	AUTH_PASS_INTR	Authentication interrupt. 0x1- indicates MIC matched 0x0 indicated MIC mismatched Writing 1 to this register clears the interrupt. Default Value: 0

2.1.138 BLE_BLELL_CONN_TXMEM_BASE_ADDR

Connection TX memory base address

Address: 0x402E1600

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CONN_TX_MEM_BASE_ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CONN_TX_MEM_BASE_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CONN_TX_MEM_BASE_ADDR	Data values written to Tx memory are written as 16-bit wide data. Default Value: 0

2.1.139 BLE_BLELL_CONN_RXMEM_BASE_ADDR

Connection RX memory base address

Address: 0x402E1800

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CONN_RX_MEM_BASE_ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CONN_RX_MEM_BASE_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CONN_RX_MEM_BASE_ADDR	Data values written to Rx memory are written as 16-bit wide data Default Value: 0

2.1.140 BLE_BLELL_PDU_RESP_TIMER

PDU response timer

Address: 0x402E1A04

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	PDU_RESP_TIME_VAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	PDU_RESP_TIME_VAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	PDU_RESP_TIME_VAL	This register is loaded with the count value to monitor the time to get a response for a PDU from peer device. Firmware starts the timer by issuing the command, RESP_TIMER_ON, after it has queued a PDU for transmission, that requires a response. If a response is received, firmware stops and clears the timer by issuing the command RESP_TIMER_OFF. If this timer expires, it results in hardware closing the connection and triggering a conn_closed interrupt. The discon_status field in the Connection status register is set with the appropriate reason. Units : Milliseconds. Resolution : 1.25 ms Default Value: 0

2.1.141 BLE_BLELL_NEXT_RESP_TIMER_EXP

Next response timeout instant

Address: 0x402E1A08

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	NEXT_RESPONSE_INSTANT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	NEXT_RESPONSE_INSTANT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	NEXT_RESPONSE_INSTANT	This field defines the clock instant at which the next PDU response timeout event will occur on a connection. This is with reference to the 16-bit internal reference clock. Default Value: 0

2.1.142 BLE_BLELL_NEXT_SUP_TO

Next supervision timeout instant

Address: 0x402E1A0C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	NEXT_TIMEOUT_INSTANT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	NEXT_TIMEOUT_INSTANT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	NEXT_TIMEOUT_INSTANT	This field defines the clock instant at which the next connection supervision timeout event will occur on a connection This is with reference to the 16-bit internal reference clock. Default Value: 0

2.1.143 BLE_BLELL_LLH_FEATURE_CONFIG

Feature enable

Address: 0x402E1A10

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						SL_DSM_EN	QUICK_TRANSMIT

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	SL_DSM_EN	Enable/Disable Slave Latency Period DSM. Default Value: 1
0	QUICK_TRANSMIT	Quick transmit feature in slave latency is enabled by setting this bit. When slave latency is enabled, this feature enables the slave to transmit in the immediate connection interval, in case required, instead of waiting till the end of slave latency Default Value: 0

2.1.144 BLE_BLELL_WIN_MIN_STEP_SIZE

Window minimum step size

Address: 0x402E1A14

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	STEPUP [7:4]				STEPDN [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	WINDOW_MIN_FW [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 8	WINDOW_MIN_FW	Minimum window interval value programmed by firmware. While the slave receive window is decremented, the windows_min_fw sets the lowest value of the window widen value to ensure packets are not missed. The unit is in microseconds. Default Value: 32
7 : 4	STEPUP	If packets are missed, the reference window is gradually increased by step up size, until it receives 2 consecutive good packets. The unit is in microseconds Default Value: 6
3 : 0	STEPDN	After receiving 2 consecutive good packets the reference window is gradually decremented by step down size until it reaches window minimum. The unit is in microseconds Default Value: 4

2.1.145 BLE_BLELL_SLV_WIN_ADJ

Slave window adjustment

Address: 0x402E1A18

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SLV_WIN_ADJ [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW		
HW Access	None					R		
Name	None [15:11]					SLV_WIN_ADJ [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10 : 0	SLV_WIN_ADJ	Window Adjust value. This value is added to the calculated slave window widening value to be used as final window widen value. Default Value: 16

2.1.146 BLE_BLELL_SL_CONN_INTERVAL

Slave Latency X Conn Interval Value

Address: 0x402E1A1C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	SL_CONN_INTERVAL_VAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	SL_CONN_INTERVAL_VAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	SL_CONN_INTERVAL_VAL	This field defines the (SL*CI) product for the ongoing connection. This value is used in calculation of next connection instant during slave latency. Default Value: 0

2.1.147 BLE_BLELL_LE_PING_TIMER_ADDR

LE Ping connection timer address

Address: 0x402E1A20

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CONN_PING_TIMER_ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CONN_PING_TIMER_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CONN_PING_TIMER_ADDR	The register used to configure the LE Au-thenticated payload Timeout (LE APTO) which is the Maximum amount of time specified between packets authenticated by a MIC. This value of ping timer is in the order of 10ms, valid range 0x1 ~ 0xFFFF Default Value: 0

2.1.148 BLE_BLELL_LE_PING_TIMER_OFFSET

LE Ping connection timer offset

Address: 0x402E1A24

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CONN_PING_TIMER_OFFSET [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CONN_PING_TIMER_OFFSET [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CONN_PING_TIMER_OFFSET	The value of ping timer nearly expired offset in the order of 10ms, valid range 0x0 ~ 0xFFFF. This is the time period after which the ping timer nearly expired interrupt is generated. Default Value: 0

2.1.149 BLE_BLELL_LE_PING_TIMER_NEXT_EXP

LE Ping timer next expiry instant

Address: 0x402E1A28

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	CONN_PING_TIMER_NEXT_EXP [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	CONN_PING_TIMER_NEXT_EXP [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CONN_PING_TIMER_NEXT_EXP	The value of ping timer next expiry instant in the terms of native clock value (least 16 bit value of the 17 bit ping counter). This together with CONN_PING_TIMER_NEXT_EXP_WRAP will provide the correct status of ping timer duration. Default Value: 0

2.1.150 BLE_BLELL_LE_PING_TIMER_WRAP_COUNT

LE Ping Timer wrap count

Address: 0x402E1A2C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	CONN_SEC_CURRENT_WRAP [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	CONN_SEC_CURRENT_WRAP [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CONN_SEC_CURRENT_WRAP	This register holds the current position of the Ping timer. Default Value: 0

2.1.151 BLE_BLELL_TX_EN_EXT_DELAY

Transmit enable extension delay

Address: 0x402E1E00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:5]				TXEN_EXT_DELAY [4:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4 : 0	TXEN_EXT_DELAY	Transmit enable extension delay. This is to extend the active state (high) of rif_tx_en signal after the last bit is sent out from LLH. The unit is in microsecond and the supported range is 00 31 us. Default Value: 5

2.1.152 BLE_BLELL_TX_RX_SYNTH_DELAY

Transmit/Receive enable delay

Address: 0x402E1E04

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	RX_EN_DELAY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	TX_EN_DELAY [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 8	TX_EN_DELAY	The delay used to assert rif_tx_en exactly Tx_tRamp micro-seconds ahead of the first bit of the tx_data, which can be used to turn on the Radio transmitter. The value to be programmed to the Tx_en_delay [7:0] = tx_on_delay - Tx_tRamp tx_on_delay[7:0] = TX_RX_ON_DELAY[15:8]) Tx_tRamp = Radio transmitter ramp_up Default Value: 0
7 : 0	RX_EN_DELAY	The delay used to assert rif_rx_en, Rx_tRamp micro-seconds, ahead of first bit of the expected rx_data, which can be used to turn on the Radio receiver. The value to be programmed to the Rx_en_delay [7:0] = rx_on_delay - Rx_tRamp rx_on_delay[7:0] = TX_RX_ON_DELAY[7:0]) Rx_tRamp = Radio receiver rampup time Default Value: 0

3 BLE Radio (BLERD) Registers

This section discusses the BLERD registers. It lists all the registers in mapping tables, in address order.

3.1 Register Details

Register Name	Address
BLE_BLERD_CFG1	0x402E0000
BLE_BLERD_CFG2	0x402E0004
BLE_BLERD_MODEM	0x402E0008
BLE_BLERD_FSM	0x402E000C
BLE_BLERD_DBUS	0x402E0010
BLE_BLERD_CFGCTRL	0x402E0014
BLE_BLERD_RSSI	0x402E0018
BLE_BLERD_RMAP	0x402E0024
BLE_BLERD_KVCAL	0x402E0028
BLE_BLERD_CFG_1_FCAL	0x402E002C
BLE_BLERD_CFG_2_FCAL	0x402E0030
BLE_BLERD_CFG_3_FCAL	0x402E0034
BLE_BLERD_CFG_4_FCAL	0x402E0038
BLE_BLERD_CFG_5_FCAL	0x402E003C
BLE_BLERD_CFG_6_FCAL	0x402E0040
BLE_BLERD_FCAL_TEST	0x402E0044
BLE_BLERD_TEST	0x402E0048
BLE_BLERD_FPD_TEST	0x402E004C
BLE_BLERD_SY	0x402E0050
BLE_BLERD_TEST2_SY	0x402E0054
BLE_BLERD_TX	0x402E0058
BLE_BLERD_RX	0x402E005C
BLE_BLERD_DIAG1	0x402E0060
BLE_BLERD_IM	0x402E0064
BLE_BLERD_LDO_BYPASS	0x402E0068
BLE_BLERD_LDO	0x402E006C
BLE_BLERD_BB_BUMP1	0x402E0070

Register Name	Address
BLE_BLERD_BB_BUMP2	0x402E0074
BLE_BLERD_BB_XO	0x402E0078
BLE_BLERD_BB_XO_CAPTRIM	0x402E007C
BLE_BLERD_SY_BUMP1	0x402E0080
BLE_BLERD_SY_BUMP2	0x402E0084
BLE_BLERD_TX_BUMP1	0x402E0088
BLE_BLERD_TX_BUMP2	0x402E008C
BLE_BLERD_RX_BUMP1	0x402E0090
BLE_BLERD_RX_BUMP2	0x402E0094
BLE_BLERD_ADC_BUMP1	0x402E0098
BLE_BLERD_ADC_BUMP2	0x402E009C
BLE_BLERD_BALUN	0x402E00A0
BLE_BLERD_CTR1	0x402E00A4
BLE_BLERD_AGC	0x402E00A8
BLE_BLERD_THRSHD1	0x402E00AC
BLE_BLERD_THRSHD2	0x402E00B0
BLE_BLERD_THRSHD3	0x402E00B4
BLE_BLERD_THRSHD4	0x402E00B8
BLE_BLERD_THRSHD5	0x402E00BC
BLE_BLERD_DC	0x402E00C0
BLE_BLERD_IQMIS	0x402E00C4
BLE_BLERD_DCCAL	0x402E00C8
BLE_BLERD_RCCAL	0x402E00CC
BLE_BLERD_DSM1	0x402E00D0
BLE_BLERD_DSM2	0x402E00D4
BLE_BLERD_DSM3	0x402E00D8
BLE_BLERD_DSM4	0x402E00DC
BLE_BLERD_DSM5	0x402E00E0
BLE_BLERD_DSM6	0x402E00E4
BLE_BLERD_MONI	0x402E00E8
BLE_BLERD_DBG_BB	0x402E00EC
BLE_BLERD_DBG_1	0x402E00F0
BLE_BLERD_DBG_2	0x402E00F4
BLE_BLERD_DBG_3	0x402E00F8
BLE_BLERD_READ_IQ_1	0x402E0100
BLE_BLERD_READ_IQ_2	0x402E0104
BLE_BLERD_READ_IQ_3	0x402E0108
BLE_BLERD_READ_IQ_4	0x402E010C

3.1.1 BLE_BLERD_CFG1

Generic configure register.

Address: 0x402E0000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	TX_PA_RAMP_MODE	ADC_IQ_INVERSE	EN_BR_CLK	CLKGATING_DISABLE	RF_PLL_DIRECT	AGC_DISABLE	TX_DATA_INVERSE	RX_DATA_INVERSE

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW		RW	RW	RW
HW Access	R			R		R	R	R
Name	LNA_GAIN [15:13]			CBPF_GAIN [12:11]		BURNIN_CLK_EN	ADC_DC_CAPTURE_EN	RADIO_STANDALONE

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 13	LNA_GAIN	LNA+TIA manually gain setting when AGC is disabled by asserting bit[2]. The gain obtained is a funcion of the LNA gm as well as the TIA feedback resister. 101: VHG, 100: HG, 011: IHG, 010: MH, 001: LG, 000: VLG Default Value: 5
12 : 11	CBPF_GAIN	CBPF manually gain setting when AGC is disabled by asserting bit[2]. This gain is truly reflective of the voltage gain across the CBPF and is determined by the ratio of resisters 11: 15dB, 10: 12dB, 01: 3dB, 00: 0dB Default Value: 3
10	BURNIN_CLK_EN	burn in function mode 1: digital main clock from clk_core. 0: digital main clock from HardIP Default Value: 0
9	ADC_DC_CAPTURE_EN	1: ADC DC capture enable Default Value: 1

(continued)

8	RADIO_STANDALONE	1: radio standalone without link layer controller in SoC, Tx command from reg0x10[13] and RX command from reg0x10[12] Default Value: 0
7	TX_PA_RAMP_MODE	1:ramp to PA gain which given txpa_gain in 2dB steps, starting from min gain. 0: ramp to PA gin which given in txpa_gain in one short from min gain Default Value: 0
6	ADC_IQ_INVERSE	1: swap ADC I, Q path Default Value: 1
5	EN_BR_CLK	1: enable brclk output Default Value: 0
4	CLKGATING_DISABLE	1. disable the clock gating logic golbally. Indepenedent of any other cnditions. None of the clocks can be gated when this bit is set. 0: clock gating logic is enabled, the logic in clk_gen will determine which clocks are to be gated. Default Value: 0
3	RF_PLL_DIRECT	program channel freqency as direct frequency mode. high active. When RF_PLL_DIRECT = 1, RF = reg0x10[11:0] Mhz. When RF_PLL_DIRECT = 0, RF = 2402 + 2*reg7[5:0] Mhz. Default Value: 0
2	AGC_DISABLE	1: disabel the AGC, the LNA+TIA and CBPF gain are given based on bits [15:11] of reg0. Default Value: 0
1	TX_DATA_INVERSE	invert modulation transmit data, high active Default Value: 0
0	RX_DATA_INVERSE	Invert demodulation receiving data,high active Default Value: 0

3.1.2 BLE_BLERD_CFG2

Generic configure register.

Address: 0x402E0004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DAC_REG_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW		RW	RW		RW	
HW Access	R	R		R	R		R	
Name	ADC_DFT_EN	ADC_DFT_MODE [14:13]		DAC_DFT_EN	DAC_DFT_MODE [11:10]		DAC_REG_DATA [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15	ADC_DFT_EN	1: ADC DFT enable Default Value: 0
14 : 13	ADC_DFT_MODE	Reserved - this bit is not available and should be set to 0. Default Value: 0
12	DAC_DFT_EN	1: DAC DFT mode enable Default Value: 0
11 : 10	DAC_DFT_MODE	DAC DFT mode definition 00: DAC input from dac_reg_data[9:0] 01: DAC input as 12Mhz increased value 10: DAC input as 1MHz Sine Wave 11: DAC input as 4MHz SIN wave Default Value: 0
9 : 0	DAC_REG_DATA	DAC input from this register when CFG2_DAC_DFT_EN =1 and dft_mode = 2'b00 Default Value: 512

3.1.3 BLE_BLERD_MODEM

modem configuration

Address: 0x402E0008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW	RW	RW		RW	
HW Access	R		R	R	R		R	
Name	DC_PARAM [7:6]		RESET2_EN	RST_CNT2_SEL	WIDE_SPD [3:2]		NARROW_SPD [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	CW_MODE	ADCDFT_SEL	READ_DC_OFFSET_SEL	LOAD_PREV_GAIN_EN	ADC_PWR_EST_EN	DC_SCALING_EN	ADC_FULL_SWING_DETECT_EN	IMREJ_BYPASS

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15	CW_MODE	1: modulation continue wave output Default Value: 0
14	ADCDFT_SEL	1: ADC DFT capture data after image filter 0: ADC DFT capture data before image filter Default Value: 0
13	READ_DC_OFFSET_SEL	1: read back of analog DC CAL result. 0: read back of DC capture in digital Default Value: 0
12	LOAD_PREV_GAIN_EN	1: load previous RX packet gain setting at first gain change step 0: not load previous RX packet gain. Default Value: 1
11	ADC_PWR_EST_EN	1: power estimation for ADC output is enabled. Default Value: 0

(continued)

10	DC_SCALING_EN	1: DC scaling is enabled in the Demodulator. The Scaling happens when CBPF gain changes. Default Value: 0
9	ADC_FULL_SWING_DETECT_EN	1: select new AGC methodology with ADC full swing detection Default Value: 0
8	IMREJ_BYPASS	bypass image filter in demoulation Default Value: 0
7 : 6	DC_PARAM	demodulation frequency deviation selection 00: 320K, 01: 350K, 10: 400K, 11:430K Default Value: 1
5	RESET2_EN	demodulation soft reset enable, 0: diable, 1: enable soft reset Default Value: 1
4	RST_CNT2_SEL	soft reset condition selection, 0: 32bits all "0'/'1', 1: 16bits all '0'/'1' Default Value: 0
3 : 2	WIDE_SPD	demodulation alpha value for DC offset tracking in wide speed 00: dc value times 8 01: dc value times 10 10: dc value times 12 11: dc value times 14 Default Value: 2
1 : 0	NARROW_SPD	set alpha value for dC offset tracking speed in narrow mode 00: dc value times 1 01: dc value times 2 10: dc value times 3 11: dc value times 4 Default Value: 0

3.1.4 BLE_BLERD_FSM

RFCTRL state information

Address: 0x402E000C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R			R	R	R	R	R
HW Access	W			W	W	W	W	W
Name	RX_STATE [7:5]			ISO_ENABLE	FCAL_PASS_DETECT	LFLDO_OK	LSLDO_OK	XO_AMP_DETECT

Bits	15	14	13	12	11	10	9	8
SW Access	R		R			R		
HW Access	W		W			W		
Name	STATE [15:14]		SY_STATE [13:11]			TX_STATE [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 14	STATE	RFCTRL major state, 00: sleep mode, 11: idle mode, 10: TX mode, 01: RX mode Default Value: 3
13 : 11	SY_STATE	RFCTRL SYNTH state 000: SY off, 001: SY Regulator power up, 010: SY VCO pup up 011: SY LO path power up, 100: Frequency calibration, 101: PLL setting. 110: PLL locked Default Value: 0

(continued)

10 : 8	TX_STATE	RFCTRL TX state 000: TX Off 001: TX Regulator Powerup 010: TX Baseband Powerup 011: KV Calibration 100: TX PLL Settling 101: TX Ready Default Value: 0
7 : 5	RX_STATE	RFCTRL RX state 000: RX Off 001: RX Regulator Powerup 010: RX Baseband and IF Powerup 011: DC Calibration 100: RX Wait for PLL settling 101: RX ADC DC value capture 110: RX Receive ON Default Value: 0
4	ISO_ENABLE	monitor isolation cell enable signal 1: isolation cell enabled. Default Value: 1
3	FCAL_PASS_DETECT	TX balun power detector, 1: Frequency calibration has passed. 0: Frequency calibration has failed Default Value: 0
2	LFLDO_OK	1: LF LDO powered up Default Value: 0
1	LSLDO_OK	1: LS LDO powered up Default Value: 0
0	XO_AMP_DETECT	1: XO is oscillating reached 60% ampitude. 0: XO is no oscillating or not reached 60% ampitude. BLERD_BB_XO[1] determines fast or normal charge. XO within 50ppm needs 2 times of XO detection BLERD_BB_XO[1] XO_amp_detect XO stable 1 320us 640us 0 1120us 2.24ms Default Value: 0

3.1.5 BLE_BLERD_DBUS

RFCTRL mode transition control

Address: 0x402E0010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	RF_FREQ [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW			
HW Access	R	R	R	R	R			
Name	XTAL_ENABLE	ISOLATE_N	DIRECT_TXEN	DIRECT_RXEN	RF_FREQ [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15	XTAL_ENABLE	crystal enable. High active Default Value: 0
14	ISOLATE_N	force isolation cell enable of analog / digital boundary. low active Default Value: 1
13	DIRECT_TXEN	When cfg1_radio_standalone =1, debus_direct_rxen replace dbus_rx_en Default Value: 0
12	DIRECT_RXEN	When cfg1_radio_standalone =1, debus_direct_rxen replace dbus_rx_en Default Value: 0
11 : 0	RF_FREQ	When CFG1_RF_PLL_DIRECT=1, RF frequency is direct program from DBUS register [11:0] Default Value: 2450

3.1.6 BLE_BLERD_CFGCTRL

RFCTRL running configuration

Address: 0x402E0014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW				
HW Access	R	R	R	R				
Name	DCCAL_MODE	DCCAL_RERUN	IGNORE_FRAC	DSM_MODE [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	RW	None			RW	RW	RW	RW
HW Access	R	None			R	R	R	R
Name	TESTMODE_EN	None [14:12]			FCAL_RERUN	KVCAL_RERUN	RCCAL_MODE	RCCAL_RERUN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15	TESTMODE_EN	1: enables the test mode feature of RFCTRL Default Value: 0
11	FCAL_RERUN	1: KVCAL will be force rerun when cfgctrl_testmode_en = 1 Default Value: 0
10	KVCAL_RERUN	1: FCAL will be force rerun when cfgctrl_testmode_en = 1 Default Value: 0
9	RCCAL_MODE	0: normal mode 1: slow mode, The timer for each setp in calibration is doubled with normal mode Default Value: 0
8	RCCAL_RERUN	1: RC-cal force to rerun when cfgctrl_testmode_en = 1 Default Value: 0
7	DCCAL_MODE	0: RX DC offset calibration in run normal mode 1: RX DC offset calibration is run in slow mode. Here each step in calibration is given double time compared to the normal mode Default Value: 0

(continued)

6	DCCAL_RERUN	1: DC CAL is forced to run when cfgctrl_testmode_en = 1 Default Value: 0
5	IGNORE_FRAC	0: Do not ignore fractional part in DSM (Frac-N PLL). 1: Ignore the fractional part in DSM (Int-N PLL). Default Value: 0
4 : 0	DSM_MODE	Cfgctrl_dsm_mode[4]: 1b0: Third order PLL is used in TX mode, this is not effective in RX mode 1b1: First order PLL is used in TX mode, this is not effective in RX mode Cfgctrl_dsm_mode[3:2] The following bits determine the DSM mode in TX 00: Input dither but no initial condition for DSM 01: Input dither and initial condition to DSM. 10: No input dither and initial condition 11: No input dither but initial condition is given Cfgctrl_dsm_mode[1:0] The following bits determine the DSM mode in RX 00: Input dither but no initial condition for DSM 01: Input dither and initial condition to DSM. 10: No input dither and initial condition 11: No input dither but initial condition is given Default Value: 24

3.1.7 BLE_BLERD_RSSI

RX envelpe detector and RSSI value

Address: 0x402E0018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	R						
HW Access	None	W						
Name	None	PREFILT [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None	R						
HW Access	None	W						
Name	None	POSTFILT [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
14 : 8	POSTFILT	RSSI value after the filter in digital, 0 represents -85dBm Default Value: 0
6 : 0	PREFILT	RSSI value before the filter in thd digital, 0 represents -85dBm Default Value: 0

3.1.8 BLE_BLERD_RMAP

BG LDO bypass mode

Address: 0x402E0024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	BB_BYPASS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	BB_BYPASS [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description

(continued)

15 : 0	BB_BYPASS	[0]:bypass lsldo ok signal if set this bit [1]:bypass lfldo ok signal if set this bit [2]:bypass xo amp detect if set this bit [3]:BG output is force external by enabling T-gate if set this bit [4]: bypass LF LDO and the line supply is directly given out as regulator output. This field should not be enable if line supply is moreh than 2.1V. This should not toggled in Scan Mode [5]: bypass LS LDO and the line supply is directly given out as regulator output. This field should not be enable if line supply is moreh than 2.1V. This should not toggled in Scan Mode [6]: bypass BBV2LDO and the line supply is directly given out as regulator output. This field should not be enable if line supply is moreh than 2.1V. This should not toggled in Scan Mode [7]:spare bit [8]:0: LF LDO power down controlled by m0s8blerd 1: powerdown LF LDO [9]:0: LS LDO power down controlled by m0s8blerd 1: power done LS LDO [10]:0: BG LDO power down controlled by m0s8blerd 1: power down BG LDO [11]:0: V2ILDO power down controlled by m0s8blerd 1: power done V2ILDO [15:12]:reserved for furture Default Value: 0

3.1.9 BLE_BLERD_KVCAL

KVCAL running configuration

Address: 0x402E0028

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW		RW	
HW Access	R				R		R	
Name	EXP_FREQ_DIFF [7:4]				RUN_DURATION [3:2]		DAC_STEP [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				EXP_FREQ_DIFF [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11 : 4	EXP_FREQ_DIFF	This expected difference in KVCAL configuration counts(100 counts for an idela modulalation path gain) Default Value: 100
3 : 2	RUN_DURATION	This values tells by what value should the DAC be offset from the mid-code, when the KVCAL is running. 00 : 512 (1MHz deviation). 01: 376 (0.75 Mhz deviation). 10: 256 (0.5 Mhz deviation) 11 : 128 (0.25 Mhz deviation Default Value: 0
1 : 0	DAC_STEP	This values tells by what value should the DAC be offset from the mid-code, when the KVCAL is running. 00 : 512 (1MHz deviation). 01: 376 (0.75 Mhz deviation). 10: 256 (0.5 Mhz deviation) 11 : 128 (0.25 Mhz deviation Default Value: 0

3.1.10 BLE_BLERD_CFG_1_FCAL

FCAL running configure 5_6

Address: 0x402E002C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW						
HW Access	R	R						
Name	COARSE_FRAMES_7	COARSE_FRAMES_6 [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW					
HW Access	None		R					
Name	None [15:14]		COARSE_FRAMES_7 [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
13 : 7	COARSE_FRAMES_7	numbere of frames to run for the calibration 7th coarse bit Default Value: 7
6 : 0	COARSE_FRAMES_6	numbere of frames to run for the calibration 6th coarse bit Default Value: 7

3.1.11 BLE_BLERD_CFG_2_FCAL

FCAL running configure 7_2

Address: 0x402E0030

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW						
HW Access	R	R						
Name	COARSE_FRAMES_5	COARSE_FRAMES_4 [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW					
HW Access	None		R					
Name	None [15:14]		COARSE_FRAMES_5 [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
13 : 7	COARSE_FRAMES_5	numbere of frames to run for the calibration 5th coarse bit Default Value: 7
6 : 0	COARSE_FRAMES_4	numbere of frames to run for the calibration 4th coarse bit Default Value: 7

3.1.12 BLE_BLERD_CFG_3_FCAL

FCAL running configure 3_4

Address: 0x402E0034

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW						
HW Access	R	R						
Name	COARSE_FRAMES_3	COARSE_FRAMES_2 [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW					
HW Access	None		R					
Name	None [15:14]		COARSE_FRAMES_3 [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
13 : 7	COARSE_FRAMES_3	numbere of frames to run for the calibration 3rd coarse bit Default Value: 7
6 : 0	COARSE_FRAMES_2	numbere of frames to run for the calibration 2nd coarse bit Default Value: 7

3.1.13 BLE_BLERD_CFG_4_FCAL

FCAL running configure 0_1

Address: 0x402E0038

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW						
HW Access	R	R						
Name	COARSE_FRAMES_1	COARSE_FRAMES_0 [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW					
HW Access	None		R					
Name	None [15:14]		COARSE_FRAMES_1 [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
13 : 7	COARSE_FRAMES_1	numbere of frames to run for the calibration 1st coarse bit Default Value: 7
6 : 0	COARSE_FRAMES_0	numbere of frames to run for the calibration 0th coarse bit Default Value: 7

3.1.14 BLE_BLERD_CFG_5_FCAL

FCAL running framer fine

Address: 0x402E003C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW						
HW Access	R	R						
Name	CNT_SEL	FINE_FRAMES [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW		
HW Access	None					R		
Name	None [15:11]					CNT_SEL [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10 : 7	CNT_SEL	select which count should be reflected in the FCAL_DBG_2 and FCAL_DBG_3 registers 4d1: FCAL 7th Coarse bit calibration 4d2: FCAL 6th Coarse bit calibration 4d3: FCAL 5th Coarse bit calibration 4d4: FCAL 4th Coarse bit calibration 4d5: FCAL 3rd Coarse bit calibration 4d6: FCAL 2nd Coarse bit calibration 4d7: FCAL 1st Coarse bit calibration 4d8: FCAL 0th Coarse bit calibration 4d9: FCAL 3rd Fine bit calibration 4d10: FCAL 2nd Fine bit calibration 4d11: FCAL 1st Fine bit calibration 4d12: FCAL 0th Fine bit calibration 4d13: VCO Open loop count 4d14: KVCAL Observed Count 4d15: KVCAL Gain Default: Gives zero output Default Value: 15
6 : 0	FINE_FRAMES	numbere of frames to run for all the calibration of all the Fine bits Default Value: 14

3.1.15 BLE_BLERD_CFG_6_FCAL

FCAL running VCO OL

Address: 0x402E0040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	FRAMES_VCO_OL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW		RW	RW	RW		
HW Access	None	R		R	R	R		
Name	None	DRIFT_CHECK [14:13]		DRIFT_CHECK_EN	VCO_OL_ENBL	FRAMES_VCO_OL [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
14 : 13	DRIFT_CHECK	00: start drift check when the TX driver is powered up 01: start drift check measurement 100us after TX driver is power ed up 10: start drift check measurement 200us after the TX driver is powered up 11: start drift check measurement 300us after the TX drive is powered up Default Value: 0
12	DRIFT_CHECK_EN	enables the FCAL drift check, This needs to be set prior to the TX burst being programmed as it affects the timing sequence. Ensure that FB buffer has not been powered down such that the FCAL counter is left alive. This requires a cahgne to reg0xcc[5] to be set to 0 (disable FB buffer power save). This needs to be set piror to placing the part in TX mode Default Value: 0
11	VCO_OL_ENBL	1:enable vco openloop characterization Default Value: 0
10 : 0	FRAMES_VCO_OL	Number of frames to run in VCO openloop Characterization . If bit[12] fcal_drift_check_en is asserted, then this field indicates for how many frames the FCAL drift has to be measured Default Value: 512

3.1.16 BLE_BLERD_FCAL_TEST

FCAL test mode configuration

Address: 0x402E0044

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	COARSE [7:4]				FINE [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW	RW	RW	RW			
HW Access	None	R	R	R	R			
Name	None	LOOP_POLARITY	CNT_POLARITY	MODE	COARSE [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
14	LOOP_POLARITY	1: Inverts the polarity of the FCAL loop. In this mode the DCAP code is decreased if observed count is greater than target count. 0: This is normal FCAL loop, where DCAP code is increased if the observed count is greater than target_count Default Value: 0
13	CNT_POLARITY	1: Inverts the polarity of the FCAL counter output coming in to the RFCTRL Default Value: 0
12	MODE	force the coarse and fine bits of FCAL output enable, high active Default Value: 0
11 : 4	COARSE	force coarse bits output of the FCAL engine when test_mode is set Default Value: 0
3 : 0	FINE	force fine bits output of the FCAL engine when test_mode is set Default Value: 0

3.1.17 BLE_BLERD_TEST

RCCAL and procmon test configuration

Address: 0x402E0048

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW						
HW Access	R	R						
Name	KVCAL_MODE	KVCAL_GAIN [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW	RW	RW				
HW Access	None	R	R	R				
Name	None	FRCCAL_POLARITY	FRCCAL_MODE	FRCCAL_CODE [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
14	FRCCAL_POLARITY	1: invert RC CAL polarity. Default Value: 0
13	FRCCAL_MODE	1: RC-CAL code is forced to the given code Default Value: 0
12 : 8	FRCCAL_CODE	this code is forced as the RC_CAL code when test_frccal_mode = 1 Default Value: 0
7	KVCAL_MODE	1: KV-CAL code is forced to the given code Default Value: 0
6 : 0	KVCAL_GAIN	this code is forced as the KV_CAL code when when test_kvcal_mode = 1 Default Value: 0

3.1.18 BLE_BLERD_FPD_TEST

LDOs test

Address: 0x402E004C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	None		RW	RW	RW	None	RW
HW Access	R	None		R	R	R	None	R
Name	FAST_CHARGE	None [6:5]		BB_RCCAL_BLOCK	BB_XO_BUF_SY	BB_XO_BUF_ADC	None	BB_FPUP_XO_BUF_ALL

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		R	R	R	R	R	R
Name	None [15:14]		FPUP_ALL	BALUN_CTUNE	BALUN_HFLDO	SY_LDOFFFB	SY_LDOLOPATH	SY_LDOVCO

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
13	FPUP_ALL	1: This is used to force powerup the blocks controlled by this register. Fpd has higher precedence over force_powerup if cfgctrl_testmode_en = 1 Default Value: 0
12	BALUN_CTUNE	1: force powerdown Balun Ctune block if cfgctrl_testmode_en = 1 Default Value: 0
11	BALUN_HFLDO	1: Balun HF LDO is forced power down if cfgctrl_testmode_en = 1 Default Value: 0
10	SY_LDOFFFB	1: force power down SY LDO LOFFFB if cfgctrl_testmode_en = 1 Default Value: 0
9	SY_LDOLOPATH	1: force power down SY LDO LOPATH if cfgctrl_testmode_en = 1 Default Value: 0
8	SY_LDOVCO	1: force power down SY LDOVCO if cfgctrl_testmode_en = 1 Default Value: 0

(continued)

7	FAST_CHARGE	1: force power the fast charge bit for LDO Lopath if cfgctrl_testmode_en = 1 Default Value: 0
4	BB_RCCAL_BLOCK	1: forcefully powers down the RC CAL block if cfgctrl_testmode_en = 1 Default Value: 0
3	BB_XO_BUF_SY	1: forcefully powers down xo buffer to synth if cfgctrl_testmode_en = 1 Default Value: 0
2	BB_XO_BUF_ADC	1: forcefully powers down xo buffer to ADC if cfgctrl_testmode_en = 1 Default Value: 0
0	BB_FPUP_XO_BUF_ALL	1: forcefully powers down all the buffers in XO if cfgctrl_testmode_en = 1 Default Value: 0

3.1.19 BLE_BLERD_SY

SY test configuration 1

Address: 0x402E0050

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	None	RW	RW	RW
HW Access	R	R	R	R	None	R	R	R
Name	TEST_FPD_FCAL	TEST_FPD_DIVN	TEST_FPD_DIV2_BUF	TEST_FPD_LOPATHDIVN	None	TEST_FPD_DIV2	TEST_FPD_VCO	TEST_FPD_IBIAS

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	TEST_FPUP_ALL	TEST_FPD_LOOP_FREEZE	TEST_FPD_OPENLOOP	TEST_FPD_FCAL_AMP	TEST_FPD_TX_POWERSAVE	TEST_FPD_DIV2_DRV	TEST_FPD_LOPATHTX	TEST_FPD_CPLPF

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15	TEST_FPUP_ALL	1: all the blocks in SY are forced power up if cfgctrl_testmode_en = 1 Default Value: 0
14	TEST_FPD_LOOP_FREEZE	1: loop freeze is forced low if cfgctrl_testmode_en = 1 Default Value: 0
13	TEST_FPD_OPENLOOP	The loop_freeze is forced low if this bit is asserted and cfgctrl_testmode_en = 1 Default Value: 0
12	TEST_FPD_FCAL_AMP	The fcal amp is forced powered down, if this bit is asserted and cfgctrl_testmode_en = 1 Default Value: 0
11	TEST_FPD_TX_POWERSAVE	The fcal amp is forced powered down, if this bit is asserted and cfgctrl_testmode_en = 1 Default Value: 0
10	TEST_FPD_DIV2_DRV	the TX powersave bit si force to zero if this bit is asserted and and cfgctrl_testmode_en = 1 Default Value: 0

(continued)

9	TEST_FPD_LOPATHTX	SY LOpath TX buffer is forced powered down, if this bit is set and cfgctrl_testmode_en = 1 Default Value: 0
8	TEST_FPD_CPLPF	SY CP and LPF are forced powered down, if this bit is set and cfgctrl_testmode_en = 1 Default Value: 0
7	TEST_FPD_FCAL	SY FCAL counter is forced powered down, if this bit is set and cfgctrl_testmode_en = 1 Default Value: 0
6	TEST_FPD_DIVN	SY DIVN block is forced powered down, if this bit is set and cfgctrl_testmode_en = 1 Default Value: 0
5	TEST_FPD_DIV2_BUF	SY LOpath FCAL buffer is forced powered down, if this bit is set and cfgctrl_testmode_en = 1 Default Value: 0
4	TEST_FPD_LOPATHDIVN	SY LOpath DIVN buffer is forced powered down, if this bit is set and cfgctrl_testmode_en = 1 Default Value: 0
2	TEST_FPD_DIV2	SY high speed divider block is forced powered down, if this bit is set and cfgctrl_testmode_en = 1 Default Value: 0
1	TEST_FPD_VCO	SY VCO block is forced powered down, if this bit is set and RF_TST_EN = 1 Default Value: 0
0	TEST_FPD_IBIAS	SY IBIAS block is forced powered down, if this bit is set and cfgctrl_testmode_en = 1 Default Value: 0

3.1.20 BLE_BLERD_TEST2_SY

SY test configuration 2

Address: 0x402E0054

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	None	RW			
HW Access	R	R	R	None	R			
Name	FORCE_DSM_FRAC	FORCE_DSM_RUN	FPD_DSM_RUN	None	ICP_CODE [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DSM_FRAC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 8	DSM_FRAC	fore bits for DSM fractional bits if test2_sy_force_dsm_frac=1 Default Value: 0
7	FORCE_DSM_FRAC	1: Force the MSB 8bit of the DSM fractional part with Reg[15-8]. The LSB bits should be 0. 0: DSM fractional bits will be driven by Timing Engine Default Value: 0
6	FORCE_DSM_RUN	DSM_run signal is asserted if this bit is set and rfctrl_testmode_en = 1 Default Value: 0
5	FPD_DSM_RUN	DSM run signal is de-asserted if this bit si set and rfctrl_testmode_en = 1 Default Value: 0
3 : 0	ICP_CODE	ICP code will be programmed with these bits. Default Value: 0

3.1.21 BLE_BLERD_TX

transmit test configuration

Address: 0x402E0058

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	TEST_FPD_KVM_PFDEV	TEST_FPD_KVM_NFDEV	TEST_FPD_FN_TXEN	TEST_FPD_PREDRIVER	TEST_FPD_DRIVER	TEST_FPD_LPF	TEST_FPD_DAC	TEST_FPD_IBIAS

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							TEST_FPUP_TX_ALL

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	TEST_FPUP_TX_ALL	force powerup all the TX blocks if rfctrl_testmode_en = 1 Default Value: 0
7	TEST_FPD_KVM_PFDEV	modulator will not enable positive 1Mhz frequency deviation mode, if this bit is set and rfctrl_testmdoe_en = 1 Default Value: 0
6	TEST_FPD_KVM_NFDEV	modulator will not enable negative 1Mhz frequency deviation mode, if this bit is set and rfctrl_testmdoe_en = 1 Default Value: 0
5	TEST_FPD_FN_TXEN	the modulator control signal f_n_txen is deasswerted, if this bit is set and rfctrl_testmode_en = 1 Default Value: 0
4	TEST_FPD_PREDRIVER	1: forced power down TX pre-drive if rfctrl_testmode_en = 1 Default Value: 0
3	TEST_FPD_DRIVER	1: forced power down TX driver if rfctrl_testmode_en = 1 Default Value: 0

(continued)

2	TEST_FPD_LPF	1: forced power down TX LPF if rfctrl_testmode_en = 1 Default Value: 0
1	TEST_FPD_DAC	1: forced power down TX DAC if rfctrl_testmode_en = 1 Default Value: 0
0	TEST_FPD_IBIAS	1: forced power down TX ibias if rfctrl_testmode_en = 1 Default Value: 0

3.1.22 BLE_BLERD_RX

RX test configuration

Address: 0x402E005C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	TEST_FPD_MIXER_LO	TEST_FPD_TIA	TEST_FPD_BPF	TEST_FPD_ADC_QREFGEN	TEST_FPD_ADC_QCORE	TEST_FPD_ADC_IREFGEN	TEST_FPD_ADC_ICORE	TEST_FPD_IBIAS

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [15:13]			TEST_FPUP_RX_ALL	TEST_FPD_FN_RXEN	TEST_FPD_LNA_HIZ	TEST_FPD_LNA	TEST_FPD_MIXER_RF

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
12	TEST_FPUP_RX_ALL	1:force powerup all RX blocks,if this bit is set and rfctrl_testmode_en = 1 Default Value: 0
11	TEST_FPD_FN_RXEN	1:the demodulator control signal f_n_rxen is deasserted if this bit is set and rfctrl_tesmode_en=1 Default Value: 0
10	TEST_FPD_LNA_HIZ	1:LNA HIZ signal is deasserted, if this bit is set and rfctrl_testmode_en = 1 Default Value: 0
9	TEST_FPD_LNA	1: force power down RX LNA if this bit is set and rfctrl_testmode_en = 1 Default Value: 0
8	TEST_FPD_MIXER_RF	1: force power down RX MIXER RF block if rfctrl_testmode_en = 1. Default Value: 0
7	TEST_FPD_MIXER_LO	1:force power down RX MIXER LO block if this bit is set and rfctrl_testmode_en = 1 Default Value: 0

(continued)

6	TEST_FPD_TIA	1:force power down RX TIA if this bit is set and rfctrl_testmode_en = 1 Default Value: 0
5	TEST_FPD_BPF	1:force power down RX BPF, if this bit is set and rfctrl_testmode_en = 1 Default Value: 0
4	TEST_FPD_ADC_QREFGEN	1:force power donw RX ADC QREF generation lock,if this bit is set and rfctrl_testmode_en = 1 Default Value: 0
3	TEST_FPD_ADC_QCORE	1:force power down RX ADC Q Core block is force powerdown if this bit is set and rfctrl_testmode_en = 1 Default Value: 0
2	TEST_FPD_ADC_IREFGEN	1:force power donw RX ADC IREF generation lock,if this bit is set and rfctrl_testmode_en = 1 Default Value: 0
1	TEST_FPD_ADC_ICORE	1:force power down RX ADC I Core block is force powerdown if this bit is set and rfctrl_testmode_en = 1 Default Value: 0
0	TEST_FPD_IBIAS	1:force power down RX IBIAS block if this bit is set and rfctrl_testmode_en = 1 Default Value: 0

3.1.23 BLE_BLERD_DIAG1

RF diagnostics configuration 1

Address: 0x402E0060

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW			RW				RW
HW Access	R			R				R
Name	SEL [7:5]			CODE [4:1]				DISABLE

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						SEL [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description

(continued)

9 : 5	SEL	This needs to be decoded and given to HardIP 5'd31 Injection_Monitor 5'd30 SY_PDCPLPF 5'd29 SY_DIVN_FCAL 5'd28 Reserved 5'd27 SY LO Path 5'd26 SY IBIAS 5'd25 SY LDO FFFB 5'd24 Reserved 5'd23 SY LDO Lopath 5'd22 TX Driver 5'd21 reserved 5'd20 TX LPF 5'd19 TX DAC 5'd18 TX IBIAS 5'd17 RX LNA 5'd16 RX Mixer 5'd15 RX TIA 5'd14 RX CBPF1 5'd13 RX CBPF2 5'd12 RX ADC 5'd11 RX IBIAS 5'd10 BB XO 5'd9 BB Refcore 5'd8 BB RCCAL 5'd7 BB LFLDO 5'd6 BB BGAP 5'd5 BB_V2I 5'd4 BB_V2ILDO 5'd3 BB_LSLDO 5'd2 BB_TRANCHAR 5'd1 Balun 5'd0 HFLDO Default Value: 0
4 : 1	CODE	global diagnositic code, this is given to all the blocks. The block wihich has the diagnostics enabled will decode this code Default Value: 0
0	DISABLE	1: diagnaositcs fro all blocks are disabled 0: diagnostics are enabled an global level. The diagnostics for each block is controlled by as corresponding block level diag_enable signal Default Value: 1

3.1.24 BLE_BLERD_IM

inject monitor configuration

Address: 0x402E0064

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW	RW				RW
HW Access	R		R	R				R
Name	DIAG_INJ_CODE [7:6]		DIAG_INJ_DISABLE	DIAG_MONI_CODE [4:1]				DIAG_MON_DISABLE

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW				RW	RW	
HW Access	R	R				R	R	
Name	DIAG_RESV	DIAG_BUMP [14:11]				DIAG_LOOPBACK	DIAG_INJ_CODE [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15	DIAG_RESV	reserved for feature Default Value: 0
14 : 11	DIAG_BUMP	diag bump code im_diag_bump[3:2] 2b00: Mon OTA ref. voltage is 0.9V 2'b01: Mon OTA ref: vlotage is 1.0V 2'b10: Mon OTA ref: vlotage is 1.1V 2'b11: Mon OTA ref: vlotage is 0.8V im_diag_bump[1:0] 2b00: Inj OTA ref. voltage is 0.9V 2'b01: Inj OTA ref: vlotage is 1.0V 2'b10: Inj OTA ref: vlotage is 1.1V 2'b11: Inj OTA ref: vlotage is 0.8V Default Value: 0
10	DIAG_LOOPBACK	1: This will be used to monitor various outputs in the chip and inject them to on-chip ADC 0: no monitor to injection loopback Default Value: 0

(continued)

9 : 6	DIAG_INJ_CODE	injection code. This determines for which block is the injection enabled Code: inj_p inj_n 4h1: vin_lpf unused 4d 4 I TIA in_p I TIA in_n 4d 5 Q TIA in_p Q TIA in_n 4d 6 I TIA in_p Q TIA in_n 4d 7 Q TIA in_p I TIA in_n 4d 8 I ADC in_p I ADC in_n 4d 9 Q ADC in_p Q ADC in_n 4h0, 4d2, 4d2, 4d10, 4d11, 4d12, 4d13, 4d14, 4d15 are unused Default Value: 0
5	DIAG_INJ_DISABLE	1:globally disable the injection Default Value: 1
4 : 1	DIAG_MONI_CODE	monitor code, this determine from lock the monitor is being driven Code moni_p moni_n 4d 1 dac_outp gnd 4d 2 lpf_out gnd 4d 4 I TIA out_p I TIA out_n 4d 5 Q TIA out_p Q TIA out_n 4d 6 I CBPF out_p I CBPF out_n 4d 7 Q CBPF out_p Q CBPF out_n 4d 8 I CBPF out_p Q CBPF out_n 4d 9 Q CBPF out_p I CBPF out_n 4d0, 4d10, 4d11, 4d12, 4d13, 4d14, 4d15: unused Default Value: 0
0	DIAG_MON_DISABLE	1:globally disable the monitor Default Value: 1

3.1.25 BLE_BLERD_LDO_BYPASS

LDOs bypass configuration

Address: 0x402E0068

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW	RW	RW	RW
HW Access	R				R	R	R	R
Name	RESV_LDOBP [7:4]				HFLDO	SYL-DOFFFB	SYLDOLO-PATH	SYLDOV-CO

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	RESV_LDOBP [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 4	RESV_LDOBP	reserved for feature Default Value: 0
3	HFLDO	1: BB SY HF LDO is bypassed. It should not be enable if line voltage is more than 2.1V. This bit should not toggle in scan mode Default Value: 0
2	SYLDOFFFB	1: Synth LDO_FFFB is bypassed. It should not be enable if line voltage is more than 2.1V. This bit should not toggle in scan mode Default Value: 0
1	SYLDOLOPATH	1: Synth LDO_LOPATH is bypassed. It should not be enable if line voltage is more than 2.1V. This bit should not toggle in scan mode Default Value: 0
0	SYLDOVCO	1: Synth LDO_VCO is bypassed. It should not be enable if line voltage is more than 2.1V. This bit should not toggle in scan mode Default Value: 0

3.1.26 BLE_BLERD_LDO

bump bit for LDOs Atlantis

Address: 0x402E006C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW		RW		RW		
HW Access	R	R		R		R		
Name	BUMP_SY_LHV	BUMP_SY_LOPATH [6:5]		BUMP_SY_VCO [4:3]		BUMP_BALUM_HF [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			RW
HW Access	R				R			R
Name	REV_LDO [15:12]				BUMP_SY_FFFB [11:9]			BUMP_SY_LHV

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 12	REV_LDO	received for feature Default Value: 0
11 : 9	BUMP_SY_FFFB	3d0: FF and FB LDO outputs are 1.800V 3d1: FF and FB LDO outputs are 1.846V 3d2: FF and FB LDO outputs are 1.894V 3d3: FF and FB LDO outputs are 1.946V 3d4: FF and FB LDO outputs are 2.000V 3d5: FF and FB LDO outputs are 1.649V 3d6: FF and FB LDO outputs are 1.701V 3d7: FF and FB LDO outputs are 1.756V Default Value: 0
8 : 7	BUMP_SY_LHV	2d0: HV LDO outputs are 1.894V 2d1: HV LDO outputs are 2.000V 2d2: HV LDO outputs are 1.800V 2d3: HV LDO outputs are 1.846V Default Value: 0

(continued)

6 : 5	BUMP_SY_LOPATH	2d0: LOPATH LDO outputs are 1.762V 2d1: LOPATH LDO outputs are 1.861V 2d2: LOPATH LDO outputs are 1.673V 2d3: LOPATH LDO outputs are 1.716V Default Value: 0
4 : 3	BUMP_SY_VCO	2d0: VCO LDO outputs are 1.413V 2d1: VCO LDO outputs are 1.494V 2d2: VCO LDO outputs are 1.329V 2d3: VCO LDO outputs are 1.371V Default Value: 0
2 : 0	BUMP_BALUM_HF	3d0: HF LDO output is 1.800V 3d1: HF LDO output is 1.846V 3d2: HF LDO output is 1.894V 3d3: HF LDO output is 1.946V Default Value: 0

3.1.27 BLE_BLERD_BB_BUMP1

bump bit for LDOs BB,TXRX

Address: 0x402E0070

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW			RW			RW	
HW Access	R			R			R	
Name	LFLDO [7:5]			V2I_REG [4:2]			REFCORE_VDD [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	None	RW		RW		
HW Access	R	R	None	R		R		
Name	FPD_REFORCE	FORCE_BGSTARTUP	None	REV_BBBUMP [12:11]		LSLDO [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15	FPD_REFORCE	1: Force Power down for refcore Default Value: 0
14	FORCE_BGSTARTUP	1: force BG start u\p Default Value: 0
12 : 11	REV_BBBUMP	reserved for feature Default Value: 0
10 : 8	LSLDO	3d0: LS LDO output is 1.708V 3d1: LS LDO output is 1.747V 3d2: LS LDO output is 1.802V 3d3: LS LDO output is 1.849V 3d4: LS LDO output is 1.904V 3d5: LS LDO output is 1.552V 3d6: LS LDO output is 1.591V 3d7: LS LDO output is 1.650V Default Value: 0

(continued)

7 : 5	LFLDO	3d0: XO LDO output is 1.894V; BB LDO output is 1.800V 3d1: XO LDO output is 1.946V; BB LDO output is 1.846V 3d2: XO LDO output is 2.000V; BB LDO output is 1.894V 3d3: XO LDO output is 2.000V; BB LDO output is 1.946V 3d4: XO LDO output is 1.701V; BB LDO output is 1.649V 3d5: XO LDO output is 1.756V; BB LDO output is 1.649V 3d6: XO LDO output is 1.800V; BB LDO output is 1.701V 3d7: XO LDO output is 1.846V; BB LDO output is 1.756V Default Value: 0
4 : 2	V2I_REG	Bit[4] 1: Error amp quiescent current is 5u 0: Error amp quiescent current is 10u Bit[3:2] 2d0: V2I LDO output is 1.8V 2d1: V2I LDO output is 1.85V 2d2: V2I LDO output is 1.9V 2d3: V2I LDO output is 1.75V Default Value: 0
1 : 0	REFCORE_VDD	2d0: Bumps the Ibias current of Refcore to 10u 2d1: Bumps the Ibias current of Refcore to 9.1u 2d2: Bumps the Ibias current of Refcore to 11.1u 2d3: Bumps the Ibias current of Refcore to 12.5u Default Value: 0

3.1.28 BLE_BLERD_BB_BUMP2

BB bump configuration

Address: 0x402E0074

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW			RW				
HW Access	R			R				
Name	V2I [7:5]			V2I_RCAL [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW			RW	
HW Access	R			R			R	
Name	SY_IBIAS [15:13]			VBG_TRIM [12:10]			V2I [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 13	SY_IBIAS	3'b1xx: RCAL current bumped 3'b0xx: BG current bumped. 2'bxx: reperesent current bump 01: +12.5%, 00: 0%, 11: -12.5%, 10:-25% Default Value: 0
12 : 10	VBG_TRIM	3d0: Trims the Bandgap voltage by 0% 3d1: Trims the Bandgap voltage by 1.6% 3d2: Trims the Bandgap voltage by 3.2% 3d3: Trims the Bandgap voltage by 4.8% 3d4: Trims the Bandgap voltage by 6.4% 3d5: Trims the Bandgap voltage by -4.8% 3d6: Trims the Bandgap voltage by -3.2% 3d7: Trims the Bandgap voltage by -1.6% Default Value: 0

(continued)

9 : 5	V2I	Bit[9] 1: Error amp quiescent current is 5u 0: Error amp quiescent current is 10u Bit[8:5] 4d0: Trims the BGR current by 0% 4d1: Trims the BGR current by -2.5% 4d2: Trims the BGR current by -5% 4d3: Trims the BGR current by -7.5% 4d4: Trims the BGR current by -10% 4d5: Trims the BGR current by -12.5% 4d6: Trims the BGR current by -15% 4d7: Trims the BGR current by -17.5% 4d8: Trims the BGR current by 20% 4d9: Trims the BGR current by 17.5% 4d10: Trims the BGR current by 15% 4d11: Trims the BGR current by 12.5% 4d12: Trims the BGR current by 10% 4d13: Trims the BGR current by 7.5% 4d14: Trims the BGR current by 5% 4d15: Trims the BGR current by 2.5% Default Value: 0
4 : 0	V2I_RCAL	Bit[4] 1: Error amp quiescent current is 5u 0: Error amp quiescent current is 10u Bit[3:0] 4d0: Trims the RCAL current by 0% 4d1: Trims the RCAL current by -2.5% 4d2: Trims the RCAL current by -5% 4d3: Trims the RCAL current by -7.5% 4d4: Trims the RCAL current by -10% Default Value: 0

3.1.29 BLE_BLERD_BB_XO

BB bump configuration 1

Address: 0x402E0078

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW		RW	RW	RW	RW	RW
HW Access	R	R		R	R	R	R	R
Name	CTRL_VDDL_XO	CTRL_RC_FASTSTART_RES [6:5]		EN_AMPDET_FASTSTART	EN_AMPDET_CURMEAS	EN_CURMEAS	EN_RE_FASTSTART	DIS_XOCORE_SUPFILT

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW		RW			RW	
HW Access	R	R		R			R	
Name	rev_bb_xo	CTRL_RPREF [14:13]		CTRL_VDDL_XB [12:10]			CTRL_VDDL_XO [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15	rev_bb_xo	reserved for feature Default Value: 0
14 : 13	CTRL_RPREF	Controls the reference voltage fed as input to the regulators which generate vdd_xo and vdd_xb. 2d0 : 1.289V 2d0 : 1.227V 2d0 : 1.164V 2d0 : 1.382V Default Value: 0

(continued)

12 : 10	CTRL_VDDL_XB	Controls the value of supply filter resistance in the inverter chain. This in turn controls the supply voltage at which the inverter chain runs. 3d0 : 1.028k 3d0 : 1.172k 3d0 : 1.367k 3d0 : 1.540k 3d0 : 1.889k 3d0 : 2.055k 3d0 : 0.503k 3d0 : 0.747k Default Value: 0
9 : 7	CTRL_VDDL_XO	Controls the value of supply filter resistance in the xo core. This in turn controls the supply voltage at which the core runs. 3d0 : 0.769k 3d0 : 0.877k 3d0 : 1.023k 3d0 : 1.152k 3d0 : 1.413k 3d0 : 1.537k 3d0 : 0.376k 3d0 : 0.559k Default Value: 0
6 : 5	CTRL_RC_FASTSTART_RES	Controls the time constant with which the surge current from rc_faststart block decays down to zero. 2d0 : 387us 2d1 : 309us 2d2 : 232us 2d3 : 464us Default Value: 0
4	EN_AMPDET_FASTSTART	This bit is used to force startup of the vtnbyr circuit in the biasgen_and_reg block of the XO. 1d1 : startup forced 1d0 : Normal startup Default Value: 0
3	EN_AMPDET_CURMEAS	This bit can be used to disable all the caps on both X1 node and X2 node. 1d0 : Caps Enabled 1d1 : Caps disabled. Even when all the caps are disabled, due to finite on/off ratio of the caps, the cap on both X1 and X2 node is still 3.69pF Default Value: 0
2	EN_CURMEAS	This bit is used to force startup of the positive feedback loop in the amplitude detect block of the XO. 1d1 : startup forced 1d0 : Normal startup Default Value: 0
1	EN_RE_FASTSTART	Enables/Disables the RC faststart block in the XO. When enabled, this block provides a surge current at xo startup to reduce the settling time of the XO. 1: RC Fast start in XO is enabled 0: RC Fast start in XO is disabled Default Value: 0
0	DIS_XOCORE_SUPFILT	Enables/Disables the supply filter of the XO core. 1: Disabled 0: Enabled Default Value: 0

3.1.30 BLE_BLERD_BB_XO_CAPTRIM

BB bump configuration 2

Address: 0x402E007C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	X2 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	X1 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 8	X1	Bits 15-8 together control cap on X1 node. Bits 14-8 : Fine Control Value of 14-8 : Cap Value 7d0 : 3.6900pF 7d1 : 3.7911pF 7d2 : 3.8922pF . . . 7d127 : 16.4280pF Bit 15 : Coarse control 1d0 : No additional cap turned on 1d1 : Additional cap of 8.1pF turned on Default Value: 45

(continued)

7 : 0	X2	Bits 7-0 together control cap on X2 node. Bits 6-0 : Fine Control Value of 6-0 : Cap Value 7d0 : 3.6900pF 7d1 : 3.7911pF 7d2 : 3.8922pF . . . 7d127 : 16.4280pF Bit 7 : Coarse control 1d0 : No additional cap turned on 1d1 : Additional cap of 8.1pF turned on Default Value: 106

3.1.31 BLE_BLERD_SY_BUMP1

SY bump bits configuration 1

Address: 0x402E0080

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW		RW	RW			
HW Access	R	R		R	R			
Name	LDOLO_FORCE_STARTUP	IBIAS_LOPATH [6:5]		LOFB_POWERSAVE	VCO [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	PDCPLPF [15:12]				LOPATH [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 12	PDCPLPF	Bump for PD CP and LPF blocks.[2:0] is used to get range of -20%to +15% in 5% steps. ICP_BUMP[2:0] ICP 1 0 0 -20% 1 0 1 -15% 1 1 0 -10% 1 1 1 -05% 0 0 0 00% 0 0 1 05% 0 1 0 10% 0 1 1 15%. Default Value: 0

(continued)

11 : 8	LOPATH	Bump bits for LO path bulk bias. Goes to DIVN/FCAL/LOPATH for bumps. 2 bits for pBulk [3:2] and 2 bits for nBulk[1:0]. bump pbulk 0 0 vddx-380mV 0 1 vddx-320mV 1 0 vddx-440mV 1 1 vddx Default Value: 5
7	LDOLO_FORCE_START UP	1: force start-up of the VT/R circuit in VCOLOPATH LCO 0: no force start-up Default Value: 0
6 : 5	IBIAS_LOPATH	bump bits for clkbias in lopath bump clk bias pM clk bias nM 0 0 vddo-vgsp vgsn 0 1 vddlo-vgsp-100m vgsn+100m 1 0 vddlo-vgsp-200m vgsn+200m 1 1 vddlo-vgsp-400m vgsn+400m Default Value: 0
4	LOFB_POWERSAVE	1: enable powersave for LOFB buffer 0: disable powersave for LOFB buffer Default Value: 0
3 : 0	VCO	Bump bits for SY VCO block. Rt VCO (2 bits) - sy_bump1_vco [3:2] 00 ~ 50 Ohms 01 ~ 30 Ohms 10 ~ 22 Ohms 11 ~ 16 Ohms and Rb VCO (2 bits) - sy_bump1_vco[1:0] 00 ~ 58 Ohms 01 ~ 39 Ohms 10 ~ 22 Ohms 11 ~ 16 Ohms Default Value: 5

3.1.32 BLE_BLERD_SY_BUMP2

SY bump bits configuration 2

Address: 0x402E0084

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	ICP_OFFSET [7:6]		ICP_XFACTOR [5:4]		ACAP_BIAS_SEL [3:2]		FCAL_BIAS_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW		RW	RW	RW	RW
HW Access	R		R		R	R	R	R
Name	PDCP_OFFSET [15:14]		RST_DLY [13:12]		VMOD_PULLDN	VCTRL_PULLDN	PUP_MON	CLKNC_MODE

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 14	PDCP_OFFSET	Bump for the bias voltage of the 8x node. sel[1:0] R2 Vbp 00 38.5k 925mV (Default) 01 43.0k 925mV+108mV 10 31.9k 925mV-158mV 11 35.2k 925mV-080mV Default Value: 0
13 : 12	RST_DLY	Bumping the reset (up+down) delay. Code[1:0] delay 00 500ps 01 424ps 10 350ps 11 300ps Default Value: 0
11	VMOD_PULLDN	1: Pull down control for the modulating port Default Value: 0
10	VCTRL_PULLDN	1: Test mode to pull down for noise simulation Default Value: 0

(continued)

9	PUP_MON	1:Test mode to monitor buffered 1x output on the injmon buffer Default Value: 0
8	CLKNC_MODE	Control the NC_clock_mux. 0: The NC clock is given from DIVN once openloop is made low. 1: The NC clock is always connected to Crystal clock Default Value: 0
7 : 6	ICP_OFFSET	Bump bits to set the offset pulse width in RX mode Code[1:0] delay 00 2.45n 01 1.75ns 10 1.3ns 11 25ps Default Value: 0
5 : 4	ICP_XFACTOR	sy_bump2_icp_xfactor[1]: enable power save for SY FB buffers in TXPOWERSAVE mode, high active sy_bump2_icp_xfactor[0]: HSDIV2 is put in self oscillation mode, this can be used to find out the process corner of the chip, high active Default Value: 0
3 : 2	ACAP_BIAS_SEL	ACAP bias voltage is selected based on these bits. Code[1:0] acapbias 00 630mV 01 700mV 10 560mV 11 595mV Default Value: 0
1 : 0	FCAL_BIAS_SEL	VCTRL bias voltage is selected based on these bits. Code[1:0] fcal_bias 00 Vddvco/2 01 Vddvco/2 + 5.6%(+100mV) 10 Vddvco/2 - 2.8%(-050mV) 11 Vddvco/2 - 5.6%(-100mV) Default Value: 0

3.1.33 BLE_BLERD_TX_BUMP1

transmit bump configuration 1

Address: 0x402E0088

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW			
HW Access	R		R		R			
Name	TX_LPF [7:6]		SY_RST_DLY_TX [5:4]		TX_DRIVER [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW				RW	
HW Access	R		R				R	
Name	SY_DIVN_TXPOWERSAVE [15:14]		TX_VTXREF_PROG [13:10]				TX_LPF [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 14	SY_DIVN_TXPOWERSAVE	Divn power save bits pup freeze txpowersave<1:0> PupBlocks 0 0 X X NONE 1 0 X X ALL 1 1 0 0 ALL 1 1 0 1 ALL-D2 1 1 1 0 ALL-D2-D1 1 1 1 1 ALL-D2-D1-Buf Default Value: 3

(continued)

13 : 10	TX_VTXREF_PROG	TX Modulation port varactor vtxref bias voltage bump settings 0000 Sets vtxref value to 100mV 0001 Sets vtxref value to 150mV 0010 Sets vtxref value to 200mV 0011 Sets vtxref value to 250mV 0100 Sets vtxref value to 300mV 0101 Sets vtxref value to 350mV 0110 Sets vtxref value to 400mV 0111 Sets vtxref value to 450mV 1000 Sets vtxref value to 500mV 1001 Sets vtxref value to 550mV 1010 Sets vtxref value to 600mV Default Value: 4
9 : 6	TX_LPF	Bump bits for TX LPF op-amp reference voltage [3:2] 00 Bumps the opamp ref voltage to 400mV 01 Bumps the opamp ref voltage to 450mV 10 Bumps the opamp ref voltage to 300mV 11 Bumps the opamp ref voltage to 350mVBump bits for TX LPF op-amp bias current [1:0] 00 Bumps the opamp bias current to 10u 01 Bumps the opamp bias current to 12.5u 10 Bumps the opamp bias current to 8.3u 11 Bumps the opamp bias current to 7.7u Default Value: 0
5 : 4	SY_RST_DLY_TX	Bumping the reset (up+down) delay. Code[1:0] delay 00 500ps 01 424ps 10 350ps 11 300ps Default Value: 3
3 : 0	TX_DRIVER	Driver bias current selection bump bit tx_bump1_tx_driver[3] Driver bias current tx_bump1_tx_driver[0] PTAT current selection Additional Class AB driver bias voltage bump related to Tx_bump2_drv_ab_vbias[3:0] Default Value: 0

3.1.34 BLE_BLERD_TX_BUMP2

transmit bump configuration 2

Address: 0x402E008C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW			
HW Access	R		R		R			
Name	SY_LDOBGREF_EN [7:6]		DRV_VCASCH [5:4]		DRV_AB_VBIAS [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW				RW	
HW Access	R		R				R	
Name	SY_CP_TXPOWERSAVE [15:14]		DAC_RES [13:10]				SY_ICP_OFFSET_TX [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 14	SY_CP_TXPOWERSAVE	Charge pump power save bits pup freeze txpowersave<1:0> PupBlocks 0 0 X X NONE 1 0 X X ALL 1 1 0 0 ALL 1 1 0 1 ALL-8x CP 1 1 1 0 ALL-8x-1x CP 1 1 1 1 ALL-buffer Default Value: 3

(continued)

13 : 10	DAC_RES	TX DAC load resistor bump settings 0000 DAC output resistor bump by -20% 0001 DAC output resistor bump by -17.5% 0010 DAC output resistor bump by -15% 0011 DAC output resistor bump by -12.5% 0100 DAC output resistor bump by -10% 0101 DAC output resistor bump by -7.5% 0110 DAC output resistor bump by -5% 0111 DAC output resistor bump by -2.5% 1000 DAC output resistor bump by 0% 1001 DAC output resistor bump by 2.5% 1010 DAC output resistor bump by 5% 1011 DAC output resistor bump by 7.5% 1100 DAC output resistor bump by 10% 1101 DAC output resistor bump by 12.5% 1110 DAC output resistor bump by 15% 1111 DAC output resistor bump by 17.5% Default Value: 8
9 : 8	SY_ICP_OFFSET_TX	Bump bits to set the offset pulse width in TX mode Code[1:0] xfactor 00 : 2.45ns 01 : 1.75ns 10 : 1.3ns 11 : 25ps Default Value: 3
7 : 6	SY_LDOBGREF_EN	Enables a bandgap (low temp coeff) for the 00 None 01 VCO ldo 10 LOPATH ldo 11 VCO+LOPATH ldo Default Value: 0
5 : 4	DRV_VCASCH	Programs the driver cascode gate bias voltage Tx_bump2_drv_vcasch[1:0] Driver cascode bias voltage 00 Vdd_driver 0.3V 01 Vdd_driver 0.2V 10 Vdd_driver 0.1V 11 Vdd_driver Default Value: 3

(continued)

3 : 0	DRV_AB_VBIAS	Bias voltage for the class-AB driver with tx_bump1_tx_driver[1:0]=00 Tx_bump2_drv_ab_vbias[3:0] Vbias_AB , mV 0000 571.224 0001 604.508 0010 626.357 0011 641.856 0100 656.04 0101 667.096 0110 678.775 0111 688.005 1000 698.817 1001 707.272 1010 718.103 1011 726.411 1100 737.995 1101 746.708 1110 759.919 1111 769.735 Default Value: 8

3.1.35 BLE_BLERD_RX_BUMP1

receiver bump configuration 1

Address: 0x402E0090

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW			RW		
HW Access	R		R			R		
Name	IF_OFFSET_CALDAC [7:6]		CBPF [5:3]			TIA [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW		RW	
HW Access	R				R		R	
Name	LNA [15:12]				MIXER [11:10]		MIXER_VBIAS_SW [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 12	LNA	rx_bump1_lna[3] 1: enables the HG and LG LNA section's cascode biases to be alive independent of whether LNA is HG or LG mode. This enables fast transition from LG to HG in AGC events rx_bump1_lna[2] 1: forces pull donwn of inputs of LNA (post AC coupling) if LNA is powered up in Hi-Z mode to ensure good isolation during DC offset calibration of Receiver chain rx_bump1_lna[1] 1: Boost the LNA bias current ot HP equivalent (1.5mA current penalty) if LNA gain is at 101 (66dB setting) and this bit is set. this boosts sensitivity by 2-3dB but the hit in the current consumption is only at 66dB gain setting. so average current comsumption in field should not be impacted much but a 2dB boost in sensitivity is seen rx_bump1_lna[0] 1: Forces the TIA to have lower feedback resistor to aviode EVM degratation in the TIA dut to complex filter distortion caused by I/Q cross talk if feedback resistors is high in the TIA Default Value: 12

(continued)

11 : 10	MIXER	bump bits to control LNA gate bias voltage in RX mode 01 0.5V 00 0.4V 11 0.3V 10 0.2V Default Value: 2
9 : 8	MIXER_VBIAS_SW	Bump bits for Mixer VBIAS switch Mixer Bias Programmability 01 TIA CM + 0.38V 00 TIA CM + 0.3V 11 TIA CM + 0.255V 10 TIA CM + 0.17V Default Value: 2
7 : 6	IF_OFFSET_CALDAC	Bit Setting Offset DAC LSB 00 132.4nA 01 150.8nA 10 118.0nA 11 106.5nA Default Value: 0
5 : 3	CBPF	2'b0xx: CBPF CM ref voltage 850mV and 1V for 1st stage and 2nd stage resp. for irefbg 8.5uA. 2'b1xx: CBPF CM ref voltage 850mV and 1V for 1st stage and 2nd stage resp. for irefbg 10uA. 2'bxx0: CBPF OTA1 CMFB tail current 17.27uA (Bias current 8.5uA). 2'bxx1: CBPF OTA1 CMFB tail current 21.58uA (Bias current 8.5uA). 2'bx0x: CBPF OTA2 CMFB tail current 17.27uA (Bias current 8.5uA). 2'bx1x: CBPF OTA2 CMFB tail current 21.58uA (Bias current 8.5uA). Default Value: 0
2 : 0	TIA	2'b0xx: TIA CM ref voltage 850mV for iref bias current 8.5uA. 2'b1xx: TIA CM ref voltage 850mV for iref bias current 10uA. 2'bx00: TIA OTA CMFB tail current 69uA (Bias current 8.5uA). 2'bx01: TIA OTA CMFB tail current 78uA (Bias current 8.5uA). 2'bx10: TIA OTA CMFB tail current 86uA (Bias current 8.5uA). 2'bx11: TIA OTA CMFB tail current 95uA (Bias current 8.5uA). Default Value: 0

3.1.36 BLE_BLERD_RX_BUMP2

receiver bump configuration 2

Address: 0x402E0094

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	IF_CM_IBIAS [7:6]		CBPF_IBIAS [5:4]		TIA_IBIAS [3:2]		LNA_IBIAS [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW	RW	RW	RW	RW	RW
HW Access	R		R	R	R	R	R	R
Name	REV_RX_BUMP2 [15:14]		SY_LOWKVMMODE	SY_LOWKVAMODE	SY_HILINEARITYR2_MODE	SY_R2HIGHMODE	COMPLEX_DISABLE	CBPF_HIZ_ENABLE

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 14	REV_RX_BUMP2	reserved for feature Default Value: 0
13	SY_LOWKVMMODE	Enables a lower Kv/2 mode 0 10 MHz/V 1 5 MHz/V Default Value: 0
12	SY_LOWKVAMODE	Enables a lower Kv/2 mode 0 70 MHz/V 1 45 MHz/V Default Value: 0
11	SY_HILINEARITYR2_MODE	Switches the RX mode between settings used in TX vs a higher linearity setting. 0 Use same as TX 1 Use alternative bias for RX. Effective only in RX mode. This is don't care in TX mode Default Value: 1

(continued)

10	SY_R2HIGHMODE	Enables a higher R2 mode for loop stabilization with low Kv and debug mode. 0 40 kohms 1 60 kohms Default Value: 0
9	COMPLEX_DISABLE	setting this bit to disables the complex operation for the band pass filter configuring it as two low pass filters Default Value: 0
8	CBPF_HIZ_ENABLE	Setting this bit to 1 configures the CBPF output as hi-Z enabling independent ADC testing with the injection system Default Value: 0
7 : 6	IF_CM_IBIAS	Bump bits for Common mode setting currents of the TIA and the CBPF amplifiers (Default is 11 for current saving). 01 IBias+15% 00 IBias+0% 11 IBias-15% (Default) 10 IBias-20% Default Value: 3
5 : 4	CBPF_IBIAS	Bump bits for BGR bias currents of Offset Calibration DAC (Default is 00) 01 IBias+15% 00 IBias_0% (Default) 11 IBias-15% 10 IBias-20% Default Value: 0
3 : 2	TIA_IBIAS	Bump bits for RCAL bias currents of the TIA and the CBPF amplifiers (Default is 11 for current saving). 01 IBias+15% 00 IBias+0% 11 IBias-15% (Default) 10 IBias-20% Default Value: 3
1 : 0	LNA_IBIAS	Bump bits for PTAT bias currents of LNA (Default is 00). Play with these to enable Low Power and Ultra Low Power modes in the LNA. 01 IBias+15% 00 IBias+0% (Default) 11 IBias-25% 10 IBias-50% Default Value: 2

3.1.37 BLE_BLERD_ADC_BUMP1

ADC1 bump configuration

Address: 0x402E0098

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW			RW		
HW Access	R		R			R		
Name	IBG_CAL [7:6]		Q_REF [5:3]			I_REF [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW	RW	RW	RW		RW
HW Access	R		R	R	R	R		R
Name	BWCTRL [15:14]		OPAMP_BYPASS	LOWPOW-ER	LOOPDLY4X_EN	LOOPDLY [10:9]		IBG_CAL

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 14	BWCTRL	Reference generators bandwidth boost by injecting current in the output arm. Injection Current : 00 0 A 01 20 A 10 40 A 11 60 A Default Value: 0
13	OPAMP_BYPASS	Bypass op-amp and diode connect reference generator's servo loop 0 Op-amp enabled 1 Op-amp bypassed Default Value: 0
12	LOWPOWER	rCurrent reduction mode in the reference generator. 0 No bump 1 50% bump Default Value: 0

(continued)

11	LOOPDLY4X_EN	Loop delay increment by 4x in SAR return path 0 Delay determined by loopdly[1:0] 1 4x the delay dictated by the said bit Default Value: 0
10 : 9	LOOPDLY	Loop delay control in SAR return path. 00 Min delay 11 Max delay Default Value: 0
8 : 6	IBG_CAL	Bump bits for the preamps bias current. X00 + 0 % (Ibias - 0 A) X01 +25 % (Ibias - 12.5 A) X10 - 50 % (Ibias - 5 A) X11 - 25 % (Ibias - 7.5 A) Default Value: 0
5 : 3	Q_REF	Bump bits for the channel-Q reference voltage. (2s complement interpretation) Every bit changes the reference voltage by 10mV. 100 610 mV 000 650 mV 011 680 mV Default Value: 4
2 : 0	I_REF	Bump bits for the channel-I reference voltage. (2s complement interpretation) Every bit changes the reference voltage by 10mV. See the above table Default Value: 4

3.1.38 BLE_BLERD_ADC_BUMP2

ADC 2 bump configuration

Address: 0x402E009C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	SHORT_INPUT	PREAMP_GAINCTRL_N	PREAMP_SOURCECTRL_N	IBUMP	METADET_EN	DUTCYCLE_25	CYCLE_B5_DELAY	CYCLE_B2_DELAY

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW		RW	RW		
HW Access	R		R		R	R		
Name	REV_ADC_BUMP2 [15:14]		PREAMP_BWCTRL [13:12]		IQSWAP	RETURN_SKEW [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 14	REV_ADC_BUMP2	[1] -- not used [0] Enable clean Vdd for the cascodes & op-amp in refgen. The clean Vdd supplied through the diag. (Diag code = 0101 for channel I and Diag code =1101 for channel Q). Default connection to the internal Vdd Default Value: 0
13 : 12	PREAMP_BWCTRL	Bandwidth bump bits for the preamp. Each bit connects a 5fF cap to the output nodes. No cap is connected by default Default Value: 0
11	IQSWAP	Swaps the I and Q channel Vbg/R for ref.gen 0 No swap 1 Enable swapping Default Value: 0
10 : 8	RETURN_SKEW	Delaying the sampling clock from the comparator wrt to the data. 000 Min delay 111 Max delay Default Value: 0

(continued)

7	SHORT_INPUT	Put the ADC in idle channel mode. Inputs are shorted to locally generated 1V signal. 0 Normal operation 1 Idle channel mode Default Value: 0
6	PREAMP_GAINCTRL_N	Enable preamps low/high gain modes over conversion cycle. 0 Functionality enabled 1 Functionality disabled Default Value: 0
5	PREAMP_SOURCECTRL_N	Disconnect source coupled node of the preamp during track phase. 0 Functionality enabled 1 Functionality disabled Default Value: 0
4	IBUMP	0: 6dB attenuation in CBPF gain only at lowest gain setting to improve the Max signal level the receiver can tolarate Note: in order to chare the tub width with AGC disabled, this back off mode is effective only with AGC profile set to rev** mode. This is in reg0xa4[3] which needs to be set to '0' for rev** profile Default Value: 0
3	METADET_EN	Enable meta detection Default Value: 0
2	DUTCYCLE_25	Clock duty cycle control 0 50 % time for track phase & 50 % time for convert phase 1 25 % time for track phase & 75 % time for convert phase Default Value: 1
1	CYCLE_B5_DELAY	Enable redundant conversion cycle at b5 position. 0 Disabled 1 Enabled Default Value: 0
0	CYCLE_B2_DELAY	Enable redundant conversion cycle at b2 position. 0 Enabled 1 Disabled Default Value: 0

3.1.39 BLE_BLERD_BALUN

BALUN bump configuration

Address: 0x402E00A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	BUMP_TX_CTUNE [7:4]				BUMP_RX_CTUNE [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW		RW		
HW Access	R			R		R		
Name	REV_BALUN [15:13]			BUMP_RTUNE [12:11]		BUMP_VTUNE [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 13	REV_BALUN	resereved for feature Default Value: 0
12 : 11	BUMP_RTUNE	resereved for feature Default Value: 0
10 : 8	BUMP_VTUNE	resereved for feature Default Value: 0

(continued)

7 : 4	BUMP_TX_CTUNE	Programmable bits to change tuning capacitance in the Balun primary side in TX operation Balun_bump_tx_ctune[3:0] Ctune, fF 0000 42.5 0001 48.8 0010 55.1 0011 61.4 0100 67.7 0101 74 0110 80.3 0111 86.6 1000 92.9 1001 99.2 1010 105.5 1011 111.8 1100 118.1 1101 124.4 1110 130.7 1111 137 Default Value: 0
3 : 0	BUMP_RX_CTUNE	Programmable bits to change tuning capacitance in the Balun primary side in RX operation Balun_bump_tx_ctune[3:0] Ctune, fF 0000 42.5 0001 48.8 0010 55.1 0011 61.4 0100 67.7 0101 74 0110 80.3 0111 86.6 1000 92.9 1001 99.2 1010 105.5 1011 111.8 1100 118.1 1101 124.4 1110 130.7 1111 137 Default Value: 3

3.1.40 BLE_BLERD_CTR1

RFCTRL control timing 1

Address: 0x402E00A4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW	RW		RW		RW
HW Access	R		R	R		R		R
Name	TX_MODSTART_TIME [7:6]		TX_PREDRV_TIME	TX_FREEZE_TIME [4:3]		PLL_SETTLING_TIME [2:1]		VCO_WARMUP_TIME

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW	RW	RW		RW	RW
HW Access	R		R	R	R		R	R
Name	AGC_RST_DLY [15:14]		RX_ENV_FREEZE_EN	RX_DC_FREEZE_EN	DBG_SELECT [11:10]		ADC_FULL_SWING_MONI_EN	TX_DF2_SEL

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 14	AGC_RST_DLY	00: 0.25us delay; 01: 1.25us delay, 10: 2.25us delay, 11: 3.25us delay Default Value: 0
13	RX_ENV_FREEZE_EN	demodulation soft reset to frequency tracking enabled, high active Default Value: 1
12	RX_DC_FREEZE_EN	demodulation soft reset to DC cancellation enabled, high active Default Value: 1
11 : 10	DBG_SELECT	00: demod soft reset / AGC reset, 01: AGC FSM MSB and f_n_rxen 10: gain decrease and gain increase. 11: ADC full swing detection and ADC saturation detected signal Default Value: 0
9	ADC_FULL_SWING_MONI_EN	when ctr1_adc_full_swing_moni_en is set and ctr1_dbg_select is 2'b11. ADC full swing detection can be monitored in debug pin Default Value: 0

(continued)

8	TX_DF2_SEL	0: DF2 Max frequency deviation as 224KHz 1: DF2 Max frequency deviation as 242KHz Default Value: 1
7 : 6	TX_MODSTART_TIME	this controls the time between the PUP_TX_DRIVER going high and when f_n_txen is asserted. 00: 0us, 01: 1us, 10: 2us, 11, 3us Default Value: 3
5	TX_PREDRV_TIME	PA predrive pup time, 1:powered up after LDO, 0: powered up after KVCAL Default Value: 0
4 : 3	TX_FREEZE_TIME	tx freeze time 00: 30us, 01: 40us, 10: 50us, 11: 25us Default Value: 0
2 : 1	PLL_SETTLING_TIME	PLL setting time 00: 25us, 01: 30us, 10: 40us, 11:50us Default Value: 0
0	VCO_WARMUP_TIME	vco warm up time, 1: 10us, 0: 5us Default Value: 0

3.1.41 BLE_BLERD_AGC

AGC timing conifguration

Address: 0x402E00A8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW	RW	RW	RW
HW Access	R		R		R	R	R	R
Name	PWR_MEAS_TIM [7:6]		GAIN_SAT_THRES [5:4]		GAIN_MAPPING_MODE	SAT_CHK_TIM	CHECK_SAT_EN	RST_EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW				
HW Access	R			R				
Name	START_WAIT_TIM [15:13]			GAIN_STABLE_TIM [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 13	START_WAIT_TIM	start AGC waiting time when RFCTRL set AGC enable 1 represents 1us, base 1us Default Value: 1
12 : 8	GAIN_STABLE_TIM	gain stable time after gain assignment. 1 represents one 12Mhz clock Default Value: 5
7 : 6	PWR_MEAS_TIM	AGC power measurement time 11: 1us, 10: 0.75us, 01: 0.5us, 00:0.25us Default Value: 3
5 : 4	GAIN_SAT_THRES	ADC saturated detection threshold for doing a fast transition 00: 0dBm; 01: 1dBm; 10: 2dBm, 11: 3dBm Default Value: 3
3	GAIN_MAPPING_MODE	0: Atlantis TC rev** gaim mapping 1: Atlantis TC revA gain mapping Default Value: 1

(continued)

2	SAT_CHK_TIM	ADC saturated detection timing 0: 3 12MHz clock;1:3 12MHz clock; Default Value: 1
1	CHECK_SAT_EN	1: quick check saturated ADC 0: mearue ADC power at fixed period Default Value: 1
0	RST_EN	1: AGC soft reset enable Default Value: 1

3.1.42 BLE_BLERD_THRSHD1

AGC step threshold 1

Address: 0x402E00AC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		AGC60_66 [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW					
HW Access	None		R					
Name	None [15:14]		AGC66_60 [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
13 : 8	AGC66_60	threshold gain changge from 60dB to 48dB Default Value: 60
5 : 0	AGC60_66	threshold gain changge from 66dB to60dB Default Value: 44

3.1.43 BLE_BLERD_THRSHD2

AGC step threshold 2

Address: 0x402E00B0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		AGC48_60 [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW					
HW Access	None		R					
Name	None [15:14]		AGC60_48 [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
13 : 8	AGC60_48	threshold gain changge from 48dB to 60dB Default Value: 59
5 : 0	AGC48_60	threshold gain changge from 60dB to48dB Default Value: 42

3.1.44 BLE_BLERD_THRSHD3

AGC step threshold 3

Address: 0x402E00B4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		AGC36_48 [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW					
HW Access	None		R					
Name	None [15:14]		AGC48_36 [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
13 : 8	AGC48_36	threshold gain changge from 366dB to 48dB Default Value: 59
5 : 0	AGC36_48	threshold gain changge from 48dB to 36dB Default Value: 44

3.1.45 BLE_BLERD_THRSHD4

AGC step threshold 4

Address: 0x402E00B8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		AGC18_36 [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW					
HW Access	None		R					
Name	None [15:14]		AGC36_18 [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
13 : 8	AGC36_18	threshold gain changge from 18dB to 36dB Default Value: 60
5 : 0	AGC18_36	threshold gain changge from 36dB to 18dB Default Value: 43

3.1.46 BLE_BLERD_THRSHD5

AGC step threshold 5

Address: 0x402E00BC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		AGC0_18 [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW					
HW Access	None		R					
Name	None [15:14]		AGC18_0 [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
13 : 8	AGC18_0	threshold for gain change from 0dB to 18dB Default Value: 62
5 : 0	AGC0_18	threshold for gain change from 18dB to 0dB Default Value: 38

3.1.47 BLE_BLERD_DC

ADC I/Q DC compensate value

Address: 0x402E00C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	COMP_Q_CODE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	COMP_I_CODE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 8	COMP_I_CODE	this code is removed from the ADC Q output. This field can be progamrmed to remove systematci DC offset Default Value: 0
7 : 0	COMP_Q_CODE	this code is removed from the ADC I output. This field can be progamrmed to remove systematci DC offset Default Value: 0

3.1.48 BLE_BLERD_IQMIS

IQ mismatch correction value

Address: 0x402E00C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	IQCOMP_QVAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	IQCOMP_IVAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 8	IQCOMP_IVAL	Q-component of the IQ mismatch correction Default Value: 0
7 : 0	IQCOMP_QVAL	I-component of the IQ mismatch correction Default Value: 0

3.1.49 BLE_BLERD_DCCAL

DC CAL and setting

Address: 0x402E00C8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW					
HW Access	R		R					
Name	TEST_QBITS [7:6]		TEST_IBITS [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW	RW	RW	RW			
HW Access	None	R	R	R	R			
Name	None	TEST_I_POLARITY	TEST_Q_POLARITY	TEST_MODE	TEST_QBITS [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
14	TEST_I_POLARITY	1: inverts the polarity of DCCAL I code Default Value: 0
13	TEST_Q_POLARITY	1: inverts the polarity of DCCAL Q code Default Value: 0
12	TEST_MODE	enable the DCCAL test mode Default Value: 0
11 : 6	TEST_QBITS	this value is driven to DCCAL Qcode if the DCCA: test mode enabled Default Value: 0
5 : 0	TEST_IBITS	this value is driven to DCCAL Icode if the DCCA: test mode enabled Default Value: 0

3.1.50 BLE_BLERD_RCCAL

TX LPF and TIA/CBPF RC code

Address: 0x402E00CC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW			RW				
HW Access	R			R				
Name	CODE_TX [7:5]			CODE_RX [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW	RW	RW	None	RW	
HW Access	R		R	R	R	None	R	
Name	AGC_GAIN_INC_TIMES_THRES [15:14]		SOFTRST_EN_TODIFF	SOFTRST_EN_TOSTR	SOFTRST_POWER_DIFF	None	CODE_TX [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 14	AGC_GAIN_INC_TIMES_THRES	AGC gain increase requirement wait times: 00: respose for 1st gain increase request 01: respone for 2nd gain increase request 10: respons for 3rd gain increase request 11: respons for 4th gain increase request Default Value: 0
13	SOFTRST_EN_TODIFF	soft reset is enable to diffdet block Default Value: 0
12	SOFTRST_EN_TOSTR	soft reset is enabled to STR block Default Value: 1
11	SOFTRST_POWER_DIFF	soft reset power change detection, 1: 12dB, 0:6dB Default Value: 1
9 : 5	CODE_TX	force RC code for TX LPF under test mode Default Value: 16

(continued)

4 : 0	CODE_RX	force RC code for TIA/CBPF under test mode Default Value: 16

3.1.51 BLE_BLERD_DSM1

DSM freeze code 1

Address: 0x402E00D0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	INDX_CODE2 [7:4]				INDX_CODE3 [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	INDX_CODE0 [15:12]				INDX_CODE1 [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 12	INDX_CODE0	index at which DSM code should be freezed when fection value = 0 Default Value: 13
11 : 8	INDX_CODE1	index at which DSM code should be freezed when fection value = 1/24 Default Value: 9
7 : 4	INDX_CODE2	index at which DSM code should be freezed when fection value = 2/24 Default Value: 6
3 : 0	INDX_CODE3	index at which DSM code should be freezed when fection value = 3/24 Default Value: 4

3.1.52 BLE_BLERD_DSM2

DSM freeze code 2

Address: 0x402E00D4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	INDX_CODE6 [7:4]				INDX_CODE7 [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	INDX_CODE4 [15:12]				INDX_CODE5 [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 12	INDX_CODE4	index at which DSM code should be freezed when fection value = 4/24 Default Value: 5
11 : 8	INDX_CODE5	index at which DSM code should be freezed when fection value = 5/24 Default Value: 4
7 : 4	INDX_CODE6	index at which DSM code should be freezed when fection value = 6/24 Default Value: 12
3 : 0	INDX_CODE7	index at which DSM code should be freezed when fection value = 7/24 Default Value: 1

3.1.53 BLE_BLERD_DSM3

DSM freeze code 3

Address: 0x402E00D8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	INDX_CODE10 [7:4]				INDX_CODE11 [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	INDX_CODE8 [15:12]				INDX_CODE9 [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 12	INDX_CODE8	index at which DSM code should be freezed when fection value = 8/24 Default Value: 10
11 : 8	INDX_CODE9	index at which DSM code should be freezed when fection value = 9/24 Default Value: 10
7 : 4	INDX_CODE10	index at which DSM code should be freezed when fection value = 10/24 Default Value: 10
3 : 0	INDX_CODE11	index at which DSM code should be freezed when fection value = 11/24 Default Value: 5

3.1.54 BLE_BLERD_DSM4

DSM freeze code 4

Address: 0x402E00DC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	INDX_CODE14 [7:4]				INDX_CODE15 [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	INDX_CODE12 [15:12]				INDX_CODE13 [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 12	INDX_CODE12	index at which DSM code should be freezed when fection value = 12/24 Default Value: 8
11 : 8	INDX_CODE13	index at which DSM code should be freezed when fection value = 13/24 Default Value: 9
7 : 4	INDX_CODE14	index at which DSM code should be freezed when fection value = 14/24 Default Value: 1
3 : 0	INDX_CODE15	index at which DSM code should be freezed when fection value = 15/24 Default Value: 1

3.1.55 BLE_BLERD_DSM5

DSM freeze code 5

Address: 0x402E00E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	INDX_CODE18 [7:4]				INDX_CODE19 [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	INDX_CODE16 [15:12]				INDX_CODE17 [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 12	INDX_CODE16	index at which DSM code should be freezed when fection value = 16/24 Default Value: 9
11 : 8	INDX_CODE17	index at which DSM code should be freezed when fection value = 17/24 Default Value: 13
7 : 4	INDX_CODE18	index at which DSM code should be freezed when fection value = 18/24 Default Value: 3
3 : 0	INDX_CODE19	index at which DSM code should be freezed when fection value = 19/24 Default Value: 7

3.1.56 BLE_BLERD_DSM6

DSM freeze code 6

Address: 0x402E00E4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	INDX_CODE22 [7:4]				INDX_CODE23 [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	INDX_CODE20 [15:12]				INDX_CODE21 [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 12	INDX_CODE20	index at which DSM code should be freezed when fection value = 20/24 Default Value: 7
11 : 8	INDX_CODE21	index at which DSM code should be freezed when fection value = 21/24 Default Value: 8
7 : 4	INDX_CODE22	index at which DSM code should be freezed when fection value = 22/24 Default Value: 8
3 : 0	INDX_CODE23	index at which DSM code should be freezed when fection value = 23/24 Default Value: 12

3.1.57 BLE_BLERD_MONI

agc gain and pup signal monitor

Address: 0x402E00E8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	PUP_SIG [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R			R		R		
HW Access	W			W		W		
Name	LNA_CODE [15:13]			CBPF_CODE [12:11]		PUP_SIG [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 13	LNA_CODE	lna gain code read back Default Value: 5
12 : 11	CBPF_CODE	cbpf gain code read back Default Value: 3
10 : 0	PUP_SIG	block pup up signals monitor. 10: iso_eanble 9: balum LDO power up, high active 8: SY bias power up, high active 7. SY VCO pup up, high active 6: TX bias pup up, high active 5. TX DAC pup up, high active 4: TX LPF pup up, high active 3. TX driver pup up, high active 2: RX LNA pup up, high active 1. RX CBPF pup up, high active 0: RX ADC ICORE pup, high active Default Value: 1024

3.1.58 BLE_BLERD_DBG_BB

RX offcal and RC cal code

Address: 0x402E00EC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	RX_OFFSET_Q_CODE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	RX_OFFSET_I_CODE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 8	RX_OFFSET_I_CODE	when modem_read_dc_offset_sel = 1, RX DCCAL I path can be read through this field. When modem_read_dc_offset_sel = 0, RC DC offset capture I code can be read through this field rx offsetcal Q code can be read through this field if modem_read_dc_offset_sel = 0 Default Value: 0
7 : 0	RX_OFFSET_Q_CODE	when modem_read_dc_offset_sel = 1, RX DCCAL Q path can be read through this field. When modem_read_dc_offset_sel = 0, RC DC offset capture Q code can be read through this field rx offsetcal Q code can be read through this field if modem_read_dc_offset_sel = 0 Default Value: 0

3.1.59 BLE_BLERD_DBG_1

FCAL coarse / fine code is reflected in this field

Address: 0x402E00F0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	W				W			
Name	FCAL_COARSE_CODE [7:4]				FCAL_FINE_CODE [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None	R	R	R	R			
HW Access	None	W	W	W	W			
Name	None	DCCAL_DONE	KVCAL_DONE	FCAL_DONE	FCAL_COARSE_CODE [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
14	DCCAL_DONE	1: indicates RX DC calibration is done for current packet Default Value: 0
13	KVCAL_DONE	1: indicates TX KV calibration is done for current packet Default Value: 0
12	FCAL_DONE	1: indicates when frequency calibration is done Default Value: 0
11 : 4	FCAL_COARSE_CODE	The FCAL coars code is reflected in this field Default Value: 128
3 : 0	FCAL_FINE_CODE	The FCAL fine code is reflected in this field Default Value: 8

3.1.60 BLE_BLERD_DBG_2

FCAL countere value ate the end of 7th bit (MSB)

Address: 0x402E00F4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	FCAL_CNT_LSB [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	FCAL_CNT_LSB [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	FCAL_CNT_LSB	the dbg_fcal_cnt_sel value, the 16 LSB bits of the corresponding debug counter is pouplated in this register [6:0] is kvcal_gain when select kvcal_gain Default Value: 0

3.1.61 BLE_BLERD_DBG_3

VCO OL count read out (MSB)

Address: 0x402E00F8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R			
HW Access	None				W			
Name	None [7:4]				FCAL_CNT_MSB [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	R	R					None	
HW Access	W	W					None	
Name	RD_RCCAL_DONE	RD_RCCAL_CODE [14:10]					None [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15	RD_RCCAL_DONE	RCCAL done indictor Default Value: 0
14 : 10	RD_RCCAL_CODE	RCCAL code read out through register Default Value: 0
3 : 0	FCAL_CNT_MSB	the dbg_fcal_cnt_sel value, the 4 MSB bits of the corresponding debug counter is pouplated in this register Default Value: 0

3.1.62 BLE_BLERD_READ_IQ_1

I Path ADC Data

Address: 0x402E0100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	ADC_1 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	ADC_1 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	ADC_1 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	ADC_1 [31:24]							

Bits	Name	Description
31 : 0	ADC_1	read out I path ADC data, first 16bits of I and Qcombination of 63bits Default Value: 0

3.1.63 BLE_BLERD_READ_IQ_2

I Path ADC Data

Address: 0x402E0104

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	ADC_2 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	ADC_2 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	ADC_2 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	ADC_2 [31:24]							

Bits	Name	Description
31 : 0	ADC_2	read out I path ADC data, second 16bits of I and Qcombination of 63bits Default Value: 0

3.1.64 BLE_BLERD_READ_IQ_3

I Path ADC Data

Address: 0x402E0108

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	ADC_3 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	ADC_3 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	ADC_3 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	ADC_3 [31:24]							

Bits	Name	Description
31 : 0	ADC_3	read out I path ADC data, third 16bits of I and Qcombination of 63bits Default Value: 0

3.1.65 BLE_BLERD_READ_IQ_4

I Path ADC Data

Address: 0x402E010C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	ADC_4 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	ADC_4 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	ADC_4 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	ADC_4 [31:24]							

Bits	Name	Description
31 : 0	ADC_4	read out I path ADC data, fourth 15bits of I and Qcombination of 63bits Default Value: 0

4 BLE Sub System (BLESS) Registers

This section discusses the BLESS registers. It lists all the registers in mapping tables, in address order.

4.1 Register Details

Register Name	Address
BLE_BLESS_WCO_CONFIG	0x402EF000
BLE_BLESS_WCO_STATUS	Address = 0x402EF004
BLE_BLESS_RF_CONFIG	Address = 0x402EF060
BLE_BLESS_XTAL_CLK_DIV_CONFIG	Address = 0x402EF064
BLE_BLESS_LL_DSM_INTR_STAT	Address = 0x402EF068
BLE_BLESS_LL_DSM_CTRL	Address = 0x402EF06C
BLE_BLESS_LL_CLK_EN	Address = 0x402EF070
BLE_BLESS_LF_CLK_CTRL	Address = 0x402EF074
BLE_BLESS_WCO_TRIM	Address = 0x402EFF00

4.1.1 BLE_BLESS_WCO_CONFIG

WCO Configuration Register

Address: 0x402EF000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [7:3]					EXT_INPUT_EN	LPM_AUTO	LPM_EN

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	ENBUS [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	ENABLE	None [30:24]						

Bits	Name	Description
31	ENABLE	Master enable for WCO oscillator Default Value: 0
23 : 16	ENBUS	Test Mode Control bits enbus[7] - N/A enbus[6] - 1=enable both primary Beta Multipliers enbus[5] - N/A enbus[4] - 1=enable digital oscillator detect enbus[3] - Load Resistor Control enbus[2] - Load Resistor Control enbus[1] - Load Resistor Control enbus[0] - Load Resistor Control Default Value: 71
2	EXT_INPUT_EN	Disables the load resistor and allows external clock input for pad_xin Default Value: 0
1	LPM_AUTO	Reserved - This bit is not functional and should be set to 0. Default Value: 1

(continued)

0	LPM_EN	Force block into Low Power Mode: 0: Do not force low power mode (LPM) on 1: Force low power mode (LPM) on Default Value: 0

4.1.2 BLE_BLESS_WCO_STATUS

WCO Status Register

Address: 0x402EF004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							OUT_BLNK_A

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	OUT_BLNK_A	Indicates that WCO clock has transitioned- This bit is intended for Test Mode Only and is not a reliable indicator. Default Value: 0

4.1.3 BLE_BLESS_RF_CONFIG

Radio configuration register

Address: 0x402EF060

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				None			RW
HW Access	R				None			R
Name	DDFT_MUX_CFG1 [7:4]				None [3:1]			RF_ENABLE

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	None		RW			
HW Access	R	R	None		R			
Name	BPKTCTL_FW_DRIVE	BPKTCTL_FW	None [13:12]		DDFT_MUX_CFG2 [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15	BPKTCTL_FW_DRIVE	Enabled FW drives BLERD bpkctl for radio standalone testing Default Value: 0
14	BPKTCTL_FW	FW drives BLERD bpktctl if this register bit 15 enabled Default Value: 0
11 : 8	DDFT_MUX_CFG2	dbg_mux_pin2 selection, combine with BLERD and BLESS 4'h0 dbg_pin_mux_2_rd 4'h1 rxdata (RD output) 4'b2 ll_decode_rx_data (llh_cy_asic output) 4'h3 dbus_tx_en (llh_cy_asic output) 4'h4 fw_clk_en (pwr_ctrl_top output) 4'h5 interrupt_ll_n (llh_cy_asic output) 4'h6 ll_st_sm (llh is in SM) 4'h7 ll_st_dsm (llh is in DSM) 4'he clk_gate_en_xtal (RD eco xtal clock gater enable) 4'hf bb_xo_amp_detect_dft_mux (RD output) Default Value: 0

(continued)

7 : 4	DDFT_MUX_CFG1	dbg_mux_pin1 selection, combine with BLERD and BLESS 4'h0 dbg_pin_mux_1_rd (RD output) 4'h1 rxclk (RD output) 4'h2 bpktctl_to_rd (RD input) 4'h3 dbus_rx_en (llh_cy_asic output) 4'h4 hw_clk_en (pwr_ctrl_top) 4'h5 clk_switch_to_sysclk (pwr_ctrl_top) 4'h6 ll_clk_en_sync (LL global clock enable from BLESS reg synced) 4'h7 dsm_entry_stat (llh_cy_asic output) 4'h8 ll_dsm_xo_on (LL in DSM, RD XO enabled) 4'h9 ll_dsm_xo_off (LL in DSM, RD XO disabled) 4'hf delayed_bg_en (m0s8bless_misc_dpslp_top output vs LS to s8blerf) Default Value: 0
0	RF_ENABLE	Enables the RF oscillator band gap. 1: band gap is enabled 0: band gap is disabled Default Value: 0

4.1.4 BLE_BLESS_XTAL_CLK_DIV_CONFIG

Crystal clock divider configuration register

Address: 0x402EF064

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW		RW	
HW Access	None				R		R	
Name	None [7:4]				LLCLK_DIV [3:2]		SYSCLK_DIV [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 2	LLCLK_DIV	Link Layer clock pre-divider value. The 24 MHz crystal clock is divided to generate the Link Layer clock. 0: NO_DIV: LLCLK= XTALCLK/1 1: DIV_BY_2: LLCLK= XTALCLK/2 2: DIV_BY_4: LLCLK= XTALCLK/4 3: DIV_BY_8: LLCLK= XTALCLK/8 Default Value: 0
1 : 0	SYSCLK_DIV	System clock pre-divider value. The 24 MHz crystal clock is divided to generate the system clock. 0: NO_DIV: SYSCLK= XTALCLK/1 1: DIV_BY_2: SYSCLK= XTALCLK/2 2: DIV_BY_4: SYSCLK= XTALCLK/4 3: DIV_BY_8: SYSCLK= XTALCLK/8 Default Value: 0

4.1.5 BLE_BLESS_LL_DSM_INTR_STAT

Link Layer interrupt status register

Address: 0x402EF068

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1C	RW1C
HW Access	None						RW1S	RW1S
Name	None [7:2]						DSM_EXITED_INTR	DSM_ENTERED_INTR

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1C
HW Access	None							RW1S
Name	None [15:9]							XTAL_ON_INTR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	XTAL_ON_INTR	enabled crystal stable signal rising edge interrupt. The interrupt can be cleared by writing one into this location. Default Value: 0
1	DSM_EXITED_INTR	On a firmware request to LL to exit from Deep Sleep Mode, working on LF clock, LL transitions from Deep Sleep Mode and asserts this interrupt when the Deep Sleep clock gater is turned ON. The interrupt can be cleared by writing one into this location. Default Value: 0
0	DSM_ENTERED_INTR	On a firmware request to LL to enter into state machine, working on LF clock, LL transitions into Deep Sleep Mode and asserts this interrupt. The interrupt can be cleared by writing one into this location. Default Value: 0

4.1.6 BLE_BLESS_LL_DSM_CTRL

Link Layer state machine control register

Address: 0x402EF06C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	RW1C
Name	None [7:4]				XTAL_ON_INTR_MASK	DSM_EXITED_INTR_MASK	DSM_ENTERED_INTR_MASK	DSM_EXIT

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	XTAL_ON_INTR_MASK	Masks the Crystal Stable Interrupt, when disabled. Default Value: 1
2	DSM_EXITED_INTR_MASK	Masks the DSM Exited Interrupt, when disabled. Default Value: 1
1	DSM_ENTERED_INTR_MASK	Masks the DSM Entered Interrupt, when disabled. Default Value: 1
0	DSM_EXIT	When the Link Layer is in Deep Sleep Mode, firmware can set this bit to wake the Link Layer. Default Value: 0

4.1.7 BLE_BLESS_LL_CLK_EN

Link Layer primary clock enable

Address: 0x402EF070

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						CY_CORREL_EN	CLK_EN

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CY_CORREL_EN	Set this bit 1 to enable Cypress Correlator logic to bypass MT logic Default Value: 1
0	CLK_EN	Set this bit 1 to enable the clock to Link Layer. Default Value: 0

4.1.8 BLE_BLESS_LF_CLK_CTRL

BLESS LF clock control

Address: 0x402EF074

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							DISABLE_LF_CLK

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	DISABLE_LF_CLK	When set to 1, gates the LF clock input to the Link Layer. Ths is done for extended DSM mode where the DSM state machine needs to be forzen to prevent a default auto exit. Default Value: 0

4.1.9 BLE_BLESS_WCO_TRIM

WCO Trim Register

Address: 0x402EFF00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW		None	RW		
HW Access	None		R		None	R		
Name	None [7:6]		LPM_GM [5:4]		None	XGM [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 4	LPM_GM	GM setting for LPM (bandwidth = DC/ms) Default Value: 1
2 : 0	XGM	Amplifier GM setting 0x0 - 3370 nA 0x1 - 2620 nA 0x2 - 2250 nA 0x3 - 1500 nA 0x4 - 1870 nA 0x5 - 1120 nA 0x6 - 750 nA 0x7 - 0 nA Default Value: 1

5 BLE Sub System Version 2 Registers

This section discusses the BLESS Version 2 registers. It lists all the registers in mapping tables, in address order.

5.1 Register Details

Register Name	Address
BLE_BLESS_WCO_CONFIG	0x402EF000
BLE_BLESS_WCO_STATUS	0x402EF004
BLE_BLESS_BIST_MODE_EN	0x402EF00C
BLE_BLESS_BIST_CMD	0x402EF010
BLE_BLESS_BIST_DATA	0x402EF014
BLE_BLESS_BIST_MASK	0x402EF018
BLE_BLESS_BIST_CTL	0x402EF01C
BLE_BLESS_BIST_STEP0_CTL	0x402EF020
BLE_BLESS_BIST_STEP1_CTL	0x402EF024
BLE_BLESS_BIST_STEP2_CTL	0x402EF028
BLE_BLESS_BIST_STEP3_CTL	0x402EF02C
BLE_BLESS_BIST_STEP4_CTL	0x402EF030
BLE_BLESS_BIST_STEP5_CTL	0x402EF034
BLE_BLESS_BIST_STEP6_CTL	0x402EF038
BLE_BLESS_BIST_STEP7_CTL	0x402EF03C
BLE_BLESS_BIST_ADDR_START	0x402EF040
BLE_BLESS_BIST_POL_MASK	0x402EF044
BLE_BLESS_BIST_STATUS	0x402EF048
BLE_BLESS_BIST_DATA_ACT	0x402EF04C
BLE_BLESS_BIST_DATA_EXP	0x402EF050
BLE_BLESS_BIST_ADDR	0x402EF054
BLE_BLESS_RF_CONFIG	0x402EF060
BLE_BLESS_XTAL_CLK_DIV_CONFIG	0x402EF064
BLE_BLESS_LL_DSM_INTR_STAT	0x402EF068
BLE_BLESS_LL_DSM_CTRL	0x402EF06C
BLE_BLESS_LL_CLK_EN	0x402EF070
BLE_BLESS_LF_CLK_CTRL	0x402EF074

Register Name	Address
BLE_BLESS_WCO_TRIM	0x402EFF00

5.1.1 BLE_BLESS_WCO_CONFIG

WCO Configuration Register

Address: 0x402EF000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [7:3]					EXT_INPUT_EN	LPM_AUTO	LPM_EN

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	ENBUS [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	ENABLE	None [30:24]						

Bits	Name	Description
31	ENABLE	Master enable for WCO oscillator Default Value: 0
23 : 16	ENBUS	Test Mode Control bits enbus[7] - N/A enbus[6] - 1=enable both primary Beta Multipliers enbus[5] - N/A enbus[4] - 1=enable digital oscillator detect enbus[3] - Load Resistor Control enbus[2] - Load Resistor Control enbus[1] - Load Resistor Control enbus[0] - Load Resistor Control Default Value: 71
2	EXT_INPUT_EN	Disables the load resistor and allows external clock input for pad_xin Default Value: 0

(continued)

1	LPM_AUTO	Automatically control low power mode (only relevant when LPM_EN=0): 0: Do not enter low power mode (LPM) in DeepSleep 1: Enter low power mode (LPM) in DeepSleep This bit is not functional and should be set to 0, While entering System Deepsleep Mode, do the following before executing WFI IOW BLESS.WCO_TRIM.XGM = 3b010 IOW BLESS.WCO_TRIM.LPM_GM = 2b10 IOW BLESS.WCO_CONFIG.LPM_EN = 1b1 While existing from System Deepsleep Mode, do the following before executing ISR IOW BLESS.WCO_CONFIG.LPM_EN = 1b0 IOW BLESS.WCO_TRIM.XGM = 3b001 IOW BLESS.WCO_TRIM.LPM_GM = 2b01 Default Value: 1
0	LPM_EN	Force block into Low Power Mode: 0: Do not force low power mode (LPM) on 1: Force low power mode (LPM) on Default Value: 0

5.1.2 BLE_BLESS_WCO_STATUS

WCO Status Register

Address: 0x402EF004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							OUT_BLNK_A

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	OUT_BLNK_A	Indicates that WCO clock has transitioned- This bit is intended for Test Mode Only and is not a reliable indicator. Default Value: 0

5.1.3 BLE_BLESS_BIST_MODE_EN

Memory BIST mode enable

Address: 0x402EF00C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							MEM_BIST_MODE

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	MEM_BIST_MODE	enables memory BIST mode 1'b0 : Memories are in functional mode and receive 24MHz Xtal clock 1'b1 : Memories are in BIST mode and receive system clock Default Value: 0

5.1.4 BLE_BLESS_BIST_CMD

Bist command register

Address: 0x402EF010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							RW1C
Name	None [7:1]							SRAM_GO

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	SRAM_GO	1': Start SRAM BIST. Hardware set this field to '0' when BIST is completed. Default Value: 0

5.1.5 BLE_BLESS_BIST_DATA

BIST data register

Address: 0x402EF014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data that is written into a SRAM during a W0 substep (~BIST_DATA.DATA is written into a SRAM during a W1 substep). Default Value: 0

5.1.6 BLE_BLESS_BIST_MASK

BIST mask register

Address: 0x402EF018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	MASK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	MASK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	MASK [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	MASK [31:24]							

Bits	Name	Description
31 : 0	MASK	Bit mask, which effectively reduces the data bits on which the BIST is performed. A '1' indicates that the corresponding data bit is partakes in BIST. Default Value: 4294967295

5.1.7 BLE_BLESS_BIST_CTL

BIST control register

Address: 0x402EF01C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		SRAMS_ENABLED [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW	RW	None	RW		
HW Access	None		R	R	None	R		
Name	None [23:22]		ADDR_START_ENABLED	ROW_FIRST	None	STEPS [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
21	ADDR_START_ENABLED	0': Row and column addresses start with their maximum/minimum values. '1': Row and column addresses start with their values as specified by BIST_ADDR_START. Default Value: 0
20	ROW_FIRST	Specifies how the SRAM addresses are generated: '0': Column address is incremented/decremented till it reaches its maximum/minimum value. Once it reach its maximum/minimum value, it is set to its mimimum/maximum value and only then is the row address incremented/decremented. '1': Row address is incremented/decremented till it reaches its maximum/minimum value. Once it reach its maximum/minimum value, it is set to its mimimum/maximum value and only then is the column address incremented/decremented. Default Value: 0

(continued)

18 : 16	STEPS	Amount of steps. The steps are further detailed by the BIST_STEPi_CTL registers. Multiple steps are used in sequence to implement a specific BIST algorithm: - MATS (4N, 3 steps: up/down W0; up/down R0_W1; up/down R1) - MATS+ (5N, 3 steps: up/down W0; up R0_W1; down R1_W0) - Marching 1/0 (14N, 6 steps: up/down W0; up R0_W1_R1; down R1_W0_R0; up/down W1; up R1_W0_R0; down R0_W1_R1) - MATS++ (6N, 3 steps: up/down W0; up R0_W1; down R1_W0_R0) - MARCH C (10N, 6 steps: up/down W0; up R0_W1; up R1_W0; up/down R0; down R1_W0_W1_W0; down R0_W1_W0) - MARCH A (15N, 5 steps: up/down W0; up R0_W1_W0_W1; up R1_W0_W1; down R1_W0_W1_W0; down R0_W1_W0) - MARCH Y (8N, 4 steps: up/down W0; up R0_W1_R1; down R1_W0_R0; up/down R0) - MARCH B (17N, 5 steps: up/down W0; up R0_W1_R1_W0_R0_W1; up R1_W0_W1; down R1_W0_W1_W0; down R0_W1_W0) - MARCH LR (14N, 6 steps: up/down W0; up R0_W1; up R1_W0_R0_W1; down R1_W0; down R0_W1_R1_W0; up/down R0) Default Value: 0
5 : 0	SRAMS_ENABLED	Hot-one mask for the SRAMs for which the BIST is performed. Default Value: 0 **0x1: ADV_TX_SRAM_MASK:** ADV TX FIFO memory **0x2: ADV_RX_SRAM_MASK:** ADV RX FIFO memory **0x4: CONN_RX_SRAM_MASK:** CONN RX FIFO0 and CONN RX FIFO1 memories **0x8: CONN_TX_SRAM_MASK:** CONN TX FIFO0 and CONN TX FIFO1 memories **0x10: DUT_SRAM_MASK:** DUP FIFO memory **0x20: WLF_SRAM_MASK:** WLF FIFO memory **0x40: ENC_SRAM_MASK:** ENC FIFO memory

5.1.8 BLE_BLESS_BIST_STEP0_CTL

BIST step 0 control register

Address: 0x402EF020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW			
HW Access	None			R	R			
Name	None [7:5]			UP	OPCODE [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4	UP	Specifies direction in which SRAM BIST steps through addresses '0': BIST steps through the SRAM from the maximum row and column addresses (as specified by a design time configurtion parameter when ADDR_START_ENABLED is '0' and as specified by BIST_ADDR_START when ADDR_START_ENABLED is '1') to the minimum row and column addresses. '1': BIST steps through the SRAM from the minimum row and column addresses ("0" when ADDR_START_ENABLED is '0' and as specified by BIST_ADDR_START when ADDR_START_ENABLED is '1') to the maximum row and column addresses. Default Value: 0

(continued)

3 : 0	OPCODE	Specifies what sequence of SRAM BIST steps (R0, R1, W0, W1) is performed (not used for SROM BIST): "0": W0. Write SRAM with BIST_DATA.DATA. "1": W1. Write SRAM with ~BIST_DATA.DATA. "2": R0. Read SRAM and compare output to BIST_DATA.DATA. "3": R1. Read SRAM and compare output to ~BIST_DATA.DATA. "4": W0, R0. Write SRAM with BIST_DATA.DATA, followed by read SRAM and compare output to BIST_DATA.DATA (all to the same address). "5": R0, W1. "6": R1, W0. "7": R0, W1, R1. "8": R1, W0, R0. "9": R0, W1, W0. "10": R1, W0, W1. "11": R0, W1, W0, W1. "12": R1, W0, W1, W0. "13": R0, W1, R1, W0. "14": R1, W0, R0, W1. "15": R0, W1, R1, W0, R0, W1. Default Value: 0

5.1.9 BLE_BLESS_BIST_STEP1_CTL

BIST step 1 control register

Address: 0x402EF024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW			
HW Access	None			R	R			
Name	None [7:5]			UP	OPCODE [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4	UP	See description of BIST_STEP0_CTL. Default Value: 0
3 : 0	OPCODE	See description of BIST_STEP0_CTL. Default Value: 0

5.1.10 BLE_BLESS_BIST_STEP2_CTL

BIST step 2 control register

Address: 0x402EF028

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW			
HW Access	None			R	R			
Name	None [7:5]			UP	OPCODE [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4	UP	See description of BIST_STEP0_CTL. Default Value: 0
3 : 0	OPCODE	See description of BIST_STEP0_CTL. Default Value: 0

5.1.11 BLE_BLESS_BIST_STEP3_CTL

BIST step 3 control register

Address: 0x402EF02C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW			
HW Access	None			R	R			
Name	None [7:5]			UP	OPCODE [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4	UP	See description of BIST_STEP0_CTL. Default Value: 0
3 : 0	OPCODE	See description of BIST_STEP0_CTL. Default Value: 0

5.1.12 BLE_BLESS_BIST_STEP4_CTL

BIST step 4 control register

Address: 0x402EF030

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW			
HW Access	None			R	R			
Name	None [7:5]			UP	OPCODE [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4	UP	See description of BIST_STEP0_CTL. Default Value: 0
3 : 0	OPCODE	See description of BIST_STEP0_CTL. Default Value: 0

5.1.13 BLE_BLESS_BIST_STEP5_CTL

BIST step 5 control register

Address: 0x402EF034

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW			
HW Access	None			R	R			
Name	None [7:5]			UP	OPCODE [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4	UP	See description of BIST_STEP0_CTL. Default Value: 0
3 : 0	OPCODE	See description of BIST_STEP0_CTL. Default Value: 0

5.1.14 BLE_BLESS_BIST_STEP6_CTL

BIST step 6 control register

Address: 0x402EF038

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW			
HW Access	None			R	R			
Name	None [7:5]			UP	OPCODE [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4	UP	See description of BIST_STEP0_CTL. Default Value: 0
3 : 0	OPCODE	See description of BIST_STEP0_CTL. Default Value: 0

5.1.15 BLE_BLESS_BIST_STEP7_CTL

BIST step 7 control register

Address: 0x402EF03C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW			
HW Access	None			R	R			
Name	None [7:5]			UP	OPCODE [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4	UP	See description of BIST_STEP0_CTL. Default Value: 0
3 : 0	OPCODE	See description of BIST_STEP0_CTL. Default Value: 0

5.1.16 BLE_BLESS_BIST_ADDR_START

BIST address start register

Address: 0x402EF040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	COL_ADDR_START [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				COL_ADDR_START [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	ROW_ADDR_START [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None				RW			
HW Access	None				R			
Name	None [31:28]				ROW_ADDR_START [27:24]			

Bits	Name	Description
27 : 16	ROW_ADDR_START	Row start address. Useful to apply BIST to a part of an SRAM. The value of this field should be in a legal range (a value outside of the legal range has an undefined result, and may lock up the BIST state machine). This legal range is dependent on the number of rows of the SRAM the BIST is applied to (as specified by BIST_CTL.SRAMS_ENABLED). E.g. for a SRAM with m columns, the legal range is [0, m-1]. Default Value: 0
11 : 0	COL_ADDR_START	Column start address. Useful to apply BIST to a part of an SRAM. The value of this field should be in a legal range (a value outside of the legal range has an undefined result, and may lock up the BIST state machine). This legal range is dependent on the number of columns of the SRAM the BIST is applied to (as specified by BIST_CTL.SRAMS_ENABLED). E.g. for a SRAM with n columns, the legal range is [0, n-1]. Default Value: 0

5.1.17 BLE_BLESS_BIST_POL_MASK

BIST address polarity mask register

Address: 0x402EF044

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	COL_POLARITY_MASK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	ROW_POLARITY_MASK [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	ROW_POLARITY_MASK	See description above. Default Value: 0
7 : 0	COL_POLARITY_MASK	Used to change the polarity of a step from R0 into R1 and vice versa or from W0 into W1 and vice versa. Given a row address ROW_ADDR and a column address COL_ADDR, the polarity is changed when the following expression is '1': ^ {(COL_ADDR[7:0] & COL_POLARITY_MASK), (ROW_ADDR[7:0] & ROW_POLARITY_MASK)} Default Value: 0

5.1.18 BLE_BLESS_BIST_STATUS

BIST status register

Address: 0x402EF048

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					R		
HW Access	None					W		
Name	None [7:3]					SUB_STEP [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None					R		
HW Access	None					W		
Name	None [15:11]					STEP [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	None				R			
HW Access	None				W			
Name	None [23:20]				SRAM [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							RW
HW Access	None							W1S
Name	None [31:25]							FAIL

Bits	Name	Description
24	FAIL	0': BIST passed. '1': BIST failed (SRAM match error or ROM MISR check error). BIST error information is found in SRAM, STEP, SUB_STEP fields and BIST_DATA_ACT, BIST_DATA_EXP and BIST_ADDR registers. Default Value: 0
19 : 16	SRAM	SRAM identifier. Default Value: Undefined **0x0: ADV_TX_SRAM:** ADV TX FIFO memory **0x1: ADV_RX_SRAM:** ADV RX FIFO memory **0x2: CONN_RX_SRAM:** CONN RX FIFO memory **0x3: CONN_TX_SRAM:** CONN TX FIFO memory **0x4: DUT_SRAM:** DUP FIFO memory

(continued)

		0x5: WLF_SRAM: WLF FIFO memory **0x6: ENC_SRAM:** ENC FIFO memory
10 : 8	STEP	BIST step (step i uses BIST_STEPi_CTL). Default Value: Undefined
2 : 0	SUB_STEP	BIST substep (either R0, R1, W0, or W1). Default Value: Undefined

5.1.19 BLE_BLESS_BIST_DATA_ACT

BIST data expected register

Address: 0x402EF04C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	For SRAM BIST, this field is the SRAM output data that caused a BIST failure. For ROM BIST, this field is the calculated Mulitple Input Shift Register (MISR). Default Value: Undefined

5.1.20 BLE_BLESS_BIST_DATA_EXP

BIST data actual register

Address: 0x402EF050

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	For SRAM BIST. This field is the expected data from SRAM. This value is BIST_DATA.DATA for a R0 substep and ~BIST_DATA.DATA for a R1 substep. Default Value: Undefined

5.1.21 BLE_BLESS_BIST_ADDR

BIST address register

Address: 0x402EF054

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	COL_ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None				R			
HW Access	None				W			
Name	None [15:12]				COL_ADDR [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	ROW_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None				R			
HW Access	None				W			
Name	None [31:28]				ROW_ADDR [27:24]			

Bits	Name	Description
27 : 16	ROW_ADDR	Current row address. Default Value: Undefined
11 : 0	COL_ADDR	Current column address. Default Value: Undefined

5.1.22 BLE_BLESS_RF_CONFIG

Radio configuration register

Address: 0x402EF060

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				None			RW
HW Access	R				None			R
Name	DDFT_MUX_CFG1 [7:4]				None [3:1]			RF_ENABLE

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	None		RW			
HW Access	R	R	None		R			
Name	BPKTCTL_FW_DRIVE	BPKTCTL_FW	None [13:12]		DDFT_MUX_CFG2 [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15	BPKTCTL_FW_DRIVE	Enabled FW drives BLERD bpkctl for radio standalone testing Default Value: 0
14	BPKTCTL_FW	FW drives BLERD bpktctl if this register bit 15 enabled Default Value: 0
11 : 8	DDFT_MUX_CFG2	dbg_mux_pin2 selection, combine with BLERD and BLESS 4'h0 dbg_pin_mux_2_rd 4'h1 rxdata (RD output) 4'b2 ll_decode_rx_data (llh_cy_asic output) 4'h3 dbus_tx_en (llh_cy_asic output) 4'h4 fw_clk_en (pwr_ctrl_top output) 4'h5 interrupt_ll_n (llh_cy_asic output) 4'h6 ll_st_sm (llh is in SM) 4'h7 ll_st_dsm (llh is in DSM) 4'he clk_gate_en_xtal (RD eco xtal clock gater enable) 4'hf bb_xo_amp_detect_dft_mux (RD output) Default Value: 0

(continued)

7 : 4	DDFT_MUX_CFG1	dbg_mux_pin1 selection, combine with BLERD and BLESS 4'h0 dbg_pin_mux_1_rd (RD output) 4'h1 rxclk (RD output) 4'h2 bpktctl_to_rd (RD input) 4'h3 dbus_rx_en (llh_cy_asic output) 4'h4 hw_clk_en (pwr_ctrl_top) 4'h5 clk_switch_to_sysclk (pwr_ctrl_top) 4'h6 ll_clk_en_sync (LL global clock enable from BLESS reg synced) 4'h7 dsm_entry_stat (llh_cy_asic output) 4'h8 ll_dsm_xo_on (LL in DSM, RD XO enabled) 4'h9 ll_dsm_xo_off (LL in DSM, RD XO disabled) 4'hf delayed_bg_en (m0s8bless_misc_dpslp_top output vs LS to s8blerf) Default Value: 0
0	RF_ENABLE	Enables the RF oscillator band gap. 1: band gap is enabled 0: band gap is disabled Default Value: 0

5.1.23 BLE_BLESS_XTAL_CLK_DIV_CONFIG

Crystal clock divider configuration register

Address: 0x402EF064

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW		RW	
HW Access	None				R		R	
Name	None [7:4]				LLCLK_DIV [3:2]		SYSCLK_DIV [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 2	LLCLK_DIV	Link Layer clock pre-divider value. The 24 MHz crystal clock is divided to generate the Link Layer clock. 0: NO_DIV: LLCLK= XTALCLK/1 1: DIV_BY_2: LLCLK= XTALCLK/2 2: DIV_BY_4: LLCLK= XTALCLK/4 3: DIV_BY_8: LLCLK= XTALCLK/8 Default Value: 0
1 : 0	SYSCLK_DIV	System clock pre-divider value. The 24 MHz crystal clock is divided to generate the system clock. 0: NO_DIV: SYSCLK= XTALCLK/1 1: DIV_BY_2: SYSCLK= XTALCLK/2 2: DIV_BY_4: SYSCLK= XTALCLK/4 3: DIV_BY_8: SYSCLK= XTALCLK/8 Default Value: 0

5.1.24 BLE_BLESS_LL_DSM_INTR_STAT

Link Layer interrupt status register

Address: 0x402EF068

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1C	RW1C
HW Access	None						RW1S	RW1S
Name	None [7:2]						DSM_EXITED_INTR	DSM_ENTERED_INTR

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1C
HW Access	None							RW1S
Name	None [15:9]							XTAL_ON_INTR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	XTAL_ON_INTR	enabled crystal stable signal rising edge interrupt. The interrupt can be cleared by writing one into this location. Default Value: 0
1	DSM_EXITED_INTR	On a firmware request to LL to exit from Deep Sleep Mode, working on LF clock, LL transitions from Deep Sleep Mode and asserts this interrupt when the Deep Sleep clock gater is turned ON. The interrupt can be cleared by writing one into this location. Default Value: 0
0	DSM_ENTERED_INTR	On a firmware request to LL to enter into state machine, working on LF clock, LL transitions into Deep Sleep Mode and asserts this interrupt. The interrupt can be cleared by writing one into this location. Default Value: 0

5.1.25 BLE_BLESS_LL_DSM_CTRL

Link Layer state machine control register

Address: 0x402EF06C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	RW1C
Name	None [7:4]				XTAL_ON_INTR_MASK	DSM_EXITED_INTR_MASK	DSM_ENTERED_INTR_MASK	DSM_EXIT

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	XTAL_ON_INTR_MASK	Masks the Crystal Stable Interrupt, when disabled. Default Value: 1
2	DSM_EXITED_INTR_MASK	Masks the DSM Exited Interrupt, when disabled. Default Value: 1
1	DSM_ENTERED_INTR_MASK	Masks the DSM Entered Interrupt, when disabled. Default Value: 1
0	DSM_EXIT	When the Link Layer is in Deep Sleep Mode, firmware can set this bit to wake the Link Layer. Default Value: 0

5.1.26 BLE_BLESS_LL_CLK_EN

Link Layer primary clock enable

Address: 0x402EF070

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						CY_CORREL_EN	CLK_EN

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CY_CORREL_EN	Set this bit 1 to enable Cypress Correlator logic to bypass MT logic Default Value: 1
0	CLK_EN	Set this bit 1 to enable the clock to Link Layer. Default Value: 0

5.1.27 BLE_BLESS_LF_CLK_CTRL

BLESS LF clock control and BLESS revision ID indicator

Address: 0x402EF074

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							DISABLE_LF_CLK

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R			None				
HW Access	R			None				
Name	M0S8BLESS_REV_ID [31:29]			None [28:24]				

Bits	Name	Description
31 : 29	M0S8BLESS_REV_ID	Indicates the m0s8bless IP revision. Default Value: 1
0	DISABLE_LF_CLK	When set to 1, gates the LF clock input to the Link Layer. Ths is done for extended DSM mode where the DSM state machine needs to be forzen to prevent a default auto exit. Default Value: 0

5.1.28 BLE_BLESS_WCO_TRIM

WCO Trim Register

Address: 0x402EFF00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW		None	RW		
HW Access	None		R		None	R		
Name	None [7:6]		LPM_GM [5:4]		None	XGM [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 4	LPM_GM	GM setting for LPM (bandwidth = DC/ms) Default Value: 1
2 : 0	XGM	Amplifier GM setting 0x0 - 3370 nA 0x1 - 2620 nA 0x2 - 2250 nA 0x3 - 1500 nA 0x4 - 1870 nA 0x5 - 1120 nA 0x6 - 750 nA 0x7 - 0 nA Default Value: 1

6 Cortex M0 (CM0) Registers

This section discusses the CM0 registers. It lists all the registers in mapping tables, in address order.

6.1 Register Details

Register Name	Address
CM0_DWT_PID4	0xE0001FD0
CM0_DWT_PID0	0xE0001FE0
CM0_DWT_PID1	0xE0001FE4
CM0_DWT_PID2	0xE0001FE8
CM0_DWT_PID3	0xE0001FEC
CM0_DWT_CID0	0xE0001FF0
CM0_DWT_CID1	0xE0001FF4
CM0_DWT_CID2	0xE0001FF8
CM0_DWT_CID3	0xE0001FFC
CM0_BP_PID4	0xE0002FD0
CM0_BP_PID0	0xE0002FE0
CM0_BP_PID1	0xE0002FE4
CM0_BP_PID2	0xE0002FE8
CM0_BP_PID3	0xE0002FEC
CM0_BP_CID0	0xE0002FF0
CM0_BP_CID1	0xE0002FF4
CM0_BP_CID2	0xE0002FF8
CM0_BP_CID3	0xE0002FFC
CM0_SYST_CSR	0xE000E010
CM0_SYST_RVR	0xE000E014
CM0_SYST_CVR	0xE000E018
CM0_SYST_CALIB	0xE000E01C
CM0_ISER	0xE000E100
CM0_ICER	0xE000E180
CM0_ISPR	0xE000E200
CM0_ICPR	0xE000E280

Register Name	Address
CM0_IPR0	0xE000E400
CM0_IPR1	0xE000E404
CM0_IPR2	0xE000E408
CM0_IPR3	0xE000E40C
CM0_IPR4	0xE000E410
CM0_IPR5	0xE000E414
CM0_IPR6	0xE000E418
CM0_IPR7	0xE000E41C
CM0_CPUID	0xE000ED00
CM0_ICSR	0xE000ED04
CM0_AIRCR	0xE000ED0C
CM0_SCR	0xE000ED10
CM0_CCR	0xE000ED14
CM0_SHPR2	0xE000ED1C
CM0_SHPR3	0xE000ED20
CM0_SHCSR	0xE000ED24
CM0_SCS_PID4	0xE000EFD0
CM0_SCS_PID0	0xE000EFE0
CM0_SCS_PID1	0xE000EFE4
CM0_SCS_PID2	0xE000EFE8
CM0_SCS_PID3	0xE000EFEC
CM0_SCS_CID0	0xE000EFF0
CM0_SCS_CID1	0xE000EFF4
CM0_SCS_CID2	0xE000EFF8
CM0_SCS_CID3	0xE000EFFC
CM0_ROM_SCS	0xE00FF000
CM0_ROM_DWT	0xE00FF004
CM0_ROM_BPU	0xE00FF008
CM0_ROM_END	0xE00FF00C
CM0_ROM_CSMT	0xE00FFFCC
CM0_ROM_PID4	0xE00FFFD0
CM0_ROM_PID0	0xE00FFFE0
CM0_ROM_PID1	0xE00FFFE4
CM0_ROM_PID2	0xE00FFFE8
CM0_ROM_PID3	0xE00FFFEC
CM0_ROM_CID0	0xE00FFFF0
CM0_ROM_CID1	0xE00FFFF4
CM0_ROM_CID2	0xE00FFFF8
CM0_ROM_CID3	0xE00FFFFC

6.1.1 CM0_DWT_PID4

Watchpoint Unit CoreSight ROM Table Peripheral ID #4

Address: 0xE0001FD0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #4 Default Value: 4

6.1.2 CM0_DWT_PID0

Watchpoint Unit CoreSight ROM Table Peripheral ID #0

Address: 0xE0001FE0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #0 Default Value: 10

6.1.3 CM0_DWT_PID1

Watchpoint Unit CoreSight ROM Table Peripheral ID #1

Address: 0xE0001FE4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #1 Default Value: 176

6.1.4 CM0_DWT_PID2

Watchpoint Unit CoreSight ROM Table Peripheral ID #2

Address: 0xE0001FE8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #2 Default Value: 11

6.1.5 CM0_DWT_PID3

Watchpoint Unit CoreSight ROM Table Peripheral ID #3

Address: 0xE0001FEC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #3 Default Value: 0

6.1.6 CM0_DWT_CID0

Watchpoint Unit CoreSight ROM Table Component ID #0

Address: 0xE0001FF0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #0 Default Value: 13

6.1.7 CM0_DWT_CID1

Watchpoint Unit CoreSight ROM Table Component ID #1

Address: 0xE0001FF4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #1 Default Value: 224

6.1.8 CM0_DWT_CID2

Watchpoint Unit CoreSight ROM Table Component ID #2

Address: 0xE0001FF8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #2 Default Value: 5

6.1.9 CM0_DWT_CID3

Watchpoint Unit CoreSight ROM Table Component ID #3

Address: 0xE0001FFC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #3 Default Value: 177

6.1.10 CM0_BP_PID4

Breakpoint Unit CoreSight ROM Table Peripheral ID #4

Address: 0xE0002FD0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #4 Default Value: 4

6.1.11 CM0_BP_PID0

Breakpoint Unit CoreSight ROM Table Peripheral ID #0

Address: 0xE0002FE0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #0 Default Value: 11

6.1.12 CM0_BP_PID1

Breakpoint Unit CoreSight ROM Table Peripheral ID #1

Address: 0xE0002FE4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #1 Default Value: 176

6.1.13 CM0_BP_PID2

Breakpoint Unit CoreSight ROM Table Peripheral ID #2

Address: 0xE0002FE8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #2 Default Value: 11

6.1.14 CM0_BP_PID3

Breakpoint Unit CoreSight ROM Table Peripheral ID #3

Address: 0xE0002FEC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #3 Default Value: 0

6.1.15 CM0_BP_CID0

Breakpoint Unit CoreSight ROM Table Component ID #0

Address: 0xE0002FF0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #0 Default Value: 13

6.1.16 CM0_BP_CID1

Breakpoint Unit CoreSight ROM Table Component ID #1

Address: 0xE0002FF4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #1 Default Value: 224

6.1.17 CM0_BP_CID2

Breakpoint Unit CoreSight ROM Table Component ID #2

Address: 0xE0002FF8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #2 Default Value: 5

6.1.18 CM0_BP_CID3

Breakpoint Unit CoreSight ROM Table Component ID #3

Address: 0xE0002FFC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #3 Default Value: 177

6.1.19 CM0_SYST_CSR

SysTick Control & Status

Address: 0xE000E010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [7:3]					CLK-SOURCE	TICKINT	ENABLE

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							R
HW Access	None							RW
Name	None [23:17]							COUNT-FLAG

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
16	COUNTFLAG	Indicates whether the counter has counted to "0" since the last read of this register: '0': counter has not counted to "0". '1': counter has counted to "0". COUNTFLAG is set to '1' by a count transition from "1" to "0". COUNTFLAG is cleared to '0' by a read of this register, and by any write to the SYST_CVR register. Default Value: 0

(continued)

2	CLKSOURCE	Indicates the SysTick counter clock source: '0': SysTick uses the low frequency clock "clk_lf". For this mode to function, "clk_lf" should be less than half the frequency of "clk_sys". Note that "clk_lf" is generated by a low accuracy ILO (Internal Low power Oscillator), with a target frequency of 32.768 kHz (frequency can be as low as 15 KHz and as high as 60 kHz). '1': SysTick uses the system/processor clock "clk_sys". In PSoC4A-BLE (and later products), SysTick counter functionality on the low frequency clock is provided. in SF, TSG6M products, this functionality is not provided. For these products, this field should be set to '1', such that SysTick uses the system clock "clk_sys". Default Value: 0
1	TICKINT	Indicates whether counting to "0" causes the status of the SysTick exception to change to pending: '0': count to "0" does not affect the SysTick exception status. '1': count to "0" changes the SysTick exception status to pending. Changing the value of the counter to "0" by writing zero to the SYST_CVR register to "0" never changes the status of the SysTick exception. Default Value: 0
0	ENABLE	Indicates the enabled status of the SysTick counter: '0': counter is disabled. '1': counter is operating. Default Value: 0

6.1.20 CM0_SYST_RVR

SysTick Reload Value

Address: 0xE000E014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	RELOAD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	RELOAD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	RELOAD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 0	RELOAD	The value to load into the SYST_CVR register when the counter reaches 0. Default Value: X

6.1.21 CM0_SYST_CVR

SysTick Current Value

Address: 0xE000E018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CURRENT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CURRENT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	CURRENT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 0	CURRENT	Current counter value. This is the value of the counter at the time it is sampled. Default Value: X

6.1.22 CM0_SYST_CALIB

SysTick Calibration Value

Address: 0xE000E01C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	TENMS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	TENMS [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	TENMS [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	None					
HW Access	None	RW	None					
Name	NOREF	SKEW	None [29:24]					

Bits	Name	Description
31	NOREF	Indicates whether a implementation defined reference clock is provided: '0': the reference clock is provided. '1': the reference clock is not provided. When this bit is '1', the SYST_CSR.CLKSOURCEis forced to '1' and cannot be cleared to '0'. In PSoC4A-BLE (and later products), SysTick counter functionality on the low frequency clock is provided and this field is '0'. In earlier products, SysTick counter functionality on the low frequency clock is NOT provided and this field is '1'. Default Value: 0
30	SKEW	Indicates whether the 10ms calibration value is exact: '0': 10ms calibration value is exact. '1': 10ms calibration value is inexact, because of the clock frequency. In PSoC4A-BLE (and later products), SysTick counter functionality on the low frequency clock is provided and this field is '1' (due to the low accuracy ILO). In earlier products, SysTick counter functionality on the low frequency clock is NOT provided and this field is '0'. Default Value: X

(continued)

23 : 0	TENMS	Optionally, holds a reload value to be used for 10ms (100Hz) timing, subject to system clock skew errors. If this field is "0", the calibration value is not known. In PSoC4A-BLE (and later products), SysTick counter functionality on the low frequency clock is provided and this field is 0x00:00147. In earlier products, SysTick counter functionality on the low frequency clock is NOT provided and this field is 0x00:0000. Default Value: X

6.1.23 CM0_ISER

Interrupt Set-Enable Register

Address: 0xE000E100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S							
HW Access	R							
Name	SETENA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1S							
HW Access	R							
Name	SETENA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW1S							
HW Access	R							
Name	SETENA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1S							
HW Access	R							
Name	SETENA [31:24]							

Bits	Name	Description
31 : 0	SETENA	Enables, or reads the enabled state of one or more interrupts. Each bit corresponds to the same numbered interrupt. Default Value: 0

6.1.24 CM0_ICER

Interrupt Clear Enable Register

Address: 0xE000E180

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C							
HW Access	R							
Name	CLRENA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1C							
HW Access	R							
Name	CLRENA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW1C							
HW Access	R							
Name	CLRENA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1C							
HW Access	R							
Name	CLRENA [31:24]							

Bits	Name	Description
31 : 0	CLRENA	Disables, or reads the enabled state of one or more interrupts. Each bit corresponds to the same numbered interrupt. Default Value: 0

6.1.25 CM0_ISPR

Interrupt Set-Pending Register

Address: 0xE000E200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S							
HW Access	R							
Name	SETPEND [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1S							
HW Access	R							
Name	SETPEND [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW1S							
HW Access	R							
Name	SETPEND [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1S							
HW Access	R							
Name	SETPEND [31:24]							

Bits	Name	Description
31 : 0	SETPEND	Changes the state of one or more interrupts to pending. Each bit corresponds to the same numbered interrupt. Default Value: 0

6.1.26 CM0_ICPR

Interrupt Clear-Pending Register

Address: 0xE000E280

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C							
HW Access	R							
Name	CLRPEND [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1C							
HW Access	R							
Name	CLRPEND [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW1C							
HW Access	R							
Name	CLRPEND [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1C							
HW Access	R							
Name	CLRPEND [31:24]							

Bits	Name	Description
31 : 0	CLRPEND	Changes the state of one or more interrupts to not pending. Each bit corresponds to the same numbered interrupt. Default Value: 0

6.1.27 CM0_IPR0

Interrupt Priority Registers

Address: 0xE000E400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N0 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N1 [15:14]		None [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N2 [23:22]		None [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N3 [31:30]		None [29:24]					

Bits	Name	Description
31 : 30	PRI_N3	Priority of interrupt number N+3. Default Value: 0
23 : 22	PRI_N2	Priority of interrupt number N+2. Default Value: 0
15 : 14	PRI_N1	Priority of interrupt number N+1. Default Value: 0
7 : 6	PRI_N0	Priority of interrupt number N. Default Value: 0

6.1.28 CM0_IPR1

Interrupt Priority Registers

Address: 0xE000E404

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N0 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N1 [15:14]		None [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N2 [23:22]		None [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N3 [31:30]		None [29:24]					

Bits	Name	Description
31 : 30	PRI_N3	Priority of interrupt number N+3. Default Value: 0
23 : 22	PRI_N2	Priority of interrupt number N+2. Default Value: 0
15 : 14	PRI_N1	Priority of interrupt number N+1. Default Value: 0
7 : 6	PRI_N0	Priority of interrupt number N. Default Value: 0

6.1.29 CM0_IPR2

Interrupt Priority Registers

Address: 0xE000E408

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N0 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N1 [15:14]		None [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N2 [23:22]		None [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N3 [31:30]		None [29:24]					

Bits	Name	Description
31 : 30	PRI_N3	Priority of interrupt number N+3. Default Value: 0
23 : 22	PRI_N2	Priority of interrupt number N+2. Default Value: 0
15 : 14	PRI_N1	Priority of interrupt number N+1. Default Value: 0
7 : 6	PRI_N0	Priority of interrupt number N. Default Value: 0

6.1.30 CM0_IPR3

Interrupt Priority Registers

Address: 0xE000E40C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N0 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N1 [15:14]		None [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N2 [23:22]		None [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N3 [31:30]		None [29:24]					

Bits	Name	Description
31 : 30	PRI_N3	Priority of interrupt number N+3. Default Value: 0
23 : 22	PRI_N2	Priority of interrupt number N+2. Default Value: 0
15 : 14	PRI_N1	Priority of interrupt number N+1. Default Value: 0
7 : 6	PRI_N0	Priority of interrupt number N. Default Value: 0

6.1.31 CM0_IPR4

Interrupt Priority Registers

Address: 0xE000E410

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N0 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N1 [15:14]		None [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N2 [23:22]		None [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N3 [31:30]		None [29:24]					

Bits	Name	Description
31 : 30	PRI_N3	Priority of interrupt number N+3. Default Value: 0
23 : 22	PRI_N2	Priority of interrupt number N+2. Default Value: 0
15 : 14	PRI_N1	Priority of interrupt number N+1. Default Value: 0
7 : 6	PRI_N0	Priority of interrupt number N. Default Value: 0

6.1.32 CM0_IPR5

Interrupt Priority Registers

Address: 0xE000E414

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N0 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N1 [15:14]		None [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N2 [23:22]		None [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N3 [31:30]		None [29:24]					

Bits	Name	Description
31 : 30	PRI_N3	Priority of interrupt number N+3. Default Value: 0
23 : 22	PRI_N2	Priority of interrupt number N+2. Default Value: 0
15 : 14	PRI_N1	Priority of interrupt number N+1. Default Value: 0
7 : 6	PRI_N0	Priority of interrupt number N. Default Value: 0

6.1.33 CM0_IPR6

Interrupt Priority Registers

Address: 0xE000E418

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N0 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N1 [15:14]		None [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N2 [23:22]		None [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N3 [31:30]		None [29:24]					

Bits	Name	Description
31 : 30	PRI_N3	Priority of interrupt number N+3. Default Value: 0
23 : 22	PRI_N2	Priority of interrupt number N+2. Default Value: 0
15 : 14	PRI_N1	Priority of interrupt number N+1. Default Value: 0
7 : 6	PRI_N0	Priority of interrupt number N. Default Value: 0

6.1.34 CM0_IPR7

Interrupt Priority Registers

Address: 0xE000E41C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N0 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N1 [15:14]		None [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N2 [23:22]		None [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N3 [31:30]		None [29:24]					

Bits	Name	Description
31 : 30	PRI_N3	Priority of interrupt number N+3. Default Value: 0
23 : 22	PRI_N2	Priority of interrupt number N+2. Default Value: 0
15 : 14	PRI_N1	Priority of interrupt number N+1. Default Value: 0
7 : 6	PRI_N0	Priority of interrupt number N. Default Value: 0

6.1.35 CM0_CPUID

CPUID Register

Address: 0xE000ED00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	None				None			
Name	PARTNO [7:4]				REVISION [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	PARTNO [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R				R			
HW Access	None				None			
Name	VARIANT [23:20]				CONSTANT [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	IMPLEMENTER [31:24]							

Bits	Name	Description
31 : 24	IMPLEMENTER	Implementer code for ARM. Default Value: 65
23 : 20	VARIANT	Implementation defined. In ARM implementations this is the major revision number n in the rn part of the rnpn revision status, Product revision status on page xii. Default Value: 0
19 : 16	CONSTANT	Indicates the architecture, ARMv6-M Default Value: 12
15 : 4	PARTNO	Indicates part number, Cortex-M0 Default Value: 3104
3 : 0	REVISION	Indicates revision. In ARM implementations this is the minor revision number n in the pn part of the rnpn revision status, see Product revision status on page xii. For release r0p0. Default Value: 0

6.1.36 CM0_ICSR

Interrupt Control State Register

Address: 0xE000ED04

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	VECTACTIVE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R				None			R
HW Access	RW				None			RW
Name	VECTPENDING [15:12]				None [11:9]			VECTAC-TIVE

Bits	23	22	21	20	19	18	17	16
SW Access	R	R	None	R				
HW Access	RW	RW	None	RW				
Name	ISRPRE-EMPT	ISRPEND-ING	None	VECTPENDING [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	RW1S	None		RW1S	RW1C	RW1S	RW1C	None
HW Access	RW	None		RW	R	RW	R	None
Name	NMIPEND-SET	None [30:29]		PENDSV-SET	PENDSV-CLR	PENDST-SETb	PENDST-CLR	None

Bits	Name	Description
31	NMIPENDSET	Activates an NMI exception or reads back the current state. Because NMI is the highest priority exception, it activates as soon as it is registered. Default Value: 0
28	PENDSVSET	Sets a pending PendSV interrupt or reads back the current state. Use this normally to request a context switch. Writing PENDSVSET and PENDSVCLR to '1' concurrently is UNPREDICT-ABLE. Default Value: 0
27	PENDSVCLR	Clears a pending PendSV interrupt. Default Value: 0
26	PENDSTSETb	Sets a pending SysTick or reads back the current state. Writing PENDSTSET and PENDSTCLR to '1' concurrently is UNPREDICTABLE. Default Value: 0
25	PENDSTCLR	Clears a pending SysTick, whether set here or by the timer hardware. Default Value: 0

(continued)

23	ISRPREEMPT	Indicates whether a pending exception will be serviced on exit from debug halt state. Default Value: 0
22	ISRPENDING	Indicates if an external configurable, NVIC generated, interrupt is pending. Default Value: 0
20 : 12	VECTPENDING	The exception number for the highest priority pending exception. 0= No pending exceptions. The pending state includes the effect of memory-mapped enable and mask registers. It does not include the PRIMASK special-purpose register qualifier. Default Value: 0
8 : 0	VECTACTIVE	The exception number for the current executing exception. 0= Thread mode. This is the same value as IPSR[8:0] Default Value: 0

6.1.37 CM0_AIRCR

Application Interrupt and Reset Control Register

Address: 0xE000ED0C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW1S	RW1C	None
HW Access	None					R	R	None
Name	None [7:3]					SYSRESE-TREQ	VECTCL-RACTIVE	None

Bits	15	14	13	12	11	10	9	8
SW Access	R	None						
HW Access	None	None						
Name	ENDIAN-NESS	None [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VECTKEY [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VECTKEY [31:24]							

Bits	Name	Description
31 : 16	VECTKEY	Vector Key. The value 0x05FA must be written to this register, otherwise the register write is UN-PREDICTABLE. Readback value is UNKNOWN. Default Value: X
15	ENDIANNESS	Indicates the memory system data endianness: 0 little endian 1 big endian. See Endian support on page A3-44 for more information. Default Value: 0
2	SYSRESETREQ	System Reset Request. Writing 1 to this bit asserts a signal to request a reset by the external system. This will cause a full system reset of the CPU and all other components in the device. See Reset management on page B1-240 for more information. Default Value: 0
1	VECTCLRACTIVE	Clears all active state information for fixed and configurable exceptions. The effect of writing a 1 to this bit if the processor is not halted in Debug state is UNPREDICTABLE. Default Value: 0

6.1.38 CM0_SCR

System Control Register

Address: 0xE000ED10

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	None	RW	RW	None
HW Access	None			R	None	R	R	None
Name	None [7:5]			SEVON-PEND	None	SLEEP-DEEP	SLEEPON-EXIT	None

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4	SEVONPEND	Determines whether an interrupt transition from inactive state to pending state is a wakeup event: 0: transitions from inactive to pending are not wakeup events. 1: transitions from inactive to pending are wakeup events. See WFE on page A6-197 for more information. Default Value: 0
2	SLEEPDEEP	An implementation can use this bit to select DeepSleep/Hibernate power modes upon execution of WFI/WFE: 0: Select Sleep mode 1: Select DeepSleep/Hibernate (depends on PWR_CONTROL.HIBERNATE) Default Value: 0
1	SLEEPONEXIT	Determines whether, on an exit from an ISR that returns to the base level of execution priority, the processor enters a sleep state: 0 do not enter sleep state. 1 enter sleep state. See Power management on page B1-240 for more information. Default Value: 0

6.1.39 CM0_CCR

Configuration and Control Register

Address: 0xE000ED14

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R	None		
HW Access	None				None	None		
Name	None [7:4]				UNALIGN_ TRP	None [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None						R	None
HW Access	None						None	None
Name	None [15:10]						STKALIGN	None

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	STKALIGN	1: On exception entry, the SP used prior to the exception is adjusted to be 8-byte aligned and the context to restore it is saved. The SP is restored on the associated exception return. Default Value: 1
3	UNALIGN_TRP	1: unaligned word and halfword accesses generate a HardFault exception. Default Value: 1

6.1.40 CM0_SHPR2

System Handler Priority Register 2

Address: 0xE000ED1C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None					
HW Access	R		None					
Name	PRI_11 [31:30]		None [29:24]					

Bits	Name	Description
31 : 30	PRI_11	Priority of system handler 11, SVCall Default Value: 0

6.1.41 CM0_SHPR3

System Handler Priority Register 3

Address: 0xE000ED20

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW		None					
HW Access	R		None					
Name	PRI_14 [23:22]		None [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None					
HW Access	R		None					
Name	PRI_15 [31:30]		None [29:24]					

Bits	Name	Description
31 : 30	PRI_15	Priority of system handler 15, SysTick Default Value: 0
23 : 22	PRI_14	Priority of system handler 14, PendSV Default Value: 0

6.1.42 CM0_SHCSR

System Handler Control and State Register

Address: 0xE000ED24

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW	None						
HW Access	RW	None						
Name	SVCALL-PENDED	None [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15	SVCALLPENDED	0 SVCall is not pending. 1 SVCall is pending. This bit reflects the pending state on a read, and updates the pending state, to the value written, on a write. (Pending state bits are set to 1 when an exception occurs, and are cleared to 0 when an exception becomes active.) Default Value: 0

6.1.43 CM0_SCS_PID4

System Control Space ROM Table Peripheral ID #4

Address: 0xE000EFD0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #4 Default Value: 4

6.1.44 CM0_SCS_PID0

System Control Space ROM Table Peripheral ID #0

Address: 0xE000EFE0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #0 Default Value: 8

6.1.45 CM0_SCS_PID1

System Control Space ROM Table Peripheral ID #1

Address: 0xE000EFE4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #1 Default Value: 176

6.1.46 CM0_SCS_PID2

System Control Space ROM Table Peripheral ID #2

Address: 0xE000EFE8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #2 Default Value: 11

6.1.47 CM0_SCS_PID3

System Control Space ROM Table Peripheral ID #3

Address: 0xE000EFEC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #3 Default Value: 0

6.1.48 CM0_SCS_CID0

System Control Space ROM Table Component ID #0

Address: 0xE000EFF0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #0 Default Value: 13

6.1.49 CM0_SCS_CID1

System Control Space ROM Table Component ID #1

Address: 0xE000EFF4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #1 Default Value: 224

6.1.50 CM0_SCS_CID2

System Control Space ROM Table Component ID #2

Address: 0xE000EFF8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #2 Default Value: 5

6.1.51 CM0_SCS_CID3

System Control Space ROM Table Component ID #3

Address: 0xE000EFFC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #3 Default Value: 177

6.1.52 CM0_ROM_SCS

CM0 CoreSight ROM Table Peripheral #0

Address: 0xE00FF000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Offset to SCS ROM Table Default Value: 4293980163

6.1.53 CM0_ROM_DWT

CM0 CoreSight ROM Table Peripheral #1

Address: 0xE00FF004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Offset to DWT ROM Table Default Value: 4293926915

6.1.54 CM0_ROM_BPU

CM0 CoreSight ROM Table Peripheral #2

Address: 0xE00FF008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Offset to BPU ROM Table Default Value: 4293931011

6.1.55 CM0_ROM_END

CM0 CoreSight ROM Table End Marker

Address: 0xE00FF00C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	End marker in peripheral list Default Value: 0

6.1.56 CM0_ROM_CSMT

CM0 CoreSight ROM Table Memory Type

Address: 0xE00FFFCC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Memory Type Default Value: 1

6.1.57 CM0_ROM_PID4

CM0 CoreSight ROM Table Peripheral ID #4

Address: 0xE00FFFD0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #4 Default Value: 4

6.1.58 CM0_ROM_PID0

CM0 CoreSight ROM Table Peripheral ID #0

Address: 0xE00FFFE0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #0 Default Value: 113

6.1.59 CM0_ROM_PID1

CM0 CoreSight ROM Table Peripheral ID #1

Address: 0xE00FFFE4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #1 Default Value: 180

6.1.60 CM0_ROM_PID2

CM0 CoreSight ROM Table Peripheral ID #2

Address: 0xE00FFFE8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #2 Default Value: 11

6.1.61 CM0_ROM_PID3

CM0 CoreSight ROM Table Peripheral ID #3

Address: 0xE00FFFEC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #3 Default Value: 0

6.1.62 CM0_ROM_CID0

CM0 CoreSight ROM Table Component ID #0

Address: 0xE00FFFF0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #0 Default Value: 13

6.1.63 CM0_ROM_CID1

CM0 CoreSight ROM Table Component ID #1

Address: 0xE00FFFF4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #1 Default Value: 16

6.1.64 CM0_ROM_CID2

CM0 CoreSight ROM Table Component ID #2

Address: 0xE00FFFF8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #2 Default Value: 5

6.1.65 CM0_ROM_CID3

CM0 CoreSight ROM Table Component ID #3

Address: 0xE00FFFFC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #3 Default Value: 177

7 Timer, Counter, PWM Counter (CNT) Registers

This section discusses the CNT registers. It lists all the registers in mapping tables, in address order.

7.1 Register Details

Register Name	Address
TCPWM_CNT0_CTRL	0x40200100
TCPWM_CNT0_STATUS	0x40200104
TCPWM_CNT0_COUNTER	0x40200108
TCPWM_CNT0_CC	0x4020010C
TCPWM_CNT0_CC_BUFF	0x40200110
TCPWM_CNT0_PERIOD	0x40200114
TCPWM_CNT0_PERIOD_BUFF	0x40200118
TCPWM_CNT0_TR_CTRL0	0x40200120
TCPWM_CNT0_TR_CTRL1	0x40200124
TCPWM_CNT0_TR_CTRL2	0x40200128
TCPWM_CNT0_INTR	0x40200130
TCPWM_CNT0_INTR_SET	0x40200134
TCPWM_CNT0_INTR_MASK	0x40200138
TCPWM_CNT0_INTR_MASKED	0x4020013C
TCPWM_CNT1_CTRL	0x40200140
TCPWM_CNT1_STATUS	0x40200144
TCPWM_CNT1_COUNTER	0x40200148
TCPWM_CNT1_CC	0x4020014C
TCPWM_CNT1_CC_BUFF	0x40200150
TCPWM_CNT1_PERIOD	0x40200154
TCPWM_CNT1_PERIOD_BUFF	0x40200158
TCPWM_CNT1_TR_CTRL0	0x40200160
TCPWM_CNT1_TR_CTRL1	0x40200164
TCPWM_CNT1_TR_CTRL2	0x40200168
TCPWM_CNT1_INTR	0x40200170
TCPWM_CNT1_INTR_SET	0x40200174

Register Name	Address
TCPWM_CNT1_INTR_MASK	0x40200178
TCPWM_CNT1_INTR_MASKED	0x4020017C
TCPWM_CNT2_CTRL	0x40200180
TCPWM_CNT2_STATUS	0x40200184
TCPWM_CNT2_COUNTER	0x40200188
TCPWM_CNT2_CC	0x4020018C
TCPWM_CNT2_CC_BUFF	0x40200190
TCPWM_CNT2_PERIOD	0x40200194
TCPWM_CNT2_PERIOD_BUFF	0x40200198
TCPWM_CNT2_TR_CTRL0	0x402001A0
TCPWM_CNT2_TR_CTRL1	0x402001A4
TCPWM_CNT2_TR_CTRL2	0x402001A8
TCPWM_CNT2_INTR	0x402001B0
TCPWM_CNT2_INTR_SET	0x402001B4
TCPWM_CNT2_INTR_MASK	0x402001B8
TCPWM_CNT2_INTR_MASKED	0x402001BC
TCPWM_CNT3_CTRL	0x402001C0
TCPWM_CNT3_STATUS	0x402001C4
TCPWM_CNT3_COUNTER	0x402001C8
TCPWM_CNT3_CC	0x402001CC
TCPWM_CNT3_CC_BUFF	0x402001D0
TCPWM_CNT3_PERIOD	0x402001D4
TCPWM_CNT3_PERIOD_BUFF	0x402001D8
TCPWM_CNT3_TR_CTRL0	0x402001E0
TCPWM_CNT3_TR_CTRL1	0x402001E4
TCPWM_CNT3_TR_CTRL2	0x402001E8
TCPWM_CNT3_INTR	0x402001F0
TCPWM_CNT3_INTR_SET	0x402001F4
TCPWM_CNT3_INTR_MASK	0x402001F8
TCPWM_CNT3_INTR_MASKED	0x402001FC

7.1.1 TCPWM_CNT0_CTRL

Counter control register

Address: 0x40200100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [7:4]				PWM_STOP_ON_KILL	PWM_SYNC_KILL	AUTO_RELOAD_PERIOD	AUTO_RELOAD_CC

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	GENERIC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW		None	RW	RW	
HW Access	None		R		None	R	R	
Name	None [23:22]		QUADRATURE_MODE [21:20]		None	ONE_SHOT	UP_DOWN_MODE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None					RW		
HW Access	None					R		
Name	None [31:27]					MODE [26:24]		

Bits	Name	Description
26 : 24	MODE	Counter mode. Default Value: 0 **0x0: TIMER:** Timer mode **0x2: CAPTURE:** Capture mode **0x3: QUAD:** Quadrature encoding mode **0x4: PWM:** Pulse width modulation (PWM) mode **0x5: PWM_DT:** PWM with deadtime insertion mode **0x6: PWM_PR:** Pseudo random pulse width modulation

(continued)

21 : 20	QUADRATURE_MODE	In QUAD mode selects quadrature encoding mode (X1/X2/X4). In PWM, PWM_DT and PWM_PR modes, these two bits can be used to invert "dt_line_out" and "dt_line_compl_out". Inversion is the last step in generation of "dt_line_out" and "dt_line_compl_out"; i.e. a disabled output line "dt_line_out" has the value QUADRATURE_MODE[0] and a disabled output line "dt_line_compl_out" has the value QUADRATURE_MODE[1]. Default Value: 0 **0x0: X1:** X1 encoding (QUAD mode) **0x1: X2:** X2 encoding (QUAD mode) **0x1: INV_OUT:** When bit 0 is '1', QUADRATURE_MODE[0] inverts "dt_line_out" (PWM/PWM_DT modes) **0x2: X4:** X4 encoding (QUAD mode) **0x2: INV_COMPL_OUT:** When bit 1 is '1', QUADRATURE_MODE[1] inverts "dt_line_compl_out" (PWM/PWM_DT modes)
18	ONE_SHOT	When '0', counter runs continuous. When '1', counter is turned off by hardware when a terminal count event is generated. Default Value: 0
17 : 16	UP_DOWN_MODE	Determines counter direction. Default Value: 0 **0x0: COUNT_UP:** Count up (to PERIOD). An overflow event is generated when the counter reaches PERIOD. A terminal count event is generated when the counter reaches PERIOD. **0x1: COUNT_DOWN:** Count down (to "0"). An underflow event is generated when the counter reaches "0". A terminal count event is generated when the counter reaches "0". **0x2: COUNT_UPDN1:** Count up (to PERIOD), then count down (to "0"). An overflow event is generated when the counter reaches PERIOD. An underflow event is generated when the counter reaches "0". A terminal count event is generated when the counter reaches "0". **0x3: COUNT_UPDN2:** Count up (to PERIOD), then count down (to "0"). An overflow event is generated when the counter reaches PERIOD. An underflow event is generated when the counter reaches "0". A terminal count event is generated when the counter reaches "0" AND when the counter reaches PERIOD (this counter direction can be used for PWM functionality with asymmetrical updates).
15 : 8	GENERIC	Generic 8-bit control field. In PWM_DT mode, this field is used to determine the dead time: amount of dead time cycles in the counter clock domain. In all other modes, the lower 3 bits of this field determine pre-scaling of the selected counter clock. Default Value: 0 **0x0: DIVBY1:** Divide by 1 (other-than-PWM_DT mode) **0x1: DIVBY2:** Divide by 2 (other-than-PWM_DT mode) **0x2: DIVBY4:** Divide by 4 (other-than-PWM_DT mode)

(continued)

		0x3: DIVBY8: Divide by 8 (other-than-PWM_DT mode) **0x4: DIVBY16:** Divide by 16 (other-than-PWM_DT mode) **0x5: DIVBY32:** Divide by 32 (other-than-PWM_DT mode) **0x6: DIVBY64:** Divide by 64 (other-than-PWM_DT mode) **0x7: DIVBY128:** Divide by 128 (other-than-PWM_DT mode)
3	PWM_STOP_ON_KILL	Specifies whether the counter stops on a kill events: '0': kill event does NOT stop counter. '1': kill event stops counter. This field has a function in PWM, PWM_DT and PWM_PR modes only. Default Value: 0
2	PWM_SYNC_KILL	Specifies asynchronous/synchronous kill behavior: '1': synchronous kill mode: the kill event disables the "dt_line_out" and "dt_line_compl_out" signals till the next terminal count event (synchronous kill). In synchronous kill mode, STOP_EDGE should be RISING_EDGE. '0': asynchronous kill mode: the kill event only disables the "dt_line_out" and "dt_line_compl_out" signals when present. In asynchronous kill mode, STOP_EDGE should be NO_EDGE_DET. This field has a function in PWM and PWM_DT modes only. This field is only used when PWM_STOP_ON_KILL is '0'. Default Value: 0
1	AUTO_RELOAD_PERIOD	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM, PWM_DT and PWM_PR modes. '0': never switch. '1': switch on a terminal count event with and actively pending siwtch event. Default Value: 0
0	AUTO_RELOAD_CC	Specifies switching of the CC and buffered CC values. This field has a function in TIMER, PWM, PWM_DT and PWM_PR modes. Timer mode: '0': never switch. '1': switch on a compare match event. PWM, PWM_DT, PWM_PR modes: '0: never switch. '1': switch on a terminal count event with an actively pending switch event. Default Value: 0

7.1.2 TCPWM_CNT0_STATUS

Counter status register

Address: 0x40200104

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							DOWN

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	GENERIC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	RW	None						
Name	RUNNING	None [30:24]						

Bits	Name	Description
31	RUNNING	When '0', the counter is NOT running. When '1', the counter is running. Default Value: 0
15 : 8	GENERIC	Generic 8-bit counter field. In PWM_DT mode, this counter is used for dead time insertion. In all other modes, this counter is used for pre-scaling the selected counter clock. PWM_DT mode can NOT use prescaled clock functionality. Default Value: 0
0	DOWN	When '0', counter is counting up. When '1', counter is counting down. In QUAD mode, this field indicates the direction of the latest counter change: '0' when last incremented and '1' when last decremented. Default Value: 0

7.1.3 TCPWM_CNT0_COUNTER

Counter count register

Address: 0x40200108

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	COUNTER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	COUNTER [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	COUNTER	16-bit counter value. It is advised to not write to this field when the counter is running. Default Value: 0

7.1.4 TCPWM_CNT0_CC

Counter compare/capture register

Address: 0x4020010C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CC	In CAPTURE mode, captures the counter value. In other modes, compared to counter value. Default Value: 65535

7.1.5 TCPWM_CNT0_CC_BUFF

Counter buffered compare/capture register

Address: 0x40200110

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CC	Additional buffer for counter CC register. Default Value: 65535

7.1.6 TCPWM_CNT0_PERIOD

Counter period register

Address: 0x40200114

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	PERIOD	Period value: upper value of the counter. When the counter should count for n cycles, this field should be set to n-1. Default Value: 65535

7.1.7 TCPWM_CNT0_PERIOD_BUFF

Counter buffered period register

Address: 0x40200118

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	PERIOD	Additional buffer for counter PERIOD register. Default Value: 65535

7.1.8 TCPWM_CNT0_TR_CTRL0

Counter trigger control register 0

Address: 0x40200120

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	COUNT_SEL [7:4]				CAPTURE_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	STOP_SEL [15:12]				RELOAD_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				START_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	START_SEL	Selects one of the 16 input triggers as a start trigger. In QUAD mode, this is the second phase (phi B). Default Value: 0
15 : 12	STOP_SEL	Selects one of the 16 input triggers as a stop trigger. In PWM, PWM_DT and PWM_PR modes, this is the kill trigger. In these modes, the kill trigger is used to either temporarily block the PWM outputs (PWM_STOP_ON_KILL is '0') or stop the functionality (PWM_STOP_ON_KILL is '1'). For the PWM and PWM_DT modes, the blocking of the output signals can be asynchronous (STOP_EDGE should be NO_EDGE_DET) in which case the blocking is as long as the trigger is '1' or synchronous (STOP_EDGE should be RISING_EDGE) in which case it extends till the next terminal count event. Default Value: 0
11 : 8	RELOAD_SEL	Selects one of the 16 input triggers as a reload trigger. In QUAD mode, this is the index or revolution pulse. In this mode, it will update the counter with the value in the TCPWM_CNTn_PERIOD register. Default Value: 0
7 : 4	COUNT_SEL	Selects one of the 16 input triggers as a count trigger. In QUAD mode, this is the first phase (phi A). Default setting selects input trigger 1, which is always '1'. Default Value: 1

(continued)

3 : 0	CAPTURE_SEL	Selects one of the 16 input triggers as a capture trigger. Input trigger 0 is always '0' and input trigger is always '1'. In the PWM, PWM_DT and PWM_PR modes this trigger is used to switch the values if the compare and period registers with their buffer counterparts. Default Value: 0

7.1.9 TCPWM_CNT0_TR_CTRL1

Counter trigger control register 1

Address: 0x40200124

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	STOP_EDGE [7:6]		RELOAD_EDGE [5:4]		COUNT_EDGE [3:2]		CAPTURE_EDGE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						START_EDGE [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 8	START_EDGE	A start event will start the counter; i.e. the counter will become running. Starting does NOT enable the counter. A start event will not initialize the counter whereas the reload event does. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE:** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.
7 : 6	STOP_EDGE	A stop event, will stop the counter; i.e. it will no longer be running. Stopping will NOT disable the counter. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event.

(continued)

		0x1: FALLING_EDGE: Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.
5 : 4	RELOAD_EDGE	A reload event will initialize the counter. When counting up, the counter is initialized to "0". When counting down, the counter is initialized with PERIOD. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE:** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.
3 : 2	COUNT_EDGE	A counter event will increase or decrease the counter by '1'. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE:** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.
1 : 0	CAPTURE_EDGE	A capture event will copy the counter value into the CC register. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE:** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.

7.1.10 TCPWM_CNT0_TR_CTRL2

Counter trigger control register 2

Address: 0x40200128

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW		RW		RW	
HW Access	None		R		R		R	
Name	None [7:6]		UNDERFLOW_MODE [5:4]		OVERFLOW_MODE [3:2]		CC_MATCH_MODE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 4	UNDERFLOW_MODE	Determines the effect of a counter underflow event (COUNTER reaches "0") on the "line_out" output signals. Default Value: 3 **0x0: SET:** Set to '1' **0x1: CLEAR:** Set to '0' **0x2: INVERT:** Invert **0x3: NO_CHANGE:** No Change
3 : 2	OVERFLOW_MODE	Determines the effect of a counter overflow event (COUNTER reaches PERIOD) on the "line_out" output signals. Default Value: 3 **0x0: SET:** Set to '1'

(continued)

		0x1: CLEAR: Set to '0' **0x2: INVERT:** Invert **0x3: NO_CHANGE:** No Change
1 : 0	CC_MATCH_MODE	Determines the effect of a compare match event (COUNTER equals CC register) on the "line_out" output signals. Note that INVERT is especially useful for center aligned pulse width modulation. To generate a duty cycle of 0%, the counter CC register should be set to "0". For a 100% duty cycle, the counter CC register should be set to larger than the counter PERIOD register. Default Value: 3 **0x0: SET:** Set to '1' **0x1: CLEAR:** Set to '0' **0x2: INVERT:** Invert **0x3: NO_CHANGE:** No Change

7.1.11 TCPWM_CNT0_INTR

Interrupt request register.

Address: 0x40200130

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1C	RW1C
HW Access	None						RW1S	RW1S
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Counter matches CC register event. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
0	TC	Terminal count event. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0

7.1.12 TCPWM_CNT0_INTR_SET

Interrupt set request register.

Address: 0x40200134

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1S	RW1S
HW Access	None						A	A
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	TC	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

7.1.13 TCPWM_CNT0_INTR_MASK

Interrupt mask register.

Address: 0x40200138

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	TC	Mask bit for corresponding bit in interrupt request register. Default Value: 0

7.1.14 TCPWM_CNT0_INTR_MASKED

Interrupt masked request register

Address: 0x4020013C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						W	W
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Logical and of corresponding request and mask bits. Default Value: 0
0	TC	Logical and of corresponding request and mask bits. Default Value: 0

7.1.15 TCPWM_CNT1_CTRL

Counter control register

Address: 0x40200140

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [7:4]				PWM_STOP_ON_KILL	PWM_SYNC_KILL	AUTO_RELOAD_PERIOD	AUTO_RELOAD_CC

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	GENERIC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW		None	RW	RW	
HW Access	None		R		None	R	R	
Name	None [23:22]		QUADRATURE_MODE [21:20]		None	ONE_SHOT	UP_DOWN_MODE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None					RW		
HW Access	None					R		
Name	None [31:27]					MODE [26:24]		

Bits	Name	Description
26 : 24	MODE	Counter mode. Default Value: 0 **0x0: TIMER:** Timer mode **0x2: CAPTURE:** Capture mode **0x3: QUAD:** Quadrature encoding mode **0x4: PWM:** Pulse width modulation (PWM) mode **0x5: PWM_DT:** PWM with deadtime insertion mode **0x6: PWM_PR:** Pseudo random pulse width modulation

(continued)

21 : 20	QUADRATURE_MODE	In QUAD mode selects quadrature encoding mode (X1/X2/X4). In PWM, PWM_DT and PWM_PR modes, these two bits can be used to invert "dt_line_out" and "dt_line_compl_out". Inversion is the last step in generation of "dt_line_out" and "dt_line_compl_out"; i.e. a disabled output line "dt_line_out" has the value QUADRATURE_MODE[0] and a disabled output line "dt_line_compl_out" has the value QUADRATURE_MODE[1]. Default Value: 0 **0x0: X1:** X1 encoding (QUAD mode) **0x1: X2:** X2 encoding (QUAD mode) **0x1: INV_OUT:** When bit 0 is '1', QUADRATURE_MODE[0] inverts "dt_line_out" (PWM/PWM_DT modes) **0x2: X4:** X4 encoding (QUAD mode) **0x2: INV_COMPL_OUT:** When bit 1 is '1', QUADRATURE_MODE[1] inverts "dt_line_compl_out" (PWM/PWM_DT modes)
18	ONE_SHOT	When '0', counter runs continuous. When '1', counter is turned off by hardware when a terminal count event is generated. Default Value: 0
17 : 16	UP_DOWN_MODE	Determines counter direction. Default Value: 0 **0x0: COUNT_UP:** Count up (to PERIOD). An overflow event is generated when the counter reaches PERIOD. A terminal count event is generated when the counter reaches PERIOD. **0x1: COUNT_DOWN:** Count down (to "0"). An underflow event is generated when the counter reaches "0". A terminal count event is generated when the counter reaches "0". **0x2: COUNT_UPDN1:** Count up (to PERIOD), then count down (to "0"). An overflow event is generated when the counter reaches PERIOD. An underflow event is generated when the counter reaches "0". A terminal count event is generated when the counter reaches "0". **0x3: COUNT_UPDN2:** Count up (to PERIOD), then count down (to "0"). An overflow event is generated when the counter reaches PERIOD. An underflow event is generated when the counter reaches "0". A terminal count event is generated when the counter reaches "0" AND when the counter reaches PERIOD (this counter direction can be used for PWM functionality with asymmetrical updates).
15 : 8	GENERIC	Generic 8-bit control field. In PWM_DT mode, this field is used to determine the dead time: amount of dead time cycles in the counter clock domain. In all other modes, the lower 3 bits of this field determine pre-scaling of the selected counter clock. Default Value: 0 **0x0: DIVBY1:** Divide by 1 (other-than-PWM_DT mode) **0x1: DIVBY2:** Divide by 2 (other-than-PWM_DT mode) **0x2: DIVBY4:** Divide by 4 (other-than-PWM_DT mode)

(continued)

		0x3: DIVBY8: Divide by 8 (other-than-PWM_DT mode) **0x4: DIVBY16:** Divide by 16 (other-than-PWM_DT mode) **0x5: DIVBY32:** Divide by 32 (other-than-PWM_DT mode) **0x6: DIVBY64:** Divide by 64 (other-than-PWM_DT mode) **0x7: DIVBY128:** Divide by 128 (other-than-PWM_DT mode)
3	PWM_STOP_ON_KILL	Specifies whether the counter stops on a kill events: '0': kill event does NOT stop counter. '1': kill event stops counter. This field has a function in PWM, PWM_DT and PWM_PR modes only. Default Value: 0
2	PWM_SYNC_KILL	Specifies asynchronous/synchronous kill behavior: '1': synchronous kill mode: the kill event disables the "dt_line_out" and "dt_line_compl_out" signals till the next terminal count event (synchronous kill). In synchronous kill mode, STOP_EDGE should be RISING_EDGE. '0': asynchronous kill mode: the kill event only disables the "dt_line_out" and "dt_line_compl_out" signals when present. In asynchronous kill mode, STOP_EDGE should be NO_EDGE_DET. This field has a function in PWM and PWM_DT modes only. This field is only used when PWM_STOP_ON_KILL is '0'. Default Value: 0
1	AUTO_RELOAD_PERIOD	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM, PWM_DT and PWM_PR modes. '0': never switch. '1': switch on a terminal count event with and actively pending siwtch event. Default Value: 0
0	AUTO_RELOAD_CC	Specifies switching of the CC and buffered CC values. This field has a function in TIMER, PWM, PWM_DT and PWM_PR modes. Timer mode: '0': never switch. '1': switch on a compare match event. PWM, PWM_DT, PWM_PR modes: '0: never switch. '1': switch on a terminal count event with an actively pending switch event. Default Value: 0

7.1.16 TCPWM_CNT1_STATUS

Counter status register

Address: 0x40200144

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							DOWN

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	GENERIC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	RW	None						
Name	RUNNING	None [30:24]						

Bits	Name	Description
31	RUNNING	When '0', the counter is NOT running. When '1', the counter is running. Default Value: 0
15 : 8	GENERIC	Generic 8-bit counter field. In PWM_DT mode, this counter is used for dead time insertion. In all other modes, this counter is used for pre-scaling the selected counter clock. PWM_DT mode can NOT use prescaled clock functionality. Default Value: 0
0	DOWN	When '0', counter is counting up. When '1', counter is counting down. In QUAD mode, this field indicates the direction of the latest counter change: '0' when last incremented and '1' when last decremented. Default Value: 0

7.1.17 TCPWM_CNT1_COUNTER

Counter count register

Address: 0x40200148

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	COUNTER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	COUNTER [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	COUNTER	16-bit counter value. It is advised to not write to this field when the counter is running. Default Value: 0

7.1.18 TCPWM_CNT1_CC

Counter compare/capture register

Address: 0x4020014C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CC	In CAPTURE mode, captures the counter value. In other modes, compared to counter value. Default Value: 65535

7.1.19 TCPWM_CNT1_CC_BUFF

Counter buffered compare/capture register

Address: 0x40200150

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CC	Additional buffer for counter CC register. Default Value: 65535

7.1.20 TCPWM_CNT1_PERIOD

Counter period register

Address: 0x40200154

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	PERIOD	Period value: upper value of the counter. When the counter should count for n cycles, this field should be set to n-1. Default Value: 65535

7.1.21 TCPWM_CNT1_PERIOD_BUFF

Counter buffered period register

Address: 0x40200158

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	PERIOD	Additional buffer for counter PERIOD register. Default Value: 65535

7.1.22 TCPWM_CNT1_TR_CTRL0

Counter trigger control register 0

Address: 0x40200160

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	COUNT_SEL [7:4]				CAPTURE_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	STOP_SEL [15:12]				RELOAD_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				START_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	START_SEL	Selects one of the 16 input triggers as a start trigger. In QUAD mode, this is the second phase (phi B). Default Value: 0
15 : 12	STOP_SEL	Selects one of the 16 input triggers as a stop trigger. In PWM, PWM_DT and PWM_PR modes, this is the kill trigger. In these modes, the kill trigger is used to either temporarily block the PWM outputs (PWM_STOP_ON_KILL is '0') or stop the functionality (PWM_STOP_ON_KILL is '1'). For the PWM and PWM_DT modes, the blocking of the output signals can be asynchronous (STOP_EDGE should be NO_EDGE_DET) in which case the blocking is as long as the trigger is '1' or synchronous (STOP_EDGE should be RISING_EDGE) in which case it extends till the next terminal count event. Default Value: 0
11 : 8	RELOAD_SEL	Selects one of the 16 input triggers as a reload trigger. In QUAD mode, this is the index or revolution pulse. In this mode, it will update the counter with the value in the TCPWM_CNTn_PERIOD register. Default Value: 0
7 : 4	COUNT_SEL	Selects one of the 16 input triggers as a count trigger. In QUAD mode, this is the first phase (phi A). Default setting selects input trigger 1, which is always '1'. Default Value: 1

(continued)

3 : 0	CAPTURE_SEL	Selects one of the 16 input triggers as a capture trigger. Input trigger 0 is always '0' and input trigger is always '1'. In the PWM, PWM_DT and PWM_PR modes this trigger is used to switch the values if the compare and period registers with their buffer counterparts. Default Value: 0

7.1.23 TCPWM_CNT1_TR_CTRL1

Counter trigger control register 1

Address: 0x40200164

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	STOP_EDGE [7:6]		RELOAD_EDGE [5:4]		COUNT_EDGE [3:2]		CAPTURE_EDGE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						START_EDGE [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 8	START_EDGE	A start event will start the counter; i.e. the counter will become running. Starting does NOT enable the counter. A start event will not initialize the counter whereas the reload event does. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE:** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.
7 : 6	STOP_EDGE	A stop event, will stop the counter; i.e. it will no longer be running. Stopping will NOT disable the counter. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event.

(continued)

		0x1: FALLING_EDGE: Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.
5 : 4	RELOAD_EDGE	A reload event will initialize the counter. When counting up, the counter is initialized to "0". When counting down, the counter is initialized with PERIOD. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE:** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.
3 : 2	COUNT_EDGE	A counter event will increase or decrease the counter by '1'. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE:** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.
1 : 0	CAPTURE_EDGE	A capture event will copy the counter value into the CC register. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE:** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.

7.1.24 TCPWM_CNT1_TR_CTRL2

Counter trigger control register 2

Address: 0x40200168

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW		RW		RW	
HW Access	None		R		R		R	
Name	None [7:6]		UNDERFLOW_MODE [5:4]		OVERFLOW_MODE [3:2]		CC_MATCH_MODE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 4	UNDERFLOW_MODE	Determines the effect of a counter underflow event (COUNTER reaches "0") on the "line_out" output signals. Default Value: 3 **0x0: SET:** Set to '1' **0x1: CLEAR:** Set to '0' **0x2: INVERT:** Invert **0x3: NO_CHANGE:** No Change
3 : 2	OVERFLOW_MODE	Determines the effect of a counter overflow event (COUNTER reaches PERIOD) on the "line_out" output signals. Default Value: 3 **0x0: SET:** Set to '1'

(continued)

		0x1: CLEAR: Set to '0' **0x2: INVERT:** Invert **0x3: NO_CHANGE:** No Change
1 : 0	CC_MATCH_MODE	Determines the effect of a compare match event (COUNTER equals CC register) on the "line_out" output signals. Note that INVERT is especially useful for center aligned pulse width modulation. To generate a duty cycle of 0%, the counter CC register should be set to "0". For a 100% duty cycle, the counter CC register should be set to larger than the counter PERIOD register. Default Value: 3 **0x0: SET:** Set to '1' **0x1: CLEAR:** Set to '0' **0x2: INVERT:** Invert **0x3: NO_CHANGE:** No Change

7.1.25 TCPWM_CNT1_INTR

Interrupt request register.

Address: 0x40200170

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1C	RW1C
HW Access	None						RW1S	RW1S
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Counter matches CC register event. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
0	TC	Terminal count event. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0

7.1.26 TCPWM_CNT1_INTR_SET

Interrupt set request register.

Address: 0x40200174

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1S	RW1S
HW Access	None						A	A
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	TC	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

7.1.27 TCPWM_CNT1_INTR_MASK

Interrupt mask register.

Address: 0x40200178

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	TC	Mask bit for corresponding bit in interrupt request register. Default Value: 0

7.1.28 TCPWM_CNT1_INTR_MASKED

Interrupt masked request register

Address: 0x4020017C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						W	W
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Logical and of corresponding request and mask bits. Default Value: 0
0	TC	Logical and of corresponding request and mask bits. Default Value: 0

7.1.29 TCPWM_CNT2_CTRL

Counter control register

Address: 0x40200180

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [7:4]				PWM_STOP_ON_KILL	PWM_SYNC_KILL	AUTO_RELOAD_PERIOD	AUTO_RELOAD_CC

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	GENERIC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW		None	RW	RW	
HW Access	None		R		None	R	R	
Name	None [23:22]		QUADRATURE_MODE [21:20]		None	ONE_SHOT	UP_DOWN_MODE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None					RW		
HW Access	None					R		
Name	None [31:27]					MODE [26:24]		

Bits	Name	Description
26 : 24	MODE	Counter mode. Default Value: 0 **0x0: TIMER:** Timer mode **0x2: CAPTURE:** Capture mode **0x3: QUAD:** Quadrature encoding mode **0x4: PWM:** Pulse width modulation (PWM) mode **0x5: PWM_DT:** PWM with deadtime insertion mode **0x6: PWM_PR:** Pseudo random pulse width modulation

(continued)

21 : 20	QUADRATURE_MODE	In QUAD mode selects quadrature encoding mode (X1/X2/X4). In PWM, PWM_DT and PWM_PR modes, these two bits can be used to invert "dt_line_out" and "dt_line_compl_out". Inversion is the last step in generation of "dt_line_out" and "dt_line_compl_out"; i.e. a disabled output line "dt_line_out" has the value QUADRATURE_MODE[0] and a disabled output line "dt_line_compl_out" has the value QUADRATURE_MODE[1]. Default Value: 0 **0x0: X1:** X1 encoding (QUAD mode) **0x1: X2:** X2 encoding (QUAD mode) **0x1: INV_OUT:** When bit 0 is '1', QUADRATURE_MODE[0] inverts "dt_line_out" (PWM/PWM_DT modes) **0x2: X4:** X4 encoding (QUAD mode) **0x2: INV_COMPL_OUT:** When bit 1 is '1', QUADRATURE_MODE[1] inverts "dt_line_compl_out" (PWM/PWM_DT modes)
18	ONE_SHOT	When '0', counter runs continuous. When '1', counter is turned off by hardware when a terminal count event is generated. Default Value: 0
17 : 16	UP_DOWN_MODE	Determines counter direction. Default Value: 0 **0x0: COUNT_UP:** Count up (to PERIOD). An overflow event is generated when the counter reaches PERIOD. A terminal count event is generated when the counter reaches PERIOD. **0x1: COUNT_DOWN:** Count down (to "0"). An underflow event is generated when the counter reaches "0". A terminal count event is generated when the counter reaches "0". **0x2: COUNT_UPDN1:** Count up (to PERIOD), then count down (to "0"). An overflow event is generated when the counter reaches PERIOD. An underflow event is generated when the counter reaches "0". A terminal count event is generated when the counter reaches "0". **0x3: COUNT_UPDN2:** Count up (to PERIOD), then count down (to "0"). An overflow event is generated when the counter reaches PERIOD. An underflow event is generated when the counter reaches "0". A terminal count event is generated when the counter reaches "0" AND when the counter reaches PERIOD (this counter direction can be used for PWM functionality with asymmetrical updates).
15 : 8	GENERIC	Generic 8-bit control field. In PWM_DT mode, this field is used to determine the dead time: amount of dead time cycles in the counter clock domain. In all other modes, the lower 3 bits of this field determine pre-scaling of the selected counter clock. Default Value: 0 **0x0: DIVBY1:** Divide by 1 (other-than-PWM_DT mode) **0x1: DIVBY2:** Divide by 2 (other-than-PWM_DT mode) **0x2: DIVBY4:** Divide by 4 (other-than-PWM_DT mode)

(continued)

		0x3: DIVBY8: Divide by 8 (other-than-PWM_DT mode) **0x4: DIVBY16:** Divide by 16 (other-than-PWM_DT mode) **0x5: DIVBY32:** Divide by 32 (other-than-PWM_DT mode) **0x6: DIVBY64:** Divide by 64 (other-than-PWM_DT mode) **0x7: DIVBY128:** Divide by 128 (other-than-PWM_DT mode)
3	PWM_STOP_ON_KILL	Specifies whether the counter stops on a kill events: '0': kill event does NOT stop counter. '1': kill event stops counter. This field has a function in PWM, PWM_DT and PWM_PR modes only. Default Value: 0
2	PWM_SYNC_KILL	Specifies asynchronous/synchronous kill behavior: '1': synchronous kill mode: the kill event disables the "dt_line_out" and "dt_line_compl_out" signals till the next terminal count event (synchronous kill). In synchronous kill mode, STOP_EDGE should be RISING_EDGE. '0': asynchronous kill mode: the kill event only disables the "dt_line_out" and "dt_line_compl_out" signals when present. In asynchronous kill mode, STOP_EDGE should be NO_EDGE_DET. This field has a function in PWM and PWM_DT modes only. This field is only used when PWM_STOP_ON_KILL is '0'. Default Value: 0
1	AUTO_RELOAD_PERIOD	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM, PWM_DT and PWM_PR modes. '0': never switch. '1': switch on a terminal count event with and actively pending siwtch event. Default Value: 0
0	AUTO_RELOAD_CC	Specifies switching of the CC and buffered CC values. This field has a function in TIMER, PWM, PWM_DT and PWM_PR modes. Timer mode: '0': never switch. '1': switch on a compare match event. PWM, PWM_DT, PWM_PR modes: '0: never switch. '1': switch on a terminal count event with an actively pending switch event. Default Value: 0

7.1.30 TCPWM_CNT2_STATUS

Counter status register

Address: 0x40200184

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							DOWN

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	GENERIC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	RW	None						
Name	RUNNING	None [30:24]						

Bits	Name	Description
31	RUNNING	When '0', the counter is NOT running. When '1', the counter is running. Default Value: 0
15 : 8	GENERIC	Generic 8-bit counter field. In PWM_DT mode, this counter is used for dead time insertion. In all other modes, this counter is used for pre-scaling the selected counter clock. PWM_DT mode can NOT use prescaled clock functionality. Default Value: 0
0	DOWN	When '0', counter is counting up. When '1', counter is counting down. In QUAD mode, this field indicates the direction of the latest counter change: '0' when last incremented and '1' when last decremented. Default Value: 0

7.1.31 TCPWM_CNT2_COUNTER

Counter count register

Address: 0x40200188

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	COUNTER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	COUNTER [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	COUNTER	16-bit counter value. It is advised to not write to this field when the counter is running. Default Value: 0

7.1.32 TCPWM_CNT2_CC

Counter compare/capture register

Address: 0x4020018C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CC	In CAPTURE mode, captures the counter value. In other modes, compared to counter value. Default Value: 65535

7.1.33 TCPWM_CNT2_CC_BUFF

Counter buffered compare/capture register

Address: 0x40200190

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CC	Additional buffer for counter CC register. Default Value: 65535

7.1.34 TCPWM_CNT2_PERIOD

Counter period register

Address: 0x40200194

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	PERIOD	Period value: upper value of the counter. When the counter should count for n cycles, this field should be set to n-1. Default Value: 65535

7.1.35 TCPWM_CNT2_PERIOD_BUFF

Counter buffered period register

Address: 0x40200198

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	PERIOD	Additional buffer for counter PERIOD register. Default Value: 65535

7.1.36 TCPWM_CNT2_TR_CTRL0

Counter trigger control register 0

Address: 0x402001A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	COUNT_SEL [7:4]				CAPTURE_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	STOP_SEL [15:12]				RELOAD_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				START_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	START_SEL	Selects one of the 16 input triggers as a start trigger. In QUAD mode, this is the second phase (phi B). Default Value: 0
15 : 12	STOP_SEL	Selects one of the 16 input triggers as a stop trigger. In PWM, PWM_DT and PWM_PR modes, this is the kill trigger. In these modes, the kill trigger is used to either temporarily block the PWM outputs (PWM_STOP_ON_KILL is '0') or stop the functionality (PWM_STOP_ON_KILL is '1'). For the PWM and PWM_DT modes, the blocking of the output signals can be asynchronous (STOP_EDGE should be NO_EDGE_DET) in which case the blocking is as long as the trigger is '1' or synchronous (STOP_EDGE should be RISING_EDGE) in which case it extends till the next terminal count event. Default Value: 0
11 : 8	RELOAD_SEL	Selects one of the 16 input triggers as a reload trigger. In QUAD mode, this is the index or revolution pulse. In this mode, it will update the counter with the value in the TCPWM_CNTn_PERIOD register. Default Value: 0
7 : 4	COUNT_SEL	Selects one of the 16 input triggers as a count trigger. In QUAD mode, this is the first phase (phi A). Default setting selects input trigger 1, which is always '1'. Default Value: 1

(continued)

3 : 0	CAPTURE_SEL	Selects one of the 16 input triggers as a capture trigger. Input trigger 0 is always '0' and input trigger is always '1'. In the PWM, PWM_DT and PWM_PR modes this trigger is used to switch the values if the compare and period registers with their buffer counterparts. Default Value: 0

7.1.37 TCPWM_CNT2_TR_CTRL1

Counter trigger control register 1

Address: 0x402001A4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	STOP_EDGE [7:6]		RELOAD_EDGE [5:4]		COUNT_EDGE [3:2]		CAPTURE_EDGE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						START_EDGE [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 8	START_EDGE	A start event will start the counter; i.e. the counter will become running. Starting does NOT enable the counter. A start event will not initialize the counter whereas the reload event does. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE:** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.
7 : 6	STOP_EDGE	A stop event, will stop the counter; i.e. it will no longer be running. Stopping will NOT disable the counter. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event.

(continued)

		0x1: FALLING_EDGE: Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.
5 : 4	RELOAD_EDGE	A reload event will initialize the counter. When counting up, the counter is initialized to "0". When counting down, the counter is initialized with PERIOD. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE:** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.
3 : 2	COUNT_EDGE	A counter event will increase or decrease the counter by '1'. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE:** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.
1 : 0	CAPTURE_EDGE	A capture event will copy the counter value into the CC register. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE:** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.

7.1.38 TCPWM_CNT2_TR_CTRL2

Counter trigger control register 2

Address: 0x402001A8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW		RW		RW	
HW Access	None		R		R		R	
Name	None [7:6]		UNDERFLOW_MODE [5:4]		OVERFLOW_MODE [3:2]		CC_MATCH_MODE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 4	UNDERFLOW_MODE	Determines the effect of a counter underflow event (COUNTER reaches "0") on the "line_out" output signals. Default Value: 3 **0x0: SET:** Set to '1' **0x1: CLEAR:** Set to '0' **0x2: INVERT:** Invert **0x3: NO_CHANGE:** No Change
3 : 2	OVERFLOW_MODE	Determines the effect of a counter overflow event (COUNTER reaches PERIOD) on the "line_out" output signals. Default Value: 3 **0x0: SET:** Set to '1'

(continued)

		0x1: CLEAR: Set to '0' **0x2: INVERT:** Invert **0x3: NO_CHANGE:** No Change
1 : 0	CC_MATCH_MODE	Determines the effect of a compare match event (COUNTER equals CC register) on the "line_out" output signals. Note that INVERT is especially useful for center aligned pulse width modulation. To generate a duty cycle of 0%, the counter CC register should be set to "0". For a 100% duty cycle, the counter CC register should be set to larger than the counter PERIOD register. Default Value: 3 **0x0: SET:** Set to '1' **0x1: CLEAR:** Set to '0' **0x2: INVERT:** Invert **0x3: NO_CHANGE:** No Change

7.1.39 TCPWM_CNT2_INTR

Interrupt request register.

Address: 0x402001B0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1C	RW1C
HW Access	None						RW1S	RW1S
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Counter matches CC register event. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
0	TC	Terminal count event. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0

7.1.40 TCPWM_CNT2_INTR_SET

Interrupt set request register.

Address: 0x402001B4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1S	RW1S
HW Access	None						A	A
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	TC	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

7.1.41 TCPWM_CNT2_INTR_MASK

Interrupt mask register.

Address: 0x402001B8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	TC	Mask bit for corresponding bit in interrupt request register. Default Value: 0

7.1.42 TCPWM_CNT2_INTR_MASKED

Interrupt masked request register

Address: 0x402001BC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						W	W
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Logical and of corresponding request and mask bits. Default Value: 0
0	TC	Logical and of corresponding request and mask bits. Default Value: 0

7.1.43 TCPWM_CNT3_CTRL

Counter control register

Address: 0x402001C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [7:4]				PWM_STOP_ON_KILL	PWM_SYNC_KILL	AUTO_RELOAD_PERIOD	AUTO_RELOAD_CC

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	GENERIC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW		None	RW	RW	
HW Access	None		R		None	R	R	
Name	None [23:22]		QUADRATURE_MODE [21:20]		None	ONE_SHOT	UP_DOWN_MODE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None					RW		
HW Access	None					R		
Name	None [31:27]					MODE [26:24]		

Bits	Name	Description
26 : 24	MODE	Counter mode. Default Value: 0 **0x0: TIMER:** Timer mode **0x2: CAPTURE:** Capture mode **0x3: QUAD:** Quadrature encoding mode **0x4: PWM:** Pulse width modulation (PWM) mode **0x5: PWM_DT:** PWM with deadtime insertion mode **0x6: PWM_PR:** Pseudo random pulse width modulation

(continued)

21 : 20	QUADRATURE_MODE	In QUAD mode selects quadrature encoding mode (X1/X2/X4). In PWM, PWM_DT and PWM_PR modes, these two bits can be used to invert "dt_line_out" and "dt_line_compl_out". Inversion is the last step in generation of "dt_line_out" and "dt_line_compl_out"; i.e. a disabled output line "dt_line_out" has the value QUADRATURE_MODE[0] and a disabled output line "dt_line_compl_out" has the value QUADRATURE_MODE[1]. Default Value: 0 **0x0: X1:** X1 encoding (QUAD mode) **0x1: X2:** X2 encoding (QUAD mode) **0x1: INV_OUT:** When bit 0 is '1', QUADRATURE_MODE[0] inverts "dt_line_out" (PWM/PWM_DT modes) **0x2: X4:** X4 encoding (QUAD mode) **0x2: INV_COMPL_OUT:** When bit 1 is '1', QUADRATURE_MODE[1] inverts "dt_line_compl_out" (PWM/PWM_DT modes)
18	ONE_SHOT	When '0', counter runs continuous. When '1', counter is turned off by hardware when a terminal count event is generated. Default Value: 0
17 : 16	UP_DOWN_MODE	Determines counter direction. Default Value: 0 **0x0: COUNT_UP:** Count up (to PERIOD). An overflow event is generated when the counter reaches PERIOD. A terminal count event is generated when the counter reaches PERIOD. **0x1: COUNT_DOWN:** Count down (to "0"). An underflow event is generated when the counter reaches "0". A terminal count event is generated when the counter reaches "0". **0x2: COUNT_UPDN1:** Count up (to PERIOD), then count down (to "0"). An overflow event is generated when the counter reaches PERIOD. An underflow event is generated when the counter reaches "0". A terminal count event is generated when the counter reaches "0". **0x3: COUNT_UPDN2:** Count up (to PERIOD), then count down (to "0"). An overflow event is generated when the counter reaches PERIOD. An underflow event is generated when the counter reaches "0". A terminal count event is generated when the counter reaches "0" AND when the counter reaches PERIOD (this counter direction can be used for PWM functionality with asymmetrical updates).
15 : 8	GENERIC	Generic 8-bit control field. In PWM_DT mode, this field is used to determine the dead time: amount of dead time cycles in the counter clock domain. In all other modes, the lower 3 bits of this field determine pre-scaling of the selected counter clock. Default Value: 0 **0x0: DIVBY1:** Divide by 1 (other-than-PWM_DT mode) **0x1: DIVBY2:** Divide by 2 (other-than-PWM_DT mode) **0x2: DIVBY4:** Divide by 4 (other-than-PWM_DT mode)

(continued)

		0x3: DIVBY8: Divide by 8 (other-than-PWM_DT mode) **0x4: DIVBY16:** Divide by 16 (other-than-PWM_DT mode) **0x5: DIVBY32:** Divide by 32 (other-than-PWM_DT mode) **0x6: DIVBY64:** Divide by 64 (other-than-PWM_DT mode) **0x7: DIVBY128:** Divide by 128 (other-than-PWM_DT mode)
3	PWM_STOP_ON_KILL	Specifies whether the counter stops on a kill events: '0': kill event does NOT stop counter. '1': kill event stops counter. This field has a function in PWM, PWM_DT and PWM_PR modes only. Default Value: 0
2	PWM_SYNC_KILL	Specifies asynchronous/synchronous kill behavior: '1': synchronous kill mode: the kill event disables the "dt_line_out" and "dt_line_compl_out" signals till the next terminal count event (synchronous kill). In synchronous kill mode, STOP_EDGE should be RISING_EDGE. '0': asynchronous kill mode: the kill event only disables the "dt_line_out" and "dt_line_compl_out" signals when present. In asynchronous kill mode, STOP_EDGE should be NO_EDGE_DET. This field has a function in PWM and PWM_DT modes only. This field is only used when PWM_STOP_ON_KILL is '0'. Default Value: 0
1	AUTO_RELOAD_PERIOD	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM, PWM_DT and PWM_PR modes. '0': never switch. '1': switch on a terminal count event with and actively pending siwtch event. Default Value: 0
0	AUTO_RELOAD_CC	Specifies switching of the CC and buffered CC values. This field has a function in TIMER, PWM, PWM_DT and PWM_PR modes. Timer mode: '0': never switch. '1': switch on a compare match event. PWM, PWM_DT, PWM_PR modes: '0: never switch. '1': switch on a terminal count event with an actively pending switch event. Default Value: 0

7.1.44 TCPWM_CNT3_STATUS

Counter status register

Address: 0x402001C4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							DOWN

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	GENERIC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	RW	None						
Name	RUNNING	None [30:24]						

Bits	Name	Description
31	RUNNING	When '0', the counter is NOT running. When '1', the counter is running. Default Value: 0
15 : 8	GENERIC	Generic 8-bit counter field. In PWM_DT mode, this counter is used for dead time insertion. In all other modes, this counter is used for pre-scaling the selected counter clock. PWM_DT mode can NOT use prescaled clock functionality. Default Value: 0
0	DOWN	When '0', counter is counting up. When '1', counter is counting down. In QUAD mode, this field indicates the direction of the latest counter change: '0' when last incremented and '1' when last decremented. Default Value: 0

7.1.45 TCPWM_CNT3_COUNTER

Counter count register

Address: 0x402001C8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	COUNTER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	COUNTER [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	COUNTER	16-bit counter value. It is advised to not write to this field when the counter is running. Default Value: 0

7.1.46 TCPWM_CNT3_CC

Counter compare/capture register

Address: 0x402001CC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CC	In CAPTURE mode, captures the counter value. In other modes, compared to counter value. Default Value: 65535

7.1.47 TCPWM_CNT3_CC_BUFF

Counter buffered compare/capture register

Address: 0x402001D0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CC	Additional buffer for counter CC register. Default Value: 65535

7.1.48 TCPWM_CNT3_PERIOD

Counter period register

Address: 0x402001D4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	PERIOD	Period value: upper value of the counter. When the counter should count for n cycles, this field should be set to n-1. Default Value: 65535

7.1.49 TCPWM_CNT3_PERIOD_BUFF

Counter buffered period register

Address: 0x402001D8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	PERIOD	Additional buffer for counter PERIOD register. Default Value: 65535

7.1.50 TCPWM_CNT3_TR_CTRL0

Counter trigger control register 0

Address: 0x402001E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	COUNT_SEL [7:4]				CAPTURE_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	STOP_SEL [15:12]				RELOAD_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				START_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	START_SEL	Selects one of the 16 input triggers as a start trigger. In QUAD mode, this is the second phase (phi B). Default Value: 0
15 : 12	STOP_SEL	Selects one of the 16 input triggers as a stop trigger. In PWM, PWM_DT and PWM_PR modes, this is the kill trigger. In these modes, the kill trigger is used to either temporarily block the PWM outputs (PWM_STOP_ON_KILL is '0') or stop the functionality (PWM_STOP_ON_KILL is '1'). For the PWM and PWM_DT modes, the blocking of the output signals can be asynchronous (STOP_EDGE should be NO_EDGE_DET) in which case the blocking is as long as the trigger is '1' or synchronous (STOP_EDGE should be RISING_EDGE) in which case it extends till the next terminal count event. Default Value: 0
11 : 8	RELOAD_SEL	Selects one of the 16 input triggers as a reload trigger. In QUAD mode, this is the index or revolution pulse. In this mode, it will update the counter with the value in the TCPWM_CNTn_PERIOD register. Default Value: 0
7 : 4	COUNT_SEL	Selects one of the 16 input triggers as a count trigger. In QUAD mode, this is the first phase (phi A). Default setting selects input trigger 1, which is always '1'. Default Value: 1

(continued)

3 : 0	CAPTURE_SEL	Selects one of the 16 input triggers as a capture trigger. Input trigger 0 is always '0' and input trigger is always '1'. In the PWM, PWM_DT and PWM_PR modes this trigger is used to switch the values if the compare and period registers with their buffer counterparts. Default Value: 0

7.1.51 TCPWM_CNT3_TR_CTRL1

Counter trigger control register 1

Address: 0x402001E4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	STOP_EDGE [7:6]		RELOAD_EDGE [5:4]		COUNT_EDGE [3:2]		CAPTURE_EDGE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						START_EDGE [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 8	START_EDGE	A start event will start the counter; i.e. the counter will become running. Starting does NOT enable the counter. A start event will not initialize the counter whereas the reload event does. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE:** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.
7 : 6	STOP_EDGE	A stop event, will stop the counter; i.e. it will no longer be running. Stopping will NOT disable the counter. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event.

(continued)

		0x1: FALLING_EDGE: Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.
5 : 4	RELOAD_EDGE	A reload event will initialize the counter. When counting up, the counter is initialized to "0". When counting down, the counter is initialized with PERIOD. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE:** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.
3 : 2	COUNT_EDGE	A counter event will increase or decrease the counter by '1'. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE:** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.
1 : 0	CAPTURE_EDGE	A capture event will copy the counter value into the CC register. Default Value: 3 **0x0: RISING_EDGE:** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE:** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES:** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET:** No edge detection, use trigger as is.

7.1.52 TCPWM_CNT3_TR_CTRL2

Counter trigger control register 2

Address: 0x402001E8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW		RW		RW	
HW Access	None		R		R		R	
Name	None [7:6]		UNDERFLOW_MODE [5:4]		OVERFLOW_MODE [3:2]		CC_MATCH_MODE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 4	UNDERFLOW_MODE	Determines the effect of a counter underflow event (COUNTER reaches "0") on the "line_out" output signals. Default Value: 3 **0x0: SET:** Set to '1' **0x1: CLEAR:** Set to '0' **0x2: INVERT:** Invert **0x3: NO_CHANGE:** No Change
3 : 2	OVERFLOW_MODE	Determines the effect of a counter overflow event (COUNTER reaches PERIOD) on the "line_out" output signals. Default Value: 3 **0x0: SET:** Set to '1'

(continued)

		0x1: CLEAR: Set to '0' **0x2: INVERT:** Invert **0x3: NO_CHANGE:** No Change
1 : 0	CC_MATCH_MODE	Determines the effect of a compare match event (COUNTER equals CC register) on the "line_out" output signals. Note that INVERT is especially useful for center aligned pulse width modulation. To generate a duty cycle of 0%, the counter CC register should be set to "0". For a 100% duty cycle, the counter CC register should be set to larger than the counter PERIOD register. Default Value: 3 **0x0: SET:** Set to '1' **0x1: CLEAR:** Set to '0' **0x2: INVERT:** Invert **0x3: NO_CHANGE:** No Change

7.1.53 TCPWM_CNT3_INTR

Interrupt request register.

Address: 0x402001F0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1C	RW1C
HW Access	None						RW1S	RW1S
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Counter matches CC register event. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
0	TC	Terminal count event. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0

7.1.54 TCPWM_CNT3_INTR_SET

Interrupt set request register.

Address: 0x402001F4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1S	RW1S
HW Access	None						A	A
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	TC	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

7.1.55 TCPWM_CNT3_INTR_MASK

Interrupt mask register.

Address: 0x402001F8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	TC	Mask bit for corresponding bit in interrupt request register. Default Value: 0

7.1.56 TCPWM_CNT3_INTR_MASKED

Interrupt masked request register

Address: 0x402001FC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						W	W
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Logical and of corresponding request and mask bits. Default Value: 0
0	TC	Logical and of corresponding request and mask bits. Default Value: 0

8 System Resource Sub System Registers

This section discusses the CORE registers. It lists all the registers in mapping tables, in address order.

8.1 Register Details

Register Name	Address
PWR_CONTROL	0x400B0000
PWR_INTR	0x400B0004
PWR_INTR_MASK	0x400B0008
PWR_KEY_DELAY	0x400B000C
PWR_BG_CONFIG	0x400B0014
PWR_VMON_CONFIG	0x400B0018
PWR_DDFT_SELECT	0x400B0020
PWR_DFT_KEY	0x400B0024
PWR_BOD_KEY	0x400B0028
PWR_STOP	0x400B002C
CLK_SELECT	0x400B0100
CLK_ILO_CONFIG	0x400B0104
CLK_IMO_CONFIG	0x400B0108
CLK_IMO_SPREAD	0x400B010C
CLK_DFT_SELECT	0x400B0110
WDT_CTRLOW	0x400B0200
WDT_CTRHIGH	0x400B0204
WDT_MATCH	0x400B0208
WDT_CONFIG	0x400B020C
WDT_CONTROL	0x400B0210
RES_CAUSE	0x400B0300
PWR_BG_TRIM3	0x400BFF18
PWR_BG_TRIM4	0x400BFF1C
PWR_BG_TRIM5	0x400BFF20
CLK_ILO_TRIM	0x400BFF24
CLK_IMO_TRIM1	0x400BFF28
CLK_IMO_TRIM2	0x400BFF2C

Register Name	Address
CLK_IMO_TRIM4	0x400BFF34
PWR_RSVD_TRIM	0x400BFF38

8.1.1 PWR_CONTROL

Power Mode Control

Address: 0x400B0000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R	R	R			
HW Access	None		RW	RW	RW			
Name	None [7:6]		LPM_READY	DEBUG_SESSION	POWER_MODE [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	None						
HW Access	R	None						
Name	EXT_VCCD	None [22:16]						

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None	RW	RW1S	RW	None	RW1S	RW
HW Access	R	None	R	R	A	None	RW0C	R
Name	HIBER-NATE	None	LFCLK_SHORT	HIBERNATE_DISABLE	FIMO_DISABLE	None	HVMON_RELOAD	HVMON_ENABLE

Bits	Name	Description
31	HIBERNATE	Selects between HIBERNATE/DEEPSLEEP modes when Cortex-M0 enters low power mode (SleepDeep). Note: this bit is ignored when HIBERNATE_DISABLE=1. Default Value: 1 **0x0: DEEP_SLEEP:** Enter DeepSleep mode when CPU asserts SLEEPDEEP signal **0x1: HIBERNATE:** Enter Hibernate mode when CPU asserts SLEEPDEEP signal
29	LFCLK_SHORT	Short Vcclfclk and Vccdpslp power rails in DeepSleep power mode. This mode selection affects the accuracy specifications of the ILO oscillator due to supply noise. See Data Sheet for more details. 0: Do not short power domains 1: Short power domains Default Value: 0

(continued)

28	HIBERNATE_DISABLE	0: Normal operation, HIBERNATE works as described 1: HIBERNATE bit is ignored, Hibernate mode is permanently disabled (part will go to DeepSleep instead. Note: This bit is a write-once bit until the next reset. Default Value: 0
27	FIMO_DISABLE	This bit is asserted during the boot process 0: Forces IMO to operate at 12MHz, ignore its frequency and trim settings and operate independent on its external references. 1: Turns IMO into normal operational mode Default Value: 0
25	HVMON_RELOAD	Firmware writes 1 to reload HV State in hibernate shadow copy. Hardware clears this bit after reload was successful. Wait at least 9 cycles after writing/recalling NVL before reloading the HVMON. Default Value: 0
24	HVMON_ENABLE	0: HV State Monitoring is disabled 1: HV State Monitoring is automatically enable by sleep controller Default Value: 1
23	EXT_VCCD	Should be set by firmware if Vccd is provided externally (on Vccd pin). Setting this bit turns off the active regulator and will lead to system reset (PBOD) unless both Vddd and Vccd pins are supplied externally. Default Value: 0
5	LPM_READY	Indicates whether the low power mode regulators are ready to enter DEEPSLEEP or HIBERNATE mode. 0: If DEEPSLEEP or HIBERNATE mode is requested, device will enter SLEEP mode. When low power regulators are ready, device will automatically enter the originally requested mode. 1: Normal operation. DEEPSLEEP and HIBERNATE work as described. Default Value: 0
4	DEBUG_SESSION	Indicates whether a debug session is active (CDBGPWRUPREQ signal is 1) Default Value: 0 **0x0: NO_SESSION:** No debug session active **0x1: SESSION_ACTIVE:** Debug session is active
3 : 0	POWER_MODE	Current power mode of the device. Note that this field cannot be read in all power modes on actual silicon. Default Value: 0 **0x0: RESET:** RESET state **0x1: ACTIVE:** ACTIVE state **0x2: SLEEP:** SLEEP state **0x3: DEEP_SLEEP:** DEEP_SLEEP state **0x4: HIBERNATE:** HIBERNATE state

8.1.2 PWR_INTR

Power System Interrupt Register

Address: 0x400B0004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1C	None
HW Access	None						A	None
Name	None [7:2]						LVD	None

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	LVD	Indicates an Low Voltage Detect interrupt Default Value: 0

8.1.3 PWR_INTR_MASK

Power System Interrupt Mask Register

Address: 0x400B0008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	None
HW Access	None						R	None
Name	None [7:2]						LVD	None

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	LVD	1: Propagate interrupt to CPU Default Value: 0

8.1.4 PWR_KEY_DELAY

Power System Key Register

Address: 0x400B000C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	WAKEUP_HOLDOFF [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						WAKEUP_HOLDOFF [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 0	WAKEUP_HOLDOFF	Delay (in 12MHz IMO clock cycles) to wait for references to settle on wakeup from hibernate/ deepsleep. PBOD is ignored and system does not resume until this delay expires. Note that the same delay on POR is hard-coded. Default Value: 780

8.1.5 PWR_BG_CONFIG

Bandgap Trim and Configuration

Address: 0x400B0014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW	RW				RW
HW Access	R		R	R				R
Name	BG_DFT_ICORE_SEL [7:6]		BG_DFT_CORE_SEL	BG_DFT_VREF_SEL [4:1]				BG_DFT_EN

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							BG_DFT_VCORE_SEL

Bits	23	22	21	20	19	18	17	16
SW Access	None					RW		
HW Access	None					R		
Name	None [23:19]					VREF_EN [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
18 : 16	VREF_EN	Reference voltage enable. Each bit enables a reference voltage used by a peripheral: vref[0] = 1 enables SRSS.VREF[0] to 1.024V vref[1] = 1 enables SRSS.VREF[1] to 1.024V vref[2] = 1 enables SRSS.VREF[2] to 1.2V These references require 40us to settle after enabling them and 30us to settle after waknng from DeepSleep. Default Value: 0
8	BG_DFT_VCORE_SEL	ADFT mux select for Bandgap characterization (engineering only). Selects a BG core voltage to output on mux2out 0=vout 1=vgnd Default Value: 0

(continued)

7 : 6	BG_DFT_ICORE_SEL	ADFT mux select for Bandgap characterization (engineering only). Selects a BG core current to output on mux1out 0=iptat (current 1=ictat (current) 2=inl_cross_over detect (voltage) 3=iref9p6u_dft (dedicated output for DFT) Also selects a currect for iref_dft (when BG_DFT_VREF_SEL=13) 0=iref2p4u[1] 1=iptat2p4u[7] 2=iref_imo (9.6uA current output from IMO IBG) 3=iref3u_dft (dedicated output for DFT) Default Value: 0
5	BG_DFT_CORE_SEL	ADFT mux select for Bandgap characterization (engineering only). Selects which BG core signal to output on adft_bg_core 0=BG core voltage selected by BG_DFT_VCORE_SEL (mux2out) 1=BG core current selected by BG_DFT_ICORE_SEL (mux1out) Default Value: 0
4 : 1	BG_DFT_VREF_SEL	ADFT mux select for Reference System characterization (engineering only). Select a voltage reference to output on adft_bg_ref 0=vgnd 1=vref_fast[0] 2=vref_fast[1] 3=vref_fast[2] 4=vref_fast[3] 5=vref_fast[4] 6=vref_fast[5] 7=vref_fast[6] 8=vref_fast[7] 9=vref[0] 10=vref[1] 11=vref[2] 12=vctat 13=iref_dft (see BG_DFT_ICORE_SEL) 14=imo_iref (current) 15=inl_imoref (voltage) Default Value: 0
0	BG_DFT_EN	Enables DFT capability for Bandgap. (engineering only) Default Value: 0

8.1.6 PWR_VMON_CONFIG

Voltage Monitoring Trim and Configuration

Address: 0x400B0018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW			RW				RW
HW Access	R			R				R
Name	VMON_DDFT_SEL [7:5]			LVD_SEL [4:1]				LVD_EN

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						VMON_ADFT_SEL [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 8	VMON_ADFT_SEL	ADFT mux select for HVPOR, PBOD, and LVD circuits (engineering only). Selects a signal to output on adft_vmon 0: Hi-Z 1: Comparator Input of pbod Monitor 2: Comparator Input of hvpbod Monitor 3: Comparator Input of lvi Monitor Default Value: 0
7 : 5	VMON_DDFT_SEL	DDFT mux select for HVPOR, PBOD, and LVD circuits (engineering only). Selects a signal to output on adft_vmon 0: 0 1: pbod_out 2: Pulse Strecher output of pbod Monitor 3: hvpbod_out 4: Pulse Strecher output of hvpbod Monitor 5: lvi_out 6: Pulse Strecher output of lvi Monitor 7: 0 Default Value: 0

(continued)

4 : 1	LVD_SEL	Threshold selection for Low Voltage Detect circuit. Disable the LVD (LVD_EN=0) before changing the threshold. Threshold variation is +/- 2.5% from these typical voltage choices: 0: 1.7500 V 1: 1.8000 V 2: 1.9000 V 3: 2.0000 V 4: 2.1000 V 5: 2.2000 V 6: 2.3000 V 7: 2.4000 V 8: 2.5000 V 9: 2.6000 V 10: 2.7000 V 11: 2.8000 V 12: 2.9000 V 13: 3.0000 V 14: 3.2000 V 15: 4.5000 V Default Value: 0
0	LVD_EN	Enable Low Voltage Detect circuit. Default Value: 0

8.1.7 PWR_DDFT_SELECT

Digital DFT Select

Address: 0x400B0020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	DDFT2_SEL [7:4]				DDFT1_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	DDFT2_SEL	Signal select for ddft2 output: 0: act_power_en_a 1: power_up_raw 2: act_power_good_a 3: fastrefs_valid 4: vmon 5: bootref_outen 6: bootref_refsw 7: active_inrush_dis 8: awake 9: hvpor_reset_n 10: lpcomp_dis 11: wakeup_a 12: vmon_valid 13: block_rst_awake 14: slpholdreq_n 15: io_disable_delayed Default Value: 0

(continued)

3 : 0	DDFT1_SEL	Signal select for ddft1 output: 0: wakeup_a 1: ipor_reset 2: hbod_reset_raw_n 3: lpcomp_dis 4: power_up_delayed 5: awake 6: hvmon_out_of_sync 7: pbod_reset 8: hvbod_reset 9: lpm_ready 10: io_disable_req_lv (excluding por_force_in_hv) 11: bootref_en Default Value: 0

8.1.8 PWR_DFT_KEY

DFT Safety Override

Address: 0x400B0024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	KEY16 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	KEY16 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [23:21]			VMON_PD	IO_DISABLE_BYPASS	DFT_MODE	BODS_OFF	HBOD_OFF_AWAKE

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
20	VMON_PD	Disables the VMON block, which includes PBOD, HVBOD, and LVD circuits. Set BODS_OFF=1 in a previous write cycle to prevent an unintended reset. Default Value: 0
19	IO_DISABLE_BYPASS	Bypasses the IO disable logic for testing the delay-line that is part of the glitch-free IO reset circuitry. Internally, prevents the outputs from getting disabled (io_disable_req_hv=0) and blocks resets (io_disable_ack_hv=0). The delay-line continues to function and can be routed to DDFT for testing. Default Value: 0
18	DFT_MODE	Enable DfT modes other than the above. Currently gates power_up comparator for characterization. Default Value: 0
17	BODS_OFF	Forces all outputs of BOD detectors to be ignored, effectively disabling all brown-out detection. Can be used in conjunction with DDFT to test the detectors without triggering reset. Default Value: 0
16	HBOD_OFF_AWAKE	Forces the output of the HBOD to be blocked (ignored) while in Active or Sleep mode (i.e. when under the umbrella of PBOD). Default Value: 0

(continued)

15 : 0	KEY16	This field must be set to 0xE4C5 for any of the other fields in this register to have effect and for scan_mode to be allowed. When this fields has any other value, all other fields in this register are ignored and assumed to be 0 by the hardware, and scan_mode is ignored inside the power generation system. It is assumed that this register will always be set to 0xE4C5 before entering scan. Default Value: 0

8.1.9 PWR_BOD_KEY

BOD Detection Key

Address: 0x400B0028

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	KEY16 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	KEY16 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	KEY16	To detect brown-outs firmware should do this on boot: 1. Set key= KEY16 2. Set KEY16= 0x3A71 3. If key==0x3A71 this was a brown-out event. Default Value: X

8.1.10 PWR_STOP

STOP Mode Register

Address: 0x400B002C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	TOKEN [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	UNLOCK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	RW
HW Access	None						A	A
Name	None [23:18]						FREEZE	POLARITY

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	A	None						
Name	STOP	None [30:24]						

Bits	Name	Description
31	STOP	Firmware sets this bit to enter STOP mode. Both UNLOCK and FREEZE must have been set correctly in a previous write operation. Otherwise, writes to this bit will affect the freeze override but will not actually set the STOP bit. The system will enter STOP mode immediately after writing to this bit and will wakeup only in response to XRES or WAKEUP event. Default Value: 0
17	FREEZE	Firmware sets this bit to freeze the configuration, mode and state of all GPIOs and SIOs in the system. Two identical write cycles are required to freeze the IO explicitly. The first cycle instructs DEEPSLEEP and HIBERNATE peripherals whether they can override upcoming freeze command(s). UNLOCK setting does not affect this. If firmware writes FREEZE=1 and STOP=0, peripherals can override the freeze and remain functional according to their configuration. If firmware writes FREEZE=1 and STOP=1, peripherals cannot override the next freeze command. The second write cycle freezes the IO if UNLOCK is set and the peripheral does not override the freeze. While FREEZE=1, peripherals will automatically freeze according to the override directive when entering DEEPSLEEP or HIBERNATE, regardless of the UNLOCK setting. Default Value: 0
16	POLARITY	0: WAKEUP=0 will wakeup the part from STOP 1: WAKEUP=1 will wakeup the part from STOP Default Value: 0

(continued)

15 : 8	UNLOCK	This byte must be set to 0x3A for FREEZE or STOP fields to operate. Any other value in this register will cause FREEZE/STOP to have no effect, except as noted in the FREEZE description. Default Value: 0
7 : 0	TOKEN	Contains a 8-bit token that is retained through a STOP/WAKEUP sequence that can be used by firmware to differentiate WAKEUP from a general RESET event. Note that waking up from STOP using XRES will reset this register. Default Value: 0

8.1.11 CLK_SELECT

Clock Select Register

Address: 0x400B0100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW			RW		
HW Access	R		R			R		
Name	PLL_SEL [7:6]		DBL_SEL [5:3]			DIRECT_SEL [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW		RW			RW
HW Access	A		R		R			R
Name	WDT_LOCK [15:14]		DPLLREF_SEL [13:12]		DPLLIN_SEL [11:9]			PLL_SEL

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW			RW	RW	
HW Access	None		R			R	R	
Name	None [23:22]		SYSCLK_DIV [21:19]			HALF_EN	HFCLK_SEL [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
21 : 19	SYSCLK_DIV	SYSCLK Pre-Scaler Value. Default Value: 0 **0x0: NO_DIV:** SYSCLK= HFCLK/1 **0x1: DIV_BY_2:** SYSCLK= HFCLK/2 **0x2: DIV_BY_4:** SYSCLK= HFCLK/4 **0x3: DIV_BY_8:** SYSCLK= HFCLK/8 **0x4: DIV_BY_16:** SYSCLK= HFCLK/16 **0x5: DIV_BY_32:** SYSCLK= HFCLK/32 **0x6: DIV_BY_64:** SYSCLK= HFCLK/64

(continued)

		0x7: DIV_BY_128: SYSCLK= HFCLK/128
18	HALF_EN	This bit impact products using CPUSSv1 only. It has no effect on products using CPUSSv2. FLASH Wait-state selection. This must be set to 1 when clk_sys is set to a frequency greater than 24MHz. 0: Access FLASH using 0 wait-states. Only use this setting when HFCLK is <=24MHz. 1: Access FLASH using 1 wait-state. Safe to use this setting for any clock frequency. Default Value: 0
17 : 16	HFCLK_SEL	Selects the source for HFCLK. Default Value: 0 **0x0: DIRECT_SEL:** Source selected by DIRECT_SEL **0x1: DBL:** Output of DBL (Doubler) - Selects output of EXCO PLL1 if supported. Note that not all products support all clock sources. Selecting a clock source that is not supported will result in undefined behavior. Note: this is called DBL for legacy reasons, and cannot be changed without breaking collateral for multiple existing products. **0x2: PLL:** Output of PLL - Selects output of EXCO PLL0 if supported. Note that not all products support all clock sources. Selecting a clock source that is not supported will result in undefined behavior. Note: this is called PLL for legacy reasons, and cannot be changed without breaking collateral for multiple existing products.
15 : 14	WDT_LOCK	Prohibits writing to WDT_* registers and CLK_ILO register when not equal 0. Requires at least two different writes to unlock. Note that this field is 2 bits to force multiple writes only. It represents only a single write protect signal protecting all WATCHDOG registers at the same time. Default Value: 0 **0x0: NO_CHG:** No effect **0x1: CLR0:** Clears bit 0 **0x2: CLR1:** Clears bit 1 **0x3: SET01:** Sets both bits 0 and 1
13 : 12	DPLLREF_SEL	Selects a source for the reference (tracking) input of DPLL: 0: DSI_OUT[0] 1: DSI_OUT[1] 2: DSI_OUT[2] 3: DSI_OUT[3] Default Value: 0 **0x0: DSI0:** DSI_OUT[0] **0x1: DSI1:** DSI_OUT[1] **0x2: DSI2:** DSI_OUT[2]

(continued)

		0x3: DSI3: DSI_OUT[3]
11 : 9	DPLLIN_SEL	Selects a source for the input of DPLL. Note that not all products support all clock sources. Selecting a clock source that is not supported will result in undefined behavior. Default Value: 0 **0x0: IMO:** IMO - Internal R/C Oscillator **0x1: EXTCLK:** EXTCLK - External Clock Pin **0x2: ECO:** ECO - External-Crystal Oscillator (Crystal external, Oscilator internal) **0x4: DSI0:** DSI_OUT[0] **0x5: DSI1:** DSI_OUT[1] **0x6: DSI2:** DSI_OUT[2] **0x7: DSI3:** DSI_OUT[3]
8 : 6	PLL_SEL	Selects a source the input of EXCO PLL0, if supported. Note that not all products support all clock sources. Selecting a clock source that is not supported will result in undefined behavior. Note: this is called PLL_SEL for legacy reasons, and cannot be changed without breaking collateral for multiple existing products. Default Value: 0 **0x0: IMO:** IMO - Internal R/C Oscillator **0x1: EXTCLK:** EXTCLK - External Clock Pin **0x2: ECO:** ECO - External-Crystal Oscillator (Crystal external, Oscilator internal) **0x3: DPLL:** DPLL - DPLL Output **0x4: DSI0:** DSI_OUT[0] **0x5: DSI1:** DSI_OUT[1] **0x6: DSI2:** DSI_OUT[2] **0x7: DSI3:** DSI_OUT[3]

(continued)

5 : 3	DBL_SEL	Selects a source the input of EXCO PLL1, if supported. Note that not all products support all clock sources. Selecting a clock source that is not supported will result in undefined behavior. Note: this is called DBL_SEL for legacy reasons, and cannot be changed without breaking collateral for multiple existing products. Default Value: 0 **0x0: IMO:** IMO - Internal R/C Oscillator **0x1: EXTCLK:** EXTCLK - External Clock Pin **0x2: ECO:** ECO - External-Crystal Oscillator (Crystal external, Oscilator internal) **0x4: DSI0:** DSI_OUT[0] **0x5: DSI1:** DSI_OUT[1] **0x6: DSI2:** DSI_OUT[2] **0x7: DSI3:** DSI_OUT[3]
2 : 0	DIRECT_SEL	Selects a source for HFCLK (when HFCLK_SEL=0) and DSI_IN[0]. Note that not all products support all clock sources. Selecting a clock source that is not supported will result in undefined behavior. Note that using DSI_OUT[3:0] as HFCLK source will also result in undefined behavior. These values are available strictly to provide a clock in DSI_IN[0]. Default Value: 0 **0x0: IMO:** IMO - Internal R/C Oscillator **0x1: EXTCLK:** EXTCLK - External Clock Pin **0x2: ECO:** ECO - External-Crystal Oscillator (Crystal external, Oscilator internal) **0x4: DSI0:** DSI_OUT[0] **0x5: DSI1:** DSI_OUT[1] **0x6: DSI2:** DSI_OUT[2] **0x7: DSI3:** DSI_OUT[3]

8.1.12 CLK_ILO_CONFIG

ILO Configuration

Address: 0x400B0104

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [7:3]					SATBIAS	TURBO	PD_MODE

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	ENABLE	None [30:24]						

Bits	Name	Description
31	ENABLE	Master enable for ILO oscillator Default Value: 0
2	SATBIAS	PFET bias. Leave this bit at the default setting for normal operation. Engineering only. Default Value: 1 **0x0: SATURATED:** Enable saturated PFET bias **0x1: SUBTHRESHOLD:** Enable subthreshold PFET bias
1	TURBO	Turbo mode for faster startup from coma power down. Leave this bit at the default setting for normal operation. Engineering only. 0: turbo disabled 1: turbo enabled Default Value: 1
0	PD_MODE	Power down mode. Note: this bit must always be set to 0 and never changed. Behavior is un-defined when set to 1. Default Value: 0

(continued)

0x0: SLEEP:
Sleep (faster startup - enables pulsegen block)

0x1: COMA:
Coma (slower startup)

8.1.13 CLK_IMO_CONFIG

IMO Configuration

Address: 0x400B0108

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	None					
HW Access	R	R	None					
Name	EN_FASTBIAS	FLASHPUMP_SEL	None [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW			RW
HW Access	R	R	R	R	R			R
Name	ENABLE	EN_CLK2X	EN_CLK36	TEST_USB_MODE	PUMP_SEL [27:25]			TEST_FASTBIAS

Bits	Name	Description
31	ENABLE	Master enable for IMO oscillator. Clearing this bit will disable the IMO but not disconnect it from the power rail. This bit can also be used during IDDQ testing. Default Value: 1
30	EN_CLK2X	Enables main oscillator doubler circuit that can be used for TSS Charge Pumps. This circuit is not available to generate any digital clocks. Default Value: 0
291 and PUMP_SEL3 3. If so, set EN_CLK36 =0 4. Enable interrupts Default Value: 0	EN_CLK36	Enables 36MHz secondary oscillator that can be used for Pump or Flash Pump. Note: Since there are two consumers of the 36MHz clock, care should be taken when clearing this bit. The correct procedure for clearing this bit is: 1. Disable interrupts 2. Check if both FLASHPUMP_SEL

(continued)

28	TEST_USB_MODE	Forces IMO into USB mode. Engineering only. 1: Software can write FSOFFSET, OFFSET, and GAIN settings for characterization. Hardware updates to these registers are not blocked, so disable USB peripheral updates if they are not desired. 0: Normal operation. IMO operates in either USB or non-USB mode, depending on the USB peripheral setting. Default Value: 0
27 : 25	PUMP_SEL	Selects operating source for Pump clock. This clock is not guaranteed to be glitch free when changing IMO parameters or clock divider settings. 5-7: reserved, do not use Default Value: 0 **0x0: GND:** No clock, connect to gnd **0x1: IMO:** Use main IMO output **0x2: DBL:** Use doubler output **0x3: CLK36:** Use 36MHz oscillator. Note: always set EN_CLK36 when selecting this value for PUMP_SEL. Flash program/erase operations will set EN_CLK36=0 when PUMP_SEL!=CLK36. This selection is ONLY valid for PSoC4A-BLE. **0x4: FF1:** Use divided clock FF1
24	TEST_FASTBIAS	Forces the IMO into FIMO mode (engineering only). Only works when EN_FASTBIAS=1. Default Value: 0
23	EN_FASTBIAS	Forces the FIMO's fast bias circuits to remain powered (engineering only). This bit must be cleared by BootROM after FIMO is no longer required. Default Value: 1
22	FLASHPUMP_SEL	Selects operating source for SPCIF Timer/Flash Pump clock. Default Value: 0 **0x0: GND:** No clock, connect to gnd **0x1: CLK36:** Use 36MHz oscillator

8.1.14 CLK_IMO_SPREAD

IMO Spread Spectrum Configuration

Address: 0x400B010C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				A			
Name	None [7:5]				SS_VALUE [4:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:13]				SS_MAX [12:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW		RW		None			
HW Access	R		R		None			
Name	SS_MODE [31:30]		SS_RANGE [29:28]		None [27:24]			

Bits	Name	Description
31 : 30	SS_MODE	Spread Spectrum Mode. Default Value: 0 **0x0: OFF:** Off, do not change SS_VALUE **0x1: TRIANGLE:** Modulate using triangle wave (see SS_MAX) **0x2: LFSR:** Modulate using pseudo random sequence (using LFSR) **0x3: DSI:** Take value directly from DSI (synchronized by divided clock FF1)
29 : 28	SS_RANGE	Spread spectrum range (downspread when SS_VALUE=16). 3: reserved, do not use Default Value: 0 **0x0: M1:** 0 .. -1%

(continued)

		0x1: M2: 0 .. -2% **0x2: M4:** 0 .. -4%
12 : 8	SS_MAX	Maximum counter value for spread spectrum. Counter will count from 0..SS_MAX..0 and keep repeating this indefinitely. Only works when SS_MODE=1. Default Value: 0
4 : 0	SS_VALUE	Current offset value for spread spectrum modulation. IMO supports values 0..16. Step size is determined by SS_RANGE. Value is encoded in proper thermometric format for IMO in hardware. Value can be modified in firmware only when SS_MODE=0. Default Value: 0

8.1.15 CLK_DFT_SELECT

Clock DFT Mode Selection Register

Address: 0x400B0110

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW		RW			
HW Access	None		R		R			
Name	None [7:6]		DFT_DIV1 [5:4]		DFT_SEL1 [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW		RW			
HW Access	None		R		R			
Name	None [15:14]		DFT_DIV2 [13:12]		DFT_SEL2 [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
13 : 12	DFT_DIV2	DFT Output Divide Down. Default Value: 0 **0x0: NO_DIV:** Direct Output **0x1: DIV_BY_2:** Divide by 2 **0x2: DIV_BY_4:** Divide by 4 **0x3: DIV_BY_8:** Divide by 8
11 : 8	DFT_SEL2	Select signal for DFT output #2. Default Value: 0 **0x0: NC:** Disabled - output is not connected **0x1: ILO:** ILO output

(continued)

		0x2: WCO: WCO output **0x3: IMO:** IMO primary output **0x4: ECO:** ECO output **0x5: PLL:** PLL output **0x6: DPLL_OUT:** DPLL output **0x7: DPLL_REF:** DPLL reference input **0x8: DBL:** DBL output **0x9: IMO2X:** IMO 2x Clock Output **0xa: IMO36:** IMO 36MHz Clock Output **0xb: HFCLK:** HFCLK **0xc: LFCLK:** LFCLK **0xd: SYSCLK:** SYSCLK **0xe: EXTCLK:** EXTCLK **0xf: HALFSYSCLK:** 0 - removed
5 : 4	DFT_DIV1	DFT Output Divide Down. Default Value: 0 **0x0: NO_DIV:** Direct Output **0x1: DIV_BY_2:** Divide by 2 **0x2: DIV_BY_4:** Divide by 4 **0x3: DIV_BY_8:** Divide by 8
3 : 0	DFT_SEL1	Select signal for DFT output #1. Default Value: 0 **0x0: NC:** Disabled - output is not connected **0x1: ILO:** ILO output

(continued)

0x2: WCO:
WCO output

0x3: IMO:
IMO primary output

0x4: ECO:
ECO output

0x5: PLL:
PLL output

0x6: DPLL_OUT:
DPLL output

0x7: DPLL_REF:
DPLL reference input

0x8: DBL:
DBL output

0x9: IMO2X:
IMO 2x Clock Output

0xa: IMO36:
IMO 36MHz Clock Output

0xb: HFCLK:
HFCLK

0xc: LFCLK:
LFCLK

0xd: SYSCLK:
SYSCLK

0xe: EXTCLK:
EXTCLK

0xf: HALFSYSCLK:
0 - removed

8.1.16 WDT_CTRLOW

Watchdog Counters 0/1

Address: 0x400B0200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	WDT_CTR0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	WDT_CTR0 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	WDT_CTR1 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	WDT_CTR1 [31:24]							

Bits	Name	Description
31 : 16	WDT_CTR1	Current value of WDT Counter 1 Default Value: 0
15 : 0	WDT_CTR0	Current value of WDT Counter 0 Default Value: 0

8.1.17 WDT_CTRHIGH

Watchdog Counter 2

Address: 0x400B0204

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	WDT_CTR2 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	WDT_CTR2 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	WDT_CTR2 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	WDT_CTR2 [31:24]							

Bits	Name	Description
31 : 0	WDT_CTR2	Current value of WDT Counter 2 Default Value: 0

8.1.18 WDT_MATCH

Watchdog counter match values

Address: 0x400B0208

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	WDT_MATCH0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	WDT_MATCH0 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	WDT_MATCH1 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	WDT_MATCH1 [31:24]							

Bits	Name	Description
31 : 16	WDT_MATCH1	Match value for Watchdog Counter 1 Default Value: 0
15 : 0	WDT_MATCH0	Match value for Watchdog Counter 0 Default Value: 0

8.1.19 WDT_CONFIG

Watchdog Counters Configuration

Address: 0x400B020C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	
HW Access	None				R	R	R	
Name	None [7:4]				WDT_CASCADE0_1	WDT_CLEAR0	WDT_MODE0 [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	RW	RW	
HW Access	None				R	R	R	
Name	None [15:12]				WDT_CASCADE1_2	WDT_CLEAR1	WDT_MODE1 [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							WDT_MODE2

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None	RW				
HW Access	R		None	R				
Name	LFCLK_SEL [31:30]		None	WDT_BITS2 [28:24]				

Bits	Name	Description
31 : 30	LFCLK_SEL	Select source for LFCLK: 0: ILO - Internal R/C Oscillator 1: WCO - Internal Crystal Oscillator 2-3: Reserved - do not use Note that not all products support all clock sources. Selecting a clock source that is not supported will result in undefined behavior. To safely change LFCLK_SEL wait for WDT_CTRLOW/WDT_CTRHIGH to change then chaneg the setting immediately. Default Value: 0
28 : 24	WDT_BITS2	Bit to observe for WDT_INT2: 0: Assert when bit0 of WDT_CTR2 toggles (one int every tick) .. 31: Assert when bit31 of WDT_CTR2 toggles (one int every 2^31 ticks) Default Value: 0
16	WDT_MODE2	Watchdog Counter 2 Mode. Default Value: 0

(continued)

		0x0: NOTHING: Free running counter with no interrupt requests **0x1: INT:** Free running counter with interrupt request when a specified bit in CTR2 toggles (see WDT_BITS2)
11	WDT_CASCADE1_2	Cascade Watchdog Counters 1,2. Counter 2 increments the cycle after WDT_CTR1=WDT_MATCH1. It is allowed to cascade all three WDT counters. 0: Independent counters 1: Cascaded counters Default Value: 0
10	WDT_CLEAR1	Clear Watchdog Counter when WDT_CTR1=WDT_MATCH1. In other words WDT_CTR1 divides LFCLK by (WDT_MATCH1+1). 0: Free running counter 1: Clear on match Default Value: 0
9 : 8	WDT_MODE1	Watchdog Counter Action on Match (WDT_CTR1=WDT_MATCH1). Default Value: 0 **0x0: NOTHING:** Do nothing **0x1: INT:** Assert WDT_INTx **0x2: RESET:** Assert WDT Reset **0x3: INT_THEN_RESET:** Assert WDT_INTx, assert WDT Reset after 3rd unhandled interrupt
3	WDT_CASCADE0_1	Cascade Watchdog Counters 0,1. Counter 1 increments the cycle after WDT_CTR0=WDT_MATCH0. 0: Independent counters 1: Cascaded counters Default Value: 0
2	WDT_CLEAR0	Clear Watchdog Counter when WDT_CTR0=WDT_MATCH0. In other words WDT_CTR0 divides LFCLK by (WDT_MATCH0+1). 0: Free running counter 1: Clear on match Default Value: 0
1 : 0	WDT_MODE0	Watchdog Counter Action on Match (WDT_CTR0=WDT_MATCH0). Default Value: 0 **0x0: NOTHING:** Do nothing **0x1: INT:** Assert WDT_INTx **0x2: RESET:** Assert WDT Reset **0x3: INT_THEN_RESET:** Assert WDT_INTx, assert WDT Reset after 3rd unhandled interrupt

8.1.20 WDT_CONTROL

Watchdog Counters Control

Address: 0x400B0210

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1S	RW1C	R	RW
HW Access	None				RW0C	A	RW	R
Name	None [7:4]				WDT_RESET0	WDT_INT0	WDT_ENABLED0	WDT_ENABLE0

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW1S	RW1C	R	RW
HW Access	None				RW0C	A	RW	R
Name	None [15:12]				WDT_RESET1	WDT_INT1	WDT_ENABLED1	WDT_ENABLE1

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW1S	RW1C	R	RW
HW Access	None				RW0C	A	RW	R
Name	None [23:20]				WDT_RESET2	WDT_INT2	WDT_ENABLED2	WDT_ENABLE2

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19	WDT_RESET2	Resets counter 2 back to 0000_0000. Hardware will reset this bit after counter was reset. This will take several LFCLK cycles to take effect. Wait until the reset completes before enabling the WDT. Default Value: 0
18	WDT_INT2	WDT Interrupt Request. This bit is set by hardware as configured by this registers. This bit must be cleared by firmware. Clearing this bit also prevents Reset from happening when WDT_MODEx=3. After W1C, WDT_CONTROL must be read for the hardware to internally re-move the clear flag. Failure to do this may result in missing the next interrupt. Default Value: 0
17	WDT_ENABLED2	Indicates actual state of counter. May lag WDT_ENABLE2 by up to 3 LFCLK cycles. After changing WDT_ENABLE2, do not enter DEEPSLEEP mode until this field acknowledges the change. Default Value: 0

(continued)

16	WDT_ENABLE2	Enable Counter 2 0: Counter is disabled (not clocked) 1: Counter is enabled (counting up) Note: This field takes considerable time (up to 3 LFCLK cycles) to take effect. It must not be changed more than once in that period. Default Value: 0
11	WDT_RESET1	Resets counter 1 back to 0000. Hardware will reset this bit after counter was reset. This will take several LFCLK cycles to take effect. Wait until the reset completes before enabling the WDT. Default Value: 0
10	WDT_INT1	WDT Interrupt Request. This bit is set by hardware as configured by this registers. This bit must be cleared by firmware. Clearing this bit also prevents Reset from happening when WDT_MODEx=3. After W1C, WDT_CONTROL must be read for the hardware to internally remove the clear flag. Failure to do this may result in missing the next interrupt. Default Value: 0
9	WDT_ENABLED1	Indicates actual state of counter. May lag WDT_ENABLE1 by up to 3 LFCLK cycles. After changing WDT_ENABLE1, do not enter DEEPSLEEP mode until this field acknowledges the change. Default Value: 0
8	WDT_ENABLE1	Enable Counter 1 0: Counter is disabled (not clocked) 1: Counter is enabled (counting up) Note: This field takes considerable time (up to 3 LFCLK cycles) to take effect. It must not be changed more than once in that period. Default Value: 0
3	WDT_RESET0	Resets counter 0 back to 0000. Hardware will reset this bit after counter was reset. This will take several LFCLK cycles to take effect. Wait until the reset completes before enabling the WDT. Default Value: 0
2	WDT_INT0	WDT Interrupt Request. This bit is set by hardware as configured by this registers. This bit must be cleared by firmware. Clearing this bit also prevents Reset from happening when WDT_MODEx=3. After W1C, WDT_CONTROL must be read for the hardware to internally remove the clear flag. Failure to do this may result in missing the next interrupt. Default Value: 0
1	WDT_ENABLED0	Indicates actual state of counter. May lag WDT_ENABLE0 by up to 3 LFCLK cycles. After changing WDT_ENABLE0, do not enter DEEPSLEEP mode until this field acknowledges the change. Default Value: 0
0	WDT_ENABLE0	Enable Counter 0 0: Counter is disabled (not clocked) 1: Counter is enabled (counting up) Note: This field takes considerable time (up to 3 LFCLK cycles) to take effect. It must not be changed more than once in that period. Default Value: 0

8.1.21 RES_CAUSE

Reset Cause Observation Register

Address: 0x400B0300

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
Name	RESET_XRES	RESET_PBOD	RESET_HVBOD	RESET_SOFT	RESET_PROT_FAULT	RESET_LOCKUP	RESET_DSBOD	RESET_WDT

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	RESET_XRES	This field is deprecated and will always read 0. Default Value: 0
6	RESET_PBOD	This field is deprecated and will always read 0. Default Value: 0
5	RESET_HVBOD	This field is deprecated and will always read 0. Default Value: 0
4	RESET_SOFT	Cortex-M0 requested a system reset through it's SYSRESETREQ. This can be done via a debugger probe or in firmware. Default Value: 0
3	RESET_PROT_FAULT	A protection violation occurred that requires a RESET. This includes, but is not limited to, hitting a debug breakpoint while in Privileged Mode. Default Value: 0
2	RESET_LOCKUP	This field is deprecated and will always read 0. Cortex-M0 LOCKUP is no longer a reset source. Default Value: 0
1	RESET_DSBOD	This field is deprecated and will always read 0. Default Value: 0

(continued)

0	RESET_WDT	A WatchDog Timer reset has occurred since last power cycle. Default Value: 0

8.1.22 PWR_BG_TRIM3

Bandgap Trim Register

Address: 0x400BFF18

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW				RW		
HW Access	None	R				R		
Name	None	INL_CROSS_IMO [6:3]				INL_TRIM_IMO [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
6 : 3	INL_CROSS_IMO	IMO Irefgen INL cross-over point control for centering curve at 30C. Default Value: 11
2 : 0	INL_TRIM_IMO	IMO Irefgen nonlinear current trim for curvature correction. Default Value: 7

8.1.23 PWR_BG_TRIM4

Bandgap Trim Register

Address: 0x400BFF1C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		ABS_TRIM_IMO [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	ABS_TRIM_IMO	IMO-irefgen output current magnitude trim Default Value: 32

8.1.24 PWR_BG_TRIM5

Bandgap Trim Register

Address: 0x400BFF20

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		TMPCO_TRIM_IMO [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	TMPCO_TRIM_IMO	IMO-irefgen output current temperature co-efficient trim Default Value: 32

8.1.25 CLK_ILO_TRIM

ILO Trim Register

Address: 0x400BFF24

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	COARSE_TRIM [7:4]				TRIM [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	COARSE_TRIM	Adjusts the bias in the event of high current after fab. Leave these bits at the default setting for normal operation.: Bias trim: bit3=0: Normal Mode bit3=1:Low Current Mode Resistor Trim (Short R to gnd): bit2=0: Normal Mode bit2=1: Short R/4 bit1=0: Unshort R/2 bit1=1: Normal Mode (Short R/2) bit0=0: Unshort R/4 bit0=1: Normal Mode (Short 3R/4) Default Value: 3
3 : 0	TRIM	Trim bits to control frequency 0: Minimum frequency 15: Maximum frequency Default Value: 8

8.1.26 CLK_IMO_TRIM1

IMO Trim Register

Address: 0x400BFF28

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	OFFSET [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. This field is hardware updated during USB osclock mode. Default Value: 128

8.1.27 CLK_IMO_TRIM2

IMO Trim Register

Address: 0x400BFF2C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		FREQ [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	FREQ	Frequency to be selected (default 24MHz). Frequencies can be selected from 3..48MHz. When changing this field approriate values for IMO_CLK_TRIM1, PWR_BG_TRIM4 and PWR_BG_TRIM5 must be selected from trim tables determined at manufacturing time and stored in SFLASH. This process is documented in the SAS under "Clocks - Selecting IMO Frequency". For encoding of this field a lookup table is required, where the frequency increases in 1MHz steps in the regions listed below. Unspecified values have undefined behavior. A complete lookup table is in BROS 001-59652 Sec 4.2.2. [3-12] => [3MHz-12MHz] [14-25] => [13MHz-24MHz] [27-35] => [25MHz-33MHz] [37-43] => [34MHz-40MHz] [46-53] => [41MHz-48MHz] Default Value: 25

8.1.28 CLK_IMO_TRIM4

IMO Trim Register

Address: 0x400BFF34

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	RW				R			
Name	FSOFFSET [7:5]				GAIN [4:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 5	FSOFFSET	Full-speed USB offset. Updated by hardware during USB osclock mode. Can be updated by software when TEST_USB_MODE=1. Otherwise writes are ignored. Engineering only. Default Value: 0
4 : 0	GAIN	Gain for IMO. Typically stored in SFLASH and copied here on boot. Only used during USB mode, either during USB operation or when CLK_IMO_CONFIG.TEST_USB_MODE=1. When not in USB mode, this register is not used and the actual IMO gain is forced to a setting of 0. Default Value: 0

8.1.29 PWR_RSVD_TRIM

Reserved, unused registers

Address: 0x400BFF38

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				RSVD_TRIM [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	RSVD_TRIM	Reserved, unused registers. Default Value: 0

9 CPU Sub System (CPUSS) Registers

This section discusses the CPUSS registers. It lists all the registers in mapping tables, in address order.

9.1 Register Details

Register Name	Address
CPUSS_CONFIG	0x40100000
CPUSS_SYSREQ	0x40100004
CPUSS_SYSARG	0x40100008
CPUSS_INT_SEL	0x40100020
CPUSS_INT_MODE	0x40100024
CPUSS_NMI_MODE	0x40100028
CPUSS_FLASH_CTL	0x40100030
CPUSS_ROM_CTL	0x40100034

9.1.1 CPUSS_CONFIG

Configuration register

Address: 0x40100000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							VECT_IN_RAM

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	VECT_IN_RAM	0': Vector Table is located at 0x0000:0000 in flash '1': Vector Table is located at 0x2000:0000 in SRAM Note that vectors for RESET and FAULT are always fetched from ROM. Value in flash/RAM is ignored for these vectors. Default Value: 0

9.1.2 CPUSS_SYSREQ

SYSCALL control register

Address: 0x40100004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	SYSCALL_COMMAND [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	SYSCALL_COMMAND [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	R	R	RW	RW	None		
HW Access	R	A	RW	A	R	None		
Name	SYSCALL_REQ	HMASTER_0	ROM_ACCESS_EN	PRIVI-LEGED	DIS_RESET_VECT_REL	None [26:24]		

Bits	Name	Description
31	SYSCALL_REQ	CPU/DAP writes a '1' to this field to request a SystemCall. The HMASTER_0 field indicates the source of the write access. Setting this field to '1' immediate results in a NMI. The SystemCall NMI interrupt handler sets this field to '0' after servicing the request. Default Value: 0
30	HMASTER_0	Indicates the source of the write access to the SYSREQ register. '0': CPU write access. '1': DAP write access. HW sets this field when the SYSREQ register is written to and SYSCALL_REQ is '0' (the last time it is set is when SW sets SYSCALL_REQ from '0' to '1'). Default Value: 0
29	ROM_ACCESS_EN	Indicates that executing from Boot ROM is enabled. HW sets this field to '1', on reset or when the SystemCall NMI vector is fetched from Boot ROM. HW sets this field to '0', when the CPU is NOT executing from either Boot or System ROM. This bit is used for debug purposes only. Default Value: 1

(continued)

28	PRIVILEGED	Indicates whether the system is in privileged ('1') or user mode ('0'). Only CPU SW executing from ROM can set this field to '1' when ROM_ACCESS_EN is '1' (the CPU is executing a SystemCall NMI interrupt handler). Any other write to this field sets is to '0'. This field is used as the AHB-Lite hprot[1] signal to implement Cypress proprietary user/privileged modes. These modes are used to enable/disable access to specific MMIO registers and memory regions. Default Value: 1
27	DIS_RESET_VECT_REL	Disable Reset Vector fetch relocation: '0': CPU accesses to locations 0x0000:0000 - 0x0000:0007 are redirected to ROM. '1': CPU accesses to locations 0x0000:0000 - 0x0000:0007 are made to flash. Note that this field defaults to '0' on reset, ensuring actual reset vector fetches are always made to ROM. Note that this field does not affect DAP accesses. Flash DfT routines may set this bit to '1' to enable uninhibited read-back of programmed data in the first flash page. Default Value: 0
15 : 0	SYSCALL_COMMAND	Opcode of the system call being requested. Default Value: 0

9.1.3 CPUSS_SYSARG

SYSARG control register

Address: 0x40100008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	SYSCALL_ARG [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	SYSCALL_ARG [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	SYSCALL_ARG [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	SYSCALL_ARG [31:24]							

Bits	Name	Description
31 : 0	SYSCALL_ARG	Argument to System Call specified in SYSREQ. Semantics of argument depends on system call made. Typically a pointer to a parameter block. Default Value: 0

9.1.4 CPUSS_INT_SEL

Interrupt multiplexer select register

Address: 0x40100020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DSI [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DSI [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DSI [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	DSI [31:24]							

Bits	Name	Description
31 : 0	DSI	Specifies interrupt source: '0': Fixed Function. '1': DSI. When changing the source of a specific interrupt, it is advised to temporarily disable the interrupt using the CM0 NVIC's CLRENA and SETENA interrupt enable clear and set registers to prevent a spurious interrupt activation. In addition, the CM0 NVIC's CLRPEND interrupt pending clear register should be used clear a pending interrupt before re-enabling the interrupt. Default Value: 0

9.1.5 CPUSS_INT_MODE

DSI interrupt pulse mode register

Address: 0x40100024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DSI_INT_PULSE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DSI_INT_PULSE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DSI_INT_PULSE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	DSI_INT_PULSE [31:24]							

Bits	Name	Description
31 : 0	DSI_INT_PULSE	Specifies DSI interrupt format: '0': level sensitive; i.e. no pulse generator. '1': pulse generator on rising edge. Default Value: 0

9.1.6 CPUSS_NMI_MODE

DSI NMI pulse mode register

Address: 0x40100028

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							DSI_NMI_PULSE

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	DSI_NMI_PULSE	Specifies DSI NMI format: '0': level sensitive; i.e. no pulse generator. '1': pulse generator on rising edge. Default Value: 0

9.1.7 CPUSS_FLASH_CTL

FLASH control register

Address: 0x40100030

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	None		RW	
HW Access	None			R	None		R	
Name	None [7:5]			PREF_EN	None [3:2]		FLASH_WS [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							RW1C
Name	None [15:9]							FLASH_INVALIDATE

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLASH_INVALIDATE	1': Invalidates the content of the flash controller's buffers. Default Value: 0
4	PREF_EN	Prefetch enable: '0': disabled. This is a desirable seeting when FLASH_WS is "0" or when predictable execution behavior is required. '1': enabled. Default Value: 0
1 : 0	FLASH_WS	Amount of ROM wait states: "0": 0 wait states (fast flash: [0, 24] MHz system frequency, slow flash: [0, 16] MHz system frequency) "1": 1 wait state (fast flash: [24, 48] MHz system frequency, slow flash: [16, 32] MHz system frequency) "2": 2 wait states (slow flash: [32, 48] MHz system frequency) "3": undefined Default Value: 0

9.1.8 CPUSS_ROM_CTL

ROM control register

Address: 0x40100034

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							ROM_WS

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	ROM_WS	Amount of ROM wait states: '0': 0 wait states. Use this setting for newer, faster ROM design. Use this setting for older, slower ROM design and frequencies in the range [0, 24] MHz. '1': 1 wait state. Use this setting for older, slower ROM design and frequencies in the range <24, 48] MHz. CPUSSv2 supports two types of ROM memory: an older, slower design (operating at up to 24 MHz) and a newer, faster design (operating at up to 48 MHz). The older design requires 1 wait state for frequencies above 24 MHz. The newer design never requires wait states. All chips after Street Fighter will use the newer design. As a result, all chips after Street Fighter can always use 0 wait states. Default Value: 0

10 DMA Controller Registers

This section discusses the DMA Controller registers. It lists all the registers in mapping tables, in address order.

10.1 Register Details

Register Name	Address
DMAC_CTL	0x40101000
DMAC_STATUS	0x40101010
DMAC_STATUS_SRC_ADDR	0x40101014
DMAC_STATUS_DST_ADDR	0x40101018
DMAC_STATUS_CH_ACT	0x4010101C
DMAC_CH_CTL0	0x40101080
DMAC_CH_CTL1	0x40101084
DMAC_CH_CTL2	0x40101088
DMAC_CH_CTL3	0x4010108C
DMAC_CH_CTL4	0x40101090
DMAC_CH_CTL5	0x40101094
DMAC_CH_CTL6	0x40101098
DMAC_CH_CTL7	0x4010109C
DMAC_INTR	0x401017F0
DMAC_INTR_SET	0x401017F4
DMAC_INTR_MASK	0x401017F8
DMAC_INTR_MASKED	0x401017FC

10.1.1 DMAC_CTL

Control register

Address: 0x40101000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	ENABLED	None [30:24]						

Bits	Name	Description
31	ENABLED	0': IP is disabled. Non-retainable MMIO registers and logic functionality are reset (retainable MMIO registers are NOT reset): - INTR register is set to "0". - DW/DMA functionality is aborted. - DW/DMA controller input/pending triggers are de-activated. - DW/DMA controller output triggers are de-activated. Disabling the IP has the same effect as an active "rst_sys_act_n" reset in DeepSleep power mode. To prevent a loss of active (pending) DW/DMA triggers when disabling the IP or when transitioning from Active to DeepSleep power mode, the STATUS.ACTIVE and STATUS_CH_ACTIVE.CH fields can be used. Note that most MMIO registers are retainable, and a transition from DeepSleep to Active/Sleep power modes makes the DW/DMA controller operational, and ready to react to DW/DMA input triggers that are activated after the transition. Triggers are Active/Sleep functionality. '1': IP is enabled. Default Value: 0

10.1.2 DMAC_STATUS

Status register

Address: 0x40101010

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None					R		
HW Access	None					W		
Name	None [23:19]					CH_ADDR [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	R		None	R		
HW Access	W	W	W		None	W		
Name	ACTIVE	PING_PONG	PRIO [29:28]		None	STATE [26:24]		

Bits	Name	Description
31	ACTIVE	Specifies if there is a currently active (pending) channel in the data transfer engine: 0: no currently active channel. 1: currently active channel. Default Value: 0
30	PING_PONG	Specifies whether the PING descriptor (0) or PONG descriptor (1) of the channel is currently in use. Default Value: Undefined
29 : 28	PRIO	Specifies the priority of the currently active channel. Default Value: Undefined
26 : 24	STATE	State of the data transfer engine. 0: DEFAULT state. 1: Loading descriptor (SRC, DST, CONTROL and STATUS words). 2: Loading data element from source location. 3: Storing data element to destination location. 4: Storing descriptor (STATUS word). 5: Wait for trigger de-activation. 6: Storing descriptor with error response (STATUS word). Default Value: 0

(continued)

18 : 16	CH_ADDR	Specifies the channel number of the currently active channel. E.g. if we have 32 channels, the channel number address with CH_ADDR_WIDTH is LOG2 (32) = 5, and this field is a 5-bit field. If channel 7 is active, STATUS.ACTIVE is '1' and STATUS.CH_ADDR is "7". Default Value: Undefined
15 : 0	DATA_NR	Specifies the index of the currently active data transfer. This value increases from "0" to CONTROL.DATA_NR. Default Value: Undefined

10.1.3 DMAC_STATUS_SRC_ADDR

Source address status register

Address: 0x40101014

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Base address or current address of source location of currently active channel. The specific address information is cycle dependent. This is field is provided for debug purposes. Functionally, no assumption should be made on whether the base or current address is provided. The specifics of the currently active channel are available through STATUS. Note while reading the STATUS, STATUS_SRC and STATUS_DST registers, the transfer engine may have moved from one active channel to another. Default Value: Undefined

10.1.4 DMAC_STATUS_DST_ADDR

Destination address register

Address: 0x40101018

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Base address or current address of destination location of currently active channel. The specific address information is cycle dependent. This is field is provided for debug purposes. Functionally, no assumption should be made on whether the base or current address is provided. The specifics of the currently active channel are available through STATUS. Note while reading the STATUS, STATUS_SRC and STATUS_DST registers, the transfer engine may have moved from one active channel to another. Default Value: Undefined

10.1.5 DMAC_STATUS_CH_ACT

Channel activation status register

Address: 0x4010101C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	CH [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	CH	Channel activation status. Bit i is associated to channel i, with i = 0, , CH_NR-1. Software reads this field to get information on all actively pending channels (either in pending or in the data transfer engine). Default Value: 0

10.1.6 DMAC_CH_CTL0

Channel control register

Address: 0x40101080

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW		None			
HW Access	RW1C	RW	R		None			
Name	ENABLED	PING_PONG	PRIO [29:28]		None [27:24]			

Bits	Name	Description
31	ENABLED	0: channel disabled. The channels trigger is ignored and the channel cannot be activated. If the activated channel is disabled, the data transfer(s) are aborted. 1: channel enabled. Software sets this field to 1 to enable a specific channel. Hardware sets this field to 0 on erroneous channel behavior (the specific error is specified by STATUS.RESP in the channels descriptor structure). Default Value: 0

(continued)

30	PING_PONG	Each channel has two descriptor structures for double buffering purposes. As the controller operates on one structure, the main CPU can operate on the other structure. The descriptor structures are identified as PING (0) and PONG (1). This field identifies the descriptor structure that is currently in use by the controller. Software sets this field to the desired descriptor structure. Hardware inverts the field value on the completion of a descriptor structure when CONTROL.FLIPPING of the current descriptor structure is set to 1. Each channel has two descriptor structures for double buffering purposes. As the controller operates on one structure, the main CPU can operate on the other structure. The descriptor structures are identified as PING (0) and PONG (1). This field identifies the descriptor structure that is currently in use by the controller. Default Value: 0
29 : 28	PRIO	Channel priority, with 0 representing the highest priority and 3 representing the lowest priority. Priority decoding uses the channel priority to determine the highest priority activated channel. If multiple activated channels have the same highest priority, the channel with the lowest index i, is considered the highest priority activated channel. Default Value: 0

10.1.7 DMAC_CH_CTL1

Channel control register

Address: 0x40101084

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW		None			
HW Access	RW1C	RW	R		None			
Name	ENABLED	PING_PONG	PRIO [29:28]		None [27:24]			

Bits	Name	Description
31	ENABLED	0: channel disabled. The channels trigger is ignored and the channel cannot be activated. If the activated channel is disabled, the data transfer(s) are aborted. 1: channel enabled. Software sets this field to 1 to enable a specific channel. Hardware sets this field to 0 on erroneous channel behavior (the specific error is specified by STATUS.RESP in the channels descriptor structure). Default Value: 0

(continued)

30	PING_PONG	Each channel has two descriptor structures for double buffering purposes. As the controller operates on one structure, the main CPU can operate on the other structure. The descriptor structures are identified as PING (0) and PONG (1). This field identifies the descriptor structure that is currently in use by the controller. Software sets this field to the desired descriptor structure. Hardware inverts the field value on the completion of a descriptor structure when CONTROL.FLIPPING of the current descriptor structure is set to 1. Each channel has two descriptor structures for double buffering purposes. As the controller operates on one structure, the main CPU can operate on the other structure. The descriptor structures are identified as PING (0) and PONG (1). This field identifies the descriptor structure that is currently in use by the controller. Default Value: 0
29 : 28	PRIO	Channel priority, with 0 representing the highest priority and 3 representing the lowest priority. Priority decoding uses the channel priority to determine the highest priority activated channel. If multiple activated channels have the same highest priority, the channel with the lowest index i, is considered the highest priority activated channel. Default Value: 0

10.1.8 DMAC_CH_CTL2

Channel control register

Address: 0x40101088

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW		None			
HW Access	RW1C	RW	R		None			
Name	ENABLED	PING_PONG	PRIO [29:28]		None [27:24]			

Bits	Name	Description
31	ENABLED	0: channel disabled. The channels trigger is ignored and the channel cannot be activated. If the activated channel is disabled, the data transfer(s) are aborted. 1: channel enabled. Software sets this field to 1 to enable a specific channel. Hardware sets this field to 0 on erroneous channel behavior (the specific error is specified by STATUS.RESP in the channels descriptor structure). Default Value: 0

(continued)

30	PING_PONG	Each channel has two descriptor structures for double buffering purposes. As the controller operates on one structure, the main CPU can operate on the other structure. The descriptor structures are identified as PING (0) and PONG (1). This field identifies the descriptor structure that is currently in use by the controller. Software sets this field to the desired descriptor structure. Hardware inverts the field value on the completion of a descriptor structure when CONTROL.FLIPPING of the current descriptor structure is set to 1. Each channel has two descriptor structures for double buffering purposes. As the controller operates on one structure, the main CPU can operate on the other structure. The descriptor structures are identified as PING (0) and PONG (1). This field identifies the descriptor structure that is currently in use by the controller. Default Value: 0
29 : 28	PRIO	Channel priority, with 0 representing the highest priority and 3 representing the lowest priority. Priority decoding uses the channel priority to determine the highest priority activated channel. If multiple activated channels have the same highest priority, the channel with the lowest index i, is considered the highest priority activated channel. Default Value: 0

10.1.9 DMAC_CH_CTL3

Channel control register

Address: 0x4010108C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW		None			
HW Access	RW1C	RW	R		None			
Name	ENABLED	PING_PONG	PRIO [29:28]		None [27:24]			

Bits	Name	Description
31	ENABLED	0: channel disabled. The channels trigger is ignored and the channel cannot be activated. If the activated channel is disabled, the data transfer(s) are aborted. 1: channel enabled. Software sets this field to 1 to enable a specific channel. Hardware sets this field to 0 on erroneous channel behavior (the specific error is specified by STATUS.RESP in the channels descriptor structure). Default Value: 0

(continued)

30	PING_PONG	Each channel has two descriptor structures for double buffering purposes. As the controller operates on one structure, the main CPU can operate on the other structure. The descriptor structures are identified as PING (0) and PONG (1). This field identifies the descriptor structure that is currently in use by the controller. Software sets this field to the desired descriptor structure. Hardware inverts the field value on the completion of a descriptor structure when CONTROL.FLIPPING of the current descriptor structure is set to 1. Each channel has two descriptor structures for double buffering purposes. As the controller operates on one structure, the main CPU can operate on the other structure. The descriptor structures are identified as PING (0) and PONG (1). This field identifies the descriptor structure that is currently in use by the controller. Default Value: 0
29 : 28	PRIO	Channel priority, with 0 representing the highest priority and 3 representing the lowest priority. Priority decoding uses the channel priority to determine the highest priority activated channel. If multiple activated channels have the same highest priority, the channel with the lowest index i, is considered the highest priority activated channel. Default Value: 0

10.1.10 DMAC_CH_CTL4

Channel control register

Address: 0x40101090

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW		None			
HW Access	RW1C	RW	R		None			
Name	ENABLED	PING_PONG	PRIO [29:28]		None [27:24]			

Bits	Name	Description
31	ENABLED	0: channel disabled. The channels trigger is ignored and the channel cannot be activated. If the activated channel is disabled, the data transfer(s) are aborted. 1: channel enabled. Software sets this field to 1 to enable a specific channel. Hardware sets this field to 0 on erroneous channel behavior (the specific error is specified by STATUS.RESP in the channels descriptor structure). Default Value: 0

(continued)

30	PING_PONG	Each channel has two descriptor structures for double buffering purposes. As the controller operates on one structure, the main CPU can operate on the other structure. The descriptor structures are identified as PING (0) and PONG (1). This field identifies the descriptor structure that is currently in use by the controller. Software sets this field to the desired descriptor structure. Hardware inverts the field value on the completion of a descriptor structure when CONTROL.FLIPPING of the current descriptor structure is set to 1. Each channel has two descriptor structures for double buffering purposes. As the controller operates on one structure, the main CPU can operate on the other structure. The descriptor structures are identified as PING (0) and PONG (1). This field identifies the descriptor structure that is currently in use by the controller. Default Value: 0
29 : 28	PRIO	Channel priority, with 0 representing the highest priority and 3 representing the lowest priority. Priority decoding uses the channel priority to determine the highest priority activated channel. If multiple activated channels have the same highest priority, the channel with the lowest index i, is considered the highest priority activated channel. Default Value: 0

10.1.11 DMAC_CH_CTL5

Channel control register

Address: 0x40101094

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW		None			
HW Access	RW1C	RW	R		None			
Name	ENABLED	PING_PONG	PRIO [29:28]		None [27:24]			

Bits	Name	Description
31	ENABLED	0: channel disabled. The channels trigger is ignored and the channel cannot be activated. If the activated channel is disabled, the data transfer(s) are aborted. 1: channel enabled. Software sets this field to 1 to enable a specific channel. Hardware sets this field to 0 on erroneous channel behavior (the specific error is specified by STATUS.RESP in the channels descriptor structure). Default Value: 0

(continued)

30	PING_PONG	Each channel has two descriptor structures for double buffering purposes. As the controller operates on one structure, the main CPU can operate on the other structure. The descriptor structures are identified as PING (0) and PONG (1). This field identifies the descriptor structure that is currently in use by the controller. Software sets this field to the desired descriptor structure. Hardware inverts the field value on the completion of a descriptor structure when CONTROL.FLIPPING of the current descriptor structure is set to 1. Each channel has two descriptor structures for double buffering purposes. As the controller operates on one structure, the main CPU can operate on the other structure. The descriptor structures are identified as PING (0) and PONG (1). This field identifies the descriptor structure that is currently in use by the controller. Default Value: 0
29 : 28	PRIO	Channel priority, with 0 representing the highest priority and 3 representing the lowest priority. Priority decoding uses the channel priority to determine the highest priority activated channel. If multiple activated channels have the same highest priority, the channel with the lowest index i, is considered the highest priority activated channel. Default Value: 0

10.1.12 DMAC_CH_CTL6

Channel control register

Address: 0x40101098

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW		None			
HW Access	RW1C	RW	R		None			
Name	ENABLED	PING_PONG	PRIO [29:28]		None [27:24]			

Bits	Name	Description
31	ENABLED	0: channel disabled. The channels trigger is ignored and the channel cannot be activated. If the activated channel is disabled, the data transfer(s) are aborted. 1: channel enabled. Software sets this field to 1 to enable a specific channel. Hardware sets this field to 0 on erroneous channel behavior (the specific error is specified by STATUS.RESP in the channels descriptor structure). Default Value: 0

(continued)

30	PING_PONG	Each channel has two descriptor structures for double buffering purposes. As the controller operates on one structure, the main CPU can operate on the other structure. The descriptor structures are identified as PING (0) and PONG (1). This field identifies the descriptor structure that is currently in use by the controller. Software sets this field to the desired descriptor structure. Hardware inverts the field value on the completion of a descriptor structure when CONTROL.FLIPPING of the current descriptor structure is set to 1. Each channel has two descriptor structures for double buffering purposes. As the controller operates on one structure, the main CPU can operate on the other structure. The descriptor structures are identified as PING (0) and PONG (1). This field identifies the descriptor structure that is currently in use by the controller. Default Value: 0
29 : 28	PRIO	Channel priority, with 0 representing the highest priority and 3 representing the lowest priority. Priority decoding uses the channel priority to determine the highest priority activated channel. If multiple activated channels have the same highest priority, the channel with the lowest index i, is considered the highest priority activated channel. Default Value: 0

10.1.13 DMAC_CH_CTL7

Channel control register

Address: 0x4010109C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW		None			
HW Access	RW1C	RW	R		None			
Name	ENABLED	PING_PONG	PRIO [29:28]		None [27:24]			

Bits	Name	Description
31	ENABLED	0: channel disabled. The channels trigger is ignored and the channel cannot be activated. If the activated channel is disabled, the data transfer(s) are aborted. 1: channel enabled. Software sets this field to 1 to enable a specific channel. Hardware sets this field to 0 on erroneous channel behavior (the specific error is specified by STATUS.RESP in the channels descriptor structure). Default Value: 0

(continued)

30	PING_PONG	Each channel has two descriptor structures for double buffering purposes. As the controller operates on one structure, the main CPU can operate on the other structure. The descriptor structures are identified as PING (0) and PONG (1). This field identifies the descriptor structure that is currently in use by the controller. Software sets this field to the desired descriptor structure. Hardware inverts the field value on the completion of a descriptor structure when CONTROL.FLIPPING of the current descriptor structure is set to 1. Each channel has two descriptor structures for double buffering purposes. As the controller operates on one structure, the main CPU can operate on the other structure. The descriptor structures are identified as PING (0) and PONG (1). This field identifies the descriptor structure that is currently in use by the controller. Default Value: 0
29 : 28	PRIO	Channel priority, with 0 representing the highest priority and 3 representing the lowest priority. Priority decoding uses the channel priority to determine the highest priority activated channel. If multiple activated channels have the same highest priority, the channel with the lowest index i, is considered the highest priority activated channel. Default Value: 0

10.1.14 DMAC_INTR

Interrupt register

Address: 0x401017F0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C							
HW Access	RW1S							
Name	CH [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	CH	Set to '1', when event is detected. Write INTR field with '1', to clear bit. Write INTR_SET field with '1', to set bit. Default Value: 0

10.1.15 DMAC_INTR_SET

Interrupt set register

Address: 0x401017F4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S							
HW Access	A							
Name	CH [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	CH	Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect). Default Value: 0

10.1.16 DMAC_INTR_MASK

Interrupt mask register

Address: 0x401017F8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CH [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	CH	Mask for corresponding field in INTR register. Default Value: 0

10.1.17 DMAC_INTR_MASKED

Interrupt masked register

Address: 0x401017FC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	CH [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	CH	Logical and of corresponding request and mask fields. Default Value: 0

11 DMA Descriptor Registers

This section discusses the DMA Descriptor registers. It lists all the registers in mapping tables, in address order.

11.1 Register Details

Register Name	Address
DMAC_DESCR0_PING_SRC	0x40101800
DMAC_DESCR0_PING_DST	0x40101804
DMAC_DESCR0_PING_CTL	0x40101808
DMAC_DESCR0_PING_STATUS	0x4010180C
DMAC_DESCR0_PONG_SRC	0x40101810
DMAC_DESCR0_PONG_DST	0x40101814
DMAC_DESCR0_PONG_CTL	0x40101818
DMAC_DESCR0_PONG_STATUS	0x4010181C
DMAC_DESCR1_PING_SRC	0x40101820
DMAC_DESCR1_PING_DST	0x40101824
DMAC_DESCR1_PING_CTL	0x40101828
DMAC_DESCR1_PING_STATUS	0x4010182C
DMAC_DESCR1_PONG_SRC	0x40101830
DMAC_DESCR1_PONG_DST	0x40101834
DMAC_DESCR1_PONG_CTL	0x40101838
DMAC_DESCR1_PONG_STATUS	0x4010183C
DMAC_DESCR2_PING_SRC	0x40101840
DMAC_DESCR2_PING_DST	0x40101844
DMAC_DESCR2_PING_CTL	0x40101848
DMAC_DESCR2_PING_STATUS	0x4010184C
DMAC_DESCR2_PONG_SRC	0x40101850
DMAC_DESCR2_PONG_DST	0x40101854
DMAC_DESCR2_PONG_CTL	0x40101858
DMAC_DESCR2_PONG_STATUS	0x4010185C
DMAC_DESCR3_PING_SRC	0x40101860
DMAC_DESCR3_PING_DST	0x40101864
DMAC_DESCR3_PING_CTL	0x40101868

Register Name	Address
DMAC_DESCR3_PING_STATUS	0x4010186C
DMAC_DESCR3_PONG_SRC	0x40101870
DMAC_DESCR3_PONG_DST	0x40101874
DMAC_DESCR3_PONG_CTL	0x40101878
DMAC_DESCR3_PONG_STATUS	0x4010187C
DMAC_DESCR4_PING_SRC	0x40101880
DMAC_DESCR4_PING_DST	0x40101884
DMAC_DESCR4_PING_CTL	0x40101888
DMAC_DESCR4_PING_STATUS	0x4010188C
DMAC_DESCR4_PONG_SRC	0x40101890
DMAC_DESCR4_PONG_DST	0x40101894
DMAC_DESCR4_PONG_CTL	0x40101898
DMAC_DESCR4_PONG_STATUS	0x4010189C
DMAC_DESCR5_PING_SRC	0x401018A0
DMAC_DESCR5_PING_DST	0x401018A4
DMAC_DESCR5_PING_CTL	0x401018A8
DMAC_DESCR5_PING_STATUS	0x401018AC
DMAC_DESCR5_PONG_SRC	0x401018B0
DMAC_DESCR5_PONG_DST	0x401018B4
DMAC_DESCR5_PONG_CTL	0x401018B8
DMAC_DESCR5_PONG_STATUS	0x401018BC
DMAC_DESCR6_PING_SRC	0x401018C0
DMAC_DESCR6_PING_DST	0x401018C4
DMAC_DESCR6_PING_CTL	0x401018C8
DMAC_DESCR6_PING_STATUS	0x401018CC
DMAC_DESCR6_PONG_SRC	0x401018D0
DMAC_DESCR6_PONG_DST	0x401018D4
DMAC_DESCR6_PONG_CTL	0x401018D8
DMAC_DESCR6_PONG_STATUS	0x401018DC
DMAC_DESCR7_PING_SRC	0x401018E0
DMAC_DESCR7_PING_DST	0x401018E4
DMAC_DESCR7_PING_CTL	0x401018E8
DMAC_DESCR7_PING_STATUS	0x401018EC
DMAC_DESCR7_PONG_SRC	0x401018F0
DMAC_DESCR7_PONG_DST	0x401018F4
DMAC_DESCR7_PONG_CTL	0x401018F8
DMAC_DESCR7_PONG_STATUS	0x401018FC

11.1.1 DMAC_DESCR0_PING_SRC

Ping source address

Address: 0x40101800

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Base address of source location. The effective source location is calculated by adding on offset (derived from PING.STATUS.CURR_DATA_NR) to this base address. Default Value: Undefined

11.1.2 DMAC_DESCR0_PING_DST

Ping destination address

Address: 0x40101804

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Base address of destination location. The effective destination location is calculated by adding on offset (derived from PING.STATUS.CURR_DATA_NR) to this base address. Default Value: Undefined

11.1.3 DMAC_DESCR0_PING_CTL

Ping control word

Address: 0x40101808

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	None		RW	
HW Access	RW	RW	RW	RW	None		RW	
Name	SRC_ADDR_INCR	SRC_TRANSFER_SIZE	DST_ADDR_INCR	DST_TRANSFER_SIZE	None [19:18]		DATA_SIZE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW		RW	RW	RW	RW	RW	
HW Access	RW		RW	RW	RW	RW	RW	
Name	OPCODE [31:30]		FLIPPING	PREEMPT-ABLE	SET_CAUSE	INV_DESCR	WAIT_FOR_DEACT [25:24]	

Bits	Name	Description

(continued)

31 : 30	OPCODE	Specifies the specific data transfer (only when the VALID bit of the descriptors STATUS word is 1): 0: A single trigger initiates a single data element transfer (DW mode). This opcode specifies a transfer of a single data element. The current descriptor is completed when the amount of transferred single data elements equals the programmed buffer size (DATA_NR+1). 1: A single trigger initiates a single descriptor transfer (DMA mode). This opcode specifies a transfer of DATA_NR+1 data elements as specified by the current descriptor structure. The current descriptor is completed when its data transfer is completed. 2: A single trigger initiates a descriptor list transfer (DMA mode). This opcode specifies a transfer of DATA_NR+1 data elements as specified by the current descriptor structure and by successive valid descriptors. The current descriptor is completed when its data transfer is completed. This OPCODE relies on FLIPPING to be set to '1', such that the CHi_CTL.PING_PONG field is flipped/inverted and the successive descriptor is used. This continues for as long as the successive descriptor is valid. Note that as the HW is using the PING/PONG descriptor, the SW can prepare the alternate PONG/PING descriptor. The interrupt mechanism is used by HW to convey to the SW that the current descriptor is completed (and can be prepared for a successive transfer). After completerion of the opcode (and waiting for de-activation, the channel's output trigger is activated). Default Value: Undefined
29	FLIPPING	1: On completion of the current descriptor structure, the current descriptor identifier CHi_CTL.PING_PONG is flipped/inverted. In DMA mode, descriptor list transfer, flipping of the current descriptor identifier can be used to construct a linked list of descriptor structures. Default Value: Undefined
28	PREEMPTABLE	1: Transfer is preemptable. In DMA mode (OPCODE is 1 or 2), multi data element transfers are constructed out of multiple single data element load (from the source location) and store (to the destination location) sequences. This field allows higher priority activated channels to preempt the current transfer in between these atomic (load, store) sequences. Preemption will NOT deactivate the current channel. As a result, after completion of a higher priority activated channel, the current channel is rescheduled. Default Value: Undefined
27	SET_CAUSE	1: On completion of the current descriptor structure, the interrupt cause field of the channel is set to 1 (INTR.CH[i]). Default Value: Undefined
26	INV_DESCR	1: On completion of the current descriptor structure, the VALID bit of the descriptors STATUS word is set to 0. Default Value: Undefined

(continued)

25 : 24	WAIT_FOR_DEACT	Specifies whether the data transfer engine should wait for the channel to be deactivated; i.e. the selected system trigger is not active. This field is used to synchronize the controllers data transfer(s) with the agent that generated the trigger. This field is ONLY used at the completion of an opcode. E.g., a FIFO indicates that it is empty and it needs a new data sample. The agent removes the trigger ONLY when the data sample has been written by the transfer engine AND received by the agent. Furthermore, the agents trigger may be delayed by a few cycles before it reaches the DW/DMA controller. This field is used for level sensitive trigger, which reflect state (pulse sensitive triggers should have this field set to "0"). The wait cycles incurred by this field reduce DW/DMA controller performance. 0: Do not wait for de-activation (for pulse sensitive triggers). 1: Wait for up to 4 cycles. 2: Wait for up to 8 cycles. 3: Wait indefinitely. This option may result in DW/DMA controller lockup if the system trigger is not de-activated by the source agent. Default Value: Undefined
23	SRC_ADDR_INCR	Specifies whether the source location address is incremented by the SRC_TRANSFER_SIZE after each single data element transfer or not. 0: No increment, typically used for receive (RX) FIFO structures. 1: Increment, typically used for memory structures. Default Value: Undefined
22	SRC_TRANSFER_SIZE	Specifies the bus transfer size to the source location: 0: As specified by DATA_SIZE. 1: Word (32 bits). Distinguishing bus transfer size from data element size allows for source components with data elements that are smaller than their 32-bit bus interface width. E.g., an ADC source has a 32-bit bus transfer size, but only provides a 16-bit data element. Default Value: Undefined
21	DST_ADDR_INCR	Specifies whether the destination location address is incremented by the DST_TRANSFER_SIZE after each single data element transfer or not. 0 : No increment, typically used for transmit (TX) FIFO structures. 1: Increment, typically used for memory structures. Default Value: Undefined
20	DST_TRANSFER_SIZE	Specifies the bus transfer size to the destination location: 0: As specified by DATA_SIZE. 1: Word (32 bits). Distinguishing bus transfer size from data element size allows for destination components with data elements that are smaller than their 32-bit bus interface width. E.g., a DAC destination has a 32-bit bus transfer size, but only requires a 16-bit data element. Default Value: Undefined

(continued)

17 : 16	DATA_SIZE	Specifies the data element size: 0: Byte (8 bits). 1: Halfword (16 bits). 2: Word (32 bits). DATA_SIZE, SRC_TRANSFER_SIZE and DST_TRANSFER_SIZE together determine how data elements are transferred. The following are the 9 legal settings: - DATA is 8 bit, SRC is 8 bit, DST is 8 bit - DATA is 8 bit, SRC is 32 bit (higher 24 bits are dropped), DST is 8 bit - DATA is 8 bit, SRC is 8 bit, DST is 32 bit (higher 24 bits are made 0) - DATA is 8 bit, SRC is 32 bit (higher 24 bits are dropped), DST is 32 bit (higher 24 bits are made 0) - DATA is 16 bit, SRC is 16 bit, DST is 16 bit - DATA is 16 bit, SRC is 32 bit (higher 16 bits are dropped), DST is 16 bit - DATA is 16 bit, SRC is 16 bit, DST is 32 bit (higher 16 bits are made 0) - DATA is 16 bit, SRC is 32 bit (higher 16 bits are dropped), DST is 32 bit (higher 16 bits are made 0) - DATA is 32 bit, SRC is 32 bit, DST is 32 bit Default Value: Undefined
15 : 0	DATA_NR	Number of data elements that are transferred by a single descriptor. In DW mode (OPCODE is 0) each trigger initiates the transfer of a single data element. This field specifies the source and/or destination buffer size in data elements: buffer size = DATA_NR+1. The buffer is typically associated to a memory structure. In DMA mode (OPCODE is 1 or 2) each trigger initiates the transfer of DATA_NR+1 data elements. Default Value: Undefined

11.1.4 DMAC_DESCR0_PING_STATUS

Ping status word

Address: 0x4010180C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None					RW		
HW Access	None					RW		
Name	None [23:19]					RESPONSE [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	RW	None						
Name	VALID	None [30:24]						

Bits	Name	Description
31	VALID	0: Invalid, cannot be used for a data transfer. An attempt to use this descriptor for a data transfer will result in an INVALID_DESCR response code (and the interrupt cause bit is set to 1). 1: Valid. Hardware set this field to 0 when a descriptor is done, but only if CONTROL.INV_DESCR is 1. Software sets this field to 1 when a descriptor is initialized. Default Value: Undefined

(continued)

18 : 16	RESPONSE	Response code (the first two codes NO_ERROR and DONE are the result of normal behavior, the other codes are the result of erroneous behavior). 0/NO_ERROR: No error. Setting this response does NOT set the interrupt cause bit to 1. STATUS.VALID is NOT affected. CHi_CTL.ENABLED is NOT affected. CHi_CTL.PING_PONG is not updated. This response is used for an unused or not completed descriptor. Software should set the RESPONSE field to 0/NO_ERROR during descriptor initialization. 1/DONE: Descriptor is done (without errors). Setting this response sets the interrupt cause bit to 1 if CONTROL.SET_CAUSE is 1. STATUS.VALID is set to 0 if CONTROL.INV_DESCR is 1. CHi_CTL.ENABLED is NOT affected. CHi_CTL.PING_PONG is updated if CONTROL.FLIPPING is 1. 2/SRC_BUS_ERROR: Bus error while loading data from the source location. Setting this response sets the interrupt cause bit to 1. STATUS.VALID is set 0. CHi_CTL.ENABLED is set to 0. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). 3/DST_BUS_ERROR: Bus error while storing data to the destination location. Setting this response sets the interrupt cause bit to 1. STATUS.VALID is set 0. CHi_CTL.ENABLED is set to 0. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). 4/SRC_MISAL: Misalignment of source address. This occurs on a 16-bit bus transfer that is not 2-byte aligned or on a 32-bit bus transfer that is not 4-byte aligned. Setting this response sets the interrupt cause bit to 1. STATUS.VALID is set 0. CHi_CTL.ENABLED is set to 0. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). 5/DST_MISAL: Misalignment of destination address. This occurs on a 16-bit bus transfer that is not 2-byte aligned or on a 32-bit bus transfer that is not 4-byte aligned. Setting this response sets the interrupt cause bit to 1. STATUS.VALID is set 0. CHi_CTL.ENABLED is set to 0. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). 6/INVALID_DESCR: Invalid descriptor (STATUS.VALID is 0). This occurs when an activated channel has an invalid descriptor. CHi_CTL.ENABLED is set to 0. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). Default Value: Undefined
15 : 0	CURR_DATA_NR	Specifies the index of the current data transfer. This value increases from 0 to CONTROL.DATA_NR. HW sets this field: - When a descriptor is done (RESPONSE is DONE), the field is set to "0" when PING_CTL.INV_DESCR is '0' and the field is set to PING_CTL.DATA_NR when PING_CTL.INV_DESCR is '1'. - When a descriptor is not done (RESPONSE is NO_ERROR), the field reflects the progress of a data transfer. - In case of erroneous behavior (RESPONSE is neither DONE or NO_ERROR), the field is not updated, but keeps its value to ease debugging. HW only modifies this field for an active descriptor (STATUS.VALID to be 1). At descriptor initialization, SW should set this field to 0. This field allows software to read the progress of the data transfer. Note that SRC.ADDR and DST.ADDR represent base addresses and are not modified during data transfer. However, STATUS.CURR_DATA_NR is modified during data transfer and provides an offset wrt. the base addresses. Default Value: Undefined

11.1.5 DMAC_DESCR0_PONG_SRC

Pong source address

Address: 0x40101810

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	See description of PING_SRC. Default Value: Undefined

11.1.6 DMAC_DESCR0_PONG_DST

Pong destination address

Address: 0x40101814

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	See description of PING_DST. Default Value: Undefined

11.1.7 DMAC_DESCR0_PONG_CTL

Pong control word

Address: 0x40101818

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	None		RW	
HW Access	RW	RW	RW	RW	None		RW	
Name	SRC_ADDR_INCR	SRC_TRANSFER_SIZE	DST_ADDR_INCR	DST_TRANSFER_SIZE	None [19:18]		DATA_SIZE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW		RW	RW	RW	RW	RW	
HW Access	RW		RW	RW	RW	RW	RW	
Name	OPCODE [31:30]		FLIPPING	PREEMPT-ABLE	SET_CAUSE	INV_DESCR	WAIT_FOR_DEACT [25:24]	

Bits	Name	Description
31 : 30	OPCODE	See description of PING_CTL. Default Value: Undefined
29	FLIPPING	See description of PING_CTL. Default Value: Undefined
28	PREEMPTABLE	See description of PING_CTL. Default Value: Undefined
27	SET_CAUSE	See description of PING_CTL. Default Value: Undefined
26	INV_DESCR	See description of PING_CTL. Default Value: Undefined
25 : 24	WAIT_FOR_DEACT	See description of PING_CTL. Default Value: Undefined
23	SRC_ADDR_INCR	See description of PING_CTL. Default Value: Undefined

(continued)

22	SRC_TRANSFER_SIZE	See description of PING_CTL. Default Value: Undefined
21	DST_ADDR_INCR	See description of PING_CTL. Default Value: Undefined
20	DST_TRANSFER_SIZE	See description of PING_CTL. Default Value: Undefined
17 : 16	DATA_SIZE	See description of PING_CTL. Default Value: Undefined
15 : 0	DATA_NR	See description of PING_CTL. Default Value: Undefined

11.1.8 DMAC_DESCR0_PONG_STATUS

Pong status word

Address: 0x4010181C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None					RW		
HW Access	None					RW		
Name	None [23:19]					RESPONSE [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	RW	None						
Name	VALID	None [30:24]						

Bits	Name	Description
31	VALID	See description of PING_STATUS. Default Value: Undefined
18 : 16	RESPONSE	See description of PING_STATUS. Default Value: Undefined
15 : 0	CURR_DATA_NR	See description of PING_STATUS. Default Value: Undefined

11.1.9 DMAC_DESCR1_PING_SRC

Ping source address

Address: 0x40101820

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Base address of source location. The effective source location is calculated by adding on offset (derived from PING.STATUS.CURR_DATA_NR) to this base address. Default Value: Undefined

11.1.10 DMAC_DESCR1_PING_DST

Ping destination address

Address: 0x40101824

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Base address of destination location. The effective destination location is calculated by adding on offset (derived from PING.STATUS.CURR_DATA_NR) to this base address. Default Value: Undefined

11.1.11 DMAC_DESCR1_PING_CTL

Ping control word

Address: 0x40101828

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	None		RW	
HW Access	RW	RW	RW	RW	None		RW	
Name	SRC_ADDR_INCR	SRC_TRANSFER_SIZE	DST_ADDR_INCR	DST_TRANSFER_SIZE	None [19:18]		DATA_SIZE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW		RW	RW	RW	RW	RW	
HW Access	RW		RW	RW	RW	RW	RW	
Name	OPCODE [31:30]		FLIPPING	PREEMPT-ABLE	SET_CAUSE	INV_DESCR	WAIT_FOR_DEACT [25:24]	

Bits	Name	Description

(continued)

31 : 30	OPCODE	Specifies the specific data transfer (only when the VALID bit of the descriptors STATUS word is 1): 0: A single trigger initiates a single data element transfer (DW mode). This opcode specifies a transfer of a single data element. The current descriptor is completed when the amount of transferred single data elements equals the programmed buffer size (DATA_NR+1). 1: A single trigger initiates a single descriptor transfer (DMA mode). This opcode specifies a transfer of DATA_NR+1 data elements as specified by the current descriptor structure. The current descriptor is completed when its data transfer is completed. 2: A single trigger initiates a descriptor list transfer (DMA mode). This opcode specifies a transfer of DATA_NR+1 data elements as specified by the current descriptor structure and by successive valid descriptors. The current descriptor is completed when its data transfer is completed. This OPCODE relies on FLIPPING to be set to '1', such that the CHi_CTL.PING_PONG field is flipped/inverted and the successive descriptor is used. This continues for as long as the successive descriptor is valid. Note that as the HW is using the PING/PONG descriptor, the SW can prepare the alternate PONG/PING descriptor. The interrupt mechanism is used by HW to convey to the SW that the current descriptor is completed (and can be prepared for a successive transfer). After completerion of the opcode (and waiting for de-activation, the channel's output trigger is activated). Default Value: Undefined
29	FLIPPING	1: On completion of the current descriptor structure, the current descriptor identifier CHi_CTL.PING_PONG is flipped/inverted. In DMA mode, descriptor list transfer, flipping of the current descriptor identifier can be used to construct a linked list of descriptor structures. Default Value: Undefined
28	PREEMPTABLE	1: Transfer is preemptable. In DMA mode (OPCODE is 1 or 2), multi data element transfers are constructed out of multiple single data element load (from the source location) and store (to the destination location) sequences. This field allows higher priority activated channels to preempt the current transfer in between these atomic (load, store) sequences. Preemption will NOT deactivate the current channel. As a result, after completion of a higher priority activated channel, the current channel is rescheduled. Default Value: Undefined
27	SET_CAUSE	1: On completion of the current descriptor structure, the interrupt cause field of the channel is set to 1 (INTR.CH[i]). Default Value: Undefined
26	INV_DESCR	1: On completion of the current descriptor structure, the VALID bit of the descriptors STATUS word is set to 0. Default Value: Undefined

(continued)

25 : 24	WAIT_FOR_DEACT	Specifies whether the data transfer engine should wait for the channel to be deactivated; i.e. the selected system trigger is not active. This field is used to synchronize the controllers data transfer(s) with the agent that generated the trigger. This field is ONLY used at the completion of an opcode. E.g., a FIFO indicates that it is empty and it needs a new data sample. The agent removes the trigger ONLY when the data sample has been written by the transfer engine AND received by the agent. Furthermore, the agents trigger may be delayed by a few cycles before it reaches the DW/DMA controller. This field is used for level sensitive trigger, which reflect state (pulse sensitive triggers should have this field set to "0"). The wait cycles incurred by this field reduce DW/DMA controller performance. 0: Do not wait for de-activation (for pulse sensitive triggers). 1: Wait for up to 4 cycles. 2: Wait for up to 8 cycles. 3: Wait indefinitely. This option may result in DW/DMA controller lockup if the system trigger is not de-activated by the source agent. Default Value: Undefined
23	SRC_ADDR_INCR	Specifies whether the source location address is incremented by the SRC_TRANSFER_SIZE after each single data element transfer or not. 0: No increment, typically used for receive (RX) FIFO structures. 1: Increment, typically used for memory structures. Default Value: Undefined
22	SRC_TRANSFER_SIZE	Specifies the bus transfer size to the source location: 0: As specified by DATA_SIZE. 1: Word (32 bits). Distinguishing bus transfer size from data element size allows for source components with data elements that are smaller than their 32-bit bus interface width. E.g., an ADC source has a 32-bit bus transfer size, but only provides a 16-bit data element. Default Value: Undefined
21	DST_ADDR_INCR	Specifies whether the destination location address is incremented by the DST_TRANSFER_SIZE after each single data element transfer or not. 0 : No increment, typically used for transmit (TX) FIFO structures. 1: Increment, typically used for memory structures. Default Value: Undefined
20	DST_TRANSFER_SIZE	Specifies the bus transfer size to the destination location: 0: As specified by DATA_SIZE. 1: Word (32 bits). Distinguishing bus transfer size from data element size allows for destination components with data elements that are smaller than their 32-bit bus interface width. E.g., a DAC destination has a 32-bit bus transfer size, but only requires a 16-bit data element. Default Value: Undefined

(continued)

17 : 16	DATA_SIZE	Specifies the data element size: 0: Byte (8 bits). 1: Halfword (16 bits). 2: Word (32 bits). DATA_SIZE, SRC_TRANSFER_SIZE and DST_TRANSFER_SIZE together determine how data elements are transferred. The following are the 9 legal settings: - DATA is 8 bit, SRC is 8 bit, DST is 8 bit - DATA is 8 bit, SRC is 32 bit (higher 24 bits are dropped), DST is 8 bit - DATA is 8 bit, SRC is 8 bit, DST is 32 bit (higher 24 bits are made 0) - DATA is 8 bit, SRC is 32 bit (higher 24 bits are dropped), DST is 32 bit (higher 24 bits are made 0) - DATA is 16 bit, SRC is 16 bit, DST is 16 bit - DATA is 16 bit, SRC is 32 bit (higher 16 bits are dropped), DST is 16 bit - DATA is 16 bit, SRC is 16 bit, DST is 32 bit (higher 16 bits are made 0) - DATA is 16 bit, SRC is 32 bit (higher 16 bits are dropped), DST is 32 bit (higher 16 bits are made 0) - DATA is 32 bit, SRC is 32 bit, DST is 32 bit Default Value: Undefined
15 : 0	DATA_NR	Number of data elements that are transferred by a single descriptor. In DW mode (OPCODE is 0) each trigger initiates the transfer of a single data element. This field specifies the source and/or destination buffer size in data elements: buffer size = DATA_NR+1. The buffer is typically associated to a memory structure. In DMA mode (OPCODE is 1 or 2) each trigger initiates the transfer of DATA_NR+1 data elements. Default Value: Undefined

11.1.12 DMAC_DESCR1_PING_STATUS

Ping status word

Address: 0x4010182C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None					RW		
HW Access	None					RW		
Name	None [23:19]					RESPONSE [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	RW	None						
Name	VALID	None [30:24]						

Bits	Name	Description
31	VALID	0: Invalid, cannot be used for a data transfer. An attempt to use this descriptor for a data transfer will result in an INVALID_DESCR response code (and the interrupt cause bit is set to 1). 1: Valid. Hardware set this field to 0 when a descriptor is done, but only if CONTROL.INV_DESCR is 1. Software sets this field to 1 when a descriptor is initialized. Default Value: Undefined

(continued)

18 : 16	RESPONSE	Response code (the first two codes NO_ERROR and DONE are the result of normal behavior, the other codes are the result of erroneous behavior). 0/NO_ERROR: No error. Setting this response does NOT set the interrupt cause bit to 1. STATUS.VALID is NOT affected. CHi_CTL.ENABLED is NOT affected. CHi_CTL.PING_PONG is not updated. This response is used for an unused or not completed descriptor. Software should set the RESPONSE field to 0/NO_ERROR during descriptor initialization. 1/DONE: Descriptor is done (without errors). Setting this response sets the interrupt cause bit to 1 if CONTROL.SET_CAUSE is 1. STATUS.VALID is set to 0 if CONTROL.INV_DESCR is 1. CHi_CTL.ENABLED is NOT affected. CHi_CTL.PING_PONG is updated if CONTROL.FLIPPING is 1. 2/SRC_BUS_ERROR: Bus error while loading data from the source location. Setting this response sets the interrupt cause bit to 1. STATUS.VALID is set 0. CHi_CTL.ENABLED is set to 0. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). 3/DST_BUS_ERROR: Bus error while storing data to the destination location. Setting this response sets the interrupt cause bit to 1. STATUS.VALID is set 0. CHi_CTL.ENABLED is set to 0. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). 4/SRC_MISAL: Misalignment of source address. This occurs on a 16-bit bus transfer that is not 2-byte aligned or on a 32-bit bus transfer that is not 4-byte aligned. Setting this response sets the interrupt cause bit to 1. STATUS.VALID is set 0. CHi_CTL.ENABLED is set to 0. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). 5/DST_MISAL: Misalignment of destination address. This occurs on a 16-bit bus transfer that is not 2-byte aligned or on a 32-bit bus transfer that is not 4-byte aligned. Setting this response sets the interrupt cause bit to 1. STATUS.VALID is set 0. CHi_CTL.ENABLED is set to 0. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). 6/INVALID_DESCR: Invalid descriptor (STATUS.VALID is 0). This occurs when an activated channel has an invalid descriptor. CHi_CTL.ENABLED is set to 0. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). Default Value: Undefined
15 : 0	CURR_DATA_NR	Specifies the index of the current data transfer. This value increases from 0 to CONTROL.DATA_NR. HW sets this field: - When a descriptor is done (RESPONSE is DONE), the field is set to "0" when PING_CTL.INV_DESCR is '0' and the field is set to PING_CTL.DATA_NR when PING_CTL.INV_DESCR is '1'. - When a descriptor is not done (RESPONSE is NO_ERROR), the field reflects the progress of a data transfer. - In case of erroneous behavior (RESPONSE is neither DONE or NO_ERROR), the field is not updated, but keeps its value to ease debugging. HW only modifies this field for an active descriptor (STATUS.VALID to be 1). At descriptor initialization, SW should set this field to 0. This field allows software to read the progress of the data transfer. Note that SRC.ADDR and DST.ADDR represent base addresses and are not modified during data transfer. However, STATUS.CURR_DATA_NR is modified during data transfer and provides an offset wrt. the base addresses. Default Value: Undefined

11.1.13 DMAC_DESCR1_PONG_SRC

Pong source address

Address: 0x40101830

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	See description of PING_SRC. Default Value: Undefined

11.1.14 DMAC_DESCR1_PONG_DST

Pong destination address

Address: 0x40101834

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	See description of PING_DST. Default Value: Undefined

11.1.15 DMAC_DESCR1_PONG_CTL

Pong control word

Address: 0x40101838

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	None		RW	
HW Access	RW	RW	RW	RW	None		RW	
Name	SRC_ADDR_INCR	SRC_TRANSFER_SIZE	DST_ADDR_INCR	DST_TRANSFER_SIZE	None [19:18]		DATA_SIZE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW		RW	RW	RW	RW	RW	
HW Access	RW		RW	RW	RW	RW	RW	
Name	OPCODE [31:30]		FLIPPING	PREEMPT-ABLE	SET_CAUSE	INV_DESCR	WAIT_FOR_DEACT [25:24]	

Bits	Name	Description
31 : 30	OPCODE	See description of PING_CTL. Default Value: Undefined
29	FLIPPING	See description of PING_CTL. Default Value: Undefined
28	PREEMPTABLE	See description of PING_CTL. Default Value: Undefined
27	SET_CAUSE	See description of PING_CTL. Default Value: Undefined
26	INV_DESCR	See description of PING_CTL. Default Value: Undefined
25 : 24	WAIT_FOR_DEACT	See description of PING_CTL. Default Value: Undefined
23	SRC_ADDR_INCR	See description of PING_CTL. Default Value: Undefined

(continued)

22	SRC_TRANSFER_SIZE	See description of PING_CTL. Default Value: Undefined
21	DST_ADDR_INCR	See description of PING_CTL. Default Value: Undefined
20	DST_TRANSFER_SIZE	See description of PING_CTL. Default Value: Undefined
17 : 16	DATA_SIZE	See description of PING_CTL. Default Value: Undefined
15 : 0	DATA_NR	See description of PING_CTL. Default Value: Undefined

11.1.16 DMAC_DESCR1_PONG_STATUS

Pong status word

Address: 0x4010183C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None					RW		
HW Access	None					RW		
Name	None [23:19]					RESPONSE [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	RW	None						
Name	VALID	None [30:24]						

Bits	Name	Description
31	VALID	See description of PING_STATUS. Default Value: Undefined
18 : 16	RESPONSE	See description of PING_STATUS. Default Value: Undefined
15 : 0	CURR_DATA_NR	See description of PING_STATUS. Default Value: Undefined

11.1.17 DMAC_DESCR2_PING_SRC

Ping source address

Address: 0x40101840

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Base address of source location. The effective source location is calculated by adding on offset (derived from PING.STATUS.CURR_DATA_NR) to this base address. Default Value: Undefined

11.1.18 DMAC_DESCR2_PING_DST

Ping destination address

Address: 0x40101844

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Base address of destination location. The effective destination location is calculated by adding on offset (derived from PING.STATUS.CURR_DATA_NR) to this base address. Default Value: Undefined

11.1.19 DMAC_DESCR2_PING_CTL

Ping control word

Address: 0x40101848

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	None		RW	
HW Access	RW	RW	RW	RW	None		RW	
Name	SRC_ADDR_INCR	SRC_TRANSFER_SIZE	DST_ADDR_INCR	DST_TRANSFER_SIZE	None [19:18]		DATA_SIZE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW		RW	RW	RW	RW	RW	
HW Access	RW		RW	RW	RW	RW	RW	
Name	OPCODE [31:30]		FLIPPING	PREEMPT-ABLE	SET_CAUSE	INV_DESCR	WAIT_FOR_DEACT [25:24]	

Bits	Name	Description

(continued)

31 : 30	OPCODE	Specifies the specific data transfer (only when the VALID bit of the descriptors STATUS word is 1): 0: A single trigger initiates a single data element transfer (DW mode). This opcode specifies a transfer of a single data element. The current descriptor is completed when the amount of transferred single data elements equals the programmed buffer size (DATA_NR+1). 1: A single trigger initiates a single descriptor transfer (DMA mode). This opcode specifies a transfer of DATA_NR+1 data elements as specified by the current descriptor structure. The current descriptor is completed when its data transfer is completed. 2: A single trigger initiates a descriptor list transfer (DMA mode). This opcode specifies a transfer of DATA_NR+1 data elements as specified by the current descriptor structure and by successive valid descriptors. The current descriptor is completed when its data transfer is completed. This OPCODE relies on FLIPPING to be set to '1', such that the CHi_CTL.PING_PONG field is flipped/inverted and the successive descriptor is used. This continues for as long as the successive descriptor is valid. Note that as the HW is using the PING/PONG descriptor, the SW can prepare the alternate PONG/PING descriptor. The interrupt mechanism is used by HW to convey to the SW that the current descriptor is completed (and can be prepared for a successive transfer). After completerion of the opcode (and waiting for de-activation, the channel's output trigger is activated). Default Value: Undefined
29	FLIPPING	1: On completion of the current descriptor structure, the current descriptor identifier CHi_CTL.PING_PONG is flipped/inverted. In DMA mode, descriptor list transfer, flipping of the current descriptor identifier can be used to construct a linked list of descriptor structures. Default Value: Undefined
28	PREEMPTABLE	1: Transfer is preemptable. In DMA mode (OPCODE is 1 or 2), multi data element transfers are constructed out of multiple single data element load (from the source location) and store (to the destination location) sequences. This field allows higher priority activated channels to preempt the current transfer in between these atomic (load, store) sequences. Preemption will NOT deactivate the current channel. As a result, after completion of a higher priority activated channel, the current channel is rescheduled. Default Value: Undefined
27	SET_CAUSE	1: On completion of the current descriptor structure, the interrupt cause field of the channel is set to 1 (INTR.CH[i]). Default Value: Undefined
26	INV_DESCR	1: On completion of the current descriptor structure, the VALID bit of the descriptors STATUS word is set to 0. Default Value: Undefined

(continued)

25 : 24	WAIT_FOR_DEACT	Specifies whether the data transfer engine should wait for the channel to be deactivated; i.e. the selected system trigger is not active. This field is used to synchronize the controllers data transfer(s) with the agent that generated the trigger. This field is ONLY used at the completion of an opcode. E.g., a FIFO indicates that it is empty and it needs a new data sample. The agent removes the trigger ONLY when the data sample has been written by the transfer engine AND received by the agent. Furthermore, the agents trigger may be delayed by a few cycles before it reaches the DW/DMA controller. This field is used for level sensitive trigger, which reflect state (pulse sensitive triggers should have this field set to "0"). The wait cycles incurred by this field reduce DW/DMA controller performance. 0: Do not wait for de-activation (for pulse sensitive triggers). 1: Wait for up to 4 cycles. 2: Wait for up to 8 cycles. 3: Wait indefinitely. This option may result in DW/DMA controller lockup if the system trigger is not de-activated by the source agent. Default Value: Undefined
23	SRC_ADDR_INCR	Specifies whether the source location address is incremented by the SRC_TRANSFER_SIZE after each single data element transfer or not. 0: No increment, typically used for receive (RX) FIFO structures. 1: Increment, typically used for memory structures. Default Value: Undefined
22	SRC_TRANSFER_SIZE	Specifies the bus transfer size to the source location: 0: As specified by DATA_SIZE. 1: Word (32 bits). Distinguishing bus transfer size from data element size allows for source components with data elements that are smaller than their 32-bit bus interface width. E.g., an ADC source has a 32-bit bus transfer size, but only provides a 16-bit data element. Default Value: Undefined
21	DST_ADDR_INCR	Specifies whether the destination location address is incremented by the DST_TRANSFER_SIZE after each single data element transfer or not. 0 : No increment, typically used for transmit (TX) FIFO structures. 1: Increment, typically used for memory structures. Default Value: Undefined
20	DST_TRANSFER_SIZE	Specifies the bus transfer size to the destination location: 0: As specified by DATA_SIZE. 1: Word (32 bits). Distinguishing bus transfer size from data element size allows for destination components with data elements that are smaller than their 32-bit bus interface width. E.g., a DAC destination has a 32-bit bus transfer size, but only requires a 16-bit data element. Default Value: Undefined

(continued)

17 : 16	DATA_SIZE	Specifies the data element size: 0: Byte (8 bits). 1: Halfword (16 bits). 2: Word (32 bits). DATA_SIZE, SRC_TRANSFER_SIZE and DST_TRANSFER_SIZE together determine how data elements are transferred. The following are the 9 legal settings: - DATA is 8 bit, SRC is 8 bit, DST is 8 bit - DATA is 8 bit, SRC is 32 bit (higher 24 bits are dropped), DST is 8 bit - DATA is 8 bit, SRC is 8 bit, DST is 32 bit (higher 24 bits are made 0) - DATA is 8 bit, SRC is 32 bit (higher 24 bits are dropped), DST is 32 bit (higher 24 bits are made 0) - DATA is 16 bit, SRC is 16 bit, DST is 16 bit - DATA is 16 bit, SRC is 32 bit (higher 16 bits are dropped), DST is 16 bit - DATA is 16 bit, SRC is 16 bit, DST is 32 bit (higher 16 bits are made 0) - DATA is 16 bit, SRC is 32 bit (higher 16 bits are dropped), DST is 32 bit (higher 16 bits are made 0) - DATA is 32 bit, SRC is 32 bit, DST is 32 bit Default Value: Undefined
15 : 0	DATA_NR	Number of data elements that are transferred by a single descriptor. In DW mode (OPCODE is 0) each trigger initiates the transfer of a single data element. This field specifies the source and/or destination buffer size in data elements: buffer size = DATA_NR+1. The buffer is typically associated to a memory structure. In DMA mode (OPCODE is 1 or 2) each trigger initiates the transfer of DATA_NR+1 data elements. Default Value: Undefined

11.1.20 DMAC_DESCR2_PING_STATUS

Ping status word

Address: 0x4010184C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None					RW		
HW Access	None					RW		
Name	None [23:19]					RESPONSE [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	RW	None						
Name	VALID	None [30:24]						

Bits	Name	Description
31	VALID	0: Invalid, cannot be used for a data transfer. An attempt to use this descriptor for a data transfer will result in an INVALID_DESCR response code (and the interrupt cause bit is set to 1). 1: Valid. Hardware set this field to 0 when a descriptor is done, but only if CONTROL.INV_DESCR is 1. Software sets this field to 1 when a descriptor is initialized. Default Value: Undefined

(continued)

18 : 16	RESPONSE	Response code (the first two codes NO_ERROR and DONE are the result of normal behavior, the other codes are the result of erroneous behavior). 0/NO_ERROR: No error. Setting this response does NOT set the interrupt cause bit to 1. STATUS.VALID is NOT affected. CHi_CTL.ENABLED is NOT affected. CHi_CTL.PING_PONG is not updated. This response is used for an unused or not completed descriptor. Software should set the RESPONSE field to 0/NO_ERROR during descriptor initialization. 1/DONE: Descriptor is done (without errors). Setting this response sets the interrupt cause bit to 1 if CONTROL.SET_CAUSE is 1. STATUS.VALID is set to 0 if CONTROL.INV_DESCR is 1. CHi_CTL.ENABLED is NOT affected. CHi_CTL.PING_PONG is updated if CONTROL.FLIPPING is 1. 2/SRC_BUS_ERROR: Bus error while loading data from the source location. Setting this response sets the interrupt cause bit to 1. STATUS.VALID is set 0. CHi_CTL.ENABLED is set to 0. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). 3/DST_BUS_ERROR: Bus error while storing data to the destination location. Setting this response sets the interrupt cause bit to 1. STATUS.VALID is set 0. CHi_CTL.ENABLED is set to 0. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). 4/SRC_MISAL: Misalignment of source address. This occurs on a 16-bit bus transfer that is not 2-byte aligned or on a 32-bit bus transfer that is not 4-byte aligned. Setting this response sets the interrupt cause bit to 1. STATUS.VALID is set 0. CHi_CTL.ENABLED is set to 0. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). 5/DST_MISAL: Misalignment of destination address. This occurs on a 16-bit bus transfer that is not 2-byte aligned or on a 32-bit bus transfer that is not 4-byte aligned. Setting this response sets the interrupt cause bit to 1. STATUS.VALID is set 0. CHi_CTL.ENABLED is set to 0. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). 6/INVALID_DESCR: Invalid descriptor (STATUS.VALID is 0). This occurs when an activated channel has an invalid descriptor. CHi_CTL.ENABLED is set to 0. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). Default Value: Undefined
15 : 0	CURR_DATA_NR	Specifies the index of the current data transfer. This value increases from 0 to CONTROL.DATA_NR. HW sets this field: - When a descriptor is done (RESPONSE is DONE), the field is set to "0" when PING_CTL.INV_DESCR is '0' and the field is set to PING_CTL.DATA_NR when PING_CTL.INV_DESCR is '1'. - When a descriptor is not done (RESPONSE is NO_ERROR), the field reflects the progress of a data transfer. - In case of erroneous behavior (RESPONSE is neither DONE or NO_ERROR), the field is not updated, but keeps its value to ease debugging. HW only modifies this field for an active descriptor (STATUS.VALID to be 1). At descriptor initialization, SW should set this field to 0. This field allows software to read the progress of the data transfer. Note that SRC.ADDR and DST.ADDR represent base addresses and are not modified during data transfer. However, STATUS.CURR_DATA_NR is modified during data transfer and provides an offset wrt. the base addresses. Default Value: Undefined

11.1.21 DMAC_DESCR2_PONG_SRC

Pong source address

Address: 0x40101850

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	See description of PING_SRC. Default Value: Undefined

11.1.22 DMAC_DESCR2_PONG_DST

Pong destination address

Address: 0x40101854

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	See description of PING_DST. Default Value: Undefined

11.1.23 DMAC_DESCR2_PONG_CTL

Pong control word

Address: 0x40101858

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	None		RW	
HW Access	RW	RW	RW	RW	None		RW	
Name	SRC_ADDR_INCR	SRC_TRANSFER_SIZE	DST_ADDR_INCR	DST_TRANSFER_SIZE	None [19:18]		DATA_SIZE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW		RW	RW	RW	RW	RW	
HW Access	RW		RW	RW	RW	RW	RW	
Name	OPCODE [31:30]		FLIPPING	PREEMPT-ABLE	SET_CAUSE	INV_DESCR	WAIT_FOR_DEACT [25:24]	

Bits	Name	Description
31 : 30	OPCODE	See description of PING_CTL. Default Value: Undefined
29	FLIPPING	See description of PING_CTL. Default Value: Undefined
28	PREEMPTABLE	See description of PING_CTL. Default Value: Undefined
27	SET_CAUSE	See description of PING_CTL. Default Value: Undefined
26	INV_DESCR	See description of PING_CTL. Default Value: Undefined
25 : 24	WAIT_FOR_DEACT	See description of PING_CTL. Default Value: Undefined
23	SRC_ADDR_INCR	See description of PING_CTL. Default Value: Undefined

(continued)

22	SRC_TRANSFER_SIZE	See description of PING_CTL. Default Value: Undefined
21	DST_ADDR_INCR	See description of PING_CTL. Default Value: Undefined
20	DST_TRANSFER_SIZE	See description of PING_CTL. Default Value: Undefined
17 : 16	DATA_SIZE	See description of PING_CTL. Default Value: Undefined
15 : 0	DATA_NR	See description of PING_CTL. Default Value: Undefined

11.1.24 DMAC_DESCR2_PONG_STATUS

Pong status word

Address: 0x4010185C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None					RW		
HW Access	None					RW		
Name	None [23:19]					RESPONSE [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	RW	None						
Name	VALID	None [30:24]						

Bits	Name	Description
31	VALID	See description of PING_STATUS. Default Value: Undefined
18 : 16	RESPONSE	See description of PING_STATUS. Default Value: Undefined
15 : 0	CURR_DATA_NR	See description of PING_STATUS. Default Value: Undefined

11.1.25 DMAC_DESCR3_PING_SRC

Ping source address

Address: 0x40101860

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Base address of source location. The effective source location is calculated by adding on offset (derived from PING.STATUS.CURR_DATA_NR) to this base address. Default Value: Undefined

11.1.26 DMAC_DESCR3_PING_DST

Ping destination address

Address: 0x40101864

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Base address of destination location. The effective destination location is calculated by adding on offset (derived from PING.STATUS.CURR_DATA_NR) to this base address. Default Value: Undefined

11.1.27 DMAC_DESCR3_PING_CTL

Ping control word

Address: 0x40101868

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	None		RW	
HW Access	RW	RW	RW	RW	None		RW	
Name	SRC_ADDR_INCR	SRC_TRANSFER_SIZE	DST_ADDR_INCR	DST_TRANSFER_SIZE	None [19:18]		DATA_SIZE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW		RW	RW	RW	RW	RW	
HW Access	RW		RW	RW	RW	RW	RW	
Name	OPCODE [31:30]		FLIPPING	PREEMPT-ABLE	SET_CAUSE	INV_DESCR	WAIT_FOR_DEACT [25:24]	

Bits	Name	Description

(continued)

31 : 30	OPCODE	Specifies the specific data transfer (only when the VALID bit of the descriptors STATUS word is 1): 0: A single trigger initiates a single data element transfer (DW mode). This opcode specifies a transfer of a single data element. The current descriptor is completed when the amount of transferred single data elements equals the programmed buffer size (DATA_NR+1). 1: A single trigger initiates a single descriptor transfer (DMA mode). This opcode specifies a transfer of DATA_NR+1 data elements as specified by the current descriptor structure. The current descriptor is completed when its data transfer is completed. 2: A single trigger initiates a descriptor list transfer (DMA mode). This opcode specifies a transfer of DATA_NR+1 data elements as specified by the current descriptor structure and by successive valid descriptors. The current descriptor is completed when its data transfer is completed. This OPCODE relies on FLIPPING to be set to '1', such that the CHi_CTL.PING_PONG field is flipped/inverted and the successive descriptor is used. This continues for as long as the successive descriptor is valid. Note that as the HW is using the PING/PONG descriptor, the SW can prepare the alternate PONG/PING descriptor. The interrupt mechanism is used by HW to convey to the SW that the current descriptor is completed (and can be prepared for a successive transfer). After completerion of the opcode (and waiting for de-activation, the channel's output trigger is activated). Default Value: Undefined
29	FLIPPING	1: On completion of the current descriptor structure, the current descriptor identifier CHi_CTL.PING_PONG is flipped/inverted. In DMA mode, descriptor list transfer, flipping of the current descriptor identifier can be used to construct a linked list of descriptor structures. Default Value: Undefined
28	PREEMPTABLE	1: Transfer is preemptable. In DMA mode (OPCODE is 1 or 2), multi data element transfers are constructed out of multiple single data element load (from the source location) and store (to the destination location) sequences. This field allows higher priority activated channels to preempt the current transfer in between these atomic (load, store) sequences. Preemption will NOT deactivate the current channel. As a result, after completion of a higher priority activated channel, the current channel is rescheduled. Default Value: Undefined
27	SET_CAUSE	1: On completion of the current descriptor structure, the interrupt cause field of the channel is set to 1 (INTR.CH[i]). Default Value: Undefined
26	INV_DESCR	1: On completion of the current descriptor structure, the VALID bit of the descriptors STATUS word is set to 0. Default Value: Undefined

(continued)

25 : 24	WAIT_FOR_DEACT	Specifies whether the data transfer engine should wait for the channel to be deactivated; i.e. the selected system trigger is not active. This field is used to synchronize the controllers data transfer(s) with the agent that generated the trigger. This field is ONLY used at the completion of an opcode. E.g., a FIFO indicates that it is empty and it needs a new data sample. The agent removes the trigger ONLY when the data sample has been written by the transfer engine AND received by the agent. Furthermore, the agents trigger may be delayed by a few cycles before it reaches the DW/DMA controller. This field is used for level sensitive trigger, which reflect state (pulse sensitive triggers should have this field set to "0"). The wait cycles incurred by this field reduce DW/DMA controller performance. 0: Do not wait for de-activation (for pulse sensitive triggers). 1: Wait for up to 4 cycles. 2: Wait for up to 8 cycles. 3: Wait indefinitely. This option may result in DW/DMA controller lockup if the system trigger is not de-activated by the source agent. Default Value: Undefined
23	SRC_ADDR_INCR	Specifies whether the source location address is incremented by the SRC_TRANSFER_SIZE after each single data element transfer or not. 0: No increment, typically used for receive (RX) FIFO structures. 1: Increment, typically used for memory structures. Default Value: Undefined
22	SRC_TRANSFER_SIZE	Specifies the bus transfer size to the source location: 0: As specified by DATA_SIZE. 1: Word (32 bits). Distinguishing bus transfer size from data element size allows for source components with data elements that are smaller than their 32-bit bus interface width. E.g., an ADC source has a 32-bit bus transfer size, but only provides a 16-bit data element. Default Value: Undefined
21	DST_ADDR_INCR	Specifies whether the destination location address is incremented by the DST_TRANSFER_SIZE after each single data element transfer or not. 0 : No increment, typically used for transmit (TX) FIFO structures. 1: Increment, typically used for memory structures. Default Value: Undefined
20	DST_TRANSFER_SIZE	Specifies the bus transfer size to the destination location: 0: As specified by DATA_SIZE. 1: Word (32 bits). Distinguishing bus transfer size from data element size allows for destination components with data elements that are smaller than their 32-bit bus interface width. E.g., a DAC destination has a 32-bit bus transfer size, but only requires a 16-bit data element. Default Value: Undefined

(continued)

17 : 16	DATA_SIZE	Specifies the data element size: 0: Byte (8 bits). 1: Halfword (16 bits). 2: Word (32 bits). DATA_SIZE, SRC_TRANSFER_SIZE and DST_TRANSFER_SIZE together determine how data elements are transferred. The following are the 9 legal settings: - DATA is 8 bit, SRC is 8 bit, DST is 8 bit - DATA is 8 bit, SRC is 32 bit (higher 24 bits are dropped), DST is 8 bit - DATA is 8 bit, SRC is 8 bit, DST is 32 bit (higher 24 bits are made 0) - DATA is 8 bit, SRC is 32 bit (higher 24 bits are dropped), DST is 32 bit (higher 24 bits are made 0) - DATA is 16 bit, SRC is 16 bit, DST is 16 bit - DATA is 16 bit, SRC is 32 bit (higher 16 bits are dropped), DST is 16 bit - DATA is 16 bit, SRC is 16 bit, DST is 32 bit (higher 16 bits are made 0) - DATA is 16 bit, SRC is 32 bit (higher 16 bits are dropped), DST is 32 bit (higher 16 bits are made 0) - DATA is 32 bit, SRC is 32 bit, DST is 32 bit Default Value: Undefined
15 : 0	DATA_NR	Number of data elements that are transferred by a single descriptor. In DW mode (OPCODE is 0) each trigger initiates the transfer of a single data element. This field specifies the source and/or destination buffer size in data elements: buffer size = DATA_NR+1. The buffer is typically associated to a memory structure. In DMA mode (OPCODE is 1 or 2) each trigger initiates the transfer of DATA_NR+1 data elements. Default Value: Undefined

11.1.28 DMAC_DESCR3_PING_STATUS

Ping status word

Address: 0x4010186C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None					RW		
HW Access	None					RW		
Name	None [23:19]					RESPONSE [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	RW	None						
Name	VALID	None [30:24]						

Bits	Name	Description
31	VALID	0: Invalid, cannot be used for a data transfer. An attempt to use this descriptor for a data transfer will result in an INVALID_DESCR response code (and the interrupt cause bit is set to 1). 1: Valid. Hardware set this field to 0 when a descriptor is done, but only if CONTROL.INV_DESCR is 1. Software sets this field to 1 when a descriptor is initialized. Default Value: Undefined

(continued)

18 : 16	RESPONSE	Response code (the first two codes NO_ERROR and DONE are the result of normal behavior, the other codes are the result of erroneous behavior). 0/NO_ERROR: No error. Setting this response does NOT set the interrupt cause bit to 1. STATUS.VALID is NOT affected. CHi_CTL.ENABLED is NOT affected. CHi_CTL.PING_PONG is not updated. This response is used for an unused or not completed descriptor. Software should set the RESPONSE field to 0/NO_ERROR during descriptor initialization. 1/DONE: Descriptor is done (without errors). Setting this response sets the interrupt cause bit to 1 if CONTROL.SET_CAUSE is 1. STATUS.VALID is set to 0 if CONTROL.INV_DESCR is 1. CHi_CTL.ENABLED is NOT affected. CHi_CTL.PING_PONG is updated if CONTROL.FLIPPING is 1. 2/SRC_BUS_ERROR: Bus error while loading data from the source location. Setting this response sets the interrupt cause bit to 1. STATUS.VALID is set 0. CHi_CTL.ENABLED is set to 0. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). 3/DST_BUS_ERROR: Bus error while storing data to the destination location. Setting this response sets the interrupt cause bit to 1. STATUS.VALID is set 0. CHi_CTL.ENABLED is set to 0. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). 4/SRC_MISAL: Misalignment of source address. This occurs on a 16-bit bus transfer that is not 2-byte aligned or on a 32-bit bus transfer that is not 4-byte aligned. Setting this response sets the interrupt cause bit to 1. STATUS.VALID is set 0. CHi_CTL.ENABLED is set to 0. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). 5/DST_MISAL: Misalignment of destination address. This occurs on a 16-bit bus transfer that is not 2-byte aligned or on a 32-bit bus transfer that is not 4-byte aligned. Setting this response sets the interrupt cause bit to 1. STATUS.VALID is set 0. CHi_CTL.ENABLED is set to 0. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). 6/INVALID_DESCR: Invalid descriptor (STATUS.VALID is 0). This occurs when an activated channel has an invalid descriptor. CHi_CTL.ENABLED is set to 0. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). Default Value: Undefined
15 : 0	CURR_DATA_NR	Specifies the index of the current data transfer. This value increases from 0 to CONTROL.DATA_NR. HW sets this field: - When a descriptor is done (RESPONSE is DONE), the field is set to "0" when PING_CTL.INV_DESCR is '0' and the field is set to PING_CTL.DATA_NR when PING_CTL.INV_DESCR is '1'. - When a descriptor is not done (RESPONSE is NO_ERROR), the field reflects the progress of a data transfer. - In case of erroneous behavior (RESPONSE is neither DONE or NO_ERROR), the field is not updated, but keeps its value to ease debugging. HW only modifies this field for an active descriptor (STATUS.VALID to be 1). At descriptor initialization, SW should set this field to 0. This field allows software to read the progress of the data transfer. Note that SRC.ADDR and DST.ADDR represent base addresses and are not modified during data transfer. However, STATUS.CURR_DATA_NR is modified during data transfer and provides an offset wrt. the base addresses. Default Value: Undefined

11.1.29 DMAC_DESCR3_PONG_SRC

Pong source address

Address: 0x40101870

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	See description of PING_SRC. Default Value: Undefined

11.1.30 DMAC_DESCR3_PONG_DST

Pong destination address

Address: 0x40101874

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	See description of PING_DST. Default Value: Undefined

11.1.31 DMAC_DESCR3_PONG_CTL

Pong control word

Address: 0x40101878

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	None		RW	
HW Access	RW	RW	RW	RW	None		RW	
Name	SRC_ADDR_INCR	SRC_TRANSFER_SIZE	DST_ADDR_INCR	DST_TRANSFER_SIZE	None [19:18]		DATA_SIZE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW		RW	RW	RW	RW	RW	
HW Access	RW		RW	RW	RW	RW	RW	
Name	OPCODE [31:30]		FLIPPING	PREEMPT-ABLE	SET_CAUSE	INV_DESCR	WAIT_FOR_DEACT [25:24]	

Bits	Name	Description
31 : 30	OPCODE	See description of PING_CTL. Default Value: Undefined
29	FLIPPING	See description of PING_CTL. Default Value: Undefined
28	PREEMPTABLE	See description of PING_CTL. Default Value: Undefined
27	SET_CAUSE	See description of PING_CTL. Default Value: Undefined
26	INV_DESCR	See description of PING_CTL. Default Value: Undefined
25 : 24	WAIT_FOR_DEACT	See description of PING_CTL. Default Value: Undefined
23	SRC_ADDR_INCR	See description of PING_CTL. Default Value: Undefined

(continued)

22	SRC_TRANSFER_SIZE	See description of PING_CTL. Default Value: Undefined
21	DST_ADDR_INCR	See description of PING_CTL. Default Value: Undefined
20	DST_TRANSFER_SIZE	See description of PING_CTL. Default Value: Undefined
17 : 16	DATA_SIZE	See description of PING_CTL. Default Value: Undefined
15 : 0	DATA_NR	See description of PING_CTL. Default Value: Undefined

11.1.32 DMAC_DESCR3_PONG_STATUS

Pong status word

Address: 0x4010187C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None					RW		
HW Access	None					RW		
Name	None [23:19]					RESPONSE [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	RW	None						
Name	VALID	None [30:24]						

Bits	Name	Description
31	VALID	See description of PING_STATUS. Default Value: Undefined
18 : 16	RESPONSE	See description of PING_STATUS. Default Value: Undefined
15 : 0	CURR_DATA_NR	See description of PING_STATUS. Default Value: Undefined

11.1.33 DMAC_DESCR4_PING_SRC

Ping source address

Address: 0x40101880

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Base address of source location. The effective source location is calculated by adding on offset (derived from PING.STATUS.CURR_DATA_NR) to this base address. Default Value: Undefined

11.1.34 DMAC_DESCR4_PING_DST

Ping destination address

Address: 0x40101884

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Base address of destination location. The effective destination location is calculated by adding on offset (derived from PING.STATUS.CURR_DATA_NR) to this base address. Default Value: Undefined

11.1.35 DMAC_DESCR4_PING_CTL

Ping control word

Address: 0x40101888

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	None		RW	
HW Access	RW	RW	RW	RW	None		RW	
Name	SRC_ADDR_INCR	SRC_TRANSFER_SIZE	DST_ADDR_INCR	DST_TRANSFER_SIZE	None [19:18]		DATA_SIZE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW		RW	RW	RW	RW	RW	
HW Access	RW		RW	RW	RW	RW	RW	
Name	OPCODE [31:30]		FLIPPING	PREEMPT-ABLE	SET_CAUSE	INV_DESCR	WAIT_FOR_DEACT [25:24]	

Bits	Name	Description

(continued)

31 : 30	OPCODE	Specifies the specific data transfer (only when the VALID bit of the descriptors STATUS word is 1): 0: A single trigger initiates a single data element transfer (DW mode). This opcode specifies a transfer of a single data element. The current descriptor is completed when the amount of transferred single data elements equals the programmed buffer size (DATA_NR+1). 1: A single trigger initiates a single descriptor transfer (DMA mode). This opcode specifies a transfer of DATA_NR+1 data elements as specified by the current descriptor structure. The current descriptor is completed when its data transfer is completed. 2: A single trigger initiates a descriptor list transfer (DMA mode). This opcode specifies a transfer of DATA_NR+1 data elements as specified by the current descriptor structure and by successive valid descriptors. The current descriptor is completed when its data transfer is completed. This OPCODE relies on FLIPPING to be set to '1', such that the CHi_CTL.PING_PONG field is flipped/inverted and the successive descriptor is used. This continues for as long as the successive descriptor is valid. Note that as the HW is using the PING/PONG descriptor, the SW can prepare the alternate PONG/PING descriptor. The interrupt mechanism is used by HW to convey to the SW that the current descriptor is completed (and can be prepared for a successive transfer). After completerion of the opcode (and waiting for de-activation, the channel's output trigger is activated). Default Value: Undefined
29	FLIPPING	1: On completion of the current descriptor structure, the current descriptor identifier CHi_CTL.PING_PONG is flipped/inverted. In DMA mode, descriptor list transfer, flipping of the current descriptor identifier can be used to construct a linked list of descriptor structures. Default Value: Undefined
28	PREEMPTABLE	1: Transfer is preemptable. In DMA mode (OPCODE is 1 or 2), multi data element transfers are constructed out of multiple single data element load (from the source location) and store (to the destination location) sequences. This field allows higher priority activated channels to preempt the current transfer in between these atomic (load, store) sequences. Preemption will NOT deactivate the current channel. As a result, after completion of a higher priority activated channel, the current channel is rescheduled. Default Value: Undefined
27	SET_CAUSE	1: On completion of the current descriptor structure, the interrupt cause field of the channel is set to 1 (INTR.CH[i]). Default Value: Undefined
26	INV_DESCR	1: On completion of the current descriptor structure, the VALID bit of the descriptors STATUS word is set to 0. Default Value: Undefined

(continued)

25 : 24	WAIT_FOR_DEACT	Specifies whether the data transfer engine should wait for the channel to be deactivated; i.e. the selected system trigger is not active. This field is used to synchronize the controllers data transfer(s) with the agent that generated the trigger. This field is ONLY used at the completion of an opcode. E.g., a FIFO indicates that it is empty and it needs a new data sample. The agent removes the trigger ONLY when the data sample has been written by the transfer engine AND received by the agent. Furthermore, the agents trigger may be delayed by a few cycles before it reaches the DW/DMA controller. This field is used for level sensitive trigger, which reflect state (pulse sensitive triggers should have this field set to "0"). The wait cycles incurred by this field reduce DW/DMA controller performance. 0: Do not wait for de-activation (for pulse sensitive triggers). 1: Wait for up to 4 cycles. 2: Wait for up to 8 cycles. 3: Wait indefinitely. This option may result in DW/DMA controller lockup if the system trigger is not de-activated by the source agent. Default Value: Undefined
23	SRC_ADDR_INCR	Specifies whether the source location address is incremented by the SRC_TRANSFER_SIZE after each single data element transfer or not. 0: No increment, typically used for receive (RX) FIFO structures. 1: Increment, typically used for memory structures. Default Value: Undefined
22	SRC_TRANSFER_SIZE	Specifies the bus transfer size to the source location: 0: As specified by DATA_SIZE. 1: Word (32 bits). Distinguishing bus transfer size from data element size allows for source components with data elements that are smaller than their 32-bit bus interface width. E.g., an ADC source has a 32-bit bus transfer size, but only provides a 16-bit data element. Default Value: Undefined
21	DST_ADDR_INCR	Specifies whether the destination location address is incremented by the DST_TRANSFER_SIZE after each single data element transfer or not. 0 : No increment, typically used for transmit (TX) FIFO structures. 1: Increment, typically used for memory structures. Default Value: Undefined
20	DST_TRANSFER_SIZE	Specifies the bus transfer size to the destination location: 0: As specified by DATA_SIZE. 1: Word (32 bits). Distinguishing bus transfer size from data element size allows for destination components with data elements that are smaller than their 32-bit bus interface width. E.g., a DAC destination has a 32-bit bus transfer size, but only requires a 16-bit data element. Default Value: Undefined

(continued)

17 : 16	DATA_SIZE	Specifies the data element size: 0: Byte (8 bits). 1: Halfword (16 bits). 2: Word (32 bits). DATA_SIZE, SRC_TRANSFER_SIZE and DST_TRANSFER_SIZE together determine how data elements are transferred. The following are the 9 legal settings: - DATA is 8 bit, SRC is 8 bit, DST is 8 bit - DATA is 8 bit, SRC is 32 bit (higher 24 bits are dropped), DST is 8 bit - DATA is 8 bit, SRC is 8 bit, DST is 32 bit (higher 24 bits are made 0) - DATA is 8 bit, SRC is 32 bit (higher 24 bits are dropped), DST is 32 bit (higher 24 bits are made 0) - DATA is 16 bit, SRC is 16 bit, DST is 16 bit - DATA is 16 bit, SRC is 32 bit (higher 16 bits are dropped), DST is 16 bit - DATA is 16 bit, SRC is 16 bit, DST is 32 bit (higher 16 bits are made 0) - DATA is 16 bit, SRC is 32 bit (higher 16 bits are dropped), DST is 32 bit (higher 16 bits are made 0) - DATA is 32 bit, SRC is 32 bit, DST is 32 bit Default Value: Undefined
15 : 0	DATA_NR	Number of data elements that are transferred by a single descriptor. In DW mode (OPCODE is 0) each trigger initiates the transfer of a single data element. This field specifies the source and/or destination buffer size in data elements: buffer size = DATA_NR+1. The buffer is typically associated to a memory structure. In DMA mode (OPCODE is 1 or 2) each trigger initiates the transfer of DATA_NR+1 data elements. Default Value: Undefined

11.1.36 DMAC_DESCR4_PING_STATUS

Ping status word

Address: 0x4010188C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None					RW		
HW Access	None					RW		
Name	None [23:19]					RESPONSE [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	RW	None						
Name	VALID	None [30:24]						

Bits	Name	Description
31	VALID	0: Invalid, cannot be used for a data transfer. An attempt to use this descriptor for a data transfer will result in an INVALID_DESCR response code (and the interrupt cause bit is set to 1). 1: Valid. Hardware set this field to 0 when a descriptor is done, but only if CONTROL.INV_DESCR is 1. Software sets this field to 1 when a descriptor is initialized. Default Value: Undefined

(continued)

18 : 16	RESPONSE	Response code (the first two codes NO_ERROR and DONE are the result of normal behavior, the other codes are the result of erroneous behavior). 0/NO_ERROR: No error. Setting this response does NOT set the interrupt cause bit to 1. STATUS.VALID is NOT affected. CHi_CTL.ENABLED is NOT affected. CHi_CTL.PING_PONG is not updated. This response is used for an unused or not completed descriptor. Software should set the RESPONSE field to 0/NO_ERROR during descriptor initialization. 1/DONE: Descriptor is done (without errors). Setting this response sets the interrupt cause bit to 1 if CONTROL.SET_CAUSE is 1. STATUS.VALID is set to 0 if CONTROL.INV_DESCR is 1. CHi_CTL.ENABLED is NOT affected. CHi_CTL.PING_PONG is updated if CONTROL.FLIPPING is 1. 2/SRC_BUS_ERROR: Bus error while loading data from the source location. Setting this response sets the interrupt cause bit to 1. STATUS.VALID is set 0. CHi_CTL.ENABLED is set to 0. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). 3/DST_BUS_ERROR: Bus error while storing data to the destination location. Setting this response sets the interrupt cause bit to 1. STATUS.VALID is set 0. CHi_CTL.ENABLED is set to 0. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). 4/SRC_MISAL: Misalignment of source address. This occurs on a 16-bit bus transfer that is not 2-byte aligned or on a 32-bit bus transfer that is not 4-byte aligned. Setting this response sets the interrupt cause bit to 1. STATUS.VALID is set 0. CHi_CTL.ENABLED is set to 0. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). 5/DST_MISAL: Misalignment of destination address. This occurs on a 16-bit bus transfer that is not 2-byte aligned or on a 32-bit bus transfer that is not 4-byte aligned. Setting this response sets the interrupt cause bit to 1. STATUS.VALID is set 0. CHi_CTL.ENABLED is set to 0. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). 6/INVALID_DESCR: Invalid descriptor (STATUS.VALID is 0). This occurs when an activated channel has an invalid descriptor. CHi_CTL.ENABLED is set to 0. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). Default Value: Undefined
15 : 0	CURR_DATA_NR	Specifies the index of the current data transfer. This value increases from 0 to CONTROL.DATA_NR. HW sets this field: - When a descriptor is done (RESPONSE is DONE), the field is set to "0" when PING_CTL.INV_DESCR is '0' and the field is set to PING_CTL.DATA_NR when PING_CTL.INV_DESCR is '1'. - When a descriptor is not done (RESPONSE is NO_ERROR), the field reflects the progress of a data transfer. - In case of erroneous behavior (RESPONSE is neither DONE or NO_ERROR), the field is not updated, but keeps its value to ease debugging. HW only modifies this field for an active descriptor (STATUS.VALID to be 1). At descriptor initialization, SW should set this field to 0. This field allows software to read the progress of the data transfer. Note that SRC.ADDR and DST.ADDR represent base addresses and are not modified during data transfer. However, STATUS.CURR_DATA_NR is modified during data transfer and provides an offset wrt. the base addresses. Default Value: Undefined

11.1.37 DMAC_DESCR4_PONG_SRC

Pong source address

Address: 0x40101890

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	See description of PING_SRC. Default Value: Undefined

11.1.38 DMAC_DESCR4_PONG_DST

Pong destination address

Address: 0x40101894

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	See description of PING_DST. Default Value: Undefined

11.1.39 DMAC_DESCR4_PONG_CTL

Pong control word

Address: 0x40101898

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	None		RW	
HW Access	RW	RW	RW	RW	None		RW	
Name	SRC_ADDR_INCR	SRC_TRANSFER_SIZE	DST_ADDR_INCR	DST_TRANSFER_SIZE	None [19:18]		DATA_SIZE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW		RW	RW	RW	RW	RW	
HW Access	RW		RW	RW	RW	RW	RW	
Name	OPCODE [31:30]		FLIPPING	PREEMPT-ABLE	SET_CAUSE	INV_DESCR	WAIT_FOR_DEACT [25:24]	

Bits	Name	Description
31 : 30	OPCODE	See description of PING_CTL. Default Value: Undefined
29	FLIPPING	See description of PING_CTL. Default Value: Undefined
28	PREEMPTABLE	See description of PING_CTL. Default Value: Undefined
27	SET_CAUSE	See description of PING_CTL. Default Value: Undefined
26	INV_DESCR	See description of PING_CTL. Default Value: Undefined
25 : 24	WAIT_FOR_DEACT	See description of PING_CTL. Default Value: Undefined
23	SRC_ADDR_INCR	See description of PING_CTL. Default Value: Undefined

(continued)

22	SRC_TRANSFER_SIZE	See description of PING_CTL. Default Value: Undefined
21	DST_ADDR_INCR	See description of PING_CTL. Default Value: Undefined
20	DST_TRANSFER_SIZE	See description of PING_CTL. Default Value: Undefined
17 : 16	DATA_SIZE	See description of PING_CTL. Default Value: Undefined
15 : 0	DATA_NR	See description of PING_CTL. Default Value: Undefined

11.1.40 DMAC_DESCR4_PONG_STATUS

Pong status word

Address: 0x4010189C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None					RW		
HW Access	None					RW		
Name	None [23:19]					RESPONSE [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	RW	None						
Name	VALID	None [30:24]						

Bits	Name	Description
31	VALID	See description of PING_STATUS. Default Value: Undefined
18 : 16	RESPONSE	See description of PING_STATUS. Default Value: Undefined
15 : 0	CURR_DATA_NR	See description of PING_STATUS. Default Value: Undefined

11.1.41 DMAC_DESCR5_PING_SRC

Ping source address

Address: 0x401018A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Base address of source location. The effective source location is calculated by adding on offset (derived from PING.STATUS.CURR_DATA_NR) to this base address. Default Value: Undefined

11.1.42 DMAC_DESCR5_PING_DST

Ping destination address

Address: 0x401018A4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Base address of destination location. The effective destination location is calculated by adding on offset (derived from PING.STATUS.CURR_DATA_NR) to this base address. Default Value: Undefined

11.1.43 DMAC_DESCR5_PING_CTL

Ping control word

Address: 0x401018A8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	None		RW	
HW Access	RW	RW	RW	RW	None		RW	
Name	SRC_ADDR_INCR	SRC_TRANSFER_SIZE	DST_ADDR_INCR	DST_TRANSFER_SIZE	None [19:18]		DATA_SIZE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW		RW	RW	RW	RW	RW	
HW Access	RW		RW	RW	RW	RW	RW	
Name	OPCODE [31:30]		FLIPPING	PREEMPT-ABLE	SET_CAUSE	INV_DESCR	WAIT_FOR_DEACT [25:24]	

Bits	Name	Description

(continued)

31 : 30	OPCODE	Specifies the specific data transfer (only when the VALID bit of the descriptors STATUS word is 1): 0: A single trigger initiates a single data element transfer (DW mode). This opcode specifies a transfer of a single data element. The current descriptor is completed when the amount of transferred single data elements equals the programmed buffer size (DATA_NR+1). 1: A single trigger initiates a single descriptor transfer (DMA mode). This opcode specifies a transfer of DATA_NR+1 data elements as specified by the current descriptor structure. The current descriptor is completed when its data transfer is completed. 2: A single trigger initiates a descriptor list transfer (DMA mode). This opcode specifies a transfer of DATA_NR+1 data elements as specified by the current descriptor structure and by successive valid descriptors. The current descriptor is completed when its data transfer is completed. This OPCODE relies on FLIPPING to be set to '1', such that the CHi_CTL.PING_PONG field is flipped/inverted and the successive descriptor is used. This continues for as long as the successive descriptor is valid. Note that as the HW is using the PING/PONG descriptor, the SW can prepare the alternate PONG/PING descriptor. The interrupt mechanism is used by HW to convey to the SW that the current descriptor is completed (and can be prepared for a successive transfer). After completerion of the opcode (and waiting for de-activation, the channel's output trigger is activated). Default Value: Undefined
29	FLIPPING	1: On completion of the current descriptor structure, the current descriptor identifier CHi_CTL.PING_PONG is flipped/inverted. In DMA mode, descriptor list transfer, flipping of the current descriptor identifier can be used to construct a linked list of descriptor structures. Default Value: Undefined
28	PREEMPTABLE	1: Transfer is preemptable. In DMA mode (OPCODE is 1 or 2), multi data element transfers are constructed out of multiple single data element load (from the source location) and store (to the destination location) sequences. This field allows higher priority activated channels to preempt the current transfer in between these atomic (load, store) sequences. Preemption will NOT deactivate the current channel. As a result, after completion of a higher priority activated channel, the current channel is rescheduled. Default Value: Undefined
27	SET_CAUSE	1: On completion of the current descriptor structure, the interrupt cause field of the channel is set to 1 (INTR.CH[i]). Default Value: Undefined
26	INV_DESCR	1: On completion of the current descriptor structure, the VALID bit of the descriptors STATUS word is set to 0. Default Value: Undefined

(continued)

25 : 24	WAIT_FOR_DEACT	Specifies whether the data transfer engine should wait for the channel to be deactivated; i.e. the selected system trigger is not active. This field is used to synchronize the controllers data transfer(s) with the agent that generated the trigger. This field is ONLY used at the completion of an opcode. E.g., a FIFO indicates that it is empty and it needs a new data sample. The agent removes the trigger ONLY when the data sample has been written by the transfer engine AND received by the agent. Furthermore, the agents trigger may be delayed by a few cycles before it reaches the DW/DMA controller. This field is used for level sensitive trigger, which reflect state (pulse sensitive triggers should have this field set to "0"). The wait cycles incurred by this field reduce DW/DMA controller performance. 0: Do not wait for de-activation (for pulse sensitive triggers). 1: Wait for up to 4 cycles. 2: Wait for up to 8 cycles. 3: Wait indefinitely. This option may result in DW/DMA controller lockup if the system trigger is not de-activated by the source agent. Default Value: Undefined
23	SRC_ADDR_INCR	Specifies whether the source location address is incremented by the SRC_TRANSFER_SIZE after each single data element transfer or not. 0: No increment, typically used for receive (RX) FIFO structures. 1: Increment, typically used for memory structures. Default Value: Undefined
22	SRC_TRANSFER_SIZE	Specifies the bus transfer size to the source location: 0: As specified by DATA_SIZE. 1: Word (32 bits). Distinguishing bus transfer size from data element size allows for source components with data elements that are smaller than their 32-bit bus interface width. E.g., an ADC source has a 32-bit bus transfer size, but only provides a 16-bit data element. Default Value: Undefined
21	DST_ADDR_INCR	Specifies whether the destination location address is incremented by the DST_TRANSFER_SIZE after each single data element transfer or not. 0 : No increment, typically used for transmit (TX) FIFO structures. 1: Increment, typically used for memory structures. Default Value: Undefined
20	DST_TRANSFER_SIZE	Specifies the bus transfer size to the destination location: 0: As specified by DATA_SIZE. 1: Word (32 bits). Distinguishing bus transfer size from data element size allows for destination components with data elements that are smaller than their 32-bit bus interface width. E.g., a DAC destination has a 32-bit bus transfer size, but only requires a 16-bit data element. Default Value: Undefined

(continued)

17 : 16	DATA_SIZE	Specifies the data element size: 0: Byte (8 bits). 1: Halfword (16 bits). 2: Word (32 bits). DATA_SIZE, SRC_TRANSFER_SIZE and DST_TRANSFER_SIZE together determine how data elements are transferred. The following are the 9 legal settings: - DATA is 8 bit, SRC is 8 bit, DST is 8 bit - DATA is 8 bit, SRC is 32 bit (higher 24 bits are dropped), DST is 8 bit - DATA is 8 bit, SRC is 8 bit, DST is 32 bit (higher 24 bits are made 0) - DATA is 8 bit, SRC is 32 bit (higher 24 bits are dropped), DST is 32 bit (higher 24 bits are made 0) - DATA is 16 bit, SRC is 16 bit, DST is 16 bit - DATA is 16 bit, SRC is 32 bit (higher 16 bits are dropped), DST is 16 bit - DATA is 16 bit, SRC is 16 bit, DST is 32 bit (higher 16 bits are made 0) - DATA is 16 bit, SRC is 32 bit (higher 16 bits are dropped), DST is 32 bit (higher 16 bits are made 0) - DATA is 32 bit, SRC is 32 bit, DST is 32 bit Default Value: Undefined
15 : 0	DATA_NR	Number of data elements that are transferred by a single descriptor. In DW mode (OPCODE is 0) each trigger initiates the transfer of a single data element. This field specifies the source and/or destination buffer size in data elements: buffer size = DATA_NR+1. The buffer is typically associated to a memory structure. In DMA mode (OPCODE is 1 or 2) each trigger initiates the transfer of DATA_NR+1 data elements. Default Value: Undefined

11.1.44 DMAC_DESCR5_PING_STATUS

Ping status word

Address: 0x401018AC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None					RW		
HW Access	None					RW		
Name	None [23:19]					RESPONSE [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	RW	None						
Name	VALID	None [30:24]						

Bits	Name	Description
31	VALID	0: Invalid, cannot be used for a data transfer. An attempt to use this descriptor for a data transfer will result in an INVALID_DESCR response code (and the interrupt cause bit is set to 1). 1: Valid. Hardware set this field to 0 when a descriptor is done, but only if CONTROL.INV_DESCR is 1. Software sets this field to 1 when a descriptor is initialized. Default Value: Undefined

(continued)

18 : 16	RESPONSE	Response code (the first two codes NO_ERROR and DONE are the result of normal behavior, the other codes are the result of erroneous behavior). 0/NO_ERROR: No error. Setting this response does NOT set the interrupt cause bit to 1. STATUS.VALID is NOT affected. CHi_CTL.ENABLED is NOT affected. CHi_CTL.PING_PONG is not updated. This response is used for an unused or not completed descriptor. Software should set the RESPONSE field to 0/NO_ERROR during descriptor initialization. 1/DONE: Descriptor is done (without errors). Setting this response sets the interrupt cause bit to 1 if CONTROL.SET_CAUSE is 1. STATUS.VALID is set to 0 if CONTROL.INV_DESCR is 1. CHi_CTL.ENABLED is NOT affected. CHi_CTL.PING_PONG is updated if CONTROL.FLIPPING is 1. 2/SRC_BUS_ERROR: Bus error while loading data from the source location. Setting this response sets the interrupt cause bit to 1. STATUS.VALID is set 0. CHi_CTL.ENABLED is set to 0. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). 3/DST_BUS_ERROR: Bus error while storing data to the destination location. Setting this response sets the interrupt cause bit to 1. STATUS.VALID is set 0. CHi_CTL.ENABLED is set to 0. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). 4/SRC_MISAL: Misalignment of source address. This occurs on a 16-bit bus transfer that is not 2-byte aligned or on a 32-bit bus transfer that is not 4-byte aligned. Setting this response sets the interrupt cause bit to 1. STATUS.VALID is set 0. CHi_CTL.ENABLED is set to 0. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). 5/DST_MISAL: Misalignment of destination address. This occurs on a 16-bit bus transfer that is not 2-byte aligned or on a 32-bit bus transfer that is not 4-byte aligned. Setting this response sets the interrupt cause bit to 1. STATUS.VALID is set 0. CHi_CTL.ENABLED is set to 0. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). 6/INVALID_DESCR: Invalid descriptor (STATUS.VALID is 0). This occurs when an activated channel has an invalid descriptor. CHi_CTL.ENABLED is set to 0. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). Default Value: Undefined
15 : 0	CURR_DATA_NR	Specifies the index of the current data transfer. This value increases from 0 to CONTROL.DATA_NR. HW sets this field: - When a descriptor is done (RESPONSE is DONE), the field is set to "0" when PING_CTL.INV_DESCR is '0' and the field is set to PING_CTL.DATA_NR when PING_CTL.INV_DESCR is '1'. - When a descriptor is not done (RESPONSE is NO_ERROR), the field reflects the progress of a data transfer. - In case of erroneous behavior (RESPONSE is neither DONE or NO_ERROR), the field is not updated, but keeps its value to ease debugging. HW only modifies this field for an active descriptor (STATUS.VALID to be 1). At descriptor initialization, SW should set this field to 0. This field allows software to read the progress of the data transfer. Note that SRC.ADDR and DST.ADDR represent base addresses and are not modified during data transfer. However, STATUS.CURR_DATA_NR is modified during data transfer and provides an offset wrt. the base addresses. Default Value: Undefined

11.1.45 DMAC_DESCR5_PONG_SRC

Pong source address

Address: 0x401018B0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	See description of PING_SRC. Default Value: Undefined

11.1.46 DMAC_DESCR5_PONG_DST

Pong destination address

Address: 0x401018B4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	See description of PING_DST. Default Value: Undefined

11.1.47 DMAC_DESCR5_PONG_CTL

Pong control word

Address: 0x401018B8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	None		RW	
HW Access	RW	RW	RW	RW	None		RW	
Name	SRC_ADDR_INCR	SRC_TRANSFER_SIZE	DST_ADDR_INCR	DST_TRANSFER_SIZE	None [19:18]		DATA_SIZE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW		RW	RW	RW	RW	RW	
HW Access	RW		RW	RW	RW	RW	RW	
Name	OPCODE [31:30]		FLIPPING	PREEMPT-ABLE	SET_CAUSE	INV_DESCR	WAIT_FOR_DEACT [25:24]	

Bits	Name	Description
31 : 30	OPCODE	See description of PING_CTL. Default Value: Undefined
29	FLIPPING	See description of PING_CTL. Default Value: Undefined
28	PREEMPTABLE	See description of PING_CTL. Default Value: Undefined
27	SET_CAUSE	See description of PING_CTL. Default Value: Undefined
26	INV_DESCR	See description of PING_CTL. Default Value: Undefined
25 : 24	WAIT_FOR_DEACT	See description of PING_CTL. Default Value: Undefined
23	SRC_ADDR_INCR	See description of PING_CTL. Default Value: Undefined

(continued)

22	SRC_TRANSFER_SIZE	See description of PING_CTL. Default Value: Undefined
21	DST_ADDR_INCR	See description of PING_CTL. Default Value: Undefined
20	DST_TRANSFER_SIZE	See description of PING_CTL. Default Value: Undefined
17 : 16	DATA_SIZE	See description of PING_CTL. Default Value: Undefined
15 : 0	DATA_NR	See description of PING_CTL. Default Value: Undefined

11.1.48 DMAC_DESCR5_PONG_STATUS

Pong status word

Address: 0x401018BC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None					RW		
HW Access	None					RW		
Name	None [23:19]					RESPONSE [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	RW	None						
Name	VALID	None [30:24]						

Bits	Name	Description
31	VALID	See description of PING_STATUS. Default Value: Undefined
18 : 16	RESPONSE	See description of PING_STATUS. Default Value: Undefined
15 : 0	CURR_DATA_NR	See description of PING_STATUS. Default Value: Undefined

11.1.49 DMAC_DESCR6_PING_SRC

Ping source address

Address: 0x401018C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Base address of source location. The effective source location is calculated by adding on offset (derived from PING.STATUS.CURR_DATA_NR) to this base address. Default Value: Undefined

11.1.50 DMAC_DESCR6_PING_DST

Ping destination address

Address: 0x401018C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Base address of destination location. The effective destination location is calculated by adding on offset (derived from PING.STATUS.CURR_DATA_NR) to this base address. Default Value: Undefined

11.1.51 DMAC_DESCR6_PING_CTL

Ping control word

Address: 0x401018C8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	None		RW	
HW Access	RW	RW	RW	RW	None		RW	
Name	SRC_ADDR_INCR	SRC_TRANSFER_SIZE	DST_ADDR_INCR	DST_TRANSFER_SIZE	None [19:18]		DATA_SIZE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW		RW	RW	RW	RW	RW	
HW Access	RW		RW	RW	RW	RW	RW	
Name	OPCODE [31:30]		FLIPPING	PREEMPT-ABLE	SET_CAUSE	INV_DESCR	WAIT_FOR_DEACT [25:24]	

Bits	Name	Description

(continued)

31 : 30	OPCODE	Specifies the specific data transfer (only when the VALID bit of the descriptors STATUS word is 1): 0: A single trigger initiates a single data element transfer (DW mode). This opcode specifies a transfer of a single data element. The current descriptor is completed when the amount of transferred single data elements equals the programmed buffer size (DATA_NR+1). 1: A single trigger initiates a single descriptor transfer (DMA mode). This opcode specifies a transfer of DATA_NR+1 data elements as specified by the current descriptor structure. The current descriptor is completed when its data transfer is completed. 2: A single trigger initiates a descriptor list transfer (DMA mode). This opcode specifies a transfer of DATA_NR+1 data elements as specified by the current descriptor structure and by successive valid descriptors. The current descriptor is completed when its data transfer is completed. This OPCODE relies on FLIPPING to be set to '1', such that the CHi_CTL.PING_PONG field is flipped/inverted and the successive descriptor is used. This continues for as long as the successive descriptor is valid. Note that as the HW is using the PING/PONG descriptor, the SW can prepare the alternate PONG/PING descriptor. The interrupt mechanism is used by HW to convey to the SW that the current descriptor is completed (and can be prepared for a successive transfer). After completerion of the opcode (and waiting for de-activation, the channel's output trigger is activated). Default Value: Undefined
29	FLIPPING	1: On completion of the current descriptor structure, the current descriptor identifier CHi_CTL.PING_PONG is flipped/inverted. In DMA mode, descriptor list transfer, flipping of the current descriptor identifier can be used to construct a linked list of descriptor structures. Default Value: Undefined
28	PREEMPTABLE	1: Transfer is preemptable. In DMA mode (OPCODE is 1 or 2), multi data element transfers are constructed out of multiple single data element load (from the source location) and store (to the destination location) sequences. This field allows higher priority activated channels to preempt the current transfer in between these atomic (load, store) sequences. Preemption will NOT deactivate the current channel. As a result, after completion of a higher priority activated channel, the current channel is rescheduled. Default Value: Undefined
27	SET_CAUSE	1: On completion of the current descriptor structure, the interrupt cause field of the channel is set to 1 (INTR.CH[i]). Default Value: Undefined
26	INV_DESCR	1: On completion of the current descriptor structure, the VALID bit of the descriptors STATUS word is set to 0. Default Value: Undefined

(continued)

25 : 24	WAIT_FOR_DEACT	Specifies whether the data transfer engine should wait for the channel to be deactivated; i.e. the selected system trigger is not active. This field is used to synchronize the controllers data transfer(s) with the agent that generated the trigger. This field is ONLY used at the completion of an opcode. E.g., a FIFO indicates that it is empty and it needs a new data sample. The agent removes the trigger ONLY when the data sample has been written by the transfer engine AND received by the agent. Furthermore, the agents trigger may be delayed by a few cycles before it reaches the DW/DMA controller. This field is used for level sensitive trigger, which reflect state (pulse sensitive triggers should have this field set to "0"). The wait cycles incurred by this field reduce DW/DMA controller performance. 0: Do not wait for de-activation (for pulse sensitive triggers). 1: Wait for up to 4 cycles. 2: Wait for up to 8 cycles. 3: Wait indefinitely. This option may result in DW/DMA controller lockup if the system trigger is not de-activated by the source agent. Default Value: Undefined
23	SRC_ADDR_INCR	Specifies whether the source location address is incremented by the SRC_TRANSFER_SIZE after each single data element transfer or not. 0: No increment, typically used for receive (RX) FIFO structures. 1: Increment, typically used for memory structures. Default Value: Undefined
22	SRC_TRANSFER_SIZE	Specifies the bus transfer size to the source location: 0: As specified by DATA_SIZE. 1: Word (32 bits). Distinguishing bus transfer size from data element size allows for source components with data elements that are smaller than their 32-bit bus interface width. E.g., an ADC source has a 32-bit bus transfer size, but only provides a 16-bit data element. Default Value: Undefined
21	DST_ADDR_INCR	Specifies whether the destination location address is incremented by the DST_TRANSFER_SIZE after each single data element transfer or not. 0 : No increment, typically used for transmit (TX) FIFO structures. 1: Increment, typically used for memory structures. Default Value: Undefined
20	DST_TRANSFER_SIZE	Specifies the bus transfer size to the destination location: 0: As specified by DATA_SIZE. 1: Word (32 bits). Distinguishing bus transfer size from data element size allows for destination components with data elements that are smaller than their 32-bit bus interface width. E.g., a DAC destination has a 32-bit bus transfer size, but only requires a 16-bit data element. Default Value: Undefined

(continued)

17 : 16	DATA_SIZE	Specifies the data element size: 0: Byte (8 bits). 1: Halfword (16 bits). 2: Word (32 bits). DATA_SIZE, SRC_TRANSFER_SIZE and DST_TRANSFER_SIZE together determine how data elements are transferred. The following are the 9 legal settings: - DATA is 8 bit, SRC is 8 bit, DST is 8 bit - DATA is 8 bit, SRC is 32 bit (higher 24 bits are dropped), DST is 8 bit - DATA is 8 bit, SRC is 8 bit, DST is 32 bit (higher 24 bits are made 0) - DATA is 8 bit, SRC is 32 bit (higher 24 bits are dropped), DST is 32 bit (higher 24 bits are made 0) - DATA is 16 bit, SRC is 16 bit, DST is 16 bit - DATA is 16 bit, SRC is 32 bit (higher 16 bits are dropped), DST is 16 bit - DATA is 16 bit, SRC is 16 bit, DST is 32 bit (higher 16 bits are made 0) - DATA is 16 bit, SRC is 32 bit (higher 16 bits are dropped), DST is 32 bit (higher 16 bits are made 0) - DATA is 32 bit, SRC is 32 bit, DST is 32 bit Default Value: Undefined
15 : 0	DATA_NR	Number of data elements that are transferred by a single descriptor. In DW mode (OPCODE is 0) each trigger initiates the transfer of a single data element. This field specifies the source and/or destination buffer size in data elements: buffer size = DATA_NR+1. The buffer is typically associated to a memory structure. In DMA mode (OPCODE is 1 or 2) each trigger initiates the transfer of DATA_NR+1 data elements. Default Value: Undefined

11.1.52 DMAC_DESCR6_PING_STATUS

Ping status word

Address: 0x401018CC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None					RW		
HW Access	None					RW		
Name	None [23:19]					RESPONSE [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	RW	None						
Name	VALID	None [30:24]						

Bits	Name	Description
31	VALID	0: Invalid, cannot be used for a data transfer. An attempt to use this descriptor for a data transfer will result in an INVALID_DESCR response code (and the interrupt cause bit is set to 1). 1: Valid. Hardware set this field to 0 when a descriptor is done, but only if CONTROL.INV_DESCR is 1. Software sets this field to 1 when a descriptor is initialized. Default Value: Undefined

(continued)

18 : 16	RESPONSE	Response code (the first two codes NO_ERROR and DONE are the result of normal behavior, the other codes are the result of erroneous behavior). 0/NO_ERROR: No error. Setting this response does NOT set the interrupt cause bit to 1. STATUS.VALID is NOT affected. CHi_CTL.ENABLED is NOT affected. CHi_CTL.PING_PONG is not updated. This response is used for an unused or not completed descriptor. Software should set the RESPONSE field to 0/NO_ERROR during descriptor initialization. 1/DONE: Descriptor is done (without errors). Setting this response sets the interrupt cause bit to 1 if CONTROL.SET_CAUSE is 1. STATUS.VALID is set to 0 if CONTROL.INV_DESCR is 1. CHi_CTL.ENABLED is NOT affected. CHi_CTL.PING_PONG is updated if CONTROL.FLIPPING is 1. 2/SRC_BUS_ERROR: Bus error while loading data from the source location. Setting this response sets the interrupt cause bit to 1. STATUS.VALID is set 0. CHi_CTL.ENABLED is set to 0. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). 3/DST_BUS_ERROR: Bus error while storing data to the destination location. Setting this response sets the interrupt cause bit to 1. STATUS.VALID is set 0. CHi_CTL.ENABLED is set to 0. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). 4/SRC_MISAL: Misalignment of source address. This occurs on a 16-bit bus transfer that is not 2-byte aligned or on a 32-bit bus transfer that is not 4-byte aligned. Setting this response sets the interrupt cause bit to 1. STATUS.VALID is set 0. CHi_CTL.ENABLED is set to 0. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). 5/DST_MISAL: Misalignment of destination address. This occurs on a 16-bit bus transfer that is not 2-byte aligned or on a 32-bit bus transfer that is not 4-byte aligned. Setting this response sets the interrupt cause bit to 1. STATUS.VALID is set 0. CHi_CTL.ENABLED is set to 0. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). 6/INVALID_DESCR: Invalid descriptor (STATUS.VALID is 0). This occurs when an activated channel has an invalid descriptor. CHi_CTL.ENABLED is set to 0. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). Default Value: Undefined
15 : 0	CURR_DATA_NR	Specifies the index of the current data transfer. This value increases from 0 to CONTROL.DATA_NR. HW sets this field: - When a descriptor is done (RESPONSE is DONE), the field is set to "0" when PING_CTL.INV_DESCR is '0' and the field is set to PING_CTL.DATA_NR when PING_CTL.INV_DESCR is '1'. - When a descriptor is not done (RESPONSE is NO_ERROR), the field reflects the progress of a data transfer. - In case of erroneous behavior (RESPONSE is neither DONE or NO_ERROR), the field is not updated, but keeps its value to ease debugging. HW only modifies this field for an active descriptor (STATUS.VALID to be 1). At descriptor initialization, SW should set this field to 0. This field allows software to read the progress of the data transfer. Note that SRC.ADDR and DST.ADDR represent base addresses and are not modified during data transfer. However, STATUS.CURR_DATA_NR is modified during data transfer and provides an offset wrt. the base addresses. Default Value: Undefined

11.1.53 DMAC_DESCR6_PONG_SRC

Pong source address

Address: 0x401018D0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	See description of PING_SRC. Default Value: Undefined

11.1.54 DMAC_DESCR6_PONG_DST

Pong destination address

Address: 0x401018D4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	See description of PING_DST. Default Value: Undefined

11.1.55 DMAC_DESCR6_PONG_CTL

Pong control word

Address: 0x401018D8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	None		RW	
HW Access	RW	RW	RW	RW	None		RW	
Name	SRC_ADDR_INCR	SRC_TRANSFER_SIZE	DST_ADDR_INCR	DST_TRANSFER_SIZE	None [19:18]		DATA_SIZE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW		RW	RW	RW	RW	RW	
HW Access	RW		RW	RW	RW	RW	RW	
Name	OPCODE [31:30]		FLIPPING	PREEMPT-ABLE	SET_CAUSE	INV_DESCR	WAIT_FOR_DEACT [25:24]	

Bits	Name	Description
31 : 30	OPCODE	See description of PING_CTL. Default Value: Undefined
29	FLIPPING	See description of PING_CTL. Default Value: Undefined
28	PREEMPTABLE	See description of PING_CTL. Default Value: Undefined
27	SET_CAUSE	See description of PING_CTL. Default Value: Undefined
26	INV_DESCR	See description of PING_CTL. Default Value: Undefined
25 : 24	WAIT_FOR_DEACT	See description of PING_CTL. Default Value: Undefined
23	SRC_ADDR_INCR	See description of PING_CTL. Default Value: Undefined

(continued)

22	SRC_TRANSFER_SIZE	See description of PING_CTL. Default Value: Undefined
21	DST_ADDR_INCR	See description of PING_CTL. Default Value: Undefined
20	DST_TRANSFER_SIZE	See description of PING_CTL. Default Value: Undefined
17 : 16	DATA_SIZE	See description of PING_CTL. Default Value: Undefined
15 : 0	DATA_NR	See description of PING_CTL. Default Value: Undefined

11.1.56 DMAC_DESCR6_PONG_STATUS

Pong status word

Address: 0x401018DC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None					RW		
HW Access	None					RW		
Name	None [23:19]					RESPONSE [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	RW	None						
Name	VALID	None [30:24]						

Bits	Name	Description
31	VALID	See description of PING_STATUS. Default Value: Undefined
18 : 16	RESPONSE	See description of PING_STATUS. Default Value: Undefined
15 : 0	CURR_DATA_NR	See description of PING_STATUS. Default Value: Undefined

11.1.57 DMAC_DESCR7_PING_SRC

Ping source address

Address: 0x401018E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Base address of source location. The effective source location is calculated by adding on offset (derived from PING.STATUS.CURR_DATA_NR) to this base address. Default Value: Undefined

11.1.58 DMAC_DESCR7_PING_DST

Ping destination address

Address: 0x401018E4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Base address of destination location. The effective destination location is calculated by adding on offset (derived from PING.STATUS.CURR_DATA_NR) to this base address. Default Value: Undefined

11.1.59 DMAC_DESCR7_PING_CTL

Ping control word

Address: 0x401018E8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	None		RW	
HW Access	RW	RW	RW	RW	None		RW	
Name	SRC_ADDR_INCR	SRC_TRANSFER_SIZE	DST_ADDR_INCR	DST_TRANSFER_SIZE	None [19:18]		DATA_SIZE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW		RW	RW	RW	RW	RW	
HW Access	RW		RW	RW	RW	RW	RW	
Name	OPCODE [31:30]		FLIPPING	PREEMPT-ABLE	SET_CAUSE	INV_DESCR	WAIT_FOR_DEACT [25:24]	

Bits	Name	Description

(continued)

31 : 30	OPCODE	Specifies the specific data transfer (only when the VALID bit of the descriptors STATUS word is 1): 0: A single trigger initiates a single data element transfer (DW mode). This opcode specifies a transfer of a single data element. The current descriptor is completed when the amount of transferred single data elements equals the programmed buffer size (DATA_NR+1). 1: A single trigger initiates a single descriptor transfer (DMA mode). This opcode specifies a transfer of DATA_NR+1 data elements as specified by the current descriptor structure. The current descriptor is completed when its data transfer is completed. 2: A single trigger initiates a descriptor list transfer (DMA mode). This opcode specifies a transfer of DATA_NR+1 data elements as specified by the current descriptor structure and by successive valid descriptors. The current descriptor is completed when its data transfer is completed. This OPCODE relies on FLIPPING to be set to '1', such that the CHi_CTL.PING_PONG field is flipped/inverted and the successive descriptor is used. This continues for as long as the successive descriptor is valid. Note that as the HW is using the PING/PONG descriptor, the SW can prepare the alternate PONG/PING descriptor. The interrupt mechanism is used by HW to convey to the SW that the current descriptor is completed (and can be prepared for a successive transfer). After completerion of the opcode (and waiting for de-activation, the channel's output trigger is activated). Default Value: Undefined
29	FLIPPING	1: On completion of the current descriptor structure, the current descriptor identifier CHi_CTL.PING_PONG is flipped/inverted. In DMA mode, descriptor list transfer, flipping of the current descriptor identifier can be used to construct a linked list of descriptor structures. Default Value: Undefined
28	PREEMPTABLE	1: Transfer is preemptable. In DMA mode (OPCODE is 1 or 2), multi data element transfers are constructed out of multiple single data element load (from the source location) and store (to the destination location) sequences. This field allows higher priority activated channels to preempt the current transfer in between these atomic (load, store) sequences. Preemption will NOT deactivate the current channel. As a result, after completion of a higher priority activated channel, the current channel is rescheduled. Default Value: Undefined
27	SET_CAUSE	1: On completion of the current descriptor structure, the interrupt cause field of the channel is set to 1 (INTR.CH[i]). Default Value: Undefined
26	INV_DESCR	1: On completion of the current descriptor structure, the VALID bit of the descriptors STATUS word is set to 0. Default Value: Undefined

(continued)

25 : 24	WAIT_FOR_DEACT	Specifies whether the data transfer engine should wait for the channel to be deactivated; i.e. the selected system trigger is not active. This field is used to synchronize the controllers data transfer(s) with the agent that generated the trigger. This field is ONLY used at the completion of an opcode. E.g., a FIFO indicates that it is empty and it needs a new data sample. The agent removes the trigger ONLY when the data sample has been written by the transfer engine AND received by the agent. Furthermore, the agents trigger may be delayed by a few cycles before it reaches the DW/DMA controller. This field is used for level sensitive trigger, which reflect state (pulse sensitive triggers should have this field set to "0"). The wait cycles incurred by this field reduce DW/DMA controller performance. 0: Do not wait for de-activation (for pulse sensitive triggers). 1: Wait for up to 4 cycles. 2: Wait for up to 8 cycles. 3: Wait indefinitely. This option may result in DW/DMA controller lockup if the system trigger is not de-activated by the source agent. Default Value: Undefined
23	SRC_ADDR_INCR	Specifies whether the source location address is incremented by the SRC_TRANSFER_SIZE after each single data element transfer or not. 0: No increment, typically used for receive (RX) FIFO structures. 1: Increment, typically used for memory structures. Default Value: Undefined
22	SRC_TRANSFER_SIZE	Specifies the bus transfer size to the source location: 0: As specified by DATA_SIZE. 1: Word (32 bits). Distinguishing bus transfer size from data element size allows for source components with data elements that are smaller than their 32-bit bus interface width. E.g., an ADC source has a 32-bit bus transfer size, but only provides a 16-bit data element. Default Value: Undefined
21	DST_ADDR_INCR	Specifies whether the destination location address is incremented by the DST_TRANSFER_SIZE after each single data element transfer or not. 0 : No increment, typically used for transmit (TX) FIFO structures. 1: Increment, typically used for memory structures. Default Value: Undefined
20	DST_TRANSFER_SIZE	Specifies the bus transfer size to the destination location: 0: As specified by DATA_SIZE. 1: Word (32 bits). Distinguishing bus transfer size from data element size allows for destination components with data elements that are smaller than their 32-bit bus interface width. E.g., a DAC destination has a 32-bit bus transfer size, but only requires a 16-bit data element. Default Value: Undefined

(continued)

17 : 16	DATA_SIZE	Specifies the data element size: 0: Byte (8 bits). 1: Halfword (16 bits). 2: Word (32 bits). DATA_SIZE, SRC_TRANSFER_SIZE and DST_TRANSFER_SIZE together determine how data elements are transferred. The following are the 9 legal settings: - DATA is 8 bit, SRC is 8 bit, DST is 8 bit - DATA is 8 bit, SRC is 32 bit (higher 24 bits are dropped), DST is 8 bit - DATA is 8 bit, SRC is 8 bit, DST is 32 bit (higher 24 bits are made 0) - DATA is 8 bit, SRC is 32 bit (higher 24 bits are dropped), DST is 32 bit (higher 24 bits are made 0) - DATA is 16 bit, SRC is 16 bit, DST is 16 bit - DATA is 16 bit, SRC is 32 bit (higher 16 bits are dropped), DST is 16 bit - DATA is 16 bit, SRC is 16 bit, DST is 32 bit (higher 16 bits are made 0) - DATA is 16 bit, SRC is 32 bit (higher 16 bits are dropped), DST is 32 bit (higher 16 bits are made 0) - DATA is 32 bit, SRC is 32 bit, DST is 32 bit Default Value: Undefined
15 : 0	DATA_NR	Number of data elements that are transferred by a single descriptor. In DW mode (OPCODE is 0) each trigger initiates the transfer of a single data element. This field specifies the source and/or destination buffer size in data elements: buffer size = DATA_NR+1. The buffer is typically associated to a memory structure. In DMA mode (OPCODE is 1 or 2) each trigger initiates the transfer of DATA_NR+1 data elements. Default Value: Undefined

11.1.60 DMAC_DESCR7_PING_STATUS

Ping status word

Address: 0x401018EC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None					RW		
HW Access	None					RW		
Name	None [23:19]					RESPONSE [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	RW	None						
Name	VALID	None [30:24]						

Bits	Name	Description
31	VALID	0: Invalid, cannot be used for a data transfer. An attempt to use this descriptor for a data transfer will result in an INVALID_DESCR response code (and the interrupt cause bit is set to 1). 1: Valid. Hardware set this field to 0 when a descriptor is done, but only if CONTROL.INV_DESCR is 1. Software sets this field to 1 when a descriptor is initialized. Default Value: Undefined

(continued)

18 : 16	RESPONSE	Response code (the first two codes NO_ERROR and DONE are the result of normal behavior, the other codes are the result of erroneous behavior). 0/NO_ERROR: No error. Setting this response does NOT set the interrupt cause bit to 1. STATUS.VALID is NOT affected. CHi_CTL.ENABLED is NOT affected. CHi_CTL.PING_PONG is not updated. This response is used for an unused or not completed descriptor. Software should set the RESPONSE field to 0/NO_ERROR during descriptor initialization. 1/DONE: Descriptor is done (without errors). Setting this response sets the interrupt cause bit to 1 if CONTROL.SET_CAUSE is 1. STATUS.VALID is set to 0 if CONTROL.INV_DESCR is 1. CHi_CTL.ENABLED is NOT affected. CHi_CTL.PING_PONG is updated if CONTROL.FLIPPING is 1. 2/SRC_BUS_ERROR: Bus error while loading data from the source location. Setting this response sets the interrupt cause bit to 1. STATUS.VALID is set 0. CHi_CTL.ENABLED is set to 0. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). 3/DST_BUS_ERROR: Bus error while storing data to the destination location. Setting this response sets the interrupt cause bit to 1. STATUS.VALID is set 0. CHi_CTL.ENABLED is set to 0. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). 4/SRC_MISAL: Misalignment of source address. This occurs on a 16-bit bus transfer that is not 2-byte aligned or on a 32-bit bus transfer that is not 4-byte aligned. Setting this response sets the interrupt cause bit to 1. STATUS.VALID is set 0. CHi_CTL.ENABLED is set to 0. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). 5/DST_MISAL: Misalignment of destination address. This occurs on a 16-bit bus transfer that is not 2-byte aligned or on a 32-bit bus transfer that is not 4-byte aligned. Setting this response sets the interrupt cause bit to 1. STATUS.VALID is set 0. CHi_CTL.ENABLED is set to 0. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). 6/INVALID_DESCR: Invalid descriptor (STATUS.VALID is 0). This occurs when an activated channel has an invalid descriptor. CHi_CTL.ENABLED is set to 0. CHi_CTL.PING_PONG is not updated (it identifies the descriptor that caused the error). Default Value: Undefined
15 : 0	CURR_DATA_NR	Specifies the index of the current data transfer. This value increases from 0 to CONTROL.DATA_NR. HW sets this field: - When a descriptor is done (RESPONSE is DONE), the field is set to "0" when PING_CTL.INV_DESCR is '0' and the field is set to PING_CTL.DATA_NR when PING_CTL.INV_DESCR is '1'. - When a descriptor is not done (RESPONSE is NO_ERROR), the field reflects the progress of a data transfer. - In case of erroneous behavior (RESPONSE is neither DONE or NO_ERROR), the field is not updated, but keeps its value to ease debugging. HW only modifies this field for an active descriptor (STATUS.VALID to be 1). At descriptor initialization, SW should set this field to 0. This field allows software to read the progress of the data transfer. Note that SRC.ADDR and DST.ADDR represent base addresses and are not modified during data transfer. However, STATUS.CURR_DATA_NR is modified during data transfer and provides an offset wrt. the base addresses. Default Value: Undefined

11.1.61 DMAC_DESCR7_PONG_SRC

Pong source address

Address: 0x401018F0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	See description of PING_SRC. Default Value: Undefined

11.1.62 DMAC_DESCR7_PONG_DST

Pong destination address

Address: 0x401018F4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	See description of PING_DST. Default Value: Undefined

11.1.63 DMAC_DESCR7_PONG_CTL

Pong control word

Address: 0x401018F8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	None		RW	
HW Access	RW	RW	RW	RW	None		RW	
Name	SRC_ADDR_INCR	SRC_TRANSFER_SIZE	DST_ADDR_INCR	DST_TRANSFER_SIZE	None [19:18]		DATA_SIZE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW		RW	RW	RW	RW	RW	
HW Access	RW		RW	RW	RW	RW	RW	
Name	OPCODE [31:30]		FLIPPING	PREEMPT-ABLE	SET_CAUSE	INV_DESCR	WAIT_FOR_DEACT [25:24]	

Bits	Name	Description
31 : 30	OPCODE	See description of PING_CTL. Default Value: Undefined
29	FLIPPING	See description of PING_CTL. Default Value: Undefined
28	PREEMPTABLE	See description of PING_CTL. Default Value: Undefined
27	SET_CAUSE	See description of PING_CTL. Default Value: Undefined
26	INV_DESCR	See description of PING_CTL. Default Value: Undefined
25 : 24	WAIT_FOR_DEACT	See description of PING_CTL. Default Value: Undefined
23	SRC_ADDR_INCR	See description of PING_CTL. Default Value: Undefined

(continued)

22	SRC_TRANSFER_SIZE	See description of PING_CTL. Default Value: Undefined
21	DST_ADDR_INCR	See description of PING_CTL. Default Value: Undefined
20	DST_TRANSFER_SIZE	See description of PING_CTL. Default Value: Undefined
17 : 16	DATA_SIZE	See description of PING_CTL. Default Value: Undefined
15 : 0	DATA_NR	See description of PING_CTL. Default Value: Undefined

11.1.64 DMAC_DESCR7_PONG_STATUS

Pong status word

Address: 0x401018FC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None					RW		
HW Access	None					RW		
Name	None [23:19]					RESPONSE [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	RW	None						
Name	VALID	None [30:24]						

Bits	Name	Description
31	VALID	See description of PING_STATUS. Default Value: Undefined
18 : 16	RESPONSE	See description of PING_STATUS. Default Value: Undefined
15 : 0	CURR_DATA_NR	See description of PING_STATUS. Default Value: Undefined

12 CapSense Sigma Delta (CSD) Registers

This section discusses the CSD registers. It lists all the registers in mapping tables, in address order.

12.1 Register Details

Register Name	Address
CSD_ID	0x40280000
CSD_INTR	0x40280014
CSD_INTR_SET	0x40280018
CSD_PWM	0x4028001C

12.1.1 CSD_ID

ID & Revision Number

Address: 0x40280000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	ID [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	REVISION [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	REVISION [31:24]							

Bits	Name	Description
31 : 16	REVISION	the version number is 0x0001 Default Value: 1
15 : 0	ID	the ID of CSD peripheral is 0xE0E1 Default Value: 57569

12.1.2 CSD_INTR

CSD Interrupt Request Register

Address: 0x40280014

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1C
HW Access	None							RW1S
Name	None [7:1]							CSD

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	CSD	The CSD IRQ bit is set. Firmware must clear this bit as part of the interrupt handler. Default Value: 0

12.1.3 CSD_INTR_SET

CSD Interrupt set register

Address: 0x40280018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1S
HW Access	None							A
Name	None [7:1]							CSD

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	CSD	Only for debug/test purpose this field can be set to '1' to set corresponding bit in interrupt request register INTR. Default Value: 0

12.1.4 CSD_PWM

CSD PWM Register

Address: 0x4028001C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW		RW			
HW Access	None		R		R			
Name	None [7:6]		PWM_SEL [5:4]		PWM_COUNT [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 4	PWM_SEL	The mode of the PWM modulator Default Value: 0 **0x0: OFF:** The PWM modulator is OFF and it has no effect on sensor clock generated by PRS/divide-by-2 **0x2: FIXED_HIGH:** The PWM modulator changes the low phase of sensor clock to a fixed length (used during negative charge transfer mode). **0x3: FIXED_LOW:** The PWM modulator changes the high phase of sensor clock to a fixed length (used during positive charge transfer mode).
3 : 0	PWM_COUNT	Pulse widht modulation can be used to change the length of sensor clock pulse (low time/high time) when using PRS/Divide-by-2 as source of sensor clock. The length of the sensor clock pulse low/high time is multiples of clk_csd2 cycles. Default Value: 0

13 Continuous Time Block Mini (CTBM)

This section discusses the CTBM registers. It lists all the registers in mapping tables, in address order.

13.1 Register Details

Register Name	Address
CTBM0_CTB_CTRL	0x40300000
CTBM0_OA_RES0_CTRL	0x40300004
CTBM0_OA_RES1_CTRL	0x40300008
CTBM0_COMP_STAT	0x4030000C
CTBM0_INTR	0x40300020
CTBM0_INTR_SET	0x40300024
CTBM0_INTR_MASK	0x40300028
CTBM0_INTR_MASKED	0x4030002C
CTBM0_DFT_CTRL	0x40300030
CTBM0_OA0_SW	0x40300080
CTBM0_OA0_SW_CLEAR	0x40300084
CTBM0_OA1_SW	0x40300088
CTBM0_OA1_SW_CLEAR	0x4030008C
CTBM0_CTB_SW_HW_CTRL	0x403000C0
CTBM0_CTB_SW_STATUS	0x403000C4
CTBM0_OA0_OFFSET_TRIM	0x40300F00
CTBM0_OA0_SLOPE_OFFSET_TRIM	0x40300F04
CTBM0_OA0_COMP_TRIM	0x40300F08
CTBM0_OA1_OFFSET_TRIM	0x40300F0C
CTBM0_OA1_SLOPE_OFFSET_TRIM	0x40300F10
CTBM0_OA1_COMP_TRIM	0x40300F14
CTBM1_CTB_CTRL	0x40310000
CTBM1_OA_RES0_CTRL	0x40310004
CTBM1_OA_RES1_CTRL	0x40310008
CTBM1_COMP_STAT	0x4031000C
CTBM1_INTR	0x40310020
CTBM1_INTR_SET	0x40310024

Register Name	Address
CTBM1_INTR_MASK	0x40310028
CTBM1_INTR_MASKED	0x4031002C
CTBM1_DFT_CTRL	0x40310030
CTBM1_OA0_SW	0x40310080
CTBM1_OA0_SW_CLEAR	0x40310084
CTBM1_OA1_SW	0x40310088
CTBM1_OA1_SW_CLEAR	0x4031008C
CTBM1_CTB_SW_HW_CTRL	0x403100C0
CTBM1_CTB_SW_STATUS	0x403100C4
CTBM1_OA0_OFFSET_TRIM	0x40310F00
CTBM1_OA0_SLOPE_OFFSET_TRIM	0x40310F04
CTBM1_OA0_COMP_TRIM	0x40310F08
CTBM1_OA1_OFFSET_TRIM	0x40310F0C
CTBM1_OA1_SLOPE_OFFSET_TRIM	0x40310F10
CTBM1_OA1_COMP_TRIM	0x40310F14

13.1.1 CTBM0_CTB_CTRL

global CTB and power control

Address: 0x40300000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None					
HW Access	R	R	None					
Name	ENABLED	DEEPSLEEP_ON	None [29:24]					

Bits	Name	Description
31	ENABLED	- 0: CTB IP disabled (put analog in power down, open all switches) - 1: CTB IP enabled Default Value: 0
30	DEEPSLEEP_ON	- 0: CTB IP disabled off during DeepSleep power mode - 1: CTB IP remains enabled during DeepSleep power mode (if ENABLED=1) Default Value: 0

13.1.2 CTBM0_OA_RES0_CTRL

Opamp0 and resistor0 control

Address: 0x40300004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	None	RW	RW	
HW Access	R	R	R	R	None	R	R	
Name	OA0_DSI_LEVEL	OA0_BYPASS_DSI_SYNC	OA0_HYST_EN	OA0_COMP_EN	None	OA0_DRIVE_STR_SEL	OA0_PWR_MODE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	None	RW	
HW Access	None				R	None	R	
Name	None [15:12]				OA0_PUMP_EN	None	OA0_COMPINT [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	OA0_PUMP_EN	Opamp0 pump enable Default Value: 0
9 : 8	OA0_COMPINT	Opamp0 comparator edge detect Default Value: 0 **0x0: DISABLE:** Disabled, no interrupts will be detected **0x1: RISING:** Rising edge **0x2: FALLING:** Falling edge **0x3: BOTH:** Both rising and falling edges
7	OA0_DSI_LEVEL	Opamp0 comparator DSI (trigger) out level : 0=pulse, 1=level Default Value: 0

(continued)

6	OA0_BYPASS_DSI_SYNC	Opamp0 bypass comparator output synchronization for DSI (trigger) output: 0=synchronize (level or pulse), 1=bypass (output async) Default Value: 0
5	OA0_HYST_EN	Opamp0 hysteresis enable (10mV) Default Value: 0
4	OA0_COMP_EN	Opamp0 comparator enable Default Value: 0
2	OA0_DRIVE_STR_SEL	Opamp0 output strenght select 0=1x, 1=10x Default Value: 0
1 : 0	OA0_PWR_MODE	Opamp0 power level: 0=off Default Value: 0

13.1.3 CTBM0_OA_RES1_CTRL

Opamp1 and resistor1 control

Address: 0x40300008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	None	RW	RW	
HW Access	R	R	R	R	None	R	R	
Name	OA1_DSI_LEVEL	OA1_BYPASS_DSI_SYNC	OA1_HYST_EN	OA1_COMP_EN	None	OA1_DRIVE_STR_SEL	OA1_PWR_MODE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	None	RW	
HW Access	None				R	None	R	
Name	None [15:12]				OA1_PUMP_EN	None	OA1_COMPINT [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	OA1_PUMP_EN	Opamp1 pump enable Default Value: 0
9 : 8	OA1_COMPINT	Opamp0 comparator edge detect Default Value: 0 **0x0: DISABLE:** Disabled, no interrupts will be detected **0x1: RISING:** Rising edge **0x2: FALLING:** Falling edge **0x3: BOTH:** Both rising and falling edges
7	OA1_DSI_LEVEL	Opamp0 comparator DSI (trigger) out level : 0=pulse, 1=level Default Value: 0

(continued)

6	OA1_BYPASS_DSI_SYNC	Opamp1 bypass comparator output synchronization for DSI output: 0=synchronize, 1=bypass Default Value: 0
5	OA1_HYST_EN	Opamp1 hysteresis enable (10mV) Default Value: 0
4	OA1_COMP_EN	Opamp1 comparator enable Default Value: 0
2	OA1_DRIVE_STR_SEL	Opamp1 output strenght select 0=1x, 1=10x Default Value: 0
1 : 0	OA1_PWR_MODE	Opamp1 power level: 0=off Default Value: 0

13.1.4 CTBM0_COMP_STAT

Comparator status

Address: 0x4030000C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							W
Name	None [7:1]							OA0_COMP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							R
HW Access	None							W
Name	None [23:17]							OA1_COMP

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
16	OA1_COMP	Opamp1 current comparator status Default Value: 0
0	OA0_COMP	Opamp0 current comparator status Default Value: 0

13.1.5 CTBM0_INTR

Interrupt request register

Address: 0x40300020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1C	RW1C
HW Access	None						RW1S	RW1S
Name	None [7:2]						COMP1	COMP0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	COMP1	Comparator 1 Interrupt: hardware sets this interrupt when comparator 1 triggers. Write with '1' to clear bit. Default Value: 0
0	COMP0	Comparator 0 Interrupt: hardware sets this interrupt when comparator 0 triggers. Write with '1' to clear bit. Default Value: 0

13.1.6 CTBM0_INTR_SET

Interrupt request set register

Address: 0x40300024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1S	RW1S
HW Access	None						A	A
Name	None [7:2]						COMP1_SET	COMP0_SET

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	COMP1_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	COMP0_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

13.1.7 CTBM0_INTR_MASK

Interrupt request mask

Address: 0x40300028

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						COMP1_MASK	COMP0_MASK

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	COMP1_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	COMP0_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0

13.1.8 CTBM0_INTR_MASKED

Interrupt request masked

Address: 0x4030002C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						W	W
Name	None [7:2]						COMP1_MASKED	COMP0_MASKED

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	COMP1_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
0	COMP0_MASKED	Logical and of corresponding request and mask bits. Default Value: 0

13.1.9 CTBM0_DFT_CTRL

Was 'Analog DfT controls', now used as Risk Mitigation bits (RMP)

Address: 0x40300030

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW		
HW Access	None					R		
Name	None [7:3]					DFT_MODE [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	DFT_EN	None [30:24]						

Bits	Name	Description
31	DFT_EN	this bit is combined with the 3 bits 2:0, to form RMP[3:0] Default Value: 0
2 : 0	DFT_MODE	this bit is combined with bit 31, to form RMP[3:0], it must always be written with '3' for correct operation. Default Value: 0

13.1.10 CTBM0_OA0_SW

Opamp0 switch control

Address: 0x40300080

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1S	RW1S	None	RW1S
HW Access	None				RW1C	RW1C	None	RW1C
Name	None [7:4]				OA0P_A30	OA0P_A20	None	OA0P_A00

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW1S	None					RW1S
HW Access	None	RW1C	None					RW1C
Name	None	OA0M_A81	None [13:9]					OA0M_A11

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW1S	None		RW1S	None	
HW Access	None		RW1C	None		RW1C	None	
Name	None [23:22]		OA0O_D81	None [20:19]		OA0O_D51	None [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
21	OA0O_D81	Opamp0 output switch to short 1x with 10x drive Default Value: 0
18	OA0O_D51	Opamp0 output sarbus0 (ctbbus2 in CTB) Default Value: 0
14	OA0M_A81	Opamp0 negative terminal Opamp0 bottom Default Value: 0
8	OA0M_A11	Opamp0 negative terminal P1 Default Value: 0
3	OA0P_A30	Opamp0 positive terminal ctbbus0 Default Value: 0
2	OA0P_A20	Opamp0 positive terminal P0 Default Value: 0
0	OA0P_A00	Opamp0 positive terminal amuxbusa Default Value: 0

13.1.11 CTBM0_OA0_SW_CLEAR

Opamp0 switch control clear

Address: 0x40300084

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1C	RW1C	None	RW1C
HW Access	None				A	A	None	A
Name	None [7:4]				OA0P_A30	OA0P_A20	None	OA0P_A00

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW1C	None					RW1C
HW Access	None	A	None					A
Name	None	OA0M_A81	None [13:9]					OA0M_A11

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW1C	None		RW1C	None	
HW Access	None		A	None		A	None	
Name	None [23:22]		OA0O_D81	None [20:19]		OA0O_D51	None [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
21	OA0O_D81	see corresponding bit in OA0_SW Default Value: 0
18	OA0O_D51	see corresponding bit in OA0_SW Default Value: 0
14	OA0M_A81	see corresponding bit in OA0_SW Default Value: 0
8	OA0M_A11	see corresponding bit in OA0_SW Default Value: 0
3	OA0P_A30	see corresponding bit in OA0_SW Default Value: 0
2	OA0P_A20	see corresponding bit in OA0_SW Default Value: 0
0	OA0P_A00	see corresponding bit in OA0_SW Default Value: 0

13.1.12 CTBM0_OA1_SW

Opamp1 switch control

Address: 0x40300088

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW1S	None		RW1S	RW1S
HW Access	None			RW1C	None		RW1C	RW1C
Name	None [7:5]			OA1P_A43	None [3:2]		OA1P_A13	OA1P_A03

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW1S	None					RW1S
HW Access	None	RW1C	None					RW1C
Name	None	OA1M_A82	None [13:9]					OA1M_A22

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW1S	None	RW1S	RW1S	None	
HW Access	None		RW1C	None	RW1C	RW1C	None	
Name	None [23:22]		OA1O_D82	None	OA1O_D62	OA1O_D52	None [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
21	OA1O_D82	Opamp1 output switch to short 1x with 10x drive Default Value: 0
19	OA1O_D62	Opamp1 output sarbus1 (ctbbus3 in CTB) Default Value: 0
18	OA1O_D52	Opamp1 output sarbus0 (ctbbus2 in CTB) Default Value: 0
14	OA1M_A82	Opamp1 negative terminal Opamp1 bottom Default Value: 0
8	OA1M_A22	Opamp1 negative terminal P4 Default Value: 0
4	OA1P_A43	Opamp1 positive terminal ctbbus1 Default Value: 0
1	OA1P_A13	Opamp1 positive terminal P5 Default Value: 0
0	OA1P_A03	Opamp1 positive terminal amuxbusb Default Value: 0

13.1.13 CTBM0_OA1_SW_CLEAR

Opamp1 switch control clear

Address: 0x4030008C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW1C	None		RW1C	RW1C
HW Access	None			A	None		A	A
Name	None [7:5]			OA1P_A43	None [3:2]		OA1P_A13	OA1P_A03

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW1C	None					RW1C
HW Access	None	A	None					A
Name	None	OA1M_A82	None [13:9]					OA1M_A22

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW1C	None	RW1C	RW1C	None	
HW Access	None		A	None	A	A	None	
Name	None [23:22]		OA1O_D82	None	OA1O_D62	OA1O_D52	None [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
21	OA1O_D82	see corresponding bit in OA1_SW Default Value: 0
19	OA1O_D62	see corresponding bit in OA1_SW Default Value: 0
18	OA1O_D52	see corresponding bit in OA1_SW Default Value: 0
14	OA1M_A82	see corresponding bit in OA1_SW Default Value: 0
8	OA1M_A22	see corresponding bit in OA1_SW Default Value: 0
4	OA1P_A43	see corresponding bit in OA1_SW Default Value: 0
1	OA1P_A13	see corresponding bit in OA1_SW Default Value: 0
0	OA1P_A03	see corresponding bit in OA1_SW Default Value: 0

13.1.14 CTBM0_CTB_SW_HW_CTRL

CTB bus switch control status

Address: 0x403000C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	None	
HW Access	None				R	R	None	
Name	None [7:4]				P3_HW_CTRL	P2_HW_CTRL	None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	P3_HW_CTRL	Pin P3 switches Default Value: 0
2	P2_HW_CTRL	Pin P2 switches Default Value: 0

13.1.15 CTBM0_CTB_SW_STATUS

CTB bus switch control status

Address: 0x403000C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None	R	R	R	None			
HW Access	None	W	W	W	None			
Name	None	OA1O_D62_STAT	OA1O_D52_STAT	OA0O_D51_STAT	None [27:24]			

Bits	Name	Description
30	OA1O_D62_STAT	see OA1O_D62 bit in OA1_SW Default Value: 0
29	OA1O_D52_STAT	see OA1O_D52 bit in OA1_SW Default Value: 0
28	OA0O_D51_STAT	see OA0O_D51 bit in OA0_SW Default Value: 0

13.1.16 CTBM0_OA0_OFFSET_TRIM

Opamp0 trim control

Address: 0x40300F00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		OA0_OFFSET_TRIM [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	OA0_OFFSET_TRIM	Opamp0 offset trim Default Value: 0

13.1.17 CTBM0_OA0_SLOPE_OFFSET_TRIM

Opamp0 trim control

Address: 0x40300F04

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		OA0_SLOPE_OFFSET_TRIM [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	OA0_SLOPE_OFFSET_TRIM	Opamp0 slope offset drift trim Default Value: 0

13.1.18 CTBM0_OA0_COMP_TRIM

Opamp0 trim control

Address: 0x40300F08

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	
HW Access	None						R	
Name	None [7:2]						OA0_COMP_TRIM [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1 : 0	OA0_COMP_TRIM	Opamp0 Compenation Capacitor Trim Default Value: 0

13.1.19 CTBM0_OA1_OFFSET_TRIM

Opamp1 trim control

Address: 0x40300F0C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		OA1_OFFSET_TRIM [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	OA1_OFFSET_TRIM	Opamp1 offset trim Default Value: 0

13.1.20 CTBM0_OA1_SLOPE_OFFSET_TRIM

Opamp1 trim control

Address: 0x40300F10

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		OA1_SLOPE_OFFSET_TRIM [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	OA1_SLOPE_OFFSET_TRIM	Opamp1 slope offset drift trim Default Value: 0

13.1.21 CTBM0_OA1_COMP_TRIM

Opamp1 trim control

Address: 0x40300F14

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	
HW Access	None						R	
Name	None [7:2]						OA1_COMP_TRIM [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1 : 0	OA1_COMP_TRIM	Opamp1 Compenation Capacitor Trim Default Value: 0

13.1.22 CTBM1_CTB_CTRL

global CTB and power control

Address: 0x40310000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None					
HW Access	R	R	None					
Name	ENABLED	DEEPSLEEP_ON	None [29:24]					

Bits	Name	Description
31	ENABLED	- 0: CTB IP disabled (put analog in power down, open all switches) - 1: CTB IP enabled Default Value: 0
30	DEEPSLEEP_ON	- 0: CTB IP disabled off during DeepSleep power mode - 1: CTB IP remains enabled during DeepSleep power mode (if ENABLED=1) Default Value: 0

13.1.23 CTBM1_OA_RES0_CTRL

Opamp0 and resistor0 control

Address: 0x40310004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	None	RW	RW	
HW Access	R	R	R	R	None	R	R	
Name	OA0_DSI_LEVEL	OA0_BYPASS_DSI_SYNC	OA0_HYST_EN	OA0_COMP_EN	None	OA0_DRIVE_STR_SEL	OA0_PWR_MODE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	None	RW	
HW Access	None				R	None	R	
Name	None [15:12]				OA0_PUMP_EN	None	OA0_COMPINT [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	OA0_PUMP_EN	Opamp0 pump enable Default Value: 0
9 : 8	OA0_COMPINT	Opamp0 comparator edge detect Default Value: 0 **0x0: DISABLE:** Disabled, no interrupts will be detected **0x1: RISING:** Rising edge **0x2: FALLING:** Falling edge **0x3: BOTH:** Both rising and falling edges
7	OA0_DSI_LEVEL	Opamp0 comparator DSI (trigger) out level : 0=pulse, 1=level Default Value: 0

(continued)

6	OA0_BYPASS_DSI_SYNC	Opamp0 bypass comparator output synchronization for DSI (trigger) output: 0=synchronize (level or pulse), 1=bypass (output async) Default Value: 0
5	OA0_HYST_EN	Opamp0 hysteresis enable (10mV) Default Value: 0
4	OA0_COMP_EN	Opamp0 comparator enable Default Value: 0
2	OA0_DRIVE_STR_SEL	Opamp0 output strenght select 0=1x, 1=10x Default Value: 0
1 : 0	OA0_PWR_MODE	Opamp0 power level: 0=off Default Value: 0

13.1.24 CTBM1_OA_RES1_CTRL

Opamp1 and resistor1 control

Address: 0x40310008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	None	RW	RW	
HW Access	R	R	R	R	None	R	R	
Name	OA1_DSI_LEVEL	OA1_BYPASS_DSI_SYNC	OA1_HYST_EN	OA1_COMP_EN	None	OA1_DRIVE_STR_SEL	OA1_PWR_MODE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	None	RW	
HW Access	None				R	None	R	
Name	None [15:12]				OA1_PUMP_EN	None	OA1_COMPINT [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	OA1_PUMP_EN	Opamp1 pump enable Default Value: 0
9 : 8	OA1_COMPINT	Opamp0 comparator edge detect Default Value: 0 **0x0: DISABLE:** Disabled, no interrupts will be detected **0x1: RISING:** Rising edge **0x2: FALLING:** Falling edge **0x3: BOTH:** Both rising and falling edges
7	OA1_DSI_LEVEL	Opamp0 comparator DSI (trigger) out level : 0=pulse, 1=level Default Value: 0

(continued)

6	OA1_BYPASS_DSI_SYNC	Opamp1 bypass comparator output synchronization for DSI output: 0=synchronize, 1=bypass Default Value: 0
5	OA1_HYST_EN	Opamp1 hysteresis enable (10mV) Default Value: 0
4	OA1_COMP_EN	Opamp1 comparator enable Default Value: 0
2	OA1_DRIVE_STR_SEL	Opamp1 output strenght select 0=1x, 1=10x Default Value: 0
1 : 0	OA1_PWR_MODE	Opamp1 power level: 0=off Default Value: 0

13.1.25 CTBM1_COMP_STAT

Comparator status

Address: 0x4031000C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							W
Name	None [7:1]							OA0_COMP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							R
HW Access	None							W
Name	None [23:17]							OA1_COMP

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
16	OA1_COMP	Opamp1 current comparator status Default Value: 0
0	OA0_COMP	Opamp0 current comparator status Default Value: 0

13.1.26 CTBM1_INTR

Interrupt request register

Address: 0x40310020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1C	RW1C
HW Access	None						RW1S	RW1S
Name	None [7:2]						COMP1	COMP0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	COMP1	Comparator 1 Interrupt: hardware sets this interrupt when comparator 1 triggers. Write with '1' to clear bit. Default Value: 0
0	COMP0	Comparator 0 Interrupt: hardware sets this interrupt when comparator 0 triggers. Write with '1' to clear bit. Default Value: 0

13.1.27 CTBM1_INTR_SET

Interrupt request set register

Address: 0x40310024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1S	RW1S
HW Access	None						A	A
Name	None [7:2]						COMP1_SET	COMP0_SET

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	COMP1_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	COMP0_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

13.1.28 CTBM1_INTR_MASK

Interrupt request mask

Address: 0x40310028

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						COMP1_MASK	COMP0_MASK

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	COMP1_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	COMP0_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0

13.1.29 CTBM1_INTR_MASKED

Interrupt request masked

Address: 0x4031002C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						W	W
Name	None [7:2]						COMP1_MASKED	COMP0_MASKED

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	COMP1_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
0	COMP0_MASKED	Logical and of corresponding request and mask bits. Default Value: 0

13.1.30 CTBM1_DFT_CTRL

Was 'Analog DfT controls', now used as Risk Mitigation bits (RMP)

Address: 0x40310030

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW		
HW Access	None					R		
Name	None [7:3]					DFT_MODE [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	DFT_EN	None [30:24]						

Bits	Name	Description
31	DFT_EN	this bit is combined with the 3 bits 2:0, to form RMP[3:0] Default Value: 0
2 : 0	DFT_MODE	this bit is combined with bit 31, to form RMP[3:0], it must always be written with '3' for correct operation. Default Value: 0

13.1.31 CTBM1_OA0_SW

Opamp0 switch control

Address: 0x40310080

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1S	RW1S	None	RW1S
HW Access	None				RW1C	RW1C	None	RW1C
Name	None [7:4]				OA0P_A30	OA0P_A20	None	OA0P_A00

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW1S	None					RW1S
HW Access	None	RW1C	None					RW1C
Name	None	OA0M_A81	None [13:9]					OA0M_A11

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW1S	None		RW1S	None	
HW Access	None		RW1C	None		RW1C	None	
Name	None [23:22]		OA0O_D81	None [20:19]		OA0O_D51	None [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
21	OA0O_D81	Opamp0 output switch to short 1x with 10x drive Default Value: 0
18	OA0O_D51	Opamp0 output sarbus0 (ctbbus2 in CTB) Default Value: 0
14	OA0M_A81	Opamp0 negative terminal Opamp0 bottom Default Value: 0
8	OA0M_A11	Opamp0 negative terminal P1 Default Value: 0
3	OA0P_A30	Opamp0 positive terminal ctbbus0 Default Value: 0
2	OA0P_A20	Opamp0 positive terminal P0 Default Value: 0
0	OA0P_A00	Opamp0 positive terminal amuxbusa Default Value: 0

13.1.32 CTBM1_OA0_SW_CLEAR

Opamp0 switch control clear

Address: 0x40310084

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1C	RW1C	None	RW1C
HW Access	None				A	A	None	A
Name	None [7:4]				OA0P_A30	OA0P_A20	None	OA0P_A00

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW1C	None					RW1C
HW Access	None	A	None					A
Name	None	OA0M_A81	None [13:9]					OA0M_A11

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW1C	None		RW1C	None	
HW Access	None		A	None		A	None	
Name	None [23:22]		OA0O_D81	None [20:19]		OA0O_D51	None [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
21	OA0O_D81	see corresponding bit in OA0_SW Default Value: 0
18	OA0O_D51	see corresponding bit in OA0_SW Default Value: 0
14	OA0M_A81	see corresponding bit in OA0_SW Default Value: 0
8	OA0M_A11	see corresponding bit in OA0_SW Default Value: 0
3	OA0P_A30	see corresponding bit in OA0_SW Default Value: 0
2	OA0P_A20	see corresponding bit in OA0_SW Default Value: 0
0	OA0P_A00	see corresponding bit in OA0_SW Default Value: 0

13.1.33 CTBM1_OA1_SW

Opamp1 switch control

Address: 0x40310088

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW1S	None		RW1S	RW1S
HW Access	None			RW1C	None		RW1C	RW1C
Name	None [7:5]			OA1P_A43	None [3:2]		OA1P_A13	OA1P_A03

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW1S	None					RW1S
HW Access	None	RW1C	None					RW1C
Name	None	OA1M_A82	None [13:9]					OA1M_A22

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW1S	None	RW1S	RW1S	None	
HW Access	None		RW1C	None	RW1C	RW1C	None	
Name	None [23:22]		OA1O_D82	None	OA1O_D62	OA1O_D52	None [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
21	OA1O_D82	Opamp1 output switch to short 1x with 10x drive Default Value: 0
19	OA1O_D62	Opamp1 output sarbus1 (ctbbus3 in CTB) Default Value: 0
18	OA1O_D52	Opamp1 output sarbus0 (ctbbus2 in CTB) Default Value: 0
14	OA1M_A82	Opamp1 negative terminal Opamp1 bottom Default Value: 0
8	OA1M_A22	Opamp1 negative terminal P4 Default Value: 0
4	OA1P_A43	Opamp1 positive terminal ctbbus1 Default Value: 0
1	OA1P_A13	Opamp1 positive terminal P5 Default Value: 0
0	OA1P_A03	Opamp1 positive terminal amuxbusb Default Value: 0

13.1.34 CTBM1_OA1_SW_CLEAR

Opamp1 switch control clear

Address: 0x4031008C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW1C	None		RW1C	RW1C
HW Access	None			A	None		A	A
Name	None [7:5]			OA1P_A43	None [3:2]		OA1P_A13	OA1P_A03

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW1C	None					RW1C
HW Access	None	A	None					A
Name	None	OA1M_A82	None [13:9]					OA1M_A22

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW1C	None	RW1C	RW1C	None	
HW Access	None		A	None	A	A	None	
Name	None [23:22]		OA1O_D82	None	OA1O_D62	OA1O_D52	None [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
21	OA1O_D82	see corresponding bit in OA1_SW Default Value: 0
19	OA1O_D62	see corresponding bit in OA1_SW Default Value: 0
18	OA1O_D52	see corresponding bit in OA1_SW Default Value: 0
14	OA1M_A82	see corresponding bit in OA1_SW Default Value: 0
8	OA1M_A22	see corresponding bit in OA1_SW Default Value: 0
4	OA1P_A43	see corresponding bit in OA1_SW Default Value: 0
1	OA1P_A13	see corresponding bit in OA1_SW Default Value: 0
0	OA1P_A03	see corresponding bit in OA1_SW Default Value: 0

13.1.35 CTBM1_CTB_SW_HW_CTRL

CTB bus switch control status

Address: 0x403100C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	None	
HW Access	None				R	R	None	
Name	None [7:4]				P3_HW_CTRL	P2_HW_CTRL	None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	P3_HW_CTRL	Pin P3 switches Default Value: 0
2	P2_HW_CTRL	Pin P2 switches Default Value: 0

13.1.36 CTBM1_CTB_SW_STATUS

CTB bus switch control status

Address: 0x403100C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None	R	R	R	None			
HW Access	None	W	W	W	None			
Name	None	OA1O_D62_STAT	OA1O_D52_STAT	OA0O_D51_STAT	None [27:24]			

Bits	Name	Description
30	OA1O_D62_STAT	see OA1O_D62 bit in OA1_SW Default Value: 0
29	OA1O_D52_STAT	see OA1O_D52 bit in OA1_SW Default Value: 0
28	OA0O_D51_STAT	see OA0O_D51 bit in OA0_SW Default Value: 0

13.1.37 CTBM1_OA0_OFFSET_TRIM

Opamp0 trim control

Address: 0x40310F00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		OA0_OFFSET_TRIM [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	OA0_OFFSET_TRIM	Opamp0 offset trim Default Value: 0

13.1.38 CTBM1_OA0_SLOPE_OFFSET_TRIM

Opamp0 trim control

Address: 0x40310F04

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		OA0_SLOPE_OFFSET_TRIM [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	OA0_SLOPE_OFFSET_TRIM	Opamp0 slope offset drift trim Default Value: 0

13.1.39 CTBM1_OA0_COMP_TRIM

Opamp0 trim control

Address: 0x40310F08

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	
HW Access	None						R	
Name	None [7:2]						OA0_COMP_TRIM [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1 : 0	OA0_COMP_TRIM	Opamp0 Compenation Capacitor Trim Default Value: 0

13.1.40 CTBM1_OA1_OFFSET_TRIM

Opamp1 trim control

Address: 0x40310F0C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		OA1_OFFSET_TRIM [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	OA1_OFFSET_TRIM	Opamp1 offset trim Default Value: 0

13.1.41 CTBM1_OA1_SLOPE_OFFSET_TRIM

Opamp1 trim control

Address: 0x40310F10

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		OA1_SLOPE_OFFSET_TRIM [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	OA1_SLOPE_OFFSET_TRIM	Opamp1 slope offset drift trim Default Value: 0

13.1.42 CTBM1_OA1_COMP_TRIM

Opamp1 trim control

Address: 0x40310F14

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	
HW Access	None						R	
Name	None [7:2]						OA1_COMP_TRIM [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1 : 0	OA1_COMP_TRIM	Opamp1 Compenation Capacitor Trim Default Value: 0

14 Deep Sleep Amplifier Bias (DSAB) Registers

This section discusses the DSAB registers. It lists all the registers in mapping tables, in address order.

14.1 Register Details

Register Name	Address
PASS_DSAB_DSAB_CTRL	0x403F0E00
PASS_DSAB_DSAB_DFT	0x403F0E04

14.1.1 PASS_DSAB_DSAB_CTRL

global DSAB control

Address: 0x403F0E00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		CURRENT_SEL [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				SEL_OUT [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	ENABLED	None [30:24]						

Bits	Name	Description
31	ENABLED	- 0: DSAB IP disabled (put analog in power down, put all iref in bypass) - 1: DSAB IP enabled Default Value: 0
11 : 8	SEL_OUT	selection for ibias_out and irefout_ptat_2pt4 0: bypass respectively irefin_0tc_2pt4 and bypass irefin_ptat_2pt4 1: drive respectively replicated dsab_ibias and 0. Default Value: 0
5 : 0	CURRENT_SEL	current selection for dsab_ibias, dsab_ibias = CURRENT_SEL * 0.075 uA (+/-5%) Default Value: 0

14.1.2 PASS_DSAB_DSAB_DFT

DFT bits

Address: 0x403F0E04

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				EN_DFT [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	EN_DFT	- 0: DSAB DFT disabled - 1: DSAB DFT enabled (connect output to amuxbus) Default Value: 0

15 Digital System Interconnect (DSI) Registers

This section discusses the DSI registers. It lists all the registers in mapping tables, in address order.

15.1 Register Details

Register Name	Address
UDB_DSI3_HC0	0x400F4300
UDB_DSI3_HC1	0x400F4301
UDB_DSI3_HC2	0x400F4302
UDB_DSI3_HC3	0x400F4303
UDB_DSI3_HC4	0x400F4304
UDB_DSI3_HC5	0x400F4305
UDB_DSI3_HC6	0x400F4306
UDB_DSI3_HC7	0x400F4307
UDB_DSI3_HC8	0x400F4308
UDB_DSI3_HC9	0x400F4309
UDB_DSI3_HC10	0x400F430A
UDB_DSI3_HC11	0x400F430B
UDB_DSI3_HC12	0x400F430C
UDB_DSI3_HC13	0x400F430D
UDB_DSI3_HC14	0x400F430E
UDB_DSI3_HC15	0x400F430F
UDB_DSI3_HC16	0x400F4310
UDB_DSI3_HC17	0x400F4311
UDB_DSI3_HC18	0x400F4312
UDB_DSI3_HC19	0x400F4313
UDB_DSI3_HC20	0x400F4314
UDB_DSI3_HC21	0x400F4315
UDB_DSI3_HC22	0x400F4316
UDB_DSI3_HC23	0x400F4317
UDB_DSI3_HC24	0x400F4318
UDB_DSI3_HC25	0x400F4319

Register Name	Address
UDB_DSI3_HC26	0x400F431A
UDB_DSI3_HC27	0x400F431B
UDB_DSI3_HC28	0x400F431C
UDB_DSI3_HC29	0x400F431D
UDB_DSI3_HC30	0x400F431E
UDB_DSI3_HC31	0x400F431F
UDB_DSI3_HC32	0x400F4320
UDB_DSI3_HC33	0x400F4321
UDB_DSI3_HC34	0x400F4322
UDB_DSI3_HC35	0x400F4323
UDB_DSI3_HC36	0x400F4324
UDB_DSI3_HC37	0x400F4325
UDB_DSI3_HC38	0x400F4326
UDB_DSI3_HC39	0x400F4327
UDB_DSI3_HC40	0x400F4328
UDB_DSI3_HC41	0x400F4329
UDB_DSI3_HC42	0x400F432A
UDB_DSI3_HC43	0x400F432B
UDB_DSI3_HC44	0x400F432C
UDB_DSI3_HC45	0x400F432D
UDB_DSI3_HC46	0x400F432E
UDB_DSI3_HC47	0x400F432F
UDB_DSI3_HC48	0x400F4330
UDB_DSI3_HC49	0x400F4331
UDB_DSI3_HC50	0x400F4332
UDB_DSI3_HC51	0x400F4333
UDB_DSI3_HC52	0x400F4334
UDB_DSI3_HC53	0x400F4335
UDB_DSI3_HC54	0x400F4336
UDB_DSI3_HC55	0x400F4337
UDB_DSI3_HC56	0x400F4338
UDB_DSI3_HC57	0x400F4339
UDB_DSI3_HC58	0x400F433A
UDB_DSI3_HC59	0x400F433B
UDB_DSI3_HC60	0x400F433C
UDB_DSI3_HC61	0x400F433D
UDB_DSI3_HC62	0x400F433E
UDB_DSI3_HC63	0x400F433F
UDB_DSI3_HC64	0x400F4340
UDB_DSI3_HC65	0x400F4341

Register Name	Address
UDB_DSI3_HC66	0x400F4342
UDB_DSI3_HC67	0x400F4343
UDB_DSI3_HC68	0x400F4344
UDB_DSI3_HC69	0x400F4345
UDB_DSI3_HC70	0x400F4346
UDB_DSI3_HC71	0x400F4347
UDB_DSI3_HC72	0x400F4348
UDB_DSI3_HC73	0x400F4349
UDB_DSI3_HC74	0x400F434A
UDB_DSI3_HC75	0x400F434B
UDB_DSI3_HC76	0x400F434C
UDB_DSI3_HC77	0x400F434D
UDB_DSI3_HC78	0x400F434E
UDB_DSI3_HC79	0x400F434F
UDB_DSI3_HC80	0x400F4350
UDB_DSI3_HC81	0x400F4351
UDB_DSI3_HC82	0x400F4352
UDB_DSI3_HC83	0x400F4353
UDB_DSI3_HC84	0x400F4354
UDB_DSI3_HC85	0x400F4355
UDB_DSI3_HC86	0x400F4356
UDB_DSI3_HC87	0x400F4357
UDB_DSI3_HC88	0x400F4358
UDB_DSI3_HC89	0x400F4359
UDB_DSI3_HC90	0x400F435A
UDB_DSI3_HC91	0x400F435B
UDB_DSI3_HC92	0x400F435C
UDB_DSI3_HC93	0x400F435D
UDB_DSI3_HC94	0x400F435E
UDB_DSI3_HC95	0x400F435F
UDB_DSI3_HC96	0x400F4360
UDB_DSI3_HC97	0x400F4361
UDB_DSI3_HC98	0x400F4362
UDB_DSI3_HC99	0x400F4363
UDB_DSI3_HC100	0x400F4364
UDB_DSI3_HC101	0x400F4365
UDB_DSI3_HC102	0x400F4366
UDB_DSI3_HC103	0x400F4367
UDB_DSI3_HC104	0x400F4368
UDB_DSI3_HC105	0x400F4369

Register Name	Address
UDB_DSI3_HC106	0x400F436A
UDB_DSI3_HC107	0x400F436B
UDB_DSI3_HC108	0x400F436C
UDB_DSI3_HC109	0x400F436D
UDB_DSI3_HC110	0x400F436E
UDB_DSI3_HC111	0x400F436F
UDB_DSI3_HC112	0x400F4370
UDB_DSI3_HC113	0x400F4371
UDB_DSI3_HC114	0x400F4372
UDB_DSI3_HC115	0x400F4373
UDB_DSI3_HC116	0x400F4374
UDB_DSI3_HC117	0x400F4375
UDB_DSI3_HC118	0x400F4376
UDB_DSI3_HC119	0x400F4377
UDB_DSI3_HC120	0x400F4378
UDB_DSI3_HC121	0x400F4379
UDB_DSI3_HC122	0x400F437A
UDB_DSI3_HC123	0x400F437B
UDB_DSI3_HC124	0x400F437C
UDB_DSI3_HC125	0x400F437D
UDB_DSI3_HC126	0x400F437E
UDB_DSI3_HC127	0x400F437F
UDB_DSI3_HV_L0	0x400F4380
UDB_DSI3_HV_L1	0x400F4381
UDB_DSI3_HV_L2	0x400F4382
UDB_DSI3_HV_L3	0x400F4383
UDB_DSI3_HV_L4	0x400F4384
UDB_DSI3_HV_L5	0x400F4385
UDB_DSI3_HV_L6	0x400F4386
UDB_DSI3_HV_L7	0x400F4387
UDB_DSI3_HV_L8	0x400F4388
UDB_DSI3_HV_L9	0x400F4389
UDB_DSI3_HV_L10	0x400F438A
UDB_DSI3_HV_L11	0x400F438B
UDB_DSI3_HV_L12	0x400F438C
UDB_DSI3_HV_L13	0x400F438D
UDB_DSI3_HV_L14	0x400F438E
UDB_DSI3_HV_L15	0x400F438F
UDB_DSI3_HS0	0x400F4390
UDB_DSI3_HS1	0x400F4391

Register Name	Address
UDB_DSI3_HS2	0x400F4392
UDB_DSI3_HS3	0x400F4393
UDB_DSI3_HS4	0x400F4394
UDB_DSI3_HS5	0x400F4395
UDB_DSI3_HS6	0x400F4396
UDB_DSI3_HS7	0x400F4397
UDB_DSI3_HS8	0x400F4398
UDB_DSI3_HS9	0x400F4399
UDB_DSI3_HS10	0x400F439A
UDB_DSI3_HS11	0x400F439B
UDB_DSI3_HS12	0x400F439C
UDB_DSI3_HS13	0x400F439D
UDB_DSI3_HS14	0x400F439E
UDB_DSI3_HS15	0x400F439F
UDB_DSI3_HS16	0x400F43A0
UDB_DSI3_HS17	0x400F43A1
UDB_DSI3_HS18	0x400F43A2
UDB_DSI3_HS19	0x400F43A3
UDB_DSI3_HS20	0x400F43A4
UDB_DSI3_HS21	0x400F43A5
UDB_DSI3_HS22	0x400F43A6
UDB_DSI3_HS23	0x400F43A7
UDB_DSI3_HV_R0	0x400F43A8
UDB_DSI3_HV_R1	0x400F43A9
UDB_DSI3_HV_R2	0x400F43AA
UDB_DSI3_HV_R3	0x400F43AB
UDB_DSI3_HV_R4	0x400F43AC
UDB_DSI3_HV_R5	0x400F43AD
UDB_DSI3_HV_R6	0x400F43AE
UDB_DSI3_HV_R7	0x400F43AF
UDB_DSI3_HV_R8	0x400F43B0
UDB_DSI3_HV_R9	0x400F43B1
UDB_DSI3_HV_R10	0x400F43B2
UDB_DSI3_HV_R11	0x400F43B3
UDB_DSI3_HV_R12	0x400F43B4
UDB_DSI3_HV_R13	0x400F43B5
UDB_DSI3_HV_R14	0x400F43B6
UDB_DSI3_HV_R15	0x400F43B7
UDB_DSI3_DSIINP0	0x400F43C0
UDB_DSI3_DSIINP1	0x400F43C2

Register Name	Address
UDB_DSI3_DSIINP2	0x400F43C4
UDB_DSI3_DSIINP3	0x400F43C6
UDB_DSI3_DSIINP4	0x400F43C8
UDB_DSI3_DSIINP5	0x400F43CA
UDB_DSI3_DSIOUTP0	0x400F43CC
UDB_DSI3_DSIOUTP1	0x400F43CE
UDB_DSI3_DSIOUTP2	0x400F43D0
UDB_DSI3_DSIOUTP3	0x400F43D2
UDB_DSI3_DSIOUTT0	0x400F43D4
UDB_DSI3_DSIOUTT1	0x400F43D6
UDB_DSI3_DSIOUTT2	0x400F43D8
UDB_DSI3_DSIOUTT3	0x400F43DA
UDB_DSI3_DSIOUTT4	0x400F43DC
UDB_DSI3_DSIOUTT5	0x400F43DE
UDB_DSI3_VS0	0x400F43E0
UDB_DSI3_VS1	0x400F43E2
UDB_DSI3_VS2	0x400F43E4
UDB_DSI3_VS3	0x400F43E6
UDB_DSI3_VS4	0x400F43E8
UDB_DSI3_VS5	0x400F43EA
UDB_DSI3_VS6	0x400F43EC
UDB_DSI3_VS7	0x400F43EE

15.1.1 UDB_DSI3_HC0

DSI HC Tile Configuration

Address: 0x400F4300

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.2 UDB_DSI3_HC1

DSI HC Tile Configuration

Address: 0x400F4301

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.3 UDB_DSI3_HC2

DSI HC Tile Configuration

Address: 0x400F4302

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.4 UDB_DSI3_HC3

DSI HC Tile Configuration

Address: 0x400F4303

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.5 UDB_DSI3_HC4

DSI HC Tile Configuration

Address: 0x400F4304

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.6 UDB_DSI3_HC5

DSI HC Tile Configuration

Address: 0x400F4305

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.7 UDB_DSI3_HC6

DSI HC Tile Configuration

Address: 0x400F4306

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.8 UDB_DSI3_HC7

DSI HC Tile Configuration

Address: 0x400F4307

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.9 UDB_DSI3_HC8

DSI HC Tile Configuration

Address: 0x400F4308

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.10 UDB_DSI3_HC9

DSI HC Tile Configuration

Address: 0x400F4309

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.11 UDB_DSI3_HC10

DSI HC Tile Configuration

Address: 0x400F430A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.12 UDB_DSI3_HC11

DSI HC Tile Configuration

Address: 0x400F430B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.13 UDB_DSI3_HC12

DSI HC Tile Configuration

Address: 0x400F430C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.14 UDB_DSI3_HC13

DSI HC Tile Configuration

Address: 0x400F430D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.15 UDB_DSI3_HC14

DSI HC Tile Configuration

Address: 0x400F430E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.16 UDB_DSI3_HC15

DSI HC Tile Configuration

Address: 0x400F430F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.17 UDB_DSI3_HC16

DSI HC Tile Configuration

Address: 0x400F4310

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.18 UDB_DSI3_HC17

DSI HC Tile Configuration

Address: 0x400F4311

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.19 UDB_DSI3_HC18

DSI HC Tile Configuration

Address: 0x400F4312

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.20 UDB_DSI3_HC19

DSI HC Tile Configuration

Address: 0x400F4313

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.21 UDB_DSI3_HC20

DSI HC Tile Configuration

Address: 0x400F4314

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.22 UDB_DSI3_HC21

DSI HC Tile Configuration

Address: 0x400F4315

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.23 UDB_DSI3_HC22

DSI HC Tile Configuration

Address: 0x400F4316

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.24 UDB_DSI3_HC23

DSI HC Tile Configuration

Address: 0x400F4317

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.25 UDB_DSI3_HC24

DSI HC Tile Configuration

Address: 0x400F4318

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.26 UDB_DSI3_HC25

DSI HC Tile Configuration

Address: 0x400F4319

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.27 UDB_DSI3_HC26

DSI HC Tile Configuration

Address: 0x400F431A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.28 UDB_DSI3_HC27

DSI HC Tile Configuration

Address: 0x400F431B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.29 UDB_DSI3_HC28

DSI HC Tile Configuration

Address: 0x400F431C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.30 UDB_DSI3_HC29

DSI HC Tile Configuration

Address: 0x400F431D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.31 UDB_DSI3_HC30

DSI HC Tile Configuration

Address: 0x400F431E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.32 UDB_DSI3_HC31

DSI HC Tile Configuration

Address: 0x400F431F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.33 UDB_DSI3_HC32

DSI HC Tile Configuration

Address: 0x400F4320

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.34 UDB_DSI3_HC33

DSI HC Tile Configuration

Address: 0x400F4321

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.35 UDB_DSI3_HC34

DSI HC Tile Configuration

Address: 0x400F4322

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.36 UDB_DSI3_HC35

DSI HC Tile Configuration

Address: 0x400F4323

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.37 UDB_DSI3_HC36

DSI HC Tile Configuration

Address: 0x400F4324

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.38 UDB_DSI3_HC37

DSI HC Tile Configuration

Address: 0x400F4325

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.39 UDB_DSI3_HC38

DSI HC Tile Configuration

Address: 0x400F4326

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.40 UDB_DSI3_HC39

DSI HC Tile Configuration

Address: 0x400F4327

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.41 UDB_DSI3_HC40

DSI HC Tile Configuration

Address: 0x400F4328

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.42 UDB_DSI3_HC41

DSI HC Tile Configuration

Address: 0x400F4329

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.43 UDB_DSI3_HC42

DSI HC Tile Configuration

Address: 0x400F432A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.44 UDB_DSI3_HC43

DSI HC Tile Configuration

Address: 0x400F432B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.45 UDB_DSI3_HC44

DSI HC Tile Configuration

Address: 0x400F432C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.46 UDB_DSI3_HC45

DSI HC Tile Configuration

Address: 0x400F432D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.47 UDB_DSI3_HC46

DSI HC Tile Configuration

Address: 0x400F432E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.48 UDB_DSI3_HC47

DSI HC Tile Configuration

Address: 0x400F432F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.49 UDB_DSI3_HC48

DSI HC Tile Configuration

Address: 0x400F4330

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.50 UDB_DSI3_HC49

DSI HC Tile Configuration

Address: 0x400F4331

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.51 UDB_DSI3_HC50

DSI HC Tile Configuration

Address: 0x400F4332

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.52 UDB_DSI3_HC51

DSI HC Tile Configuration

Address: 0x400F4333

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.53 UDB_DSI3_HC52

DSI HC Tile Configuration

Address: 0x400F4334

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.54 UDB_DSI3_HC53

DSI HC Tile Configuration

Address: 0x400F4335

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.55 UDB_DSI3_HC54

DSI HC Tile Configuration

Address: 0x400F4336

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.56 UDB_DSI3_HC55

DSI HC Tile Configuration

Address: 0x400F4337

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.57 UDB_DSI3_HC56

DSI HC Tile Configuration

Address: 0x400F4338

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.58 UDB_DSI3_HC57

DSI HC Tile Configuration

Address: 0x400F4339

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.59 UDB_DSI3_HC58

DSI HC Tile Configuration

Address: 0x400F433A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.60 UDB_DSI3_HC59

DSI HC Tile Configuration

Address: 0x400F433B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.61 UDB_DSI3_HC60

DSI HC Tile Configuration

Address: 0x400F433C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.62 UDB_DSI3_HC61

DSI HC Tile Configuration

Address: 0x400F433D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.63 UDB_DSI3_HC62

DSI HC Tile Configuration

Address: 0x400F433E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.64 UDB_DSI3_HC63

DSI HC Tile Configuration

Address: 0x400F433F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.65 UDB_DSI3_HC64

DSI HC Tile Configuration

Address: 0x400F4340

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.66 UDB_DSI3_HC65

DSI HC Tile Configuration

Address: 0x400F4341

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.67 UDB_DSI3_HC66

DSI HC Tile Configuration

Address: 0x400F4342

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.68 UDB_DSI3_HC67

DSI HC Tile Configuration

Address: 0x400F4343

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.69 UDB_DSI3_HC68

DSI HC Tile Configuration

Address: 0x400F4344

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.70 UDB_DSI3_HC69

DSI HC Tile Configuration

Address: 0x400F4345

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.71 UDB_DSI3_HC70

DSI HC Tile Configuration

Address: 0x400F4346

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.72 UDB_DSI3_HC71

DSI HC Tile Configuration

Address: 0x400F4347

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.73 UDB_DSI3_HC72

DSI HC Tile Configuration

Address: 0x400F4348

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.74 UDB_DSI3_HC73

DSI HC Tile Configuration

Address: 0x400F4349

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.75 UDB_DSI3_HC74

DSI HC Tile Configuration

Address: 0x400F434A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.76 UDB_DSI3_HC75

DSI HC Tile Configuration

Address: 0x400F434B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.77 UDB_DSI3_HC76

DSI HC Tile Configuration

Address: 0x400F434C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.78 UDB_DSI3_HC77

DSI HC Tile Configuration

Address: 0x400F434D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.79 UDB_DSI3_HC78

DSI HC Tile Configuration

Address: 0x400F434E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.80 UDB_DSI3_HC79

DSI HC Tile Configuration

Address: 0x400F434F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.81 UDB_DSI3_HC80

DSI HC Tile Configuration

Address: 0x400F4350

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.82 UDB_DSI3_HC81

DSI HC Tile Configuration

Address: 0x400F4351

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.83 UDB_DSI3_HC82

DSI HC Tile Configuration

Address: 0x400F4352

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.84 UDB_DSI3_HC83

DSI HC Tile Configuration

Address: 0x400F4353

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.85 UDB_DSI3_HC84

DSI HC Tile Configuration

Address: 0x400F4354

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.86 UDB_DSI3_HC85

DSI HC Tile Configuration

Address: 0x400F4355

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.87 UDB_DSI3_HC86

DSI HC Tile Configuration

Address: 0x400F4356

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.88 UDB_DSI3_HC87

DSI HC Tile Configuration

Address: 0x400F4357

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.89 UDB_DSI3_HC88

DSI HC Tile Configuration

Address: 0x400F4358

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.90 UDB_DSI3_HC89

DSI HC Tile Configuration

Address: 0x400F4359

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.91 UDB_DSI3_HC90

DSI HC Tile Configuration

Address: 0x400F435A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.92 UDB_DSI3_HC91

DSI HC Tile Configuration

Address: 0x400F435B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.93 UDB_DSI3_HC92

DSI HC Tile Configuration

Address: 0x400F435C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.94 UDB_DSI3_HC93

DSI HC Tile Configuration

Address: 0x400F435D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.95 UDB_DSI3_HC94

DSI HC Tile Configuration

Address: 0x400F435E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.96 UDB_DSI3_HC95

DSI HC Tile Configuration

Address: 0x400F435F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.97 UDB_DSI3_HC96

DSI HC Tile Configuration

Address: 0x400F4360

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.98 UDB_DSI3_HC97

DSI HC Tile Configuration

Address: 0x400F4361

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.99 UDB_DSI3_HC98

DSI HC Tile Configuration

Address: 0x400F4362

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.100 UDB_DSI3_HC99

DSI HC Tile Configuration

Address: 0x400F4363

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.101 UDB_DSI3_HC100

DSI HC Tile Configuration

Address: 0x400F4364

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.102 UDB_DSI3_HC101

DSI HC Tile Configuration

Address: 0x400F4365

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.103 UDB_DSI3_HC102

DSI HC Tile Configuration

Address: 0x400F4366

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.104 UDB_DSI3_HC103

DSI HC Tile Configuration

Address: 0x400F4367

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.105 UDB_DSI3_HC104

DSI HC Tile Configuration

Address: 0x400F4368

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.106 UDB_DSI3_HC105

DSI HC Tile Configuration

Address: 0x400F4369

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.107 UDB_DSI3_HC106

DSI HC Tile Configuration

Address: 0x400F436A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.108 UDB_DSI3_HC107

DSI HC Tile Configuration

Address: 0x400F436B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.109 UDB_DSI3_HC108

DSI HC Tile Configuration

Address: 0x400F436C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.110 UDB_DSI3_HC109

DSI HC Tile Configuration

Address: 0x400F436D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.111 UDB_DSI3_HC110

DSI HC Tile Configuration

Address: 0x400F436E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.112 UDB_DSI3_HC111

DSI HC Tile Configuration

Address: 0x400F436F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.113 UDB_DSI3_HC112

DSI HC Tile Configuration

Address: 0x400F4370

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.114 UDB_DSI3_HC113

DSI HC Tile Configuration

Address: 0x400F4371

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.115 UDB_DSI3_HC114

DSI HC Tile Configuration

Address: 0x400F4372

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.116 UDB_DSI3_HC115

DSI HC Tile Configuration

Address: 0x400F4373

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.117 UDB_DSI3_HC116

DSI HC Tile Configuration

Address: 0x400F4374

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.118 UDB_DSI3_HC117

DSI HC Tile Configuration

Address: 0x400F4375

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.119 UDB_DSI3_HC118

DSI HC Tile Configuration

Address: 0x400F4376

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.120 UDB_DSI3_HC119

DSI HC Tile Configuration

Address: 0x400F4377

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.121 UDB_DSI3_HC120

DSI HC Tile Configuration

Address: 0x400F4378

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.122 UDB_DSI3_HC121

DSI HC Tile Configuration

Address: 0x400F4379

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.123 UDB_DSI3_HC122

DSI HC Tile Configuration

Address: 0x400F437A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.124 UDB_DSI3_HC123

DSI HC Tile Configuration

Address: 0x400F437B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.125 UDB_DSI3_HC124

DSI HC Tile Configuration

Address: 0x400F437C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.126 UDB_DSI3_HC125

DSI HC Tile Configuration

Address: 0x400F437D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.127 UDB_DSI3_HC126

DSI HC Tile Configuration

Address: 0x400F437E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.128 UDB_DSI3_HC127

DSI HC Tile Configuration

Address: 0x400F437F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.129 UDB_DSI3_HV_L0

DSI HV Tile Configuration; Left

Address: 0x400F4380

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.130 UDB_DSI3_HV_L1

DSI HV Tile Configuration; Left

Address: 0x400F4381

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.131 UDB_DSI3_HV_L2

DSI HV Tile Configuration; Left

Address: 0x400F4382

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.132 UDB_DSI3_HV_L3

DSI HV Tile Configuration; Left

Address: 0x400F4383

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.133 UDB_DSI3_HV_L4

DSI HV Tile Configuration; Left

Address: 0x400F4384

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.134 UDB_DSI3_HV_L5

DSI HV Tile Configuration; Left

Address: 0x400F4385

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.135 UDB_DSI3_HV_L6

DSI HV Tile Configuration; Left

Address: 0x400F4386

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.136 UDB_DSI3_HV_L7

DSI HV Tile Configuration; Left

Address: 0x400F4387

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.137 UDB_DSI3_HV_L8

DSI HV Tile Configuration; Left

Address: 0x400F4388

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.138 UDB_DSI3_HV_L9

DSI HV Tile Configuration; Left

Address: 0x400F4389

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.139 UDB_DSI3_HV_L10

DSI HV Tile Configuration; Left

Address: 0x400F438A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.140 UDB_DSI3_HV_L11

DSI HV Tile Configuration; Left

Address: 0x400F438B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.141 UDB_DSI3_HV_L12

DSI HV Tile Configuration; Left

Address: 0x400F438C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.142 UDB_DSI3_HV_L13

DSI HV Tile Configuration; Left

Address: 0x400F438D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.143 UDB_DSI3_HV_L14

DSI HV Tile Configuration; Left

Address: 0x400F438E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.144 UDB_DSI3_HV_L15

DSI HV Tile Configuration; Left

Address: 0x400F438F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.145 UDB_DSI3_HS0

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F4390

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.146 UDB_DSI3_HS1

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F4391

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.147 UDB_DSI3_HS2

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F4392

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.148 UDB_DSI3_HS3

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F4393

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.149 UDB_DSI3_HS4

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F4394

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.150 UDB_DSI3_HS5

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F4395

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.151 UDB_DSI3_HS6

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F4396

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.152 UDB_DSI3_HS7

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F4397

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.153 UDB_DSI3_HS8

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F4398

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.154 UDB_DSI3_HS9

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F4399

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.155 UDB_DSI3_HS10

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F439A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.156 UDB_DSI3_HS11

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F439B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.157 UDB_DSI3_HS12

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F439C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.158 UDB_DSI3_HS13

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F439D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.159 UDB_DSI3_HS14

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F439E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.160 UDB_DSI3_HS15

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F439F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.161 UDB_DSI3_HS16

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F43A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.162 UDB_DSI3_HS17

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F43A1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.163 UDB_DSI3_HS18

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F43A2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.164 UDB_DSI3_HS19

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F43A3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.165 UDB_DSI3_HS20

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F43A4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.166 UDB_DSI3_HS21

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F43A5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.167 UDB_DSI3_HS22

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F43A6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.168 UDB_DSI3_HS23

DSI HS Tile Configuration; Horizontal Segmentation

Address: 0x400F43A7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.169 UDB_DSI3_HV_R0

DSI HV Tile Configuration; Right

Address: 0x400F43A8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.170 UDB_DSI3_HV_R1

DSI HV Tile Configuration; Right

Address: 0x400F43A9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.171 UDB_DSI3_HV_R2

DSI HV Tile Configuration; Right

Address: 0x400F43AA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.172 UDB_DSI3_HV_R3

DSI HV Tile Configuration; Right

Address: 0x400F43AB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.173 UDB_DSI3_HV_R4

DSI HV Tile Configuration; Right

Address: 0x400F43AC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.174 UDB_DSI3_HV_R5

DSI HV Tile Configuration; Right

Address: 0x400F43AD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.175 UDB_DSI3_HV_R6

DSI HV Tile Configuration; Right

Address: 0x400F43AE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.176 UDB_DSI3_HV_R7

DSI HV Tile Configuration; Right

Address: 0x400F43AF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.177 UDB_DSI3_HV_R8

DSI HV Tile Configuration; Right

Address: 0x400F43B0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.178 UDB_DSI3_HV_R9

DSI HV Tile Configuration; Right

Address: 0x400F43B1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.179 UDB_DSI3_HV_R10

DSI HV Tile Configuration; Right

Address: 0x400F43B2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.180 UDB_DSI3_HV_R11

DSI HV Tile Configuration; Right

Address: 0x400F43B3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.181 UDB_DSI3_HV_R12

DSI HV Tile Configuration; Right

Address: 0x400F43B4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.182 UDB_DSI3_HV_R13

DSI HV Tile Configuration; Right

Address: 0x400F43B5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.183 UDB_DSI3_HV_R14

DSI HV Tile Configuration; Right

Address: 0x400F43B6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.184 UDB_DSI3_HV_R15

DSI HV Tile Configuration; Right

Address: 0x400F43B7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration for DSI channel bytes Default Value: X

15.1.185 UDB_DSI3_DSIINP0

DSI PI Tile Configuration for DSI I/O; Input

Address: 0x400F43C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks Default Value: X
3 : 0	PI_TOP	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks Default Value: X

15.1.186 UDB_DSI3_DSIINP1

DSI PI Tile Configuration for DSI I/O; Input

Address: 0x400F43C2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks Default Value: X
3 : 0	PI_TOP	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks Default Value: X

15.1.187 UDB_DSI3_DSIINP2

DSI PI Tile Configuration for DSI I/O; Input

Address: 0x400F43C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks Default Value: X
3 : 0	PI_TOP	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks Default Value: X

15.1.188 UDB_DSI3_DSIINP3

DSI PI Tile Configuration for DSI I/O; Input

Address: 0x400F43C6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks Default Value: X
3 : 0	PI_TOP	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks Default Value: X

15.1.189 UDB_DSI3_DSIINP4

DSI PI Tile Configuration for DSI I/O; Input

Address: 0x400F43C8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks Default Value: X
3 : 0	PI_TOP	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks Default Value: X

15.1.190 UDB_DSI3_DSIINP5

DSI PI Tile Configuration for DSI I/O; Input

Address: 0x400F43CA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks Default Value: X
3 : 0	PI_TOP	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks Default Value: X

15.1.191 UDB_DSI3_DSIOUTP0

DSI PI Tile Configuration for DSI I/O; Output pair

Address: 0x400F43CC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks Default Value: X
3 : 0	PI_TOP	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks Default Value: X

15.1.192 UDB_DSI3_DSIOUTP1

DSI PI Tile Configuration for DSI I/O; Output pair

Address: 0x400F43CE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks Default Value: X
3 : 0	PI_TOP	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks Default Value: X

15.1.193 UDB_DSI3_DSIOUTP2

DSI PI Tile Configuration for DSI I/O; Output pair

Address: 0x400F43D0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks Default Value: X
3 : 0	PI_TOP	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks Default Value: X

15.1.194 UDB_DSI3_DSIOUTP3

DSI PI Tile Configuration for DSI I/O; Output pair

Address: 0x400F43D2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks Default Value: X
3 : 0	PI_TOP	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks Default Value: X

15.1.195 UDB_DSI3_DSIOUTT0

DSI PI Tile Configuration for DSI I/O; Output triplet

Address: 0x400F43D4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks Default Value: X
3 : 0	PI_TOP	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks Default Value: X

15.1.196 UDB_DSI3_DSIOUTT1

DSI PI Tile Configuration for DSI I/O; Output triplet

Address: 0x400F43D6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks Default Value: X
3 : 0	PI_TOP	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks Default Value: X

15.1.197 UDB_DSI3_DSIOUTT2

DSI PI Tile Configuration for DSI I/O; Output triplet

Address: 0x400F43D8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks Default Value: X
3 : 0	PI_TOP	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks Default Value: X

15.1.198 UDB_DSI3_DSIOUTT3

DSI PI Tile Configuration for DSI I/O; Output triplet

Address: 0x400F43DA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks Default Value: X
3 : 0	PI_TOP	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks Default Value: X

15.1.199 UDB_DSI3_DSIOUTT4

DSI PI Tile Configuration for DSI I/O; Output triplet

Address: 0x400F43DC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks Default Value: X
3 : 0	PI_TOP	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks Default Value: X

15.1.200 UDB_DSI3_DSIOUTT5

DSI PI Tile Configuration for DSI I/O; Output triplet

Address: 0x400F43DE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration for BOTTOM DSI port interface, not implemented in TOP DSI blocks Default Value: X
3 : 0	PI_TOP	RAM configuration for TOP DSI port interface, not implemented in BOTTOM DSI blocks Default Value: X

15.1.201 UDB_DSI3_VS0

DSI VS Tile Configuration; Vertical Segmentation

Address: 0x400F43E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	VS_BOT [7:4]				VS_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	VS_BOT	RAM configuration for BOTTOM DSI vertical segmentation, not implemented in TOP DSI blocks Default Value: X
3 : 0	VS_TOP	RAM configuration for TOP DSI vertical segmentation, not implemented in BOTTOM DSI blocks Default Value: X

15.1.202 UDB_DSI3_VS1

DSI VS Tile Configuration; Vertical Segmentation

Address: 0x400F43E2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	VS_BOT [7:4]				VS_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	VS_BOT	RAM configuration for BOTTOM DSI vertical segmentation, not implemented in TOP DSI blocks Default Value: X
3 : 0	VS_TOP	RAM configuration for TOP DSI vertical segmentation, not implemented in BOTTOM DSI blocks Default Value: X

15.1.203 UDB_DSI3_VS2

DSI VS Tile Configuration; Vertical Segmentation

Address: 0x400F43E4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	VS_BOT [7:4]				VS_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	VS_BOT	RAM configuration for BOTTOM DSI vertical segmentation, not implemented in TOP DSI blocks Default Value: X
3 : 0	VS_TOP	RAM configuration for TOP DSI vertical segmentation, not implemented in BOTTOM DSI blocks Default Value: X

15.1.204 UDB_DSI3_VS3

DSI VS Tile Configuration; Vertical Segmentation

Address: 0x400F43E6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	VS_BOT [7:4]				VS_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	VS_BOT	RAM configuration for BOTTOM DSI vertical segmentation, not implemented in TOP DSI blocks Default Value: X
3 : 0	VS_TOP	RAM configuration for TOP DSI vertical segmentation, not implemented in BOTTOM DSI blocks Default Value: X

15.1.205 UDB_DSI3_VS4

DSI VS Tile Configuration; Vertical Segmentation

Address: 0x400F43E8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	VS_BOT [7:4]				VS_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	VS_BOT	RAM configuration for BOTTOM DSI vertical segmentation, not implemented in TOP DSI blocks Default Value: X
3 : 0	VS_TOP	RAM configuration for TOP DSI vertical segmentation, not implemented in BOTTOM DSI blocks Default Value: X

15.1.206 UDB_DSI3_VS5

DSI VS Tile Configuration; Vertical Segmentation

Address: 0x400F43EA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	VS_BOT [7:4]				VS_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	VS_BOT	RAM configuration for BOTTOM DSI vertical segmentation, not implemented in TOP DSI blocks Default Value: X
3 : 0	VS_TOP	RAM configuration for TOP DSI vertical segmentation, not implemented in BOTTOM DSI blocks Default Value: X

15.1.207 UDB_DSI3_VS6

DSI VS Tile Configuration; Vertical Segmentation

Address: 0x400F43EC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	VS_BOT [7:4]				VS_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	VS_BOT	RAM configuration for BOTTOM DSI vertical segmentation, not implemented in TOP DSI blocks Default Value: X
3 : 0	VS_TOP	RAM configuration for TOP DSI vertical segmentation, not implemented in BOTTOM DSI blocks Default Value: X

15.1.208 UDB_DSI3_VS7

DSI VS Tile Configuration; Vertical Segmentation

Address: 0x400F43EE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	VS_BOT [7:4]				VS_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	VS_BOT	RAM configuration for BOTTOM DSI vertical segmentation, not implemented in TOP DSI blocks Default Value: X
3 : 0	VS_TOP	RAM configuration for TOP DSI vertical segmentation, not implemented in BOTTOM DSI blocks Default Value: X

16 GPIO Registers

This section discusses the GPIO registers. It lists all the registers in mapping tables, in address order.

16.1 Register Details

Register Name	Address
GPIO_INTR_CAUSE	0x40041000

16.1.1 GPIO_INTR_CAUSE

Interrupt port cause register

Address: 0x40041000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	R						
HW Access	None	W						
Name	None	PORT_INT [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
6 : 0	PORT_INT	Each IO port has an associated bit field in this register. The bit field reflects the IO port's interrupt line (bit field i reflects "gpio_interrupts[i]" for IO port i). The register is used when the system uses a shared/combined interrupt line "gpio_interrupt". The SW ISR reads the register to determine which IO port(s) is responsible for the shared/combined interrupt line "gpio_interrupt". Once, the IO port(s) is determined, the IO port's INTR register is read to determine the IO pad(s) in the IO port that caused the interrupt. Default Value: 0

17 GPIO Port Registers

This section discusses the GPIO Port registers. It lists all the registers in mapping tables, in address order.

17.1 Register Details

Register Name	Address
GPIO_PRT0_DR	0x40040000
GPIO_PRT0_PS	0x40040004
GPIO_PRT0_PC	0x40040008
GPIO_PRT0_INTR_CFG	0x4004000C
GPIO_PRT0_INTR	0x40040010
GPIO_PRT0_PC2	0x40040018
GPIO_PRT0_DR_SET	0x40040040
GPIO_PRT0_DR_CLR	0x40040044
GPIO_PRT0_DR_INV	0x40040048
GPIO_PRT1_DR	0x40040100
GPIO_PRT1_PS	0x40040104
GPIO_PRT1_PC	0x40040108
GPIO_PRT1_INTR_CFG	0x4004010C
GPIO_PRT1_INTR	0x40040110
GPIO_PRT1_PC2	0x40040118
GPIO_PRT1_DR_SET	0x40040140
GPIO_PRT1_DR_CLR	0x40040144
GPIO_PRT1_DR_INV	0x40040148
GPIO_PRT2_DR	0x40040200
GPIO_PRT2_PS	0x40040204
GPIO_PRT2_PC	0x40040208
GPIO_PRT2_INTR_CFG	0x4004020C
GPIO_PRT2_INTR	0x40040210
GPIO_PRT2_PC2	0x40040218
GPIO_PRT2_DR_SET	0x40040240
GPIO_PRT2_DR_CLR	0x40040244
GPIO_PRT2_DR_INV	0x40040248

Register Name	Address
GPIO_PRT3_DR	0x40040300
GPIO_PRT3_PS	0x40040304
GPIO_PRT3_PC	0x40040308
GPIO_PRT3_INTR_CFG	0x4004030C
GPIO_PRT3_INTR	0x40040310
GPIO_PRT3_PC2	0x40040318
GPIO_PRT3_DR_SET	0x40040340
GPIO_PRT3_DR_CLR	0x40040344
GPIO_PRT3_DR_INV	0x40040348
GPIO_PRT4_DR	0x40040400
GPIO_PRT4_PS	0x40040404
GPIO_PRT4_PC	0x40040408
GPIO_PRT4_INTR_CFG	0x4004040C
GPIO_PRT4_INTR	0x40040410
GPIO_PRT4_PC2	0x40040418
GPIO_PRT4_DR_SET	0x40040440
GPIO_PRT4_DR_CLR	0x40040444
GPIO_PRT4_DR_INV	0x40040448
GPIO_PRT5_DR	0x40040500
GPIO_PRT5_PS	0x40040504
GPIO_PRT5_PC	0x40040508
GPIO_PRT5_INTR_CFG	0x4004050C
GPIO_PRT5_INTR	0x40040510
GPIO_PRT5_PC2	0x40040518
GPIO_PRT5_DR_SET	0x40040540
GPIO_PRT5_DR_CLR	0x40040544
GPIO_PRT5_DR_INV	0x40040548
GPIO_PRT6_DR	0x40040600
GPIO_PRT6_PS	0x40040604
GPIO_PRT6_PC	0x40040608
GPIO_PRT6_INTR_CFG	0x4004060C
GPIO_PRT6_INTR	0x40040610
GPIO_PRT6_PC2	0x40040618
GPIO_PRT6_DR_SET	0x40040640
GPIO_PRT6_DR_CLR	0x40040644
GPIO_PRT6_DR_INV	0x40040648

17.1.1 GPIO_PRT0_DR

Port output data register

Address: 0x40040000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	DATA7	IO pad 7 output data. Default Value: 0
6	DATA6	IO pad 6 output data. Default Value: 0
5	DATA5	IO pad 5 output data. Default Value: 0
4	DATA4	IO pad 4 output data. Default Value: 0
3	DATA3	IO pad 3 output data. Default Value: 0
2	DATA2	IO pad 2 output data. Default Value: 0
1	DATA1	IO pad 1 output data. Default Value: 0
0	DATA0	IO pad 0 output data. Default Value: 0

17.1.2 GPIO_PRT0_PS

Port IO pad state register

Address: 0x40040004

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							FLT_DATA

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_DATA	Reads of this register return the logical state of the filtered pin. Default Value: 0
7	DATA7	IO pad 7 state. Default Value: 0
6	DATA6	IO pad 6 state. Default Value: 0
5	DATA5	IO pad 5 state. Default Value: 0
4	DATA4	IO pad 4 state. Default Value: 0
3	DATA3	IO pad 3 state. Default Value: 0
2	DATA2	IO pad 2 state. Default Value: 0
1	DATA1	IO pad 1 state. Default Value: 0

(continued)

0	DATA0	IO pad 0 state: 1: Logic high, if the pin voltage is above the input buffer threshold, logic high. 0: Logic low, if the pin voltage is below that threshold, logic low. If the drive mode for the pin is set to high Z Analog, the pin state will read 0 independent of the voltage on the pin. Default Value: 0

17.1.3 GPIO_PRT0_PC

Port configuration register

Address: 0x40040008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW			RW		
HW Access	R		R			R		
Name	DM2 [7:6]		DM1 [5:3]			DM0 [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW			RW			RW
HW Access	R	R			R			R
Name	DM5	DM4 [14:12]			DM3 [11:9]			DM2

Bits	23	22	21	20	19	18	17	16
SW Access	RW			RW			RW	
HW Access	R			R			R	
Name	DM7 [23:21]			DM6 [20:18]			DM5 [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None				RW	RW
HW Access	R		None				R	R
Name	PORT_IB_MODE_SEL [31:30]		None [29:26]				PORT_SLOW	PORT_VTRIP_SEL

Bits	Name	Description
31 : 30	PORT_IB_MODE_SEL	This field selects the input buffer reference. The size (1 or 2 bits) and functionality is dependent on the IO cell. For GPIOv2 IO cells, bit PORT_IB_MODE_SEL[1] is not used (GPIOv2 IO cell replaces GPIO IO cell): "0"/"2": CMOS input buffer (PORT_VTRIP_SEL is '0'), LVTTL input buffer (PORT_VTRIP_SEL is '1') "1"/"3": vcchib. For GPIO_OVTv2 and SIOv2 IO cells: "0": CMOS input buffer (PORT_VTRIP_SEL is '0'), LVTTL input buffer (PORT_VTRIP_SEL is '1') "1": vcchib. "2": OVT. "3": Reference (possibly from reference generator cell). For SIO IO cell, this field is present but not used as the SIO IO cell does not provide input buffer mode select functionality (SIOv2 IO cell will replace SIO IO cell, as soon as it is available). Default Value: 0
25	PORT_SLOW	This field controls the output edge rate of all pins on the port: '0': fast. '1': slow. Default Value: 0

(continued)

		0x0: PORT_SLEW_CTL_0: HS mode (100pf < Cb < 400pF, 1.71<5.5, Vext>3.0) FS mode (10pf<400pf,1.71<5.5) (20-160ns) **0x1: PORT_SLEW_CTL_1:** HS mode (Cb<100pf,1.71<5.5,Vext>2.8,F=1.7MHz) (10-80ns) FS+ Mode (Vext>2.8,1.71<5.5) (20-120ns) **0x2: PORT_SLEW_CTL_2:** HS mode (100pf<400pf, 1.71<5.5,Vext<3.3) (20-160ns) **0x3: PORT_SLEW_CTL_3:** HS mode (Cb<100pf,1.71<5.5,Vext<=2.8,F=1.7MHz) (10-80ns) FS+ mode (Vext<=2.8,1.71<5.5) (20-120ns)
24	PORT_VTRIP_SEL	The GPIO cells include a VTRIP_SEL signal to alter the input buffer voltage. Note: this bit is ignored for SIO ports, the VTRIP_SEL settings in the SIO register are used instead (a separate VTRIP_SEL is provided for each pin pair). 0: input buffer functions as a CMOS input buffer. 1: input buffer functions as a LVTTL input buffer. Default Value: 0
23 : 21	DM7	The GPIO drive mode for IO pad 7. Default Value: 0
20 : 18	DM6	The GPIO drive mode for IO pad 6. Default Value: 0
17 : 15	DM5	The GPIO drive mode for IO pad 5. Default Value: 0
14 : 12	DM4	The GPIO drive mode for IO pad 4. Default Value: 0
11 : 9	DM3	The GPIO drive mode for IO pad 3. Default Value: 0
8 : 6	DM2	The GPIO drive mode for IO pad 2. Default Value: 0
5 : 3	DM1	The GPIO drive mode for IO pad 1. Default Value: 0
2 : 0	DM0	The GPIO drive mode for IO pad 0. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the HSIOM is properly configured (HSIOM_PRT_SELx) before turning the IO on here to avoid producing glitches on the bus. Default Value: 0 **0x0: OFF:** Mode 0 (analog mode): Output buffer off (high Z). Input buffer off. **0x1: INPUT:** Mode 1: Output buffer off (high Z). Input buffer on. **0x2: 0_PU:** Mode 2: Strong pull down ('0'), weak/resistive pull up (PU). Input buffer on. **0x3: PD_1:** Mode 3: Weak/resistive pull down (PD), strong pull up ('1'). Input buffer on. **0x4: 0_Z:** Mode 4: Strong pull down ('0'), open drain (pull up off). Input buffer on.

(continued)

0x5: Z_1:
Mode 5: Open drain (pull down off), strong pull up ('1'). Input buffer on.

0x6: 0_1:
Mode 6: Strong pull down ('0'), strong pull up ('1'). Input buffer on.

0x7: PD_PU:
Mode 7: Weak/resistive pull down (PD), weak/resistive pull up (PU). Input buffer on.

17.1.4 GPIO_PRT0_INTR_CFG

Port interrupt configuration register

Address: 0x4004000C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	EDGE3_SEL [7:6]		EDGE2_SEL [5:4]		EDGE1_SEL [3:2]		EDGE0_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	EDGE7_SEL [15:14]		EDGE6_SEL [13:12]		EDGE5_SEL [11:10]		EDGE4_SEL [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW			RW	
HW Access	None			R			R	
Name	None [23:21]			FLT_SEL [20:18]			FLT_EDGE_SEL [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
20 : 18	FLT_SEL	Selects which pin is routed through the 50ns glitch filter to provide a glitch-safe interrupt. Default Value: 0
17 : 16	FLT_EDGE_SEL	Same for the glitch filtered pin (selected by FLT_SELECT). Default Value: 0 **0x0: DISABLE:** Disabled **0x1: RISING:** Rising edge **0x2: FALLING:** Falling edge **0x3: BOTH:** Both rising and falling edges
15 : 14	EDGE7_SEL	Sets which edge will trigger an IRQ for IO pad 7. Default Value: 0
13 : 12	EDGE6_SEL	Sets which edge will trigger an IRQ for IO pad 6. Default Value: 0

(continued)

11 : 10	EDGE5_SEL	Sets which edge will trigger an IRQ for IO pad 5. Default Value: 0
9 : 8	EDGE4_SEL	Sets which edge will trigger an IRQ for IO pad 4. Default Value: 0
7 : 6	EDGE3_SEL	Sets which edge will trigger an IRQ for IO pad 3. Default Value: 0
5 : 4	EDGE2_SEL	Sets which edge will trigger an IRQ for IO pad 2. Default Value: 0
3 : 2	EDGE1_SEL	Sets which edge will trigger an IRQ for IO pad 1. Default Value: 0
1 : 0	EDGE0_SEL	Sets which edge will trigger an IRQ for IO pad 0. Default Value: 0 **0x0: DISABLE:** Disabled **0x1: RISING:** Rising edge **0x2: FALLING:** Falling edge **0x3: BOTH:** Both rising and falling edges

17.1.5 GPIO_PRT0_INTR

Port interrupt status register

Address: 0x40040010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	A	A	A	A	A	A	A	A
Name	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1C
HW Access	None							A
Name	None [15:9]							FLT_DATA

Bits	23	22	21	20	19	18	17	16
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	PS_DATA7	PS_DATA6	PS_DATA5	PS_DATA4	PS_DATA3	PS_DATA2	PS_DATA1	PS_DATA0

Bits	31	30	29	28	27	26	25	24
SW Access	None							R
HW Access	None							W
Name	None [31:25]							PS_FLT_DATA

Bits	Name	Description
24	PS_FLT_DATA	This is a duplicate of the contents of the PS register, provided here to allow reading of both pin state and interrupt state of the port in a single read operation. Default Value: 0
23	PS_DATA7	Default Value: 0
22	PS_DATA6	Default Value: 0
21	PS_DATA5	Default Value: 0
20	PS_DATA4	Default Value: 0
19	PS_DATA3	Default Value: 0
18	PS_DATA2	Default Value: 0
17	PS_DATA1	Default Value: 0
16	PS_DATA0	` Default Value: 0
8	FLT_DATA	Deglitched interrupt pending (selected by FLT_SELECT). Default Value: 0

(continued)

7	DATA7	Interrupt pending on IO pad 7. Firmware writes 1 to clear the interrupt. Default Value: 0
6	DATA6	Interrupt pending on IO pad 6. Firmware writes 1 to clear the interrupt. Default Value: 0
5	DATA5	Interrupt pending on IO pad 5. Firmware writes 1 to clear the interrupt. Default Value: 0
4	DATA4	Interrupt pending on IO pad 4. Firmware writes 1 to clear the interrupt. Default Value: 0
3	DATA3	Interrupt pending on IO pad 3. Firmware writes 1 to clear the interrupt. Default Value: 0
2	DATA2	Interrupt pending on IO pad 2. Firmware writes 1 to clear the interrupt. Default Value: 0
1	DATA1	Interrupt pending on IO pad 1. Firmware writes 1 to clear the interrupt. Default Value: 0
0	DATA0	Interrupt pending on IO pad 0. Firmware writes 1 to clear the interrupt. Default Value: 0

17.1.6 GPIO_PRT0_PC2

Port configuration register 2

Address: 0x40040018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	INP_DIS7	INP_DIS6	INP_DIS5	INP_DIS4	INP_DIS3	INP_DIS2	INP_DIS1	INP_DIS0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	INP_DIS7	Disables the input buffer for IO pad 7. Default Value: 0
6	INP_DIS6	Disables the input buffer for IO pad 6. Default Value: 0
5	INP_DIS5	Disables the input buffer for IO pad 5. Default Value: 0
4	INP_DIS4	Disables the input buffer for IO pad 4. Default Value: 0
3	INP_DIS3	Disables the input buffer for IO pad 3. Default Value: 0
2	INP_DIS2	Disables the input buffer for IO pad 2. Default Value: 0
1	INP_DIS1	Disables the input buffer for IO pad 1. Default Value: 0

(continued)

0	INP_DIS0	Disables the input buffer for IO pad 0 independent of the port control drive mode (PC.DM). This bit should be set when analog signals are present on the pin and PC.DM != 0 is required to use the output driver. Default Value: 0

17.1.7 GPIO_PRT0_DR_SET

Port output data set register

Address: 0x40040040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	IO pad i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] set to '1'. Default Value: 0

17.1.8 GPIO_PRT0_DR_CLR

Port output data clear register

Address: 0x40040044

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	IO pad i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] set to '0'. Default Value: 0

17.1.9 GPIO_PRT0_DR_INV

Port output data invert register

Address: 0x40040048

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	IO pad i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] inverted ('0' => '1', '1' => '0'). Default Value: 0

17.1.10 GPIO_PRT1_DR

Port output data register

Address: 0x40040100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	DATA7	IO pad 7 output data. Default Value: 0
6	DATA6	IO pad 6 output data. Default Value: 0
5	DATA5	IO pad 5 output data. Default Value: 0
4	DATA4	IO pad 4 output data. Default Value: 0
3	DATA3	IO pad 3 output data. Default Value: 0
2	DATA2	IO pad 2 output data. Default Value: 0
1	DATA1	IO pad 1 output data. Default Value: 0
0	DATA0	IO pad 0 output data. Default Value: 0

17.1.11 GPIO_PRT1_PS

Port IO pad state register

Address: 0x40040104

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							FLT_DATA

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_DATA	Reads of this register return the logical state of the filtered pin. Default Value: 0
7	DATA7	IO pad 7 state. Default Value: 0
6	DATA6	IO pad 6 state. Default Value: 0
5	DATA5	IO pad 5 state. Default Value: 0
4	DATA4	IO pad 4 state. Default Value: 0
3	DATA3	IO pad 3 state. Default Value: 0
2	DATA2	IO pad 2 state. Default Value: 0
1	DATA1	IO pad 1 state. Default Value: 0

(continued)

0	DATA0	IO pad 0 state: 1: Logic high, if the pin voltage is above the input buffer threshold, logic high. 0: Logic low, if the pin voltage is below that threshold, logic low. If the drive mode for the pin is set to high Z Analog, the pin state will read 0 independent of the voltage on the pin. Default Value: 0

17.1.12 GPIO_PRT1_PC

Port configuration register

Address: 0x40040108

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW			RW		
HW Access	R		R			R		
Name	DM2 [7:6]		DM1 [5:3]			DM0 [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW			RW			RW
HW Access	R	R			R			R
Name	DM5	DM4 [14:12]			DM3 [11:9]			DM2

Bits	23	22	21	20	19	18	17	16
SW Access	RW			RW			RW	
HW Access	R			R			R	
Name	DM7 [23:21]			DM6 [20:18]			DM5 [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None				RW	RW
HW Access	R		None				R	R
Name	PORT_IB_MODE_SEL [31:30]		None [29:26]				PORT_SLOW	PORT_VTRIP_SEL

Bits	Name	Description
31 : 30	PORT_IB_MODE_SEL	This field selects the input buffer reference. The size (1 or 2 bits) and functionality is dependent on the IO cell. For GPIOv2 IO cells, bit PORT_IB_MODE_SEL[1] is not used (GPIOv2 IO cell replaces GPIO IO cell): "0"/"2": CMOS input buffer (PORT_VTRIP_SEL is '0'), LVTTL input buffer (PORT_VTRIP_SEL is '1') "1"/"3": vcchib. For GPIO_OVTv2 and SIOv2 IO cells: "0": CMOS input buffer (PORT_VTRIP_SEL is '0'), LVTTL input buffer (PORT_VTRIP_SEL is '1') "1": vcchib. "2": OVT. "3": Reference (possibly from reference generator cell). For SIO IO cell, this field is present but not used as the SIO IO cell does not provide input buffer mode select functionality (SIOv2 IO cell will replace SIO IO cell, as soon as it is available). Default Value: 0
25	PORT_SLOW	This field controls the output edge rate of all pins on the port: '0': fast. '1': slow. Default Value: 0

(continued)

		0x0: PORT_SLEW_CTL_0: HS mode (100pf < Cb < 400pF, 1.71<5.5, Vext>3.0) FS mode (10pf<400pf,1.71<5.5) (20-160ns) **0x1: PORT_SLEW_CTL_1:** HS mode (Cb<100pf,1.71<5.5,Vext>2.8,F=1.7MHz) (10-80ns) FS+ Mode (Vext>2.8,1.71<5.5) (20-120ns) **0x2: PORT_SLEW_CTL_2:** HS mode (100pf<400pf, 1.71<5.5,Vext<3.3) (20-160ns) **0x3: PORT_SLEW_CTL_3:** HS mode (Cb<100pf,1.71<5.5,Vext<=2.8,F=1.7MHz) (10-80ns) FS+ mode (Vext<=2.8,1.71<5.5) (20-120ns)
24	PORT_VTRIP_SEL	The GPIO cells include a VTRIP_SEL signal to alter the input buffer voltage. Note: this bit is ignored for SIO ports, the VTRIP_SEL settings in the SIO register are used instead (a separate VTRIP_SEL is provided for each pin pair). 0: input buffer functions as a CMOS input buffer. 1: input buffer functions as a LVTTL input buffer. Default Value: 0
23 : 21	DM7	The GPIO drive mode for IO pad 7. Default Value: 0
20 : 18	DM6	The GPIO drive mode for IO pad 6. Default Value: 0
17 : 15	DM5	The GPIO drive mode for IO pad 5. Default Value: 0
14 : 12	DM4	The GPIO drive mode for IO pad 4. Default Value: 0
11 : 9	DM3	The GPIO drive mode for IO pad 3. Default Value: 0
8 : 6	DM2	The GPIO drive mode for IO pad 2. Default Value: 0
5 : 3	DM1	The GPIO drive mode for IO pad 1. Default Value: 0
2 : 0	DM0	The GPIO drive mode for IO pad 0. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the HSIOM is properly configured (HSIOM_PRT_SELx) before turning the IO on here to avoid producing glitches on the bus. Default Value: 0 **0x0: OFF:** Mode 0 (analog mode): Output buffer off (high Z). Input buffer off. **0x1: INPUT:** Mode 1: Output buffer off (high Z). Input buffer on. **0x2: 0_PU:** Mode 2: Strong pull down ('0'), weak/resistive pull up (PU). Input buffer on. **0x3: PD_1:** Mode 3: Weak/resistive pull down (PD), strong pull up ('1'). Input buffer on. **0x4: 0_Z:** Mode 4: Strong pull down ('0'), open drain (pull up off). Input buffer on.

(continued)

0x5: Z_1:
Mode 5: Open drain (pull down off), strong pull up ('1'). Input buffer on.

0x6: 0_1:
Mode 6: Strong pull down ('0'), strong pull up ('1'). Input buffer on.

0x7: PD_PU:
Mode 7: Weak/resistive pull down (PD), weak/resistive pull up (PU). Input buffer on.

17.1.13 GPIO_PRT1_INTR_CFG

Port interrupt configuration register

Address: 0x4004010C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	EDGE3_SEL [7:6]		EDGE2_SEL [5:4]		EDGE1_SEL [3:2]		EDGE0_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	EDGE7_SEL [15:14]		EDGE6_SEL [13:12]		EDGE5_SEL [11:10]		EDGE4_SEL [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW			RW	
HW Access	None			R			R	
Name	None [23:21]			FLT_SEL [20:18]			FLT_EDGE_SEL [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
20 : 18	FLT_SEL	Selects which pin is routed through the 50ns glitch filter to provide a glitch-safe interrupt. Default Value: 0
17 : 16	FLT_EDGE_SEL	Same for the glitch filtered pin (selected by FLT_SELECT). Default Value: 0 **0x0: DISABLE:** Disabled **0x1: RISING:** Rising edge **0x2: FALLING:** Falling edge **0x3: BOTH:** Both rising and falling edges
15 : 14	EDGE7_SEL	Sets which edge will trigger an IRQ for IO pad 7. Default Value: 0
13 : 12	EDGE6_SEL	Sets which edge will trigger an IRQ for IO pad 6. Default Value: 0

(continued)

11 : 10	EDGE5_SEL	Sets which edge will trigger an IRQ for IO pad 5. Default Value: 0
9 : 8	EDGE4_SEL	Sets which edge will trigger an IRQ for IO pad 4. Default Value: 0
7 : 6	EDGE3_SEL	Sets which edge will trigger an IRQ for IO pad 3. Default Value: 0
5 : 4	EDGE2_SEL	Sets which edge will trigger an IRQ for IO pad 2. Default Value: 0
3 : 2	EDGE1_SEL	Sets which edge will trigger an IRQ for IO pad 1. Default Value: 0
1 : 0	EDGE0_SEL	Sets which edge will trigger an IRQ for IO pad 0. Default Value: 0 **0x0: DISABLE:** Disabled **0x1: RISING:** Rising edge **0x2: FALLING:** Falling edge **0x3: BOTH:** Both rising and falling edges

17.1.14 GPIO_PRT1_INTR

Port interrupt status register

Address: 0x40040110

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	A	A	A	A	A	A	A	A
Name	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1C
HW Access	None							A
Name	None [15:9]							FLT_DATA

Bits	23	22	21	20	19	18	17	16
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	PS_DATA7	PS_DATA6	PS_DATA5	PS_DATA4	PS_DATA3	PS_DATA2	PS_DATA1	PS_DATA0

Bits	31	30	29	28	27	26	25	24
SW Access	None							R
HW Access	None							W
Name	None [31:25]							PS_FLT_DATA

Bits	Name	Description
24	PS_FLT_DATA	This is a duplicate of the contents of the PS register, provided here to allow reading of both pin state and interrupt state of the port in a single read operation. Default Value: 0
23	PS_DATA7	Default Value: 0
22	PS_DATA6	Default Value: 0
21	PS_DATA5	Default Value: 0
20	PS_DATA4	Default Value: 0
19	PS_DATA3	Default Value: 0
18	PS_DATA2	Default Value: 0
17	PS_DATA1	Default Value: 0
16	PS_DATA0	` Default Value: 0
8	FLT_DATA	Deglitched interrupt pending (selected by FLT_SELECT). Default Value: 0

(continued)

7	DATA7	Interrupt pending on IO pad 7. Firmware writes 1 to clear the interrupt. Default Value: 0
6	DATA6	Interrupt pending on IO pad 6. Firmware writes 1 to clear the interrupt. Default Value: 0
5	DATA5	Interrupt pending on IO pad 5. Firmware writes 1 to clear the interrupt. Default Value: 0
4	DATA4	Interrupt pending on IO pad 4. Firmware writes 1 to clear the interrupt. Default Value: 0
3	DATA3	Interrupt pending on IO pad 3. Firmware writes 1 to clear the interrupt. Default Value: 0
2	DATA2	Interrupt pending on IO pad 2. Firmware writes 1 to clear the interrupt. Default Value: 0
1	DATA1	Interrupt pending on IO pad 1. Firmware writes 1 to clear the interrupt. Default Value: 0
0	DATA0	Interrupt pending on IO pad 0. Firmware writes 1 to clear the interrupt. Default Value: 0

17.1.15 GPIO_PRT1_PC2

Port configuration register 2

Address: 0x40040118

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	INP_DIS7	INP_DIS6	INP_DIS5	INP_DIS4	INP_DIS3	INP_DIS2	INP_DIS1	INP_DIS0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	INP_DIS7	Disables the input buffer for IO pad 7. Default Value: 0
6	INP_DIS6	Disables the input buffer for IO pad 6. Default Value: 0
5	INP_DIS5	Disables the input buffer for IO pad 5. Default Value: 0
4	INP_DIS4	Disables the input buffer for IO pad 4. Default Value: 0
3	INP_DIS3	Disables the input buffer for IO pad 3. Default Value: 0
2	INP_DIS2	Disables the input buffer for IO pad 2. Default Value: 0
1	INP_DIS1	Disables the input buffer for IO pad 1. Default Value: 0

(continued)

0	INP_DIS0	Disables the input buffer for IO pad 0 independent of the port control drive mode (PC.DM). This bit should be set when analog signals are present on the pin and PC.DM != 0 is required to use the output driver. Default Value: 0

17.1.16 GPIO_PRT1_DR_SET

Port output data set register

Address: 0x40040140

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	IO pad i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] set to '1'. Default Value: 0

17.1.17 GPIO_PRT1_DR_CLR

Port output data clear register

Address: 0x40040144

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	IO pad i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] set to '0'. Default Value: 0

17.1.18 GPIO_PRT1_DR_INV

Port output data invert register

Address: 0x40040148

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	IO pad i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] inverted ('0' => '1', '1' => '0'). Default Value: 0

17.1.19 GPIO_PRT2_DR

Port output data register

Address: 0x40040200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	DATA7	IO pad 7 output data. Default Value: 0
6	DATA6	IO pad 6 output data. Default Value: 0
5	DATA5	IO pad 5 output data. Default Value: 0
4	DATA4	IO pad 4 output data. Default Value: 0
3	DATA3	IO pad 3 output data. Default Value: 0
2	DATA2	IO pad 2 output data. Default Value: 0
1	DATA1	IO pad 1 output data. Default Value: 0
0	DATA0	IO pad 0 output data. Default Value: 0

17.1.20 GPIO_PRT2_PS

Port IO pad state register

Address: 0x40040204

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							FLT_DATA

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_DATA	Reads of this register return the logical state of the filtered pin. Default Value: 0
7	DATA7	IO pad 7 state. Default Value: 0
6	DATA6	IO pad 6 state. Default Value: 0
5	DATA5	IO pad 5 state. Default Value: 0
4	DATA4	IO pad 4 state. Default Value: 0
3	DATA3	IO pad 3 state. Default Value: 0
2	DATA2	IO pad 2 state. Default Value: 0
1	DATA1	IO pad 1 state. Default Value: 0

(continued)

0	DATA0	IO pad 0 state: 1: Logic high, if the pin voltage is above the input buffer threshold, logic high. 0: Logic low, if the pin voltage is below that threshold, logic low. If the drive mode for the pin is set to high Z Analog, the pin state will read 0 independent of the voltage on the pin. Default Value: 0

17.1.21 GPIO_PRT2_PC

Port configuration register

Address: 0x40040208

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW			RW		
HW Access	R		R			R		
Name	DM2 [7:6]		DM1 [5:3]			DM0 [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW			RW			RW
HW Access	R	R			R			R
Name	DM5	DM4 [14:12]			DM3 [11:9]			DM2

Bits	23	22	21	20	19	18	17	16
SW Access	RW			RW			RW	
HW Access	R			R			R	
Name	DM7 [23:21]			DM6 [20:18]			DM5 [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None				RW	RW
HW Access	R		None				R	R
Name	PORT_IB_MODE_SEL [31:30]		None [29:26]				PORT_SLOW	PORT_VTRIP_SEL

Bits	Name	Description
31 : 30	PORT_IB_MODE_SEL	This field selects the input buffer reference. The size (1 or 2 bits) and functionality is dependent on the IO cell. For GPIOv2 IO cells, bit PORT_IB_MODE_SEL[1] is not used (GPIOv2 IO cell replaces GPIO IO cell): "0"/"2": CMOS input buffer (PORT_VTRIP_SEL is '0'), LVTTL input buffer (PORT_VTRIP_SEL is '1') "1"/"3": vcchib. For GPIO_OVTv2 and SIOv2 IO cells: "0": CMOS input buffer (PORT_VTRIP_SEL is '0'), LVTTL input buffer (PORT_VTRIP_SEL is '1') "1": vcchib. "2": OVT. "3": Reference (possibly from reference generator cell). For SIO IO cell, this field is present but not used as the SIO IO cell does not provide input buffer mode select functionality (SIOv2 IO cell will replace SIO IO cell, as soon as it is available). Default Value: 0
25	PORT_SLOW	This field controls the output edge rate of all pins on the port: '0': fast. '1': slow. Default Value: 0

(continued)

		0x0: PORT_SLEW_CTL_0: HS mode (100pf < Cb < 400pF, 1.71<5.5, Vext>3.0) FS mode (10pf<400pf,1.71<5.5) (20-160ns) **0x1: PORT_SLEW_CTL_1:** HS mode (Cb<100pf,1.71<5.5,Vext>2.8,F=1.7MHz) (10-80ns) FS+ Mode (Vext>2.8,1.71<5.5) (20-120ns) **0x2: PORT_SLEW_CTL_2:** HS mode (100pf<400pf, 1.71<5.5,Vext<3.3) (20-160ns) **0x3: PORT_SLEW_CTL_3:** HS mode (Cb<100pf,1.71<5.5,Vext<=2.8,F=1.7MHz) (10-80ns) FS+ mode (Vext<=2.8,1.71<5.5) (20-120ns)
24	PORT_VTRIP_SEL	The GPIO cells include a VTRIP_SEL signal to alter the input buffer voltage. Note: this bit is ignored for SIO ports, the VTRIP_SEL settings in the SIO register are used instead (a separate VTRIP_SEL is provided for each pin pair). 0: input buffer functions as a CMOS input buffer. 1: input buffer functions as a LVTTL input buffer. Default Value: 0
23 : 21	DM7	The GPIO drive mode for IO pad 7. Default Value: 0
20 : 18	DM6	The GPIO drive mode for IO pad 6. Default Value: 0
17 : 15	DM5	The GPIO drive mode for IO pad 5. Default Value: 0
14 : 12	DM4	The GPIO drive mode for IO pad 4. Default Value: 0
11 : 9	DM3	The GPIO drive mode for IO pad 3. Default Value: 0
8 : 6	DM2	The GPIO drive mode for IO pad 2. Default Value: 0
5 : 3	DM1	The GPIO drive mode for IO pad 1. Default Value: 0
2 : 0	DM0	The GPIO drive mode for IO pad 0. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the HSIOM is properly configured (HSIOM_PRT_SELx) before turning the IO on here to avoid producing glitches on the bus. Default Value: 0 **0x0: OFF:** Mode 0 (analog mode): Output buffer off (high Z). Input buffer off. **0x1: INPUT:** Mode 1: Output buffer off (high Z). Input buffer on. **0x2: 0_PU:** Mode 2: Strong pull down ('0'), weak/resistive pull up (PU). Input buffer on. **0x3: PD_1:** Mode 3: Weak/resistive pull down (PD), strong pull up ('1'). Input buffer on. **0x4: 0_Z:** Mode 4: Strong pull down ('0'), open drain (pull up off). Input buffer on.

(continued)

0x5: Z_1:
Mode 5: Open drain (pull down off), strong pull up ('1'). Input buffer on.

0x6: 0_1:
Mode 6: Strong pull down ('0'), strong pull up ('1'). Input buffer on.

0x7: PD_PU:
Mode 7: Weak/resistive pull down (PD), weak/resistive pull up (PU). Input buffer on.

17.1.22 GPIO_PRT2_INTR_CFG

Port interrupt configuration register

Address: 0x4004020C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	EDGE3_SEL [7:6]		EDGE2_SEL [5:4]		EDGE1_SEL [3:2]		EDGE0_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	EDGE7_SEL [15:14]		EDGE6_SEL [13:12]		EDGE5_SEL [11:10]		EDGE4_SEL [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW			RW	
HW Access	None			R			R	
Name	None [23:21]			FLT_SEL [20:18]			FLT_EDGE_SEL [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
20 : 18	FLT_SEL	Selects which pin is routed through the 50ns glitch filter to provide a glitch-safe interrupt. Default Value: 0
17 : 16	FLT_EDGE_SEL	Same for the glitch filtered pin (selected by FLT_SELECT). Default Value: 0 **0x0: DISABLE:** Disabled **0x1: RISING:** Rising edge **0x2: FALLING:** Falling edge **0x3: BOTH:** Both rising and falling edges
15 : 14	EDGE7_SEL	Sets which edge will trigger an IRQ for IO pad 7. Default Value: 0
13 : 12	EDGE6_SEL	Sets which edge will trigger an IRQ for IO pad 6. Default Value: 0

(continued)

11 : 10	EDGE5_SEL	Sets which edge will trigger an IRQ for IO pad 5. Default Value: 0
9 : 8	EDGE4_SEL	Sets which edge will trigger an IRQ for IO pad 4. Default Value: 0
7 : 6	EDGE3_SEL	Sets which edge will trigger an IRQ for IO pad 3. Default Value: 0
5 : 4	EDGE2_SEL	Sets which edge will trigger an IRQ for IO pad 2. Default Value: 0
3 : 2	EDGE1_SEL	Sets which edge will trigger an IRQ for IO pad 1. Default Value: 0
1 : 0	EDGE0_SEL	Sets which edge will trigger an IRQ for IO pad 0. Default Value: 0 **0x0: DISABLE:** Disabled **0x1: RISING:** Rising edge **0x2: FALLING:** Falling edge **0x3: BOTH:** Both rising and falling edges

17.1.23 GPIO_PRT2_INTR

Port interrupt status register

Address: 0x40040210

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	A	A	A	A	A	A	A	A
Name	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1C
HW Access	None							A
Name	None [15:9]							FLT_DATA

Bits	23	22	21	20	19	18	17	16
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	PS_DATA7	PS_DATA6	PS_DATA5	PS_DATA4	PS_DATA3	PS_DATA2	PS_DATA1	PS_DATA0

Bits	31	30	29	28	27	26	25	24
SW Access	None							R
HW Access	None							W
Name	None [31:25]							PS_FLT_DATA

Bits	Name	Description
24	PS_FLT_DATA	This is a duplicate of the contents of the PS register, provided here to allow reading of both pin state and interrupt state of the port in a single read operation. Default Value: 0
23	PS_DATA7	Default Value: 0
22	PS_DATA6	Default Value: 0
21	PS_DATA5	Default Value: 0
20	PS_DATA4	Default Value: 0
19	PS_DATA3	Default Value: 0
18	PS_DATA2	Default Value: 0
17	PS_DATA1	Default Value: 0
16	PS_DATA0	` Default Value: 0
8	FLT_DATA	Deglitched interrupt pending (selected by FLT_SELECT). Default Value: 0

(continued)

7	DATA7	Interrupt pending on IO pad 7. Firmware writes 1 to clear the interrupt. Default Value: 0
6	DATA6	Interrupt pending on IO pad 6. Firmware writes 1 to clear the interrupt. Default Value: 0
5	DATA5	Interrupt pending on IO pad 5. Firmware writes 1 to clear the interrupt. Default Value: 0
4	DATA4	Interrupt pending on IO pad 4. Firmware writes 1 to clear the interrupt. Default Value: 0
3	DATA3	Interrupt pending on IO pad 3. Firmware writes 1 to clear the interrupt. Default Value: 0
2	DATA2	Interrupt pending on IO pad 2. Firmware writes 1 to clear the interrupt. Default Value: 0
1	DATA1	Interrupt pending on IO pad 1. Firmware writes 1 to clear the interrupt. Default Value: 0
0	DATA0	Interrupt pending on IO pad 0. Firmware writes 1 to clear the interrupt. Default Value: 0

17.1.24 GPIO_PRT2_PC2

Port configuration register 2

Address: 0x40040218

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	INP_DIS7	INP_DIS6	INP_DIS5	INP_DIS4	INP_DIS3	INP_DIS2	INP_DIS1	INP_DIS0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	INP_DIS7	Disables the input buffer for IO pad 7. Default Value: 0
6	INP_DIS6	Disables the input buffer for IO pad 6. Default Value: 0
5	INP_DIS5	Disables the input buffer for IO pad 5. Default Value: 0
4	INP_DIS4	Disables the input buffer for IO pad 4. Default Value: 0
3	INP_DIS3	Disables the input buffer for IO pad 3. Default Value: 0
2	INP_DIS2	Disables the input buffer for IO pad 2. Default Value: 0
1	INP_DIS1	Disables the input buffer for IO pad 1. Default Value: 0

(continued)

0	INP_DIS0	Disables the input buffer for IO pad 0 independent of the port control drive mode (PC.DM). This bit should be set when analog signals are present on the pin and PC.DM != 0 is required to use the output driver. Default Value: 0

17.1.25 GPIO_PRT2_DR_SET

Port output data set register

Address: 0x40040240

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	IO pad i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] set to '1'. Default Value: 0

17.1.26 GPIO_PRT2_DR_CLR

Port output data clear register

Address: 0x40040244

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	IO pad i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] set to '0'. Default Value: 0

17.1.27 GPIO_PRT2_DR_INV

Port output data invert register

Address: 0x40040248

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	IO pad i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] inverted ('0' => '1', '1' => '0'). Default Value: 0

17.1.28 GPIO_PRT3_DR

Port output data register

Address: 0x40040300

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	DATA7	IO pad 7 output data. Default Value: 0
6	DATA6	IO pad 6 output data. Default Value: 0
5	DATA5	IO pad 5 output data. Default Value: 0
4	DATA4	IO pad 4 output data. Default Value: 0
3	DATA3	IO pad 3 output data. Default Value: 0
2	DATA2	IO pad 2 output data. Default Value: 0
1	DATA1	IO pad 1 output data. Default Value: 0
0	DATA0	IO pad 0 output data. Default Value: 0

17.1.29 GPIO_PRT3_PS

Port IO pad state register

Address: 0x40040304

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							FLT_DATA

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_DATA	Reads of this register return the logical state of the filtered pin. Default Value: 0
7	DATA7	IO pad 7 state. Default Value: 0
6	DATA6	IO pad 6 state. Default Value: 0
5	DATA5	IO pad 5 state. Default Value: 0
4	DATA4	IO pad 4 state. Default Value: 0
3	DATA3	IO pad 3 state. Default Value: 0
2	DATA2	IO pad 2 state. Default Value: 0
1	DATA1	IO pad 1 state. Default Value: 0

(continued)

0	DATA0	IO pad 0 state: 1: Logic high, if the pin voltage is above the input buffer threshold, logic high. 0: Logic low, if the pin voltage is below that threshold, logic low. If the drive mode for the pin is set to high Z Analog, the pin state will read 0 independent of the voltage on the pin. Default Value: 0

17.1.30 GPIO_PRT3_PC

Port configuration register

Address: 0x40040308

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW			RW		
HW Access	R		R			R		
Name	DM2 [7:6]		DM1 [5:3]			DM0 [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW			RW			RW
HW Access	R	R			R			R
Name	DM5	DM4 [14:12]			DM3 [11:9]			DM2

Bits	23	22	21	20	19	18	17	16
SW Access	RW			RW			RW	
HW Access	R			R			R	
Name	DM7 [23:21]			DM6 [20:18]			DM5 [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None				RW	RW
HW Access	R		None				R	R
Name	PORT_IB_MODE_SEL [31:30]		None [29:26]				PORT_SLOW	PORT_VTRIP_SEL

Bits	Name	Description
31 : 30	PORT_IB_MODE_SEL	This field selects the input buffer reference. The size (1 or 2 bits) and functionality is dependent on the IO cell. For GPIOv2 IO cells, bit PORT_IB_MODE_SEL[1] is not used (GPIOv2 IO cell replaces GPIO IO cell): "0"/"2": CMOS input buffer (PORT_VTRIP_SEL is '0'), LVTTL input buffer (PORT_VTRIP_SEL is '1') "1"/"3": vcchib. For GPIO_OVTv2 and SIOv2 IO cells: "0": CMOS input buffer (PORT_VTRIP_SEL is '0'), LVTTL input buffer (PORT_VTRIP_SEL is '1') "1": vcchib. "2": OVT. "3": Reference (possibly from reference generator cell). For SIO IO cell, this field is present but not used as the SIO IO cell does not provide input buffer mode select functionality (SIOv2 IO cell will replace SIO IO cell, as soon as it is available). Default Value: 0
25	PORT_SLOW	This field controls the output edge rate of all pins on the port: '0': fast. '1': slow. Default Value: 0

(continued)

		0x0: PORT_SLEW_CTL_0: HS mode (100pf < Cb < 400pF, 1.71<5.5, Vext>3.0) FS mode (10pf<400pf,1.71<5.5) (20-160ns) **0x1: PORT_SLEW_CTL_1:** HS mode (Cb<100pf,1.71<5.5,Vext>2.8,F=1.7MHz) (10-80ns) FS+ Mode (Vext>2.8,1.71<5.5) (20-120ns) **0x2: PORT_SLEW_CTL_2:** HS mode (100pf<400pf, 1.71<5.5,Vext<3.3) (20-160ns) **0x3: PORT_SLEW_CTL_3:** HS mode (Cb<100pf,1.71<5.5,Vext<=2.8,F=1.7MHz) (10-80ns) FS+ mode (Vext<=2.8,1.71<5.5) (20-120ns)
24	PORT_VTRIP_SEL	The GPIO cells include a VTRIP_SEL signal to alter the input buffer voltage. Note: this bit is ignored for SIO ports, the VTRIP_SEL settings in the SIO register are used instead (a separate VTRIP_SEL is provided for each pin pair). 0: input buffer functions as a CMOS input buffer. 1: input buffer functions as a LVTTL input buffer. Default Value: 0
23 : 21	DM7	The GPIO drive mode for IO pad 7. Default Value: 0
20 : 18	DM6	The GPIO drive mode for IO pad 6. Default Value: 0
17 : 15	DM5	The GPIO drive mode for IO pad 5. Default Value: 0
14 : 12	DM4	The GPIO drive mode for IO pad 4. Default Value: 0
11 : 9	DM3	The GPIO drive mode for IO pad 3. Default Value: 0
8 : 6	DM2	The GPIO drive mode for IO pad 2. Default Value: 0
5 : 3	DM1	The GPIO drive mode for IO pad 1. Default Value: 0
2 : 0	DM0	The GPIO drive mode for IO pad 0. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the HSIOM is properly configured (HSIOM_PRT_SELx) before turning the IO on here to avoid producing glitches on the bus. Default Value: 0 **0x0: OFF:** Mode 0 (analog mode): Output buffer off (high Z). Input buffer off. **0x1: INPUT:** Mode 1: Output buffer off (high Z). Input buffer on. **0x2: 0_PU:** Mode 2: Strong pull down ('0'), weak/resistive pull up (PU). Input buffer on. **0x3: PD_1:** Mode 3: Weak/resistive pull down (PD), strong pull up ('1'). Input buffer on. **0x4: 0_Z:** Mode 4: Strong pull down ('0'), open drain (pull up off). Input buffer on.

(continued)

0x5: Z_1:
Mode 5: Open drain (pull down off), strong pull up ('1'). Input buffer on.

0x6: 0_1:
Mode 6: Strong pull down ('0'), strong pull up ('1'). Input buffer on.

0x7: PD_PU:
Mode 7: Weak/resistive pull down (PD), weak/resistive pull up (PU). Input buffer on.

17.1.31 GPIO_PRT3_INTR_CFG

Port interrupt configuration register

Address: 0x4004030C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	EDGE3_SEL [7:6]		EDGE2_SEL [5:4]		EDGE1_SEL [3:2]		EDGE0_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	EDGE7_SEL [15:14]		EDGE6_SEL [13:12]		EDGE5_SEL [11:10]		EDGE4_SEL [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW			RW	
HW Access	None			R			R	
Name	None [23:21]			FLT_SEL [20:18]			FLT_EDGE_SEL [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
20 : 18	FLT_SEL	Selects which pin is routed through the 50ns glitch filter to provide a glitch-safe interrupt. Default Value: 0
17 : 16	FLT_EDGE_SEL	Same for the glitch filtered pin (selected by FLT_SELECT). Default Value: 0 **0x0: DISABLE:** Disabled **0x1: RISING:** Rising edge **0x2: FALLING:** Falling edge **0x3: BOTH:** Both rising and falling edges
15 : 14	EDGE7_SEL	Sets which edge will trigger an IRQ for IO pad 7. Default Value: 0
13 : 12	EDGE6_SEL	Sets which edge will trigger an IRQ for IO pad 6. Default Value: 0

(continued)

11 : 10	EDGE5_SEL	Sets which edge will trigger an IRQ for IO pad 5. Default Value: 0
9 : 8	EDGE4_SEL	Sets which edge will trigger an IRQ for IO pad 4. Default Value: 0
7 : 6	EDGE3_SEL	Sets which edge will trigger an IRQ for IO pad 3. Default Value: 0
5 : 4	EDGE2_SEL	Sets which edge will trigger an IRQ for IO pad 2. Default Value: 0
3 : 2	EDGE1_SEL	Sets which edge will trigger an IRQ for IO pad 1. Default Value: 0
1 : 0	EDGE0_SEL	Sets which edge will trigger an IRQ for IO pad 0. Default Value: 0 **0x0: DISABLE:** Disabled **0x1: RISING:** Rising edge **0x2: FALLING:** Falling edge **0x3: BOTH:** Both rising and falling edges

17.1.32 GPIO_PRT3_INTR

Port interrupt status register

Address: 0x40040310

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	A	A	A	A	A	A	A	A
Name	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1C
HW Access	None							A
Name	None [15:9]							FLT_DATA

Bits	23	22	21	20	19	18	17	16
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	PS_DATA7	PS_DATA6	PS_DATA5	PS_DATA4	PS_DATA3	PS_DATA2	PS_DATA1	PS_DATA0

Bits	31	30	29	28	27	26	25	24
SW Access	None							R
HW Access	None							W
Name	None [31:25]							PS_FLT_DATA

Bits	Name	Description
24	PS_FLT_DATA	This is a duplicate of the contents of the PS register, provided here to allow reading of both pin state and interrupt state of the port in a single read operation. Default Value: 0
23	PS_DATA7	Default Value: 0
22	PS_DATA6	Default Value: 0
21	PS_DATA5	Default Value: 0
20	PS_DATA4	Default Value: 0
19	PS_DATA3	Default Value: 0
18	PS_DATA2	Default Value: 0
17	PS_DATA1	Default Value: 0
16	PS_DATA0	` Default Value: 0
8	FLT_DATA	Deglitched interrupt pending (selected by FLT_SELECT). Default Value: 0

(continued)

7	DATA7	Interrupt pending on IO pad 7. Firmware writes 1 to clear the interrupt. Default Value: 0
6	DATA6	Interrupt pending on IO pad 6. Firmware writes 1 to clear the interrupt. Default Value: 0
5	DATA5	Interrupt pending on IO pad 5. Firmware writes 1 to clear the interrupt. Default Value: 0
4	DATA4	Interrupt pending on IO pad 4. Firmware writes 1 to clear the interrupt. Default Value: 0
3	DATA3	Interrupt pending on IO pad 3. Firmware writes 1 to clear the interrupt. Default Value: 0
2	DATA2	Interrupt pending on IO pad 2. Firmware writes 1 to clear the interrupt. Default Value: 0
1	DATA1	Interrupt pending on IO pad 1. Firmware writes 1 to clear the interrupt. Default Value: 0
0	DATA0	Interrupt pending on IO pad 0. Firmware writes 1 to clear the interrupt. Default Value: 0

17.1.33 GPIO_PRT3_PC2

Port configuration register 2

Address: 0x40040318

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	INP_DIS7	INP_DIS6	INP_DIS5	INP_DIS4	INP_DIS3	INP_DIS2	INP_DIS1	INP_DIS0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	INP_DIS7	Disables the input buffer for IO pad 7. Default Value: 0
6	INP_DIS6	Disables the input buffer for IO pad 6. Default Value: 0
5	INP_DIS5	Disables the input buffer for IO pad 5. Default Value: 0
4	INP_DIS4	Disables the input buffer for IO pad 4. Default Value: 0
3	INP_DIS3	Disables the input buffer for IO pad 3. Default Value: 0
2	INP_DIS2	Disables the input buffer for IO pad 2. Default Value: 0
1	INP_DIS1	Disables the input buffer for IO pad 1. Default Value: 0

(continued)

0	INP_DIS0	Disables the input buffer for IO pad 0 independent of the port control drive mode (PC.DM). This bit should be set when analog signals are present on the pin and PC.DM != 0 is required to use the output driver. Default Value: 0

17.1.34 GPIO_PRT3_DR_SET

Port output data set register

Address: 0x40040340

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	IO pad i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] set to '1'. Default Value: 0

17.1.35 GPIO_PRT3_DR_CLR

Port output data clear register

Address: 0x40040344

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	IO pad i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] set to '0'. Default Value: 0

17.1.36 GPIO_PRT3_DR_INV

Port output data invert register

Address: 0x40040348

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	IO pad i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] inverted ('0' => '1', '1' => '0'). Default Value: 0

17.1.37 GPIO_PRT4_DR

Port output data register

Address: 0x40040400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						RW	RW
Name	None [7:2]						DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	DATA1	IO pad 1 output data. Default Value: 0
0	DATA0	IO pad 0 output data. Default Value: 0

17.1.38 GPIO_PRT4_PS

Port IO pad state register

Address: 0x40040404

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						W	W
Name	None [7:2]						DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							FLT_DATA

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_DATA	Reads of this register return the logical state of the filtered pin. Default Value: 0
1	DATA1	IO pad 1 state. Default Value: 0
0	DATA0	IO pad 0 state: 1: Logic high, if the pin voltage is above the input buffer threshold, logic high. 0: Logic low, if the pin voltage is below that threshold, logic low. If the drive mode for the pin is set to high Z Analog, the pin state will read 0 independent of the voltage on the pin. Default Value: 0

17.1.39 GPIO_PRT4_PC

Port configuration register

Address: 0x40040408

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW			RW		
HW Access	None		R			R		
Name	None [7:6]		DM1 [5:3]			DM0 [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None				RW	RW
HW Access	R		None				R	R
Name	PORT_IB_MODE_SEL [31:30]		None [29:26]				PORT_SLOW	PORT_VTRIP_SEL

Bits	Name	Description
31 : 30	PORT_IB_MODE_SEL	This field selects the input buffer reference. The size (1 or 2 bits) and functionality is dependent on the IO cell. For GPIOv2 IO cells, bit PORT_IB_MODE_SEL[1] is not used (GPIOv2 IO cell replaces GPIO IO cell): "0"/"2": CMOS input buffer (PORT_VTRIP_SEL is '0'), LVTTL input buffer (PORT_VTRIP_SEL is '1') "1"/"3": vcchib. For GPIO_OVTv2 and SIOv2 IO cells: "0": CMOS input buffer (PORT_VTRIP_SEL is '0'), LVTTL input buffer (PORT_VTRIP_SEL is '1') "1": vcchib. "2": OVT. "3": Reference (possibly from reference generator cell). For SIO IO cell, this field is present but not used as the SIO IO cell does not provide input buffer mode select functionality (SIOv2 IO cell will replace SIO IO cell, as soon as it is available). Default Value: 0
25	PORT_SLOW	This field controls the output edge rate of all pins on the port: '0': fast. '1': slow. Default Value: 0

(continued)

		0x0: PORT_SLEW_CTL_0: HS mode (100pf < Cb < 400pF, 1.71<5.5, Vext>3.0) FS mode (10pf<400pf,1.71<5.5) (20-160ns) **0x1: PORT_SLEW_CTL_1:** HS mode (Cb<100pf,1.71<5.5,Vext>2.8,F=1.7MHz) (10-80ns) FS+ Mode (Vext>2.8,1.71<5.5) (20-120ns) **0x2: PORT_SLEW_CTL_2:** HS mode (100pf<400pf, 1.71<5.5,Vext<3.3) (20-160ns) **0x3: PORT_SLEW_CTL_3:** HS mode (Cb<100pf,1.71<5.5,Vext<=2.8,F=1.7MHz) (10-80ns) FS+ mode (Vext<=2.8,1.71<5.5) (20-120ns)
24	PORT_VTRIP_SEL	The GPIO cells include a VTRIP_SEL signal to alter the input buffer voltage. Note: this bit is ignored for SIO ports, the VTRIP_SEL settings in the SIO register are used instead (a separate VTRIP_SEL is provided for each pin pair). 0: input buffer functions as a CMOS input buffer. 1: input buffer functions as a LVTTL input buffer. Default Value: 0
5 : 3	DM1	The GPIO drive mode for IO pad 1. Default Value: 0
2 : 0	DM0	The GPIO drive mode for IO pad 0. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the HSIOM is properly configured (HSIOM_PRT_SELx) before turning the IO on here to avoid producing glitches on the bus. Default Value: 0 **0x0: OFF:** Mode 0 (analog mode): Output buffer off (high Z). Input buffer off. **0x1: INPUT:** Mode 1: Output buffer off (high Z). Input buffer on. **0x2: 0_PU:** Mode 2: Strong pull down ('0'), weak/resistive pull up (PU). Input buffer on. **0x3: PD_1:** Mode 3: Weak/resistive pull down (PD), strong pull up ('1'). Input buffer on. **0x4: 0_Z:** Mode 4: Strong pull down ('0'), open drain (pull up off). Input buffer on. **0x5: Z_1:** Mode 5: Open drain (pull down off), strong pull up ('1'). Input buffer on. **0x6: 0_1:** Mode 6: Strong pull down ('0'), strong pull up ('1'). Input buffer on. **0x7: PD_PU:** Mode 7: Weak/resistive pull down (PD), weak/resistive pull up (PU). Input buffer on.

17.1.40 GPIO_PRT4_INTR_CFG

Port interrupt configuration register

Address: 0x4004040C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW		RW	
HW Access	None				R		R	
Name	None [7:4]				EDGE1_SEL [3:2]		EDGE0_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW			RW	
HW Access	None			R			R	
Name	None [23:21]			FLT_SEL [20:18]			FLT_EDGE_SEL [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
20 : 18	FLT_SEL	Selects which pin is routed through the 50ns glitch filter to provide a glitch-safe interrupt. Default Value: 0
17 : 16	FLT_EDGE_SEL	Same for the glitch filtered pin (selected by FLT_SELECT). Default Value: 0 **0x0: DISABLE:** Disabled **0x1: RISING:** Rising edge **0x2: FALLING:** Falling edge **0x3: BOTH:** Both rising and falling edges
3 : 2	EDGE1_SEL	Sets which edge will trigger an IRQ for IO pad 1. Default Value: 0
1 : 0	EDGE0_SEL	Sets which edge will trigger an IRQ for IO pad 0. Default Value: 0

(continued)

0x0: DISABLE:
Disabled

0x1: RISING:
Rising edge

0x2: FALLING:
Falling edge

0x3: BOTH:
Both rising and falling edges

17.1.41 GPIO_PRT4_INTR

Port interrupt status register

Address: 0x40040410

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1C	RW1C
HW Access	None						A	A
Name	None [7:2]						DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1C
HW Access	None							A
Name	None [15:9]							FLT_DATA

Bits	23	22	21	20	19	18	17	16
SW Access	None						R	R
HW Access	None						W	W
Name	None [23:18]						PS_DATA1	PS_DATA0

Bits	31	30	29	28	27	26	25	24
SW Access	None							R
HW Access	None							W
Name	None [31:25]							PS_FLT_DATA

Bits	Name	Description
24	PS_FLT_DATA	This is a duplicate of the contents of the PS register, provided here to allow reading of both pin state and interrupt state of the port in a single read operation. Default Value: 0
17	PS_DATA1	Default Value: 0
16	PS_DATA0	` Default Value: 0
8	FLT_DATA	Deglitched interrupt pending (selected by FLT_SELECT). Default Value: 0
1	DATA1	Interrupt pending on IO pad 1. Firmware writes 1 to clear the interrupt. Default Value: 0
0	DATA0	Interrupt pending on IO pad 0. Firmware writes 1 to clear the interrupt. Default Value: 0

17.1.42 GPIO_PRT4_PC2

Port configuration register 2

Address: 0x40040418

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						INP_DIS1	INP_DIS0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	INP_DIS1	Disables the input buffer for IO pad 1. Default Value: 0
0	INP_DIS0	Disables the input buffer for IO pad 0 independent of the port control drive mode (PC.DM). This bit should be set when analog signals are present on the pin and PC.DM != 0 is required to use the output driver. Default Value: 0

17.1.43 GPIO_PRT4_DR_SET

Port output data set register

Address: 0x40040440

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	IO pad i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] set to '1'. Default Value: 0

17.1.44 GPIO_PRT4_DR_CLR

Port output data clear register

Address: 0x40040444

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	IO pad i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] set to '0'. Default Value: 0

17.1.45 GPIO_PRT4_DR_INV

Port output data invert register

Address: 0x40040448

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	IO pad i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] inverted ('0' => '1', '1' => '0'). Default Value: 0

17.1.46 GPIO_PRT5_DR

Port output data register

Address: 0x40040500

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						RW	RW
Name	None [7:2]						DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	DATA1	IO pad 1 output data. Default Value: 0
0	DATA0	IO pad 0 output data. Default Value: 0

17.1.47 GPIO_PRT5_PS

Port IO pad state register

Address: 0x40040504

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						W	W
Name	None [7:2]						DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							FLT_DATA

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_DATA	Reads of this register return the logical state of the filtered pin. Default Value: 0
1	DATA1	IO pad 1 state. Default Value: 0
0	DATA0	IO pad 0 state: 1: Logic high, if the pin voltage is above the input buffer threshold, logic high. 0: Logic low, if the pin voltage is below that threshold, logic low. If the drive mode for the pin is set to high Z Analog, the pin state will read 0 independent of the voltage on the pin. Default Value: 0

17.1.48 GPIO_PRT5_PC

Port configuration register

Address: 0x40040508

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW			RW		
HW Access	None		R			R		
Name	None [7:6]		DM1 [5:3]			DM0 [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW		RW		RW	None	RW	RW
HW Access	R		R		R	None	R	R
Name	PORT_IB_MODE_SEL [31:30]		PORT_SLEW_CTL [29:28]		PORT_HYST_TRIM	None	PORT_SLOW	PORT_VTRIP_SEL

Bits	Name	Description
31 : 30	PORT_IB_MODE_SEL	This field selects the input buffer reference. The size (1 or 2 bits) and functionality is dependent on the IO cell. For GPIOv2 IO cells, bit PORT_IB_MODE_SEL[1] is not used (GPIOv2 IO cell replaces GPIO IO cell): "0"/"2": CMOS input buffer (PORT_VTRIP_SEL is '0'), LVTTL input buffer (PORT_VTRIP_SEL is '1') "1"/"3": vcchib. For GPIO_OVTv2 and SIOv2 IO cells: "0": CMOS input buffer (PORT_VTRIP_SEL is '0'), LVTTL input buffer (PORT_VTRIP_SEL is '1') "1": vcchib. "2": OVT. "3": Reference (possibly from reference generator cell). For SIO IO cell, this field is present but not used as the SIO IO cell does not provide input buffer mode select functionality (SIOv2 IO cell will replace SIO IO cell, as soon as it is available). Default Value: 0
29 : 28	PORT_SLEW_CTL	Slew control. Only used in the O_Z drive mode (mode 4: strong pull down, open drain): This field is intended for I2C functionality. Default Value: 0

(continued)

		0x0: PORT_SLEW_CTL_0: HS mode (100pf < Cb < 400pF, 1.71<5.5, Vext>3.0) FS mode (10pf<400pf,1.71<5.5) (20-160ns) **0x1: PORT_SLEW_CTL_1:** HS mode (Cb<100pf,1.71<5.5,Vext>2.8,F=1.7MHz) (10-80ns) FS+ Mode (Vext>2.8,1.71<5.5) (20-120ns) **0x2: PORT_SLEW_CTL_2:** HS mode (100pf<400pf, 1.71<5.5,Vext<3.3) (20-160ns) **0x3: PORT_SLEW_CTL_3:** HS mode (Cb<100pf,1.71<5.5,Vext<=2.8,F=1.7MHz) (10-80ns) FS+ mode (Vext<=2.8,1.71<5.5) (20-120ns)
27	PORT_HYST_TRIM	This field is used to improve the hysteresis (to 10% of vddio) of the selectable trip point input buffer. The voltage reference comes from the VREFGEN block and is only available when using the VREFGEN block: '0': <= 2.2 V input signaling Voltage. '1': > 2.2 V input signaling Voltage. Default Value: 0
25	PORT_SLOW	This field controls the output edge rate of all pins on the port: '0': fast. '1': slow. Default Value: 0
24	PORT_VTRIP_SEL	The GPIO cells include a VTRIP_SEL signal to alter the input buffer voltage. Note: this bit is ignored for SIO ports, the VTRIP_SEL settings in the SIO register are used instead (a separate VTRIP_SEL is provided for each pin pair). 0: input buffer functions as a CMOS input buffer. 1: input buffer functions as a LVTTL input buffer. Default Value: 0
5 : 3	DM1	The GPIO drive mode for IO pad 1. Default Value: 0
2 : 0	DM0	The GPIO drive mode for IO pad 0. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the HSIOM is properly configured (HSIOM_PRT_SELx) before turning the IO on here to avoid producing glitches on the bus. Default Value: 0 **0x0: OFF:** Mode 0 (analog mode): Output buffer off (high Z). Input buffer off. **0x1: INPUT:** Mode 1: Output buffer off (high Z). Input buffer on. **0x2: 0_PU:** Mode 2: Strong pull down ('0'), weak/resistive pull up (PU). Input buffer on. **0x3: PD_1:** Mode 3: Weak/resistive pull down (PD), strong pull up ('1'). Input buffer on. **0x4: 0_Z:** Mode 4: Strong pull down ('0'), open drain (pull up off). Input buffer on. **0x5: Z_1:** Mode 5: Open drain (pull down off), strong pull up ('1'). Input buffer on. **0x6: 0_1:** Mode 6: Strong pull down ('0'), strong pull up ('1'). Input buffer on.

(continued)

0x7: PD_PU:
Mode 7: Weak/resistive pull down (PD), weak/resistive pull up (PU). Input buffer on.

17.1.49 GPIO_PRT5_INTR_CFG

Port interrupt configuration register

Address: 0x4004050C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW		RW	
HW Access	None				R		R	
Name	None [7:4]				EDGE1_SEL [3:2]		EDGE0_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW			RW	
HW Access	None			R			R	
Name	None [23:21]			FLT_SEL [20:18]			FLT_EDGE_SEL [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
20 : 18	FLT_SEL	Selects which pin is routed through the 50ns glitch filter to provide a glitch-safe interrupt. Default Value: 0
17 : 16	FLT_EDGE_SEL	Same for the glitch filtered pin (selected by FLT_SELECT). Default Value: 0 **0x0: DISABLE:** Disabled **0x1: RISING:** Rising edge **0x2: FALLING:** Falling edge **0x3: BOTH:** Both rising and falling edges
3 : 2	EDGE1_SEL	Sets which edge will trigger an IRQ for IO pad 1. Default Value: 0
1 : 0	EDGE0_SEL	Sets which edge will trigger an IRQ for IO pad 0. Default Value: 0

(continued)

0x0: DISABLE:
Disabled

0x1: RISING:
Rising edge

0x2: FALLING:
Falling edge

0x3: BOTH:
Both rising and falling edges

17.1.50 GPIO_PRT5_INTR

Port interrupt status register

Address: 0x40040510

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1C	RW1C
HW Access	None						A	A
Name	None [7:2]						DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1C
HW Access	None							A
Name	None [15:9]							FLT_DATA

Bits	23	22	21	20	19	18	17	16
SW Access	None						R	R
HW Access	None						W	W
Name	None [23:18]						PS_DATA1	PS_DATA0

Bits	31	30	29	28	27	26	25	24
SW Access	None							R
HW Access	None							W
Name	None [31:25]							PS_FLT_DATA

Bits	Name	Description
24	PS_FLT_DATA	This is a duplicate of the contents of the PS register, provided here to allow reading of both pin state and interrupt state of the port in a single read operation. Default Value: 0
17	PS_DATA1	Default Value: 0
16	PS_DATA0	` Default Value: 0
8	FLT_DATA	Deglitched interrupt pending (selected by FLT_SELECT). Default Value: 0
1	DATA1	Interrupt pending on IO pad 1. Firmware writes 1 to clear the interrupt. Default Value: 0
0	DATA0	Interrupt pending on IO pad 0. Firmware writes 1 to clear the interrupt. Default Value: 0

17.1.51 GPIO_PRT5_PC2

Port configuration register 2

Address: 0x40040518

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						INP_DIS1	INP_DIS0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	INP_DIS1	Disables the input buffer for IO pad 1. Default Value: 0
0	INP_DIS0	Disables the input buffer for IO pad 0 independent of the port control drive mode (PC.DM). This bit should be set when analog signals are present on the pin and PC.DM != 0 is required to use the output driver. Default Value: 0

17.1.52 GPIO_PRT5_DR_SET

Port output data set register

Address: 0x40040540

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	IO pad i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] set to '1'. Default Value: 0

17.1.53 GPIO_PRT5_DR_CLR

Port output data clear register

Address: 0x40040544

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	IO pad i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] set to '0'. Default Value: 0

17.1.54 GPIO_PRT5_DR_INV

Port output data invert register

Address: 0x40040548

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	IO pad i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] inverted ('0' => '1', '1' => '0'). Default Value: 0

17.1.55 GPIO_PRT6_DR

Port output data register

Address: 0x40040600

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						RW	RW
Name	None [7:2]						DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	DATA1	IO pad 1 output data. Default Value: 0
0	DATA0	IO pad 0 output data. Default Value: 0

17.1.56 GPIO_PRT6_PS

Port IO pad state register

Address: 0x40040604

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						W	W
Name	None [7:2]						DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							FLT_DATA

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_DATA	Reads of this register return the logical state of the filtered pin. Default Value: 0
1	DATA1	IO pad 1 state. Default Value: 0
0	DATA0	IO pad 0 state: 1: Logic high, if the pin voltage is above the input buffer threshold, logic high. 0: Logic low, if the pin voltage is below that threshold, logic low. If the drive mode for the pin is set to high Z Analog, the pin state will read 0 independent of the voltage on the pin. Default Value: 0

17.1.57 GPIO_PRT6_PC

Port configuration register

Address: 0x40040608

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW			RW		
HW Access	None		R			R		
Name	None [7:6]		DM1 [5:3]			DM0 [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None				RW	RW
HW Access	R		None				R	R
Name	PORT_IB_MODE_SEL [31:30]		None [29:26]				PORT_SLOW	PORT_VTRIP_SEL

Bits	Name	Description
31 : 30	PORT_IB_MODE_SEL	This field selects the input buffer reference. The size (1 or 2 bits) and functionality is dependent on the IO cell. For GPIOv2 IO cells, bit PORT_IB_MODE_SEL[1] is not used (GPIOv2 IO cell replaces GPIO IO cell): "0"/"2": CMOS input buffer (PORT_VTRIP_SEL is '0'), LVTTL input buffer (PORT_VTRIP_SEL is '1') "1"/"3": vcchib. For GPIO_OVTv2 and SIOv2 IO cells: "0": CMOS input buffer (PORT_VTRIP_SEL is '0'), LVTTL input buffer (PORT_VTRIP_SEL is '1') "1": vcchib. "2": OVT. "3": Reference (possibly from reference generator cell). For SIO IO cell, this field is present but not used as the SIO IO cell does not provide input buffer mode select functionality (SIOv2 IO cell will replace SIO IO cell, as soon as it is available). Default Value: 0
25	PORT_SLOW	This field controls the output edge rate of all pins on the port: '0': fast. '1': slow. Default Value: 0

(continued)

		0x0: PORT_SLEW_CTL_0: HS mode (100pf < Cb < 400pF, 1.71<5.5, Vext>3.0) FS mode (10pf<400pf,1.71<5.5) (20-160ns) **0x1: PORT_SLEW_CTL_1:** HS mode (Cb<100pf,1.71<5.5,Vext>2.8,F=1.7MHz) (10-80ns) FS+ Mode (Vext>2.8,1.71<5.5) (20-120ns) **0x2: PORT_SLEW_CTL_2:** HS mode (100pf<400pf, 1.71<5.5,Vext<3.3) (20-160ns) **0x3: PORT_SLEW_CTL_3:** HS mode (Cb<100pf,1.71<5.5,Vext<=2.8,F=1.7MHz) (10-80ns) FS+ mode (Vext<=2.8,1.71<5.5) (20-120ns)
24	PORT_VTRIP_SEL	The GPIO cells include a VTRIP_SEL signal to alter the input buffer voltage. Note: this bit is ignored for SIO ports, the VTRIP_SEL settings in the SIO register are used instead (a separate VTRIP_SEL is provided for each pin pair). 0: input buffer functions as a CMOS input buffer. 1: input buffer functions as a LVTTL input buffer. Default Value: 0
5 : 3	DM1	The GPIO drive mode for IO pad 1. Default Value: 0
2 : 0	DM0	The GPIO drive mode for IO pad 0. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the HSIOM is properly configured (HSIOM_PRT_SELx) before turning the IO on here to avoid producing glitches on the bus. Default Value: 0 **0x0: OFF:** Mode 0 (analog mode): Output buffer off (high Z). Input buffer off. **0x1: INPUT:** Mode 1: Output buffer off (high Z). Input buffer on. **0x2: 0_PU:** Mode 2: Strong pull down ('0'), weak/resistive pull up (PU). Input buffer on. **0x3: PD_1:** Mode 3: Weak/resistive pull down (PD), strong pull up ('1'). Input buffer on. **0x4: 0_Z:** Mode 4: Strong pull down ('0'), open drain (pull up off). Input buffer on. **0x5: Z_1:** Mode 5: Open drain (pull down off), strong pull up ('1'). Input buffer on. **0x6: 0_1:** Mode 6: Strong pull down ('0'), strong pull up ('1'). Input buffer on. **0x7: PD_PU:** Mode 7: Weak/resistive pull down (PD), weak/resistive pull up (PU). Input buffer on.

17.1.58 GPIO_PRT6_INTR_CFG

Port interrupt configuration register

Address: 0x4004060C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW		RW	
HW Access	None				R		R	
Name	None [7:4]				EDGE1_SEL [3:2]		EDGE0_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW			RW	
HW Access	None			R			R	
Name	None [23:21]			FLT_SEL [20:18]			FLT_EDGE_SEL [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
20 : 18	FLT_SEL	Selects which pin is routed through the 50ns glitch filter to provide a glitch-safe interrupt. Default Value: 0
17 : 16	FLT_EDGE_SEL	Same for the glitch filtered pin (selected by FLT_SELECT). Default Value: 0 **0x0: DISABLE:** Disabled **0x1: RISING:** Rising edge **0x2: FALLING:** Falling edge **0x3: BOTH:** Both rising and falling edges
3 : 2	EDGE1_SEL	Sets which edge will trigger an IRQ for IO pad 1. Default Value: 0
1 : 0	EDGE0_SEL	Sets which edge will trigger an IRQ for IO pad 0. Default Value: 0

(continued)

0x0: DISABLE:
Disabled

0x1: RISING:
Rising edge

0x2: FALLING:
Falling edge

0x3: BOTH:
Both rising and falling edges

17.1.59 GPIO_PRT6_INTR

Port interrupt status register

Address: 0x40040610

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1C	RW1C
HW Access	None						A	A
Name	None [7:2]						DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1C
HW Access	None							A
Name	None [15:9]							FLT_DATA

Bits	23	22	21	20	19	18	17	16
SW Access	None						R	R
HW Access	None						W	W
Name	None [23:18]						PS_DATA1	PS_DATA0

Bits	31	30	29	28	27	26	25	24
SW Access	None							R
HW Access	None							W
Name	None [31:25]							PS_FLT_DATA

Bits	Name	Description
24	PS_FLT_DATA	This is a duplicate of the contents of the PS register, provided here to allow reading of both pin state and interrupt state of the port in a single read operation. Default Value: 0
17	PS_DATA1	Default Value: 0
16	PS_DATA0	` Default Value: 0
8	FLT_DATA	Deglitched interrupt pending (selected by FLT_SELECT). Default Value: 0
1	DATA1	Interrupt pending on IO pad 1. Firmware writes 1 to clear the interrupt. Default Value: 0
0	DATA0	Interrupt pending on IO pad 0. Firmware writes 1 to clear the interrupt. Default Value: 0

17.1.60 GPIO_PRT6_PC2

Port configuration register 2

Address: 0x40040618

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						INP_DIS1	INP_DIS0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	INP_DIS1	Disables the input buffer for IO pad 1. Default Value: 0
0	INP_DIS0	Disables the input buffer for IO pad 0 independent of the port control drive mode (PC.DM). This bit should be set when analog signals are present on the pin and PC.DM != 0 is required to use the output driver. Default Value: 0

17.1.61 GPIO_PRT6_DR_SET

Port output data set register

Address: 0x40040640

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	IO pad i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] set to '1'. Default Value: 0

17.1.62 GPIO_PRT6_DR_CLR

Port output data clear register

Address: 0x40040644

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	IO pad i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] set to '0'. Default Value: 0

17.1.63 GPIO_PRT6_DR_INV

Port output data invert register

Address: 0x40040648

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	IO pad i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] inverted ('0' => '1', '1' => '0'). Default Value: 0

18 High Speed IO Matrix (HSIOM) Registers

This section discusses the HSIOM registers. It lists all the registers in mapping tables, in address order.

18.1 Register Details

Register Name	Address
HSIOM_AMUX_SPLIT_CTL0	0x40022100
HSIOM_AMUX_SPLIT_CTL1	0x40022104
HSIOM_AMUX_SPLIT_CTL2	0x40022108

18.1.1 HSIOM_AMUX_SPLIT_CTL0

AMUX splitter cell control

Address: 0x40022100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	RW	RW	None	RW	RW	RW
HW Access	None	R	R	R	None	R	R	R
Name	None	SWITCH_BB_S0	SWITCH_BB_SR	SWITCH_BB_SL	None	SWITCH_AA_S0	SWITCH_AA_SR	SWITCH_AA_SL

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
6	SWITCH_BB_S0	T-switch control for AMUXBUSB vssa/ground switch. Default Value: 0
5	SWITCH_BB_SR	T-switch control for Right AMUXBUSB switch. Default Value: 0
4	SWITCH_BB_SL	T-switch control for Left AMUXBUSB switch. Default Value: 0
2	SWITCH_AA_S0	T-switch control for AMUXBUSA vssa/ground switch: '0': switch open. '1': switch closed. Default Value: 0
1	SWITCH_AA_SR	T-switch control for Right AMUXBUSA switch: '0': switch open. '1': switch closed. Default Value: 0

(continued)

0	SWITCH_AA_SL	T-switch control for Left AMUXBUSA switch: '0': switch open. '1': switch closed. Default Value: 0

18.1.2 HSIOM_AMUX_SPLIT_CTL1

AMUX splitter cell control

Address: 0x40022104

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	RW	RW	None	RW	RW	RW
HW Access	None	R	R	R	None	R	R	R
Name	None	SWITCH_BB_S0	SWITCH_BB_SR	SWITCH_BB_SL	None	SWITCH_AA_S0	SWITCH_AA_SR	SWITCH_AA_SL

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
6	SWITCH_BB_S0	T-switch control for AMUXBUSB vssa/ground switch. Default Value: 0
5	SWITCH_BB_SR	T-switch control for Right AMUXBUSB switch. Default Value: 0
4	SWITCH_BB_SL	T-switch control for Left AMUXBUSB switch. Default Value: 0
2	SWITCH_AA_S0	T-switch control for AMUXBUSA vssa/ground switch: '0': switch open. '1': switch closed. Default Value: 0
1	SWITCH_AA_SR	T-switch control for Right AMUXBUSA switch: '0': switch open. '1': switch closed. Default Value: 0

(continued)

0	SWITCH_AA_SL	T-switch control for Left AMUXBUSA switch: '0': switch open. '1': switch closed. Default Value: 0

18.1.3 HSIOM_AMUX_SPLIT_CTL2

AMUX splitter cell control

Address: 0x40022108

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	RW	RW	None	RW	RW	RW
HW Access	None	R	R	R	None	R	R	R
Name	None	SWITCH_BB_S0	SWITCH_BB_SR	SWITCH_BB_SL	None	SWITCH_AA_S0	SWITCH_AA_SR	SWITCH_AA_SL

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
6	SWITCH_BB_S0	T-switch control for AMUXBUSB vssa/ground switch. Default Value: 0
5	SWITCH_BB_SR	T-switch control for Right AMUXBUSB switch. Default Value: 0
4	SWITCH_BB_SL	T-switch control for Left AMUXBUSB switch. Default Value: 0
2	SWITCH_AA_S0	T-switch control for AMUXBUSA vssa/ground switch: '0': switch open. '1': switch closed. Default Value: 0
1	SWITCH_AA_SR	T-switch control for Right AMUXBUSA switch: '0': switch open. '1': switch closed. Default Value: 0

(continued)

0	SWITCH_AA_SL	T-switch control for Left AMUXBUSA switch: '0': switch open. '1': switch closed. Default Value: 0

19 HSIOM Port Registers

This section discusses the HSIOM Port registers. It lists all the registers in mapping tables, in address order.

19.1 Register Details

Register Name	Address
HSIOM_PORT_SEL0	0x40020000
HSIOM_PORT_SEL1	0x40020100
HSIOM_PORT_SEL2	0x40020200
HSIOM_PORT_SEL3	0x40020300
HSIOM_PORT_SEL4	0x40020400
HSIOM_PORT_SEL5	0x40020500
HSIOM_PORT_SEL6	0x40020600

19.1.1 HSIOM_PORT_SEL0

Port selection register

Address: 0x40020000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO1_SEL [7:4]				IO0_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO3_SEL [15:12]				IO2_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO5_SEL [23:20]				IO4_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO7_SEL [31:28]				IO6_SEL [27:24]			

Bits	Name	Description
31 : 28	IO7_SEL	Selects connection for IO pad 7 route. Default Value: 0
27 : 24	IO6_SEL	Selects connection for IO pad 6 route. Default Value: 0
23 : 20	IO5_SEL	Selects connection for IO pad 5 route. Default Value: 0
19 : 16	IO4_SEL	Selects connection for IO pad 4 route. Default Value: 0
15 : 12	IO3_SEL	Selects connection for IO pad 3 route. Default Value: 0
11 : 8	IO2_SEL	Selects connection for IO pad 2 route. Default Value: 0
7 : 4	IO1_SEL	Selects connection for IO pad 1 route. Default Value: 0
3 : 0	IO0_SEL	Selects connection for IO pad 0 route. Default Value: 0

(continued)

0x0: GPIO:
SW controlled GPIO.

0x1: GPIO_DSI:
SW controlled "out", DSI controlled "oe_n".

0x2: DSI_DSI:
DSI controlled "out" and "oe_n".

0x3: DSI_GPIO:
DSI controlled "out", SW controlled "oe_n".

0x4: CSD_SENSE:
CSD sense connection (analog mode)

0x5: CSD_SHIELD:
CSD shield connection (analog mode)

0x6: AMUXA:
AMUXBUS A connection.

0x7: AMUXB:
AMUXBUS B connection. This mode is also used for CSD GPIO charging. When CSD GPIO charging is enabled in CSD_CONTROL, "oe_n" is connected to "!csd_charge" signal (and IO pad is also still connected to AMUXBUS B).

0x8: ACT_0:
Chip specific Active source 0 connection.

0x9: ACT_1:
Chip specific Active source 1 connection.

0xa: ACT_2:
Chip specific Active source 2 connection.

0xb: ACT_3:
Chip specific Active source 3 connection.

0xc: LCD_COM:
LCD common connection. This mode provides DeepSleep functionality (provided that the LCD block is enabled and properly configured).

0xc: DS_0:
Chip specific DeepSleep source 0 connection.

0xd: LCD_SEG:
LCD segment connection. This mode provides DeepSleep functionality (provided that the LCD block is enabled and properly configured).

0xd: DS_1:
Chip specific DeepSleep source 1 connection.

0xe: DS_2:
Chip specific DeepSleep source 2 connection.

0xf: DS_3:
Chip specific DeepSleep source 3 connection.

19.1.2 HSIOM_PORT_SEL1

Port selection register

Address: 0x40020100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO1_SEL [7:4]				IO0_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO3_SEL [15:12]				IO2_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO5_SEL [23:20]				IO4_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO7_SEL [31:28]				IO6_SEL [27:24]			

Bits	Name	Description
31 : 28	IO7_SEL	Selects connection for IO pad 7 route. Default Value: 0
27 : 24	IO6_SEL	Selects connection for IO pad 6 route. Default Value: 0
23 : 20	IO5_SEL	Selects connection for IO pad 5 route. Default Value: 0
19 : 16	IO4_SEL	Selects connection for IO pad 4 route. Default Value: 0
15 : 12	IO3_SEL	Selects connection for IO pad 3 route. Default Value: 0
11 : 8	IO2_SEL	Selects connection for IO pad 2 route. Default Value: 0
7 : 4	IO1_SEL	Selects connection for IO pad 1 route. Default Value: 0
3 : 0	IO0_SEL	Selects connection for IO pad 0 route. Default Value: 0

(continued)

0x0: GPIO:
SW controlled GPIO.

0x1: GPIO_DSI:
SW controlled "out", DSI controlled "oe_n".

0x2: DSI_DSI:
DSI controlled "out" and "oe_n".

0x3: DSI_GPIO:
DSI controlled "out", SW controlled "oe_n".

0x4: CSD_SENSE:
CSD sense connection (analog mode)

0x5: CSD_SHIELD:
CSD shield connection (analog mode)

0x6: AMUXA:
AMUXBUS A connection.

0x7: AMUXB:
AMUXBUS B connection. This mode is also used for CSD GPIO charging. When CSD GPIO charging is enabled in CSD_CONTROL, "oe_n" is connected to "!csd_charge" signal (and IO pad is also still connected to AMUXBUS B).

0x8: ACT_0:
Chip specific Active source 0 connection.

0x9: ACT_1:
Chip specific Active source 1 connection.

0xa: ACT_2:
Chip specific Active source 2 connection.

0xb: ACT_3:
Chip specific Active source 3 connection.

0xc: LCD_COM:
LCD common connection. This mode provides DeepSleep functionality (provided that the LCD block is enabled and properly configured).

0xc: DS_0:
Chip specific DeepSleep source 0 connection.

0xd: LCD_SEG:
LCD segment connection. This mode provides DeepSleep functionality (provided that the LCD block is enabled and properly configured).

0xd: DS_1:
Chip specific DeepSleep source 1 connection.

0xe: DS_2:
Chip specific DeepSleep source 2 connection.

0xf: DS_3:
Chip specific DeepSleep source 3 connection.

19.1.3 HSIOM_PORT_SEL2

Port selection register

Address: 0x40020200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO1_SEL [7:4]				IO0_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO3_SEL [15:12]				IO2_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO5_SEL [23:20]				IO4_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO7_SEL [31:28]				IO6_SEL [27:24]			

Bits	Name	Description
31 : 28	IO7_SEL	Selects connection for IO pad 7 route. Default Value: 0
27 : 24	IO6_SEL	Selects connection for IO pad 6 route. Default Value: 0
23 : 20	IO5_SEL	Selects connection for IO pad 5 route. Default Value: 0
19 : 16	IO4_SEL	Selects connection for IO pad 4 route. Default Value: 0
15 : 12	IO3_SEL	Selects connection for IO pad 3 route. Default Value: 0
11 : 8	IO2_SEL	Selects connection for IO pad 2 route. Default Value: 0
7 : 4	IO1_SEL	Selects connection for IO pad 1 route. Default Value: 0
3 : 0	IO0_SEL	Selects connection for IO pad 0 route. Default Value: 0

(continued)

0x0: GPIO:
SW controlled GPIO.

0x1: GPIO_DSI:
SW controlled "out", DSI controlled "oe_n".

0x2: DSI_DSI:
DSI controlled "out" and "oe_n".

0x3: DSI_GPIO:
DSI controlled "out", SW controlled "oe_n".

0x4: CSD_SENSE:
CSD sense connection (analog mode)

0x5: CSD_SHIELD:
CSD shield connection (analog mode)

0x6: AMUXA:
AMUXBUS A connection.

0x7: AMUXB:
AMUXBUS B connection. This mode is also used for CSD GPIO charging. When CSD GPIO charging is enabled in CSD_CONTROL, "oe_n" is connected to "!csd_charge" signal (and IO pad is also still connected to AMUXBUS B).

0x8: ACT_0:
Chip specific Active source 0 connection.

0x9: ACT_1:
Chip specific Active source 1 connection.

0xa: ACT_2:
Chip specific Active source 2 connection.

0xb: ACT_3:
Chip specific Active source 3 connection.

0xc: LCD_COM:
LCD common connection. This mode provides DeepSleep functionality (provided that the LCD block is enabled and properly configured).

0xc: DS_0:
Chip specific DeepSleep source 0 connection.

0xd: LCD_SEG:
LCD segment connection. This mode provides DeepSleep functionality (provided that the LCD block is enabled and properly configured).

0xd: DS_1:
Chip specific DeepSleep source 1 connection.

0xe: DS_2:
Chip specific DeepSleep source 2 connection.

0xf: DS_3:
Chip specific DeepSleep source 3 connection.

19.1.4 HSIOM_PORT_SEL3

Port selection register

Address: 0x40020300

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO1_SEL [7:4]				IO0_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO3_SEL [15:12]				IO2_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO5_SEL [23:20]				IO4_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO7_SEL [31:28]				IO6_SEL [27:24]			

Bits	Name	Description
31 : 28	IO7_SEL	Selects connection for IO pad 7 route. Default Value: 0
27 : 24	IO6_SEL	Selects connection for IO pad 6 route. Default Value: 0
23 : 20	IO5_SEL	Selects connection for IO pad 5 route. Default Value: 0
19 : 16	IO4_SEL	Selects connection for IO pad 4 route. Default Value: 0
15 : 12	IO3_SEL	Selects connection for IO pad 3 route. Default Value: 0
11 : 8	IO2_SEL	Selects connection for IO pad 2 route. Default Value: 0
7 : 4	IO1_SEL	Selects connection for IO pad 1 route. Default Value: 0
3 : 0	IO0_SEL	Selects connection for IO pad 0 route. Default Value: 0

(continued)

0x0: GPIO:
SW controlled GPIO.

0x1: GPIO_DSI:
SW controlled "out", DSI controlled "oe_n".

0x2: DSI_DSI:
DSI controlled "out" and "oe_n".

0x3: DSI_GPIO:
DSI controlled "out", SW controlled "oe_n".

0x4: CSD_SENSE:
CSD sense connection (analog mode)

0x5: CSD_SHIELD:
CSD shield connection (analog mode)

0x6: AMUXA:
AMUXBUS A connection.

0x7: AMUXB:
AMUXBUS B connection. This mode is also used for CSD GPIO charging. When CSD GPIO charging is enabled in CSD_CONTROL, "oe_n" is connected to "!csd_charge" signal (and IO pad is also still connected to AMUXBUS B).

0x8: ACT_0:
Chip specific Active source 0 connection.

0x9: ACT_1:
Chip specific Active source 1 connection.

0xa: ACT_2:
Chip specific Active source 2 connection.

0xb: ACT_3:
Chip specific Active source 3 connection.

0xc: LCD_COM:
LCD common connection. This mode provides DeepSleep functionality (provided that the LCD block is enabled and properly configured).

0xc: DS_0:
Chip specific DeepSleep source 0 connection.

0xd: LCD_SEG:
LCD segment connection. This mode provides DeepSleep functionality (provided that the LCD block is enabled and properly configured).

0xd: DS_1:
Chip specific DeepSleep source 1 connection.

0xe: DS_2:
Chip specific DeepSleep source 2 connection.

0xf: DS_3:
Chip specific DeepSleep source 3 connection.

19.1.5 HSIOM_PORT_SEL4

Port selection register

Address: 0x40020400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO1_SEL [7:4]				IO0_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	IO1_SEL	Selects connection for IO pad 1 route. Default Value: 0
3 : 0	IO0_SEL	Selects connection for IO pad 0 route. Default Value: 0 **0x0: GPIO:** SW controlled GPIO. **0x1: GPIO_DSI:** SW controlled "out", DSI controlled "oe_n". **0x2: DSI_DSI:** DSI controlled "out" and "oe_n". **0x3: DSI_GPIO:** DSI controlled "out", SW controlled "oe_n". **0x4: CSD_SENSE:** CSD sense connection (analog mode) **0x5: CSD_SHIELD:** CSD shield connection (analog mode)

(continued)

0x6: AMUXA:
AMUXBUS A connection.

0x7: AMUXB:
AMUXBUS B connection. This mode is also used for CSD GPIO charging. When CSD GPIO charging is enabled in CSD_CONTROL, "oe_n" is connected to "!csd_charge" signal (and IO pad is also still connected to AMUXBUS B).

0x8: ACT_0:
Chip specific Active source 0 connection.

0x9: ACT_1:
Chip specific Active source 1 connection.

0xa: ACT_2:
Chip specific Active source 2 connection.

0xb: ACT_3:
Chip specific Active source 3 connection.

0xc: LCD_COM:
LCD common connection. This mode provides DeepSleep functionality (provided that the LCD block is enabled and properly configured).

0xc: DS_0:
Chip specific DeepSleep source 0 connection.

0xd: LCD_SEG:
LCD segment connection. This mode provides DeepSleep functionality (provided that the LCD block is enabled and properly configured).

0xd: DS_1:
Chip specific DeepSleep source 1 connection.

0xe: DS_2:
Chip specific DeepSleep source 2 connection.

0xf: DS_3:
Chip specific DeepSleep source 3 connection.

19.1.6 HSIOM_PORT_SEL5

Port selection register

Address: 0x40020500

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO1_SEL [7:4]				IO0_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	IO1_SEL	Selects connection for IO pad 1 route. Default Value: 0
3 : 0	IO0_SEL	Selects connection for IO pad 0 route. Default Value: 0 **0x0: GPIO:** SW controlled GPIO. **0x1: GPIO_DSI:** SW controlled "out", DSI controlled "oe_n". **0x2: DSI_DSI:** DSI controlled "out" and "oe_n". **0x3: DSI_GPIO:** DSI controlled "out", SW controlled "oe_n". **0x4: CSD_SENSE:** CSD sense connection (analog mode) **0x5: CSD_SHIELD:** CSD shield connection (analog mode)

(continued)

0x6: AMUXA:
AMUXBUS A connection.

0x7: AMUXB:
AMUXBUS B connection. This mode is also used for CSD GPIO charging. When CSD GPIO charging is enabled in CSD_CONTROL, "oe_n" is connected to "!csd_charge" signal (and IO pad is also still connected to AMUXBUS B).

0x8: ACT_0:
Chip specific Active source 0 connection.

0x9: ACT_1:
Chip specific Active source 1 connection.

0xa: ACT_2:
Chip specific Active source 2 connection.

0xb: ACT_3:
Chip specific Active source 3 connection.

0xc: LCD_COM:
LCD common connection. This mode provides DeepSleep functionality (provided that the LCD block is enabled and properly configured).

0xc: DS_0:
Chip specific DeepSleep source 0 connection.

0xd: LCD_SEG:
LCD segment connection. This mode provides DeepSleep functionality (provided that the LCD block is enabled and properly configured).

0xd: DS_1:
Chip specific DeepSleep source 1 connection.

0xe: DS_2:
Chip specific DeepSleep source 2 connection.

0xf: DS_3:
Chip specific DeepSleep source 3 connection.

19.1.7 HSIOM_PORT_SEL6

Port selection register

Address: 0x40020600

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO1_SEL [7:4]				IO0_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	IO1_SEL	Selects connection for IO pad 1 route. Default Value: 0
3 : 0	IO0_SEL	Selects connection for IO pad 0 route. Default Value: 0 **0x0: GPIO:** SW controlled GPIO. **0x1: GPIO_DSI:** SW controlled "out", DSI controlled "oe_n". **0x2: DSI_DSI:** DSI controlled "out" and "oe_n". **0x3: DSI_GPIO:** DSI controlled "out", SW controlled "oe_n". **0x4: CSD_SENSE:** CSD sense connection (analog mode) **0x5: CSD_SHIELD:** CSD shield connection (analog mode)

(continued)

0x6: AMUXA:
AMUXBUS A connection.

0x7: AMUXB:
AMUXBUS B connection. This mode is also used for CSD GPIO charging. When CSD GPIO charging is enabled in CSD_CONTROL, "oe_n" is connected to "!csd_charge" signal (and IO pad is also still connected to AMUXBUS B).

0x8: ACT_0:
Chip specific Active source 0 connection.

0x9: ACT_1:
Chip specific Active source 1 connection.

0xa: ACT_2:
Chip specific Active source 2 connection.

0xb: ACT_3:
Chip specific Active source 3 connection.

0xc: LCD_COM:
LCD common connection. This mode provides DeepSleep functionality (provided that the LCD block is enabled and properly configured).

0xc: DS_0:
Chip specific DeepSleep source 0 connection.

0xd: LCD_SEG:
LCD segment connection. This mode provides DeepSleep functionality (provided that the LCD block is enabled and properly configured).

0xd: DS_1:
Chip specific DeepSleep source 1 connection.

0xe: DS_2:
Chip specific DeepSleep source 2 connection.

0xf: DS_3:
Chip specific DeepSleep source 3 connection.

20 LCD Registers

This section discusses the LCD registers. It lists all the registers in mapping tables, in address order.

20.1 Register Details

Register Name	Address
LCD_ID	0x402A0000
LCD_DIVIDER	0x402A0004
LCD_CONTROL	0x402A0008
LCD_DATA00	0x402A0100
LCD_DATA01	0x402A0104
LCD_DATA02	0x402A0108
LCD_DATA03	0x402A010C
LCD_DATA04	0x402A0110
LCD_DATA05	0x402A0114
LCD_DATA06	0x402A0118
LCD_DATA07	0x402A011C

20.1.1 LCD_ID

ID & Revision

Address: 0x402A0000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	ID [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	REVISION [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	REVISION [31:24]							

Bits	Name	Description
31 : 16	REVISION	the version number is 0x0001 Default Value: 1
15 : 0	ID	the ID of LCD controller peripheral is 0xF0F0 Default Value: 61680

20.1.2 LCD_DIVIDER

LCD Divider Register

Address: 0x402A0004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SUBFR_DIV [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	SUBFR_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DEAD_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	DEAD_DIV [31:24]							

Bits	Name	Description
31 : 16	DEAD_DIV	Length of the dead time period in cycles. When set to zero, no dead time period exists. Default Value: 0
15 : 0	SUBFR_DIV	Input clock frequency divide value, to generate the 1/4 sub-frame period. The sub-frame period is 4*(SUBFR_DIV+1) cycles long. Default Value: 0

20.1.3 LCD_CONTROL

LCD Configuration Register

Address: 0x402A0008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW		RW	RW	RW	RW	RW
HW Access	None	R		R	R	R	R	R
Name	None	BIAS [6:5]		OP_MODE	TYPE	LCD_MODE	HS_EN	LS_EN

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				COM_NUM [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	LS_EN_STAT	None [30:24]						

Bits	Name	Description
31	LS_EN_STAT	LS enable status bit. This bit is a copy of LS_EN that is synchronized to the low speed clock domain and back to the system clock domain. Firmware can use this bit to observe whether LS_EN has taken effect in the low speed clock domain. Firmware should never change the configuration for the LS generator without ensuring this bit is 0. The following procedure should be followed to disable the LS generator: 1. If LS_EN=0 we are done. Exit the procedure. 2. Check that LS_EN_STAT=1. If not, wait until it is. This will catch the case of a recent enable (LS_EN=1) that has not taken effect yet. 3. Set LS_EN=0. 4. Wait until LS_EN_STAT=0. Default Value: 0

(continued)

11 : 8	COM_NUM	The number of COM connections minus 2. So: 0: 2 COM's 1: 3 COM's ... 13: 15 COM's 14: 16 COM's 15: undefined Default Value: 0
6 : 5	BIAS	PWM bias selection Default Value: 0 **0x0: HALF:** 1/2 Bias **0x1: THIRD:** 1/3 Bias **0x2: FOURTH:** 1/4 Bias (not supported by LS generator) **0x3: FIFTH:** 1/5 Bias (not supported by LS generator)
4	OP_MODE	Driving mode configuration Default Value: 0 **0x0: PWM:** PWM Mode **0x1: CORRELATION:** Digital Correlation Mode
3	TYPE	LCD driving waveform type configuration. Default Value: 0 **0x0: TYPE_A:** Type A - Each frame addresses each COM pin only once with a balanced (DC=0) waveform. **0x1: TYPE_B:** Type B - Each frame addresses each COM pin twice in sequence with a positive and negative waveform that together are balanced (DC=0).
2	LCD_MODE	HS/LS Mode selection Default Value: 0 **0x0: LS:** Select Low Speed (32kHz) Generator (Works in Active, Sleep and DeepSleep power modes). **0x1: HS:** Select High Speed (system clock) Generator (Works in Active and Sleep power modes only).
1	HS_EN	High speed (HS) generator enable 1: enable 0: disable Default Value: 0
0	LS_EN	Low speed (LS) generator enable 1: enable 0: disable Default Value: 0

20.1.4 LCD_DATA00

LCD Pin Data Registers

Address: 0x402A0100

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Bits [4i+3:4i] represent the pin data for pin [i] for COMS 1-4 (COM1 is lsb). Default Value: 0

20.1.5 LCD_DATA01

LCD Pin Data Registers

Address: 0x402A0104

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Bits [4i+3:4i] represent the pin data for pin [i] for COMS 1-4 (COM1 is lsb). Default Value: 0

20.1.6 LCD_DATA02

LCD Pin Data Registers

Address: 0x402A0108

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Bits [4i+3:4i] represent the pin data for pin [i] for COMS 1-4 (COM1 is lsb). Default Value: 0

20.1.7 LCD_DATA03

LCD Pin Data Registers

Address: 0x402A010C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Bits [4i+3:4i] represent the pin data for pin [i] for COMS 1-4 (COM1 is lsb). Default Value: 0

20.1.8 LCD_DATA04

LCD Pin Data Registers

Address: 0x402A0110

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Bits [4i+3:4i] represent the pin data for pin [i] for COMS 1-4 (COM1 is lsb). Default Value: 0

20.1.9 LCD_DATA05

LCD Pin Data Registers

Address: 0x402A0114

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Bits [4i+3:4i] represent the pin data for pin [i] for COMS 1-4 (COM1 is lsb). Default Value: 0

20.1.10 LCD_DATA06

LCD Pin Data Registers

Address: 0x402A0118

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Bits [4i+3:4i] represent the pin data for pin [i] for COMS 1-4 (COM1 is lsb). Default Value: 0

20.1.11 LCD_DATA07

LCD Pin Data Registers

Address: 0x402A011C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Bits [4i+3:4i] represent the pin data for pin [i] for COMS 1-4 (COM1 is lsb). Default Value: 0

21 Low Power Comparator (LPCOMP) Registers

This section discusses the LPCOMP registers. It lists all the registers in mapping tables, in address order.

21.1 Register Details

Register Name	Address
LPCOMP_ID	0x402B0000
LPCOMP_CONFIG	0x402B0004
LPCOMP_INTR	0x402B0010
LPCOMP_INTR_SET	0x402B0014
LPCOMP_INTR_MASK	0x402B0018
LPCOMP_INTR_MASKED	0x402B001C
LPCOMP_TRIM1	0x402BFF00
LPCOMP_TRIM2	0x402BFF04
LPCOMP_TRIM3	0x402BFF08
LPCOMP_TRIM4	0x402BFF0C

21.1.1 LPCOMP_ID

ID & Revision

Address: 0x402B0000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	None							
Name	ID [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	None							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	None							
Name	REVISION [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	None							
Name	REVISION [31:24]							

Bits	Name	Description
31 : 16	REVISION	the version number is 0x0001 Default Value: 1
15 : 0	ID	the ID of LPCOMP peripheral is 0xE0E0 Default Value: 57568

21.1.2 LPCOMP_CONFIG

LPCOMP Configuration Register

Address: 0x402B0004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	R	RW		RW	RW	RW	
HW Access	R	RW	R		R	R	R	
Name	ENABLE1	OUT1	INTTYPE1 [5:4]		FILTER1	HYST1	MODE1 [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW	R	RW		RW	RW	RW	
HW Access	R	RW	R		R	R	R	
Name	ENABLE2	OUT2	INTTYPE2 [13:12]		FILTER2	HYST2	MODE2 [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW	RW	None		RW	RW
HW Access	None		R	R	None		R	R
Name	None [23:22]		DSI_LEVEL2	DSI_BYPASS2	None [19:18]		DSI_LEVEL1	DSI_BYPASS1

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
21	DSI_LEVEL2	Opamp2 comparator DSI (trigger) out level : 0=pulse, 1=level Default Value: 0
20	DSI_BYPASS2	Opamp2 bypass comparator output synchronization for DSI output: 0=synchronize (level or pulse), 1=bypass (output async) Default Value: 0
17	DSI_LEVEL1	Opamp1 comparator DSI (trigger) out level : 0=pulse, 1=level Default Value: 0
16	DSI_BYPASS1	Opamp1 bypass comparator output synchronization for DSI output: 0=synchronize (level or pulse), 1=bypass (output async) Default Value: 0
15	ENABLE2	Enable comparator #2 Default Value: 0
14	OUT2	Current output value of the comparator. Default Value: 0
13 : 12	INTTYPE2	Sets which edge will trigger an IRQ Default Value: 0

(continued)

		0x0: DISABLE: Disabled, no interrupts will be detected
		0x1: RISING: Rising edge
		0x2: FALLING: Falling edge
		0x3: BOTH: Both rising and falling edges
11	FILTER2	Deprecated, Reserved, must be written 0 Default Value: 0
10	HYST2	Add 10mV hysteresis to the comparator - 0: Enable Hysteresis - 1: Disable Hysteresis Default Value: 0
9 : 8	MODE2	Operating mode for the comparator Default Value: 0
		0x0: SLOW: Slow operating mode (uses less power, <50uA)
		0x1: FAST: Fast operating mode (uses more power, <400uA)
		0x2: ULP: Ultra low power operting mode (uses ~2-4uA)
7	ENABLE1	Enable comparator #1 Default Value: 0
6	OUT1	Current output value of the comparator. Default Value: 0
5 : 4	INTTYPE1	Sets which edge will trigger an IRQ Default Value: 0
		0x0: DISABLE: Disabled, no interrupts will be detected
		0x1: RISING: Rising edge
		0x2: FALLING: Falling edge
		0x3: BOTH: Both rising and falling edges
3	FILTER1	Deprecated, Reserved, must be written 0 Default Value: 0
2	HYST1	Add 10mV hysteresis to the comparator - 0: Enable Hysteresis - 1: Disable Hysteresis Default Value: 0
1 : 0	MODE1	Operating mode for the comparator Default Value: 0
		0x0: SLOW: Slow operating mode (uses less power, <50uA)

(continued)

0x1: FAST:
Fast operating mode (uses more power, <400uA)

0x2: ULP:
Ultra low power operting mode (uses ~2-4uA)

21.1.3 LPCOMP_INTR

LPCOMP Interrupt request register

Address: 0x402B0010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1C	RW1C
HW Access	None						RW1S	RW1S
Name	None [7:2]						COMP2	COMP1

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	COMP2	Comparator 2 Interrupt: hardware sets this interrupt when comparator 0 triggers. Write with '1' to clear bit. Default Value: 0
0	COMP1	Comparator 1 Interrupt: hardware sets this interrupt when comparator 0 triggers. Write with '1' to clear bit. Default Value: 0

21.1.4 LPCOMP_INTR_SET

LPCOMP Interrupt set register

Address: 0x402B0014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1S	RW1S
HW Access	None						A	A
Name	None [7:2]						COMP2	COMP1

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	COMP2	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	COMP1	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

21.1.5 LPCOMP_INTR_MASK

LPCOMP Interrupt request mask

Address: 0x402B0018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						COMP2_MASK	COMP1_MASK

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	COMP2_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	COMP1_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0

21.1.6 LPCOMP_INTR_MASKED

LPCOMP Interrupt request masked

Address: 0x402B001C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						W	W
Name	None [7:2]						COMP2_MASKED	COMP1_MASKED

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	COMP2_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
0	COMP1_MASKED	Logical and of corresponding request and mask bits. Default Value: 0

21.1.7 LPCOMP_TRIM1

LPCOMP Trim Register

Address: 0x402BFF00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			R				
Name	None [7:5]			COMP1_TRIMA [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4 : 0	COMP1_TRIMA	Trim A for Comparator #1 Default Value: 0

21.1.8 LPCOMP_TRIM2

LPCOMP Trim Register

Address: 0x402BFF04

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			R				
Name	None [7:5]			COMP1_TRIMB [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4 : 0	COMP1_TRIMB	Trim B for Comparator #1 Default Value: 0

21.1.9 LPCOMP_TRIM3

LPCOMP Trim Register

Address: 0x402BFF08

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			R				
Name	None [7:5]			COMP2_TRIMA [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4 : 0	COMP2_TRIMA	Trim A for Comparator #2 Default Value: 0

21.1.10 LPCOMP_TRIM4

LPCOMP Trim Register

Address: 0x402BFF0C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			R				
Name	None [7:5]			COMP2_TRIMB [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4 : 0	COMP2_TRIMB	Trim B for Comparator #2 Default Value: 0

22 Port Adaptor (PA) Registers

This section discusses the PA registers. It lists all the registers in mapping tables, in address order.

22.1 Register Details

Register Name	Address
UDB_PA0_CFG0	0x400F5000
UDB_PA0_CFG1	0x400F5001
UDB_PA0_CFG2	0x400F5002
UDB_PA0_CFG3	0x400F5003
UDB_PA0_CFG4	0x400F5004
UDB_PA0_CFG5	0x400F5005
UDB_PA0_CFG6	0x400F5006
UDB_PA0_CFG7	0x400F5007
UDB_PA0_CFG8	0x400F5008
UDB_PA0_CFG9	0x400F5009
UDB_PA0_CFG10	0x400F500A
UDB_PA0_CFG11	0x400F500B
UDB_PA0_CFG12	0x400F500C
UDB_PA0_CFG13	0x400F500D
UDB_PA0_CFG14	0x400F500E
UDB_PA1_CFG0	0x400F5010
UDB_PA1_CFG1	0x400F5011
UDB_PA1_CFG2	0x400F5012
UDB_PA1_CFG3	0x400F5013
UDB_PA1_CFG4	0x400F5014
UDB_PA1_CFG5	0x400F5015
UDB_PA1_CFG6	0x400F5016
UDB_PA1_CFG7	0x400F5017
UDB_PA1_CFG8	0x400F5018
UDB_PA1_CFG9	0x400F5019
UDB_PA1_CFG10	0x400F501A

Register Name	Address
UDB_PA1_CFG11	0x400F501B
UDB_PA1_CFG12	0x400F501C
UDB_PA1_CFG13	0x400F501D
UDB_PA1_CFG14	0x400F501E
UDB_PA2_CFG0	0x400F5020
UDB_PA2_CFG1	0x400F5021
UDB_PA2_CFG2	0x400F5022
UDB_PA2_CFG3	0x400F5023
UDB_PA2_CFG4	0x400F5024
UDB_PA2_CFG5	0x400F5025
UDB_PA2_CFG6	0x400F5026
UDB_PA2_CFG7	0x400F5027
UDB_PA2_CFG8	0x400F5028
UDB_PA2_CFG9	0x400F5029
UDB_PA2_CFG10	0x400F502A
UDB_PA2_CFG11	0x400F502B
UDB_PA2_CFG12	0x400F502C
UDB_PA2_CFG13	0x400F502D
UDB_PA2_CFG14	0x400F502E
UDB_PA3_CFG0	0x400F5030
UDB_PA3_CFG1	0x400F5031
UDB_PA3_CFG2	0x400F5032
UDB_PA3_CFG3	0x400F5033
UDB_PA3_CFG4	0x400F5034
UDB_PA3_CFG5	0x400F5035
UDB_PA3_CFG6	0x400F5036
UDB_PA3_CFG7	0x400F5037
UDB_PA3_CFG8	0x400F5038
UDB_PA3_CFG9	0x400F5039
UDB_PA3_CFG10	0x400F503A
UDB_PA3_CFG11	0x400F503B
UDB_PA3_CFG12	0x400F503C
UDB_PA3_CFG13	0x400F503D
UDB_PA3_CFG14	0x400F503E

22.1.1 UDB_PA0_CFG0

PA Data In Clock Control Register

Address: 0x400F5000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW	RW	RW		RW	
HW Access	R		R	R	R		R	
Name	NC [7:6]		CLKIN_INV	CLKIN_EN_INV	CLKIN_EN_MODE [3:2]		CLKIN_EN_SEL [1:0]	

Bits	Name	Description
7 : 6	NC	Spare register bits Default Value: 0
5	CLKIN_INV	Determines whether the selected clock is inverted or not. Default Value: 0 **0x0: NOINV:** Not Inverted **0x1: INV:** Inverted
4	CLKIN_EN_INV	Determines whether the selected enable is inverted or not. Default Value: 0 **0x0: NOINV:** Not Inverted **0x1: INV:** Inverted
3 : 2	CLKIN_EN_MODE	Select one of four operating modes Default Value: 0 **0x0: OFF:** Always off **0x1: ON:** Always on **0x2: POSEDGE:** Positive edge - A clock is output on a 0 to 1 transition on the enable input **0x3: LEVEL:** Level sensitive - A clock is output when the enable is high.
1 : 0	CLKIN_EN_SEL	Select one of four choices for clock enable Default Value: 0 **0x0: PIN_RC:** pin_rc - port pin multiplexer output **0x1: DSI_RC_0:** dsi_rc[0] - dsi_xx_out_p[4]

(continued)

0x2: DSI_RC_1:
dsi_rc[1] - dsi_xx_out_p[5]

0x3: DSI_RC_2:
dsi_rc{1} - dsi_xx_out_p[6]

22.1.2 UDB_PA0_CFG1

PA Data Out Clock Control Register

Address: 0x400F5001

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW	RW	RW		RW	
HW Access	R		R	R	R		R	
Name	NC [7:6]		CLKOUT_INV	CLKOUT_EN_INV	CLKOUT_EN_MODE [3:2]		CLKOUT_EN_SEL [1:0]	

Bits	Name	Description
7 : 6	NC	Spare register bits Default Value: 0
5	CLKOUT_INV	Determines whether the selected clock is inverted or not. Default Value: 0 **0x0: NOINV:** Not Inverted **0x1: INV:** Inverted
4	CLKOUT_EN_INV	Determines whether the selected enable is inverted or not. Default Value: 0 **0x0: NOINV:** Not Inverted **0x1: INV:** Inverted
3 : 2	CLKOUT_EN_MODE	Select one of four operating modes Default Value: 0 **0x0: OFF:** Always off **0x1: ON:** Always on **0x2: POSEDGE:** Positive edge - A clock is output on a 0 to 1 transition on the enable input **0x3: LEVEL:** Level sensitive - A clock is output when the enable is high.
1 : 0	CLKOUT_EN_SEL	Select one of four choices for clock enable Default Value: 0 **0x0: PIN_RC:** pin_rc - port pin multiplexer output **0x1: DSI_RC_0:** dsi_rc[0] - dsi_xx_out_p[4]

(continued)

0x2: DSI_RC_1:
dsi_rc[1] - dsi_xx_out_p[5]

0x3: DSI_RC_2:
dsi_rc{1} - dsi_xx_out_p[6]

22.1.3 UDB_PA0_CFG2

PA Clock Select Register

Address: 0x400F5002

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	CLKOUT_SEL [7:4]				CLKIN_SEL [3:0]			

Bits	Name	Description
7 : 4	CLKOUT_SEL	Select one of four choices for clock enable Default Value: 0 **0x0: GCLK0:** gclk[0] **0x1: GCLK1:** gclk[1] **0x2: GCLK2:** gclk[2] **0x3: GCLK3:** gclk[3] **0x4: GCLK4:** gclk[4] **0x5: GCLK5:** gclk[5] **0x6: GCLK6:** gclk[6] **0x7: GCLK7:** gclk[7] **0x9: BUS_CLK_APP:** bus_clk_app **0xc: PIN_RC:** pin_rc - port pin multiplexer output **0xd: DSI_RC_0:** dsi_rc[0] - dsi_xx_out_p[4] **0xe: DSI_RC_1:** dsi_rc[1] - dsi_xx_out_p[5] **0xf: DSI_RC_2:** dsi_rc{1} - dsi_xx_out_p[6]
3 : 0	CLKIN_SEL	Select one of four choices for clock enable Default Value: 0 **0x0: GCLK0:** gclk[0]

(continued)

0x1: GCLK1:
gclk[1]

0x2: GCLK2:
gclk[2]

0x3: GCLK3:
gclk[3]

0x4: GCLK4:
gclk[4]

0x5: GCLK5:
gclk[5]

0x6: GCLK6:
gclk[6]

0x7: GCLK7:
gclk[7]

0x9: BUS_CLK_APP:
bus_clk_app

0xc: PIN_RC:
pin_rc - port pin multiplexer output

0xd: DSI_RC_0:
dsi_rc[0] - dsi_xx_out_p[4]

0xe: DSI_RC_1:
dsi_rc[1] - dsi_xx_out_p[5]

0xf: DSI_RC_2:
dsi_rc{1} - dsi_xx_out_p[6]

22.1.4 UDB_PA0_CFG3

PA Reset Select Register

Address: 0x400F5003

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW		RW	RW	RW	
HW Access	R	R	R		R	R	R	
Name	NC7	RES_OUT_INV	RES_OUT_SEL [5:4]		NC0	RES_IN_INV	RES_IN_SEL [1:0]	

Bits	Name	Description
7	NC7	Spare register bit Default Value: 0
6	RES_OUT_INV	Select the polarity of the reset control. Default Value: 0 **0x0: NOINV:** Not Inverted **0x1: INV:** Inverted
5 : 4	RES_OUT_SEL	Select one of four inputs to serve as the reset control to the block. Default Value: 0 **0x0: PIN_RC:** pin_rc - port pin multiplexer output **0x1: DSI_RC_0:** dsi_rc[0] - dsi_xx_out_p[4] **0x2: DSI_RC_1:** dsi_rc[1] - dsi_xx_out_p[5] **0x3: DSI_RC_2:** dsi_rc{1} - dsi_xx_out_p[6]
3	NC0	Spare register bit Default Value: 0
2	RES_IN_INV	Select the polarity of the reset control. Default Value: 0 **0x0: NOINV:** Not Inverted **0x1: INV:** Inverted
1 : 0	RES_IN_SEL	Select one of four inputs to serve as the reset control to the block. Default Value: 0 **0x0: PIN_RC:** pin_rc - port pin multiplexer output

(continued)

0x1: DSI_RC_0:
dsi_rc[0] - dsi_xx_out_p[4]

0x2: DSI_RC_1:
dsi_rc[1] - dsi_xx_out_p[5]

0x3: DSI_RC_2:
dsi_rc{1} - dsi_xx_out_p[6]

22.1.5 UDB_PA0_CFG4

PA Reset Enable Register

Address: 0x400F5004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	RW
HW Access	R					R	R	R
Name	NC7654 [7:3]					RES_OE_EN	RES_OUT_EN	RES_IN_EN

Bits	Name	Description
7 : 3	NC7654	Spare register bits Default Value: 0
2	RES_OE_EN	Enable the selected reset Default Value: 0 **0x0: DISABLE:** Reset Disabled **0x1: ENABLE:** Reset Enabled
1	RES_OUT_EN	Enable the selected reset Default Value: 0 **0x0: DISABLE:** Reset Disabled **0x1: ENABLE:** Reset Enabled
0	RES_IN_EN	Enable the selected reset Default Value: 0 **0x0: DISABLE:** Reset Disabled **0x1: ENABLE:** Reset Enabled

22.1.6 UDB_PA0_CFG5

PA Reset Pin Select Register

Address: 0x400F5005

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		RW
HW Access	R					None		R
Name	NC7654 [7:3]					None [2:1]		PIN_SEL

Bits	Name	Description
7 : 3	NC7654	Spare register bits Default Value: 0
0	PIN_SEL	Select port input to route to reset multiplexer (dsi_xx_input_p[7:0]) Default Value: 0 **0x0: PIN0:** dsi_from_port_pin[0] **0x1: PIN1:** dsi_from_port_pin[1] **0x2: PIN2:** dsi_from_port_pin[2] **0x3: PIN3:** dsi_from_port_pin[3] **0x4: PIN4:** dsi_from_port_pin[4] **0x5: PIN5:** dsi_from_port_pin[5] **0x6: PIN6:** dsi_from_port_pin[6] **0x7: PIN7:** dsi_from_port_pin[7]

22.1.7 UDB_PA0_CFG6

PA Input Data Sync Control Register - Low

Address: 0x400F5006

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	IN_SYNC3 [7:6]		IN_SYNC2 [5:4]		IN_SYNC1 [3:2]		IN_SYNC0 [1:0]	

Bits	Name	Description
7 : 6	IN_SYNC3	Synchronization selection for PA input 3 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: DOUBLESYNC:** double sync **0x3: RSVD:** reserved
5 : 4	IN_SYNC2	Synchronization selection for PA input 2 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: DOUBLESYNC:** double sync **0x3: RSVD:** reserved
3 : 2	IN_SYNC1	Synchronization selection for PA input 1 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: DOUBLESYNC:** double sync **0x3: RSVD:** reserved
1 : 0	IN_SYNC0	Synchronization selection for PA input 0 Default Value: 0

(continued)

0x0: TRANSPARENT:
transparent

0x1: SINGLESYNC:
single sync

0x2: DOUBLESYNC:
double sync

0x3: RSVD:
reserved

22.1.8 UDB_PA0_CFG7

PA Input Data Sync Control Register - High

Address: 0x400F5007

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	IN_SYNC7 [7:6]		IN_SYNC6 [5:4]		IN_SYNC5 [3:2]		IN_SYNC4 [1:0]	

Bits	Name	Description
7 : 6	IN_SYNC7	Synchronization selection for PA input 7 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: DOUBLESYNC:** double sync **0x3: RSVD:** reserved
5 : 4	IN_SYNC6	Synchronization selection for PA input 6 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: DOUBLESYNC:** double sync **0x3: RSVD:** reserved
3 : 2	IN_SYNC5	Synchronization selection for PA input 5 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: DOUBLESYNC:** double sync **0x3: RSVD:** reserved
1 : 0	IN_SYNC4	Synchronization selection for PA input 4 Default Value: 0

(continued)

0x0: TRANSPARENT:
transparent

0x1: SINGLESYNC:
single sync

0x2: DOUBLESYNC:
double sync

0x3: RSVD:
reserved

22.1.9 UDB_PA0_CFG8

PA Output Data Sync Control Register - Low

Address: 0x400F5008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	OUT_SYNC3 [7:6]		OUT_SYNC2 [5:4]		OUT_SYNC1 [3:2]		OUT_SYNC0 [1:0]	

Bits	Name	Description
7 : 6	OUT_SYNC3	Synchronization selection for PA output 3 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: CLOCK:** clock **0x3: CLOCKINV:** clock inverted
5 : 4	OUT_SYNC2	Synchronization selection for PA output 2 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: CLOCK:** clock **0x3: CLOCKINV:** clock inverted
3 : 2	OUT_SYNC1	Synchronization selection for PA output 1 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: CLOCK:** clock **0x3: CLOCKINV:** clock inverted
1 : 0	OUT_SYNC0	Synchronization selection for PA output 0 Default Value: 0

(continued)

0x0: TRANSPARENT:
transparent

0x1: SINGLESYNC:
single sync

0x2: CLOCK:
clock

0x3: CLOCKINV:
clock inverted

22.1.10 UDB_PA0_CFG9

PA Output Data Sync Control Register - High

Address: 0x400F5009

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	OUT_SYNC7 [7:6]		OUT_SYNC6 [5:4]		OUT_SYNC5 [3:2]		OUT_SYNC4 [1:0]	

Bits	Name	Description
7 : 6	OUT_SYNC7	Synchronization selection for PA output 7 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: CLOCK:** clock **0x3: CLOCKINV:** clock inverted
5 : 4	OUT_SYNC6	Synchronization selection for PA output 6 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: CLOCK:** clock **0x3: CLOCKINV:** clock inverted
3 : 2	OUT_SYNC5	Synchronization selection for PA output 5 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: CLOCK:** clock **0x3: CLOCKINV:** clock inverted
1 : 0	OUT_SYNC4	Synchronization selection for PA output 4 Default Value: 0

(continued)

0x0: TRANSPARENT:
transparent

0x1: SINGLESYNC:
single sync

0x2: CLOCK:
clock

0x3: CLOCKINV:
clock inverted

22.1.11 UDB_PA0_CFG10

PA Output Data Select Register - Low

Address: 0x400F500A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	DATA_SEL3 [7:6]		DATA_SEL2 [5:4]		DATA_SEL1 [3:2]		DATA_SEL0 [1:0]	

Bits	Name	Description
7 : 6	DATA_SEL3	Data selection for PA output 3 Default Value: 0 **0x0: DSI_OUTPUT0:** dsi output 0 **0x1: DSI_OUTPUT1:** dsi output 1 **0x2: DSI_OUTPUT2:** dsi output 2 **0x3: DSI_OUTPUT3:** dsi output 3
5 : 4	DATA_SEL2	Data selection for PA output 2 Default Value: 0 **0x0: DSI_OUTPUT0:** dsi output 0 **0x1: DSI_OUTPUT1:** dsi output 1 **0x2: DSI_OUTPUT2:** dsi output 2 **0x3: DSI_OUTPUT3:** dsi output 3
3 : 2	DATA_SEL1	Data selection for PA output 1 Default Value: 0 **0x0: DSI_OUTPUT0:** dsi output 0 **0x1: DSI_OUTPUT1:** dsi output 1 **0x2: DSI_OUTPUT2:** dsi output 2 **0x3: DSI_OUTPUT3:** dsi output 3
1 : 0	DATA_SEL0	Data selection for PA output 0 Default Value: 0

(continued)

0x0: DSI_OUTPUT0:
dsi output 0

0x1: DSI_OUTPUT1:
dsi output 1

0x2: DSI_OUTPUT2:
dsi output 2

0x3: DSI_OUTPUT3:
dsi output 3

22.1.12 UDB_PA0_CFG11

PA Output Data Select Register - High

Address: 0x400F500B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	DATA_SEL7 [7:6]		DATA_SEL6 [5:4]		DATA_SEL5 [3:2]		DATA_SEL4 [1:0]	

Bits	Name	Description
7 : 6	DATA_SEL7	Data selection for PA output 7 Default Value: 0 **0x0: DSI_OUTPUT0:** dsi output 0 **0x1: DSI_OUTPUT1:** dsi output 1 **0x2: DSI_OUTPUT2:** dsi output 2 **0x3: DSI_OUTPUT3:** dsi output 3
5 : 4	DATA_SEL6	Data selection for PA output 6 Default Value: 0 **0x0: DSI_OUTPUT0:** dsi output 0 **0x1: DSI_OUTPUT1:** dsi output 1 **0x2: DSI_OUTPUT2:** dsi output 2 **0x3: DSI_OUTPUT3:** dsi output 3
3 : 2	DATA_SEL5	Data selection for PA output 5 Default Value: 0 **0x0: DSI_OUTPUT0:** dsi output 0 **0x1: DSI_OUTPUT1:** dsi output 1 **0x2: DSI_OUTPUT2:** dsi output 2 **0x3: DSI_OUTPUT3:** dsi output 3
1 : 0	DATA_SEL4	Data selection for PA output 4 Default Value: 0

(continued)

0x0: DSI_OUTPUT0:
dsi output 0

0x1: DSI_OUTPUT1:
dsi output 1

0x2: DSI_OUTPUT2:
dsi output 2

0x3: DSI_OUTPUT3:
dsi output 3

22.1.13 UDB_PA0_CFG12

PA OE Select Register - Low

Address: 0x400F500C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	OE_SEL3 [7:6]		OE_SEL2 [5:4]		OE_SEL1 [3:2]		OE_SEL0 [1:0]	

Bits	Name	Description
7 : 6	OE_SEL3	Data selection for PA oe 3 Default Value: 0 **0x0: DSI_OE_OUT0:** synchronized dsi oe output 0 **0x1: DSI_OE_OUT1:** synchronized dsi oe output 1 **0x2: DSI_OE_OUT2:** synchronized dsi oe output 2 **0x3: DSI_OE_OUT3:** synchronized dsi oe output 3
5 : 4	OE_SEL2	Data selection for PA oe 2 Default Value: 0 **0x0: DSI_OE_OUT0:** synchronized dsi oe output 0 **0x1: DSI_OE_OUT1:** synchronized dsi oe output 1 **0x2: DSI_OE_OUT2:** synchronized dsi oe output 2 **0x3: DSI_OE_OUT3:** synchronized dsi oe output 3
3 : 2	OE_SEL1	Data selection for PA oe 1 Default Value: 0 **0x0: DSI_OE_OUT0:** synchronized dsi oe output 0 **0x1: DSI_OE_OUT1:** synchronized dsi oe output 1 **0x2: DSI_OE_OUT2:** synchronized dsi oe output 2 **0x3: DSI_OE_OUT3:** synchronized dsi oe output 3
1 : 0	OE_SEL0	Data selection for PA oe 0 Default Value: 0

(continued)

0x0: DSI_OE_OUT0:
synchronized dsi oe output 0

0x1: DSI_OE_OUT1:
synchronized dsi oe output 1

0x2: DSI_OE_OUT2:
synchronized dsi oe output 2

0x3: DSI_OE_OUT3:
synchronized dsi oe output 3

22.1.14 UDB_PA0_CFG13

PA OE Select Register - High

Address: 0x400F500D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	OE_SEL7 [7:6]		OE_SEL6 [5:4]		OE_SEL5 [3:2]		OE_SEL4 [1:0]	

Bits	Name	Description
7 : 6	OE_SEL7	Data selection for PA oe 7 Default Value: 0 **0x0: DSI_OE_OUT0:** synchronized dsi oe output 0 **0x1: DSI_OE_OUT1:** synchronized dsi oe output 1 **0x2: DSI_OE_OUT2:** synchronized dsi oe output 2 **0x3: DSI_OE_OUT3:** synchronized dsi oe output 3
5 : 4	OE_SEL6	Data selection for PA oe 6 Default Value: 0 **0x0: DSI_OE_OUT0:** synchronized dsi oe output 0 **0x1: DSI_OE_OUT1:** synchronized dsi oe output 1 **0x2: DSI_OE_OUT2:** synchronized dsi oe output 2 **0x3: DSI_OE_OUT3:** synchronized dsi oe output 3
3 : 2	OE_SEL5	Data selection for PA oe 5 Default Value: 0 **0x0: DSI_OE_OUT0:** synchronized dsi oe output 0 **0x1: DSI_OE_OUT1:** synchronized dsi oe output 1 **0x2: DSI_OE_OUT2:** synchronized dsi oe output 2 **0x3: DSI_OE_OUT3:** synchronized dsi oe output 3
1 : 0	OE_SEL4	Data selection for PA oe 4 Default Value: 0

(continued)

0x0: DSI_OE_OUT0:
synchronized dsi oe output 0

0x1: DSI_OE_OUT1:
synchronized dsi oe output 1

0x2: DSI_OE_OUT2:
synchronized dsi oe output 2

0x3: DSI_OE_OUT3:
synchronized dsi oe output 3

22.1.15 UDB_PA0_CFG14

PA OE Sync Register

Address: 0x400F500E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	OE_SYNC3 [7:6]		OE_SYNC2 [5:4]		OE_SYNC1 [3:2]		OE_SYNC0 [1:0]	

Bits	Name	Description
7 : 6	OE_SYNC3	Synchronization options for dsi_to_oe[3] Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: CONSTANT1:** 1 **0x3: CONSTANT0:** 0
5 : 4	OE_SYNC2	Synchronization options for dsi_to_oe[2] Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: CONSTANT1:** 1 **0x3: CONSTANT0:** 0
3 : 2	OE_SYNC1	Synchronization options for dsi_to_oe[1] Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: CONSTANT1:** 1 **0x3: CONSTANT0:** 0
1 : 0	OE_SYNC0	Synchronization options for dsi_to_oe[0] Default Value: 0

(continued)

0x0: TRANSPARENT:
transparent

0x1: SINGLESYNC:
single sync

0x2: CONSTANT1:
1

0x3: CONSTANT0:
0

22.1.16 UDB_PA1_CFG0

PA Data In Clock Control Register

Address: 0x400F5010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW	RW	RW		RW	
HW Access	R		R	R	R		R	
Name	NC [7:6]		CLKIN_INV	CLKIN_EN_INV	CLKIN_EN_MODE [3:2]		CLKIN_EN_SEL [1:0]	

Bits	Name	Description
7 : 6	NC	Spare register bits Default Value: 0
5	CLKIN_INV	Determines whether the selected clock is inverted or not. Default Value: 0 **0x0: NOINV:** Not Inverted **0x1: INV:** Inverted
4	CLKIN_EN_INV	Determines whether the selected enable is inverted or not. Default Value: 0 **0x0: NOINV:** Not Inverted **0x1: INV:** Inverted
3 : 2	CLKIN_EN_MODE	Select one of four operating modes Default Value: 0 **0x0: OFF:** Always off **0x1: ON:** Always on **0x2: POSEDGE:** Positive edge - A clock is output on a 0 to 1 transition on the enable input **0x3: LEVEL:** Level sensitive - A clock is output when the enable is high.
1 : 0	CLKIN_EN_SEL	Select one of four choices for clock enable Default Value: 0 **0x0: PIN_RC:** pin_rc - port pin multiplexer output **0x1: DSI_RC_0:** dsi_rc[0] - dsi_xx_out_p[4]

(continued)

0x2: DSI_RC_1:
dsi_rc[1] - dsi_xx_out_p[5]

0x3: DSI_RC_2:
dsi_rc{1} - dsi_xx_out_p[6]

22.1.17 UDB_PA1_CFG1

PA Data Out Clock Control Register

Address: 0x400F5011

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW	RW	RW		RW	
HW Access	R		R	R	R		R	
Name	NC [7:6]		CLKOUT_INV	CLKOUT_EN_INV	CLKOUT_EN_MODE [3:2]		CLKOUT_EN_SEL [1:0]	

Bits	Name	Description
7 : 6	NC	Spare register bits Default Value: 0
5	CLKOUT_INV	Determines whether the selected clock is inverted or not. Default Value: 0 **0x0: NOINV:** Not Inverted **0x1: INV:** Inverted
4	CLKOUT_EN_INV	Determines whether the selected enable is inverted or not. Default Value: 0 **0x0: NOINV:** Not Inverted **0x1: INV:** Inverted
3 : 2	CLKOUT_EN_MODE	Select one of four operating modes Default Value: 0 **0x0: OFF:** Always off **0x1: ON:** Always on **0x2: POSEDGE:** Positive edge - A clock is output on a 0 to 1 transition on the enable input **0x3: LEVEL:** Level sensitive - A clock is output when the enable is high.
1 : 0	CLKOUT_EN_SEL	Select one of four choices for clock enable Default Value: 0 **0x0: PIN_RC:** pin_rc - port pin multiplexer output **0x1: DSI_RC_0:** dsi_rc[0] - dsi_xx_out_p[4]

(continued)

0x2: DSI_RC_1:
dsi_rc[1] - dsi_xx_out_p[5]

0x3: DSI_RC_2:
dsi_rc{1} - dsi_xx_out_p[6]

22.1.18 UDB_PA1_CFG2

PA Clock Select Register

Address: 0x400F5012

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	CLKOUT_SEL [7:4]				CLKIN_SEL [3:0]			

Bits	Name	Description
7 : 4	CLKOUT_SEL	Select one of four choices for clock enable Default Value: 0 **0x0: GCLK0:** gclk[0] **0x1: GCLK1:** gclk[1] **0x2: GCLK2:** gclk[2] **0x3: GCLK3:** gclk[3] **0x4: GCLK4:** gclk[4] **0x5: GCLK5:** gclk[5] **0x6: GCLK6:** gclk[6] **0x7: GCLK7:** gclk[7] **0x9: BUS_CLK_APP:** bus_clk_app **0xc: PIN_RC:** pin_rc - port pin multiplexer output **0xd: DSI_RC_0:** dsi_rc[0] - dsi_xx_out_p[4] **0xe: DSI_RC_1:** dsi_rc[1] - dsi_xx_out_p[5] **0xf: DSI_RC_2:** dsi_rc{1} - dsi_xx_out_p[6]
3 : 0	CLKIN_SEL	Select one of four choices for clock enable Default Value: 0 **0x0: GCLK0:** gclk[0]

(continued)

0x1: GCLK1:
gclk[1]

0x2: GCLK2:
gclk[2]

0x3: GCLK3:
gclk[3]

0x4: GCLK4:
gclk[4]

0x5: GCLK5:
gclk[5]

0x6: GCLK6:
gclk[6]

0x7: GCLK7:
gclk[7]

0x9: BUS_CLK_APP:
bus_clk_app

0xc: PIN_RC:
pin_rc - port pin multiplexer output

0xd: DSI_RC_0:
dsi_rc[0] - dsi_xx_out_p[4]

0xe: DSI_RC_1:
dsi_rc[1] - dsi_xx_out_p[5]

0xf: DSI_RC_2:
dsi_rc{1} - dsi_xx_out_p[6]

22.1.19 UDB_PA1_CFG3

PA Reset Select Register

Address: 0x400F5013

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW		RW	RW	RW	
HW Access	R	R	R		R	R	R	
Name	NC7	RES_OUT_INV	RES_OUT_SEL [5:4]		NC0	RES_IN_INV	RES_IN_SEL [1:0]	

Bits	Name	Description
7	NC7	Spare register bit Default Value: 0
6	RES_OUT_INV	Select the polarity of the reset control. Default Value: 0 **0x0: NOINV:** Not Inverted **0x1: INV:** Inverted
5 : 4	RES_OUT_SEL	Select one of four inputs to serve as the reset control to the block. Default Value: 0 **0x0: PIN_RC:** pin_rc - port pin multiplexer output **0x1: DSI_RC_0:** dsi_rc[0] - dsi_xx_out_p[4] **0x2: DSI_RC_1:** dsi_rc[1] - dsi_xx_out_p[5] **0x3: DSI_RC_2:** dsi_rc{1} - dsi_xx_out_p[6]
3	NC0	Spare register bit Default Value: 0
2	RES_IN_INV	Select the polarity of the reset control. Default Value: 0 **0x0: NOINV:** Not Inverted **0x1: INV:** Inverted
1 : 0	RES_IN_SEL	Select one of four inputs to serve as the reset control to the block. Default Value: 0 **0x0: PIN_RC:** pin_rc - port pin multiplexer output

(continued)

0x1: DSI_RC_0:
dsi_rc[0] - dsi_xx_out_p[4]

0x2: DSI_RC_1:
dsi_rc[1] - dsi_xx_out_p[5]

0x3: DSI_RC_2:
dsi_rc{1} - dsi_xx_out_p[6]

22.1.20 UDB_PA1_CFG4

PA Reset Enable Register

Address: 0x400F5014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	RW
HW Access	R					R	R	R
Name	NC7654 [7:3]					RES_OE_EN	RES_OUT_EN	RES_IN_EN

Bits	Name	Description
7 : 3	NC7654	Spare register bits Default Value: 0
2	RES_OE_EN	Enable the selected reset Default Value: 0 **0x0: DISABLE:** Reset Disabled **0x1: ENABLE:** Reset Enabled
1	RES_OUT_EN	Enable the selected reset Default Value: 0 **0x0: DISABLE:** Reset Disabled **0x1: ENABLE:** Reset Enabled
0	RES_IN_EN	Enable the selected reset Default Value: 0 **0x0: DISABLE:** Reset Disabled **0x1: ENABLE:** Reset Enabled

22.1.21 UDB_PA1_CFG5

PA Reset Pin Select Register

Address: 0x400F5015

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		RW
HW Access	R					None		R
Name	NC7654 [7:3]					None [2:1]		PIN_SEL

Bits	Name	Description
7 : 3	NC7654	Spare register bits Default Value: 0
0	PIN_SEL	Select port input to route to reset multiplexer (dsi_xx_input_p[7:0]) Default Value: 0 **0x0: PIN0:** dsi_from_port_pin[0] **0x1: PIN1:** dsi_from_port_pin[1] **0x2: PIN2:** dsi_from_port_pin[2] **0x3: PIN3:** dsi_from_port_pin[3] **0x4: PIN4:** dsi_from_port_pin[4] **0x5: PIN5:** dsi_from_port_pin[5] **0x6: PIN6:** dsi_from_port_pin[6] **0x7: PIN7:** dsi_from_port_pin[7]

22.1.22 UDB_PA1_CFG6

PA Input Data Sync Control Register - Low

Address: 0x400F5016

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	IN_SYNC3 [7:6]		IN_SYNC2 [5:4]		IN_SYNC1 [3:2]		IN_SYNC0 [1:0]	

Bits	Name	Description
7 : 6	IN_SYNC3	Synchronization selection for PA input 3 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: DOUBLESYNC:** double sync **0x3: RSVD:** reserved
5 : 4	IN_SYNC2	Synchronization selection for PA input 2 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: DOUBLESYNC:** double sync **0x3: RSVD:** reserved
3 : 2	IN_SYNC1	Synchronization selection for PA input 1 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: DOUBLESYNC:** double sync **0x3: RSVD:** reserved
1 : 0	IN_SYNC0	Synchronization selection for PA input 0 Default Value: 0

(continued)

0x0: TRANSPARENT:
transparent

0x1: SINGLESYNC:
single sync

0x2: DOUBLESYNC:
double sync

0x3: RSVD:
reserved

22.1.23 UDB_PA1_CFG7

PA Input Data Sync Control Register - High

Address: 0x400F5017

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	IN_SYNC7 [7:6]		IN_SYNC6 [5:4]		IN_SYNC5 [3:2]		IN_SYNC4 [1:0]	

Bits	Name	Description
7 : 6	IN_SYNC7	Synchronization selection for PA input 7 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: DOUBLESYNC:** double sync **0x3: RSVD:** reserved
5 : 4	IN_SYNC6	Synchronization selection for PA input 6 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: DOUBLESYNC:** double sync **0x3: RSVD:** reserved
3 : 2	IN_SYNC5	Synchronization selection for PA input 5 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: DOUBLESYNC:** double sync **0x3: RSVD:** reserved
1 : 0	IN_SYNC4	Synchronization selection for PA input 4 Default Value: 0

(continued)

0x0: TRANSPARENT:
transparent

0x1: SINGLESYNC:
single sync

0x2: DOUBLESYNC:
double sync

0x3: RSVD:
reserved

22.1.24 UDB_PA1_CFG8

PA Output Data Sync Control Register - Low

Address: 0x400F5018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	OUT_SYNC3 [7:6]		OUT_SYNC2 [5:4]		OUT_SYNC1 [3:2]		OUT_SYNC0 [1:0]	

Bits	Name	Description
7 : 6	OUT_SYNC3	Synchronization selection for PA output 3 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: CLOCK:** clock **0x3: CLOCKINV:** clock inverted
5 : 4	OUT_SYNC2	Synchronization selection for PA output 2 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: CLOCK:** clock **0x3: CLOCKINV:** clock inverted
3 : 2	OUT_SYNC1	Synchronization selection for PA output 1 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: CLOCK:** clock **0x3: CLOCKINV:** clock inverted
1 : 0	OUT_SYNC0	Synchronization selection for PA output 0 Default Value: 0

(continued)

0x0: TRANSPARENT:
transparent

0x1: SINGLESYNC:
single sync

0x2: CLOCK:
clock

0x3: CLOCKINV:
clock inverted

22.1.25 UDB_PA1_CFG9

PA Output Data Sync Control Register - High

Address: 0x400F5019

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	OUT_SYNC7 [7:6]		OUT_SYNC6 [5:4]		OUT_SYNC5 [3:2]		OUT_SYNC4 [1:0]	

Bits	Name	Description
7 : 6	OUT_SYNC7	Synchronization selection for PA output 7 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: CLOCK:** clock **0x3: CLOCKINV:** clock inverted
5 : 4	OUT_SYNC6	Synchronization selection for PA output 6 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: CLOCK:** clock **0x3: CLOCKINV:** clock inverted
3 : 2	OUT_SYNC5	Synchronization selection for PA output 5 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: CLOCK:** clock **0x3: CLOCKINV:** clock inverted
1 : 0	OUT_SYNC4	Synchronization selection for PA output 4 Default Value: 0

(continued)

0x0: TRANSPARENT:
transparent

0x1: SINGLESYNC:
single sync

0x2: CLOCK:
clock

0x3: CLOCKINV:
clock inverted

22.1.26 UDB_PA1_CFG10

PA Output Data Select Register - Low

Address: 0x400F501A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	DATA_SEL3 [7:6]		DATA_SEL2 [5:4]		DATA_SEL1 [3:2]		DATA_SEL0 [1:0]	

Bits	Name	Description
7 : 6	DATA_SEL3	Data selection for PA output 3 Default Value: 0 **0x0: DSI_OUTPUT0:** dsi output 0 **0x1: DSI_OUTPUT1:** dsi output 1 **0x2: DSI_OUTPUT2:** dsi output 2 **0x3: DSI_OUTPUT3:** dsi output 3
5 : 4	DATA_SEL2	Data selection for PA output 2 Default Value: 0 **0x0: DSI_OUTPUT0:** dsi output 0 **0x1: DSI_OUTPUT1:** dsi output 1 **0x2: DSI_OUTPUT2:** dsi output 2 **0x3: DSI_OUTPUT3:** dsi output 3
3 : 2	DATA_SEL1	Data selection for PA output 1 Default Value: 0 **0x0: DSI_OUTPUT0:** dsi output 0 **0x1: DSI_OUTPUT1:** dsi output 1 **0x2: DSI_OUTPUT2:** dsi output 2 **0x3: DSI_OUTPUT3:** dsi output 3
1 : 0	DATA_SEL0	Data selection for PA output 0 Default Value: 0

(continued)

0x0: DSI_OUTPUT0:
dsi output 0

0x1: DSI_OUTPUT1:
dsi output 1

0x2: DSI_OUTPUT2:
dsi output 2

0x3: DSI_OUTPUT3:
dsi output 3

22.1.27 UDB_PA1_CFG11

PA Output Data Select Register - High

Address: 0x400F501B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	DATA_SEL7 [7:6]		DATA_SEL6 [5:4]		DATA_SEL5 [3:2]		DATA_SEL4 [1:0]	

Bits	Name	Description
7 : 6	DATA_SEL7	Data selection for PA output 7 Default Value: 0 **0x0: DSI_OUTPUT0:** dsi output 0 **0x1: DSI_OUTPUT1:** dsi output 1 **0x2: DSI_OUTPUT2:** dsi output 2 **0x3: DSI_OUTPUT3:** dsi output 3
5 : 4	DATA_SEL6	Data selection for PA output 6 Default Value: 0 **0x0: DSI_OUTPUT0:** dsi output 0 **0x1: DSI_OUTPUT1:** dsi output 1 **0x2: DSI_OUTPUT2:** dsi output 2 **0x3: DSI_OUTPUT3:** dsi output 3
3 : 2	DATA_SEL5	Data selection for PA output 5 Default Value: 0 **0x0: DSI_OUTPUT0:** dsi output 0 **0x1: DSI_OUTPUT1:** dsi output 1 **0x2: DSI_OUTPUT2:** dsi output 2 **0x3: DSI_OUTPUT3:** dsi output 3
1 : 0	DATA_SEL4	Data selection for PA output 4 Default Value: 0

(continued)

0x0: DSI_OUTPUT0:
dsi output 0

0x1: DSI_OUTPUT1:
dsi output 1

0x2: DSI_OUTPUT2:
dsi output 2

0x3: DSI_OUTPUT3:
dsi output 3

22.1.28 UDB_PA1_CFG12

PA OE Select Register - Low

Address: 0x400F501C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	OE_SEL3 [7:6]		OE_SEL2 [5:4]		OE_SEL1 [3:2]		OE_SEL0 [1:0]	

Bits	Name	Description
7 : 6	OE_SEL3	Data selection for PA oe 3 Default Value: 0 **0x0: DSI_OE_OUT0:** synchronized dsi oe output 0 **0x1: DSI_OE_OUT1:** synchronized dsi oe output 1 **0x2: DSI_OE_OUT2:** synchronized dsi oe output 2 **0x3: DSI_OE_OUT3:** synchronized dsi oe output 3
5 : 4	OE_SEL2	Data selection for PA oe 2 Default Value: 0 **0x0: DSI_OE_OUT0:** synchronized dsi oe output 0 **0x1: DSI_OE_OUT1:** synchronized dsi oe output 1 **0x2: DSI_OE_OUT2:** synchronized dsi oe output 2 **0x3: DSI_OE_OUT3:** synchronized dsi oe output 3
3 : 2	OE_SEL1	Data selection for PA oe 1 Default Value: 0 **0x0: DSI_OE_OUT0:** synchronized dsi oe output 0 **0x1: DSI_OE_OUT1:** synchronized dsi oe output 1 **0x2: DSI_OE_OUT2:** synchronized dsi oe output 2 **0x3: DSI_OE_OUT3:** synchronized dsi oe output 3
1 : 0	OE_SEL0	Data selection for PA oe 0 Default Value: 0

(continued)

0x0: DSI_OE_OUT0:
synchronized dsi oe output 0

0x1: DSI_OE_OUT1:
synchronized dsi oe output 1

0x2: DSI_OE_OUT2:
synchronized dsi oe output 2

0x3: DSI_OE_OUT3:
synchronized dsi oe output 3

22.1.29 UDB_PA1_CFG13

PA OE Select Register - High

Address: 0x400F501D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	OE_SEL7 [7:6]		OE_SEL6 [5:4]		OE_SEL5 [3:2]		OE_SEL4 [1:0]	

Bits	Name	Description
7 : 6	OE_SEL7	Data selection for PA oe 7 Default Value: 0 **0x0: DSI_OE_OUT0:** synchronized dsi oe output 0 **0x1: DSI_OE_OUT1:** synchronized dsi oe output 1 **0x2: DSI_OE_OUT2:** synchronized dsi oe output 2 **0x3: DSI_OE_OUT3:** synchronized dsi oe output 3
5 : 4	OE_SEL6	Data selection for PA oe 6 Default Value: 0 **0x0: DSI_OE_OUT0:** synchronized dsi oe output 0 **0x1: DSI_OE_OUT1:** synchronized dsi oe output 1 **0x2: DSI_OE_OUT2:** synchronized dsi oe output 2 **0x3: DSI_OE_OUT3:** synchronized dsi oe output 3
3 : 2	OE_SEL5	Data selection for PA oe 5 Default Value: 0 **0x0: DSI_OE_OUT0:** synchronized dsi oe output 0 **0x1: DSI_OE_OUT1:** synchronized dsi oe output 1 **0x2: DSI_OE_OUT2:** synchronized dsi oe output 2 **0x3: DSI_OE_OUT3:** synchronized dsi oe output 3
1 : 0	OE_SEL4	Data selection for PA oe 4 Default Value: 0

(continued)

0x0: DSI_OE_OUT0:
synchronized dsi oe output 0

0x1: DSI_OE_OUT1:
synchronized dsi oe output 1

0x2: DSI_OE_OUT2:
synchronized dsi oe output 2

0x3: DSI_OE_OUT3:
synchronized dsi oe output 3

22.1.30 UDB_PA1_CFG14

PA OE Sync Register

Address: 0x400F501E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	OE_SYNC3 [7:6]		OE_SYNC2 [5:4]		OE_SYNC1 [3:2]		OE_SYNC0 [1:0]	

Bits	Name	Description
7 : 6	OE_SYNC3	Synchronization options for dsi_to_oe[3] Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: CONSTANT1:** 1 **0x3: CONSTANT0:** 0
5 : 4	OE_SYNC2	Synchronization options for dsi_to_oe[2] Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: CONSTANT1:** 1 **0x3: CONSTANT0:** 0
3 : 2	OE_SYNC1	Synchronization options for dsi_to_oe[1] Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: CONSTANT1:** 1 **0x3: CONSTANT0:** 0
1 : 0	OE_SYNC0	Synchronization options for dsi_to_oe[0] Default Value: 0

(continued)

0x0: TRANSPARENT:
transparent

0x1: SINGLESYNC:
single sync

0x2: CONSTANT1:
1

0x3: CONSTANT0:
0

22.1.31 UDB_PA2_CFG0

PA Data In Clock Control Register

Address: 0x400F5020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW	RW	RW		RW	
HW Access	R		R	R	R		R	
Name	NC [7:6]		CLKIN_INV	CLKIN_EN_INV	CLKIN_EN_MODE [3:2]		CLKIN_EN_SEL [1:0]	

Bits	Name	Description
7 : 6	NC	Spare register bits Default Value: 0
5	CLKIN_INV	Determines whether the selected clock is inverted or not. Default Value: 0 **0x0: NOINV:** Not Inverted **0x1: INV:** Inverted
4	CLKIN_EN_INV	Determines whether the selected enable is inverted or not. Default Value: 0 **0x0: NOINV:** Not Inverted **0x1: INV:** Inverted
3 : 2	CLKIN_EN_MODE	Select one of four operating modes Default Value: 0 **0x0: OFF:** Always off **0x1: ON:** Always on **0x2: POSEDGE:** Positive edge - A clock is output on a 0 to 1 transition on the enable input **0x3: LEVEL:** Level sensitive - A clock is output when the enable is high.
1 : 0	CLKIN_EN_SEL	Select one of four choices for clock enable Default Value: 0 **0x0: PIN_RC:** pin_rc - port pin multiplexer output **0x1: DSI_RC_0:** dsi_rc[0] - dsi_xx_out_p[4]

(continued)

0x2: DSI_RC_1:
dsi_rc[1] - dsi_xx_out_p[5]

0x3: DSI_RC_2:
dsi_rc{1} - dsi_xx_out_p[6]

22.1.32 UDB_PA2_CFG1

PA Data Out Clock Control Register

Address: 0x400F5021

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW	RW	RW		RW	
HW Access	R		R	R	R		R	
Name	NC [7:6]		CLKOUT_INV	CLKOUT_EN_INV	CLKOUT_EN_MODE [3:2]		CLKOUT_EN_SEL [1:0]	

Bits	Name	Description
7 : 6	NC	Spare register bits Default Value: 0
5	CLKOUT_INV	Determines whether the selected clock is inverted or not. Default Value: 0 **0x0: NOINV:** Not Inverted **0x1: INV:** Inverted
4	CLKOUT_EN_INV	Determines whether the selected enable is inverted or not. Default Value: 0 **0x0: NOINV:** Not Inverted **0x1: INV:** Inverted
3 : 2	CLKOUT_EN_MODE	Select one of four operating modes Default Value: 0 **0x0: OFF:** Always off **0x1: ON:** Always on **0x2: POSEDGE:** Positive edge - A clock is output on a 0 to 1 transition on the enable input **0x3: LEVEL:** Level sensitive - A clock is output when the enable is high.
1 : 0	CLKOUT_EN_SEL	Select one of four choices for clock enable Default Value: 0 **0x0: PIN_RC:** pin_rc - port pin multiplexer output **0x1: DSI_RC_0:** dsi_rc[0] - dsi_xx_out_p[4]

(continued)

0x2: DSI_RC_1:
dsi_rc[1] - dsi_xx_out_p[5]

0x3: DSI_RC_2:
dsi_rc{1} - dsi_xx_out_p[6]

22.1.33 UDB_PA2_CFG2

PA Clock Select Register

Address: 0x400F5022

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	CLKOUT_SEL [7:4]				CLKIN_SEL [3:0]			

Bits	Name	Description
7 : 4	CLKOUT_SEL	Select one of four choices for clock enable Default Value: 0 **0x0: GCLK0:** gclk[0] **0x1: GCLK1:** gclk[1] **0x2: GCLK2:** gclk[2] **0x3: GCLK3:** gclk[3] **0x4: GCLK4:** gclk[4] **0x5: GCLK5:** gclk[5] **0x6: GCLK6:** gclk[6] **0x7: GCLK7:** gclk[7] **0x9: BUS_CLK_APP:** bus_clk_app **0xc: PIN_RC:** pin_rc - port pin multiplexer output **0xd: DSI_RC_0:** dsi_rc[0] - dsi_xx_out_p[4] **0xe: DSI_RC_1:** dsi_rc[1] - dsi_xx_out_p[5] **0xf: DSI_RC_2:** dsi_rc{1} - dsi_xx_out_p[6]
3 : 0	CLKIN_SEL	Select one of four choices for clock enable Default Value: 0 **0x0: GCLK0:** gclk[0]

(continued)

0x1: GCLK1:
gclk[1]

0x2: GCLK2:
gclk[2]

0x3: GCLK3:
gclk[3]

0x4: GCLK4:
gclk[4]

0x5: GCLK5:
gclk[5]

0x6: GCLK6:
gclk[6]

0x7: GCLK7:
gclk[7]

0x9: BUS_CLK_APP:
bus_clk_app

0xc: PIN_RC:
pin_rc - port pin multiplexer output

0xd: DSI_RC_0:
dsi_rc[0] - dsi_xx_out_p[4]

0xe: DSI_RC_1:
dsi_rc[1] - dsi_xx_out_p[5]

0xf: DSI_RC_2:
dsi_rc{1} - dsi_xx_out_p[6]

22.1.34 UDB_PA2_CFG3

PA Reset Select Register

Address: 0x400F5023

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW		RW	RW	RW	
HW Access	R	R	R		R	R	R	
Name	NC7	RES_OUT_INV	RES_OUT_SEL [5:4]		NC0	RES_IN_INV	RES_IN_SEL [1:0]	

Bits	Name	Description
7	NC7	Spare register bit Default Value: 0
6	RES_OUT_INV	Select the polarity of the reset control. Default Value: 0 **0x0: NOINV:** Not Inverted **0x1: INV:** Inverted
5 : 4	RES_OUT_SEL	Select one of four inputs to serve as the reset control to the block. Default Value: 0 **0x0: PIN_RC:** pin_rc - port pin multiplexer output **0x1: DSI_RC_0:** dsi_rc[0] - dsi_xx_out_p[4] **0x2: DSI_RC_1:** dsi_rc[1] - dsi_xx_out_p[5] **0x3: DSI_RC_2:** dsi_rc{1} - dsi_xx_out_p[6]
3	NC0	Spare register bit Default Value: 0
2	RES_IN_INV	Select the polarity of the reset control. Default Value: 0 **0x0: NOINV:** Not Inverted **0x1: INV:** Inverted
1 : 0	RES_IN_SEL	Select one of four inputs to serve as the reset control to the block. Default Value: 0 **0x0: PIN_RC:** pin_rc - port pin multiplexer output

(continued)

0x1: DSI_RC_0:
dsi_rc[0] - dsi_xx_out_p[4]

0x2: DSI_RC_1:
dsi_rc[1] - dsi_xx_out_p[5]

0x3: DSI_RC_2:
dsi_rc{1} - dsi_xx_out_p[6]

22.1.35 UDB_PA2_CFG4

PA Reset Enable Register

Address: 0x400F5024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	RW
HW Access	R					R	R	R
Name	NC7654 [7:3]					RES_OE_EN	RES_OUT_EN	RES_IN_EN

Bits	Name	Description
7 : 3	NC7654	Spare register bits Default Value: 0
2	RES_OE_EN	Enable the selected reset Default Value: 0 **0x0: DISABLE:** Reset Disabled **0x1: ENABLE:** Reset Enabled
1	RES_OUT_EN	Enable the selected reset Default Value: 0 **0x0: DISABLE:** Reset Disabled **0x1: ENABLE:** Reset Enabled
0	RES_IN_EN	Enable the selected reset Default Value: 0 **0x0: DISABLE:** Reset Disabled **0x1: ENABLE:** Reset Enabled

22.1.36 UDB_PA2_CFG5

PA Reset Pin Select Register

Address: 0x400F5025

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		RW
HW Access	R					None		R
Name	NC7654 [7:3]					None [2:1]		PIN_SEL

Bits	Name	Description
7 : 3	NC7654	Spare register bits Default Value: 0
0	PIN_SEL	Select port input to route to reset multiplexer (dsi_xx_input_p[7:0]) Default Value: 0 **0x0: PIN0:** dsi_from_port_pin[0] **0x1: PIN1:** dsi_from_port_pin[1] **0x2: PIN2:** dsi_from_port_pin[2] **0x3: PIN3:** dsi_from_port_pin[3] **0x4: PIN4:** dsi_from_port_pin[4] **0x5: PIN5:** dsi_from_port_pin[5] **0x6: PIN6:** dsi_from_port_pin[6] **0x7: PIN7:** dsi_from_port_pin[7]

22.1.37 UDB_PA2_CFG6

PA Input Data Sync Control Register - Low

Address: 0x400F5026

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	IN_SYNC3 [7:6]		IN_SYNC2 [5:4]		IN_SYNC1 [3:2]		IN_SYNC0 [1:0]	

Bits	Name	Description
7 : 6	IN_SYNC3	Synchronization selection for PA input 3 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: DOUBLESYNC:** double sync **0x3: RSVD:** reserved
5 : 4	IN_SYNC2	Synchronization selection for PA input 2 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: DOUBLESYNC:** double sync **0x3: RSVD:** reserved
3 : 2	IN_SYNC1	Synchronization selection for PA input 1 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: DOUBLESYNC:** double sync **0x3: RSVD:** reserved
1 : 0	IN_SYNC0	Synchronization selection for PA input 0 Default Value: 0

(continued)

0x0: TRANSPARENT:
transparent

0x1: SINGLESYNC:
single sync

0x2: DOUBLESYNC:
double sync

0x3: RSVD:
reserved

22.1.38 UDB_PA2_CFG7

PA Input Data Sync Control Register - High

Address: 0x400F5027

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	IN_SYNC7 [7:6]		IN_SYNC6 [5:4]		IN_SYNC5 [3:2]		IN_SYNC4 [1:0]	

Bits	Name	Description
7 : 6	IN_SYNC7	Synchronization selection for PA input 7 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: DOUBLESYNC:** double sync **0x3: RSVD:** reserved
5 : 4	IN_SYNC6	Synchronization selection for PA input 6 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: DOUBLESYNC:** double sync **0x3: RSVD:** reserved
3 : 2	IN_SYNC5	Synchronization selection for PA input 5 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: DOUBLESYNC:** double sync **0x3: RSVD:** reserved
1 : 0	IN_SYNC4	Synchronization selection for PA input 4 Default Value: 0

(continued)

0x0: TRANSPARENT:
transparent

0x1: SINGLESYNC:
single sync

0x2: DOUBLESYNC:
double sync

0x3: RSVD:
reserved

22.1.39 UDB_PA2_CFG8

PA Output Data Sync Control Register - Low

Address: 0x400F5028

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	OUT_SYNC3 [7:6]		OUT_SYNC2 [5:4]		OUT_SYNC1 [3:2]		OUT_SYNC0 [1:0]	

Bits	Name	Description
7 : 6	OUT_SYNC3	Synchronization selection for PA output 3 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: CLOCK:** clock **0x3: CLOCKINV:** clock inverted
5 : 4	OUT_SYNC2	Synchronization selection for PA output 2 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: CLOCK:** clock **0x3: CLOCKINV:** clock inverted
3 : 2	OUT_SYNC1	Synchronization selection for PA output 1 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: CLOCK:** clock **0x3: CLOCKINV:** clock inverted
1 : 0	OUT_SYNC0	Synchronization selection for PA output 0 Default Value: 0

(continued)

0x0: TRANSPARENT:
transparent

0x1: SINGLESYNC:
single sync

0x2: CLOCK:
clock

0x3: CLOCKINV:
clock inverted

22.1.40 UDB_PA2_CFG9

PA Output Data Sync Control Register - High

Address: 0x400F5029

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	OUT_SYNC7 [7:6]		OUT_SYNC6 [5:4]		OUT_SYNC5 [3:2]		OUT_SYNC4 [1:0]	

Bits	Name	Description
7 : 6	OUT_SYNC7	Synchronization selection for PA output 7 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: CLOCK:** clock **0x3: CLOCKINV:** clock inverted
5 : 4	OUT_SYNC6	Synchronization selection for PA output 6 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: CLOCK:** clock **0x3: CLOCKINV:** clock inverted
3 : 2	OUT_SYNC5	Synchronization selection for PA output 5 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: CLOCK:** clock **0x3: CLOCKINV:** clock inverted
1 : 0	OUT_SYNC4	Synchronization selection for PA output 4 Default Value: 0

(continued)

0x0: TRANSPARENT:
transparent

0x1: SINGLESYNC:
single sync

0x2: CLOCK:
clock

0x3: CLOCKINV:
clock inverted

22.1.41 UDB_PA2_CFG10

PA Output Data Select Register - Low

Address: 0x400F502A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	DATA_SEL3 [7:6]		DATA_SEL2 [5:4]		DATA_SEL1 [3:2]		DATA_SEL0 [1:0]	

Bits	Name	Description
7 : 6	DATA_SEL3	Data selection for PA output 3 Default Value: 0 **0x0: DSI_OUTPUT0:** dsi output 0 **0x1: DSI_OUTPUT1:** dsi output 1 **0x2: DSI_OUTPUT2:** dsi output 2 **0x3: DSI_OUTPUT3:** dsi output 3
5 : 4	DATA_SEL2	Data selection for PA output 2 Default Value: 0 **0x0: DSI_OUTPUT0:** dsi output 0 **0x1: DSI_OUTPUT1:** dsi output 1 **0x2: DSI_OUTPUT2:** dsi output 2 **0x3: DSI_OUTPUT3:** dsi output 3
3 : 2	DATA_SEL1	Data selection for PA output 1 Default Value: 0 **0x0: DSI_OUTPUT0:** dsi output 0 **0x1: DSI_OUTPUT1:** dsi output 1 **0x2: DSI_OUTPUT2:** dsi output 2 **0x3: DSI_OUTPUT3:** dsi output 3
1 : 0	DATA_SEL0	Data selection for PA output 0 Default Value: 0

(continued)

0x0: DSI_OUTPUT0:
dsi output 0

0x1: DSI_OUTPUT1:
dsi output 1

0x2: DSI_OUTPUT2:
dsi output 2

0x3: DSI_OUTPUT3:
dsi output 3

22.1.42 UDB_PA2_CFG11

PA Output Data Select Register - High

Address: 0x400F502B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	DATA_SEL7 [7:6]		DATA_SEL6 [5:4]		DATA_SEL5 [3:2]		DATA_SEL4 [1:0]	

Bits	Name	Description
7 : 6	DATA_SEL7	Data selection for PA output 7 Default Value: 0 **0x0: DSI_OUTPUT0:** dsi output 0 **0x1: DSI_OUTPUT1:** dsi output 1 **0x2: DSI_OUTPUT2:** dsi output 2 **0x3: DSI_OUTPUT3:** dsi output 3
5 : 4	DATA_SEL6	Data selection for PA output 6 Default Value: 0 **0x0: DSI_OUTPUT0:** dsi output 0 **0x1: DSI_OUTPUT1:** dsi output 1 **0x2: DSI_OUTPUT2:** dsi output 2 **0x3: DSI_OUTPUT3:** dsi output 3
3 : 2	DATA_SEL5	Data selection for PA output 5 Default Value: 0 **0x0: DSI_OUTPUT0:** dsi output 0 **0x1: DSI_OUTPUT1:** dsi output 1 **0x2: DSI_OUTPUT2:** dsi output 2 **0x3: DSI_OUTPUT3:** dsi output 3
1 : 0	DATA_SEL4	Data selection for PA output 4 Default Value: 0

(continued)

0x0: DSI_OUTPUT0:
dsi output 0

0x1: DSI_OUTPUT1:
dsi output 1

0x2: DSI_OUTPUT2:
dsi output 2

0x3: DSI_OUTPUT3:
dsi output 3

22.1.43 UDB_PA2_CFG12

PA OE Select Register - Low

Address: 0x400F502C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	OE_SEL3 [7:6]		OE_SEL2 [5:4]		OE_SEL1 [3:2]		OE_SEL0 [1:0]	

Bits	Name	Description
7 : 6	OE_SEL3	Data selection for PA oe 3 Default Value: 0 **0x0: DSI_OE_OUT0:** synchronized dsi oe output 0 **0x1: DSI_OE_OUT1:** synchronized dsi oe output 1 **0x2: DSI_OE_OUT2:** synchronized dsi oe output 2 **0x3: DSI_OE_OUT3:** synchronized dsi oe output 3
5 : 4	OE_SEL2	Data selection for PA oe 2 Default Value: 0 **0x0: DSI_OE_OUT0:** synchronized dsi oe output 0 **0x1: DSI_OE_OUT1:** synchronized dsi oe output 1 **0x2: DSI_OE_OUT2:** synchronized dsi oe output 2 **0x3: DSI_OE_OUT3:** synchronized dsi oe output 3
3 : 2	OE_SEL1	Data selection for PA oe 1 Default Value: 0 **0x0: DSI_OE_OUT0:** synchronized dsi oe output 0 **0x1: DSI_OE_OUT1:** synchronized dsi oe output 1 **0x2: DSI_OE_OUT2:** synchronized dsi oe output 2 **0x3: DSI_OE_OUT3:** synchronized dsi oe output 3
1 : 0	OE_SEL0	Data selection for PA oe 0 Default Value: 0

(continued)

0x0: DSI_OE_OUT0:
synchronized dsi oe output 0

0x1: DSI_OE_OUT1:
synchronized dsi oe output 1

0x2: DSI_OE_OUT2:
synchronized dsi oe output 2

0x3: DSI_OE_OUT3:
synchronized dsi oe output 3

22.1.44 UDB_PA2_CFG13

PA OE Select Register - High

Address: 0x400F502D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	OE_SEL7 [7:6]		OE_SEL6 [5:4]		OE_SEL5 [3:2]		OE_SEL4 [1:0]	

Bits	Name	Description
7 : 6	OE_SEL7	Data selection for PA oe 7 Default Value: 0 **0x0: DSI_OE_OUT0:** synchronized dsi oe output 0 **0x1: DSI_OE_OUT1:** synchronized dsi oe output 1 **0x2: DSI_OE_OUT2:** synchronized dsi oe output 2 **0x3: DSI_OE_OUT3:** synchronized dsi oe output 3
5 : 4	OE_SEL6	Data selection for PA oe 6 Default Value: 0 **0x0: DSI_OE_OUT0:** synchronized dsi oe output 0 **0x1: DSI_OE_OUT1:** synchronized dsi oe output 1 **0x2: DSI_OE_OUT2:** synchronized dsi oe output 2 **0x3: DSI_OE_OUT3:** synchronized dsi oe output 3
3 : 2	OE_SEL5	Data selection for PA oe 5 Default Value: 0 **0x0: DSI_OE_OUT0:** synchronized dsi oe output 0 **0x1: DSI_OE_OUT1:** synchronized dsi oe output 1 **0x2: DSI_OE_OUT2:** synchronized dsi oe output 2 **0x3: DSI_OE_OUT3:** synchronized dsi oe output 3
1 : 0	OE_SEL4	Data selection for PA oe 4 Default Value: 0

(continued)

0x0: DSI_OE_OUT0:
synchronized dsi oe output 0

0x1: DSI_OE_OUT1:
synchronized dsi oe output 1

0x2: DSI_OE_OUT2:
synchronized dsi oe output 2

0x3: DSI_OE_OUT3:
synchronized dsi oe output 3

22.1.45 UDB_PA2_CFG14

PA OE Sync Register

Address: 0x400F502E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	OE_SYNC3 [7:6]		OE_SYNC2 [5:4]		OE_SYNC1 [3:2]		OE_SYNC0 [1:0]	

Bits	Name	Description
7 : 6	OE_SYNC3	Synchronization options for dsi_to_oe[3] Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: CONSTANT1:** 1 **0x3: CONSTANT0:** 0
5 : 4	OE_SYNC2	Synchronization options for dsi_to_oe[2] Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: CONSTANT1:** 1 **0x3: CONSTANT0:** 0
3 : 2	OE_SYNC1	Synchronization options for dsi_to_oe[1] Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: CONSTANT1:** 1 **0x3: CONSTANT0:** 0
1 : 0	OE_SYNC0	Synchronization options for dsi_to_oe[0] Default Value: 0

(continued)

0x0: TRANSPARENT:
transparent

0x1: SINGLESYNC:
single sync

0x2: CONSTANT1:
1

0x3: CONSTANT0:
0

22.1.46 UDB_PA3_CFG0

PA Data In Clock Control Register

Address: 0x400F5030

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW	RW	RW		RW	
HW Access	R		R	R	R		R	
Name	NC [7:6]		CLKIN_INV	CLKIN_EN_INV	CLKIN_EN_MODE [3:2]		CLKIN_EN_SEL [1:0]	

Bits	Name	Description
7 : 6	NC	Spare register bits Default Value: 0
5	CLKIN_INV	Determines whether the selected clock is inverted or not. Default Value: 0 **0x0: NOINV:** Not Inverted **0x1: INV:** Inverted
4	CLKIN_EN_INV	Determines whether the selected enable is inverted or not. Default Value: 0 **0x0: NOINV:** Not Inverted **0x1: INV:** Inverted
3 : 2	CLKIN_EN_MODE	Select one of four operating modes Default Value: 0 **0x0: OFF:** Always off **0x1: ON:** Always on **0x2: POSEDGE:** Positive edge - A clock is output on a 0 to 1 transition on the enable input **0x3: LEVEL:** Level sensitive - A clock is output when the enable is high.
1 : 0	CLKIN_EN_SEL	Select one of four choices for clock enable Default Value: 0 **0x0: PIN_RC:** pin_rc - port pin multiplexer output **0x1: DSI_RC_0:** dsi_rc[0] - dsi_xx_out_p[4]

(continued)

0x2: DSI_RC_1:
dsi_rc[1] - dsi_xx_out_p[5]

0x3: DSI_RC_2:
dsi_rc{1} - dsi_xx_out_p[6]

22.1.47 UDB_PA3_CFG1

PA Data Out Clock Control Register

Address: 0x400F5031

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW	RW	RW		RW	
HW Access	R		R	R	R		R	
Name	NC [7:6]		CLKOUT_INV	CLKOUT_EN_INV	CLKOUT_EN_MODE [3:2]		CLKOUT_EN_SEL [1:0]	

Bits	Name	Description
7 : 6	NC	Spare register bits Default Value: 0
5	CLKOUT_INV	Determines whether the selected clock is inverted or not. Default Value: 0 **0x0: NOINV:** Not Inverted **0x1: INV:** Inverted
4	CLKOUT_EN_INV	Determines whether the selected enable is inverted or not. Default Value: 0 **0x0: NOINV:** Not Inverted **0x1: INV:** Inverted
3 : 2	CLKOUT_EN_MODE	Select one of four operating modes Default Value: 0 **0x0: OFF:** Always off **0x1: ON:** Always on **0x2: POSEDGE:** Positive edge - A clock is output on a 0 to 1 transition on the enable input **0x3: LEVEL:** Level sensitive - A clock is output when the enable is high.
1 : 0	CLKOUT_EN_SEL	Select one of four choices for clock enable Default Value: 0 **0x0: PIN_RC:** pin_rc - port pin multiplexer output **0x1: DSI_RC_0:** dsi_rc[0] - dsi_xx_out_p[4]

(continued)

0x2: DSI_RC_1:
dsi_rc[1] - dsi_xx_out_p[5]

0x3: DSI_RC_2:
dsi_rc{1} - dsi_xx_out_p[6]

22.1.48 UDB_PA3_CFG2

PA Clock Select Register

Address: 0x400F5032

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	CLKOUT_SEL [7:4]				CLKIN_SEL [3:0]			

Bits	Name	Description
7 : 4	CLKOUT_SEL	Select one of four choices for clock enable Default Value: 0 **0x0: GCLK0:** gclk[0] **0x1: GCLK1:** gclk[1] **0x2: GCLK2:** gclk[2] **0x3: GCLK3:** gclk[3] **0x4: GCLK4:** gclk[4] **0x5: GCLK5:** gclk[5] **0x6: GCLK6:** gclk[6] **0x7: GCLK7:** gclk[7] **0x9: BUS_CLK_APP:** bus_clk_app **0xc: PIN_RC:** pin_rc - port pin multiplexer output **0xd: DSI_RC_0:** dsi_rc[0] - dsi_xx_out_p[4] **0xe: DSI_RC_1:** dsi_rc[1] - dsi_xx_out_p[5] **0xf: DSI_RC_2:** dsi_rc{1} - dsi_xx_out_p[6]
3 : 0	CLKIN_SEL	Select one of four choices for clock enable Default Value: 0 **0x0: GCLK0:** gclk[0]

(continued)

0x1: GCLK1:
gclk[1]

0x2: GCLK2:
gclk[2]

0x3: GCLK3:
gclk[3]

0x4: GCLK4:
gclk[4]

0x5: GCLK5:
gclk[5]

0x6: GCLK6:
gclk[6]

0x7: GCLK7:
gclk[7]

0x9: BUS_CLK_APP:
bus_clk_app

0xc: PIN_RC:
pin_rc - port pin multiplexer output

0xd: DSI_RC_0:
dsi_rc[0] - dsi_xx_out_p[4]

0xe: DSI_RC_1:
dsi_rc[1] - dsi_xx_out_p[5]

0xf: DSI_RC_2:
dsi_rc{1} - dsi_xx_out_p[6]

22.1.49 UDB_PA3_CFG3

PA Reset Select Register

Address: 0x400F5033

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW		RW	RW	RW	
HW Access	R	R	R		R	R	R	
Name	NC7	RES_OUT_INV	RES_OUT_SEL [5:4]		NC0	RES_IN_INV	RES_IN_SEL [1:0]	

Bits	Name	Description
7	NC7	Spare register bit Default Value: 0
6	RES_OUT_INV	Select the polarity of the reset control. Default Value: 0 **0x0: NOINV:** Not Inverted **0x1: INV:** Inverted
5 : 4	RES_OUT_SEL	Select one of four inputs to serve as the reset control to the block. Default Value: 0 **0x0: PIN_RC:** pin_rc - port pin multiplexer output **0x1: DSI_RC_0:** dsi_rc[0] - dsi_xx_out_p[4] **0x2: DSI_RC_1:** dsi_rc[1] - dsi_xx_out_p[5] **0x3: DSI_RC_2:** dsi_rc{1} - dsi_xx_out_p[6]
3	NC0	Spare register bit Default Value: 0
2	RES_IN_INV	Select the polarity of the reset control. Default Value: 0 **0x0: NOINV:** Not Inverted **0x1: INV:** Inverted
1 : 0	RES_IN_SEL	Select one of four inputs to serve as the reset control to the block. Default Value: 0 **0x0: PIN_RC:** pin_rc - port pin multiplexer output

(continued)

0x1: DSI_RC_0:
dsi_rc[0] - dsi_xx_out_p[4]

0x2: DSI_RC_1:
dsi_rc[1] - dsi_xx_out_p[5]

0x3: DSI_RC_2:
dsi_rc{1} - dsi_xx_out_p[6]

22.1.50 UDB_PA3_CFG4

PA Reset Enable Register

Address: 0x400F5034

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					RW	RW	RW
HW Access	R					R	R	R
Name	NC7654 [7:3]					RES_OE_EN	RES_OUT_EN	RES_IN_EN

Bits	Name	Description
7 : 3	NC7654	Spare register bits Default Value: 0
2	RES_OE_EN	Enable the selected reset Default Value: 0 **0x0: DISABLE:** Reset Disabled **0x1: ENABLE:** Reset Enabled
1	RES_OUT_EN	Enable the selected reset Default Value: 0 **0x0: DISABLE:** Reset Disabled **0x1: ENABLE:** Reset Enabled
0	RES_IN_EN	Enable the selected reset Default Value: 0 **0x0: DISABLE:** Reset Disabled **0x1: ENABLE:** Reset Enabled

22.1.51 UDB_PA3_CFG5

PA Reset Pin Select Register

Address: 0x400F5035

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		RW
HW Access	R					None		R
Name	NC7654 [7:3]					None [2:1]		PIN_SEL

Bits	Name	Description
7 : 3	NC7654	Spare register bits Default Value: 0
0	PIN_SEL	Select port input to route to reset multiplexer (dsi_xx_input_p[7:0]) Default Value: 0 **0x0: PIN0:** dsi_from_port_pin[0] **0x1: PIN1:** dsi_from_port_pin[1] **0x2: PIN2:** dsi_from_port_pin[2] **0x3: PIN3:** dsi_from_port_pin[3] **0x4: PIN4:** dsi_from_port_pin[4] **0x5: PIN5:** dsi_from_port_pin[5] **0x6: PIN6:** dsi_from_port_pin[6] **0x7: PIN7:** dsi_from_port_pin[7]

22.1.52 UDB_PA3_CFG6

PA Input Data Sync Control Register - Low

Address: 0x400F5036

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	IN_SYNC3 [7:6]		IN_SYNC2 [5:4]		IN_SYNC1 [3:2]		IN_SYNC0 [1:0]	

Bits	Name	Description
7 : 6	IN_SYNC3	Synchronization selection for PA input 3 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: DOUBLESYNC:** double sync **0x3: RSVD:** reserved
5 : 4	IN_SYNC2	Synchronization selection for PA input 2 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: DOUBLESYNC:** double sync **0x3: RSVD:** reserved
3 : 2	IN_SYNC1	Synchronization selection for PA input 1 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: DOUBLESYNC:** double sync **0x3: RSVD:** reserved
1 : 0	IN_SYNC0	Synchronization selection for PA input 0 Default Value: 0

(continued)

0x0: TRANSPARENT:
transparent

0x1: SINGLESYNC:
single sync

0x2: DOUBLESYNC:
double sync

0x3: RSVD:
reserved

22.1.53 UDB_PA3_CFG7

PA Input Data Sync Control Register - High

Address: 0x400F5037

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	IN_SYNC7 [7:6]		IN_SYNC6 [5:4]		IN_SYNC5 [3:2]		IN_SYNC4 [1:0]	

Bits	Name	Description
7 : 6	IN_SYNC7	Synchronization selection for PA input 7 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: DOUBLESYNC:** double sync **0x3: RSVD:** reserved
5 : 4	IN_SYNC6	Synchronization selection for PA input 6 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: DOUBLESYNC:** double sync **0x3: RSVD:** reserved
3 : 2	IN_SYNC5	Synchronization selection for PA input 5 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: DOUBLESYNC:** double sync **0x3: RSVD:** reserved
1 : 0	IN_SYNC4	Synchronization selection for PA input 4 Default Value: 0

(continued)

0x0: TRANSPARENT:
transparent

0x1: SINGLESYNC:
single sync

0x2: DOUBLESYNC:
double sync

0x3: RSVD:
reserved

22.1.54 UDB_PA3_CFG8

PA Output Data Sync Control Register - Low

Address: 0x400F5038

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	OUT_SYNC3 [7:6]		OUT_SYNC2 [5:4]		OUT_SYNC1 [3:2]		OUT_SYNC0 [1:0]	

Bits	Name	Description
7 : 6	OUT_SYNC3	Synchronization selection for PA output 3 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: CLOCK:** clock **0x3: CLOCKINV:** clock inverted
5 : 4	OUT_SYNC2	Synchronization selection for PA output 2 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: CLOCK:** clock **0x3: CLOCKINV:** clock inverted
3 : 2	OUT_SYNC1	Synchronization selection for PA output 1 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: CLOCK:** clock **0x3: CLOCKINV:** clock inverted
1 : 0	OUT_SYNC0	Synchronization selection for PA output 0 Default Value: 0

(continued)

0x0: TRANSPARENT:
transparent

0x1: SINGLESYNC:
single sync

0x2: CLOCK:
clock

0x3: CLOCKINV:
clock inverted

22.1.55 UDB_PA3_CFG9

PA Output Data Sync Control Register - High

Address: 0x400F5039

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	OUT_SYNC7 [7:6]		OUT_SYNC6 [5:4]		OUT_SYNC5 [3:2]		OUT_SYNC4 [1:0]	

Bits	Name	Description
7 : 6	OUT_SYNC7	Synchronization selection for PA output 7 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: CLOCK:** clock **0x3: CLOCKINV:** clock inverted
5 : 4	OUT_SYNC6	Synchronization selection for PA output 6 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: CLOCK:** clock **0x3: CLOCKINV:** clock inverted
3 : 2	OUT_SYNC5	Synchronization selection for PA output 5 Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: CLOCK:** clock **0x3: CLOCKINV:** clock inverted
1 : 0	OUT_SYNC4	Synchronization selection for PA output 4 Default Value: 0

(continued)

0x0: TRANSPARENT:
transparent

0x1: SINGLESYNC:
single sync

0x2: CLOCK:
clock

0x3: CLOCKINV:
clock inverted

22.1.56 UDB_PA3_CFG10

PA Output Data Select Register - Low

Address: 0x400F503A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	DATA_SEL3 [7:6]		DATA_SEL2 [5:4]		DATA_SEL1 [3:2]		DATA_SEL0 [1:0]	

Bits	Name	Description
7 : 6	DATA_SEL3	Data selection for PA output 3 Default Value: 0 **0x0: DSI_OUTPUT0:** dsi output 0 **0x1: DSI_OUTPUT1:** dsi output 1 **0x2: DSI_OUTPUT2:** dsi output 2 **0x3: DSI_OUTPUT3:** dsi output 3
5 : 4	DATA_SEL2	Data selection for PA output 2 Default Value: 0 **0x0: DSI_OUTPUT0:** dsi output 0 **0x1: DSI_OUTPUT1:** dsi output 1 **0x2: DSI_OUTPUT2:** dsi output 2 **0x3: DSI_OUTPUT3:** dsi output 3
3 : 2	DATA_SEL1	Data selection for PA output 1 Default Value: 0 **0x0: DSI_OUTPUT0:** dsi output 0 **0x1: DSI_OUTPUT1:** dsi output 1 **0x2: DSI_OUTPUT2:** dsi output 2 **0x3: DSI_OUTPUT3:** dsi output 3
1 : 0	DATA_SEL0	Data selection for PA output 0 Default Value: 0

(continued)

0x0: DSI_OUTPUT0:
dsi output 0

0x1: DSI_OUTPUT1:
dsi output 1

0x2: DSI_OUTPUT2:
dsi output 2

0x3: DSI_OUTPUT3:
dsi output 3

22.1.57 UDB_PA3_CFG11

PA Output Data Select Register - High

Address: 0x400F503B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	DATA_SEL7 [7:6]		DATA_SEL6 [5:4]		DATA_SEL5 [3:2]		DATA_SEL4 [1:0]	

Bits	Name	Description
7 : 6	DATA_SEL7	Data selection for PA output 7 Default Value: 0 **0x0: DSI_OUTPUT0:** dsi output 0 **0x1: DSI_OUTPUT1:** dsi output 1 **0x2: DSI_OUTPUT2:** dsi output 2 **0x3: DSI_OUTPUT3:** dsi output 3
5 : 4	DATA_SEL6	Data selection for PA output 6 Default Value: 0 **0x0: DSI_OUTPUT0:** dsi output 0 **0x1: DSI_OUTPUT1:** dsi output 1 **0x2: DSI_OUTPUT2:** dsi output 2 **0x3: DSI_OUTPUT3:** dsi output 3
3 : 2	DATA_SEL5	Data selection for PA output 5 Default Value: 0 **0x0: DSI_OUTPUT0:** dsi output 0 **0x1: DSI_OUTPUT1:** dsi output 1 **0x2: DSI_OUTPUT2:** dsi output 2 **0x3: DSI_OUTPUT3:** dsi output 3
1 : 0	DATA_SEL4	Data selection for PA output 4 Default Value: 0

(continued)

0x0: DSI_OUTPUT0:
dsi output 0

0x1: DSI_OUTPUT1:
dsi output 1

0x2: DSI_OUTPUT2:
dsi output 2

0x3: DSI_OUTPUT3:
dsi output 3

22.1.58 UDB_PA3_CFG12

PA OE Select Register - Low

Address: 0x400F503C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	OE_SEL3 [7:6]		OE_SEL2 [5:4]		OE_SEL1 [3:2]		OE_SEL0 [1:0]	

Bits	Name	Description
7 : 6	OE_SEL3	Data selection for PA oe 3 Default Value: 0 **0x0: DSI_OE_OUT0:** synchronized dsi oe output 0 **0x1: DSI_OE_OUT1:** synchronized dsi oe output 1 **0x2: DSI_OE_OUT2:** synchronized dsi oe output 2 **0x3: DSI_OE_OUT3:** synchronized dsi oe output 3
5 : 4	OE_SEL2	Data selection for PA oe 2 Default Value: 0 **0x0: DSI_OE_OUT0:** synchronized dsi oe output 0 **0x1: DSI_OE_OUT1:** synchronized dsi oe output 1 **0x2: DSI_OE_OUT2:** synchronized dsi oe output 2 **0x3: DSI_OE_OUT3:** synchronized dsi oe output 3
3 : 2	OE_SEL1	Data selection for PA oe 1 Default Value: 0 **0x0: DSI_OE_OUT0:** synchronized dsi oe output 0 **0x1: DSI_OE_OUT1:** synchronized dsi oe output 1 **0x2: DSI_OE_OUT2:** synchronized dsi oe output 2 **0x3: DSI_OE_OUT3:** synchronized dsi oe output 3
1 : 0	OE_SEL0	Data selection for PA oe 0 Default Value: 0

(continued)

0x0: DSI_OE_OUT0:
synchronized dsi oe output 0

0x1: DSI_OE_OUT1:
synchronized dsi oe output 1

0x2: DSI_OE_OUT2:
synchronized dsi oe output 2

0x3: DSI_OE_OUT3:
synchronized dsi oe output 3

22.1.59 UDB_PA3_CFG13

PA OE Select Register - High

Address: 0x400F503D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	OE_SEL7 [7:6]		OE_SEL6 [5:4]		OE_SEL5 [3:2]		OE_SEL4 [1:0]	

Bits	Name	Description
7 : 6	OE_SEL7	Data selection for PA oe 7 Default Value: 0 **0x0: DSI_OE_OUT0:** synchronized dsi oe output 0 **0x1: DSI_OE_OUT1:** synchronized dsi oe output 1 **0x2: DSI_OE_OUT2:** synchronized dsi oe output 2 **0x3: DSI_OE_OUT3:** synchronized dsi oe output 3
5 : 4	OE_SEL6	Data selection for PA oe 6 Default Value: 0 **0x0: DSI_OE_OUT0:** synchronized dsi oe output 0 **0x1: DSI_OE_OUT1:** synchronized dsi oe output 1 **0x2: DSI_OE_OUT2:** synchronized dsi oe output 2 **0x3: DSI_OE_OUT3:** synchronized dsi oe output 3
3 : 2	OE_SEL5	Data selection for PA oe 5 Default Value: 0 **0x0: DSI_OE_OUT0:** synchronized dsi oe output 0 **0x1: DSI_OE_OUT1:** synchronized dsi oe output 1 **0x2: DSI_OE_OUT2:** synchronized dsi oe output 2 **0x3: DSI_OE_OUT3:** synchronized dsi oe output 3
1 : 0	OE_SEL4	Data selection for PA oe 4 Default Value: 0

(continued)

0x0: DSI_OE_OUT0:
synchronized dsi oe output 0

0x1: DSI_OE_OUT1:
synchronized dsi oe output 1

0x2: DSI_OE_OUT2:
synchronized dsi oe output 2

0x3: DSI_OE_OUT3:
synchronized dsi oe output 3

22.1.60 UDB_PA3_CFG14

PA OE Sync Register

Address: 0x400F503E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	OE_SYNC3 [7:6]		OE_SYNC2 [5:4]		OE_SYNC1 [3:2]		OE_SYNC0 [1:0]	

Bits	Name	Description
7 : 6	OE_SYNC3	Synchronization options for dsi_to_oe[3] Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: CONSTANT1:** 1 **0x3: CONSTANT0:** 0
5 : 4	OE_SYNC2	Synchronization options for dsi_to_oe[2] Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: CONSTANT1:** 1 **0x3: CONSTANT0:** 0
3 : 2	OE_SYNC1	Synchronization options for dsi_to_oe[1] Default Value: 0 **0x0: TRANSPARENT:** transparent **0x1: SINGLESYNC:** single sync **0x2: CONSTANT1:** 1 **0x3: CONSTANT0:** 0
1 : 0	OE_SYNC0	Synchronization options for dsi_to_oe[0] Default Value: 0

(continued)

0x0: TRANSPARENT:
transparent

0x1: SINGLESYNC:
single sync

0x2: CONSTANT1:
1

0x3: CONSTANT0:
0

23 PASS MMIO Registers

This section discusses the Programmable Analog Sub System Memory Mapped IO (PASS MMIO) registers. It lists all the registers in mapping tables, in address order.

23.1 Register Details

Register Name	Address
PASS_INTR_CAUSE	0x403F0000
PASS_DFT_CTRL	0x403F0030
PASS_DSAB_TRIM	0x403F0F00

23.1.1 PASS_INTR_CAUSE

Interrupt cause register

Address: 0x403F0000

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						W	W
Name	None [7:2]						CTB1_INT	CTB0_INT

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CTB1_INT	CTB1 interrupt pending Default Value: 0
0	CTB0_INT	CTB0 interrupt pending Default Value: 0

23.1.2 PASS_DFT_CTRL

DFT control register

Address: 0x403F0030

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							DSAB_ADFT_RES_EN

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	DSAB_ADFT_RES_EN	Close the switch to connect the DSAB ADFT resistor to the AMUXBUS Default Value: 0

23.1.3 PASS_DSAB_TRIM

DSAB Trim bits

Address: 0x403F0F00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				IBIAS_TRIM [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	IBIAS_TRIM	1111=lowest, 0000=highest Default Value: 0

24 Peripheral Interconnect (PERI) Registers

This section discusses the PERI registers. It lists all the registers in mapping tables, in address order.

24.1 Register Details

Register Name	Address
PERI_DIV_CMD	0x40010000
PERI_PCLK_CTL0	0x40010100
PERI_PCLK_CTL1	0x40010104
PERI_PCLK_CTL2	0x40010108
PERI_PCLK_CTL3	0x4001010C
PERI_PCLK_CTL4	0x40010110
PERI_PCLK_CTL5	0x40010114
PERI_PCLK_CTL6	0x40010118
PERI_PCLK_CTL7	0x4001011C
PERI_PCLK_CTL8	0x40010120
PERI_PCLK_CTL9	0x40010124
PERI_PCLK_CTL10	0x40010128
PERI_PCLK_CTL11	0x4001012C
PERI_PCLK_CTL12	0x40010130
PERI_PCLK_CTL13	0x40010134
PERI_PCLK_CTL14	0x40010138
PERI_PCLK_CTL15	0x4001013C
PERI_DIV_16_CTL0	0x40010300
PERI_DIV_16_CTL1	0x40010304
PERI_DIV_16_CTL2	0x40010308
PERI_DIV_16_CTL3	0x4001030C
PERI_DIV_16_CTL4	0x40010310
PERI_DIV_16_CTL5	0x40010314
PERI_DIV_16_CTL6	0x40010318
PERI_DIV_16_CTL7	0x4001031C
PERI_DIV_16_CTL8	0x40010320

Register Name	Address
PERI_DIV_16_CTL9	0x40010324
PERI_DIV_16_5_CTL0	0x40010400
PERI_DIV_16_5_CTL1	0x40010404

24.1.1 PERI_DIV_CMD

Divider command register

Address: 0x40010000

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW					
HW Access	R		R					
Name	SEL_TYPE [7:6]		SEL_DIV [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW					
HW Access	R		R					
Name	PA_SEL_TYPE [15:14]		PA_SEL_DIV [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None					
HW Access	RW1C	RW1C	None					
Name	ENABLE	DISABLE	None [29:24]					

Bits	Name	Description

(continued)

31	ENABLE	Clock divider enable command (mutually exclusive with DISABLE). Typically, SW sets this field to '1' to enable a divider and HW sets this field to '0' to indicate that divider enabling has completed. When a divider is enabled, its integer and fractional (if present) counters are initialized to "0". If a divider is to be re-enabled using different integer and fractional divider values, the SW should follow these steps: 0: Disable the divider using the DIV_CMD.DISABLE field. 1: Configure the divider's DIV_XXX_CTL register. 2: Enable the divider using the DIV_CMD_ENABLE field. The SEL_DIV and SEL_TYPE fields specify which divider is to be enabled. The enabled divider may be phase aligned to either "clk_hf" (typical usage) or to ANY enabled divider. The PA_SEL_DIV and P_SEL_TYPE fields specify the reference divider. The HW sets the ENABLE field to '0' when the enabling is performed and the HW set the DIV_XXX_CTL.EN field of the divider to '1' when the enabling is performed. Note that enabling with phase alignment to a low frequency divider takes time. E.g. To align to a divider that generates a clock of "clk_hf"/n (with n being the integer divider value INT_DIV+1), up to n cycles may be required to perform alignment. Phase alignment to "clk_hf" takes affect immediately. SW can set this field to '0' during phase alignment to abort the enabling process. Default Value: 0
30	DISABLE	Clock divider disable command (mutually exlusive with ENABLE). SW sets this field to '1' and HW sets this field to '0'. The SEL_DIV and SEL_TYPE fields specify which divider is to be disabled. The HW sets the DISABLE field to '0' immediately and the HW sets the DIV_XXX_CTL.EN field of the divider to '0' immediately. Default Value: 0
15 : 14	PA_SEL_TYPE	Specifies the divider type of the divider to which phase alignment is performed for the clock enable command: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
13 : 8	PA_SEL_DIV	(PA_SEL_TYPE, PA_SEL_DIV) pecifies the divider to which phase alignment is performed for the clock enable command. Any enabled divider can be used as reference. This allows all dividers to be aligned with each other, even when they are enabled at different times. If PA_SEL_DIV is "63" and "PA_SEL_TYPE" is "3", "clk_hf" is used as reference. Default Value: 63
7 : 6	SEL_TYPE	Specifies the divider type of the divider on which the command is performed: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
5 : 0	SEL_DIV	(SEL_TYPE, SEL_DIV) specifies the divider on which the command (DISABLE/ENABLE) is performed. If SEL_DIV is "63" and "SEL_TYPE" is "3" (default/reset value), no divider is specified and no clock signal(s) are generated. Default Value: 63

24.1.2 PERI_PCLK_CTL0

Programmable clock control register

Address: 0x40010100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None		RW			
HW Access	R		None		R			
Name	SEL_TYPE [7:6]		None [5:4]		SEL_DIV [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	SEL_TYPE	Specifies divider type: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
3 : 0	SEL_DIV	Specifies one of the dividers of the divider type specified by SEL_TYPE. If SEL_DIV is "63" and "SEL_TYPE" is "3" (default/reset value), no divider is specified and no clock control signal(s) are generated. When transitioning a clock between two out of phase dividers, spurious clock control signals may be generated for one clk_hf cycle during this transition. These clock control signals may cause a single clock period that is smaller than any of the two divider periods. To prevent these spurious clock signals, the clock multiplexer can be disconnected (SEL_DIV is "63" and "SEL_TYPE" is "3") for a transition time that is larger than the smaller of the two divider periods. Default Value: 15

24.1.3 PERI_PCLK_CTL1

Programmable clock control register

Address: 0x40010104

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None		RW			
HW Access	R		None		R			
Name	SEL_TYPE [7:6]		None [5:4]		SEL_DIV [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	SEL_TYPE	Specifies divider type: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
3 : 0	SEL_DIV	Specifies one of the dividers of the divider type specified by SEL_TYPE. If SEL_DIV is "63" and "SEL_TYPE" is "3" (default/reset value), no divider is specified and no clock control signal(s) are generated. When transitioning a clock between two out of phase dividers, spurious clock control signals may be generated for one clk_hf cycle during this transition. These clock control signals may cause a single clock period that is smaller than any of the two divider periods. To prevent these spurious clock signals, the clock multiplexer can be disconnected (SEL_DIV is "63" and "SEL_TYPE" is "3") for a transition time that is larger than the smaller of the two divider periods. Default Value: 15

24.1.4 PERI_PCLK_CTL2

Programmable clock control register

Address: 0x40010108

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None		RW			
HW Access	R		None		R			
Name	SEL_TYPE [7:6]		None [5:4]		SEL_DIV [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	SEL_TYPE	Specifies divider type: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
3 : 0	SEL_DIV	Specifies one of the dividers of the divider type specified by SEL_TYPE. If SEL_DIV is "63" and "SEL_TYPE" is "3" (default/reset value), no divider is specified and no clock control signal(s) are generated. When transitioning a clock between two out of phase dividers, spurious clock control signals may be generated for one clk_hf cycle during this transition. These clock control signals may cause a single clock period that is smaller than any of the two divider periods. To prevent these spurious clock signals, the clock multiplexer can be disconnected (SEL_DIV is "63" and "SEL_TYPE" is "3") for a transition time that is larger than the smaller of the two divider periods. Default Value: 15

24.1.5 PERI_PCLK_CTL3

Programmable clock control register

Address: 0x4001010C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None		RW			
HW Access	R		None		R			
Name	SEL_TYPE [7:6]		None [5:4]		SEL_DIV [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	SEL_TYPE	Specifies divider type: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
3 : 0	SEL_DIV	Specifies one of the dividers of the divider type specified by SEL_TYPE. If SEL_DIV is "63" and "SEL_TYPE" is "3" (default/reset value), no divider is specified and no clock control signal(s) are generated. When transitioning a clock between two out of phase dividers, spurious clock control signals may be generated for one clk_hf cycle during this transition. These clock control signals may cause a single clock period that is smaller than any of the two divider periods. To prevent these spurious clock signals, the clock multiplexer can be disconnected (SEL_DIV is "63" and "SEL_TYPE" is "3") for a transition time that is larger than the smaller of the two divider periods. Default Value: 15

24.1.6 PERI_PCLK_CTL4

Programmable clock control register

Address: 0x40010110

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None		RW			
HW Access	R		None		R			
Name	SEL_TYPE [7:6]		None [5:4]		SEL_DIV [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	SEL_TYPE	Specifies divider type: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
3 : 0	SEL_DIV	Specifies one of the dividers of the divider type specified by SEL_TYPE. If SEL_DIV is "63" and "SEL_TYPE" is "3" (default/reset value), no divider is specified and no clock control signal(s) are generated. When transitioning a clock between two out of phase dividers, spurious clock control signals may be generated for one clk_hf cycle during this transition. These clock control signals may cause a single clock period that is smaller than any of the two divider periods. To prevent these spurious clock signals, the clock multiplexer can be disconnected (SEL_DIV is "63" and "SEL_TYPE" is "3") for a transition time that is larger than the smaller of the two divider periods. Default Value: 15

24.1.7 PERI_PCLK_CTL5

Programmable clock control register

Address: 0x40010114

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None		RW			
HW Access	R		None		R			
Name	SEL_TYPE [7:6]		None [5:4]		SEL_DIV [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	SEL_TYPE	Specifies divider type: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
3 : 0	SEL_DIV	Specifies one of the dividers of the divider type specified by SEL_TYPE. If SEL_DIV is "63" and "SEL_TYPE" is "3" (default/reset value), no divider is specified and no clock control signal(s) are generated. When transitioning a clock between two out of phase dividers, spurious clock control signals may be generated for one clk_hf cycle during this transition. These clock control signals may cause a single clock period that is smaller than any of the two divider periods. To prevent these spurious clock signals, the clock multiplexer can be disconnected (SEL_DIV is "63" and "SEL_TYPE" is "3") for a transition time that is larger than the smaller of the two divider periods. Default Value: 15

24.1.8 PERI_PCLK_CTL6

Programmable clock control register

Address: 0x40010118

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None		RW			
HW Access	R		None		R			
Name	SEL_TYPE [7:6]		None [5:4]		SEL_DIV [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	SEL_TYPE	Specifies divider type: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
3 : 0	SEL_DIV	Specifies one of the dividers of the divider type specified by SEL_TYPE. If SEL_DIV is "63" and "SEL_TYPE" is "3" (default/reset value), no divider is specified and no clock control signal(s) are generated. When transitioning a clock between two out of phase dividers, spurious clock control signals may be generated for one clk_hf cycle during this transition. These clock control signals may cause a single clock period that is smaller than any of the two divider periods. To prevent these spurious clock signals, the clock multiplexer can be disconnected (SEL_DIV is "63" and "SEL_TYPE" is "3") for a transition time that is larger than the smaller of the two divider periods. Default Value: 15

24.1.9 PERI_PCLK_CTL7

Programmable clock control register

Address: 0x4001011C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None		RW			
HW Access	R		None		R			
Name	SEL_TYPE [7:6]		None [5:4]		SEL_DIV [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	SEL_TYPE	Specifies divider type: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
3 : 0	SEL_DIV	Specifies one of the dividers of the divider type specified by SEL_TYPE. If SEL_DIV is "63" and "SEL_TYPE" is "3" (default/reset value), no divider is specified and no clock control signal(s) are generated. When transitioning a clock between two out of phase dividers, spurious clock control signals may be generated for one clk_hf cycle during this transition. These clock control signals may cause a single clock period that is smaller than any of the two divider periods. To prevent these spurious clock signals, the clock multiplexer can be disconnected (SEL_DIV is "63" and "SEL_TYPE" is "3") for a transition time that is larger than the smaller of the two divider periods. Default Value: 15

24.1.10 PERI_PCLK_CTL8

Programmable clock control register

Address: 0x40010120

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None		RW			
HW Access	R		None		R			
Name	SEL_TYPE [7:6]		None [5:4]		SEL_DIV [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	SEL_TYPE	Specifies divider type: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
3 : 0	SEL_DIV	Specifies one of the dividers of the divider type specified by SEL_TYPE. If SEL_DIV is "63" and "SEL_TYPE" is "3" (default/reset value), no divider is specified and no clock control signal(s) are generated. When transitioning a clock between two out of phase dividers, spurious clock control signals may be generated for one clk_hf cycle during this transition. These clock control signals may cause a single clock period that is smaller than any of the two divider periods. To prevent these spurious clock signals, the clock multiplexer can be disconnected (SEL_DIV is "63" and "SEL_TYPE" is "3") for a transition time that is larger than the smaller of the two divider periods. Default Value: 15

24.1.11 PERI_PCLK_CTL9

Programmable clock control register

Address: 0x40010124

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None		RW			
HW Access	R		None		R			
Name	SEL_TYPE [7:6]		None [5:4]		SEL_DIV [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	SEL_TYPE	Specifies divider type: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
3 : 0	SEL_DIV	Specifies one of the dividers of the divider type specified by SEL_TYPE. If SEL_DIV is "63" and "SEL_TYPE" is "3" (default/reset value), no divider is specified and no clock control signal(s) are generated. When transitioning a clock between two out of phase dividers, spurious clock control signals may be generated for one clk_hf cycle during this transition. These clock control signals may cause a single clock period that is smaller than any of the two divider periods. To prevent these spurious clock signals, the clock multiplexer can be disconnected (SEL_DIV is "63" and "SEL_TYPE" is "3") for a transition time that is larger than the smaller of the two divider periods. Default Value: 15

24.1.12 PERI_PCLK_CTL10

Programmable clock control register

Address: 0x40010128

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None		RW			
HW Access	R		None		R			
Name	SEL_TYPE [7:6]		None [5:4]		SEL_DIV [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	SEL_TYPE	Specifies divider type: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
3 : 0	SEL_DIV	Specifies one of the dividers of the divider type specified by SEL_TYPE. If SEL_DIV is "63" and "SEL_TYPE" is "3" (default/reset value), no divider is specified and no clock control signal(s) are generated. When transitioning a clock between two out of phase dividers, spurious clock control signals may be generated for one clk_hf cycle during this transition. These clock control signals may cause a single clock period that is smaller than any of the two divider periods. To prevent these spurious clock signals, the clock multiplexer can be disconnected (SEL_DIV is "63" and "SEL_TYPE" is "3") for a transition time that is larger than the smaller of the two divider periods. Default Value: 15

24.1.13 PERI_PCLK_CTL11

Programmable clock control register

Address: 0x4001012C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None		RW			
HW Access	R		None		R			
Name	SEL_TYPE [7:6]		None [5:4]		SEL_DIV [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	SEL_TYPE	Specifies divider type: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
3 : 0	SEL_DIV	Specifies one of the dividers of the divider type specified by SEL_TYPE. If SEL_DIV is "63" and "SEL_TYPE" is "3" (default/reset value), no divider is specified and no clock control signal(s) are generated. When transitioning a clock between two out of phase dividers, spurious clock control signals may be generated for one clk_hf cycle during this transition. These clock control signals may cause a single clock period that is smaller than any of the two divider periods. To prevent these spurious clock signals, the clock multiplexer can be disconnected (SEL_DIV is "63" and "SEL_TYPE" is "3") for a transition time that is larger than the smaller of the two divider periods. Default Value: 15

24.1.14 PERI_PCLK_CTL12

Programmable clock control register

Address: 0x40010130

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None		RW			
HW Access	R		None		R			
Name	SEL_TYPE [7:6]		None [5:4]		SEL_DIV [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	SEL_TYPE	Specifies divider type: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
3 : 0	SEL_DIV	Specifies one of the dividers of the divider type specified by SEL_TYPE. If SEL_DIV is "63" and "SEL_TYPE" is "3" (default/reset value), no divider is specified and no clock control signal(s) are generated. When transitioning a clock between two out of phase dividers, spurious clock control signals may be generated for one clk_hf cycle during this transition. These clock control signals may cause a single clock period that is smaller than any of the two divider periods. To prevent these spurious clock signals, the clock multiplexer can be disconnected (SEL_DIV is "63" and "SEL_TYPE" is "3") for a transition time that is larger than the smaller of the two divider periods. Default Value: 15

24.1.15 PERI_PCLK_CTL13

Programmable clock control register

Address: 0x40010134

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None		RW			
HW Access	R		None		R			
Name	SEL_TYPE [7:6]		None [5:4]		SEL_DIV [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	SEL_TYPE	Specifies divider type: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
3 : 0	SEL_DIV	Specifies one of the dividers of the divider type specified by SEL_TYPE. If SEL_DIV is "63" and "SEL_TYPE" is "3" (default/reset value), no divider is specified and no clock control signal(s) are generated. When transitioning a clock between two out of phase dividers, spurious clock control signals may be generated for one clk_hf cycle during this transition. These clock control signals may cause a single clock period that is smaller than any of the two divider periods. To prevent these spurious clock signals, the clock multiplexer can be disconnected (SEL_DIV is "63" and "SEL_TYPE" is "3") for a transition time that is larger than the smaller of the two divider periods. Default Value: 15

24.1.16 PERI_PCLK_CTL14

Programmable clock control register

Address: 0x40010138

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None		RW			
HW Access	R		None		R			
Name	SEL_TYPE [7:6]		None [5:4]		SEL_DIV [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	SEL_TYPE	Specifies divider type: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
3 : 0	SEL_DIV	Specifies one of the dividers of the divider type specified by SEL_TYPE. If SEL_DIV is "63" and "SEL_TYPE" is "3" (default/reset value), no divider is specified and no clock control signal(s) are generated. When transitioning a clock between two out of phase dividers, spurious clock control signals may be generated for one clk_hf cycle during this transition. These clock control signals may cause a single clock period that is smaller than any of the two divider periods. To prevent these spurious clock signals, the clock multiplexer can be disconnected (SEL_DIV is "63" and "SEL_TYPE" is "3") for a transition time that is larger than the smaller of the two divider periods. Default Value: 15

24.1.17 PERI_PCLK_CTL15

Programmable clock control register

Address: 0x4001013C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None		RW			
HW Access	R		None		R			
Name	SEL_TYPE [7:6]		None [5:4]		SEL_DIV [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	SEL_TYPE	Specifies divider type: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
3 : 0	SEL_DIV	Specifies one of the dividers of the divider type specified by SEL_TYPE. If SEL_DIV is "63" and "SEL_TYPE" is "3" (default/reset value), no divider is specified and no clock control signal(s) are generated. When transitioning a clock between two out of phase dividers, spurious clock control signals may be generated for one clk_hf cycle during this transition. These clock control signals may cause a single clock period that is smaller than any of the two divider periods. To prevent these spurious clock signals, the clock multiplexer can be disconnected (SEL_DIV is "63" and "SEL_TYPE" is "3") for a transition time that is larger than the smaller of the two divider periods. Default Value: 15

24.1.18 PERI_DIV_16_CTL0

Divider control register (for 16.0 divider)

Address: 0x40010300

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INT16_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INT16_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 8	INT16_DIV	Integer division by (1+INT16_DIV). Allows for integer divisions in the range [1, 65,536]. Note: this type of divider does NOT allow for a fractional division. For the generation of a divided clock, the integer division range is restricted to [2, 65,536]. For the generation of a 50/50% duty cycle digital divided clock, the integer division range is restricted to even numbers in the range [2, 65,536]. The generation of a 50/50 % duty cycle analog divided clock has no restrictions. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0
0	EN	Divider enabled. HW sets this field to '1' as a result of an ENABLE command. HW sets this field to '0' as a result on a DISABLE command. Note that this field is retained. As a result, the divider does NOT have to be re-enabled after transitioning from DeepSleep to Active power mode. Default Value: 0

24.1.19 PERI_DIV_16_CTL1

Divider control register (for 16.0 divider)

Address: 0x40010304

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INT16_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INT16_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 8	INT16_DIV	Integer division by (1+INT16_DIV). Allows for integer divisions in the range [1, 65,536]. Note: this type of divider does NOT allow for a fractional division. For the generation of a divided clock, the integer division range is restricted to [2, 65,536]. For the generation of a 50/50% duty cycle digital divided clock, the integer division range is restricted to even numbers in the range [2, 65,536]. The generation of a 50/50 % duty cycle analog divided clock has no restrictions. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0
0	EN	Divider enabled. HW sets this field to '1' as a result of an ENABLE command. HW sets this field to '0' as a result on a DISABLE command. Note that this field is retained. As a result, the divider does NOT have to be re-enabled after transitioning from DeepSleep to Active power mode. Default Value: 0

24.1.20 PERI_DIV_16_CTL2

Divider control register (for 16.0 divider)

Address: 0x40010308

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INT16_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INT16_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 8	INT16_DIV	Integer division by (1+INT16_DIV). Allows for integer divisions in the range [1, 65,536]. Note: this type of divider does NOT allow for a fractional division. For the generation of a divided clock, the integer division range is restricted to [2, 65,536]. For the generation of a 50/50% duty cycle digital divided clock, the integer division range is restricted to even numbers in the range [2, 65,536]. The generation of a 50/50 % duty cycle analog divided clock has no restrictions. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0
0	EN	Divider enabled. HW sets this field to '1' as a result of an ENABLE command. HW sets this field to '0' as a result on a DISABLE command. Note that this field is retained. As a result, the divider does NOT have to be re-enabled after transitioning from DeepSleep to Active power mode. Default Value: 0

24.1.21 PERI_DIV_16_CTL3

Divider control register (for 16.0 divider)

Address: 0x4001030C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INT16_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INT16_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 8	INT16_DIV	Integer division by (1+INT16_DIV). Allows for integer divisions in the range [1, 65,536]. Note: this type of divider does NOT allow for a fractional division. For the generation of a divided clock, the integer division range is restricted to [2, 65,536]. For the generation of a 50/50% duty cycle digital divided clock, the integer division range is restricted to even numbers in the range [2, 65,536]. The generation of a 50/50 % duty cycle analog divided clock has no restrictions. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0
0	EN	Divider enabled. HW sets this field to '1' as a result of an ENABLE command. HW sets this field to '0' as a result on a DISABLE command. Note that this field is retained. As a result, the divider does NOT have to be re-enabled after transitioning from DeepSleep to Active power mode. Default Value: 0

24.1.22 PERI_DIV_16_CTL4

Divider control register (for 16.0 divider)

Address: 0x40010310

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INT16_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INT16_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 8	INT16_DIV	Integer division by (1+INT16_DIV). Allows for integer divisions in the range [1, 65,536]. Note: this type of divider does NOT allow for a fractional division. For the generation of a divided clock, the integer division range is restricted to [2, 65,536]. For the generation of a 50/50% duty cycle digital divided clock, the integer division range is restricted to even numbers in the range [2, 65,536]. The generation of a 50/50 % duty cycle analog divided clock has no restrictions. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0
0	EN	Divider enabled. HW sets this field to '1' as a result of an ENABLE command. HW sets this field to '0' as a result on a DISABLE command. Note that this field is retained. As a result, the divider does NOT have to be re-enabled after transitioning from DeepSleep to Active power mode. Default Value: 0

24.1.23 PERI_DIV_16_CTL5

Divider control register (for 16.0 divider)

Address: 0x40010314

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INT16_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INT16_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 8	INT16_DIV	Integer division by (1+INT16_DIV). Allows for integer divisions in the range [1, 65,536]. Note: this type of divider does NOT allow for a fractional division. For the generation of a divided clock, the integer division range is restricted to [2, 65,536]. For the generation of a 50/50% duty cycle digital divided clock, the integer division range is restricted to even numbers in the range [2, 65,536]. The generation of a 50/50 % duty cycle analog divided clock has no restrictions. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0
0	EN	Divider enabled. HW sets this field to '1' as a result of an ENABLE command. HW sets this field to '0' as a result on a DISABLE command. Note that this field is retained. As a result, the divider does NOT have to be re-enabled after transitioning from DeepSleep to Active power mode. Default Value: 0

24.1.24 PERI_DIV_16_CTL6

Divider control register (for 16.0 divider)

Address: 0x40010318

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INT16_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INT16_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 8	INT16_DIV	Integer division by (1+INT16_DIV). Allows for integer divisions in the range [1, 65,536]. Note: this type of divider does NOT allow for a fractional division. For the generation of a divided clock, the integer division range is restricted to [2, 65,536]. For the generation of a 50/50% duty cycle digital divided clock, the integer division range is restricted to even numbers in the range [2, 65,536]. The generation of a 50/50 % duty cycle analog divided clock has no restrictions. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0
0	EN	Divider enabled. HW sets this field to '1' as a result of an ENABLE command. HW sets this field to '0' as a result on a DISABLE command. Note that this field is retained. As a result, the divider does NOT have to be re-enabled after transitioning from DeepSleep to Active power mode. Default Value: 0

24.1.25 PERI_DIV_16_CTL7

Divider control register (for 16.0 divider)

Address: 0x4001031C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INT16_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INT16_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 8	INT16_DIV	Integer division by (1+INT16_DIV). Allows for integer divisions in the range [1, 65,536]. Note: this type of divider does NOT allow for a fractional division. For the generation of a divided clock, the integer division range is restricted to [2, 65,536]. For the generation of a 50/50% duty cycle digital divided clock, the integer division range is restricted to even numbers in the range [2, 65,536]. The generation of a 50/50 % duty cycle analog divided clock has no restrictions. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0
0	EN	Divider enabled. HW sets this field to '1' as a result of an ENABLE command. HW sets this field to '0' as a result on a DISABLE command. Note that this field is retained. As a result, the divider does NOT have to be re-enabled after transitioning from DeepSleep to Active power mode. Default Value: 0

24.1.26 PERI_DIV_16_CTL8

Divider control register (for 16.0 divider)

Address: 0x40010320

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INT16_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INT16_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 8	INT16_DIV	Integer division by (1+INT16_DIV). Allows for integer divisions in the range [1, 65,536]. Note: this type of divider does NOT allow for a fractional division. For the generation of a divided clock, the integer division range is restricted to [2, 65,536]. For the generation of a 50/50% duty cycle digital divided clock, the integer division range is restricted to even numbers in the range [2, 65,536]. The generation of a 50/50 % duty cycle analog divided clock has no restrictions. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0
0	EN	Divider enabled. HW sets this field to '1' as a result of an ENABLE command. HW sets this field to '0' as a result on a DISABLE command. Note that this field is retained. As a result, the divider does NOT have to be re-enabled after transitioning from DeepSleep to Active power mode. Default Value: 0

24.1.27 PERI_DIV_16_CTL9

Divider control register (for 16.0 divider)

Address: 0x40010324

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INT16_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INT16_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 8	INT16_DIV	Integer division by (1+INT16_DIV). Allows for integer divisions in the range [1, 65,536]. Note: this type of divider does NOT allow for a fractional division. For the generation of a divided clock, the integer division range is restricted to [2, 65,536]. For the generation of a 50/50% duty cycle digital divided clock, the integer division range is restricted to even numbers in the range [2, 65,536]. The generation of a 50/50 % duty cycle analog divided clock has no restrictions. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0
0	EN	Divider enabled. HW sets this field to '1' as a result of an ENABLE command. HW sets this field to '0' as a result on a DISABLE command. Note that this field is retained. As a result, the divider does NOT have to be re-enabled after transitioning from DeepSleep to Active power mode. Default Value: 0

24.1.28 PERI_DIV_16_5_CTL0

Divider control register (for 16.5 divider)

Address: 0x40010400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		R
HW Access	R					None		RW
Name	FRAC5_DIV [7:3]					None [2:1]		EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INT16_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INT16_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 8	INT16_DIV	Integer division by (1+INT16_DIV). Allows for integer divisions in the range [1, 65,536]. Note: combined with fractional division, this divider type allows for a division in the range [1, 65,536 31/32] in 1/32 increments. For the generation of a divided clock, the division range is restricted to [2, 65,536 31/32]. For the generation of a 50/50% duty cycle divided clock, the division range is restricted to [2, 65,536]. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0
7 : 3	FRAC5_DIV	Fractional division by (FRAC5_DIV/32). Allows for fractional divisions in the range [0, 31/32]. Note that fractional division results in clock jitter as some clock periods may be 1 "clk_hf" cycle longer than other clock periods. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0

(continued)

0	EN	Divider enabled. HW sets this field to '1' as a result of an ENABLE command. HW sets this field to '0' as a result on a DISABLE command. Note that this field is retained. As a result, the divider does NOT have to be re-enabled after transitioning from DeepSleep to Active power mode. Default Value: 0

24.1.29 PERI_DIV_16_5_CTL1

Divider control register (for 16.5 divider)

Address: 0x40010404

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		R
HW Access	R					None		RW
Name	FRAC5_DIV [7:3]					None [2:1]		EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INT16_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INT16_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 8	INT16_DIV	Integer division by (1+INT16_DIV). Allows for integer divisions in the range [1, 65,536]. Note: combined with fractional division, this divider type allows for a division in the range [1, 65,536 31/32] in 1/32 increments. For the generation of a divided clock, the division range is restricted to [2, 65,536 31/32]. For the generation of a 50/50% duty cycle divided clock, the division range is restricted to [2, 65,536]. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0
7 : 3	FRAC5_DIV	Fractional division by (FRAC5_DIV/32). Allows for fractional divisions in the range [0, 31/32]. Note that fractional division results in clock jitter as some clock periods may be 1 "clk_hf" cycle longer than other clock periods. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0

(continued)

0	EN	Divider enabled. HW sets this field to '1' as a result of an ENABLE command. HW sets this field to '0' as a result on a DISABLE command. Note that this field is retained. As a result, the divider does NOT have to be re-enabled after transitioning from DeepSleep to Active power mode. Default Value: 0

25 ROM Table Registers

This section discusses the ROM Table registers. It lists all the registers in mapping tables, in address order.

25.1 Register Details

Register Name	Address
ROMTABLE_ADDR	0xF0000000
ROMTABLE_DID	0xF0000FCC
ROMTABLE_PID4	0xF0000FD0
ROMTABLE_PID5	0xF0000FD4
ROMTABLE_PID6	0xF0000FD8
ROMTABLE_PID7	0xF0000FDC
ROMTABLE_PID0	0xF0000FE0
ROMTABLE_PID1	0xF0000FE4
ROMTABLE_PID2	0xF0000FE8
ROMTABLE_PID3	0xF0000FEC
ROMTABLE_CID0	0xF0000FF0
ROMTABLE_CID1	0xF0000FF4
ROMTABLE_CID2	0xF0000FF8
ROMTABLE_CID3	0xF0000FFC

25.1.1 ROMTABLE_ADDR

Link to Cortex M0 ROM Table.

Address: 0xF0000000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						R	R
Name	None [7:2]						FORMAT_32BIT	PRESENT

Bits	15	14	13	12	11	10	9	8
SW Access	R				None			
HW Access	R				None			
Name	ADDR_OFFSET [15:12]				None [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR_OFFSET [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR_OFFSET [31:24]							

Bits	Name	Description
31 : 12	ADDR_OFFSET	Address offset of the Cortex-M0 ROM Table base address (0xe00f:f000) wrt. Cypress chip specific ROM Table base address (0xf000:0000). ADDR_OFFSET[19:0] = 0xe00f:f - 0xf000:0 = 0xf00f:f. Default Value: 983295
1	FORMAT_32BIT	ROM Table format: '0: 8-bit format. '1': 32-bit format. Default Value: 1
0	PRESENT	Entry present. Default Value: 1

25.1.2 ROMTABLE_DID

Device Type Identifier register.

Address: 0xF0000FCC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	. Default Value: 1

25.1.3 ROMTABLE_PID4

Peripheral Identification Register 4.

Address: 0xF0000FD0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	R				R			
Name	COUNT [7:4]				JEP_CONTINUATION [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	COUNT	Size of ROM Table is 2^COUNT * 4 KByte. Default Value: 0
3 : 0	JEP_CONTINUATION	JEP106 continuation code. This value is product specific and specified as part of the product definition in the CPUSS.JEPCONTINUATION parameter. Default Value: Undefined

25.1.4 ROMTABLE_PID5

Peripheral Identification Register 5.

Address: 0xF0000FD4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	. Default Value: 0

25.1.5 ROMTABLE_PID6

Peripheral Identification Register 6.

Address: 0xF0000FD8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	. Default Value: 0

25.1.6 ROMTABLE_PID7

Peripheral Identification Register 7.

Address: 0xF0000FDC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	. Default Value: 0

25.1.7 ROMTABLE_PID0

Peripheral Identification Register 0.

Address: 0xF0000FE0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	PN_MIN [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	PN_MIN	JEP106 part number. 4 lsbs of CPUSS.PARTNUMBER parameter. These part numbers are maintained in spec 40-9500. Default Value: Undefined

25.1.8 ROMTABLE_PID1

Peripheral Identification Register 1.

Address: 0xF0000FE4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	R				R			
Name	JEPID_MIN [7:4]				PN_MAJ [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	JEPID_MIN	JEP106 vendor id. 4 lsbs of CPUSS.JEPID parameter. This number is maintained in spec 40-9500. Default Value: Undefined
3 : 0	PN_MAJ	JEP106 part number. 4 msbs of CPUSS.PARTNUMBER parameter. These part numbers are maintained in spec 40-9500. Default Value: Undefined

25.1.9 ROMTABLE_PID2

Peripheral Identification Register 2.

Address: 0xF0000FE8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				None	R		
HW Access	R				None	R		
Name	REV [7:4]				None	JEPID_MAJ [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	REV	Major REVision number (chip specific). Identifies the design iteration of the component. For first tape out: 0x1. This field is implemented in RTL by an ECO-able tie-off structure and is incremented on subsequent tape outs. Default Value: Undefined
2 : 0	JEPID_MAJ	JEP106 vendor id. 4 msbs of CPUSS.JEPID parameter. This number is maintained in spec 40-9500. Default Value: Undefined

25.1.10 ROMTABLE_PID3

Peripheral Identification Register 3.

Address: 0xF0000FEC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	R				R			
Name	REV_AND [7:4]				CM [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	REV_AND	Minor REVision number (chip specific). For first tape out: 0x1. This field is implemented in RTL by an ECO-able tie-off structure and is incremented on subsequent tape outs. Default Value: Undefined
3 : 0	CM	Customer modified field. This field is used to track modifications to the original component design as a result of componenet IP reuse. Default Value: 0

25.1.11 ROMTABLE_CID0

Component Identification Register 0.

Address: 0xF0000FF0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component identification byte 0 of 4-byte component identification 0xB105:100D. Default Value: 13

25.1.12 ROMTABLE_CID1

Component Identification Register 1.

Address: 0xF0000FF4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component identification byte 1 of 4-byte component identification 0xB105:100D. Component class: "ROM Table". Default Value: 16

25.1.13 ROMTABLE_CID2

Component Identification Register 2.

Address: 0xF0000FF8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component identification byte 2 of 4-byte component identification 0xB105:100D. Default Value: 5

25.1.14 ROMTABLE_CID3

Component Identification Register 3.

Address: 0xF0000FFC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component identification byte 3 of 4-byte component identification 0xB105:100D. Default Value: 177

26 ROUTE Registers

This section discusses the ROUTE registers. It lists all the registers in mapping tables, in address order.

26.1 Register Details

Register Name	Address
UDB_P0_ROUTE_HC0	0x400F3100
UDB_P0_ROUTE_HC1	0x400F3101
UDB_P0_ROUTE_HC2	0x400F3102
UDB_P0_ROUTE_HC3	0x400F3103
UDB_P0_ROUTE_HC4	0x400F3104
UDB_P0_ROUTE_HC5	0x400F3105
UDB_P0_ROUTE_HC6	0x400F3106
UDB_P0_ROUTE_HC7	0x400F3107
UDB_P0_ROUTE_HC8	0x400F3108
UDB_P0_ROUTE_HC9	0x400F3109
UDB_P0_ROUTE_HC10	0x400F310A
UDB_P0_ROUTE_HC11	0x400F310B
UDB_P0_ROUTE_HC12	0x400F310C
UDB_P0_ROUTE_HC13	0x400F310D
UDB_P0_ROUTE_HC14	0x400F310E
UDB_P0_ROUTE_HC15	0x400F310F
UDB_P0_ROUTE_HC16	0x400F3110
UDB_P0_ROUTE_HC17	0x400F3111
UDB_P0_ROUTE_HC18	0x400F3112
UDB_P0_ROUTE_HC19	0x400F3113
UDB_P0_ROUTE_HC20	0x400F3114
UDB_P0_ROUTE_HC21	0x400F3115
UDB_P0_ROUTE_HC22	0x400F3116
UDB_P0_ROUTE_HC23	0x400F3117
UDB_P0_ROUTE_HC24	0x400F3118
UDB_P0_ROUTE_HC25	0x400F3119

Register Name	Address
UDB_P0_ROUTE_HC26	0x400F311A
UDB_P0_ROUTE_HC27	0x400F311B
UDB_P0_ROUTE_HC28	0x400F311C
UDB_P0_ROUTE_HC29	0x400F311D
UDB_P0_ROUTE_HC30	0x400F311E
UDB_P0_ROUTE_HC31	0x400F311F
UDB_P0_ROUTE_HC32	0x400F3120
UDB_P0_ROUTE_HC33	0x400F3121
UDB_P0_ROUTE_HC34	0x400F3122
UDB_P0_ROUTE_HC35	0x400F3123
UDB_P0_ROUTE_HC36	0x400F3124
UDB_P0_ROUTE_HC37	0x400F3125
UDB_P0_ROUTE_HC38	0x400F3126
UDB_P0_ROUTE_HC39	0x400F3127
UDB_P0_ROUTE_HC40	0x400F3128
UDB_P0_ROUTE_HC41	0x400F3129
UDB_P0_ROUTE_HC42	0x400F312A
UDB_P0_ROUTE_HC43	0x400F312B
UDB_P0_ROUTE_HC44	0x400F312C
UDB_P0_ROUTE_HC45	0x400F312D
UDB_P0_ROUTE_HC46	0x400F312E
UDB_P0_ROUTE_HC47	0x400F312F
UDB_P0_ROUTE_HC48	0x400F3130
UDB_P0_ROUTE_HC49	0x400F3131
UDB_P0_ROUTE_HC50	0x400F3132
UDB_P0_ROUTE_HC51	0x400F3133
UDB_P0_ROUTE_HC52	0x400F3134
UDB_P0_ROUTE_HC53	0x400F3135
UDB_P0_ROUTE_HC54	0x400F3136
UDB_P0_ROUTE_HC55	0x400F3137
UDB_P0_ROUTE_HC56	0x400F3138
UDB_P0_ROUTE_HC57	0x400F3139
UDB_P0_ROUTE_HC58	0x400F313A
UDB_P0_ROUTE_HC59	0x400F313B
UDB_P0_ROUTE_HC60	0x400F313C
UDB_P0_ROUTE_HC61	0x400F313D
UDB_P0_ROUTE_HC62	0x400F313E
UDB_P0_ROUTE_HC63	0x400F313F
UDB_P0_ROUTE_HC64	0x400F3140
UDB_P0_ROUTE_HC65	0x400F3141

Register Name	Address
UDB_P0_ROUTE_HC66	0x400F3142
UDB_P0_ROUTE_HC67	0x400F3143
UDB_P0_ROUTE_HC68	0x400F3144
UDB_P0_ROUTE_HC69	0x400F3145
UDB_P0_ROUTE_HC70	0x400F3146
UDB_P0_ROUTE_HC71	0x400F3147
UDB_P0_ROUTE_HC72	0x400F3148
UDB_P0_ROUTE_HC73	0x400F3149
UDB_P0_ROUTE_HC74	0x400F314A
UDB_P0_ROUTE_HC75	0x400F314B
UDB_P0_ROUTE_HC76	0x400F314C
UDB_P0_ROUTE_HC77	0x400F314D
UDB_P0_ROUTE_HC78	0x400F314E
UDB_P0_ROUTE_HC79	0x400F314F
UDB_P0_ROUTE_HC80	0x400F3150
UDB_P0_ROUTE_HC81	0x400F3151
UDB_P0_ROUTE_HC82	0x400F3152
UDB_P0_ROUTE_HC83	0x400F3153
UDB_P0_ROUTE_HC84	0x400F3154
UDB_P0_ROUTE_HC85	0x400F3155
UDB_P0_ROUTE_HC86	0x400F3156
UDB_P0_ROUTE_HC87	0x400F3157
UDB_P0_ROUTE_HC88	0x400F3158
UDB_P0_ROUTE_HC89	0x400F3159
UDB_P0_ROUTE_HC90	0x400F315A
UDB_P0_ROUTE_HC91	0x400F315B
UDB_P0_ROUTE_HC92	0x400F315C
UDB_P0_ROUTE_HC93	0x400F315D
UDB_P0_ROUTE_HC94	0x400F315E
UDB_P0_ROUTE_HC95	0x400F315F
UDB_P0_ROUTE_HC96	0x400F3160
UDB_P0_ROUTE_HC97	0x400F3161
UDB_P0_ROUTE_HC98	0x400F3162
UDB_P0_ROUTE_HC99	0x400F3163
UDB_P0_ROUTE_HC100	0x400F3164
UDB_P0_ROUTE_HC101	0x400F3165
UDB_P0_ROUTE_HC102	0x400F3166
UDB_P0_ROUTE_HC103	0x400F3167
UDB_P0_ROUTE_HC104	0x400F3168
UDB_P0_ROUTE_HC105	0x400F3169

Register Name	Address
UDB_P0_ROUTE_HC106	0x400F316A
UDB_P0_ROUTE_HC107	0x400F316B
UDB_P0_ROUTE_HC108	0x400F316C
UDB_P0_ROUTE_HC109	0x400F316D
UDB_P0_ROUTE_HC110	0x400F316E
UDB_P0_ROUTE_HC111	0x400F316F
UDB_P0_ROUTE_HC112	0x400F3170
UDB_P0_ROUTE_HC113	0x400F3171
UDB_P0_ROUTE_HC114	0x400F3172
UDB_P0_ROUTE_HC115	0x400F3173
UDB_P0_ROUTE_HC116	0x400F3174
UDB_P0_ROUTE_HC117	0x400F3175
UDB_P0_ROUTE_HC118	0x400F3176
UDB_P0_ROUTE_HC119	0x400F3177
UDB_P0_ROUTE_HC120	0x400F3178
UDB_P0_ROUTE_HC121	0x400F3179
UDB_P0_ROUTE_HC122	0x400F317A
UDB_P0_ROUTE_HC123	0x400F317B
UDB_P0_ROUTE_HC124	0x400F317C
UDB_P0_ROUTE_HC125	0x400F317D
UDB_P0_ROUTE_HC126	0x400F317E
UDB_P0_ROUTE_HC127	0x400F317F
UDB_P0_ROUTE_HV_L0	0x400F3180
UDB_P0_ROUTE_HV_L1	0x400F3181
UDB_P0_ROUTE_HV_L2	0x400F3182
UDB_P0_ROUTE_HV_L3	0x400F3183
UDB_P0_ROUTE_HV_L4	0x400F3184
UDB_P0_ROUTE_HV_L5	0x400F3185
UDB_P0_ROUTE_HV_L6	0x400F3186
UDB_P0_ROUTE_HV_L7	0x400F3187
UDB_P0_ROUTE_HV_L8	0x400F3188
UDB_P0_ROUTE_HV_L9	0x400F3189
UDB_P0_ROUTE_HV_L10	0x400F318A
UDB_P0_ROUTE_HV_L11	0x400F318B
UDB_P0_ROUTE_HV_L12	0x400F318C
UDB_P0_ROUTE_HV_L13	0x400F318D
UDB_P0_ROUTE_HV_L14	0x400F318E
UDB_P0_ROUTE_HV_L15	0x400F318F
UDB_P0_ROUTE_HS0	0x400F3190
UDB_P0_ROUTE_HS1	0x400F3191

Register Name	Address
UDB_P0_ROUTE_HS2	0x400F3192
UDB_P0_ROUTE_HS3	0x400F3193
UDB_P0_ROUTE_HS4	0x400F3194
UDB_P0_ROUTE_HS5	0x400F3195
UDB_P0_ROUTE_HS6	0x400F3196
UDB_P0_ROUTE_HS7	0x400F3197
UDB_P0_ROUTE_HS8	0x400F3198
UDB_P0_ROUTE_HS9	0x400F3199
UDB_P0_ROUTE_HS10	0x400F319A
UDB_P0_ROUTE_HS11	0x400F319B
UDB_P0_ROUTE_HS12	0x400F319C
UDB_P0_ROUTE_HS13	0x400F319D
UDB_P0_ROUTE_HS14	0x400F319E
UDB_P0_ROUTE_HS15	0x400F319F
UDB_P0_ROUTE_HS16	0x400F31A0
UDB_P0_ROUTE_HS17	0x400F31A1
UDB_P0_ROUTE_HS18	0x400F31A2
UDB_P0_ROUTE_HS19	0x400F31A3
UDB_P0_ROUTE_HS20	0x400F31A4
UDB_P0_ROUTE_HS21	0x400F31A5
UDB_P0_ROUTE_HS22	0x400F31A6
UDB_P0_ROUTE_HS23	0x400F31A7
UDB_P0_ROUTE_HV_R0	0x400F31A8
UDB_P0_ROUTE_HV_R1	0x400F31A9
UDB_P0_ROUTE_HV_R2	0x400F31AA
UDB_P0_ROUTE_HV_R3	0x400F31AB
UDB_P0_ROUTE_HV_R4	0x400F31AC
UDB_P0_ROUTE_HV_R5	0x400F31AD
UDB_P0_ROUTE_HV_R6	0x400F31AE
UDB_P0_ROUTE_HV_R7	0x400F31AF
UDB_P0_ROUTE_HV_R8	0x400F31B0
UDB_P0_ROUTE_HV_R9	0x400F31B1
UDB_P0_ROUTE_HV_R10	0x400F31B2
UDB_P0_ROUTE_HV_R11	0x400F31B3
UDB_P0_ROUTE_HV_R12	0x400F31B4
UDB_P0_ROUTE_HV_R13	0x400F31B5
UDB_P0_ROUTE_HV_R14	0x400F31B6
UDB_P0_ROUTE_HV_R15	0x400F31B7
UDB_P0_ROUTE_PLD0IN0	0x400F31C0
UDB_P0_ROUTE_PLD0IN1	0x400F31C2

Register Name	Address
UDB_P0_ROUTE_PLD0IN2	0x400F31C4
UDB_P0_ROUTE_PLD1IN0	0x400F31CA
UDB_P0_ROUTE_PLD1IN1	0x400F31CC
UDB_P0_ROUTE_PLD1IN2	0x400F31CE
UDB_P0_ROUTE_DPIN0	0x400F31D0
UDB_P0_ROUTE_DPIN1	0x400F31D2
UDB_P0_ROUTE_SCIN	0x400F31D6
UDB_P0_ROUTE_SCIOIN	0x400F31D8
UDB_P0_ROUTE_RCIN	0x400F31DE
UDB_P0_ROUTE_VS0	0x400F31E0
UDB_P0_ROUTE_VS1	0x400F31E2
UDB_P0_ROUTE_VS2	0x400F31E4
UDB_P0_ROUTE_VS3	0x400F31E6
UDB_P0_ROUTE_VS4	0x400F31E8
UDB_P0_ROUTE_VS5	0x400F31EA
UDB_P0_ROUTE_VS6	0x400F31EC
UDB_P0_ROUTE_VS7	0x400F31EE
UDB_P1_ROUTE_HC0	0x400F3300
UDB_P1_ROUTE_HC1	0x400F3301
UDB_P1_ROUTE_HC2	0x400F3302
UDB_P1_ROUTE_HC3	0x400F3303
UDB_P1_ROUTE_HC4	0x400F3304
UDB_P1_ROUTE_HC5	0x400F3305
UDB_P1_ROUTE_HC6	0x400F3306
UDB_P1_ROUTE_HC7	0x400F3307
UDB_P1_ROUTE_HC8	0x400F3308
UDB_P1_ROUTE_HC9	0x400F3309
UDB_P1_ROUTE_HC10	0x400F330A
UDB_P1_ROUTE_HC11	0x400F330B
UDB_P1_ROUTE_HC12	0x400F330C
UDB_P1_ROUTE_HC13	0x400F330D
UDB_P1_ROUTE_HC14	0x400F330E
UDB_P1_ROUTE_HC15	0x400F330F
UDB_P1_ROUTE_HC16	0x400F3310
UDB_P1_ROUTE_HC17	0x400F3311
UDB_P1_ROUTE_HC18	0x400F3312
UDB_P1_ROUTE_HC19	0x400F3313
UDB_P1_ROUTE_HC20	0x400F3314
UDB_P1_ROUTE_HC21	0x400F3315
UDB_P1_ROUTE_HC22	0x400F3316

Register Name	Address
UDB_P1_ROUTE_HC23	0x400F3317
UDB_P1_ROUTE_HC24	0x400F3318
UDB_P1_ROUTE_HC25	0x400F3319
UDB_P1_ROUTE_HC26	0x400F331A
UDB_P1_ROUTE_HC27	0x400F331B
UDB_P1_ROUTE_HC28	0x400F331C
UDB_P1_ROUTE_HC29	0x400F331D
UDB_P1_ROUTE_HC30	0x400F331E
UDB_P1_ROUTE_HC31	0x400F331F
UDB_P1_ROUTE_HC32	0x400F3320
UDB_P1_ROUTE_HC33	0x400F3321
UDB_P1_ROUTE_HC34	0x400F3322
UDB_P1_ROUTE_HC35	0x400F3323
UDB_P1_ROUTE_HC36	0x400F3324
UDB_P1_ROUTE_HC37	0x400F3325
UDB_P1_ROUTE_HC38	0x400F3326
UDB_P1_ROUTE_HC39	0x400F3327
UDB_P1_ROUTE_HC40	0x400F3328
UDB_P1_ROUTE_HC41	0x400F3329
UDB_P1_ROUTE_HC42	0x400F332A
UDB_P1_ROUTE_HC43	0x400F332B
UDB_P1_ROUTE_HC44	0x400F332C
UDB_P1_ROUTE_HC45	0x400F332D
UDB_P1_ROUTE_HC46	0x400F332E
UDB_P1_ROUTE_HC47	0x400F332F
UDB_P1_ROUTE_HC48	0x400F3330
UDB_P1_ROUTE_HC49	0x400F3331
UDB_P1_ROUTE_HC50	0x400F3332
UDB_P1_ROUTE_HC51	0x400F3333
UDB_P1_ROUTE_HC52	0x400F3334
UDB_P1_ROUTE_HC53	0x400F3335
UDB_P1_ROUTE_HC54	0x400F3336
UDB_P1_ROUTE_HC55	0x400F3337
UDB_P1_ROUTE_HC56	0x400F3338
UDB_P1_ROUTE_HC57	0x400F3339
UDB_P1_ROUTE_HC58	0x400F333A
UDB_P1_ROUTE_HC59	0x400F333B
UDB_P1_ROUTE_HC60	0x400F333C
UDB_P1_ROUTE_HC61	0x400F333D
UDB_P1_ROUTE_HC62	0x400F333E

Register Name	Address
UDB_P1_ROUTE_HC63	0x400F333F
UDB_P1_ROUTE_HC64	0x400F3340
UDB_P1_ROUTE_HC65	0x400F3341
UDB_P1_ROUTE_HC66	0x400F3342
UDB_P1_ROUTE_HC67	0x400F3343
UDB_P1_ROUTE_HC68	0x400F3344
UDB_P1_ROUTE_HC69	0x400F3345
UDB_P1_ROUTE_HC70	0x400F3346
UDB_P1_ROUTE_HC71	0x400F3347
UDB_P1_ROUTE_HC72	0x400F3348
UDB_P1_ROUTE_HC73	0x400F3349
UDB_P1_ROUTE_HC74	0x400F334A
UDB_P1_ROUTE_HC75	0x400F334B
UDB_P1_ROUTE_HC76	0x400F334C
UDB_P1_ROUTE_HC77	0x400F334D
UDB_P1_ROUTE_HC78	0x400F334E
UDB_P1_ROUTE_HC79	0x400F334F
UDB_P1_ROUTE_HC80	0x400F3350
UDB_P1_ROUTE_HC81	0x400F3351
UDB_P1_ROUTE_HC82	0x400F3352
UDB_P1_ROUTE_HC83	0x400F3353
UDB_P1_ROUTE_HC84	0x400F3354
UDB_P1_ROUTE_HC85	0x400F3355
UDB_P1_ROUTE_HC86	0x400F3356
UDB_P1_ROUTE_HC87	0x400F3357
UDB_P1_ROUTE_HC88	0x400F3358
UDB_P1_ROUTE_HC89	0x400F3359
UDB_P1_ROUTE_HC90	0x400F335A
UDB_P1_ROUTE_HC91	0x400F335B
UDB_P1_ROUTE_HC92	0x400F335C
UDB_P1_ROUTE_HC93	0x400F335D
UDB_P1_ROUTE_HC94	0x400F335E
UDB_P1_ROUTE_HC95	0x400F335F
UDB_P1_ROUTE_HC96	0x400F3360
UDB_P1_ROUTE_HC97	0x400F3361
UDB_P1_ROUTE_HC98	0x400F3362
UDB_P1_ROUTE_HC99	0x400F3363
UDB_P1_ROUTE_HC100	0x400F3364
UDB_P1_ROUTE_HC101	0x400F3365
UDB_P1_ROUTE_HC102	0x400F3366

Register Name	Address
UDB_P1_ROUTE_HC103	0x400F3367
UDB_P1_ROUTE_HC104	0x400F3368
UDB_P1_ROUTE_HC105	0x400F3369
UDB_P1_ROUTE_HC106	0x400F336A
UDB_P1_ROUTE_HC107	0x400F336B
UDB_P1_ROUTE_HC108	0x400F336C
UDB_P1_ROUTE_HC109	0x400F336D
UDB_P1_ROUTE_HC110	0x400F336E
UDB_P1_ROUTE_HC111	0x400F336F
UDB_P1_ROUTE_HC112	0x400F3370
UDB_P1_ROUTE_HC113	0x400F3371
UDB_P1_ROUTE_HC114	0x400F3372
UDB_P1_ROUTE_HC115	0x400F3373
UDB_P1_ROUTE_HC116	0x400F3374
UDB_P1_ROUTE_HC117	0x400F3375
UDB_P1_ROUTE_HC118	0x400F3376
UDB_P1_ROUTE_HC119	0x400F3377
UDB_P1_ROUTE_HC120	0x400F3378
UDB_P1_ROUTE_HC121	0x400F3379
UDB_P1_ROUTE_HC122	0x400F337A
UDB_P1_ROUTE_HC123	0x400F337B
UDB_P1_ROUTE_HC124	0x400F337C
UDB_P1_ROUTE_HC125	0x400F337D
UDB_P1_ROUTE_HC126	0x400F337E
UDB_P1_ROUTE_HC127	0x400F337F
UDB_P1_ROUTE_HV_L0	0x400F3380
UDB_P1_ROUTE_HV_L1	0x400F3381
UDB_P1_ROUTE_HV_L2	0x400F3382
UDB_P1_ROUTE_HV_L3	0x400F3383
UDB_P1_ROUTE_HV_L4	0x400F3384
UDB_P1_ROUTE_HV_L5	0x400F3385
UDB_P1_ROUTE_HV_L6	0x400F3386
UDB_P1_ROUTE_HV_L7	0x400F3387
UDB_P1_ROUTE_HV_L8	0x400F3388
UDB_P1_ROUTE_HV_L9	0x400F3389
UDB_P1_ROUTE_HV_L10	0x400F338A
UDB_P1_ROUTE_HV_L11	0x400F338B
UDB_P1_ROUTE_HV_L12	0x400F338C
UDB_P1_ROUTE_HV_L13	0x400F338D
UDB_P1_ROUTE_HV_L14	0x400F338E

Register Name	Address
UDB_P1_ROUTE_HV_L15	0x400F338F
UDB_P1_ROUTE_HS0	0x400F3390
UDB_P1_ROUTE_HS1	0x400F3391
UDB_P1_ROUTE_HS2	0x400F3392
UDB_P1_ROUTE_HS3	0x400F3393
UDB_P1_ROUTE_HS4	0x400F3394
UDB_P1_ROUTE_HS5	0x400F3395
UDB_P1_ROUTE_HS6	0x400F3396
UDB_P1_ROUTE_HS7	0x400F3397
UDB_P1_ROUTE_HS8	0x400F3398
UDB_P1_ROUTE_HS9	0x400F3399
UDB_P1_ROUTE_HS10	0x400F339A
UDB_P1_ROUTE_HS11	0x400F339B
UDB_P1_ROUTE_HS12	0x400F339C
UDB_P1_ROUTE_HS13	0x400F339D
UDB_P1_ROUTE_HS14	0x400F339E
UDB_P1_ROUTE_HS15	0x400F339F
UDB_P1_ROUTE_HS16	0x400F33A0
UDB_P1_ROUTE_HS17	0x400F33A1
UDB_P1_ROUTE_HS18	0x400F33A2
UDB_P1_ROUTE_HS19	0x400F33A3
UDB_P1_ROUTE_HS20	0x400F33A4
UDB_P1_ROUTE_HS21	0x400F33A5
UDB_P1_ROUTE_HS22	0x400F33A6
UDB_P1_ROUTE_HS23	0x400F33A7
UDB_P1_ROUTE_HV_R0	0x400F33A8
UDB_P1_ROUTE_HV_R1	0x400F33A9
UDB_P1_ROUTE_HV_R2	0x400F33AA
UDB_P1_ROUTE_HV_R3	0x400F33AB
UDB_P1_ROUTE_HV_R4	0x400F33AC
UDB_P1_ROUTE_HV_R5	0x400F33AD
UDB_P1_ROUTE_HV_R6	0x400F33AE
UDB_P1_ROUTE_HV_R7	0x400F33AF
UDB_P1_ROUTE_HV_R8	0x400F33B0
UDB_P1_ROUTE_HV_R9	0x400F33B1
UDB_P1_ROUTE_HV_R10	0x400F33B2
UDB_P1_ROUTE_HV_R11	0x400F33B3
UDB_P1_ROUTE_HV_R12	0x400F33B4
UDB_P1_ROUTE_HV_R13	0x400F33B5
UDB_P1_ROUTE_HV_R14	0x400F33B6

Register Name	Address
UDB_P1_ROUTE_HV_R15	0x400F33B7
UDB_P1_ROUTE_PLD0IN0	0x400F33C0
UDB_P1_ROUTE_PLD0IN1	0x400F33C2
UDB_P1_ROUTE_PLD0IN2	0x400F33C4
UDB_P1_ROUTE_PLD1IN0	0x400F33CA
UDB_P1_ROUTE_PLD1IN1	0x400F33CC
UDB_P1_ROUTE_PLD1IN2	0x400F33CE
UDB_P1_ROUTE_DPIN0	0x400F33D0
UDB_P1_ROUTE_DPIN1	0x400F33D2
UDB_P1_ROUTE_SCIN	0x400F33D6
UDB_P1_ROUTE_SCIOIN	0x400F33D8
UDB_P1_ROUTE_RCIN	0x400F33DE
UDB_P1_ROUTE_VS0	0x400F33E0
UDB_P1_ROUTE_VS1	0x400F33E2
UDB_P1_ROUTE_VS2	0x400F33E4
UDB_P1_ROUTE_VS3	0x400F33E6
UDB_P1_ROUTE_VS4	0x400F33E8
UDB_P1_ROUTE_VS5	0x400F33EA
UDB_P1_ROUTE_VS6	0x400F33EC
UDB_P1_ROUTE_VS7	0x400F33EE

26.1.1 UDB_P0_ROUTE_HC0

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.2 UDB_P0_ROUTE_HC1

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3101

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.3 UDB_P0_ROUTE_HC2

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3102

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.4 UDB_P0_ROUTE_HC3

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3103

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.5 UDB_P0_ROUTE_HC4

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3104

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.6 UDB_P0_ROUTE_HC5

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3105

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.7 UDB_P0_ROUTE_HC6

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3106

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.8 UDB_P0_ROUTE_HC7

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3107

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.9 UDB_P0_ROUTE_HC8

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3108

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.10 UDB_P0_ROUTE_HC9

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3109

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.11 UDB_P0_ROUTE_HC10

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F310A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.12 UDB_P0_ROUTE_HC11

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F310B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.13 UDB_P0_ROUTE_HC12

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F310C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.14 UDB_P0_ROUTE_HC13

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F310D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.15 UDB_P0_ROUTE_HC14

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F310E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.16 UDB_P0_ROUTE_HC15

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F310F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.17 UDB_P0_ROUTE_HC16

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3110

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.18 UDB_P0_ROUTE_HC17

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3111

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.19 UDB_P0_ROUTE_HC18

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3112

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.20 UDB_P0_ROUTE_HC19

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3113

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.21 UDB_P0_ROUTE_HC20

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3114

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.22 UDB_P0_ROUTE_HC21

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3115

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.23 UDB_P0_ROUTE_HC22

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3116

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.24 UDB_P0_ROUTE_HC23

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3117

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.25 UDB_P0_ROUTE_HC24

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3118

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.26 UDB_P0_ROUTE_HC25

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3119

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.27 UDB_P0_ROUTE_HC26

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F311A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.28 UDB_P0_ROUTE_HC27

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F311B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.29 UDB_P0_ROUTE_HC28

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F311C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.30 UDB_P0_ROUTE_HC29

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F311D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.31 UDB_P0_ROUTE_HC30

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F311E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.32 UDB_P0_ROUTE_HC31

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F311F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.33 UDB_P0_ROUTE_HC32

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3120

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.34 UDB_P0_ROUTE_HC33

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3121

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.35 UDB_P0_ROUTE_HC34

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3122

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.36 UDB_P0_ROUTE_HC35

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3123

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.37 UDB_P0_ROUTE_HC36

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3124

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.38 UDB_P0_ROUTE_HC37

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3125

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.39 UDB_P0_ROUTE_HC38

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3126

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.40 UDB_P0_ROUTE_HC39

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3127

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.41 UDB_P0_ROUTE_HC40

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3128

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.42 UDB_P0_ROUTE_HC41

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3129

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.43 UDB_P0_ROUTE_HC42

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F312A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.44 UDB_P0_ROUTE_HC43

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F312B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.45 UDB_P0_ROUTE_HC44

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F312C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.46 UDB_P0_ROUTE_HC45

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F312D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.47 UDB_P0_ROUTE_HC46

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F312E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.48 UDB_P0_ROUTE_HC47

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F312F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.49 UDB_P0_ROUTE_HC48

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3130

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.50 UDB_P0_ROUTE_HC49

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3131

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.51 UDB_P0_ROUTE_HC50

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3132

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.52 UDB_P0_ROUTE_HC51

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3133

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.53 UDB_P0_ROUTE_HC52

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3134

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.54 UDB_P0_ROUTE_HC53

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3135

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.55 UDB_P0_ROUTE_HC54

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3136

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.56 UDB_P0_ROUTE_HC55

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3137

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.57 UDB_P0_ROUTE_HC56

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3138

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.58 UDB_P0_ROUTE_HC57

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3139

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.59 UDB_P0_ROUTE_HC58

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F313A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.60 UDB_P0_ROUTE_HC59

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F313B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.61 UDB_P0_ROUTE_HC60

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F313C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.62 UDB_P0_ROUTE_HC61

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F313D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.63 UDB_P0_ROUTE_HC62

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F313E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.64 UDB_P0_ROUTE_HC63

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F313F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.65 UDB_P0_ROUTE_HC64

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3140

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.66 UDB_P0_ROUTE_HC65

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3141

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.67 UDB_P0_ROUTE_HC66

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3142

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.68 UDB_P0_ROUTE_HC67

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3143

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.69 UDB_P0_ROUTE_HC68

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3144

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.70 UDB_P0_ROUTE_HC69

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3145

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.71 UDB_P0_ROUTE_HC70

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3146

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.72 UDB_P0_ROUTE_HC71

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3147

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.73 UDB_P0_ROUTE_HC72

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3148

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.74 UDB_P0_ROUTE_HC73

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3149

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.75 UDB_P0_ROUTE_HC74

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F314A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.76 UDB_P0_ROUTE_HC75

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F314B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.77 UDB_P0_ROUTE_HC76

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F314C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.78 UDB_P0_ROUTE_HC77

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F314D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.79 UDB_P0_ROUTE_HC78

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F314E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.80 UDB_P0_ROUTE_HC79

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F314F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.81 UDB_P0_ROUTE_HC80

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3150

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.82 UDB_P0_ROUTE_HC81

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3151

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.83 UDB_P0_ROUTE_HC82

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3152

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.84 UDB_P0_ROUTE_HC83

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3153

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.85 UDB_P0_ROUTE_HC84

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3154

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.86 UDB_P0_ROUTE_HC85

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3155

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.87 UDB_P0_ROUTE_HC86

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3156

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.88 UDB_P0_ROUTE_HC87

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3157

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.89 UDB_P0_ROUTE_HC88

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3158

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.90 UDB_P0_ROUTE_HC89

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3159

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.91 UDB_P0_ROUTE_HC90

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F315A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.92 UDB_P0_ROUTE_HC91

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F315B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.93 UDB_P0_ROUTE_HC92

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F315C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.94 UDB_P0_ROUTE_HC93

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F315D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.95 UDB_P0_ROUTE_HC94

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F315E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.96 UDB_P0_ROUTE_HC95

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F315F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.97 UDB_P0_ROUTE_HC96

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3160

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.98 UDB_P0_ROUTE_HC97

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3161

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.99 UDB_P0_ROUTE_HC98

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3162

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.100 UDB_P0_ROUTE_HC99

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3163

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.101 UDB_P0_ROUTE_HC100

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3164

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.102 UDB_P0_ROUTE_HC101

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3165

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.103 UDB_P0_ROUTE_HC102

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3166

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.104 UDB_P0_ROUTE_HC103

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3167

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.105 UDB_P0_ROUTE_HC104

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3168

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.106 UDB_P0_ROUTE_HC105

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3169

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.107 UDB_P0_ROUTE_HC106

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F316A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.108 UDB_P0_ROUTE_HC107

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F316B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.109 UDB_P0_ROUTE_HC108

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F316C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.110 UDB_P0_ROUTE_HC109

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F316D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.111 UDB_P0_ROUTE_HC110

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F316E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.112 UDB_P0_ROUTE_HC111

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F316F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.113 UDB_P0_ROUTE_HC112

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3170

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.114 UDB_P0_ROUTE_HC113

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3171

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.115 UDB_P0_ROUTE_HC114

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3172

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.116 UDB_P0_ROUTE_HC115

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3173

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.117 UDB_P0_ROUTE_HC116

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3174

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.118 UDB_P0_ROUTE_HC117

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3175

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.119 UDB_P0_ROUTE_HC118

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3176

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.120 UDB_P0_ROUTE_HC119

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3177

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.121 UDB_P0_ROUTE_HC120

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3178

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.122 UDB_P0_ROUTE_HC121

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3179

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.123 UDB_P0_ROUTE_HC122

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F317A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.124 UDB_P0_ROUTE_HC123

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F317B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.125 UDB_P0_ROUTE_HC124

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F317C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.126 UDB_P0_ROUTE_HC125

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F317D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.127 UDB_P0_ROUTE_HC126

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F317E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.128 UDB_P0_ROUTE_HC127

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F317F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.129 UDB_P0_ROUTE_HV_L0

UDB Channel HV Tile Configuration; Left

Address: 0x400F3180

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

26.1.130 UDB_P0_ROUTE_HV_L1

UDB Channel HV Tile Configuration; Left

Address: 0x400F3181

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

26.1.131 UDB_P0_ROUTE_HV_L2

UDB Channel HV Tile Configuration; Left

Address: 0x400F3182

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

26.1.132 UDB_P0_ROUTE_HV_L3

UDB Channel HV Tile Configuration; Left

Address: 0x400F3183

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

26.1.133 UDB_P0_ROUTE_HV_L4

UDB Channel HV Tile Configuration; Left

Address: 0x400F3184

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

26.1.134 UDB_P0_ROUTE_HV_L5

UDB Channel HV Tile Configuration; Left

Address: 0x400F3185

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

26.1.135 UDB_P0_ROUTE_HV_L6

UDB Channel HV Tile Configuration; Left

Address: 0x400F3186

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

26.1.136 UDB_P0_ROUTE_HV_L7

UDB Channel HV Tile Configuration; Left

Address: 0x400F3187

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

26.1.137 UDB_P0_ROUTE_HV_L8

UDB Channel HV Tile Configuration; Left

Address: 0x400F3188

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

26.1.138 UDB_P0_ROUTE_HV_L9

UDB Channel HV Tile Configuration; Left

Address: 0x400F3189

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

26.1.139 UDB_P0_ROUTE_HV_L10

UDB Channel HV Tile Configuration; Left

Address: 0x400F318A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

26.1.140 UDB_P0_ROUTE_HV_L11

UDB Channel HV Tile Configuration; Left

Address: 0x400F318B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

26.1.141 UDB_P0_ROUTE_HV_L12

UDB Channel HV Tile Configuration; Left

Address: 0x400F318C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

26.1.142 UDB_P0_ROUTE_HV_L13

UDB Channel HV Tile Configuration; Left

Address: 0x400F318D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

26.1.143 UDB_P0_ROUTE_HV_L14

UDB Channel HV Tile Configuration; Left

Address: 0x400F318E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

26.1.144 UDB_P0_ROUTE_HV_L15

UDB Channel HV Tile Configuration; Left

Address: 0x400F318F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

26.1.145 UDB_P0_ROUTE_HS0

UDB Channel HS Tile Configuration; Horizontal Segmentation

Address: 0x400F3190

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration bytes for channel Default Value: X

26.1.146 UDB_P0_ROUTE_HS1

UDB Channel HS Tile Configuration; Horizontal Segmentation

Address: 0x400F3191

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration bytes for channel Default Value: X

26.1.147 UDB_P0_ROUTE_HS2

UDB Channel HS Tile Configuration; Horizontal Segmentation

Address: 0x400F3192

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration bytes for channel Default Value: X

26.1.148 UDB_P0_ROUTE_HS3

UDB Channel HS Tile Configuration; Horizontal Segmentation

Address: 0x400F3193

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration bytes for channel Default Value: X

26.1.149 UDB_P0_ROUTE_HS4

UDB Channel HS Tile Configuration; Horizontal Segmentation

Address: 0x400F3194

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration bytes for channel Default Value: X

26.1.150 UDB_P0_ROUTE_HS5

UDB Channel HS Tile Configuration; Horizontal Segmentation

Address: 0x400F3195

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration bytes for channel Default Value: X

26.1.151 UDB_P0_ROUTE_HS6

UDB Channel HS Tile Configuration; Horizontal Segmentation

Address: 0x400F3196

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration bytes for channel Default Value: X

26.1.152 UDB_P0_ROUTE_HS7

UDB Channel HS Tile Configuration; Horizontal Segmentation

Address: 0x400F3197

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration bytes for channel Default Value: X

26.1.153 UDB_P0_ROUTE_HS8

UDB Channel HS Tile Configuration; Horizontal Segmentation

Address: 0x400F3198

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration bytes for channel Default Value: X

26.1.154 UDB_P0_ROUTE_HS9

UDB Channel HS Tile Configuration; Horizontal Segmentation

Address: 0x400F3199

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration bytes for channel Default Value: X

26.1.155 UDB_P0_ROUTE_HS10

UDB Channel HS Tile Configuration; Horizontal Segmentation

Address: 0x400F319A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration bytes for channel Default Value: X

26.1.156 UDB_P0_ROUTE_HS11

UDB Channel HS Tile Configuration; Horizontal Segmentation

Address: 0x400F319B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration bytes for channel Default Value: X

26.1.157 UDB_P0_ROUTE_HS12

UDB Channel HS Tile Configuration; Horizontal Segmentation

Address: 0x400F319C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration bytes for channel Default Value: X

26.1.158 UDB_P0_ROUTE_HS13

UDB Channel HS Tile Configuration; Horizontal Segmentation

Address: 0x400F319D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration bytes for channel Default Value: X

26.1.159 UDB_P0_ROUTE_HS14

UDB Channel HS Tile Configuration; Horizontal Segmentation

Address: 0x400F319E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration bytes for channel Default Value: X

26.1.160 UDB_P0_ROUTE_HS15

UDB Channel HS Tile Configuration; Horizontal Segmentation

Address: 0x400F319F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration bytes for channel Default Value: X

26.1.161 UDB_P0_ROUTE_HS16

UDB Channel HS Tile Configuration; Horizontal Segmentation

Address: 0x400F31A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration bytes for channel Default Value: X

26.1.162 UDB_P0_ROUTE_HS17

UDB Channel HS Tile Configuration; Horizontal Segmentation

Address: 0x400F31A1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration bytes for channel Default Value: X

26.1.163 UDB_P0_ROUTE_HS18

UDB Channel HS Tile Configuration; Horizontal Segmentation

Address: 0x400F31A2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration bytes for channel Default Value: X

26.1.164 UDB_P0_ROUTE_HS19

UDB Channel HS Tile Configuration; Horizontal Segmentation

Address: 0x400F31A3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration bytes for channel Default Value: X

26.1.165 UDB_P0_ROUTE_HS20

UDB Channel HS Tile Configuration; Horizontal Segmentation

Address: 0x400F31A4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration bytes for channel Default Value: X

26.1.166 UDB_P0_ROUTE_HS21

UDB Channel HS Tile Configuration; Horizontal Segmentation

Address: 0x400F31A5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration bytes for channel Default Value: X

26.1.167 UDB_P0_ROUTE_HS22

UDB Channel HS Tile Configuration; Horizontal Segmentation

Address: 0x400F31A6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration bytes for channel Default Value: X

26.1.168 UDB_P0_ROUTE_HS23

UDB Channel HS Tile Configuration; Horizontal Segmentation

Address: 0x400F31A7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration bytes for channel Default Value: X

26.1.169 UDB_P0_ROUTE_HV_R0

UDB Channel HV Tile Configuration; Right

Address: 0x400F31A8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

26.1.170 UDB_P0_ROUTE_HV_R1

UDB Channel HV Tile Configuration; Right

Address: 0x400F31A9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

26.1.171 UDB_P0_ROUTE_HV_R2

UDB Channel HV Tile Configuration; Right

Address: 0x400F31AA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

26.1.172 UDB_P0_ROUTE_HV_R3

UDB Channel HV Tile Configuration; Right

Address: 0x400F31AB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

26.1.173 UDB_P0_ROUTE_HV_R4

UDB Channel HV Tile Configuration; Right

Address: 0x400F31AC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

26.1.174 UDB_P0_ROUTE_HV_R5

UDB Channel HV Tile Configuration; Right

Address: 0x400F31AD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

26.1.175 UDB_P0_ROUTE_HV_R6

UDB Channel HV Tile Configuration; Right

Address: 0x400F31AE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

26.1.176 UDB_P0_ROUTE_HV_R7

UDB Channel HV Tile Configuration; Right

Address: 0x400F31AF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

26.1.177 UDB_P0_ROUTE_HV_R8

UDB Channel HV Tile Configuration; Right

Address: 0x400F31B0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

26.1.178 UDB_P0_ROUTE_HV_R9

UDB Channel HV Tile Configuration; Right

Address: 0x400F31B1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

26.1.179 UDB_P0_ROUTE_HV_R10

UDB Channel HV Tile Configuration; Right

Address: 0x400F31B2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

26.1.180 UDB_P0_ROUTE_HV_R11

UDB Channel HV Tile Configuration; Right

Address: 0x400F31B3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

26.1.181 UDB_P0_ROUTE_HV_R12

UDB Channel HV Tile Configuration; Right

Address: 0x400F31B4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

26.1.182 UDB_P0_ROUTE_HV_R13

UDB Channel HV Tile Configuration; Right

Address: 0x400F31B5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

26.1.183 UDB_P0_ROUTE_HV_R14

UDB Channel HV Tile Configuration; Right

Address: 0x400F31B6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

26.1.184 UDB_P0_ROUTE_HV_R15

UDB Channel HV Tile Configuration; Right

Address: 0x400F31B7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

26.1.185 UDB_P0_ROUTE_PLD0IN0

UDB Channel PI Tile Configuration; PLD Input

Address: 0x400F31C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration nibble for BOTTOM UDB port interface configuration Default Value: X
3 : 0	PI_TOP	RAM configuration nibble for TOP UDB port interface configuration Default Value: X

26.1.186 UDB_P0_ROUTE_PLD0IN1

UDB Channel PI Tile Configuration; PLD Input

Address: 0x400F31C2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration nibble for BOTTOM UDB port interface configuration Default Value: X
3 : 0	PI_TOP	RAM configuration nibble for TOP UDB port interface configuration Default Value: X

26.1.187 UDB_P0_ROUTE_PLD0IN2

UDB Channel PI Tile Configuration; PLD Input

Address: 0x400F31C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration nibble for BOTTOM UDB port interface configuration Default Value: X
3 : 0	PI_TOP	RAM configuration nibble for TOP UDB port interface configuration Default Value: X

26.1.188 UDB_P0_ROUTE_PLD1IN0

UDB Channel PI Tile Configuration; PLD Input

Address: 0x400F31CA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration nibble for BOTTOM UDB port interface configuration Default Value: X
3 : 0	PI_TOP	RAM configuration nibble for TOP UDB port interface configuration Default Value: X

26.1.189 UDB_P0_ROUTE_PLD1IN1

UDB Channel PI Tile Configuration; PLD Input

Address: 0x400F31CC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration nibble for BOTTOM UDB port interface configuration Default Value: X
3 : 0	PI_TOP	RAM configuration nibble for TOP UDB port interface configuration Default Value: X

26.1.190 UDB_P0_ROUTE_PLD1IN2

UDB Channel PI Tile Configuration; PLD Input

Address: 0x400F31CE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration nibble for BOTTOM UDB port interface configuration Default Value: X
3 : 0	PI_TOP	RAM configuration nibble for TOP UDB port interface configuration Default Value: X

26.1.191 UDB_P0_ROUTE_DPIN0

UDB Channel PI Tile Configuration; Datapath Input

Address: 0x400F31D0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration nibble for BOTTOM UDB port interface configuration Default Value: X
3 : 0	PI_TOP	RAM configuration nibble for TOP UDB port interface configuration Default Value: X

26.1.192 UDB_P0_ROUTE_DPIN1

UDB Channel PI Tile Configuration; Datapath Input

Address: 0x400F31D2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW		RW		None	
HW Access	None		R		R		None	
Name	None [7:6]		PI_BOT2 [5:4]		PI_TOP2 [3:2]		None [1:0]	

Bits	Name	Description
5 : 4	PI_BOT2	RAM configuration bits (2) for BOTTOM UDB port interface configuration Default Value: X
3 : 2	PI_TOP2	RAM configuration bits (2) for TOP UDB port interface configuration Default Value: X

26.1.193 UDB_P0_ROUTE_SCIN

UDB Channel PI Tile Configuration; Status / Control Blocks Input Control

Address: 0x400F31D6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration nibble for BOTTOM UDB port interface configuration Default Value: X
3 : 0	PI_TOP	RAM configuration nibble for TOP UDB port interface configuration Default Value: X

26.1.194 UDB_P0_ROUTE_SCIOIN

UDB Channel PI Tile Configuration; Status / Control Blocks Input / Output Control

Address: 0x400F31D8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration nibble for BOTTOM UDB port interface configuration Default Value: X
3 : 0	PI_TOP	RAM configuration nibble for TOP UDB port interface configuration Default Value: X

26.1.195 UDB_P0_ROUTE_RCIN

UDB Channel PI Tile Configuration; Reset and Clock Blocks Input Control

Address: 0x400F31DE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration nibble for BOTTOM UDB port interface configuration Default Value: X
3 : 0	PI_TOP	RAM configuration nibble for TOP UDB port interface configuration Default Value: X

26.1.196 UDB_P0_ROUTE_VS0

UDB Channel VS Tile Configuration; Vertical Segmentation

Address: 0x400F31E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	VS_BOT [7:4]				VS_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	VS_BOT	RAM configuration nibble for BOTTOM UDB vertical segmentation configuration Default Value: X
3 : 0	VS_TOP	RAM configuration nibble for TOP UDB vertical segmentation configuration Default Value: X

26.1.197 UDB_P0_ROUTE_VS1

UDB Channel VS Tile Configuration; Vertical Segmentation

Address: 0x400F31E2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	VS_BOT [7:4]				VS_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	VS_BOT	RAM configuration nibble for BOTTOM UDB vertical segmentation configuration Default Value: X
3 : 0	VS_TOP	RAM configuration nibble for TOP UDB vertical segmentation configuration Default Value: X

26.1.198 UDB_P0_ROUTE_VS2

UDB Channel VS Tile Configuration; Vertical Segmentation

Address: 0x400F31E4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	VS_BOT [7:4]				VS_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	VS_BOT	RAM configuration nibble for BOTTOM UDB vertical segmentation configuration Default Value: X
3 : 0	VS_TOP	RAM configuration nibble for TOP UDB vertical segmentation configuration Default Value: X

26.1.199 UDB_P0_ROUTE_VS3

UDB Channel VS Tile Configuration; Vertical Segmentation

Address: 0x400F31E6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	VS_BOT [7:4]				VS_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	VS_BOT	RAM configuration nibble for BOTTOM UDB vertical segmentation configuration Default Value: X
3 : 0	VS_TOP	RAM configuration nibble for TOP UDB vertical segmentation configuration Default Value: X

26.1.200 UDB_P0_ROUTE_VS4

UDB Channel VS Tile Configuration; Vertical Segmentation

Address: 0x400F31E8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	VS_BOT [7:4]				VS_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	VS_BOT	RAM configuration nibble for BOTTOM UDB vertical segmentation configuration Default Value: X
3 : 0	VS_TOP	RAM configuration nibble for TOP UDB vertical segmentation configuration Default Value: X

26.1.201 UDB_P0_ROUTE_VS5

UDB Channel VS Tile Configuration; Vertical Segmentation

Address: 0x400F31EA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	VS_BOT [7:4]				VS_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	VS_BOT	RAM configuration nibble for BOTTOM UDB vertical segmentation configuration Default Value: X
3 : 0	VS_TOP	RAM configuration nibble for TOP UDB vertical segmentation configuration Default Value: X

26.1.202 UDB_P0_ROUTE_VS6

UDB Channel VS Tile Configuration; Vertical Segmentation

Address: 0x400F31EC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	VS_BOT [7:4]				VS_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	VS_BOT	RAM configuration nibble for BOTTOM UDB vertical segmentation configuration Default Value: X
3 : 0	VS_TOP	RAM configuration nibble for TOP UDB vertical segmentation configuration Default Value: X

26.1.203 UDB_P0_ROUTE_VS7

UDB Channel VS Tile Configuration; Vertical Segmentation

Address: 0x400F31EE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	VS_BOT [7:4]				VS_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	VS_BOT	RAM configuration nibble for BOTTOM UDB vertical segmentation configuration Default Value: X
3 : 0	VS_TOP	RAM configuration nibble for TOP UDB vertical segmentation configuration Default Value: X

26.1.204 UDB_P1_ROUTE_HC0

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3300

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.205 UDB_P1_ROUTE_HC1

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3301

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.206 UDB_P1_ROUTE_HC2

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3302

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.207 UDB_P1_ROUTE_HC3

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3303

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.208 UDB_P1_ROUTE_HC4

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3304

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.209 UDB_P1_ROUTE_HC5

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3305

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.210 UDB_P1_ROUTE_HC6

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3306

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.211 UDB_P1_ROUTE_HC7

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3307

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.212 UDB_P1_ROUTE_HC8

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3308

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.213 UDB_P1_ROUTE_HC9

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3309

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.214 UDB_P1_ROUTE_HC10

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F330A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.215 UDB_P1_ROUTE_HC11

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F330B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.216 UDB_P1_ROUTE_HC12

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F330C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.217 UDB_P1_ROUTE_HC13

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F330D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.218 UDB_P1_ROUTE_HC14

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F330E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.219 UDB_P1_ROUTE_HC15

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F330F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.220 UDB_P1_ROUTE_HC16

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3310

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.221 UDB_P1_ROUTE_HC17

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3311

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.222 UDB_P1_ROUTE_HC18

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3312

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.223 UDB_P1_ROUTE_HC19

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3313

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.224 UDB_P1_ROUTE_HC20

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3314

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.225 UDB_P1_ROUTE_HC21

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3315

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.226 UDB_P1_ROUTE_HC22

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3316

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.227 UDB_P1_ROUTE_HC23

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3317

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.228 UDB_P1_ROUTE_HC24

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3318

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.229 UDB_P1_ROUTE_HC25

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3319

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.230 UDB_P1_ROUTE_HC26

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F331A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.231 UDB_P1_ROUTE_HC27

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F331B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.232 UDB_P1_ROUTE_HC28

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F331C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.233 UDB_P1_ROUTE_HC29

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F331D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.234 UDB_P1_ROUTE_HC30

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F331E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.235 UDB_P1_ROUTE_HC31

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F331F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.236 UDB_P1_ROUTE_HC32

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3320

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.237 UDB_P1_ROUTE_HC33

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3321

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.238 UDB_P1_ROUTE_HC34

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3322

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.239 UDB_P1_ROUTE_HC35

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3323

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.240 UDB_P1_ROUTE_HC36

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3324

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.241 UDB_P1_ROUTE_HC37

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3325

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.242 UDB_P1_ROUTE_HC38

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3326

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.243 UDB_P1_ROUTE_HC39

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3327

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.244 UDB_P1_ROUTE_HC40

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3328

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.245 UDB_P1_ROUTE_HC41

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3329

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.246 UDB_P1_ROUTE_HC42

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F332A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.247 UDB_P1_ROUTE_HC43

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F332B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.248 UDB_P1_ROUTE_HC44

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F332C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.249 UDB_P1_ROUTE_HC45

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F332D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.250 UDB_P1_ROUTE_HC46

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F332E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.251 UDB_P1_ROUTE_HC47

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F332F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.252 UDB_P1_ROUTE_HC48

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3330

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.253 UDB_P1_ROUTE_HC49

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3331

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.254 UDB_P1_ROUTE_HC50

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3332

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.255 UDB_P1_ROUTE_HC51

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3333

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.256 UDB_P1_ROUTE_HC52

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3334

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.257 UDB_P1_ROUTE_HC53

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3335

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.258 UDB_P1_ROUTE_HC54

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3336

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.259 UDB_P1_ROUTE_HC55

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3337

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.260 UDB_P1_ROUTE_HC56

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3338

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.261 UDB_P1_ROUTE_HC57

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3339

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.262 UDB_P1_ROUTE_HC58

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F333A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.263 UDB_P1_ROUTE_HC59

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F333B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.264 UDB_P1_ROUTE_HC60

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F333C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.265 UDB_P1_ROUTE_HC61

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F333D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.266 UDB_P1_ROUTE_HC62

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F333E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.267 UDB_P1_ROUTE_HC63

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F333F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.268 UDB_P1_ROUTE_HC64

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3340

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.269 UDB_P1_ROUTE_HC65

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3341

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.270 UDB_P1_ROUTE_HC66

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3342

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.271 UDB_P1_ROUTE_HC67

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3343

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.272 UDB_P1_ROUTE_HC68

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3344

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.273 UDB_P1_ROUTE_HC69

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3345

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.274 UDB_P1_ROUTE_HC70

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3346

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.275 UDB_P1_ROUTE_HC71

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3347

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.276 UDB_P1_ROUTE_HC72

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3348

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.277 UDB_P1_ROUTE_HC73

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3349

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.278 UDB_P1_ROUTE_HC74

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F334A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.279 UDB_P1_ROUTE_HC75

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F334B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.280 UDB_P1_ROUTE_HC76

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F334C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.281 UDB_P1_ROUTE_HC77

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F334D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.282 UDB_P1_ROUTE_HC78

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F334E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.283 UDB_P1_ROUTE_HC79

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F334F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.284 UDB_P1_ROUTE_HC80

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3350

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.285 UDB_P1_ROUTE_HC81

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3351

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.286 UDB_P1_ROUTE_HC82

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3352

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.287 UDB_P1_ROUTE_HC83

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3353

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.288 UDB_P1_ROUTE_HC84

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3354

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.289 UDB_P1_ROUTE_HC85

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3355

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.290 UDB_P1_ROUTE_HC86

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3356

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.291 UDB_P1_ROUTE_HC87

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3357

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.292 UDB_P1_ROUTE_HC88

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3358

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.293 UDB_P1_ROUTE_HC89

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3359

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.294 UDB_P1_ROUTE_HC90

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F335A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.295 UDB_P1_ROUTE_HC91

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F335B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.296 UDB_P1_ROUTE_HC92

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F335C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.297 UDB_P1_ROUTE_HC93

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F335D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.298 UDB_P1_ROUTE_HC94

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F335E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.299 UDB_P1_ROUTE_HC95

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F335F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.300 UDB_P1_ROUTE_HC96

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3360

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.301 UDB_P1_ROUTE_HC97

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3361

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.302 UDB_P1_ROUTE_HC98

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3362

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.303 UDB_P1_ROUTE_HC99

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3363

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.304 UDB_P1_ROUTE_HC100

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3364

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.305 UDB_P1_ROUTE_HC101

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3365

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.306 UDB_P1_ROUTE_HC102

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3366

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.307 UDB_P1_ROUTE_HC103

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3367

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.308 UDB_P1_ROUTE_HC104

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3368

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.309 UDB_P1_ROUTE_HC105

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3369

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.310 UDB_P1_ROUTE_HC106

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F336A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.311 UDB_P1_ROUTE_HC107

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F336B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.312 UDB_P1_ROUTE_HC108

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F336C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.313 UDB_P1_ROUTE_HC109

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F336D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.314 UDB_P1_ROUTE_HC110

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F336E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.315 UDB_P1_ROUTE_HC111

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F336F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.316 UDB_P1_ROUTE_HC112

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3370

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.317 UDB_P1_ROUTE_HC113

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3371

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.318 UDB_P1_ROUTE_HC114

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3372

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.319 UDB_P1_ROUTE_HC115

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3373

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.320 UDB_P1_ROUTE_HC116

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3374

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.321 UDB_P1_ROUTE_HC117

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3375

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.322 UDB_P1_ROUTE_HC118

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3376

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.323 UDB_P1_ROUTE_HC119

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3377

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.324 UDB_P1_ROUTE_HC120

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3378

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.325 UDB_P1_ROUTE_HC121

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F3379

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.326 UDB_P1_ROUTE_HC122

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F337A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.327 UDB_P1_ROUTE_HC123

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F337B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.328 UDB_P1_ROUTE_HC124

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F337C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.329 UDB_P1_ROUTE_HC125

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F337D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.330 UDB_P1_ROUTE_HC126

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F337E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.331 UDB_P1_ROUTE_HC127

UDB Channel HC Tile Configuration; Horizontal Channel

Address: 0x400F337F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HC_BYTE [7:0]							

Bits	Name	Description
7 : 0	HC_BYTE	RAM configuration bytes for channel Default Value: X

26.1.332 UDB_P1_ROUTE_HV_L0

UDB Channel HV Tile Configuration; Left

Address: 0x400F3380

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

26.1.333 UDB_P1_ROUTE_HV_L1

UDB Channel HV Tile Configuration; Left

Address: 0x400F3381

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

26.1.334 UDB_P1_ROUTE_HV_L2

UDB Channel HV Tile Configuration; Left

Address: 0x400F3382

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

26.1.335 UDB_P1_ROUTE_HV_L3

UDB Channel HV Tile Configuration; Left

Address: 0x400F3383

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

26.1.336 UDB_P1_ROUTE_HV_L4

UDB Channel HV Tile Configuration; Left

Address: 0x400F3384

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

26.1.337 UDB_P1_ROUTE_HV_L5

UDB Channel HV Tile Configuration; Left

Address: 0x400F3385

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

26.1.338 UDB_P1_ROUTE_HV_L6

UDB Channel HV Tile Configuration; Left

Address: 0x400F3386

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

26.1.339 UDB_P1_ROUTE_HV_L7

UDB Channel HV Tile Configuration; Left

Address: 0x400F3387

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

26.1.340 UDB_P1_ROUTE_HV_L8

UDB Channel HV Tile Configuration; Left

Address: 0x400F3388

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

26.1.341 UDB_P1_ROUTE_HV_L9

UDB Channel HV Tile Configuration; Left

Address: 0x400F3389

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

26.1.342 UDB_P1_ROUTE_HV_L10

UDB Channel HV Tile Configuration; Left

Address: 0x400F338A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

26.1.343 UDB_P1_ROUTE_HV_L11

UDB Channel HV Tile Configuration; Left

Address: 0x400F338B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

26.1.344 UDB_P1_ROUTE_HV_L12

UDB Channel HV Tile Configuration; Left

Address: 0x400F338C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

26.1.345 UDB_P1_ROUTE_HV_L13

UDB Channel HV Tile Configuration; Left

Address: 0x400F338D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

26.1.346 UDB_P1_ROUTE_HV_L14

UDB Channel HV Tile Configuration; Left

Address: 0x400F338E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

26.1.347 UDB_P1_ROUTE_HV_L15

UDB Channel HV Tile Configuration; Left

Address: 0x400F338F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

26.1.348 UDB_P1_ROUTE_HS0

UDB Channel HS Tile Configuration; Horizontal Segmentation

Address: 0x400F3390

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration bytes for channel Default Value: X

26.1.349 UDB_P1_ROUTE_HS1

UDB Channel HS Tile Configuration; Horizontal Segmentation

Address: 0x400F3391

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration bytes for channel Default Value: X

26.1.350 UDB_P1_ROUTE_HS2

UDB Channel HS Tile Configuration; Horizontal Segmentation

Address: 0x400F3392

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration bytes for channel Default Value: X

26.1.351 UDB_P1_ROUTE_HS3

UDB Channel HS Tile Configuration; Horizontal Segmentation

Address: 0x400F3393

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration bytes for channel Default Value: X

26.1.352 UDB_P1_ROUTE_HS4

UDB Channel HS Tile Configuration; Horizontal Segmentation

Address: 0x400F3394

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration bytes for channel Default Value: X

26.1.353 UDB_P1_ROUTE_HS5

UDB Channel HS Tile Configuration; Horizontal Segmentation

Address: 0x400F3395

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration bytes for channel Default Value: X

26.1.354 UDB_P1_ROUTE_HS6

UDB Channel HS Tile Configuration; Horizontal Segmentation

Address: 0x400F3396

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration bytes for channel Default Value: X

26.1.355 UDB_P1_ROUTE_HS7

UDB Channel HS Tile Configuration; Horizontal Segmentation

Address: 0x400F3397

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration bytes for channel Default Value: X

26.1.356 UDB_P1_ROUTE_HS8

UDB Channel HS Tile Configuration; Horizontal Segmentation

Address: 0x400F3398

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration bytes for channel Default Value: X

26.1.357 UDB_P1_ROUTE_HS9

UDB Channel HS Tile Configuration; Horizontal Segmentation

Address: 0x400F3399

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration bytes for channel Default Value: X

26.1.358 UDB_P1_ROUTE_HS10

UDB Channel HS Tile Configuration; Horizontal Segmentation

Address: 0x400F339A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration bytes for channel Default Value: X

26.1.359 UDB_P1_ROUTE_HS11

UDB Channel HS Tile Configuration; Horizontal Segmentation

Address: 0x400F339B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration bytes for channel Default Value: X

26.1.360 UDB_P1_ROUTE_HS12

UDB Channel HS Tile Configuration; Horizontal Segmentation

Address: 0x400F339C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration bytes for channel Default Value: X

26.1.361 UDB_P1_ROUTE_HS13

UDB Channel HS Tile Configuration; Horizontal Segmentation

Address: 0x400F339D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration bytes for channel Default Value: X

26.1.362 UDB_P1_ROUTE_HS14

UDB Channel HS Tile Configuration; Horizontal Segmentation

Address: 0x400F339E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration bytes for channel Default Value: X

26.1.363 UDB_P1_ROUTE_HS15

UDB Channel HS Tile Configuration; Horizontal Segmentation

Address: 0x400F339F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration bytes for channel Default Value: X

26.1.364 UDB_P1_ROUTE_HS16

UDB Channel HS Tile Configuration; Horizontal Segmentation

Address: 0x400F33A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration bytes for channel Default Value: X

26.1.365 UDB_P1_ROUTE_HS17

UDB Channel HS Tile Configuration; Horizontal Segmentation

Address: 0x400F33A1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration bytes for channel Default Value: X

26.1.366 UDB_P1_ROUTE_HS18

UDB Channel HS Tile Configuration; Horizontal Segmentation

Address: 0x400F33A2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration bytes for channel Default Value: X

26.1.367 UDB_P1_ROUTE_HS19

UDB Channel HS Tile Configuration; Horizontal Segmentation

Address: 0x400F33A3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration bytes for channel Default Value: X

26.1.368 UDB_P1_ROUTE_HS20

UDB Channel HS Tile Configuration; Horizontal Segmentation

Address: 0x400F33A4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration bytes for channel Default Value: X

26.1.369 UDB_P1_ROUTE_HS21

UDB Channel HS Tile Configuration; Horizontal Segmentation

Address: 0x400F33A5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration bytes for channel Default Value: X

26.1.370 UDB_P1_ROUTE_HS22

UDB Channel HS Tile Configuration; Horizontal Segmentation

Address: 0x400F33A6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration bytes for channel Default Value: X

26.1.371 UDB_P1_ROUTE_HS23

UDB Channel HS Tile Configuration; Horizontal Segmentation

Address: 0x400F33A7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HS_BYTE [7:0]							

Bits	Name	Description
7 : 0	HS_BYTE	RAM configuration bytes for channel Default Value: X

26.1.372 UDB_P1_ROUTE_HV_R0

UDB Channel HV Tile Configuration; Right

Address: 0x400F33A8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

26.1.373 UDB_P1_ROUTE_HV_R1

UDB Channel HV Tile Configuration; Right

Address: 0x400F33A9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

26.1.374 UDB_P1_ROUTE_HV_R2

UDB Channel HV Tile Configuration; Right

Address: 0x400F33AA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

26.1.375 UDB_P1_ROUTE_HV_R3

UDB Channel HV Tile Configuration; Right

Address: 0x400F33AB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

26.1.376 UDB_P1_ROUTE_HV_R4

UDB Channel HV Tile Configuration; Right

Address: 0x400F33AC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

26.1.377 UDB_P1_ROUTE_HV_R5

UDB Channel HV Tile Configuration; Right

Address: 0x400F33AD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

26.1.378 UDB_P1_ROUTE_HV_R6

UDB Channel HV Tile Configuration; Right

Address: 0x400F33AE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

26.1.379 UDB_P1_ROUTE_HV_R7

UDB Channel HV Tile Configuration; Right

Address: 0x400F33AF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

26.1.380 UDB_P1_ROUTE_HV_R8

UDB Channel HV Tile Configuration; Right

Address: 0x400F33B0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

26.1.381 UDB_P1_ROUTE_HV_R9

UDB Channel HV Tile Configuration; Right

Address: 0x400F33B1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

26.1.382 UDB_P1_ROUTE_HV_R10

UDB Channel HV Tile Configuration; Right

Address: 0x400F33B2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

26.1.383 UDB_P1_ROUTE_HV_R11

UDB Channel HV Tile Configuration; Right

Address: 0x400F33B3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

26.1.384 UDB_P1_ROUTE_HV_R12

UDB Channel HV Tile Configuration; Right

Address: 0x400F33B4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

26.1.385 UDB_P1_ROUTE_HV_R13

UDB Channel HV Tile Configuration; Right

Address: 0x400F33B5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

26.1.386 UDB_P1_ROUTE_HV_R14

UDB Channel HV Tile Configuration; Right

Address: 0x400F33B6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

26.1.387 UDB_P1_ROUTE_HV_R15

UDB Channel HV Tile Configuration; Right

Address: 0x400F33B7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	HV_BYTE [7:0]							

Bits	Name	Description
7 : 0	HV_BYTE	RAM configuration bytes for channel Default Value: X

26.1.388 UDB_P1_ROUTE_PLD0IN0

UDB Channel PI Tile Configuration; PLD Input

Address: 0x400F33C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration nibble for BOTTOM UDB port interface configuration Default Value: X
3 : 0	PI_TOP	RAM configuration nibble for TOP UDB port interface configuration Default Value: X

26.1.389 UDB_P1_ROUTE_PLD0IN1

UDB Channel PI Tile Configuration; PLD Input

Address: 0x400F33C2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration nibble for BOTTOM UDB port interface configuration Default Value: X
3 : 0	PI_TOP	RAM configuration nibble for TOP UDB port interface configuration Default Value: X

26.1.390 UDB_P1_ROUTE_PLD0IN2

UDB Channel PI Tile Configuration; PLD Input

Address: 0x400F33C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration nibble for BOTTOM UDB port interface configuration Default Value: X
3 : 0	PI_TOP	RAM configuration nibble for TOP UDB port interface configuration Default Value: X

26.1.391 UDB_P1_ROUTE_PLD1IN0

UDB Channel PI Tile Configuration; PLD Input

Address: 0x400F33CA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration nibble for BOTTOM UDB port interface configuration Default Value: X
3 : 0	PI_TOP	RAM configuration nibble for TOP UDB port interface configuration Default Value: X

26.1.392 UDB_P1_ROUTE_PLD1IN1

UDB Channel PI Tile Configuration; PLD Input

Address: 0x400F33CC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration nibble for BOTTOM UDB port interface configuration Default Value: X
3 : 0	PI_TOP	RAM configuration nibble for TOP UDB port interface configuration Default Value: X

26.1.393 UDB_P1_ROUTE_PLD1IN2

UDB Channel PI Tile Configuration; PLD Input

Address: 0x400F33CE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration nibble for BOTTOM UDB port interface configuration Default Value: X
3 : 0	PI_TOP	RAM configuration nibble for TOP UDB port interface configuration Default Value: X

26.1.394 UDB_P1_ROUTE_DPIN0

UDB Channel PI Tile Configuration; Datapath Input

Address: 0x400F33D0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration nibble for BOTTOM UDB port interface configuration Default Value: X
3 : 0	PI_TOP	RAM configuration nibble for TOP UDB port interface configuration Default Value: X

26.1.395 UDB_P1_ROUTE_DPIN1

UDB Channel PI Tile Configuration; Datapath Input

Address: 0x400F33D2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW		RW		None	
HW Access	None		R		R		None	
Name	None [7:6]		PI_BOT2 [5:4]		PI_TOP2 [3:2]		None [1:0]	

Bits	Name	Description
5 : 4	PI_BOT2	RAM configuration bits (2) for BOTTOM UDB port interface configuration Default Value: X
3 : 2	PI_TOP2	RAM configuration bits (2) for TOP UDB port interface configuration Default Value: X

26.1.396 UDB_P1_ROUTE_SCIN

UDB Channel PI Tile Configuration; Status / Control Blocks Input Control

Address: 0x400F33D6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration nibble for BOTTOM UDB port interface configuration Default Value: X
3 : 0	PI_TOP	RAM configuration nibble for TOP UDB port interface configuration Default Value: X

26.1.397 UDB_P1_ROUTE_SCIOIN

UDB Channel PI Tile Configuration; Status / Control Blocks Input / Output Control

Address: 0x400F33D8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration nibble for BOTTOM UDB port interface configuration Default Value: X
3 : 0	PI_TOP	RAM configuration nibble for TOP UDB port interface configuration Default Value: X

26.1.398 UDB_P1_ROUTE_RCIN

UDB Channel PI Tile Configuration; Reset and Clock Blocks Input Control

Address: 0x400F33DE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PI_BOT [7:4]				PI_TOP [3:0]			

Bits	Name	Description
7 : 4	PI_BOT	RAM configuration nibble for BOTTOM UDB port interface configuration Default Value: X
3 : 0	PI_TOP	RAM configuration nibble for TOP UDB port interface configuration Default Value: X

26.1.399 UDB_P1_ROUTE_VS0

UDB Channel VS Tile Configuration; Vertical Segmentation

Address: 0x400F33E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	VS_BOT [7:4]				VS_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	VS_BOT	RAM configuration nibble for BOTTOM UDB vertical segmentation configuration Default Value: X
3 : 0	VS_TOP	RAM configuration nibble for TOP UDB vertical segmentation configuration Default Value: X

26.1.400 UDB_P1_ROUTE_VS1

UDB Channel VS Tile Configuration; Vertical Segmentation

Address: 0x400F33E2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	VS_BOT [7:4]				VS_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	VS_BOT	RAM configuration nibble for BOTTOM UDB vertical segmentation configuration Default Value: X
3 : 0	VS_TOP	RAM configuration nibble for TOP UDB vertical segmentation configuration Default Value: X

26.1.401 UDB_P1_ROUTE_VS2

UDB Channel VS Tile Configuration; Vertical Segmentation

Address: 0x400F33E4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	VS_BOT [7:4]				VS_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	VS_BOT	RAM configuration nibble for BOTTOM UDB vertical segmentation configuration Default Value: X
3 : 0	VS_TOP	RAM configuration nibble for TOP UDB vertical segmentation configuration Default Value: X

26.1.402 UDB_P1_ROUTE_VS3

UDB Channel VS Tile Configuration; Vertical Segmentation

Address: 0x400F33E6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	VS_BOT [7:4]				VS_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	VS_BOT	RAM configuration nibble for BOTTOM UDB vertical segmentation configuration Default Value: X
3 : 0	VS_TOP	RAM configuration nibble for TOP UDB vertical segmentation configuration Default Value: X

26.1.403 UDB_P1_ROUTE_VS4

UDB Channel VS Tile Configuration; Vertical Segmentation

Address: 0x400F33E8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	VS_BOT [7:4]				VS_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	VS_BOT	RAM configuration nibble for BOTTOM UDB vertical segmentation configuration Default Value: X
3 : 0	VS_TOP	RAM configuration nibble for TOP UDB vertical segmentation configuration Default Value: X

26.1.404 UDB_P1_ROUTE_VS5

UDB Channel VS Tile Configuration; Vertical Segmentation

Address: 0x400F33EA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	VS_BOT [7:4]				VS_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	VS_BOT	RAM configuration nibble for BOTTOM UDB vertical segmentation configuration Default Value: X
3 : 0	VS_TOP	RAM configuration nibble for TOP UDB vertical segmentation configuration Default Value: X

26.1.405 UDB_P1_ROUTE_VS6

UDB Channel VS Tile Configuration; Vertical Segmentation

Address: 0x400F33EC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	VS_BOT [7:4]				VS_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	VS_BOT	RAM configuration nibble for BOTTOM UDB vertical segmentation configuration Default Value: X
3 : 0	VS_TOP	RAM configuration nibble for TOP UDB vertical segmentation configuration Default Value: X

26.1.406 UDB_P1_ROUTE_VS7

UDB Channel VS Tile Configuration; Vertical Segmentation

Address: 0x400F33EE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	VS_BOT [7:4]				VS_TOP [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	VS_BOT	RAM configuration nibble for BOTTOM UDB vertical segmentation configuration Default Value: X
3 : 0	VS_TOP	RAM configuration nibble for TOP UDB vertical segmentation configuration Default Value: X

27 SAR Registers

This section discusses the SAR registers. It lists all the registers in mapping tables, in address order.

27.1 Register Details

Register Name	Address
SAR_CTRL	0x403A0000
SAR_SAMPLE_CTRL	0x403A0004
SAR_SAMPLE_TIME01	0x403A0010
SAR_SAMPLE_TIME23	0x403A0014
SAR_RANGE_THRES	0x403A0018
SAR_RANGE_COND	0x403A001C
SAR_CHAN_EN	0x403A0020
SAR_START_CTRL	0x403A0024
SAR_DFT_CTRL	0x403A0030
SAR_CHAN_CONFIG0	0x403A0080
SAR_CHAN_CONFIG1	0x403A0084
SAR_CHAN_CONFIG2	0x403A0088
SAR_CHAN_CONFIG3	0x403A008C
SAR_CHAN_CONFIG4	0x403A0090
SAR_CHAN_CONFIG5	0x403A0094
SAR_CHAN_CONFIG6	0x403A0098
SAR_CHAN_CONFIG7	0x403A009C
SAR_CHAN_CONFIG8	0x403A00A0
SAR_CHAN_CONFIG9	0x403A00A4
SAR_CHAN_CONFIG10	0x403A00A8
SAR_CHAN_CONFIG11	0x403A00AC
SAR_CHAN_CONFIG12	0x403A00B0
SAR_CHAN_CONFIG13	0x403A00B4
SAR_CHAN_CONFIG14	0x403A00B8
SAR_CHAN_CONFIG15	0x403A00BC
SAR_CHAN_WORK0	0x403A0100

Register Name	Address
SAR_CHAN_WORK1	0x403A0104
SAR_CHAN_WORK2	0x403A0108
SAR_CHAN_WORK3	0x403A010C
SAR_CHAN_WORK4	0x403A0110
SAR_CHAN_WORK5	0x403A0114
SAR_CHAN_WORK6	0x403A0118
SAR_CHAN_WORK7	0x403A011C
SAR_CHAN_WORK8	0x403A0120
SAR_CHAN_WORK9	0x403A0124
SAR_CHAN_WORK10	0x403A0128
SAR_CHAN_WORK11	0x403A012C
SAR_CHAN_WORK12	0x403A0130
SAR_CHAN_WORK13	0x403A0134
SAR_CHAN_WORK14	0x403A0138
SAR_CHAN_WORK15	0x403A013C
SAR_CHAN_RESULT0	0x403A0180
SAR_CHAN_RESULT1	0x403A0184
SAR_CHAN_RESULT2	0x403A0188
SAR_CHAN_RESULT3	0x403A018C
SAR_CHAN_RESULT4	0x403A0190
SAR_CHAN_RESULT5	0x403A0194
SAR_CHAN_RESULT6	0x403A0198
SAR_CHAN_RESULT7	0x403A019C
SAR_CHAN_RESULT8	0x403A01A0
SAR_CHAN_RESULT9	0x403A01A4
SAR_CHAN_RESULT10	0x403A01A8
SAR_CHAN_RESULT11	0x403A01AC
SAR_CHAN_RESULT12	0x403A01B0
SAR_CHAN_RESULT13	0x403A01B4
SAR_CHAN_RESULT14	0x403A01B8
SAR_CHAN_RESULT15	0x403A01BC
SAR_CHAN_WORK_VALID	0x403A0200
SAR_CHAN_RESULT_VALID	0x403A0204
SAR_STATUS	0x403A0208
SAR_AVG_STAT	0x403A020C
SAR_INTR	0x403A0210
SAR_INTR_SET	0x403A0214
SAR_INTR_MASK	0x403A0218
SAR_INTR_MASKED	0x403A021C
SAR_SATURATE_INTR	0x403A0220

Register Name	Address
SAR_SATURATE_INTR_SET	0x403A0224
SAR_SATURATE_INTR_MASK	0x403A0228
SAR_SATURATE_INTR_MASKED	0x403A022C
SAR_RANGE_INTR	0x403A0230
SAR_RANGE_INTR_SET	0x403A0234
SAR_RANGE_INTR_MASK	0x403A0238
SAR_RANGE_INTR_MASKED	0x403A023C
SAR_INTR_CAUSE	0x403A0240
SAR_INJ_CHAN_CONFIG	0x403A0280
SAR_INJ_RESULT	0x403A0290
SAR_MUX_SWITCH0	0x403A0300
SAR_MUX_SWITCH_CLEAR0	0x403A0304
SAR_MUX_SWITCH1	0x403A0308
SAR_MUX_SWITCH_CLEAR1	0x403A030C
SAR_MUX_SWITCH_HW_CTRL	0x403A0340
SAR_MUX_SWITCH_STATUS	0x403A0348
SAR_PUMP_CTRL	0x403A0380
SAR_ANA_TRIM	0x403A0F00
SAR_WOUNDING	0x403A0F04

27.1.1 SAR_CTRL

Analog control register.

Address: 0x403A0000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW			None			
HW Access	R	R			None			
Name	VREF_BYP_CAP_EN	VREF_SEL [6:4]			None [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW	None	RW			None
HW Access	R		R	None	R			None
Name	PWR_CTRL_VREF [15:14]		SAR_HW_CTRL_NEGVREF	None	NEG_SEL [11:9]			None

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW	RW			
HW Access	None			R	R			
Name	None [23:21]			BOOSTPUMP_EN	SPARE [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	None	RW	
HW Access	R	R	R	R	R	None	R	
Name	ENABLED	SWITCH_DISABLE	DSI_MODE	DSI_SYNC_CONFIG	DEEPSLEEP_ON	None	ICONT_LV [25:24]	

Bits	Name	Description
31	ENABLED	Before enabling always make sure the SAR is idle (STATUS.BUSY==0) - 0: SAR IP disabled (put analog in power down and stop clocks), also can clear FW_TRIGGER and INJ_START_EN (if not tailgaiting) on write. - 1: SAR IP enabled. Default Value: 0
30	SWITCH_DISABLE	Disable SAR sequencer from enabling routing switches (note DSI and firmware can always close switches independent of this control) - 0: Normal mode, SAR sequencer changes switches according to pin address in channel configurations - 1: Switches disabled, SAR sequencer does not enable any switches, it is the responsibility of the firmware or UDBs (through DSI) to set the switches to route the signal to be converted through the SARMUX Default Value: 0

(continued)

29	DSI_MODE	SAR sequencer takes configuration from DSI signals (note this also has the same effect as SWITCH_DISABLE==1) - 0: Normal mode, SAR sequencer operates according to CHAN_EN enables and CHAN_CONFIG channel configurations - 1: CHAN_EN, INJ_START_EN and channel configurations in CHAN_CONFIG and INJ_CHAN_CONFIG are ignored Default Value: 0
28	DSI_SYNC_CONFIG	- 0: bypass clock domain synchronisation of the DSI config signals. - 1: synchronize the DSI config signals to peripheral clock domain. Default Value: 1
27	DEEPSLEEP_ON	- 0: SARMUX IP disabled off during DeepSleep power mode - 1: SARMUX IP remains enabled during DeepSleep power mode (if ENABLED=1) Default Value: 0
25 : 24	ICONT_LV	SARADC low power mode. Default Value: 0 **0x0: NORMAL_PWR:** normal power (default), max clk_sar is 18MHz. **0x1: HALF_PWR:** 1/2 power mode, max clk_sar is 9MHz. **0x2: MORE_PWR:** 1.333 power mode, max clk_sar is 18MHz. **0x3: QUARTER_PWR:** 1/4 power mode, max clk_sar is 4.5MHz.
20	BOOSTPUMP_EN	SARADC internal pump: 0=disabled: pump output is VDDA, 1=enabled: pump output is boosted. Default Value: 0
19 : 16	SPARE	Spare controls, not yet designated, for late changes done with an ECO Default Value: 0
15 : 14	PWR_CTRL_VREF	VREF buffer low power mode. Default Value: 0 **0x0: NORMAL_PWR:** normal power (default), bypass cap, max clk_sar is 18MHz. **0x1: HALF_PWR:** deprecated **0x2: THIRD_PWR:** Invalid for PSoC4A, otherwise 2X power, no bypass cap, max clk_sar is 1.8MHz **0x3: QUARTER_PWR:** deprecated
13	SAR_HW_CTRL_NEGVREF	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for VREF to NEG switch. Default Value: 0
11 : 9	NEG_SEL	SARADC internal NEG selection for Single ended conversion Default Value: 0 **0x0: VSSA_KELVIN:** NEG input of SARADC is connected to "vssa_kelvin", gives more precision around zero. Note this opens both SARADC internal switches, therefore use this value to insert a break-before-make cycle on those switches when SWITCH_DISABLE is high.

(continued)

		0x1: ART_VSSA: NEG input of SARADC is connected to VSSA in AROUTE close to the SARADC **0x2: P1:** NEG input of SARADC is connected to P1 pin of SARMUX **0x3: P3:** NEG input of SARADC is connected to P3 pin of SARMUX **0x4: P5:** NEG input of SARADC is connected to P5 pin of SARMUX **0x5: P7:** NEG input of SARADC is connected to P7 pin of SARMUX **0x6: ACORE:** NEG input of SARADC is connected to an ACORE in AROUTE **0x7: VREF:** NEG input of SARADC is shorted with VREF input of SARADC.
7	VREF_BYP_CAP_EN	VREF bypass cap enable for when VREF buffer is on Default Value: 0
6 : 4	VREF_SEL	SARADC internal VREF selection. Default Value: 0 **0x0: VREF0:** VREF0 from PRB (VREF buffer on) **0x1: VREF1:** VREF1 from PRB (VREF buffer on) **0x2: VREF2:** VREF2 from PRB (VREF buffer on) **0x3: VREF_AROUTE:** VREF from AROUTE (VREF buffer on) **0x4: VBGR:** 1.024V from BandGap (VREF buffer on) **0x5: VREF_EXT:** External precision Vref direct from a pin (low impedance path). **0x6: VDDA_DIV_2:** Vdda/2 (VREF buffer on) **0x7: VDDA:** Vdda.

27.1.2 SAR_SAMPLE_CTRL

Sample control register.

Address: 0x403A0004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW			RW	RW	RW	RW
HW Access	R	R			R	R	R	R
Name	AVG_SHIFT	AVG_CNT [6:4]			DIFFERENTIAL_SIGNED	SINGLE_ENDED_SIGNED	LEFT_ALIGN	SUB_RESOLUTION

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [23:20]				DSI_SYNC_TRIGGER	DSI_TRIGGER_LEVEL	DSI_TRIGGER_EN	CONTINU-OUS

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	EOS_DSI_OUT_EN	None [30:24]						

Bits	Name	Description
31	EOS_DSI_OUT_EN	Enable to output EOS_INTR to DSI. When enabled each time EOS_INTR is set by the hardware also a pulse is send on the dsi_eos signal. Default Value: 0
19	DSI_SYNC_TRIGGER	- 0: bypass clock domain synchronisation of the DSI trigger signal. - 1: synchronize the DSI trigger signal to the SAR clock domain, if needed an edge detect is done in the peripheral clock domain. Default Value: 1
18	DSI_TRIGGER_LEVEL	- 0: DSI trigger signal is a pulse input, a positive edge detected on the DSI trigger signal triggers a new scan. - 1: DSI trigger signal is a level input, as long as the DSI trigger signal remains high the SAR will do continuous scans. Default Value: 0
17	DSI_TRIGGER_EN	- 0: firmware trigger only: disable hardware (DSI) trigger. - 1: enable hardware (DSI) trigger (e.g. from TCPWM, GPIO or UDB). Default Value: 0

(continued)

16	CONTINUOUS	- 0: Wait for next FW_TRIGGER (one shot) or hardware (DSI) trigger (e.g. from TPWM for periodic triggering) before scanning enabled channels. - 1: Continuously scan enabled channels, ignore triggers. Default Value: 0
7	AVG_SHIFT	Averaging shifting: after averaging the result is shifted right to fit in the sample resolution. For averaging the sample resolution is the highest resolution allowed by wounding. Default Value: 0
6 : 4	AVG_CNT	Averaging Count for channels that have over sampling enabled (AVG_EN). A channel will be sampled back to back (1<<(AVG_CNT+1)) = [2..256] times before the result is stored and the next enabled channel is sampled (1st order accumulate and dump filter). If shifting is not enabled (AVG_SHIFT=0) then the result is forced to shift right so that is fits in 16 bits, so right shift is done by max(0,AVG_CNT-3). Default Value: 0
3	DIFFERENTIAL_SIGNED	Output data from a differential conversion as a signed value Default Value: 1 **0x0: UNSIGNED:** result data is unsigned (zero extended if needed) **0x1: SIGNED:** Default: result data is signed (sign extended if needed)
2	SINGLE_ENDED_SIGNED	Output data from a single ended conversion as a signed value Default Value: 0 **0x0: UNSIGNED:** Default: result data is unsigned (zero extended if needed) **0x1: SIGNED:** result data is signed (sign extended if needed)
1	LEFT_ALIGN	Left align data in data[15:0], default data is right aligned in data[11:0], with sign extension to 16 bits if the channel is differential. Default Value: 0
0	SUB_RESOLUTION	Conversion resolution for channels that have sub-resolution enabled (RESOLUTION=1) (otherwise resolution is 12-bit). Default Value: 0 **0x0: 8B:** 8-bit. **0x1: 10B:** 10-bit.

27.1.3 SAR_SAMPLE_TIME01

Sample time specification ST0 and ST1

Address: 0x403A0010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SAMPLE_TIME0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						SAMPLE_TIME0 [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	SAMPLE_TIME1 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None						RW	
HW Access	None						R	
Name	None [31:26]						SAMPLE_TIME1 [25:24]	

Bits	Name	Description
25 : 16	SAMPLE_TIME1	Sample time1 Default Value: 4
9 : 0	SAMPLE_TIME0	Sample time0 (aperture) in ADC clock cycles. Note that actual sample time is half a clock less than specified here. The minimum sample time is 194ns, which is 3.5 cycles (4 in this field) with an 18MHz clock. Minimum legal value in this register is 2. Default Value: 4

27.1.4 SAR_SAMPLE_TIME23

Sample time specification ST2 and ST3

Address: 0x403A0014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SAMPLE_TIME2 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						SAMPLE_TIME2 [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	SAMPLE_TIME3 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None						RW	
HW Access	None						R	
Name	None [31:26]						SAMPLE_TIME3 [25:24]	

Bits	Name	Description
25 : 16	SAMPLE_TIME3	Sample time3 Default Value: 4
9 : 0	SAMPLE_TIME2	Sample time2 Default Value: 4

27.1.5 SAR_RANGE_THRES

Global range detect threshold register.

Address: 0x403A0018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	RANGE_LOW [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	RANGE_LOW [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	RANGE_HIGH [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	RANGE_HIGH [31:24]							

Bits	Name	Description
31 : 16	RANGE_HIGH	High threshold for range detect. Default Value: 0
15 : 0	RANGE_LOW	Low threshold for range detect. Default Value: 0

27.1.6 SAR_RANGE_COND

Global range detect mode register.

Address: 0x403A001C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None					
HW Access	R		None					
Name	RANGE_COND [31:30]		None [29:24]					

Bits	Name	Description
31 : 30	RANGE_COND	Range condition select. Default Value: 0 **0x0: BELOW:** result < RANGE_LOW **0x1: INSIDE:** RANGE_LOW <= result < RANGE_HIGH **0x2: ABOVE:** RANGE_HIGH <= result **0x3: OUTSIDE:** result < RANGE_LOW || RANGE_HIGH <= result

27.1.7 SAR_CHAN_EN

Enable bits for the channels

Address: 0x403A0020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CHAN_EN [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CHAN_EN [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CHAN_EN	Channel enable. - 0: the corresponding channel is disabled. - 1: the corresponding channel is enabled, it will be included in the next scan. Default Value: 0

27.1.8 SAR_START_CTRL

Start control register (firmware trigger).

Address: 0x403A0024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1S
HW Access	None							RW1C
Name	None [7:1]							FW_TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	FW_TRIGGER	When firmware writes a 1 here it will trigger the next scan of enabled channels, hardware clears this bit when the scan started with this trigger is completed. If scanning continuously the trigger is ignored and hardware clears this bit after the next scan is done. This bit is also cleared when the SAR is disabled. Default Value: 0

27.1.9 SAR_DFT_CTRL

DFT control register.

Address: 0x403A0030

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						HIZ	DLY_INC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None	RW			RW			
HW Access	None	R			R			
Name	None	DFT_OUTC [22:20]			DFT_INC [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None	RW	RW	RW			
HW Access	R	None	R	R	R			
Name	ADFT_OVERRIDE	None	DCEN	EN_CSEL_DFT	SEL_CSEL_DFT [27:24]			

Bits	Name	Description
31	ADFT_OVERRIDE	During deepsleep/ hibernate mode keep SARMUX active, i.e. do not open all switches (disconnect), to be used for ADFT Default Value: 0
29	DCEN	Delay Control Enable for latch. - 0: doubles the latch enable time. - 1: normal latch enable time (default). Default Value: 0
28	EN_CSEL_DFT	Mux select signal for DAC control Default Value: 0
27 : 24	SEL_CSEL_DFT	Usage 1: DFT bits for DAC array Usage 2: For [0]=1 (when dcen=0): Delay timing for latch enable increased by 20% [1]=1: comparator preamp power level increased by 25% Default Value: 0
22 : 20	DFT_OUTC	DFT control for preamp outputs Default Value: 0

(continued)

19 : 16	DFT_INC	DFT control for preamp inputs Default Value: 0
1	HIZ	DFT control for getting higher input impedance, must be 1 (0 is deprecated) Default Value: 1
0	DLY_INC	DFT control: Control for delay circuits on sampling phase, =1 doubes the non-overlap delay Default Value: 0

27.1.10 SAR_CHAN_CONFIG0

Channel configuration register.

Address: 0x403A0080

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	PORT_ADDR [6:4]			None	PIN_ADDR [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW		None	RW	RW	RW
HW Access	None		R		None	R	R	R
Name	None [15:14]		SAMPLE_TIME_SEL [13:12]		None	AVG_EN	RESOLU-TION	DIFFEREN TIAL_EN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	DSI_OUT_ EN	None [30:24]						

Bits	Name	Description
31	DSI_OUT_EN	DSI data output enable for this channel. - 0: the conversion result for this channel is only stored in the channel data register and the corresponding CHAN_DATA_VALID bit is set. - 1: the conversion result for this channel is stored in the channel data register and the corresponding CHAN_DATA_VALID bit is set. The same data (same formating), together with the channel number, is sent out on the DSI communication channel for processing in UDBs. Default Value: 0
13 : 12	SAMPLE_TIME_SEL	Sample time select: select which of the 4 global sample times to use for this channel Default Value: 0
10	AVG_EN	Averaging enable for this channel. If set the AVG_CNT and AVG_SHIFT settings are used for sampling the addressed pin(s) Default Value: 0
9	RESOLUTION	Resolution for this channel. When AVG_EN is set this bit is ignored and always a 12-bit resolution (or highest resolution allowed by wounding) is used for this channel. Default Value: 0

(continued)

		0x0: MAXRES: The maximum resolution is used for this channel (maximum resolution depends on wounding). **0x1: SUBRES:** The resolution specified by SUB_RESOLUTION in the SAR_SAMPLE_CTRL register is used for this channel.
8	DIFFERENTIAL_EN	Differential enable for this channel. - 0: The voltage on the addressed pin is measured (Single-ended) and the resulting value is stored in the corresponding data register. - 1: The differential voltage on the addressed pin pair is measured and the resulting value is stored in the corresponding data register. (PIN_ADDR[0] is ignored). Default Value: 0
6 : 4	PORT_ADDR	Address of the port that contains the pin to be sampled by this channel. Default Value: 0 **0x0: SARMUX:** SARMUX pins. **0x1: CTB0:** CTB0 **0x2: CTB1:** CTB1 **0x3: CTB2:** CTB2 **0x4: CTB3:** CTB3 **0x5: AROUTE_VIRT2:** AROUTE virtual port2 (VPORT2) **0x6: AROUTE_VIRT1:** AROUTE virtual port1 (VPORT1) **0x7: SARMUX_VIRT:** SARMUX virtual port (VPORT0)
2 : 0	PIN_ADDR	Address of the pin to be sampled by this channel. If differential is enabled then PIN_ADDR[0] is ignored and considered to be 0, i.e. PIN_ADDR points to the even pin of a pin pair. For differential the even pin of the pair is connected to Vplus and the odd pin of the pair is connected to Vminus. Default Value: 0

27.1.11 SAR_CHAN_CONFIG1

Channel configuration register.

Address: 0x403A0084

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	PORT_ADDR [6:4]			None	PIN_ADDR [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW		None	RW	RW	RW
HW Access	None		R		None	R	R	R
Name	None [15:14]		SAMPLE_TIME_SEL [13:12]		None	AVG_EN	RESOLU-TION	DIFFEREN TIAL_EN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	DSI_OUT_ EN	None [30:24]						

Bits	Name	Description
31	DSI_OUT_EN	DSI data output enable for this channel. - 0: the conversion result for this channel is only stored in the channel data register and the corresponding CHAN_DATA_VALID bit is set. - 1: the conversion result for this channel is stored in the channel data register and the corresponding CHAN_DATA_VALID bit is set. The same data (same formating), together with the channel number, is sent out on the DSI communication channel for processing in UDBs. Default Value: 0
13 : 12	SAMPLE_TIME_SEL	Sample time select: select which of the 4 global sample times to use for this channel Default Value: 0
10	AVG_EN	Averaging enable for this channel. If set the AVG_CNT and AVG_SHIFT settings are used for sampling the addressed pin(s) Default Value: 0
9	RESOLUTION	Resolution for this channel. When AVG_EN is set this bit is ignored and always a 12-bit resolution (or highest resolution allowed by wounding) is used for this channel. Default Value: 0

(continued)

		0x0: MAXRES: The maximum resolution is used for this channel (maximum resolution depends on wounding). **0x1: SUBRES:** The resolution specified by SUB_RESOLUTION in the SAR_SAMPLE_CTRL register is used for this channel.
8	DIFFERENTIAL_EN	Differential enable for this channel. - 0: The voltage on the addressed pin is measured (Single-ended) and the resulting value is stored in the corresponding data register. - 1: The differential voltage on the addressed pin pair is measured and the resulting value is stored in the corresponding data register. (PIN_ADDR[0] is ignored). Default Value: 0
6 : 4	PORT_ADDR	Address of the port that contains the pin to be sampled by this channel. Default Value: 0 **0x0: SARMUX:** SARMUX pins. **0x1: CTB0:** CTB0 **0x2: CTB1:** CTB1 **0x3: CTB2:** CTB2 **0x4: CTB3:** CTB3 **0x5: AROUTE_VIRT2:** AROUTE virtual port2 (VPORT2) **0x6: AROUTE_VIRT1:** AROUTE virtual port1 (VPORT1) **0x7: SARMUX_VIRT:** SARMUX virtual port (VPORT0)
2 : 0	PIN_ADDR	Address of the pin to be sampled by this channel. If differential is enabled then PIN_ADDR[0] is ignored and considered to be 0, i.e. PIN_ADDR points to the even pin of a pin pair. For differential the even pin of the pair is connected to Vplus and the odd pin of the pair is connected to Vminus. Default Value: 0

27.1.12 SAR_CHAN_CONFIG2

Channel configuration register.

Address: 0x403A0088

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	PORT_ADDR [6:4]			None	PIN_ADDR [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW		None	RW	RW	RW
HW Access	None		R		None	R	R	R
Name	None [15:14]		SAMPLE_TIME_SEL [13:12]		None	AVG_EN	RESOLU-TION	DIFFEREN TIAL_EN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	DSI_OUT_ EN	None [30:24]						

Bits	Name	Description
31	DSI_OUT_EN	DSI data output enable for this channel. - 0: the conversion result for this channel is only stored in the channel data register and the corresponding CHAN_DATA_VALID bit is set. - 1: the conversion result for this channel is stored in the channel data register and the corresponding CHAN_DATA_VALID bit is set. The same data (same formating), together with the channel number, is sent out on the DSI communication channel for processing in UDBs. Default Value: 0
13 : 12	SAMPLE_TIME_SEL	Sample time select: select which of the 4 global sample times to use for this channel Default Value: 0
10	AVG_EN	Averaging enable for this channel. If set the AVG_CNT and AVG_SHIFT settings are used for sampling the addressed pin(s) Default Value: 0
9	RESOLUTION	Resolution for this channel. When AVG_EN is set this bit is ignored and always a 12-bit resolution (or highest resolution allowed by wounding) is used for this channel. Default Value: 0

(continued)

		0x0: MAXRES: The maximum resolution is used for this channel (maximum resolution depends on wounding). **0x1: SUBRES:** The resolution specified by SUB_RESOLUTION in the SAR_SAMPLE_CTRL register is used for this channel.
8	DIFFERENTIAL_EN	Differential enable for this channel. - 0: The voltage on the addressed pin is measured (Single-ended) and the resulting value is stored in the corresponding data register. - 1: The differential voltage on the addressed pin pair is measured and the resulting value is stored in the corresponding data register. (PIN_ADDR[0] is ignored). Default Value: 0
6 : 4	PORT_ADDR	Address of the port that contains the pin to be sampled by this channel. Default Value: 0 **0x0: SARMUX:** SARMUX pins. **0x1: CTB0:** CTB0 **0x2: CTB1:** CTB1 **0x3: CTB2:** CTB2 **0x4: CTB3:** CTB3 **0x5: AROUTE_VIRT2:** AROUTE virtual port2 (VPORT2) **0x6: AROUTE_VIRT1:** AROUTE virtual port1 (VPORT1) **0x7: SARMUX_VIRT:** SARMUX virtual port (VPORT0)
2 : 0	PIN_ADDR	Address of the pin to be sampled by this channel. If differential is enabled then PIN_ADDR[0] is ignored and considered to be 0, i.e. PIN_ADDR points to the even pin of a pin pair. For differential the even pin of the pair is connected to Vplus and the odd pin of the pair is connected to Vminus. Default Value: 0

27.1.13 SAR_CHAN_CONFIG3

Channel configuration register.

Address: 0x403A008C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	PORT_ADDR [6:4]			None	PIN_ADDR [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW		None	RW	RW	RW
HW Access	None		R		None	R	R	R
Name	None [15:14]		SAMPLE_TIME_SEL [13:12]		None	AVG_EN	RESOLU-TION	DIFFEREN TIAL_EN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	DSI_OUT_ EN	None [30:24]						

Bits	Name	Description
31	DSI_OUT_EN	DSI data output enable for this channel. - 0: the conversion result for this channel is only stored in the channel data register and the corresponding CHAN_DATA_VALID bit is set. - 1: the conversion result for this channel is stored in the channel data register and the corresponding CHAN_DATA_VALID bit is set. The same data (same formating), together with the channel number, is sent out on the DSI communication channel for processing in UDBs. Default Value: 0
13 : 12	SAMPLE_TIME_SEL	Sample time select: select which of the 4 global sample times to use for this channel Default Value: 0
10	AVG_EN	Averaging enable for this channel. If set the AVG_CNT and AVG_SHIFT settings are used for sampling the addressed pin(s) Default Value: 0
9	RESOLUTION	Resolution for this channel. When AVG_EN is set this bit is ignored and always a 12-bit resolution (or highest resolution allowed by wounding) is used for this channel. Default Value: 0

(continued)

		0x0: MAXRES: The maximum resolution is used for this channel (maximum resolution depends on wounding). **0x1: SUBRES:** The resolution specified by SUB_RESOLUTION in the SAR_SAMPLE_CTRL register is used for this channel.
8	DIFFERENTIAL_EN	Differential enable for this channel. - 0: The voltage on the addressed pin is measured (Single-ended) and the resulting value is stored in the corresponding data register. - 1: The differential voltage on the addressed pin pair is measured and the resulting value is stored in the corresponding data register. (PIN_ADDR[0] is ignored). Default Value: 0
6 : 4	PORT_ADDR	Address of the port that contains the pin to be sampled by this channel. Default Value: 0 **0x0: SARMUX:** SARMUX pins. **0x1: CTB0:** CTB0 **0x2: CTB1:** CTB1 **0x3: CTB2:** CTB2 **0x4: CTB3:** CTB3 **0x5: AROUTE_VIRT2:** AROUTE virtual port2 (VPORT2) **0x6: AROUTE_VIRT1:** AROUTE virtual port1 (VPORT1) **0x7: SARMUX_VIRT:** SARMUX virtual port (VPORT0)
2 : 0	PIN_ADDR	Address of the pin to be sampled by this channel. If differential is enabled then PIN_ADDR[0] is ignored and considered to be 0, i.e. PIN_ADDR points to the even pin of a pin pair. For differential the even pin of the pair is connected to Vplus and the odd pin of the pair is connected to Vminus. Default Value: 0

27.1.14 SAR_CHAN_CONFIG4

Channel configuration register.

Address: 0x403A0090

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	PORT_ADDR [6:4]			None	PIN_ADDR [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW		None	RW	RW	RW
HW Access	None		R		None	R	R	R
Name	None [15:14]		SAMPLE_TIME_SEL [13:12]		None	AVG_EN	RESOLU-TION	DIFFEREN TIAL_EN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	DSI_OUT_ EN	None [30:24]						

Bits	Name	Description
31	DSI_OUT_EN	DSI data output enable for this channel. - 0: the conversion result for this channel is only stored in the channel data register and the corresponding CHAN_DATA_VALID bit is set. - 1: the conversion result for this channel is stored in the channel data register and the corresponding CHAN_DATA_VALID bit is set. The same data (same formating), together with the channel number, is sent out on the DSI communication channel for processing in UDBs. Default Value: 0
13 : 12	SAMPLE_TIME_SEL	Sample time select: select which of the 4 global sample times to use for this channel Default Value: 0
10	AVG_EN	Averaging enable for this channel. If set the AVG_CNT and AVG_SHIFT settings are used for sampling the addressed pin(s) Default Value: 0
9	RESOLUTION	Resolution for this channel. When AVG_EN is set this bit is ignored and always a 12-bit resolution (or highest resolution allowed by wounding) is used for this channel. Default Value: 0

(continued)

		0x0: MAXRES: The maximum resolution is used for this channel (maximum resolution depends on wounding). **0x1: SUBRES:** The resolution specified by SUB_RESOLUTION in the SAR_SAMPLE_CTRL register is used for this channel.
8	DIFFERENTIAL_EN	Differential enable for this channel. - 0: The voltage on the addressed pin is measured (Single-ended) and the resulting value is stored in the corresponding data register. - 1: The differential voltage on the addressed pin pair is measured and the resulting value is stored in the corresponding data register. (PIN_ADDR[0] is ignored). Default Value: 0
6 : 4	PORT_ADDR	Address of the port that contains the pin to be sampled by this channel. Default Value: 0 **0x0: SARMUX:** SARMUX pins. **0x1: CTB0:** CTB0 **0x2: CTB1:** CTB1 **0x3: CTB2:** CTB2 **0x4: CTB3:** CTB3 **0x5: AROUTE_VIRT2:** AROUTE virtual port2 (VPORT2) **0x6: AROUTE_VIRT1:** AROUTE virtual port1 (VPORT1) **0x7: SARMUX_VIRT:** SARMUX virtual port (VPORT0)
2 : 0	PIN_ADDR	Address of the pin to be sampled by this channel. If differential is enabled then PIN_ADDR[0] is ignored and considered to be 0, i.e. PIN_ADDR points to the even pin of a pin pair. For differential the even pin of the pair is connected to Vplus and the odd pin of the pair is connected to Vminus. Default Value: 0

27.1.15 SAR_CHAN_CONFIG5

Channel configuration register.

Address: 0x403A0094

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	PORT_ADDR [6:4]			None	PIN_ADDR [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW		None	RW	RW	RW
HW Access	None		R		None	R	R	R
Name	None [15:14]		SAMPLE_TIME_SEL [13:12]		None	AVG_EN	RESOLU-TION	DIFFEREN TIAL_EN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	DSI_OUT_ EN	None [30:24]						

Bits	Name	Description
31	DSI_OUT_EN	DSI data output enable for this channel. - 0: the conversion result for this channel is only stored in the channel data register and the corresponding CHAN_DATA_VALID bit is set. - 1: the conversion result for this channel is stored in the channel data register and the corresponding CHAN_DATA_VALID bit is set. The same data (same formating), together with the channel number, is sent out on the DSI communication channel for processing in UDBs. Default Value: 0
13 : 12	SAMPLE_TIME_SEL	Sample time select: select which of the 4 global sample times to use for this channel Default Value: 0
10	AVG_EN	Averaging enable for this channel. If set the AVG_CNT and AVG_SHIFT settings are used for sampling the addressed pin(s) Default Value: 0
9	RESOLUTION	Resolution for this channel. When AVG_EN is set this bit is ignored and always a 12-bit resolution (or highest resolution allowed by wounding) is used for this channel. Default Value: 0

(continued)

		0x0: MAXRES: The maximum resolution is used for this channel (maximum resolution depends on wounding). **0x1: SUBRES:** The resolution specified by SUB_RESOLUTION in the SAR_SAMPLE_CTRL register is used for this channel.
8	DIFFERENTIAL_EN	Differential enable for this channel. - 0: The voltage on the addressed pin is measured (Single-ended) and the resulting value is stored in the corresponding data register. - 1: The differential voltage on the addressed pin pair is measured and the resulting value is stored in the corresponding data register. (PIN_ADDR[0] is ignored). Default Value: 0
6 : 4	PORT_ADDR	Address of the port that contains the pin to be sampled by this channel. Default Value: 0 **0x0: SARMUX:** SARMUX pins. **0x1: CTB0:** CTB0 **0x2: CTB1:** CTB1 **0x3: CTB2:** CTB2 **0x4: CTB3:** CTB3 **0x5: AROUTE_VIRT2:** AROUTE virtual port2 (VPORT2) **0x6: AROUTE_VIRT1:** AROUTE virtual port1 (VPORT1) **0x7: SARMUX_VIRT:** SARMUX virtual port (VPORT0)
2 : 0	PIN_ADDR	Address of the pin to be sampled by this channel. If differential is enabled then PIN_ADDR[0] is ignored and considered to be 0, i.e. PIN_ADDR points to the even pin of a pin pair. For differential the even pin of the pair is connected to Vplus and the odd pin of the pair is connected to Vminus. Default Value: 0

27.1.16 SAR_CHAN_CONFIG6

Channel configuration register.

Address: 0x403A0098

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	PORT_ADDR [6:4]			None	PIN_ADDR [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW		None	RW	RW	RW
HW Access	None		R		None	R	R	R
Name	None [15:14]		SAMPLE_TIME_SEL [13:12]		None	AVG_EN	RESOLU-TION	DIFFEREN TIAL_EN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	DSI_OUT_ EN	None [30:24]						

Bits	Name	Description
31	DSI_OUT_EN	DSI data output enable for this channel. - 0: the conversion result for this channel is only stored in the channel data register and the corresponding CHAN_DATA_VALID bit is set. - 1: the conversion result for this channel is stored in the channel data register and the corresponding CHAN_DATA_VALID bit is set. The same data (same formating), together with the channel number, is sent out on the DSI communication channel for processing in UDBs. Default Value: 0
13 : 12	SAMPLE_TIME_SEL	Sample time select: select which of the 4 global sample times to use for this channel Default Value: 0
10	AVG_EN	Averaging enable for this channel. If set the AVG_CNT and AVG_SHIFT settings are used for sampling the addressed pin(s) Default Value: 0
9	RESOLUTION	Resolution for this channel. When AVG_EN is set this bit is ignored and always a 12-bit resolution (or highest resolution allowed by wounding) is used for this channel. Default Value: 0

(continued)

		0x0: MAXRES: The maximum resolution is used for this channel (maximum resolution depends on wounding). **0x1: SUBRES:** The resolution specified by SUB_RESOLUTION in the SAR_SAMPLE_CTRL register is used for this channel.
8	DIFFERENTIAL_EN	Differential enable for this channel. - 0: The voltage on the addressed pin is measured (Single-ended) and the resulting value is stored in the corresponding data register. - 1: The differential voltage on the addressed pin pair is measured and the resulting value is stored in the corresponding data register. (PIN_ADDR[0] is ignored). Default Value: 0
6 : 4	PORT_ADDR	Address of the port that contains the pin to be sampled by this channel. Default Value: 0 **0x0: SARMUX:** SARMUX pins. **0x1: CTB0:** CTB0 **0x2: CTB1:** CTB1 **0x3: CTB2:** CTB2 **0x4: CTB3:** CTB3 **0x5: AROUTE_VIRT2:** AROUTE virtual port2 (VPORT2) **0x6: AROUTE_VIRT1:** AROUTE virtual port1 (VPORT1) **0x7: SARMUX_VIRT:** SARMUX virtual port (VPORT0)
2 : 0	PIN_ADDR	Address of the pin to be sampled by this channel. If differential is enabled then PIN_ADDR[0] is ignored and considered to be 0, i.e. PIN_ADDR points to the even pin of a pin pair. For differential the even pin of the pair is connected to Vplus and the odd pin of the pair is connected to Vminus. Default Value: 0

27.1.17 SAR_CHAN_CONFIG7

Channel configuration register.

Address: 0x403A009C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	PORT_ADDR [6:4]			None	PIN_ADDR [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW		None	RW	RW	RW
HW Access	None		R		None	R	R	R
Name	None [15:14]		SAMPLE_TIME_SEL [13:12]		None	AVG_EN	RESOLU-TION	DIFFEREN TIAL_EN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	DSI_OUT_ EN	None [30:24]						

Bits	Name	Description
31	DSI_OUT_EN	DSI data output enable for this channel. - 0: the conversion result for this channel is only stored in the channel data register and the corresponding CHAN_DATA_VALID bit is set. - 1: the conversion result for this channel is stored in the channel data register and the corresponding CHAN_DATA_VALID bit is set. The same data (same formating), together with the channel number, is sent out on the DSI communication channel for processing in UDBs. Default Value: 0
13 : 12	SAMPLE_TIME_SEL	Sample time select: select which of the 4 global sample times to use for this channel Default Value: 0
10	AVG_EN	Averaging enable for this channel. If set the AVG_CNT and AVG_SHIFT settings are used for sampling the addressed pin(s) Default Value: 0
9	RESOLUTION	Resolution for this channel. When AVG_EN is set this bit is ignored and always a 12-bit resolution (or highest resolution allowed by wounding) is used for this channel. Default Value: 0

(continued)

		0x0: MAXRES: The maximum resolution is used for this channel (maximum resolution depends on wounding). **0x1: SUBRES:** The resolution specified by SUB_RESOLUTION in the SAR_SAMPLE_CTRL register is used for this channel.
8	DIFFERENTIAL_EN	Differential enable for this channel. - 0: The voltage on the addressed pin is measured (Single-ended) and the resulting value is stored in the corresponding data register. - 1: The differential voltage on the addressed pin pair is measured and the resulting value is stored in the corresponding data register. (PIN_ADDR[0] is ignored). Default Value: 0
6 : 4	PORT_ADDR	Address of the port that contains the pin to be sampled by this channel. Default Value: 0 **0x0: SARMUX:** SARMUX pins. **0x1: CTB0:** CTB0 **0x2: CTB1:** CTB1 **0x3: CTB2:** CTB2 **0x4: CTB3:** CTB3 **0x5: AROUTE_VIRT2:** AROUTE virtual port2 (VPORT2) **0x6: AROUTE_VIRT1:** AROUTE virtual port1 (VPORT1) **0x7: SARMUX_VIRT:** SARMUX virtual port (VPORT0)
2 : 0	PIN_ADDR	Address of the pin to be sampled by this channel. If differential is enabled then PIN_ADDR[0] is ignored and considered to be 0, i.e. PIN_ADDR points to the even pin of a pin pair. For differential the even pin of the pair is connected to Vplus and the odd pin of the pair is connected to Vminus. Default Value: 0

27.1.18 SAR_CHAN_CONFIG8

Channel configuration register.

Address: 0x403A00A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	PORT_ADDR [6:4]			None	PIN_ADDR [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW		None	RW	RW	RW
HW Access	None		R		None	R	R	R
Name	None [15:14]		SAMPLE_TIME_SEL [13:12]		None	AVG_EN	RESOLU-TION	DIFFEREN TIAL_EN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	DSI_OUT_ EN	None [30:24]						

Bits	Name	Description
31	DSI_OUT_EN	DSI data output enable for this channel. - 0: the conversion result for this channel is only stored in the channel data register and the corresponding CHAN_DATA_VALID bit is set. - 1: the conversion result for this channel is stored in the channel data register and the corresponding CHAN_DATA_VALID bit is set. The same data (same formating), together with the channel number, is sent out on the DSI communication channel for processing in UDBs. Default Value: 0
13 : 12	SAMPLE_TIME_SEL	Sample time select: select which of the 4 global sample times to use for this channel Default Value: 0
10	AVG_EN	Averaging enable for this channel. If set the AVG_CNT and AVG_SHIFT settings are used for sampling the addressed pin(s) Default Value: 0
9	RESOLUTION	Resolution for this channel. When AVG_EN is set this bit is ignored and always a 12-bit resolution (or highest resolution allowed by wounding) is used for this channel. Default Value: 0

(continued)

		0x0: MAXRES: The maximum resolution is used for this channel (maximum resolution depends on wounding). **0x1: SUBRES:** The resolution specified by SUB_RESOLUTION in the SAR_SAMPLE_CTRL register is used for this channel.
8	DIFFERENTIAL_EN	Differential enable for this channel. - 0: The voltage on the addressed pin is measured (Single-ended) and the resulting value is stored in the corresponding data register. - 1: The differential voltage on the addressed pin pair is measured and the resulting value is stored in the corresponding data register. (PIN_ADDR[0] is ignored). Default Value: 0
6 : 4	PORT_ADDR	Address of the port that contains the pin to be sampled by this channel. Default Value: 0 **0x0: SARMUX:** SARMUX pins. **0x1: CTB0:** CTB0 **0x2: CTB1:** CTB1 **0x3: CTB2:** CTB2 **0x4: CTB3:** CTB3 **0x5: AROUTE_VIRT2:** AROUTE virtual port2 (VPORT2) **0x6: AROUTE_VIRT1:** AROUTE virtual port1 (VPORT1) **0x7: SARMUX_VIRT:** SARMUX virtual port (VPORT0)
2 : 0	PIN_ADDR	Address of the pin to be sampled by this channel. If differential is enabled then PIN_ADDR[0] is ignored and considered to be 0, i.e. PIN_ADDR points to the even pin of a pin pair. For differential the even pin of the pair is connected to Vplus and the odd pin of the pair is connected to Vminus. Default Value: 0

27.1.19 SAR_CHAN_CONFIG9

Channel configuration register.

Address: 0x403A00A4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	PORT_ADDR [6:4]			None	PIN_ADDR [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW		None	RW	RW	RW
HW Access	None		R		None	R	R	R
Name	None [15:14]		SAMPLE_TIME_SEL [13:12]		None	AVG_EN	RESOLU-TION	DIFFEREN TIAL_EN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	DSI_OUT_ EN	None [30:24]						

Bits	Name	Description
31	DSI_OUT_EN	DSI data output enable for this channel. - 0: the conversion result for this channel is only stored in the channel data register and the corresponding CHAN_DATA_VALID bit is set. - 1: the conversion result for this channel is stored in the channel data register and the corresponding CHAN_DATA_VALID bit is set. The same data (same formating), together with the channel number, is sent out on the DSI communication channel for processing in UDBs. Default Value: 0
13 : 12	SAMPLE_TIME_SEL	Sample time select: select which of the 4 global sample times to use for this channel Default Value: 0
10	AVG_EN	Averaging enable for this channel. If set the AVG_CNT and AVG_SHIFT settings are used for sampling the addressed pin(s) Default Value: 0
9	RESOLUTION	Resolution for this channel. When AVG_EN is set this bit is ignored and always a 12-bit resolution (or highest resolution allowed by wounding) is used for this channel. Default Value: 0

(continued)

		0x0: MAXRES: The maximum resolution is used for this channel (maximum resolution depends on wounding). **0x1: SUBRES:** The resolution specified by SUB_RESOLUTION in the SAR_SAMPLE_CTRL register is used for this channel.
8	DIFFERENTIAL_EN	Differential enable for this channel. - 0: The voltage on the addressed pin is measured (Single-ended) and the resulting value is stored in the corresponding data register. - 1: The differential voltage on the addressed pin pair is measured and the resulting value is stored in the corresponding data register. (PIN_ADDR[0] is ignored). Default Value: 0
6 : 4	PORT_ADDR	Address of the port that contains the pin to be sampled by this channel. Default Value: 0 **0x0: SARMUX:** SARMUX pins. **0x1: CTB0:** CTB0 **0x2: CTB1:** CTB1 **0x3: CTB2:** CTB2 **0x4: CTB3:** CTB3 **0x5: AROUTE_VIRT2:** AROUTE virtual port2 (VPORT2) **0x6: AROUTE_VIRT1:** AROUTE virtual port1 (VPORT1) **0x7: SARMUX_VIRT:** SARMUX virtual port (VPORT0)
2 : 0	PIN_ADDR	Address of the pin to be sampled by this channel. If differential is enabled then PIN_ADDR[0] is ignored and considered to be 0, i.e. PIN_ADDR points to the even pin of a pin pair. For differential the even pin of the pair is connected to Vplus and the odd pin of the pair is connected to Vminus. Default Value: 0

27.1.20 SAR_CHAN_CONFIG10

Channel configuration register.

Address: 0x403A00A8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	PORT_ADDR [6:4]			None	PIN_ADDR [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW		None	RW	RW	RW
HW Access	None		R		None	R	R	R
Name	None [15:14]		SAMPLE_TIME_SEL [13:12]		None	AVG_EN	RESOLU-TION	DIFFEREN TIAL_EN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	DSI_OUT_ EN	None [30:24]						

Bits	Name	Description
31	DSI_OUT_EN	DSI data output enable for this channel. - 0: the conversion result for this channel is only stored in the channel data register and the corresponding CHAN_DATA_VALID bit is set. - 1: the conversion result for this channel is stored in the channel data register and the corresponding CHAN_DATA_VALID bit is set. The same data (same formating), together with the channel number, is sent out on the DSI communication channel for processing in UDBs. Default Value: 0
13 : 12	SAMPLE_TIME_SEL	Sample time select: select which of the 4 global sample times to use for this channel Default Value: 0
10	AVG_EN	Averaging enable for this channel. If set the AVG_CNT and AVG_SHIFT settings are used for sampling the addressed pin(s) Default Value: 0
9	RESOLUTION	Resolution for this channel. When AVG_EN is set this bit is ignored and always a 12-bit resolution (or highest resolution allowed by wounding) is used for this channel. Default Value: 0

(continued)

		0x0: MAXRES: The maximum resolution is used for this channel (maximum resolution depends on wounding). **0x1: SUBRES:** The resolution specified by SUB_RESOLUTION in the SAR_SAMPLE_CTRL register is used for this channel.
8	DIFFERENTIAL_EN	Differential enable for this channel. - 0: The voltage on the addressed pin is measured (Single-ended) and the resulting value is stored in the corresponding data register. - 1: The differential voltage on the addressed pin pair is measured and the resulting value is stored in the corresponding data register. (PIN_ADDR[0] is ignored). Default Value: 0
6 : 4	PORT_ADDR	Address of the port that contains the pin to be sampled by this channel. Default Value: 0 **0x0: SARMUX:** SARMUX pins. **0x1: CTB0:** CTB0 **0x2: CTB1:** CTB1 **0x3: CTB2:** CTB2 **0x4: CTB3:** CTB3 **0x5: AROUTE_VIRT2:** AROUTE virtual port2 (VPORT2) **0x6: AROUTE_VIRT1:** AROUTE virtual port1 (VPORT1) **0x7: SARMUX_VIRT:** SARMUX virtual port (VPORT0)
2 : 0	PIN_ADDR	Address of the pin to be sampled by this channel. If differential is enabled then PIN_ADDR[0] is ignored and considered to be 0, i.e. PIN_ADDR points to the even pin of a pin pair. For differential the even pin of the pair is connected to Vplus and the odd pin of the pair is connected to Vminus. Default Value: 0

27.1.21 SAR_CHAN_CONFIG11

Channel configuration register.

Address: 0x403A00AC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	PORT_ADDR [6:4]			None	PIN_ADDR [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW		None	RW	RW	RW
HW Access	None		R		None	R	R	R
Name	None [15:14]		SAMPLE_TIME_SEL [13:12]		None	AVG_EN	RESOLU-TION	DIFFEREN TIAL_EN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	DSI_OUT_ EN	None [30:24]						

Bits	Name	Description
31	DSI_OUT_EN	DSI data output enable for this channel. - 0: the conversion result for this channel is only stored in the channel data register and the corresponding CHAN_DATA_VALID bit is set. - 1: the conversion result for this channel is stored in the channel data register and the corresponding CHAN_DATA_VALID bit is set. The same data (same formating), together with the channel number, is sent out on the DSI communication channel for processing in UDBs. Default Value: 0
13 : 12	SAMPLE_TIME_SEL	Sample time select: select which of the 4 global sample times to use for this channel Default Value: 0
10	AVG_EN	Averaging enable for this channel. If set the AVG_CNT and AVG_SHIFT settings are used for sampling the addressed pin(s) Default Value: 0
9	RESOLUTION	Resolution for this channel. When AVG_EN is set this bit is ignored and always a 12-bit resolution (or highest resolution allowed by wounding) is used for this channel. Default Value: 0

(continued)

		0x0: MAXRES: The maximum resolution is used for this channel (maximum resolution depends on wounding). **0x1: SUBRES:** The resolution specified by SUB_RESOLUTION in the SAR_SAMPLE_CTRL register is used for this channel.
8	DIFFERENTIAL_EN	Differential enable for this channel. - 0: The voltage on the addressed pin is measured (Single-ended) and the resulting value is stored in the corresponding data register. - 1: The differential voltage on the addressed pin pair is measured and the resulting value is stored in the corresponding data register. (PIN_ADDR[0] is ignored). Default Value: 0
6 : 4	PORT_ADDR	Address of the port that contains the pin to be sampled by this channel. Default Value: 0 **0x0: SARMUX:** SARMUX pins. **0x1: CTB0:** CTB0 **0x2: CTB1:** CTB1 **0x3: CTB2:** CTB2 **0x4: CTB3:** CTB3 **0x5: AROUTE_VIRT2:** AROUTE virtual port2 (VPORT2) **0x6: AROUTE_VIRT1:** AROUTE virtual port1 (VPORT1) **0x7: SARMUX_VIRT:** SARMUX virtual port (VPORT0)
2 : 0	PIN_ADDR	Address of the pin to be sampled by this channel. If differential is enabled then PIN_ADDR[0] is ignored and considered to be 0, i.e. PIN_ADDR points to the even pin of a pin pair. For differential the even pin of the pair is connected to Vplus and the odd pin of the pair is connected to Vminus. Default Value: 0

27.1.22 SAR_CHAN_CONFIG12

Channel configuration register.

Address: 0x403A00B0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	PORT_ADDR [6:4]			None	PIN_ADDR [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW		None	RW	RW	RW
HW Access	None		R		None	R	R	R
Name	None [15:14]		SAMPLE_TIME_SEL [13:12]		None	AVG_EN	RESOLU-TION	DIFFEREN TIAL_EN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	DSI_OUT_ EN	None [30:24]						

Bits	Name	Description
31	DSI_OUT_EN	DSI data output enable for this channel. - 0: the conversion result for this channel is only stored in the channel data register and the corresponding CHAN_DATA_VALID bit is set. - 1: the conversion result for this channel is stored in the channel data register and the corresponding CHAN_DATA_VALID bit is set. The same data (same formating), together with the channel number, is sent out on the DSI communication channel for processing in UDBs. Default Value: 0
13 : 12	SAMPLE_TIME_SEL	Sample time select: select which of the 4 global sample times to use for this channel Default Value: 0
10	AVG_EN	Averaging enable for this channel. If set the AVG_CNT and AVG_SHIFT settings are used for sampling the addressed pin(s) Default Value: 0
9	RESOLUTION	Resolution for this channel. When AVG_EN is set this bit is ignored and always a 12-bit resolution (or highest resolution allowed by wounding) is used for this channel. Default Value: 0

(continued)

		0x0: MAXRES: The maximum resolution is used for this channel (maximum resolution depends on wounding). **0x1: SUBRES:** The resolution specified by SUB_RESOLUTION in the SAR_SAMPLE_CTRL register is used for this channel.
8	DIFFERENTIAL_EN	Differential enable for this channel. - 0: The voltage on the addressed pin is measured (Single-ended) and the resulting value is stored in the corresponding data register. - 1: The differential voltage on the addressed pin pair is measured and the resulting value is stored in the corresponding data register. (PIN_ADDR[0] is ignored). Default Value: 0
6 : 4	PORT_ADDR	Address of the port that contains the pin to be sampled by this channel. Default Value: 0 **0x0: SARMUX:** SARMUX pins. **0x1: CTB0:** CTB0 **0x2: CTB1:** CTB1 **0x3: CTB2:** CTB2 **0x4: CTB3:** CTB3 **0x5: AROUTE_VIRT2:** AROUTE virtual port2 (VPORT2) **0x6: AROUTE_VIRT1:** AROUTE virtual port1 (VPORT1) **0x7: SARMUX_VIRT:** SARMUX virtual port (VPORT0)
2 : 0	PIN_ADDR	Address of the pin to be sampled by this channel. If differential is enabled then PIN_ADDR[0] is ignored and considered to be 0, i.e. PIN_ADDR points to the even pin of a pin pair. For differential the even pin of the pair is connected to Vplus and the odd pin of the pair is connected to Vminus. Default Value: 0

27.1.23 SAR_CHAN_CONFIG13

Channel configuration register.

Address: 0x403A00B4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	PORT_ADDR [6:4]			None	PIN_ADDR [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW		None	RW	RW	RW
HW Access	None		R		None	R	R	R
Name	None [15:14]		SAMPLE_TIME_SEL [13:12]		None	AVG_EN	RESOLU-TION	DIFFEREN TIAL_EN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	DSI_OUT_ EN	None [30:24]						

Bits	Name	Description
31	DSI_OUT_EN	DSI data output enable for this channel. - 0: the conversion result for this channel is only stored in the channel data register and the corresponding CHAN_DATA_VALID bit is set. - 1: the conversion result for this channel is stored in the channel data register and the corresponding CHAN_DATA_VALID bit is set. The same data (same formating), together with the channel number, is sent out on the DSI communication channel for processing in UDBs. Default Value: 0
13 : 12	SAMPLE_TIME_SEL	Sample time select: select which of the 4 global sample times to use for this channel Default Value: 0
10	AVG_EN	Averaging enable for this channel. If set the AVG_CNT and AVG_SHIFT settings are used for sampling the addressed pin(s) Default Value: 0
9	RESOLUTION	Resolution for this channel. When AVG_EN is set this bit is ignored and always a 12-bit resolution (or highest resolution allowed by wounding) is used for this channel. Default Value: 0

(continued)

		0x0: MAXRES: The maximum resolution is used for this channel (maximum resolution depends on wounding). **0x1: SUBRES:** The resolution specified by SUB_RESOLUTION in the SAR_SAMPLE_CTRL register is used for this channel.
8	DIFFERENTIAL_EN	Differential enable for this channel. - 0: The voltage on the addressed pin is measured (Single-ended) and the resulting value is stored in the corresponding data register. - 1: The differential voltage on the addressed pin pair is measured and the resulting value is stored in the corresponding data register. (PIN_ADDR[0] is ignored). Default Value: 0
6 : 4	PORT_ADDR	Address of the port that contains the pin to be sampled by this channel. Default Value: 0 **0x0: SARMUX:** SARMUX pins. **0x1: CTB0:** CTB0 **0x2: CTB1:** CTB1 **0x3: CTB2:** CTB2 **0x4: CTB3:** CTB3 **0x5: AROUTE_VIRT2:** AROUTE virtual port2 (VPORT2) **0x6: AROUTE_VIRT1:** AROUTE virtual port1 (VPORT1) **0x7: SARMUX_VIRT:** SARMUX virtual port (VPORT0)
2 : 0	PIN_ADDR	Address of the pin to be sampled by this channel. If differential is enabled then PIN_ADDR[0] is ignored and considered to be 0, i.e. PIN_ADDR points to the even pin of a pin pair. For differential the even pin of the pair is connected to Vplus and the odd pin of the pair is connected to Vminus. Default Value: 0

27.1.24 SAR_CHAN_CONFIG14

Channel configuration register.

Address: 0x403A00B8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	PORT_ADDR [6:4]			None	PIN_ADDR [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW		None	RW	RW	RW
HW Access	None		R		None	R	R	R
Name	None [15:14]		SAMPLE_TIME_SEL [13:12]		None	AVG_EN	RESOLU-TION	DIFFEREN TIAL_EN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	DSI_OUT_ EN	None [30:24]						

Bits	Name	Description
31	DSI_OUT_EN	DSI data output enable for this channel. - 0: the conversion result for this channel is only stored in the channel data register and the corresponding CHAN_DATA_VALID bit is set. - 1: the conversion result for this channel is stored in the channel data register and the corresponding CHAN_DATA_VALID bit is set. The same data (same formating), together with the channel number, is sent out on the DSI communication channel for processing in UDBs. Default Value: 0
13 : 12	SAMPLE_TIME_SEL	Sample time select: select which of the 4 global sample times to use for this channel Default Value: 0
10	AVG_EN	Averaging enable for this channel. If set the AVG_CNT and AVG_SHIFT settings are used for sampling the addressed pin(s) Default Value: 0
9	RESOLUTION	Resolution for this channel. When AVG_EN is set this bit is ignored and always a 12-bit resolution (or highest resolution allowed by wounding) is used for this channel. Default Value: 0

(continued)

		0x0: MAXRES: The maximum resolution is used for this channel (maximum resolution depends on wounding). **0x1: SUBRES:** The resolution specified by SUB_RESOLUTION in the SAR_SAMPLE_CTRL register is used for this channel.
8	DIFFERENTIAL_EN	Differential enable for this channel. - 0: The voltage on the addressed pin is measured (Single-ended) and the resulting value is stored in the corresponding data register. - 1: The differential voltage on the addressed pin pair is measured and the resulting value is stored in the corresponding data register. (PIN_ADDR[0] is ignored). Default Value: 0
6 : 4	PORT_ADDR	Address of the port that contains the pin to be sampled by this channel. Default Value: 0 **0x0: SARMUX:** SARMUX pins. **0x1: CTB0:** CTB0 **0x2: CTB1:** CTB1 **0x3: CTB2:** CTB2 **0x4: CTB3:** CTB3 **0x5: AROUTE_VIRT2:** AROUTE virtual port2 (VPORT2) **0x6: AROUTE_VIRT1:** AROUTE virtual port1 (VPORT1) **0x7: SARMUX_VIRT:** SARMUX virtual port (VPORT0)
2 : 0	PIN_ADDR	Address of the pin to be sampled by this channel. If differential is enabled then PIN_ADDR[0] is ignored and considered to be 0, i.e. PIN_ADDR points to the even pin of a pin pair. For differential the even pin of the pair is connected to Vplus and the odd pin of the pair is connected to Vminus. Default Value: 0

27.1.25 SAR_CHAN_CONFIG15

Channel configuration register.

Address: 0x403A00BC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	PORT_ADDR [6:4]			None	PIN_ADDR [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW		None	RW	RW	RW
HW Access	None		R		None	R	R	R
Name	None [15:14]		SAMPLE_TIME_SEL [13:12]		None	AVG_EN	RESOLU-TION	DIFFEREN TIAL_EN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	DSI_OUT_ EN	None [30:24]						

Bits	Name	Description
31	DSI_OUT_EN	DSI data output enable for this channel. - 0: the conversion result for this channel is only stored in the channel data register and the corresponding CHAN_DATA_VALID bit is set. - 1: the conversion result for this channel is stored in the channel data register and the corresponding CHAN_DATA_VALID bit is set. The same data (same formating), together with the channel number, is sent out on the DSI communication channel for processing in UDBs. Default Value: 0
13 : 12	SAMPLE_TIME_SEL	Sample time select: select which of the 4 global sample times to use for this channel Default Value: 0
10	AVG_EN	Averaging enable for this channel. If set the AVG_CNT and AVG_SHIFT settings are used for sampling the addressed pin(s) Default Value: 0
9	RESOLUTION	Resolution for this channel. When AVG_EN is set this bit is ignored and always a 12-bit resolution (or highest resolution allowed by wounding) is used for this channel. Default Value: 0

(continued)

		0x0: MAXRES: The maximum resolution is used for this channel (maximum resolution depends on wounding). **0x1: SUBRES:** The resolution specified by SUB_RESOLUTION in the SAR_SAMPLE_CTRL register is used for this channel.
8	DIFFERENTIAL_EN	Differential enable for this channel. - 0: The voltage on the addressed pin is measured (Single-ended) and the resulting value is stored in the corresponding data register. - 1: The differential voltage on the addressed pin pair is measured and the resulting value is stored in the corresponding data register. (PIN_ADDR[0] is ignored). Default Value: 0
6 : 4	PORT_ADDR	Address of the port that contains the pin to be sampled by this channel. Default Value: 0 **0x0: SARMUX:** SARMUX pins. **0x1: CTB0:** CTB0 **0x2: CTB1:** CTB1 **0x3: CTB2:** CTB2 **0x4: CTB3:** CTB3 **0x5: AROUTE_VIRT2:** AROUTE virtual port2 (VPORT2) **0x6: AROUTE_VIRT1:** AROUTE virtual port1 (VPORT1) **0x7: SARMUX_VIRT:** SARMUX virtual port (VPORT0)
2 : 0	PIN_ADDR	Address of the pin to be sampled by this channel. If differential is enabled then PIN_ADDR[0] is ignored and considered to be 0, i.e. PIN_ADDR points to the even pin of a pin pair. For differential the even pin of the pair is connected to Vplus and the odd pin of the pair is connected to Vminus. Default Value: 0

27.1.26 SAR_CHAN_WORK0

Channel working data register

Address: 0x403A0100

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	WORK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	WORK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	CHAN_WORK_VALID_MIR	None [30:24]						

Bits	Name	Description
31	CHAN_WORK_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_WORK_VALID register Default Value: 0
15 : 0	WORK	SAR conversion working data of the channel. The data is written here right after sampling this channel. Default Value: Undefined

27.1.27 SAR_CHAN_WORK1

Channel working data register

Address: 0x403A0104

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	WORK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	WORK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	CHAN_WORK_VALID_MIR	None [30:24]						

Bits	Name	Description
31	CHAN_WORK_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_WORK_VALID register Default Value: 0
15 : 0	WORK	SAR conversion working data of the channel. The data is written here right after sampling this channel. Default Value: Undefined

27.1.28 SAR_CHAN_WORK2

Channel working data register

Address: 0x403A0108

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	WORK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	WORK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	CHAN_WORK_VALID_MIR	None [30:24]						

Bits	Name	Description
31	CHAN_WORK_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_WORK_VALID register Default Value: 0
15 : 0	WORK	SAR conversion working data of the channel. The data is written here right after sampling this channel. Default Value: Undefined

27.1.29 SAR_CHAN_WORK3

Channel working data register

Address: 0x403A010C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	WORK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	WORK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	CHAN_WORK_VALID_MIR	None [30:24]						

Bits	Name	Description
31	CHAN_WORK_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_WORK_VALID register Default Value: 0
15 : 0	WORK	SAR conversion working data of the channel. The data is written here right after sampling this channel. Default Value: Undefined

27.1.30 SAR_CHAN_WORK4

Channel working data register

Address: 0x403A0110

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	WORK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	WORK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	CHAN_WORK_VALID_MIR	None [30:24]						

Bits	Name	Description
31	CHAN_WORK_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_WORK_VALID register Default Value: 0
15 : 0	WORK	SAR conversion working data of the channel. The data is written here right after sampling this channel. Default Value: Undefined

27.1.31 SAR_CHAN_WORK5

Channel working data register

Address: 0x403A0114

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	WORK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	WORK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	CHAN_WORK_VALID_MIR	None [30:24]						

Bits	Name	Description
31	CHAN_WORK_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_WORK_VALID register Default Value: 0
15 : 0	WORK	SAR conversion working data of the channel. The data is written here right after sampling this channel. Default Value: Undefined

27.1.32 SAR_CHAN_WORK6

Channel working data register

Address: 0x403A0118

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	WORK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	WORK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	CHAN_WORK_VALID_MIR	None [30:24]						

Bits	Name	Description
31	CHAN_WORK_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_WORK_VALID register Default Value: 0
15 : 0	WORK	SAR conversion working data of the channel. The data is written here right after sampling this channel. Default Value: Undefined

27.1.33 SAR_CHAN_WORK7

Channel working data register

Address: 0x403A011C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	WORK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	WORK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	CHAN_WORK_VALID_MIR	None [30:24]						

Bits	Name	Description
31	CHAN_WORK_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_WORK_VALID register Default Value: 0
15 : 0	WORK	SAR conversion working data of the channel. The data is written here right after sampling this channel. Default Value: Undefined

27.1.34 SAR_CHAN_WORK8

Channel working data register

Address: 0x403A0120

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	WORK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	WORK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	CHAN_WORK_VALID_MIR	None [30:24]						

Bits	Name	Description
31	CHAN_WORK_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_WORK_VALID register Default Value: 0
15 : 0	WORK	SAR conversion working data of the channel. The data is written here right after sampling this channel. Default Value: Undefined

27.1.35 SAR_CHAN_WORK9

Channel working data register

Address: 0x403A0124

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	WORK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	WORK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	CHAN_WORK_VALID_MIR	None [30:24]						

Bits	Name	Description
31	CHAN_WORK_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_WORK_VALID register Default Value: 0
15 : 0	WORK	SAR conversion working data of the channel. The data is written here right after sampling this channel. Default Value: Undefined

27.1.36 SAR_CHAN_WORK10

Channel working data register

Address: 0x403A0128

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	WORK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	WORK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	CHAN_WORK_VALID_MIR	None [30:24]						

Bits	Name	Description
31	CHAN_WORK_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_WORK_VALID register Default Value: 0
15 : 0	WORK	SAR conversion working data of the channel. The data is written here right after sampling this channel. Default Value: Undefined

27.1.37 SAR_CHAN_WORK11

Channel working data register

Address: 0x403A012C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	WORK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	WORK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	CHAN_WORK_VALID_MIR	None [30:24]						

Bits	Name	Description
31	CHAN_WORK_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_WORK_VALID register Default Value: 0
15 : 0	WORK	SAR conversion working data of the channel. The data is written here right after sampling this channel. Default Value: Undefined

27.1.38 SAR_CHAN_WORK12

Channel working data register

Address: 0x403A0130

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	WORK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	WORK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	CHAN_WORK_VALID_MIR	None [30:24]						

Bits	Name	Description
31	CHAN_WORK_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_WORK_VALID register Default Value: 0
15 : 0	WORK	SAR conversion working data of the channel. The data is written here right after sampling this channel. Default Value: Undefined

27.1.39 SAR_CHAN_WORK13

Channel working data register

Address: 0x403A0134

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	WORK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	WORK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	CHAN_WORK_VALID_MIR	None [30:24]						

Bits	Name	Description
31	CHAN_WORK_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_WORK_VALID register Default Value: 0
15 : 0	WORK	SAR conversion working data of the channel. The data is written here right after sampling this channel. Default Value: Undefined

27.1.40 SAR_CHAN_WORK14

Channel working data register

Address: 0x403A0138

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	WORK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	WORK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	CHAN_WORK_VALID_MIR	None [30:24]						

Bits	Name	Description
31	CHAN_WORK_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_WORK_VALID register Default Value: 0
15 : 0	WORK	SAR conversion working data of the channel. The data is written here right after sampling this channel. Default Value: Undefined

27.1.41 SAR_CHAN_WORK15

Channel working data register

Address: 0x403A013C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	WORK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	WORK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	CHAN_WORK_VALID_MIR	None [30:24]						

Bits	Name	Description
31	CHAN_WORK_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_WORK_VALID register Default Value: 0
15 : 0	WORK	SAR conversion working data of the channel. The data is written here right after sampling this channel. Default Value: Undefined

27.1.42 SAR_CHAN_RESULT0

Channel result data register

Address: 0x403A0180

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	RESULT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	RESULT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	R	None				
HW Access	W	W	W	None				
Name	CHAN_RESULT_VALID_MIR	RANGE_INTR_MIR	SATURATE_INTR_MIR	None [28:24]				

Bits	Name	Description
31	CHAN_RESULT_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_RESULT_VALID register Default Value: 0
30	RANGE_INTR_MIR	mirror bit of corresponding bit in SAR_RANGE_INTR register Default Value: 0
29	SATURATE_INTR_MIR	mirror bit of corresponding bit in SAR_SATURATE_INTR register Default Value: 0
15 : 0	RESULT	SAR conversion result of the channel. The data is copied here from the WORK field after all enabled channels in this scan have been sampled. Default Value: Undefined

27.1.43 SAR_CHAN_RESULT1

Channel result data register

Address: 0x403A0184

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	RESULT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	RESULT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	R	None				
HW Access	W	W	W	None				
Name	CHAN_RESULT_VALID_MIR	RANGE_INTR_MIR	SATURATE_INTR_MIR	None [28:24]				

Bits	Name	Description
31	CHAN_RESULT_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_RESULT_VALID register Default Value: 0
30	RANGE_INTR_MIR	mirror bit of corresponding bit in SAR_RANGE_INTR register Default Value: 0
29	SATURATE_INTR_MIR	mirror bit of corresponding bit in SAR_SATURATE_INTR register Default Value: 0
15 : 0	RESULT	SAR conversion result of the channel. The data is copied here from the WORK field after all enabled channels in this scan have been sampled. Default Value: Undefined

27.1.44 SAR_CHAN_RESULT2

Channel result data register

Address: 0x403A0188

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	RESULT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	RESULT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	R	None				
HW Access	W	W	W	None				
Name	CHAN_RESULT_VALID_MIR	RANGE_INTR_MIR	SATURATE_INTR_MIR	None [28:24]				

Bits	Name	Description
31	CHAN_RESULT_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_RESULT_VALID register Default Value: 0
30	RANGE_INTR_MIR	mirror bit of corresponding bit in SAR_RANGE_INTR register Default Value: 0
29	SATURATE_INTR_MIR	mirror bit of corresponding bit in SAR_SATURATE_INTR register Default Value: 0
15 : 0	RESULT	SAR conversion result of the channel. The data is copied here from the WORK field after all enabled channels in this scan have been sampled. Default Value: Undefined

27.1.45 SAR_CHAN_RESULT3

Channel result data register

Address: 0x403A018C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	RESULT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	RESULT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	R	None				
HW Access	W	W	W	None				
Name	CHAN_RESULT_VALID_MIR	RANGE_INTR_MIR	SATURATE_INTR_MIR	None [28:24]				

Bits	Name	Description
31	CHAN_RESULT_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_RESULT_VALID register Default Value: 0
30	RANGE_INTR_MIR	mirror bit of corresponding bit in SAR_RANGE_INTR register Default Value: 0
29	SATURATE_INTR_MIR	mirror bit of corresponding bit in SAR_SATURATE_INTR register Default Value: 0
15 : 0	RESULT	SAR conversion result of the channel. The data is copied here from the WORK field after all enabled channels in this scan have been sampled. Default Value: Undefined

27.1.46 SAR_CHAN_RESULT4

Channel result data register

Address: 0x403A0190

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	RESULT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	RESULT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	R	None				
HW Access	W	W	W	None				
Name	CHAN_RESULT_VALID_MIR	RANGE_INTR_MIR	SATURATE_INTR_MIR	None [28:24]				

Bits	Name	Description
31	CHAN_RESULT_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_RESULT_VALID register Default Value: 0
30	RANGE_INTR_MIR	mirror bit of corresponding bit in SAR_RANGE_INTR register Default Value: 0
29	SATURATE_INTR_MIR	mirror bit of corresponding bit in SAR_SATURATE_INTR register Default Value: 0
15 : 0	RESULT	SAR conversion result of the channel. The data is copied here from the WORK field after all enabled channels in this scan have been sampled. Default Value: Undefined

27.1.47 SAR_CHAN_RESULT5

Channel result data register

Address: 0x403A0194

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	RESULT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	RESULT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	R	None				
HW Access	W	W	W	None				
Name	CHAN_RESULT_VALID_MIR	RANGE_INTR_MIR	SATURATE_INTR_MIR	None [28:24]				

Bits	Name	Description
31	CHAN_RESULT_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_RESULT_VALID register Default Value: 0
30	RANGE_INTR_MIR	mirror bit of corresponding bit in SAR_RANGE_INTR register Default Value: 0
29	SATURATE_INTR_MIR	mirror bit of corresponding bit in SAR_SATURATE_INTR register Default Value: 0
15 : 0	RESULT	SAR conversion result of the channel. The data is copied here from the WORK field after all enabled channels in this scan have been sampled. Default Value: Undefined

27.1.48 SAR_CHAN_RESULT6

Channel result data register

Address: 0x403A0198

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	RESULT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	RESULT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	R	None				
HW Access	W	W	W	None				
Name	CHAN_RESULT_VALID_MIR	RANGE_INTR_MIR	SATURATE_INTR_MIR	None [28:24]				

Bits	Name	Description
31	CHAN_RESULT_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_RESULT_VALID register Default Value: 0
30	RANGE_INTR_MIR	mirror bit of corresponding bit in SAR_RANGE_INTR register Default Value: 0
29	SATURATE_INTR_MIR	mirror bit of corresponding bit in SAR_SATURATE_INTR register Default Value: 0
15 : 0	RESULT	SAR conversion result of the channel. The data is copied here from the WORK field after all enabled channels in this scan have been sampled. Default Value: Undefined

27.1.49 SAR_CHAN_RESULT7

Channel result data register

Address: 0x403A019C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	RESULT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	RESULT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	R	None				
HW Access	W	W	W	None				
Name	CHAN_RESULT_VALID_MIR	RANGE_INTR_MIR	SATURATE_INTR_MIR	None [28:24]				

Bits	Name	Description
31	CHAN_RESULT_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_RESULT_VALID register Default Value: 0
30	RANGE_INTR_MIR	mirror bit of corresponding bit in SAR_RANGE_INTR register Default Value: 0
29	SATURATE_INTR_MIR	mirror bit of corresponding bit in SAR_SATURATE_INTR register Default Value: 0
15 : 0	RESULT	SAR conversion result of the channel. The data is copied here from the WORK field after all enabled channels in this scan have been sampled. Default Value: Undefined

27.1.50 SAR_CHAN_RESULT8

Channel result data register

Address: 0x403A01A0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	RESULT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	RESULT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	R	None				
HW Access	W	W	W	None				
Name	CHAN_RESULT_VALID_MIR	RANGE_INTR_MIR	SATURATE_INTR_MIR	None [28:24]				

Bits	Name	Description
31	CHAN_RESULT_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_RESULT_VALID register Default Value: 0
30	RANGE_INTR_MIR	mirror bit of corresponding bit in SAR_RANGE_INTR register Default Value: 0
29	SATURATE_INTR_MIR	mirror bit of corresponding bit in SAR_SATURATE_INTR register Default Value: 0
15 : 0	RESULT	SAR conversion result of the channel. The data is copied here from the WORK field after all enabled channels in this scan have been sampled. Default Value: Undefined

27.1.51 SAR_CHAN_RESULT9

Channel result data register

Address: 0x403A01A4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	RESULT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	RESULT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	R	None				
HW Access	W	W	W	None				
Name	CHAN_RESULT_VALID_MIR	RANGE_INTR_MIR	SATURATE_INTR_MIR	None [28:24]				

Bits	Name	Description
31	CHAN_RESULT_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_RESULT_VALID register Default Value: 0
30	RANGE_INTR_MIR	mirror bit of corresponding bit in SAR_RANGE_INTR register Default Value: 0
29	SATURATE_INTR_MIR	mirror bit of corresponding bit in SAR_SATURATE_INTR register Default Value: 0
15 : 0	RESULT	SAR conversion result of the channel. The data is copied here from the WORK field after all enabled channels in this scan have been sampled. Default Value: Undefined

27.1.52 SAR_CHAN_RESULT10

Channel result data register

Address: 0x403A01A8

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	RESULT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	RESULT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	R	None				
HW Access	W	W	W	None				
Name	CHAN_RESULT_VALID_MIR	RANGE_INTR_MIR	SATURATE_INTR_MIR	None [28:24]				

Bits	Name	Description
31	CHAN_RESULT_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_RESULT_VALID register Default Value: 0
30	RANGE_INTR_MIR	mirror bit of corresponding bit in SAR_RANGE_INTR register Default Value: 0
29	SATURATE_INTR_MIR	mirror bit of corresponding bit in SAR_SATURATE_INTR register Default Value: 0
15 : 0	RESULT	SAR conversion result of the channel. The data is copied here from the WORK field after all enabled channels in this scan have been sampled. Default Value: Undefined

27.1.53 SAR_CHAN_RESULT11

Channel result data register

Address: 0x403A01AC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	RESULT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	RESULT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	R	None				
HW Access	W	W	W	None				
Name	CHAN_RESULT_VALID_MIR	RANGE_INTR_MIR	SATURATE_INTR_MIR	None [28:24]				

Bits	Name	Description
31	CHAN_RESULT_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_RESULT_VALID register Default Value: 0
30	RANGE_INTR_MIR	mirror bit of corresponding bit in SAR_RANGE_INTR register Default Value: 0
29	SATURATE_INTR_MIR	mirror bit of corresponding bit in SAR_SATURATE_INTR register Default Value: 0
15 : 0	RESULT	SAR conversion result of the channel. The data is copied here from the WORK field after all enabled channels in this scan have been sampled. Default Value: Undefined

27.1.54 SAR_CHAN_RESULT12

Channel result data register

Address: 0x403A01B0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	RESULT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	RESULT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	R	None				
HW Access	W	W	W	None				
Name	CHAN_RESULT_VALID_MIR	RANGE_INTR_MIR	SATURATE_INTR_MIR	None [28:24]				

Bits	Name	Description
31	CHAN_RESULT_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_RESULT_VALID register Default Value: 0
30	RANGE_INTR_MIR	mirror bit of corresponding bit in SAR_RANGE_INTR register Default Value: 0
29	SATURATE_INTR_MIR	mirror bit of corresponding bit in SAR_SATURATE_INTR register Default Value: 0
15 : 0	RESULT	SAR conversion result of the channel. The data is copied here from the WORK field after all enabled channels in this scan have been sampled. Default Value: Undefined

27.1.55 SAR_CHAN_RESULT13

Channel result data register

Address: 0x403A01B4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	RESULT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	RESULT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	R	None				
HW Access	W	W	W	None				
Name	CHAN_RESULT_VALID_MIR	RANGE_INTR_MIR	SATURATE_INTR_MIR	None [28:24]				

Bits	Name	Description
31	CHAN_RESULT_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_RESULT_VALID register Default Value: 0
30	RANGE_INTR_MIR	mirror bit of corresponding bit in SAR_RANGE_INTR register Default Value: 0
29	SATURATE_INTR_MIR	mirror bit of corresponding bit in SAR_SATURATE_INTR register Default Value: 0
15 : 0	RESULT	SAR conversion result of the channel. The data is copied here from the WORK field after all enabled channels in this scan have been sampled. Default Value: Undefined

27.1.56 SAR_CHAN_RESULT14

Channel result data register

Address: 0x403A01B8

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	RESULT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	RESULT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	R	None				
HW Access	W	W	W	None				
Name	CHAN_RESULT_VALID_MIR	RANGE_INTR_MIR	SATURATE_INTR_MIR	None [28:24]				

Bits	Name	Description
31	CHAN_RESULT_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_RESULT_VALID register Default Value: 0
30	RANGE_INTR_MIR	mirror bit of corresponding bit in SAR_RANGE_INTR register Default Value: 0
29	SATURATE_INTR_MIR	mirror bit of corresponding bit in SAR_SATURATE_INTR register Default Value: 0
15 : 0	RESULT	SAR conversion result of the channel. The data is copied here from the WORK field after all enabled channels in this scan have been sampled. Default Value: Undefined

27.1.57 SAR_CHAN_RESULT15

Channel result data register

Address: 0x403A01BC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	RESULT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	RESULT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	R	None				
HW Access	W	W	W	None				
Name	CHAN_RESULT_VALID_MIR	RANGE_INTR_MIR	SATURATE_INTR_MIR	None [28:24]				

Bits	Name	Description
31	CHAN_RESULT_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_RESULT_VALID register Default Value: 0
30	RANGE_INTR_MIR	mirror bit of corresponding bit in SAR_RANGE_INTR register Default Value: 0
29	SATURATE_INTR_MIR	mirror bit of corresponding bit in SAR_SATURATE_INTR register Default Value: 0
15 : 0	RESULT	SAR conversion result of the channel. The data is copied here from the WORK field after all enabled channels in this scan have been sampled. Default Value: Undefined

27.1.58 SAR_CHAN_WORK_VALID

Channel working data register valid bits

Address: 0x403A0200

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	CHAN_WORK_VALID [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	CHAN_WORK_VALID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CHAN_WORK_VALID	If set the corresponding WORK data is valid, i.e. was already sampled during the current scan. Default Value: 0

27.1.59 SAR_CHAN_RESULT_VALID

Channel result data register valid bits

Address: 0x403A0204

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	CHAN_RESULT_VALID [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	CHAN_RESULT_VALID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CHAN_RESULT_VALID	If set the corresponding RESULT data is valid, i.e. was sampled during the last scan. Default Value: 0

27.1.60 SAR_STATUS

Current status of internal SAR registers (mostly for debug)

Address: 0x403A0208

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			R				
HW Access	None			W				
Name	None [7:5]			CUR_CHAN [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	None					
HW Access	W	W	None					
Name	BUSY	SW_VREF_NEG	None [29:24]					

Bits	Name	Description
31	BUSY	If high then the SAR is busy with a conversion. This bit is always high when CONTINUOUS is set. Firmware should wait for this bit to be low before putting the SAR in power down. Default Value: 0
30	SW_VREF_NEG	the current switch status, including DSI and sequencer controls, of the switch in the SARADC that shorts NEG with VREF input (see NEG_SEL). Default Value: 0
4 : 0	CUR_CHAN	current channel being sampled (channel 16 indicates the injection channel), only valid if BUSY. Default Value: 0

27.1.61 SAR_AVG_STAT

Current averaging status (for debug)

Address: 0x403A020C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	CUR_AVG_ACCU [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	CUR_AVG_ACCU [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None				R			
HW Access	None				W			
Name	None [23:20]				CUR_AVG_ACCU [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	CUR_AVG_CNT [31:24]							

Bits	Name	Description
31 : 24	CUR_AVG_CNT	the current value of the averaging counter. Note that the value shown is updated after the sampling time and therefore runs ahead of the accumulator update. Default Value: 0
19 : 0	CUR_AVG_ACCU	the current value of the averaging accumulator Default Value: 0

27.1.62 SAR_INTR

Interrupt request register.

Address: 0x403A0210

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
Name	INJ_COLLISION_INTR	INJ_RANGE_INTR	INJ_SATURATE_INTR	INJ_EOC_INTR	DSI_COLLISION_INTR	FW_COLLISION_INTR	OVERFLOW_INTR	EOS_INTR

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	INJ_COLLISION_INTR	Injection Collision Interrupt: hardware sets this interrupt when the injection trigger signal is asserted (INJ_START_EN==1 && INJ_TAILGATING==0) while the SAR is BUSY. Raising this interrupt is delayed to when the sampling of the injection channel has been completed, i.e. not when the preceeding scan with which this trigger collided is completed. When this interrupt is set it implies that the injection channel was sampled later than was intended. Write with '1' to clear bit. Default Value: 0
6	INJ_RANGE_INTR	Injection Range detect Interrupt: hardware sets this interrupt if the injection conversion result (after averaging) met the condition specified by the SAR_RANGE registers. Write with '1' to clear bit. Default Value: 0
5	INJ_SATURATE_INTR	Injection Saturation Interrupt: hardware sets this interrupt if an injection conversion result (before averaging) is either 0x000 or 0xFFF (for 12-bit resolution), this is an indication that the ADC likely saturated. Write with '1' to clear bit. Default Value: 0
4	INJ_EOC_INTR	Injection End of Conversion Interrupt: hardware sets this interrupt after completing the conversion for the injection channel (irrespective of if tailgating was used). Write with '1' to clear bit. Default Value: 0

(continued)

3	DSI_COLLISION_INTR	DSI Collision Interrupt: hardware sets this interrupt when the DSI trigger signal is asserted while the SAR is BUSY. Raising this interrupt is delayed to when the scan caused by the DSI trigger has been completed, i.e. not when the preceeding scan with which this trigger collided is completed. When this interrupt is set it implies that the channels were sampled later than was intended (jitter). Write with '1' to clear bit. Default Value: 0
2	FW_COLLISION_INTR	Firmware Collision Interrupt: hardware sets this interrupt when FW_TRIGGER is asserted while the SAR is BUSY. Raising this interrupt is delayed to when the scan caused by the FW_TRIGGER has been completed, i.e. not when the preceeding scan with which this trigger collided is completed. When this interrupt is set it implies that the channels were sampled later than was intended (jitter). Write with '1' to clear bit. Default Value: 0
1	OVERFLOW_INTR	Overflow Interrupt: hardware sets this interrupt when it sets a new EOS_INTR while that bit was not yet cleared by the firmware. Write with '1' to clear bit. Default Value: 0
0	EOS_INTR	End Of Scan Interrupt: hardware sets this interrupt after completing a scan of all the enabled channels. Write with '1' to clear bit. Default Value: 0

27.1.63 SAR_INTR_SET

Interrupt set request register

Address: 0x403A0214

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	A	A	A	A	A	A	A	A
Name	INJ_COLLISION_SET	INJ_RANGE_SET	INJ_SATURATE_SET	INJ_EOC_SET	DSI_COLLISION_SET	FW_COLLISION_SET	OVERFLOW_SET	EOS_SET

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	INJ_COLLISION_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
6	INJ_RANGE_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
5	INJ_SATURATE_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
4	INJ_EOC_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
3	DSI_COLLISION_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
2	FW_COLLISION_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
1	OVERFLOW_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

(continued)

0	EOS_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

27.1.64 SAR_INTR_MASK

Interrupt mask register.

Address: 0x403A0218

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	INJ_COLLISION_MASK	INJ_RANGE_MASK	INJ_SATURATE_MASK	INJ_EOC_MASK	DSI_COLLISION_MASK	FW_COLLISION_MASK	OVERFLOW_MASK	EOS_MASK

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	INJ_COLLISION_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
6	INJ_RANGE_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
5	INJ_SATURATE_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
4	INJ_EOC_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
3	DSI_COLLISION_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	FW_COLLISION_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	OVERFLOW_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0

(continued)

0	EOS_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0

27.1.65 SAR_INTR_MASKED

Interrupt masked request register

Address: 0x403A021C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	INJ_COLLISION_MASKED	INJ_RANGE_MASKED	INJ_SATURATE_MASKED	INJ_EOC_MASKED	DSI_COLLISION_MASKED	FW_COLLISION_MASKED	OVERFLOW_MASKED	EOS_MASKED

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	INJ_COLLISION_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
6	INJ_RANGE_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
5	INJ_SATURATE_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
4	INJ_EOC_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
3	DSI_COLLISION_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
2	FW_COLLISION_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
1	OVERFLOW_MASKED	Logical and of corresponding request and mask bits. Default Value: 0

(continued)

0	EOS_MASKED	Logical and of corresponding request and mask bits. Default Value: 0

27.1.66 SAR_SATURATE_INTR

Saturate interrupt request register.

Address: 0x403A0220

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C							
HW Access	RW1S							
Name	SATURATE_INTR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1C							
HW Access	RW1S							
Name	SATURATE_INTR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	SATURATE_INTR	Saturate Interrupt: hardware sets this interrupt for each channel if a conversion result (before averaging) of that channel is either 0x000 or 0xFFF (for 12-bit resolution), this is an indication that the ADC likely saturated. Write with '1' to clear bit. Default Value: 0

27.1.67 SAR_SATURATE_INTR_SET

Saturate interrupt set request register

Address: 0x403A0224

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S							
HW Access	A							
Name	SATURATE_SET [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1S							
HW Access	A							
Name	SATURATE_SET [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	SATURATE_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

27.1.68 SAR_SATURATE_INTR_MASK

Saturate interrupt mask register.

Address: 0x403A0228

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SATURATE_MASK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	SATURATE_MASK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	SATURATE_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0

27.1.69 SAR_SATURATE_INTR_MASKED

Saturate interrupt masked request register

Address: 0x403A022C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	SATURATE_MASKED [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	SATURATE_MASKED [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	SATURATE_MASKED	Logical and of corresponding request and mask bits. Default Value: 0

27.1.70 SAR_RANGE_INTR

Range detect interrupt request register.

Address: 0x403A0230

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C							
HW Access	RW1S							
Name	RANGE_INTR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1C							
HW Access	RW1S							
Name	RANGE_INTR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	RANGE_INTR	Range detect Interrupt: hardware sets this interrupt for each channel if the conversion result (after averaging) of that channel met the condition specified by the SAR_RANGE registers. Write with '1' to clear bit. Default Value: 0

27.1.71 SAR_RANGE_INTR_SET

Range detect interrupt set request register

Address: 0x403A0234

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S							
HW Access	A							
Name	RANGE_SET [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1S							
HW Access	A							
Name	RANGE_SET [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	RANGE_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

27.1.72 SAR_RANGE_INTR_MASK

Range detect interrupt mask register.

Address: 0x403A0238

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	RANGE_MASK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	RANGE_MASK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	RANGE_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0

27.1.73 SAR_RANGE_INTR_MASKED

Range interrupt masked request register

Address: 0x403A023C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	RANGE_MASKED [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	RANGE_MASKED [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	RANGE_MASKED	Logical and of corresponding request and mask bits. Default Value: 0

27.1.74 SAR_INTR_CAUSE

Interrupt cause register

Address: 0x403A0240

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	INJ_COLLISION_MASKED_MIR	INJ_RANGE_MASKED_MIR	INJ_SATURATE_MASKED_MIR	INJ_EOC_MASKED_MIR	DSI_COLLISION_MASKED_MIR	FW_COLLISION_MASKED_MIR	OVERFLOW_MASKED_MIR	EOS_MASKED_MIR

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	None					
HW Access	W	W	None					
Name	RANGE_MASKED_RED	SATURATE_MASKED_RED	None [29:24]					

Bits	Name	Description
31	RANGE_MASKED_RED	Reduction OR of all SAR_RANGE_INTR_MASKED bits Default Value: 0
30	SATURATE_MASKED_RED	Reduction OR of all SAR_SATURATION_INTR_MASKED bits Default Value: 0
7	INJ_COLLISION_MASKED_MIR	Mirror copy of corresponding bit in SAR_INTR_MASKED Default Value: 0
6	INJ_RANGE_MASKED_MIR	Mirror copy of corresponding bit in SAR_INTR_MASKED Default Value: 0
5	INJ_SATURATE_MASKED_MIR	Mirror copy of corresponding bit in SAR_INTR_MASKED Default Value: 0
4	INJ_EOC_MASKED_MIR	Mirror copy of corresponding bit in SAR_INTR_MASKED Default Value: 0

(continued)

3	DSI_COLLISION_MASKED_MIR	Mirror copy of corresponding bit in SAR_INTR_MASKED Default Value: 0
2	FW_COLLISION_MASKED_MIR	Mirror copy of corresponding bit in SAR_INTR_MASKED Default Value: 0
1	OVERFLOW_MASKED_MIR	Mirror copy of corresponding bit in SAR_INTR_MASKED Default Value: 0
0	EOS_MASKED_MIR	Mirror copy of corresponding bit in SAR_INTR_MASKED Default Value: 0

27.1.75 SAR_INJ_CHAN_CONFIG

Injection channel configuration register.

Address: 0x403A0280

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	INJ_PORT_ADDR [6:4]			None	INJ_PIN_ADDR [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW		None	RW	RW	RW
HW Access	None		R		None	R	R	R
Name	None [15:14]		INJ_SAMPLE_TIME_SEL [13:12]		None	INJ_AVG_EN	INJ_RESOLUTION	INJ_DIFFERENTIAL_EN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1S	RW	None					
HW Access	RW1C	R	None					
Name	INJ_START_EN	INJ_TAILGATING	None [29:24]					

Bits	Name	Description
31	INJ_START_EN	Set by firmware to enable the injection channel. If INJ_TAILGATING is not set this bit also functions as trigger for this channel. Cleared by hardware after this channel has been sampled (i.e. this channel is always one shot even if CONTINUOUS is set). Also cleared if the SAR is disabled. Default Value: 0
30	INJ_TAILGATING	Injection channel tailgating. - 0: no tailgating for this channel, SAR is immediately triggered when the INJ_START_EN bit is set. - 1: injection channel tailgating. The addressed pin is sampled after the next trigger and after all enabled channels have been scanned. Default Value: 0
13 : 12	INJ_SAMPLE_TIME_SEL	Injection sample time select: select which of the 4 global sample times to use for this channel Default Value: 0
10	INJ_AVG_EN	Averaging enable for this channel. If set the AVG_CNT and AVG_SHIFT settings are used for sampling the addressed pin(s) Default Value: 0

(continued)

9	INJ_RESOLUTION	Resolution for this channel. Default Value: 0 **0x0: 12B:** 12-bit resolution is used for this channel. **0x1: SUBRES:** The resolution specified by SUB_RESOLUTION in the SAR_SAMPLE_CTRL register is used for this channel.
8	INJ_DIFFERENTIAL_EN	Differential enable for this channel. - 0: The voltage on the addressed pin is measured (Single-ended) and the resulting value is stored in the corresponding data register. - 1: The differential voltage on the addressed pin pair is measured and the resulting value is stored in the corresponding data register. (INJ_PIN_ADDR[0] is ignored). Default Value: 0
6 : 4	INJ_PORT_ADDR	Address of the port that contains the pin to be sampled by this channel. Default Value: 0 **0x0: SARMUX:** SARMUX pins. **0x1: CTB0:** CTB0 **0x2: CTB1:** CTB1 **0x3: CTB2:** CTB2 **0x4: CTB3:** CTB3 **0x6: AROUTE_VIRT:** AROUTE virtual port **0x7: SARMUX_VIRT:** SARMUX virtual port
2 : 0	INJ_PIN_ADDR	Address of the pin to be sampled by this injection channel. If differential is enabled then PIN_ADDR[0] is ignored and considered to be 0, i.e. PIN_ADDR points to the even pin of a pin pair. Default Value: 0

27.1.76 SAR_INJ_RESULT

Injection channel result register

Address: 0x403A0290

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	INJ_RESULT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	INJ_RESULT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	R	R	None			
HW Access	W	W	W	W	None			
Name	INJ_EOC_INTR_MIR	INJ_RANGE_INTR_MIR	INJ_SATURATE_INTR_MIR	INJ_COLLISION_INTR_MIR	None [27:24]			

Bits	Name	Description
31	INJ_EOC_INTR_MIR	mirror bit of corresponding bit in SAR_INTR register Default Value: 0
30	INJ_RANGE_INTR_MIR	mirror bit of corresponding bit in SAR_INTR register Default Value: 0
29	INJ_SATURATE_INTR_MIR	mirror bit of corresponding bit in SAR_INTR register Default Value: 0
28	INJ_COLLISION_INTR_MIR	mirror bit of corresponding bit in SAR_INTR register Default Value: 0
15 : 0	INJ_RESULT	SAR conversion result of the channel. Default Value: Undefined

27.1.77 SAR_MUX_SWITCH0

SARMUX Firmware switch controls

Address: 0x403A0300

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
Name	MUX_FW_P7_VPLUS	MUX_FW_P6_VPLUS	MUX_FW_P5_VPLUS	MUX_FW_P4_VPLUS	MUX_FW_P3_VPLUS	MUX_FW_P2_VPLUS	MUX_FW_P1_VPLUS	MUX_FW_P0_VPLUS

Bits	15	14	13	12	11	10	9	8
SW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
Name	MUX_FW_P7_VMINUS	MUX_FW_P6_VMINUS	MUX_FW_P5_VMINUS	MUX_FW_P4_VMINUS	MUX_FW_P3_VMINUS	MUX_FW_P2_VMINUS	MUX_FW_P1_VMINUS	MUX_FW_P0_VMINUS

Bits	23	22	21	20	19	18	17	16
SW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
Name	MUX_FW_SARBUS1_VPLUS	MUX_FW_SARBUS0_VPLUS	MUX_FW_AMUXBUSB_VMINUS	MUX_FW_AMUXBUSA_VMINUS	MUX_FW_AMUXBUSB_VPLUS	MUX_FW_AMUXBUSA_VPLUS	MUX_FW_TEMP_VPLUS	MUX_FW_VSSA_VMINUS

Bits	31	30	29	28	27	26	25	24
SW Access	None		RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	None		RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
Name	None [31:30]		MUX_FW_P7_COREIO3	MUX_FW_P6_COREIO2	MUX_FW_P5_COREIO1	MUX_FW_P4_COREIO0	MUX_FW_SARBUS1_VMINUS	MUX_FW_SARBUS0_VMINUS

Bits	Name	Description
29	MUX_FW_P7_COREIO3	Firmware control: 0=open, 1=close switch between P7 and coreio3 signal. Write with '1' to set bit. Default Value: 0
28	MUX_FW_P6_COREIO2	Firmware control: 0=open, 1=close switch between P6 and coreio2 signal. Write with '1' to set bit. Default Value: 0
27	MUX_FW_P5_COREIO1	Firmware control: 0=open, 1=close switch between P5 and coreio1 signal. Write with '1' to set bit. Default Value: 0
26	MUX_FW_P4_COREIO0	Firmware control: 0=open, 1=close switch between P4 and coreio0 signal. Write with '1' to set bit. Default Value: 0
25	MUX_FW_SARBUS1_VMINUS	Firmware control: 0=open, 1=close switch between sarbus1 and vminus signal. Write with '1' to set bit. Default Value: 0

(continued)

24	MUX_FW_SARBUS0_VMINUS	Firmware control: 0=open, 1=close switch between sarbus0 and vminus signal. Write with '1' to set bit. Default Value: 0
23	MUX_FW_SARBUS1_VPLUS	Firmware control: 0=open, 1=close switch between sarbus1 and vplus signal. Write with '1' to set bit. Default Value: 0
22	MUX_FW_SARBUS0_VPLUS	Firmware control: 0=open, 1=close switch between sarbus0 and vplus signal. Write with '1' to set bit. Default Value: 0
21	MUX_FW_AMUXBUSB_VMINUS	Firmware control: 0=open, 1=close switch between amuxbusb and vminus signal. Write with '1' to set bit. Default Value: 0
20	MUX_FW_AMUXBUSA_VMINUS	Firmware control: 0=open, 1=close switch between amuxbusa and vminus signal. Write with '1' to set bit. Default Value: 0
19	MUX_FW_AMUXBUSB_VPLUS	Firmware control: 0=open, 1=close switch between amuxbusb and vplus signal. Write with '1' to set bit. Default Value: 0
18	MUX_FW_AMUXBUSA_VPLUS	Firmware control: 0=open, 1=close switch between amuxbusa and vplus signal. Write with '1' to set bit. Default Value: 0
17	MUX_FW_TEMP_VPLUS	Firmware control: 0=open, 1=close switch between temperature sensor and vplus signal, also powers on the temperature sensor. Write with '1' to set bit. Default Value: 0
16	MUX_FW_VSSA_VMINUS	Firmware control: 0=open, 1=close switch between vssa_kelvin and vminus signal. Write with '1' to set bit. Default Value: 0
15	MUX_FW_P7_VMINUS	Firmware control: 0=open, 1=close switch between pin P7 and vminus signal. Write with '1' to set bit. Default Value: 0
14	MUX_FW_P6_VMINUS	Firmware control: 0=open, 1=close switch between pin P6 and vminus signal. Write with '1' to set bit. Default Value: 0
13	MUX_FW_P5_VMINUS	Firmware control: 0=open, 1=close switch between pin P5 and vminus signal. Write with '1' to set bit. Default Value: 0
12	MUX_FW_P4_VMINUS	Firmware control: 0=open, 1=close switch between pin P4 and vminus signal. Write with '1' to set bit. Default Value: 0
11	MUX_FW_P3_VMINUS	Firmware control: 0=open, 1=close switch between pin P3 and vminus signal. Write with '1' to set bit. Default Value: 0
10	MUX_FW_P2_VMINUS	Firmware control: 0=open, 1=close switch between pin P2 and vminus signal. Write with '1' to set bit. Default Value: 0
9	MUX_FW_P1_VMINUS	Firmware control: 0=open, 1=close switch between pin P1 and vminus signal. Write with '1' to set bit. Default Value: 0

(continued)

8	MUX_FW_P0_VMINUS	Firmware control: 0=open, 1=close switch between pin P0 and vminus signal. Write with '1' to set bit. Default Value: 0
7	MUX_FW_P7_VPLUS	Firmware control: 0=open, 1=close switch between pin P7 and vplus signal. Write with '1' to set bit. Default Value: 0
6	MUX_FW_P6_VPLUS	Firmware control: 0=open, 1=close switch between pin P6 and vplus signal. Write with '1' to set bit. Default Value: 0
5	MUX_FW_P5_VPLUS	Firmware control: 0=open, 1=close switch between pin P5 and vplus signal. Write with '1' to set bit. Default Value: 0
4	MUX_FW_P4_VPLUS	Firmware control: 0=open, 1=close switch between pin P4 and vplus signal. Write with '1' to set bit. Default Value: 0
3	MUX_FW_P3_VPLUS	Firmware control: 0=open, 1=close switch between pin P3 and vplus signal. Write with '1' to set bit. Default Value: 0
2	MUX_FW_P2_VPLUS	Firmware control: 0=open, 1=close switch between pin P2 and vplus signal. Write with '1' to set bit. Default Value: 0
1	MUX_FW_P1_VPLUS	Firmware control: 0=open, 1=close switch between pin P1 and vplus signal. Write with '1' to set bit. Default Value: 0
0	MUX_FW_P0_VPLUS	Firmware control: 0=open, 1=close switch between pin P0 and vplus signal. Write with '1' to set bit. Default Value: 0

27.1.78 SAR_MUX_SWITCH_CLEAR0

SARMUX Firmware switch control clear

Address: 0x403A0304

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	A	A	A	A	A	A	A	A
Name	MUX_FW_P7_VPLUS	MUX_FW_P6_VPLUS	MUX_FW_P5_VPLUS	MUX_FW_P4_VPLUS	MUX_FW_P3_VPLUS	MUX_FW_P2_VPLUS	MUX_FW_P1_VPLUS	MUX_FW_P0_VPLUS

Bits	15	14	13	12	11	10	9	8
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	A	A	A	A	A	A	A	A
Name	MUX_FW_P7_VMINUS	MUX_FW_P6_VMINUS	MUX_FW_P5_VMINUS	MUX_FW_P4_VMINUS	MUX_FW_P3_VMINUS	MUX_FW_P2_VMINUS	MUX_FW_P1_VMINUS	MUX_FW_P0_VMINUS

Bits	23	22	21	20	19	18	17	16
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	A	A	A	A	A	A	A	A
Name	MUX_FW_SARBUS1_VPLUS	MUX_FW_SARBUS0_VPLUS	MUX_FW_AMUXBUSB_VMINUS	MUX_FW_AMUXBUSA_VMINUS	MUX_FW_AMUXBUSB_VPLUS	MUX_FW_AMUXBUSA_VPLUS	MUX_FW_TEMP_VPLUS	MUX_FW_VSSA_VMINUS

Bits	31	30	29	28	27	26	25	24
SW Access	None		RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	None		A	A	A	A	A	A
Name	None [31:30]		MUX_FW_P7_COREIO3	MUX_FW_P6_COREIO2	MUX_FW_P5_COREIO1	MUX_FW_P4_COREIO0	MUX_FW_SARBUS1_VMINUS	MUX_FW_SARBUS0_VMINUS

Bits	Name	Description
29	MUX_FW_P7_COREIO3	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
28	MUX_FW_P6_COREIO2	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
27	MUX_FW_P5_COREIO1	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
26	MUX_FW_P4_COREIO0	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
25	MUX_FW_SARBUS1_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0

(continued)

24	MUX_FW_SARBUS0_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
23	MUX_FW_SARBUS1_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
22	MUX_FW_SARBUS0_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
21	MUX_FW_AMUXBUSB_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
20	MUX_FW_AMUXBUSA_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
19	MUX_FW_AMUXBUSB_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
18	MUX_FW_AMUXBUSA_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
17	MUX_FW_TEMP_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
16	MUX_FW_VSSA_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
15	MUX_FW_P7_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
14	MUX_FW_P6_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
13	MUX_FW_P5_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
12	MUX_FW_P4_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
11	MUX_FW_P3_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
10	MUX_FW_P2_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
9	MUX_FW_P1_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
8	MUX_FW_P0_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
7	MUX_FW_P7_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
6	MUX_FW_P6_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
5	MUX_FW_P5_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
4	MUX_FW_P4_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
3	MUX_FW_P3_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0

(continued)

2	MUX_FW_P2_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
1	MUX_FW_P1_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
0	MUX_FW_P0_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0

27.1.79 SAR_MUX_SWITCH1

SARMUX Firmware switch controls

Address: 0x403A0308

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1S	RW1S	RW1S	RW1S
HW Access	None				RW1C	RW1C	RW1C	RW1C
Name	None [7:4]				MUX_FW_ADFT1_SARBUS1	MUX_FW_ADFT0_SARBUS0	MUX_FW_P5_DFT_INM	MUX_FW_P4_DFT_INP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	MUX_FW_ADFT1_SARBUS1	Firmware control: 0=open, 1=close switch between adft1 signal and sarbus1 signal. Write with '1' to set bit. Default Value: 0
2	MUX_FW_ADFT0_SARBUS0	Firmware control: 0=open, 1=close switch between adft0 signal and sarbus0 signal. Write with '1' to set bit. Default Value: 0
1	MUX_FW_P5_DFT_INM	Firmware control: 0=open, 1=close switch between P5 pin and dft_inm signal. Write with '1' to set bit. Default Value: 0
0	MUX_FW_P4_DFT_INP	Firmware control: 0=open, 1=close switch between P4 pin and dft_inp signal. Write with '1' to set bit. Default Value: 0

27.1.80 SAR_MUX_SWITCH_CLEAR1

SARMUX Firmware switch control clear

Address: 0x403A030C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1C	RW1C	RW1C	RW1C
HW Access	None				A	A	A	A
Name	None [7:4]				MUX_FW_ADFT1_SARBUS1	MUX_FW_ADFT0_SARBUS0	MUX_FW_P5_DFT_INM	MUX_FW_P4_DFT_INP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	MUX_FW_ADFT1_SARBUS1	Write '1' to clear corresponding bit in MUX_SWITCH1 Default Value: 0
2	MUX_FW_ADFT0_SARBUS0	Write '1' to clear corresponding bit in MUX_SWITCH1 Default Value: 0
1	MUX_FW_P5_DFT_INM	Write '1' to clear corresponding bit in MUX_SWITCH1 Default Value: 0
0	MUX_FW_P4_DFT_INP	Write '1' to clear corresponding bit in MUX_SWITCH1 Default Value: 0

27.1.81 SAR_MUX_SWITCH_HW_CTRL

SARMUX switch hardware control

Address: 0x403A0340

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	MUX_HW_CTRL_P7	MUX_HW_CTRL_P6	MUX_HW_CTRL_P5	MUX_HW_CTRL_P4	MUX_HW_CTRL_P3	MUX_HW_CTRL_P2	MUX_HW_CTRL_P1	MUX_HW_CTRL_P0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	None		RW	RW	RW	RW
HW Access	R	R	None		R	R	R	R
Name	MUX_HW_CTRL_SARBUS1	MUX_HW_CTRL_SARBUS0	None [21:20]		MUX_HW_CTRL_AMUXBUSB	MUX_HW_CTRL_AMUXBUSA	MUX_HW_CTRL_TEMP	MUX_HW_CTRL_VSSA

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23	MUX_HW_CTRL_SARBUS1	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for sarbus1 switches. Default Value: 0
22	MUX_HW_CTRL_SARBUS0	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for sarbus0 switches. Default Value: 0
19	MUX_HW_CTRL_AMUXBUSB	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for amuxbusb switches. Default Value: 0
18	MUX_HW_CTRL_AMUXBUSA	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for amuxbusa switches. Default Value: 0
17	MUX_HW_CTRL_TEMP	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for temp switch. Default Value: 0

(continued)

16	MUX_HW_CTRL_VSSA	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for vssa switch. Default Value: 0
7	MUX_HW_CTRL_P7	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for pin P7 switches. Default Value: 0
6	MUX_HW_CTRL_P6	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for pin P6 switches. Default Value: 0
5	MUX_HW_CTRL_P5	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for pin P5 switches. Default Value: 0
4	MUX_HW_CTRL_P4	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for pin P4 switches. Default Value: 0
3	MUX_HW_CTRL_P3	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for pin P3 switches. Default Value: 0
2	MUX_HW_CTRL_P2	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for pin P2 switches. Default Value: 0
1	MUX_HW_CTRL_P1	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for pin P1 switches. Default Value: 0
0	MUX_HW_CTRL_P0	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for pin P0 switches. Default Value: 0

27.1.82 SAR_MUX_SWITCH_STATUS

SARMUX switch status

Address: 0x403A0348

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	MUX_FW_P7_VPLUS	MUX_FW_P6_VPLUS	MUX_FW_P5_VPLUS	MUX_FW_P4_VPLUS	MUX_FW_P3_VPLUS	MUX_FW_P2_VPLUS	MUX_FW_P1_VPLUS	MUX_FW_P0_VPLUS

Bits	15	14	13	12	11	10	9	8
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	MUX_FW_P7_VMINUS	MUX_FW_P6_VMINUS	MUX_FW_P5_VMINUS	MUX_FW_P4_VMINUS	MUX_FW_P3_VMINUS	MUX_FW_P2_VMINUS	MUX_FW_P1_VMINUS	MUX_FW_P0_VMINUS

Bits	23	22	21	20	19	18	17	16
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	MUX_FW_SARBUS1_VPLUS	MUX_FW_SARBUS0_VPLUS	MUX_FW_AMUXBUSB_VMINUS	MUX_FW_AMUXBUSA_VMINUS	MUX_FW_AMUXBUSB_VPLUS	MUX_FW_AMUXBUSA_VPLUS	MUX_FW_TEMP_VPLUS	MUX_FW_VSSA_VMINUS

Bits	31	30	29	28	27	26	25	24
SW Access	None						R	R
HW Access	None						W	W
Name	None [31:26]						MUX_FW_SARBUS1_VMINUS	MUX_FW_SARBUS0_VMINUS

Bits	Name	Description
25	MUX_FW_SARBUS1_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
24	MUX_FW_SARBUS0_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
23	MUX_FW_SARBUS1_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
22	MUX_FW_SARBUS0_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
21	MUX_FW_AMUXBUSB_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0

(continued)

20	MUX_FW_AMUXBUSA_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
19	MUX_FW_AMUXBUSB_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
18	MUX_FW_AMUXBUSA_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
17	MUX_FW_TEMP_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
16	MUX_FW_VSSA_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
15	MUX_FW_P7_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
14	MUX_FW_P6_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
13	MUX_FW_P5_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
12	MUX_FW_P4_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
11	MUX_FW_P3_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
10	MUX_FW_P2_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
9	MUX_FW_P1_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
8	MUX_FW_P0_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
7	MUX_FW_P7_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
6	MUX_FW_P6_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
5	MUX_FW_P5_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
4	MUX_FW_P4_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
3	MUX_FW_P3_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
2	MUX_FW_P2_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
1	MUX_FW_P1_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
0	MUX_FW_P0_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0

27.1.83 SAR_PUMP_CTRL

Switch pump control

Address: 0x403A0380

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							CLOCK_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	ENABLED	None [30:24]						

Bits	Name	Description
31	ENABLED	0=disabled: pump output is VDDA_PUMP, 1=enabled: pump output is boosted. Default Value: 0
0	CLOCK_SEL	Clock select: 0=external clock, 1=internal clock (deprecated). Default Value: 0

27.1.84 SAR_ANA_TRIM

Analog trim register.

Address: 0x403A0F00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW		
HW Access	None				R	R		
Name	None [7:4]				TRIMUNIT	CAP_TRIM [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	TRIMUNIT	Attenuation cap trimming Default Value: 0
2 : 0	CAP_TRIM	Attenuation cap trimming Default Value: 0

27.1.85 SAR_WOUNDING

SAR wounding register

Address: 0x403A0F04

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1S	
HW Access	None						R	
Name	None [7:2]						WOUND_RESOLUTION [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1 : 0	WOUND_RESOLUTION	Maximum SAR resolution allowed Default Value: 0 **0x0: 12BIT:** unwounded: up to full 12-bit SAR resolution allowed **0x1: 10BIT:** wounded: max resolution upto 10-bit SAR resolution allowed **0x2: 8BIT:** wounded: only 8-bit SAR resolution allowed **0x3: 8BIT_TOO:** wounded: only 8-bit SAR resolution allowed

28 SCB Registers

This section discusses the SCB registers. It lists all the registers in mapping tables, in address order.

28.1 Register Details

Register Name	Address
SCB0_CTRL	0x40240000
SCB0_STATUS	0x40240004
SCB0_SPI_CTRL	0x40240020
SCB0_SPI_STATUS	0x40240024
SCB0_UART_CTRL	0x40240040
SCB0_UART_TX_CTRL	0x40240044
SCB0_UART_RX_CTRL	0x40240048
SCB0_UART_RX_STATUS	0x4024004C
SCB0_UART_FLOW_CTRL	0x40240050
SCB0_I2C_CTRL	0x40240060
SCB0_I2C_STATUS	0x40240064
SCB0_I2C_M_CMD	0x40240068
SCB0_I2C_S_CMD	0x4024006C
SCB0_I2C_CFG	0x40240070
SCB0_TX_CTRL	0x40240200
SCB0_TX_FIFO_CTRL	0x40240204
SCB0_TX_FIFO_STATUS	0x40240208
SCB0_TX_FIFO_WR	0x40240240
SCB0_RX_CTRL	0x40240300
SCB0_RX_FIFO_CTRL	0x40240304
SCB0_RX_FIFO_STATUS	0x40240308
SCB0_RX_MATCH	0x40240310
SCB0_RX_FIFO_RD	0x40240340
SCB0_RX_FIFO_RD_SILENT	0x40240344
SCB0_EZ_DATA0	0x40240400
SCB0_EZ_DATA1	0x40240404
SCB0_EZ_DATA2	0x40240408

Register Name	Address
SCB0_EZ_DATA3	0x4024040C
SCB0_EZ_DATA4	0x40240410
SCB0_EZ_DATA5	0x40240414
SCB0_EZ_DATA6	0x40240418
SCB0_EZ_DATA7	0x4024041C
SCB0_EZ_DATA8	0x40240420
SCB0_EZ_DATA9	0x40240424
SCB0_EZ_DATA10	0x40240428
SCB0_EZ_DATA11	0x4024042C
SCB0_EZ_DATA12	0x40240430
SCB0_EZ_DATA13	0x40240434
SCB0_EZ_DATA14	0x40240438
SCB0_EZ_DATA15	0x4024043C
SCB0_EZ_DATA16	0x40240440
SCB0_EZ_DATA17	0x40240444
SCB0_EZ_DATA18	0x40240448
SCB0_EZ_DATA19	0x4024044C
SCB0_EZ_DATA20	0x40240450
SCB0_EZ_DATA21	0x40240454
SCB0_EZ_DATA22	0x40240458
SCB0_EZ_DATA23	0x4024045C
SCB0_EZ_DATA24	0x40240460
SCB0_EZ_DATA25	0x40240464
SCB0_EZ_DATA26	0x40240468
SCB0_EZ_DATA27	0x4024046C
SCB0_EZ_DATA28	0x40240470
SCB0_EZ_DATA29	0x40240474
SCB0_EZ_DATA30	0x40240478
SCB0_EZ_DATA31	0x4024047C
SCB0_INTR_CAUSE	0x40240E00
SCB0_INTR_I2C_EC	0x40240E80
SCB0_INTR_I2C_EC_MASK	0x40240E88
SCB0_INTR_I2C_EC_MASKED	0x40240E8C
SCB0_INTR_SPI_EC	0x40240EC0
SCB0_INTR_SPI_EC_MASK	0x40240EC8
SCB0_INTR_SPI_EC_MASKED	0x40240ECC
SCB0_INTR_M	0x40240F00
SCB0_INTR_M_SET	0x40240F04
SCB0_INTR_M_MASK	0x40240F08
SCB0_INTR_M_MASKED	0x40240F0C
SCB0_INTR_S	0x40240F40
SCB0_INTR_S_SET	0x40240F44

Register Name	Address
SCB0_INTR_S_MASK	0x40240F48
SCB0_INTR_S_MASKED	0x40240F4C
SCB0_INTR_TX	0x40240F80
SCB0_INTR_TX_SET	0x40240F84
SCB0_INTR_TX_MASK	0x40240F88
SCB0_INTR_TX_MASKED	0x40240F8C
SCB0_INTR_RX	0x40240FC0
SCB0_INTR_RX_SET	0x40240FC4
SCB0_INTR_RX_MASK	0x40240FC8
SCB0_INTR_RX_MASKED	0x40240FCC
SCB1_CTRL	0x40250000
SCB1_STATUS	0x40250004
SCB1_SPI_CTRL	0x40250020
SCB1_SPI_STATUS	0x40250024
SCB1_UART_CTRL	0x40250040
SCB1_UART_TX_CTRL	0x40250044
SCB1_UART_RX_CTRL	0x40250048
SCB1_UART_RX_STATUS	0x4025004C
SCB1_UART_FLOW_CTRL	0x40250050
SCB1_I2C_CTRL	0x40250060
SCB1_I2C_STATUS	0x40250064
SCB1_I2C_M_CMD	0x40250068
SCB1_I2C_S_CMD	0x4025006C
SCB1_I2C_CFG	0x40250070
SCB1_TX_CTRL	0x40250200
SCB1_TX_FIFO_CTRL	0x40250204
SCB1_TX_FIFO_STATUS	0x40250208
SCB1_TX_FIFO_WR	0x40250240
SCB1_RX_CTRL	0x40250300
SCB1_RX_FIFO_CTRL	0x40250304
SCB1_RX_FIFO_STATUS	0x40250308
SCB1_RX_MATCH	0x40250310
SCB1_RX_FIFO_RD	0x40250340
SCB1_RX_FIFO_RD_SILENT	0x40250344
SCB1_EZ_DATA0	0x40250400
SCB1_EZ_DATA1	0x40250404
SCB1_EZ_DATA2	0x40250408
SCB1_EZ_DATA3	0x4025040C
SCB1_EZ_DATA4	0x40250410
SCB1_EZ_DATA5	0x40250414
SCB1_EZ_DATA6	0x40250418
SCB1_EZ_DATA7	0x4025041C

Register Name	Address
SCB1_EZ_DATA8	0x40250420
SCB1_EZ_DATA9	0x40250424
SCB1_EZ_DATA10	0x40250428
SCB1_EZ_DATA11	0x4025042C
SCB1_EZ_DATA12	0x40250430
SCB1_EZ_DATA13	0x40250434
SCB1_EZ_DATA14	0x40250438
SCB1_EZ_DATA15	0x4025043C
SCB1_EZ_DATA16	0x40250440
SCB1_EZ_DATA17	0x40250444
SCB1_EZ_DATA18	0x40250448
SCB1_EZ_DATA19	0x4025044C
SCB1_EZ_DATA20	0x40250450
SCB1_EZ_DATA21	0x40250454
SCB1_EZ_DATA22	0x40250458
SCB1_EZ_DATA23	0x4025045C
SCB1_EZ_DATA24	0x40250460
SCB1_EZ_DATA25	0x40250464
SCB1_EZ_DATA26	0x40250468
SCB1_EZ_DATA27	0x4025046C
SCB1_EZ_DATA28	0x40250470
SCB1_EZ_DATA29	0x40250474
SCB1_EZ_DATA30	0x40250478
SCB1_EZ_DATA31	0x4025047C
SCB1_INTR_CAUSE	0x40250E00
SCB1_INTR_I2C_EC	0x40250E80
SCB1_INTR_I2C_EC_MASK	0x40250E88
SCB1_INTR_I2C_EC_MASKED	0x40250E8C
SCB1_INTR_SPI_EC	0x40250EC0
SCB1_INTR_SPI_EC_MASK	0x40250EC8
SCB1_INTR_SPI_EC_MASKED	0x40250ECC
SCB1_INTR_M	0x40250F00
SCB1_INTR_M_SET	0x40250F04
SCB1_INTR_M_MASK	0x40250F08
SCB1_INTR_M_MASKED	0x40250F0C
SCB1_INTR_S	0x40250F40
SCB1_INTR_S_SET	0x40250F44
SCB1_INTR_S_MASK	0x40250F48
SCB1_INTR_S_MASKED	0x40250F4C
SCB1_INTR_TX	0x40250F80
SCB1_INTR_TX_SET	0x40250F84
SCB1_INTR_TX_MASK	0x40250F88

Register Name	Address
SCB1_INTR_TX_MASKED	0x40250F8C
SCB1_INTR_RX	0x40250FC0
SCB1_INTR_RX_SET	0x40250FC4
SCB1_INTR_RX_MASK	0x40250FC8
SCB1_INTR_RX_MASKED	0x40250FCC

28.1.1 SCB0_CTRL

Generic control register.

Address: 0x40240000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				OVS [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [15:12]				BYTE_MODE	EZ_MODE	EC_OP_MODE	EC_AM_MODE

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [23:18]						BLOCK	ADDR_ACCEPT

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None					RW	
HW Access	R	None					R	
Name	ENABLED	None [30:26]					MODE [25:24]	

Bits	Name	Description
31	ENABLED	IP enabled ('1') or not ('0'). The proper order in which to initialize the IP is as follows: - Program protocol specific information using SPI_CTRL, UART_CTRL (and UART_TX_CTRL and UART_RX_CTRL) or I2C_CTRL. This includes selection of a submode, master/slave functionality and transmitter/receiver functionality when applicable. - Program generic transmitter (TX_CTRL) and receiver (RX_CTRL) information. This includes enabling of the transmitter and receiver functionality. - Program transmitter FIFO (TX_FIFO_CTRL) and receiver FIFO (RX_FIFO_CTRL) information. - Program CTRL to enable IP, select the specific operation mode and oversampling factor. When the IP is enabled, no control information should be changed. Changes should be made AFTER disabling the IP, e.g. to modify the operation mode (from I2C to SPI) or to go from externally to internally clocked. The change takes effect after the IP is re-enabled. Note that disabling the IP will cause re-initialization of the design and associated state is lost (e.g. FIFO content). Default Value: 0
25 : 24	MODE	Mode of operation (3: Reserved) Default Value: 3 **0x0: I2C:** Inter-Integrated Circuits (I2C) mode.

(continued)

		0x1: SPI: Serial Peripheral Interface (SPI) mode. **0x2: UART:** Universal Asynchronous Receiver/Transmitter (UART) mode.
17	BLOCK	Only used in externally clocked mode. If the externally clocked logic and the MMIO SW accesses to EZ memory coincide/collide, this bit determines whether a SW access should block and result in bus wait states ('BLOCK is 1') or not (BLOCK is '0'). IF BLOCK is 0 and the accesses collide, MMIO read operations return 0xffff:ffff and MMIO write operations are ignored. Colliding accesses are registered as interrupt causes: field BLOCKED of MMIO registers INTR_TX and INTR_RX. Default Value: 0
16	ADDR_ACCEPT	Determines whether a received matching address is accepted in the RX FIFO ('1') or not ('0'). In I2C mode, this field is used to allow the slave to put the received slave address or general call address in the RX FIFO. Note that a received matching address is put in the RX FIFO when ADDR_ACCEPT is '1' for both I2C read and write transfers. In multi-processor UART receiver mode, this field is used to allow the receiver to put the received address in the RX FIFO. Note: non-matching addresses are never put in the RX FIFO. Default Value: 0
11	BYTE_MODE	Determines the number of bits per FIFO data element: '0': 16-bit FIFO data elements. '1': 8-bit FIFO data elements. This mode doubles the amount of FIFO entries, but TX_CTRL.DATA_WIDTH and RX_CTRL.DATA_WIDTH are restricted to [0, 7]. Default Value: 0
10	EZ_MODE	Non EZ mode ('0') or EZ mode ('1'). In EZ mode, a meta protocol is applied to the serial interface protocol. This meta protocol adds meaning to the data frames transferred by the serial interface protocol: a data frame can represent a memory address, a write memory data element or a read memory data element. EZ mode is only used for synchronous serial interface protocols: SPI and I2C. In SPI mode, only Motorola submode (all Motorola modes: 0, 1, 2, 3) is supported and the transmitter should use continuous data frames; i.e. data frames mot seperated by slave deselection. This mode is only applicable to slave functionality. In EZ mode, the slave can read from and write to an addressable memory structure of 32 bytes. In EZ mode, data frames should 8-bit in size and should be transmitted and received with the Most Significant Bit (MSB) first. In UART mode this field should be '0'. Default Value: 0
9	EC_OP_MODE	Internally clocked mode ('0') or externally clocked mode ('1') operation. In internally clocked mode, the serial interface protocols run off the peripheral clock. In externally clocked mode, the serial interface protocols run off the clock as provided by the serial interface. Externally clocked operation mode is only used for synchronous serial interface protocols (SPI and I2C) in slave mode AND EZ mode. In SPI mode, only Motorola submode (all Motorola modes: 0, 1, 2, 3) is supported. The maximum SPI slave, EZ mode bitrate is 48 Mbps (transmission and IO delays outside the IP will degrade the effective bitrate). In UART mode this field should be '0'. Default Value: 0
8	EC_AM_MODE	Internally clocked mode ('0') or externally clocked mode ('1') address matching (I2C) or selection (SPI). In internally clocked mode, the serial interface protocols run off the peripheral clock. In externally clocked mode, the serial interface protocols run off the clock as provided by the serial interface. Externally clocked mode is only used for synchronous serial interface protocols (SPI and I2C) in slave mode. In SPI mode, only Motorola submode (all Motorola modes: 0, 1, 2, 3) is supported. In UART mode this field should be '0'. Default Value: 0

(continued)

3 : 0	OVS	Serial interface bit period oversampling factor expressed in IP clock cycles. Used for SPI and UART functionality. OVS + 1 IP clock cycles constitute a single serial interface clock/bit cycle. The IP clock is provided by the programmable clock IP. This field is NOT used in externally clocked mode. If OVS is odd, the oversampling factor is even and the first and second phase of the interface clock period are the same. If OVS is even, the oversampling factor is odd and the first phase of the interface clock period is 1 peripheral clock cycle longer than the second phase of the interface clock period. In SPI master mode, the valid range is [3, 15]. At an IP frequency of 48 MHz, the maximum IP bit rate is 12 Mbps. The effective system bit rate is dependent on the external SPI slave that we communicate with. If the SPI output clock "spi_clk_out" to SPI MISO input "spi_miso_in" round trip delay is introducing significant delays (multiple "spi_clk_out" cycles), it may be necessary to increase OVS and/or to set SPI_CTRL.LATE_MISO_SAMPLE to '1' to achieve the maximum possible system bit rate. The maximum IP bit rate of 12 Mbps provides an IP centric perspective, assuming ideal (0 ns) IO cell and routing (chip and board) delay. The required IP clock/IF clock ratio increases and the calculated maximum bit rate decreases, when realistic chip and routing delays are taken into account. In SPI slave mode, the OVS field is NOT used. However, there is a frequency requirement for the IP clock wrt. the interface (IF) clock to guarantee functional correct behavior. This requirement is expressed as a ratio: IP clock/IF clock. The ratio is dependent on the setting of RX_CTRL.MEDIAN and the external SPI master's capability to support "late MISO sample" functionality (similar to our SPI master functionality represented by SPI_CTRL.LATE_MISO_SAMPLE): - MEDIAN is '0' and external SPI master has NO "late MISO sample functionality": IP clock/IF clock >= 6. At a IP frequency of 48 MHz, the maximum bit rate is 8 Mbps. - MEDIAN is '0' and external SPI master has "late MISO sample functionality": IP clock/IF clock >= 3. At a IP frequency of 48 MHz, the maximum bit rate is 16 Mbps. - MEDIAN is '1' and external SPI master has NO "late MISO sample functionality": IP clock/IF clock >= 8. At a IP frequency of 48 MHz, the maximum bit rate is 6 Mbps. - MEDIAN is '1' and external SPI master has "late MISO sample functionality": IP clock/IF clock >= 4. At a IP frequency of 48 MHz, the maximum bit rate is 12 Mbps. The maximum bit rates provide an IP centric perspective, assuming ideal (0 ns) IO cell and routing (chip and board) delay. The required IP clock/IF clock ratio increases and the calculated maximum bit rate decreases, when realistic chip and routing delays are taken into account. In UART standard submode (including LIN), the valid range is [7, 15]. In UART SmartCard submode, the valid range is [7, 15]. In UART TX IrDA submode this field indirectly specifies the oversampling. The oversampling determines the interface clock/bit cycle and the width of the pulse. Only normal transmission mode is supported, the pulse is roughly 3/16 of the bit period (for all bit rates). There is only one valid OVS value: - 0: 16 times oversampling. IP clock frequency of 16*115.2 KHz for 115.2 Kbps. IP clock frequency of 16*57.6 KHz for 57.6 Kbps. IP clock frequency of 16*38.4 KHz for 38.4 Kbps. IP clock frequency of 16*19.2 KHz for 19.2 Kbps. IP clock frequency of 16*9.6 KHz for 9.6 Kbps. IP clock frequency of 16*2.4 KHz for 2.4 Kbps. IP clock frequency of 16*1.2 KHz for 1.2 Kbps. - all other values are not used in normal mode. In UART RX IrDA submode (1.2, 2.4, 9.6, 19.2, 38.4, 57.6 and 115.2 Kbps) this field indirectly specifies the oversampling. The oversampling determines the interface clock/bit cycle and the width of the pulse. In normal transmission mode, this pulse is roughly 3/16 of the bit period (for all bit rates). In low power transmission mode, this pulse is potentially smaller (down to 1.62 us typical and 1.41 us minimal) than 3/16 of the bit period (for < 115.2 Kbps bitrates). Pulse widths greater or equal than two IP clock cycles are guaranteed to be detected by the receiver. Pulse widths less than two IP clock cycles and greater or equal than one IP clock cycle may be detected by the receiver. Pulse widths less than one IP clock cycle will not be detected by the receiver. RX_CTRL.MEDIAN should be set to '1' for IrDA receiver functionality. The IP clock (as provided by the programmable clock IP) and the oversampling together determine the IrDA bitrate. Normal mode, OVS field values (with the required IP clock frequency): - 0: 16 times oversampling. IP clock frequency of 16*115.2 KHz for 115.2 Kbps. IP clock frequency of 16*57.6 KHz for 57.6 Kbps. IP clock frequency of 16*38.4 KHz for 38.4 Kbps. IP clock frequency of 16*19.2 KHz for 19.2 Kbps. IP clock frequency of 16*9.6 KHz for 9.6 Kbps. IP clock frequency of 16*2.4 KHz for 2.4 Kbps. IP clock frequency of 16*1.2 KHz for 1.2 Kbps. - all other values are not used in normal mode. Low power mode, OVS field values (with the required IP clock frequency): - 0: 16 times oversampling. IP clock frequency of 16*115.2 KHz for 115.2 Kbps. - 1: 32 times oversampling. IP clock frequency of 32*57.6 KHz for 57.6 Kbps. - 2: 48 times oversampling. IP clock frequency of 48*38.4 KHz for 38.4 Kbps. - 3: 96 times oversampling. IP clock frequency of 96*19.2 KHz for 19.2 Kbps. - 4: 192 times oversampling. IP clock frequency of 192*9.6 KHz for 9.6 Kbps. - 5: 768 times oversampling. IP clock frequency of 768*2.4 KHz for 2.4 Kbps. - 6: 1536 times oversampling. IP clock frequency of 1536*1.2 KHz for 1.2 Kbps. - all other values are not used in low power mode. Default Value: 15

(continued)

28.1.2 SCB0_STATUS

Generic status register.

Address: 0x40240004

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							W
Name	None [7:1]							EC_BUSY

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	EC_BUSY	Inidicates whether the externally clocked logic is potentially accessing the EZ memory (this is only possible in EZ mode). This bit can be used by SW to determine whether it is safe to issue a SW access to the EZ memory (without bus wait states (a blocked SW access) or bus errors being generated). Note that the INTR_TX.BLOCKED and INTR_RX.BLOCKED interrupt causes are used to indicate whether a SW access was actually blocked by externally clocked logic. Default Value: Undefined

28.1.3 SCB0_SPI_CTRL

SPI control register.

Address: 0x40240020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		R	R	R	R	R	R
Name	None [7:6]		SCLK_CONTINUOUS	LATE_MISO_SAMPLE	CPOL	CPHA	SELECT_PRECEDE	CONTINU-OUS

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [15:12]				SSEL_POLARITY3	SSEL_POLARITY2	SSEL_POLARITY1	SSEL_POLARITY0

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							LOOPBACK

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None			RW		RW	
HW Access	R	None			R		R	
Name	MASTER_MODE	None [30:28]			SLAVE_SELECT [27:26]		MODE [25:24]	

Bits	Name	Description
31	MASTER_MODE	Master ('1') or slave ('0') mode. In master mode, transmission will commence on availability of data frames in the TX FIFO. In slave mode, when selected and there is no data frame in the TX FIFO, the slave will transmit all '1's. In both master and slave modes, received data frames will be lost if the RX FIFO is full. Default Value: 0
27 : 26	SLAVE_SELECT	Selects one of the four outgoing SPI slave select signals: - 0: Slave 0, SPI_SELECT[0]. - 1: Slave 1, SPI_SELECT[1]. - 2: Slave 2, SPI_SELECT[2]. - 3: Slave 3, SPI_SELECT[3]. Only used in master mode. The IP should be disabled when changes are made to this field. Default Value: 0
25 : 24	MODE	Submode of SPI operation (3: Reserved). Default Value: 3

		0x0: SPI_MOTOROLA: SPI Motorola submode. In master mode, when not transmitting data (SELECT is inactive), SCLK is stable at CPOL. In slave mode, when not selected, SCLK is ignored; i.e. it can be either stable or clocking. In master mode, when there is no data to transmit (TX FIFO is empty), SELECT is inactive. **0x1: SPI_TI:** SPI Texas Instruments submode. In master mode, when not transmitting data, SCLK is stable at '0'. In slave mode, when not selected, SCLK is ignored; i.e. it can be either stable or clocking. In master mode, when there is no data to transmit (TX FIFO is empty), SELECT is inactive; i.e. no pulse is generated. **0x2: SPI_NS:** SPI National Semiconducturs submode. In master mode, when not transmitting data, SCLK is stable at '0'. In slave mode, when not selected, SCLK is ignored; i.e. it can be either stable or clocking. In master mode, when there is no data to transmit (TX FIFO is empty), SELECT is inactive.
16	LOOPBACK	Local loopback control (does NOT affect the information on the pins). Only used in master mode. Not used in National Semiconductors submode. '0': the SPI master MISO line "spi_miso_in" is connected to the SPI MISO pin. '1': the SPI master MISO line "spi_miso_in" is connected to the SPI master MOSI line "spi_mosi_out". In other words, in loopback mode the SPI master receives on MISO what it transmits on MOSI. Default Value: 0
11	SSEL_POLARITY3	Slave select polarity. SSEL_POLARITY3 applies to the outgoing SPI slave select signal 3 (master mode). Default Value: 0
10	SSEL_POLARITY2	Slave select polarity. SSEL_POLARITY2 applies to the outgoing SPI slave select signal 2 (master mode). Default Value: 0
9	SSEL_POLARITY1	Slave select polarity. SSEL_POLARITY1 applies to the outgoing SPI slave select signal 1 (master mode). Default Value: 0
8	SSEL_POLARITY0	Slave select polarity. SSEL_POLARITY0 applies to the outgoing SPI slave select signal 0 (master mode) and to the incoming SPI slave select signal (slave mode). For Motorola and National Semiconductors submodes: '0': slave select is low/'0' active. '1': slave select is high/'1' active. For Texas Istruments submode: '0': high/'1' active precede/coincide pulse. '1': low/'0' active precede/coincide pulse. Default Value: 0
5	SCLK_CONTINUOUS	Only applicable in master mode. '0': SCLK is generated, when the SPI master is enabled and data is transmitted. '1': SCLK is generated, when the SPI master is enabled. This mode is useful for slave devices that use SCLK for functional operation other than just SPI functionality. Default Value: 0
4	LATE_MISO_SAMPLE	Changes the SCLK edge on which MISO is captured. Only used in master mode. When '0', the default applies (for Motorola as determined by CPOL and CPHA, for Texas Instruments on the falling edge of SCLK and for National Semiconductors on the rising edge of SCLK). When '1', the alternate clock edge is used (which comes half a SPI SCLK period later). Late sampling addresses the round trip delay associated with transmitting SCLK from the master to the slave and transmitting MISO from the slave to the master. Default Value: 0

(continued)

3	CPOL	Indicates the clock polarity. Only used in SPI Motorola submode. This field, together with the CPHA field, indicates when MOSI data is driven and MISO data is captured: - CPOL is 0: SCLK is 0 when not transmitting data. - CPOL is 1: SCLK is 1 when not transmitting data. Default Value: 0
2	CPHA	Only applicable in SPI Motorola submode. Indicates the clock phase. This field, together with the CPOL field, indicates when MOSI data is driven and MISO data is captured: - Motorola mode 0. CPOL is 0, CPHA is 0: MOSI is driven on a falling edge of SCLK. MISO is captured on a rising edge of SCLK. - Motorola mode 1. CPOL is 0, CPHA is 1: MOSI is driven on a rising edge of SCLK. MISO is captured on a falling edge of SCLK. - Motorola mode 2. CPOL is 1, CPHA is 0: MOSI is driven on a rising edge of SCLK. MISO is captured on a falling edge of SCLK. - Motorola mode 3. CPOL is 1, CPHA is 1: MOSI is driven on a falling edge of SCLK. MISO is captured on a rising edge of SCLK. Default Value: 0
1	SELECT_PRECEDE	Only used in SPI Texas Instruments' submode. When '1', the data frame start indication is a pulse on the SELECT line that precedes the transfer of the first data frame bit. When '0', the data frame start indication is a pulse on the SELECT line that coincides with the transfer of the first data frame bit. Default Value: 0
0	CONTINUOUS	Continuous SPI data transfers enabled ('1') or not ('0'). This field is used in master mode. In slave mode, both continuous and non-continuous SPI data transfers are supported independent of this field. When continuous transfers are enabled individual data frame transfers are not necessarily seperated by slave deselection (as indicated by the level or pulse on the SELECT line): if the TX FIFO has multiple data frames, data frames are send out without slave deselection. When continuous transfers are not enabled individual data frame transfers are always seperated by slave deselection: independent of the availability of TX FIFO data frames, data+G65 frames are send out with slave deselection. Default Value: 0

(continued)

28.1.4 SCB0_SPI_STATUS

SPI status register.

Address: 0x40240024

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						W	W
Name	None [7:2]						SPI_EC_BUSY	BUS_BUSY

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	CURR_EZ_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	BASE_EZ_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	BASE_EZ_ADDR	SPI base EZ address. Address as provided by a SPI write transfer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable, as clock domain synchronization is not performed in the design. Default Value: Undefined
15 : 8	CURR_EZ_ADDR	SPI current EZ address. Current address pointer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable (during an ongoing transfer when SPI_EC_BUSY is '1'), as clock domain synchronization is not performed in the design. Default Value: Undefined
1	SPI_EC_BUSY	Inidicates whether the externally clocked logic is potentially accessing the EZ memory and/or updating BASE_ADDR or CURR_ADDR (this is only possible in EZ mode). This bit can be used by SW to determine whether BASE_ADDR and CURR_ADDR are reliable. Default Value: Undefined

0	BUS_BUSY	SPI bus is busy. The bus is considered busy ('1') during an ongoing transaction. For Motorola and National submodes, the busy bit is '1', when the slave selection (low active) is activated. For TI submode, the busy bit is '1' from the time the preceding/coinciding slave select (high active) is activated for the first transmitted data frame, till the last MOSI/MISO bit of the last data frame is transmitted. Default Value: Undefined

28.1.5 SCB0_UART_CTRL

UART control register.

Address: 0x40240040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							LOOPBACK

Bits	31	30	29	28	27	26	25	24
SW Access	None						RW	
HW Access	None						R	
Name	None [31:26]						MODE [25:24]	

Bits	Name	Description
25 : 24	MODE	Submode of UART operation (3: Reserved) Default Value: 3 **0x0: UART_STD:** Standard UART submode. **0x1: UART_SMARTCARD:** SmartCard (ISO7816) submode. Support for negative acknowledgement (NACK) on the receiver side and retransmission on the transmitter side. **0x2: UART_IRDA:** Infrared Data Association (IrDA) submode. Return to Zero modulation scheme. In this mode, the oversampling factor should be 16, that is OVS is 15.
16	LOOPBACK	Local loopback control (does NOT affect the information on the pins). When '0', the transmitter TX line "uart_tx_out" is connected to the TX pin and the receiver RX line "uart_rx_in" is connected to the RX pin. When '1', the transmitter TX line "uart_tx_out" is connected to the receiver RX line "uart_rx_in". A similar connections scheme is followed for "uart_rts_out" and "uart_cts_in". This allows a SCB UART transmitter to communicate with its receiver counterpart. Default Value: 0

28.1.6 SCB0_UART_TX_CTRL

UART transmitter control register.

Address: 0x40240044

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	None	RW		
HW Access	None		R	R	None	R		
Name	None [7:6]		PARITY_ENABLED	PARITY	None	STOP_BITS [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							RETRY_ON_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	RETRY_ON_NACK	When '1', a data frame is retransmitted when a negative acknowledgement is received. Only applicable to the SmartCard submode. Default Value: 0
5	PARITY_ENABLED	Parity generation enabled ('1') or not ('0'). Only applicable in standard UART submodes. In SmartCard submode, parity generation is always enabled through hardware. In IrDA submode, parity generation is always disabled through hardware Default Value: 0
4	PARITY	Parity bit. When '0', the transmitter generates an even parity. When '1', the transmitter generates an odd parity. Only applicable in standard UART and SmartCard submodes. Default Value: 0
2 : 0	STOP_BITS	Stop bits. STOP_BITS + 1 is the duration of the stop period in terms of halve bit periods. Valid range is [1, 7]; i.e. a stop period should last at least one bit period. Default Value: 2

28.1.7 SCB0_UART_RX_CTRL

UART receiver control register.

Address: 0x40240048

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	RW	RW	None	RW		
HW Access	None	R	R	R	None	R		
Name	None	POLARITY	PARITY_ENABLED	PARITY	None	STOP_BITS [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW	RW	None	RW	RW	RW
HW Access	None		R	R	None	R	R	R
Name	None [15:14]		SKIP_START	LIN_MODE	None	MP_MODE	DROP_ON_FRAME_ERROR	DROP_ON_PARITY_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				BREAK_WIDTH [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	BREAK_WIDTH	Break width. BREAK_WIDTH + 1 is the minimum width in bit periods of a break. During a break the transmitted/received line value is '0'. This feature is useful for standard UART submode and LIN submode ("break field" detection). Once, the break is detected, the INTR_RX.BREAK_DETECT bit is set to '1'. Note that break detection precedes baud rate detection, which is used to synchronize/refine the receiver clock to the transmitter clock. As a result, break detection operates with an unsynchronized/unrefined receiver clock. Therefore, the receiver's definition of a bit period is imprecise and the setting of this field should take this imprecision into account. The LIN standard also accounts for this imprecision: a LIN start bit followed by 8 data bits allows for up to 9 consecutive '0' bit periods during regular transmission, whereas the LIN break detection should be at least 13 consecutive '0' bit periods. This provides for a margin of 4 bit periods. Therefore, the default value of this field is set to 10, representing a minimal break field with of 10+1 = 11 bit periods; a value in between the 9 consecutive bit periods of a regular transmission and the 13 consecutive bit periods of a break field. This provides for slight imprecisions of the receiver clock wrt. the transmitter clock. There should not be a need to program this field to any value other than its default value. Default Value: 10

(continued)

13	SKIP_START	Only applicable in standard UART submode. When '1', the receiver skips start bit detection for the first received data frame. Instead, it synchronizes on the first received data frame bit, which should be a '1'. This functionality is intended for wake up from DeepSleep when receiving a data frame. The transition from idle ('1') to START ('0') on the RX line is used to wake up the CPU. The transition detection (and the associated wake up functionality) is performed by the GPIO2 IP. The woken up CPU will enable the SCB's UART receiver functionality. Once enabled, it is assumed that the START bit is ongoing (the CPU wakeup and SCB enable time should be less than the START bit period). The SCB will synchronize to a '0' to '1' transition, which indicates the first data frame bit is received (first data frame bit should be '1'). After synchronization to the first data frame bit, the SCB will resume normal UART functionality: subsequent data frames will be synchronized on the receipt of a START bit. Default Value: 0
12	LIN_MODE	Only applicable in standard UART submode. When '1', the receiver performs break detection and baud rate detection on the incoming data. First, break detection counts the amount of bit periods that have a line value of '0'. BREAK_WIDTH specifies the minum required amount of bit periods. Successful break detection sets the INTR_RX.BREAK_DETECT interrupt cause to '1'. Second, baud rate detection counts the amount of peripheral clock periods that are use to receive the synchronization byte (0x55; least significant bit first). The count is available through UART_RX_STATUS.BR_COUNTER. Successful baud rate detection sets the INTR_RX.BAUD_DETECT interrupt cause to '1' (BR_COUNTER is reliable). This functionality is used to synchronize/refine the receiver clock to the transmitter clock. The receiver software can use the BR_COUNTER value to set the right IP clock (from the programmable clock IP) to guarantee successful receipt of the first LIN data frame (Protected Identifier Field) after the synchronization byte. Default Value: 0
10	MP_MODE	Multi-processor mode. When '1', multi-processor mode is enabled. In this mode, RX_CTRL.DATA_WIDTH should indicate a 9-bit data frame. In multi-processor mode, the 9th received bit of a data frame seperates addresses (bit is '1') from data (bit is '0'). A received address is matched with RX_MATCH.DATA and RX_MATCH.MASK. In the case of a match, subsequent received data are sent to the RX FIFO. In the case of NO match, subsequent received data are dropped. Default Value: 0
9	DROP_ON_FRAME_ERROR	Behaviour when an error is detected in a start or stop period. When '0', received data is send to the RX FIFO. When '1', received data is dropped and lost. Default Value: 0
8	DROP_ON_PARITY_ERROR	Behaviour when a parity check fails. When '0', received data is send to the RX FIFO. When '1', received data is dropped and lost. Only applicable in standard UART and SmartCard submodes (negatively acknowledged SmartCard data frames may be dropped with this field). Default Value: 0
6	POLARITY	Inverts incoming RX line signal "uart_rx_in". Inversion is after local loopback. This functionality is intended for IrDA receiver functionality. Default Value: 0
5	PARITY_ENABLED	Parity checking enabled ('1') or not ('0'). Only applicable in standard UART submode. In SmartCard submode, parity checking is always enabled through hardware. In IrDA submode, parity checking is always disabled through hardware. Default Value: 0
4	PARITY	Parity bit. When '0', the receiver expects an even parity. When '1', the receiver expects an odd parity. Only applicable in standard UART and SmartCard submodes. Default Value: 0

(continued)

2 : 0	STOP_BITS	Stop bits. STOP_BITS + 1 is the duration of the stop period in terms of halve bit periods. Valid range is [1, 7]; i.e. a stop period should last at least one bit period. If STOP_BITS is '1', stop bits error detection is NOT performed. If STOP_BITS is in [2, 7], stop bits error detection is performed and the associated interrupt cause INTR_RX.FRAME_ERROR is set to '1' if an error is detected. In other words, the receiver supports data frames with a 1 bit period stop bit sequence, but requires at least 1.5 bit period stop bit sequences to detect errors. This limitation is due to possible transmitter and receiver clock skew that prevents the design from doing reliable stop bit detection for short (1 bit bit period) stop bit sequences. Note that in case of a stop bits error, the successive data frames may get lost as the receiver needs to resynchronize its start bit detection. The amount of lost data frames depends on both the amount of stop bits, the idle ('1') time between data frames and the data frame value. Default Value: 2

28.1.8 SCB0_UART_RX_STATUS

UART receiver status register.

Address: 0x4024004C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	BR_COUNTER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None				R			
HW Access	None				W			
Name	None [15:12]				BR_COUNTER [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11 : 0	BR_COUNTER	Amount of peripheral clock periods that constitute the transmission of a 0x55 data frame (sent least signficant bit first) as determined by the receiver. BR_COUNTER / 8 is the amount of peripheral clock periods that constitute a bit period. This field has valid data when INTR_RX.BAUD_DETECT is set to '1'. Default Value: Undefined

28.1.9 SCB0_UART_FLOW_CTRL

UART flow control register

Address: 0x40240050

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				TRIGGER_LEVEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							RTS_POLARITY

Bits	31	30	29	28	27	26	25	24
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [31:26]						CTS_ENABLED	CTS_POLARITY

Bits	Name	Description
25	CTS_ENABLED	Enable use of CTS input signal "uart_cts_in" by the UART transmitter: '0': Disabled. The UART transmitter ignores "uart_cts_in", and transmits when a data frame is available for transmission in the TX FIFO or the TX shift register. '1': Enabled. The UART transmitter uses "uart_cts_in" to qualify the transmission of data. It transmits when "uart_cts_in" is active and a data frame is available for transmission in the TX FIFO or the TX shift register. If UART_CTRL.LOOPBACK is '1', "uart_cts_in" is connected to "uart_rts_out" in the IP (both signals are subjected to signal polarity changes are indicated by RTS_POLARITY and CTS_POLARITY). Default Value: 0
24	CTS_POLARITY	Polarity of the CTS input signal "uart_cts_in": '0': CTS is low/'0' active; "uart_cts_in" is '0' when active and "uart_cts_in" is '1' when inactive. '1': CTS is high/'1' active; "uart_cts_in" is '1' when active and "uart_cts_in" is '0' when inactive. Default Value: 0

(continued)

16	RTS_POLARITY	Polarity of the RTS output signal "uart_rts_out": '0': RTS is low/'0' active; "uart_rts_out" is '0' when active and "uart_rts_out" is '1' when inactive. '1': RTS is high/'1' active; "uart_rts_out" is '1' when active and "uart_rts_out" is '0' when inactive. During IP reset (Hibernate system power mode), "uart_rts_out" is '1'. This represents an inactive state assuming a low/'0' active polarity. Default Value: 0
3 : 0	TRIGGER_LEVEL	Trigger level. When the receiver FIFO has less entries than the amount of this field, a Ready To Send (RTS) output signal "uart_rts_out" is activated. By setting this field to "0", flow control is effectively SW disabled (may be useful for debug purposes). Default Value: 0

28.1.10 SCB0_I2C_CTRL

I2C control register.

Address: 0x40240060

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	LOW_PHASE_OVS [7:4]				HIGH_PHASE_OVS [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	None	RW	RW
HW Access	R	R	R	R	R	None	R	R
Name	S_NOT_READY_DATA_NACK	S_NOT_READY_ADDR_NACK	S_READY_DATA_ACK	S_READY_ADDR_ACK	S_GENERAL_IGNORE	None	M_NOT_READY_DATA_NACK	M_READY_DATA_ACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							LOOPBACK

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None					
HW Access	R	R	None					
Name	MASTER_MODE	SLAVE_MODE	None [29:24]					

Bits	Name	Description
31	MASTER_MODE	Master mode enabled ('1') or not ('0'). Note that both master and slave modes can be enabled at the same time. This allows the IP to address itself. Default Value: 0
30	SLAVE_MODE	Slave mode enabled ('1') or not ('0'). Default Value: 0
16	LOOPBACK	Local loopback control (does NOT affect the information on the pins). Only applicable in master/slave mode. When '0', the I2C SCL and SDA lines are connected to the I2C SCL and SDA pins. When '1', I2C SCL and SDA lines are routed internally in the peripheral, and as a result unaffected by other I2C devices. This allows a SCB I2C peripheral to address itself. Default Value: 0
15	S_NOT_READY_DATA_NACK	For internally clocked logic only. Only used when: - non EZ mode. Functionality is as follows: - 1: a received data element byte the slave is immediately NACK'd when the receiver FIFO is full. - 0: clock stretching is performed (till the receiver FIFO is no longer full). Default Value: 1

(continued)

14	S_NOT_READY_ADDR_NACK	For internally clocked logic (EC_AM is '0' and EC_OP is '0') on an address match or general call address (and S_GENERAL_IGNORE is '0'). Only used when: - EC_AM is '0', EC_OP is '0' and non EZ mode. Functionality is as follows: - 1: a received (matching) slave address is immediately NACK'd when the receiver FIFO is full. - 0: clock stretching is performed (till the receiver FIFO is no longer full). For externally clocked logic (EC_AM is '1') on an address match or general call address (and S_GENERAL_IGNORE is '0'). Only used when (NOT used when EC_AM is '1' and EC_OP is '1' and address match and EZ mode): - EC_AM is '1' and EC_OP is '0'. - EC_AM is '1' and general call address match. - EC_AM is '1' and non EZ mode. Functionality is as follows: - 1: a received (matching or general) slave address is always immediately NACK'd. There are two possibilities: 1). the internally clocked logic is enabled (we are in Active system power mode) and it handles the rest of the current transfer. In this case the I2C master will not observe the NACK. 2). the internally clocked logic is not enabled (we are in DeepSleep system power mode). In this case the I2C master will observe the NACK and may retry the transfer in the future (which gives the internally clocked logic the time to wake up from DeepSleep system power mode). - 0: clock stretching is performed (till the internally clocked logic takes over). The internally clocked logic will handle the ongoing transfer as soon as it is enabled. Default Value: 1
13	S_READY_DATA_ACK	When '1', a received data element by the slave is immediately ACK'd when the receiver FIFO is not full. In EZ mode, this field should be set to '1'. Default Value: 1
12	S_READY_ADDR_ACK	When '1', a received (matching) slave address is immediately ACK'd when the receiver FIFO is not full. In EZ mode, this field should be set to '1'. Default Value: 1
11	S_GENERAL_IGNORE	When '1', a received general call slave address is immediately NACK'd (no ACK or clock stretching) and treated as a non matching slave address. This is useful for slaves that do not need any data supplied within the general call structure. Default Value: 1
9	M_NOT_READY_DATA_NACK	When '1', a received data element byte the master is immediately NACK'd when the receiver FIFO is full. When '0', clock stretching is used instead (till the receiver FIFO is no longer full). Default Value: 1
8	M_READY_DATA_ACK	When '1', a received data element by the master is immediately ACK'd when the receiver FIFO is not full. Default Value: 1
7 : 4	LOW_PHASE_OVS	Serial I2C interface low phase oversampling factor. LOW_PHASE_OVS + 1 peripheral clock periods constitute the low phase of a bit period. The valid range is [7, 15] with input signal median filtering and [6, 15] without input signal median filtering. The field is only used in master mode. In slave mode, the field is NOT used. However, there is a frequency requirement for the IP clock wrt. the regular (no stretching) interface (IF) low time to guarantee functional correct behavior. With input signal median filtering, the IF low time should be >= 8 IP clock cycles and <= 16 IP clock cycles. Without input signal median filtering, the IF low time should be >= 7 IP clock cycles and <= 16 IP clock cycles. Default Value: 8

(continued)

3 : 0	HIGH_PHASE_OVS	Serial I2C interface high phase oversampling factor. HIGH_PHASE_OVS + 1 peripheral clock periods constitute the high phase of a bit period. The valid range is [5, 15] with input signal median filtering and [4, 15] without input signal median filtering. The field is only used in master mode. In slave mode, the field is NOT used. However, there is a frequency requirement for the IP clock wrt. the regular interface (IF) high time to guarantee functional correct behavior. With input signal median filtering, the IF high time should be >= 6 IP clock cycles and <= 16 IP clock cycles. Without input signal median filtering, the IF high time should be >= 5 IP clock cycles and <= 16 IP clock cycles. Default Value: 8

28.1.11 SCB0_I2C_STATUS

I2C status register.

Address: 0x40240064

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R	R	None		R	R
HW Access	None		W	W	None		W	W
Name	None [7:6]		M_READ	S_READ	None [3:2]		I2C_EC_BUSY	BUS_BUSY

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	CURR_EZ_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	BASE_EZ_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	BASE_EZ_ADDR	I2C slave base EZ address. Address as provided by an I2C write transfer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable, as clock domain synchronization is not performed in the design. Default Value: Undefined
15 : 8	CURR_EZ_ADDR	I2C slave current EZ address. Current address pointer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable (during an ongoing transfer when I2C_EC_BUSY is '1'), as clock domain synchronization is not performed in the design. Default Value: Undefined
5	M_READ	I2C master read transfer ('1') or I2C master write transfer ('0'). When the I2C master is inactive/idle or transmitting START, REPEATED START, STOP or an address, this field is '0''. Default Value: 0
4	S_READ	I2C slave read transfer ('1') or I2C slave write transfer ('0'). When the I2C slave is inactive/idle or receiving START, REPEATED START, STOP or an address, this field is '0''. Default Value: 0

(continued)

1	I2C_EC_BUSY	Inidicates whether the externally clocked logic is potentially accessing the EZ memory and/or updating BASE_ADDR or CURR_ADDR (this is only possible in EZ mode). This bit can be used by SW to determine whether BASE_ADDR and CURR_ADDR are reliable. Default Value: Undefined
0	BUS_BUSY	I2C bus is busy. The bus is considered busy ('1'), from the time a START is detected or from the time the SCL line is '0'. The bus is considered idle ('0'), from the time a STOP is detected. If the IP is disabled, BUS_BUSY is '0'. After enabling the IP, it takes time for the BUS_BUSY to detect a busy bus. This time is the maximum high time of the SCL line. For a 100 kHz interface frequency, this maximum high time may last roughly 5 us (half a bit period). For single master systems, BUS_BUSY does not have to be used to detect an idle bus before a master starts a transfer using I2C_M_CMD.M_START (no bus collisions). For multi-master systems, BUS_BUSY can be used to detect an idle bus before a master starts a transfer using I2C_M_CMD.M_START_ON_IDLE (to prevent bus collisions). Default Value: 0

28.1.12 SCB0_I2C_M_CMD

I2C master command register.

Address: 0x40240068

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			RW1C	RW1C	RW1C	RW1C	RW1C
Name	None [7:5]			M_STOP	M_NACK	M_ACK	M_START_ON_IDLE	M_START

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4	M_STOP	When '1', attempt to transmit a STOP. When this action is performed, the hardware sets this field to '0'. This command has a higher priority than I2C_M_CMD.M_START: in situations where both a STOP and a REPEATED START could be transmitted, M_STOP takes precedence over M_START. Default Value: 0
3	M_NACK	When '1', attempt to transmit a negative acknowledgement (NACK). When this action is performed, the hardware sets this field to '0'. Default Value: 0
2	M_ACK	When '1', attempt to transmit an acknowledgement (ACK). When this action is performed, the hardware sets this field to '0'. Default Value: 0
1	M_START_ON_IDLE	When '1', transmit a START as soon as the bus is idle (I2C_STATUS.BUS_BUSY is '0', note that BUSY has a default value of '0'). For bus idle detection the hardware relies on STOP detection. As a result, bus idle detection is only functional after at least one I2C bus transfer has been detected on the bus (default/reset value of BUSY is '0') . A START is only transmitted when the master state machine is in the default state. When this action is performed, the hardware sets this field to '0'. Default Value: 0

(continued)

0	M_START	When '1', transmit a START or REPEATED START. Whether a START or REPEATED START is transmitted depends on the state of the master state machine. A START is only transmitted when the master state machine is in the default state. A REPEATED START is transmitted when the master state machine is not in the default state, but is working on an ongoing transaction. The REPEATED START can only be transmitted after a NACK or ACK has been received for a transmitted data element or after a NACK has been transmitted for a received data element. When this action is performed, the hardware sets this field to '0'. Default Value: 0

28.1.13 SCB0_I2C_S_CMD

I2C slave command register.

Address: 0x4024006C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						RW1C	RW1C
Name	None [7:2]						S_NACK	S_ACK

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	S_NACK	When '1', attempt to transmit a negative acknowledgement (NACK). When this action is performed, the hardware sets this field to '0'. In EZ mode, this field should be set to '0' (it is only to be used in non EZ mode). This command has a higher priority than I2C_S_CMD.S_ACK, I2C_CTRL.S_READY_ADDR_ACK or I2C_CTRL.S_READY_DATA_ACK. Default Value: 0
0	S_ACK	When '1', attempt to transmit an acknowledgement (ACK). When this action is performed, the hardware sets this field to '0'. In EZ mode, this field should be set to '0' (it is only to be used in non EZ mode). Default Value: 0

28.1.14 SCB0_I2C_CFG

I2C configuration register.

Address: 0x40240070

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	None		RW	
HW Access	None			R	None		R	
Name	None [7:5]			SDA_IN_FILT_SEL	None [3:2]		SDA_IN_FILT_TRIM [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	None		RW	
HW Access	None			R	None		R	
Name	None [15:13]			SCL_IN_FILT_SEL	None [11:10]		SCL_IN_FILT_TRIM [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW		RW		RW	
HW Access	None		R		R		R	
Name	None [23:22]		SDA_OUT_FILT2_TRIM [21:20]		SDA_OUT_FILT1_TRIM [19:18]		SDA_OUT_FILT0_TRIM [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None		RW		None			
HW Access	None		R		None			
Name	None [31:30]		SDA_OUT_FILT_SEL [29:28]		None [27:24]			

Bits	Name	Description
29 : 28	SDA_OUT_FILT_SEL	Selection of cumulative "i2c_sda_out" filter delay: "0": 0 ns. "1": 50 ns (filter 0 enabled). "2": 100 ns (filters 0 and 1 enabled). "3": 150 ns (filters 0, 1 and 2 enabled). Default Value: 0
21 : 20	SDA_OUT_FILT2_TRIM	Trim bits for "i2c_sda_out" 50 ns filter 2. See s8i2cs BROS (001-59539) for more details on the trim bit values. Default Value: 2
19 : 18	SDA_OUT_FILT1_TRIM	Trim bits for "i2c_sda_out" 50 ns filter 1. See s8i2cs BROS (001-59539) for more details on the trim bit values. Default Value: 2
17 : 16	SDA_OUT_FILT0_TRIM	Trim bits for "i2c_sda_out" 50 ns filter 0. See s8i2cs BROS (001-59539) for more details on the trim bit values. Default Value: 2

(continued)

12	SCL_IN_FILT_SEL	Selection of "i2c_scl_in" filter delay: '0': 0 ns. '1: 50 ns (filter enabled). Default Value: 1
9 : 8	SCL_IN_FILT_TRIM	Trim bits for "i2c_scl_in" 50 ns filter. See s8i2cs BROS (001-59539) for more details on the trim bit values. Default Value: 0
4	SDA_IN_FILT_SEL	Selection of "i2c_sda_in" filter delay: '0': 0 ns. '1: 50 ns (filter enabled). Default Value: 1
1 : 0	SDA_IN_FILT_TRIM	Trim bits for "i2c_sda_in" 50 ns filter. See s8i2cs BROS (001-59539) for more details on the trim bit values. Default Value: 3

28.1.15 SCB0_TX_CTRL

Transmitter control register.

Address: 0x40240200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				DATA_WIDTH [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							MSB_FIRST

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	MSB_FIRST	Least significant bit first ('0') or most significant bit first ('1'). For I2C, this field should be '1'. Default Value: 1
3 : 0	DATA_WIDTH	Dataframe width. DATA_WIDTH + 1 is the amount of bits in a transmitted data frame. This number does not include start, parity and stop bits. For UART mode, the valid range is [3, 8]. For SPI, the valid range is [3, 15]. For I2C the only valid value is 7. Default Value: 7

28.1.16 SCB0_TX_FIFO_CTRL

Transmitter FIFO control register.

Address: 0x40240204

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				TRIGGER_LEVEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [23:18]						FREEZE	CLEAR

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
17	FREEZE	When '1', hardware reads from the transmitter FIFO do not remove FIFO entries. Freeze will not advance the TX FIFO read pointer. Default Value: 0
16	CLEAR	When '1', the transmitter FIFO and transmitter shift register are cleared/invalidated. Invalidation will last for as long as this field is '1'. If a quick clear/invalidation is required, the field should be set to '1' and be followed by a set to '0'. If a clear/invalidation is required for an extended time period, the field should be set to '1' during the complete time period. Default Value: 0
3 : 0	TRIGGER_LEVEL	Trigger level. When the transmitter FIFO has less entries than the number of this field, a transmitter trigger event is generated. Default Value: 0

28.1.17 SCB0_TX_FIFO_STATUS

Transmitter FIFO status register.

Address: 0x40240208

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R			
HW Access	None				W			
Name	None [7:5]				USED [4:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	R	None						
HW Access	W	None						
Name	SR_VALID	None [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	None				R			
HW Access	None				W			
Name	None [23:20]				RD_PTR [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None				R			
HW Access	None				W			
Name	None [31:28]				WR_PTR [27:24]			

Bits	Name	Description
27 : 24	WR_PTR	FIFO write pointer: FIFO location at which a new data frame is written. Default Value: 0
19 : 16	RD_PTR	FIFO read pointer: FIFO location from which a data frame is read by the hardware. Default Value: 0
15	SR_VALID	Indicates whether the TX shift registers holds a valid data frame ('1') or not ('0'). The shift register can be considered the top of the TX FIFO (the data frame is not included in the USED field of the TX FIFO). The shift register is a working register and holds the data frame that is currently transmitted (when the protocol state machine is transmitting a data frame) or the data frame that is tranmitted next (when the protocol state machine is not transmitting a data frame). Default Value: 0
4 : 0	USED	Amount of enties in the transmitter FIFO. The value of this field ranges from 0 to FF_DATA_NR. Default Value: 0

28.1.18 SCB0_TX_FIFO_WR

Transmitter FIFO write register.

Address: 0x40240240

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATA	Data frame written into the transmitter FIFO. Behavior is similar to that of a PUSH operation. Note that when CTRL.BYTE_MODE is '1', only DATA[7:0] are used. A write to a full TX FIFO sets INTR_TX.OVERFLOW to '1'. Default Value: 0

28.1.19 SCB0_RX_CTRL

Receiver control register.

Address: 0x40240300

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				DATA_WIDTH [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [15:10]						MEDIAN	MSB_FIRST

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	MEDIAN	Median filter. When '1', a digital 3 taps median filter is performed on input interface lines. This filter should reduce the susceptability to errors. However, its requires higher oversampling values. For UART IrDA submode, this field should always be '1'. Default Value: 0
8	MSB_FIRST	Least significant bit first ('0') or most significant bit first ('1'). For I2C, this field should be '1'. Default Value: 1
3 : 0	DATA_WIDTH	Dataframe width. DATA_WIDTH + 1 is the expected amount of bits in received data frame. This number does not include start, parity and stop bits. For UART mode, the valid range is [3, 8]. For SPI, the valid range is [3, 15]. For I2C the only valid value is 7. In EZ mode (for both SPI and I2C), the only valid value is 7. Default Value: 7

28.1.20 SCB0_RX_FIFO_CTRL

Receiver FIFO control register.

Address: 0x40240304

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				TRIGGER_LEVEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [23:18]						FREEZE	CLEAR

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
17	FREEZE	When '1', hardware writes to the receiver FIFO have no effect. Freeze will not advance the RX FIFO write pointer. Default Value: 0
16	CLEAR	When '1', the receiver FIFO and receiver shift register are cleared/invalidated. Invalidation will last for as long as this field is '1'. If a quick clear/invalidation is required, the field should be set to '1' and be followed by a set to '0'. If a clear/invalidation is required for an extended time period, the field should be set to '1' during the complete time period. Default Value: 0
3 : 0	TRIGGER_LEVEL	Trigger level. When the receiver FIFO has more entries than the number of this field, a receiver trigger event is generated. Default Value: 0

28.1.21 SCB0_RX_FIFO_STATUS

Receiver FIFO status register.

Address: 0x40240308

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R			
HW Access	None				W			
Name	None [7:5]				USED [4:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	R	None						
HW Access	W	None						
Name	SR_VALID	None [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	None				R			
HW Access	None				W			
Name	None [23:20]				RD_PTR [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None				R			
HW Access	None				W			
Name	None [31:28]				WR_PTR [27:24]			

Bits	Name	Description
27 : 24	WR_PTR	FIFO write pointer: FIFO location at which a new data frame is written by the hardware. Default Value: 0
19 : 16	RD_PTR	FIFO read pointer: FIFO location from which a data frame is read. Default Value: 0
15	SR_VALID	Indicates whether the RX shift registers holds a (partial) valid data frame ('1') or not ('0'). The shift register can be considered the bottom of the RX FIFO (the data frame is not included in the USED field of the RX FIFO). The shift register is a working register and holds the data frame that is currently being received (when the protocol state machine is receiving a data frame). Default Value: 0
4 : 0	USED	Amount of enties in the receiver FIFO. The value of this field ranges from 0 to FF_DATA_NR. Default Value: 0

28.1.22 SCB0_RX_MATCH

Slave address and mask register.

Address: 0x40240310

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	MASK [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	MASK	Slave device address mask. This field is a mask that specifies which of the ADDR field bits in the ADDR field take part in the matching of the slave address: MATCH = ((ADDR & MASK) == ("slave address" & MASK)). Default Value: 0
7 : 0	ADDR	Slave device address. In UART multi-processor mode, all 8 bits are used. In I2C slave mode, only bits 7 down to 1 are used. This reflects the organization of the first transmitted byte in a I2C transfer: the first 7 bits represent the address of the addressed slave, and the last 1 bit is a read/write indicator ('0': write, '1': read). Default Value: 0

28.1.23 SCB0_RX_FIFO_RD

Receiver FIFO read register.

Address: 0x40240340

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATA	Data read from the receiver FIFO. Reading a data frame will remove the data frame from the FIFO; i.e. behavior is similar to that of a POP operation. Note that when CTRL.BYTE_MODE is '1', only DATA[7:0] are used. This register has a side effect when read by software: a data frame is removed from the FIFO. This may be undesirable during debug; i.e. a read during debug should NOT have a side effect. To this end, the IP uses the AHB-Lite "hmaster[0]" input signal. When this signal is '1' in the address cycle of a bus transfer, a read transfer will not have a side effect. As a result, a read from this register will not remove a data frame from the FIFO. As a result, a read from this register behaves as a read from the SCB_RX_FIFO_RD_SILENT register. A read from an empty RX FIFO sets INTR_RX.UNDERFLOW to '1'. Default Value: Undefined

28.1.24 SCB0_RX_FIFO_RD_SILENT

Receiver FIFO read register.

Address: 0x40240344

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATA	Data read from the receiver FIFO. Reading a data frame will NOT remove the data frame from the FIFO; i.e. behavior is similar to that of a PEEK operation. Note that when CTRL.BYTE_MODE is '1', only DATA[7:0] are used. A read from an empty RX FIFO sets INTR_RX.UNDERFLOW to '1'. Default Value: Undefined

28.1.25 SCB0_EZ_DATA0

Memory buffer registers.

Address: 0x40240400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

28.1.26 SCB0_EZ_DATA1

Memory buffer registers.

Address: 0x40240404

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

28.1.27 SCB0_EZ_DATA2

Memory buffer registers.

Address: 0x40240408

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

28.1.28 SCB0_EZ_DATA3

Memory buffer registers.

Address: 0x4024040C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

28.1.29 SCB0_EZ_DATA4

Memory buffer registers.

Address: 0x40240410

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

28.1.30 SCB0_EZ_DATA5

Memory buffer registers.

Address: 0x40240414

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

28.1.31 SCB0_EZ_DATA6

Memory buffer registers.

Address: 0x40240418

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

28.1.32 SCB0_EZ_DATA7

Memory buffer registers.

Address: 0x4024041C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

28.1.33 SCB0_EZ_DATA8

Memory buffer registers.

Address: 0x40240420

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

28.1.34 SCB0_EZ_DATA9

Memory buffer registers.

Address: 0x40240424

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

28.1.35 SCB0_EZ_DATA10

Memory buffer registers.

Address: 0x40240428

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

28.1.36 SCB0_EZ_DATA11

Memory buffer registers.

Address: 0x4024042C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

28.1.37 SCB0_EZ_DATA12

Memory buffer registers.

Address: 0x40240430

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

28.1.38 SCB0_EZ_DATA13

Memory buffer registers.

Address: 0x40240434

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

28.1.39 SCB0_EZ_DATA14

Memory buffer registers.

Address: 0x40240438

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

28.1.40 SCB0_EZ_DATA15

Memory buffer registers.

Address: 0x4024043C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

28.1.41 SCB0_EZ_DATA16

Memory buffer registers.

Address: 0x40240440

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

28.1.42 SCB0_EZ_DATA17

Memory buffer registers.

Address: 0x40240444

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

28.1.43 SCB0_EZ_DATA18

Memory buffer registers.

Address: 0x40240448

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

28.1.44 SCB0_EZ_DATA19

Memory buffer registers.

Address: 0x4024044C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

28.1.45 SCB0_EZ_DATA20

Memory buffer registers.

Address: 0x40240450

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

28.1.46 SCB0_EZ_DATA21

Memory buffer registers.

Address: 0x40240454

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

28.1.47 SCB0_EZ_DATA22

Memory buffer registers.

Address: 0x40240458

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

28.1.48 SCB0_EZ_DATA23

Memory buffer registers.

Address: 0x4024045C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

28.1.49 SCB0_EZ_DATA24

Memory buffer registers.

Address: 0x40240460

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

28.1.50 SCB0_EZ_DATA25

Memory buffer registers.

Address: 0x40240464

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

28.1.51 SCB0_EZ_DATA26

Memory buffer registers.

Address: 0x40240468

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

28.1.52 SCB0_EZ_DATA27

Memory buffer registers.

Address: 0x4024046C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

28.1.53 SCB0_EZ_DATA28

Memory buffer registers.

Address: 0x40240470

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

28.1.54 SCB0_EZ_DATA29

Memory buffer registers.

Address: 0x40240474

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

28.1.55 SCB0_EZ_DATA30

Memory buffer registers.

Address: 0x40240478

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

28.1.56 SCB0_EZ_DATA31

Memory buffer registers.

Address: 0x4024047C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

28.1.57 SCB0_INTR_CAUSE

Active clocked interrupt signal register

Address: 0x40240E00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R	R	R	R	R	R
HW Access	None		W	W	W	W	W	W
Name	None [7:6]		SPI_EC	I2C_EC	RX	TX	S	M

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	SPI_EC	Externally clocked SPI interrupt active ("interrupt_spi_ec"): INTR_SPI_EC_MASKED != 0. Default Value: 0
4	I2C_EC	Externally clock I2C interrupt active ("interrupt_i2c_ec"): INTR_I2C_EC_MASKED != 0. Default Value: 0
3	RX	Receiver interrupt active ("interrupt_rx"): INTR_RX_MASKED != 0. Default Value: 0
2	TX	Transmitter interrupt active ("interrupt_tx"): INTR_TX_MASKED != 0. Default Value: 0
1	S	Slave interrupt active ("interrupt_slave"): INTR_S_MASKED != 0. Default Value: 0
0	M	Master interrupt active ("interrupt_master"): INTR_M_MASKED != 0. Default Value: 0

28.1.58 SCB0_INTR_I2C_EC

Externally clocked I2C interrupt request register

Address: 0x40240E80

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1C	RW1C	RW1C	RW1C
HW Access	None				A	A	A	A
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	STOP detection after a read transfer occurred. Activated on the end of a read transfer (I2C STOP). This event is an indication that a buffer memory location has been read from. Only available for a slave request with an address match, in EZ and CMD_RESP modes, when EC_OP is '1'. Default Value: 0
2	EZ_WRITE_STOP	STOP detection after a write transfer occurred. Activated on the end of a write transfer (I2C STOP). This event is an indication that a buffer memory location has been written to. For EZ mode: a transfer that only writes the base address does NOT activate this event. Only available for a slave request with an address match, in EZ and CMD_RESP modes, when EC_OP is '1'. Default Value: 0
1	EZ_STOP	STOP detection. Activated on the end of a every transfer (I2C STOP). Only available for a slave request with an address match, in EZ and CMD_RESP modes, when EC_OP is '1'. Default Value: 0

(continued)

0	WAKE_UP	Wake up request. Active on incoming slave request (with address match). Only used when EC_AM is '1'. Default Value: 0

28.1.59 SCB0_INTR_I2C_EC_MASK

Externally clocked I2C interrupt mask register

Address: 0x40240E88

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	EZ_WRITE_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	EZ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	WAKE_UP	Mask bit for corresponding bit in interrupt request register. Default Value: 0

28.1.60 SCB0_INTR_I2C_EC_MASKED

Externally clocked I2C interrupt masked register

Address: 0x40240E8C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R	R	R	R
HW Access	None				W	W	W	W
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
2	EZ_WRITE_STOP	Logical and of corresponding request and mask bits. Default Value: 0
1	EZ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
0	WAKE_UP	Logical and of corresponding request and mask bits. Default Value: 0

28.1.61 SCB0_INTR_SPI_EC

Externally clocked SPI interrupt request register

Address: 0x40240EC0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1C	RW1C	RW1C	RW1C
HW Access	None				A	A	A	A
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	STOP detection after a read transfer occurred. Activated on the end of a read transfer (SPI de-selection). This event is an indication that a buffer memory location has been read from. Only used in EZ and CMD_RESP modes and when EC_OP is '1'. Default Value: 0
2	EZ_WRITE_STOP	STOP detection after a write transfer occurred. Activated on the end of a write transfer (SPI de-selection). This event is an indication that a buffer memory location has been written to. For EZ mode: a transfer that only writes the base address does NOT activate this event. Only used in EZ and CMD_RESP modes and when EC_OP is '1'. Default Value: 0
1	EZ_STOP	STOP detection. Activated on the end of a every transfer (SPI deselection). Only available in EZ and CMD_RESP mode and when EC_OP is '1'. Default Value: 0

(continued)

0	WAKE_UP	Wake up request. Active on incoming slave request when externally clocked selection is '1'. Only used when EC_AM is '1'. Default Value: 0

28.1.62 SCB0_INTR_SPI_EC_MASK

Externally clocked SPI interrupt mask register

Address: 0x40240EC8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	EZ_WRITE_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	EZ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	WAKE_UP	Mask bit for corresponding bit in interrupt request register. Default Value: 0

28.1.63 SCB0_INTR_SPI_EC_MASKED

Externally clocked SPI interrupt masked register

Address: 0x40240ECC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R	R	R	R
HW Access	None				W	W	W	W
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
2	EZ_WRITE_STOP	Logical and of corresponding request and mask bits. Default Value: 0
1	EZ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
0	WAKE_UP	Logical and of corresponding request and mask bits. Default Value: 0

28.1.64 SCB0_INTR_M

Master interrupt request register.

Address: 0x40240F00

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW1C	None	RW1C	RW1C	RW1C
HW Access	None			RW1S	None	RW1S	RW1S	RW1S
Name	None [7:5]			I2C_STOP	None	I2C_ACK	I2C_NACK	I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW1C	RW1C
HW Access	None						RW1S	RW1S
Name	None [15:10]						SPI_DONE	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	SPI_DONE	SPI master transfer done event: all data frames in the transmit FIFO are sent and the transmit FIFO is empty. Default Value: 0
8	I2C_BUS_ERROR	I2C master bus error (unexpected detection of START or STOP condition). Default Value: 0
4	I2C_STOP	I2C master STOP. Set to '1', when the master has transmitted a STOP. Default Value: 0
2	I2C_ACK	I2C master acknowledgement. Set to '1', when the master receives a ACK (typically after the master transmitted the slave address or TX data). Default Value: 0
1	I2C_NACK	I2C master negative acknowledgement. Set to '1', when the master receives a NACK (typically after the master transmitted the slave address or TX data). Default Value: 0

(continued)

0	I2C_ARB_LOST	I2C master lost arbitration: the value driven by the master on the SDA line is not the same as the value observed on the SDA line. Default Value: 0

28.1.65 SCB0_INTR_M_SET

Master interrupt set request register

Address: 0x40240F04

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW1S	None	RW1S	RW1S	RW1S
HW Access	None			A	None	A	A	A
Name	None [7:5]			I2C_STOP	None	I2C_ACK	I2C_NACK	I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW1S	RW1S
HW Access	None						A	A
Name	None [15:10]						SPI_DONE	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	SPI_DONE	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
8	I2C_BUS_ERROR	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
4	I2C_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
2	I2C_ACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
1	I2C_NACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	I2C_ARB_LOST	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

28.1.66 SCB0_INTR_M_MASK

Master interrupt mask register.

Address: 0x40240F08

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	None	RW	RW	RW
HW Access	None			R	None	R	R	R
Name	None [7:5]			I2C_STOP	None	I2C_ACK	I2C_NACK	I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [15:10]						SPI_DONE	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	SPI_DONE	Mask bit for corresponding bit in interrupt request register. Default Value: 0
8	I2C_BUS_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
4	I2C_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	I2C_ACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	I2C_NACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	I2C_ARB_LOST	Mask bit for corresponding bit in interrupt request register. Default Value: 0

28.1.67 SCB0_INTR_M_MASKED

Master interrupt masked request register

Address: 0x40240F0C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			R	None	R	R	R
HW Access	None			W	None	W	W	W
Name	None [7:5]			I2C_STOP	None	I2C_ACK	I2C_NACK	I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None						R	R
HW Access	None						W	W
Name	None [15:10]						SPI_DONE	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	SPI_DONE	Logical and of corresponding request and mask bits. Default Value: 0
8	I2C_BUS_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
4	I2C_STOP	Logical and of corresponding request and mask bits. Default Value: 0
2	I2C_ACK	Logical and of corresponding request and mask bits. Default Value: 0
1	I2C_NACK	Logical and of corresponding request and mask bits. Default Value: 0
0	I2C_ARB_LOST	Logical and of corresponding request and mask bits. Default Value: 0

28.1.68 SCB0_INTR_S

Slave interrupt request register.

Address: 0x40240F40

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
Name	I2C_GENERAL	I2C_ADDR_MATCH	I2C_START	I2C_STOP	I2C_WRITE_STOP	I2C_ACK	I2C_NACK	I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW1C	RW1C	RW1C	RW1C
HW Access	None				RW1S	RW1S	RW1S	RW1S
Name	None [15:12]				SPI_BUS_ERROR	SPI_EZ_STOP	SPI_EZ_WRITE_STOP	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	SPI_BUS_ERROR	SPI slave deselected at an unexpected time in the SPI transfer. The Firmware may decide to clear the TX and RX FIFOs in case of this error. Default Value: 0
10	SPI_EZ_STOP	SPI slave deselected after any EZ SPI transfer occurred. Default Value: 0
9	SPI_EZ_WRITE_STOP	SPI slave deselected after a write EZ SPI transfer occurred. Default Value: 0
8	I2C_BUS_ERROR	I2C slave bus error (unexpected detection of START or STOP condition). This should not occur, it represents erroneous I2C bus behavior. In case of a bus error, the I2C slave state machine abort the ongoing transfer. The Firmware may decide to clear the TX and RX FIFOs in case of this error. Default Value: 0

(continued)

7	I2C_GENERAL	I2C slave general call address received. If CTRL.ADDR_ACCEPT, the received address 0x00 (including the R/W bit) is available in the RX FIFO. In the case of externally clocked address matching (CTRL.EC_AM_MODE is '1') and internally clocked operation (CTRL.EC_OP_MODE is '0'), this field is set when the event is detected. Default Value: 0
6	I2C_ADDR_MATCH	I2C slave matching address received. If CTRL.ADDR_ACCEPT, the received address (including the R/W bit) is available in the RX FIFO. In the case of externally clocked address matching (CTRL.EC_AM_MODE is '1') and internally clocked operation (CTRL.EC_OP_MODE is '0'), this field is set when the event is detected. Default Value: 0
5	I2C_START	I2C slave START received. Set to '1', when START or REPEATED START event is detected. In the case of externally clocked address matching (CTRL.EC_AM_MODE is '1') AND clock stretching is performed (till the internally clocked logic takes over) (I2C_CTRL.S_NOT_READY_ADDR_NACK is '0'), this field is NOT set. The Firmware should use INTR_S_EC.WAKE_UP, INTR_S.I2C_ADDR_MATCH and INTR_S.I2C_GENERAL. Default Value: 0
4	I2C_STOP	I2C STOP event for I2C (read or write) transfer intended for this slave (address matching is performed). Set to '1', when STOP or REPEATED START event is detected. The REPEATED START event is included in this interrupt cause such that the I2C transfers separated by a REPEATED START can be distinguished and potentially treated separately by the Firmware. Note that the second I2C transfer (after a REPEATED START) may be to a different slave address. The event is detected on any I2C transfer intended for this slave. Note that a I2C address intended for the slave (address is matching) will result in a I2C_STOP event independent of whether the I2C address is ACK'd or NACK'd. Default Value: 0
3	I2C_WRITE_STOP	I2C STOP event for I2C write transfer intended for this slave (address matching is performed). Set to '1', when STOP or REPEATED START event is detected. The REPEATED START event is included in this interrupt cause such that the I2C transfers separated by a REPEATED START can be distinguished and potentially treated separately by the Firmware. Note that the second I2C transfer (after a REPEATED START) may be to a different slave address. In non EZ mode, the event is detected on any I2C write transfer intended for this slave. Note that a I2C write address intended for the slave (address is matching and a it is a write transfer) will result in a I2C_WRITE_STOP event independent of whether the I2C address is ACK'd or NACK'd. In EZ mode, the event is detected only on I2C write transfers that have EZ data written to the memory structure (an I2C write transfer that only communicates an I2C address and EZ address, will not result in this event being detected). Default Value: 0
2	I2C_ACK	I2C slave acknowledgement received. Set to '1', when the slave receives a ACK (typically after the slave transmitted TX data). Default Value: 0
1	I2C_NACK	I2C slave negative acknowledgement received. Set to '1', when the slave receives a NACK (typically after the slave transmitted TX data). Default Value: 0
0	I2C_ARB_LOST	I2C slave lost arbitration: the value driven on the SDA line is not the same as the value observed on the SDA line (while the SCL line is '1'). This should not occur, it represents erroneous I2C bus behavior. In case of lost arbitration, the I2C slave state machine abort the ongoing transfer. The Firmware may decide to clear the TX and RX FIFOs in case of this error. Default Value: 0

28.1.69 SCB0_INTR_S_SET

Slave interrupt set request register.

Address: 0x40240F44

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	A	A	A	A	A	A	A	A
Name	I2C_GENERAL	I2C_ADDR_MATCH	I2C_START	I2C_STOP	I2C_WRITE_STOP	I2C_ACK	I2C_NACK	I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW1S	RW1S	RW1S	RW1S
HW Access	None				A	A	A	A
Name	None [15:12]				SPI_BUS_ERROR	SPI_EZ_STOP	SPI_EZ_WRITE_STOP	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	SPI_BUS_ERROR	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
10	SPI_EZ_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
9	SPI_EZ_WRITE_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
8	I2C_BUS_ERROR	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
7	I2C_GENERAL	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
6	I2C_ADDR_MATCH	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
5	I2C_START	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

(continued)

4	I2C_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
3	I2C_WRITE_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
2	I2C_ACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
1	I2C_NACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	I2C_ARB_LOST	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

28.1.70 SCB0_INTR_S_MASK

Slave interrupt mask register.

Address: 0x40240F48

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	I2C_GENERAL	I2C_ADDR_MATCH	I2C_START	I2C_STOP	I2C_WRITE_STOP	I2C_ACK	I2C_NACK	I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [15:12]				SPI_BUS_ERROR	SPI_EZ_STOP	SPI_EZ_WRITE_STOP	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	SPI_BUS_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
10	SPI_EZ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
9	SPI_EZ_WRITE_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
8	I2C_BUS_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
7	I2C_GENERAL	Mask bit for corresponding bit in interrupt request register. Default Value: 0
6	I2C_ADDR_MATCH	Mask bit for corresponding bit in interrupt request register. Default Value: 0
5	I2C_START	Mask bit for corresponding bit in interrupt request register. Default Value: 0

(continued)

4	I2C_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
3	I2C_WRITE_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	I2C_ACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	I2C_NACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	I2C_ARB_LOST	Mask bit for corresponding bit in interrupt request register. Default Value: 0

28.1.71 SCB0_INTR_S_MASKED

Slave interrupt masked request register

Address: 0x40240F4C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	I2C_GENERAL	I2C_ADDR_MATCH	I2C_START	I2C_STOP	I2C_WRITE_STOP	I2C_ACK	I2C_NACK	I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None				R	R	R	R
HW Access	None				W	W	W	W
Name	None [15:12]				SPI_BUS_ERROR	SPI_EZ_STOP	SPI_EZ_WRITE_STOP	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	SPI_BUS_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
10	SPI_EZ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
9	SPI_EZ_WRITE_STOP	Logical and of corresponding request and mask bits. Default Value: 0
8	I2C_BUS_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
7	I2C_GENERAL	Logical and of corresponding request and mask bits. Default Value: 0
6	I2C_ADDR_MATCH	Logical and of corresponding request and mask bits. Default Value: 0
5	I2C_START	Logical and of corresponding request and mask bits. Default Value: 0

(continued)

4	I2C_STOP	Logical and of corresponding request and mask bits. Default Value: 0
3	I2C_WRITE_STOP	Logical and of corresponding request and mask bits. Default Value: 0
2	I2C_ACK	Logical and of corresponding request and mask bits. Default Value: 0
1	I2C_NACK	Logical and of corresponding request and mask bits. Default Value: 0
0	I2C_ARB_LOST	Logical and of corresponding request and mask bits. Default Value: 0

28.1.72 SCB0_INTR_TX

Transmitter interrupt request register.

Address: 0x40240F80

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	None		RW1C	RW1C
HW Access	RW1S	RW1S	RW1S	RW1S	None		RW1S	RW1S
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	EMPTY	None [3:2]		NOT_FULL	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW1C	RW1C	RW1C
HW Access	None					RW1S	RW1S	RW1S
Name	None [15:11]					UART_ARB_LOST	UART_DONE	UART_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10	UART_ARB_LOST	UART lost arbitration: the value driven on the TX line is not the same as the value observed on the RX line. This condition event is usefull when transmitter and receiver share a TX/RX line. This is the case in LIN or SmartCard modes. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
9	UART_DONE	UART transmitter done event. This happens when the IP is done transferring all data in the TX FIFO; i.e. EMPTY is '1'. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
8	UART_NACK	UART transmitter received a negative acknowledgement in SmartCard mode. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
7	BLOCKED	AHB-Lite write transfer can not get access to the EZ memory (EZ data access), due to an externally clocked EZ access. This may happen when STATUS.EC_BUSY is '1'. Default Value: 0

(continued)

6	UNDERFLOW	Attempt to read from an empty TX FIFO. This happens when the IP is ready to transfer data and EMPTY is '1'. Only used in FIFO mode. Default Value: 0
5	OVERFLOW	Attempt to write to a full TX FIFO. Only used in FIFO mode. Default Value: 0
4	EMPTY	TX FIFO is empty; i.e. it has 0 entries. Only used in FIFO mode. Default Value: 0
1	NOT_FULL	TX FIFO is not full. Dependent on CTRL.BYTE_MODE: BYTE_MODE is '0': # entries != FF_DATA_NR/2. BYTE_MODE is '1': # entries != FF_DATA_NR. Only used in FIFO mode. Default Value: 0
0	TRIGGER	Less entries in the TX FIFO than the value specified by TX_FIFO_CTRL. Only used in FIFO mode. Default Value: 0

28.1.73 SCB0_INTR_TX_SET

Transmitter interrupt set request register

Address: 0x40240F84

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	RW1S	None		RW1S	RW1S
HW Access	A	A	A	A	None		A	A
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	EMPTY	None [3:2]		NOT_FULL	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW1S	RW1S	RW1S
HW Access	None					A	A	A
Name	None [15:11]					UART_ARB_LOST	UART_DONE	UART_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10	UART_ARB_LOST	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
9	UART_DONE	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
8	UART_NACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
7	BLOCKED	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
6	UNDERFLOW	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
5	OVERFLOW	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
4	EMPTY	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

(continued)

1	NOT_FULL	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	TRIGGER	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

28.1.74 SCB0_INTR_TX_MASK

Transmitter interrupt mask register.

Address: 0x40240F88

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	None		RW	RW
HW Access	R	R	R	R	None		R	R
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	EMPTY	None [3:2]		NOT_FULL	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [15:11]					UART_ARB_LOST	UART_DONE	UART_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10	UART_ARB_LOST	Mask bit for corresponding bit in interrupt request register. Default Value: 0
9	UART_DONE	Mask bit for corresponding bit in interrupt request register. Default Value: 0
8	UART_NACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
7	BLOCKED	Mask bit for corresponding bit in interrupt request register. Default Value: 0
6	UNDERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
5	OVERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
4	EMPTY	Mask bit for corresponding bit in interrupt request register. Default Value: 0

(continued)

1	NOT_FULL	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	TRIGGER	Mask bit for corresponding bit in interrupt request register. Default Value: 0

28.1.75 SCB0_INTR_TX_MASKED

Transmitter interrupt masked request register

Address: 0x40240F8C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	None		R	R
HW Access	W	W	W	W	None		W	W
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	EMPTY	None [3:2]		NOT_FULL	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None					R	R	R
HW Access	None					W	W	W
Name	None [15:11]					UART_ARB_LOST	UART_DONE	UART_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10	UART_ARB_LOST	Logical and of corresponding request and mask bits. Default Value: 0
9	UART_DONE	Logical and of corresponding request and mask bits. Default Value: 0
8	UART_NACK	Logical and of corresponding request and mask bits. Default Value: 0
7	BLOCKED	Logical and of corresponding request and mask bits. Default Value: 0
6	UNDERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
5	OVERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
4	EMPTY	Logical and of corresponding request and mask bits. Default Value: 0

(continued)

1	NOT_FULL	Logical and of corresponding request and mask bits. Default Value: 0
0	TRIGGER	Logical and of corresponding request and mask bits. Default Value: 0

28.1.76 SCB0_INTR_RX

Receiver interrupt request register.

Address: 0x40240FC0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	None	RW1C	RW1C	None	RW1C
HW Access	RW1S	RW1S	RW1S	None	RW1S	RW1S	None	RW1S
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	None	FULL	NOT_EMPTY	None	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW1C	RW1C	RW1C	RW1C
HW Access	None				RW1S	RW1S	RW1S	RW1S
Name	None [15:12]				BREAK_DETECT	BAUD_DETECT	PARITY_ERROR	FRAME_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	BREAK_DETECT	Break detection is successful: the line is '0' for UART_RX_CTRL.BREAK_WIDTH + 1 bit period. Can occur at any time to address unanticipated break fields; i.e. "break-in-data" is supported. This feature is supported for the UART standard and LIN submodes. For the UART standard submodes, ongoing receipt of data frames is NOT affected; i.e. Firmware is ecpected to take the proper action. For the LIN submode, possible ongoing receipt of a data frame is stopped and the (partially) received data frame is dropped and baud rate detection is started. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
10	BAUD_DETECT	LIN baudrate detection is completed. The receiver software uses the UART_RX_STATUS.BR_COUNTER value to set the right IP clock (from the programmable clock IP) to guarantee successful receipt of the first LIN data frame (Protected Identifier Field) after the synchronization byte. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0

(continued)

9	PARITY_ERROR	Parity error in received data frame. Set to '1', when event is detected. Write with '1' to clear bit. If UART_RX_CTL.DROP_ON_PARITY_ERROR is '1', the received frame is dropped. If UART_RX_CTL.DROP_ON_PARITY_ERROR is '0', the received frame is send to the RX FIFO. In SmartCard submode, negatively acknowledged data frames generate a parity error. Note that Firmware can only identify the erroneous data frame in the RX FIFO if it is fast enough to read the data frame before the hardware writes a next data frame into the RX FIFO. Default Value: 0
8	FRAME_ERROR	Frame error in received data frame. Set to '1', when event is detected. Write with '1' to clear bit. This can be either a start or stop bit(s) error: Start bit error: after the detection of the beginning of a start bit period (RX line changes from '1' to '0'), the middle of the start bit period is sampled erroneously (RX line is '1'). Note: a start bit error is detected BEFORE a data frame is received. Stop bit error: the RX line is sampled as '0', but a '1' was expected. Note: a stop bit error may result in failure to receive successive data frame(s). Note: a stop bit error is detected AFTER a data frame is received. A stop bit error is detected after a data frame is received, and the UART_RX_CTL.DROP_ON_FRAME_ERROR field specifies whether the received frame is dropped or send to the RX FIFO. If UART_RX_CTL.DROP_ON_FRAME_ERROR is '1', the received data frame is dropped. If UART_RX_CTL.DROP_ON_FRAME_ERROR is '0', the received data frame is send to the RX FIFO. Note that Firmware can only identify the erroneous data frame in the RX FIFO if it is fast enough to read the data frame before the hardware writes a next data frame into the RX FIFO; i.e. the RX FIFO does not have error flags to tag erroneous data frames. Default Value: 0
7	BLOCKED	AHB-Lite read transfer can not get access to the EZ memory (EZ_DATA accesses), due to an externally clocked EZ access. This may happen when STATUS.EC_BUSY is '1'. Default Value: 0
6	UNDERFLOW	Attempt to read from an empty RX FIFO. Only used in FIFO mode. Default Value: 0
5	OVERFLOW	Attempt to write to a full RX FIFO. Note: in I2C mode, the OVERFLOW is set when a data frame is received and the RX FIFO is full, independent of whether it is ACK'd or NACK'd. Only used in FIFO mode. Default Value: 0
3	FULL	RX FIFO is full. Note that received data frames are lost when the RX FIFO is full. Dependent on CTRL.BYTE_MODET: BYTE_MODE is '0': # entries == FF_DATA_NR/2. BYTE_MODE is '1': # entries == FF_DATA_NR. Only used in FIFO mode. Default Value: 0
2	NOT_EMPTY	RX FIFO is not empty. Only used in FIFO mode. Default Value: 0
0	TRIGGER	More entries in the RX FIFO than the value specified by TRIGGER_LEVEL in SCB_RX_FIFO_CTL. Only used in FIFO mode. Default Value: 0

28.1.77 SCB0_INTR_RX_SET

Receiver interrupt set request register.

Address: 0x40240FC4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	None	RW1S	RW1S	None	RW1S
HW Access	A	A	A	None	A	A	None	A
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	None	FULL	NOT_EMPTY	None	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW1S	RW1S	RW1S	RW1S
HW Access	None				A	A	A	A
Name	None [15:12]				BREAK_DETECT	BAUD_DETECT	PARITY_ERROR	FRAME_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	BREAK_DETECT	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
10	BAUD_DETECT	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
9	PARITY_ERROR	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
8	FRAME_ERROR	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
7	BLOCKED	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
6	UNDERFLOW	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
5	OVERFLOW	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0

(continued)

3	FULL	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
2	NOT_EMPTY	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
0	TRIGGER	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

28.1.78 SCB0_INTR_RX_MASK

Receiver interrupt mask register.

Address: 0x40240FC8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	None	RW	RW	None	RW
HW Access	R	R	R	None	R	R	None	R
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	None	FULL	NOT_EMPTY	None	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [15:12]				BREAK_DETECT	BAUD_DETECT	PARITY_ERROR	FRAME_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	BREAK_DETECT	Mask bit for corresponding bit in interrupt request register. Default Value: 0
10	BAUD_DETECT	Mask bit for corresponding bit in interrupt request register. Default Value: 0
9	PARITY_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
8	FRAME_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
7	BLOCKED	Mask bit for corresponding bit in interrupt request register. Default Value: 0
6	UNDERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
5	OVERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0

(continued)

3	FULL	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	NOT_EMPTY	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	TRIGGER	Mask bit for corresponding bit in interrupt request register. Default Value: 0

28.1.79 SCB0_INTR_RX_MASKED

Receiver interrupt masked request register

Address: 0x40240FCC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	None	R	R	None	R
HW Access	W	W	W	None	W	W	None	W
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	None	FULL	NOT_EMPTY	None	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None				R	R	R	R
HW Access	None				W	W	W	W
Name	None [15:12]				BREAK_DETECT	BAUD_DETECT	PARITY_ERROR	FRAME_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	BREAK_DETECT	Logical and of corresponding request and mask bits. Default Value: 0
10	BAUD_DETECT	Logical and of corresponding request and mask bits. Default Value: 0
9	PARITY_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
8	FRAME_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
7	BLOCKED	Logical and of corresponding request and mask bits. Default Value: 0
6	UNDERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
5	OVERFLOW	Logical and of corresponding request and mask bits. Default Value: 0

(continued)

3	FULL	Logical and of corresponding request and mask bits. Default Value: 0
2	NOT_EMPTY	Logical and of corresponding request and mask bits. Default Value: 0
0	TRIGGER	Logical and of corresponding request and mask bits. Default Value: 0

28.1.80 SCB1_CTRL

Generic control register.

Address: 0x40250000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				OVS [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [15:12]				BYTE_MODE	EZ_MODE	EC_OP_MODE	EC_AM_MODE

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [23:18]						BLOCK	ADDR_ACCEPT

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None					RW	
HW Access	R	None					R	
Name	ENABLED	None [30:26]					MODE [25:24]	

Bits	Name	Description
31	ENABLED	IP enabled ('1') or not ('0'). The proper order in which to initialize the IP is as follows: - Program protocol specific information using SPI_CTRL, UART_CTRL (and UART_TX_CTRL and UART_RX_CTRL) or I2C_CTRL. This includes selection of a submode, master/slave functionality and transmitter/receiver functionality when applicable. - Program generic transmitter (TX_CTRL) and receiver (RX_CTRL) information. This includes enabling of the transmitter and receiver functionality. - Program transmitter FIFO (TX_FIFO_CTRL) and receiver FIFO (RX_FIFO_CTRL) information. - Program CTRL to enable IP, select the specific operation mode and oversampling factor. When the IP is enabled, no control information should be changed. Changes should be made AFTER disabling the IP, e.g. to modify the operation mode (from I2C to SPI) or to go from externally to internally clocked. The change takes effect after the IP is re-enabled. Note that disabling the IP will cause re-initialization of the design and associated state is lost (e.g. FIFO content). Default Value: 0
25 : 24	MODE	Mode of operation (3: Reserved) Default Value: 3 **0x0: I2C:** Inter-Integrated Circuits (I2C) mode. **0x1: SPI:** Serial Peripheral Interface (SPI) mode.

(continued)

		0x2: UART: Universal Asynchronous Receiver/Transmitter (UART) mode.
17	BLOCK	Only used in externally clocked mode. If the externally clocked logic and the MMIO SW accesses to EZ memory coincide/collide, this bit determines whether a SW access should block and result in bus wait states ('BLOCK is 1') or not (BLOCK is '0'). IF BLOCK is 0 and the accesses collide, MMIO read operations return 0xffff:ffff and MMIO write operations are ignored. Colliding accesses are registered as interrupt causes: field BLOCKED of MMIO registers INTR_TX and INTR_RX. Default Value: 0
16	ADDR_ACCEPT	Determines whether a received matching address is accepted in the RX FIFO ('1') or not ('0'). In I2C mode, this field is used to allow the slave to put the received slave address or general call address in the RX FIFO. Note that a received matching address is put in the RX FIFO when ADDR_ACCEPT is '1' for both I2C read and write transfers. In multi-processor UART receiver mode, this field is used to allow the receiver to put the received address in the RX FIFO. Note: non-matching addresses are never put in the RX FIFO. Default Value: 0
11	BYTE_MODE	Determines the number of bits per FIFO data element: '0': 16-bit FIFO data elements. '1': 8-bit FIFO data elements. This mode doubles the amount of FIFO entries, but TX_CTRL.DATA_WIDTH and RX_CTRL.DATA_WIDTH are restricted to [0, 7]. Default Value: 0
10	EZ_MODE	Non EZ mode ('0') or EZ mode ('1'). In EZ mode, a meta protocol is applied to the serial interface protocol. This meta protocol adds meaning to the data frames transferred by the serial interface protocol: a data frame can represent a memory address, a write memory data element or a read memory data element. EZ mode is only used for synchronous serial interface protocols: SPI and I2C. In SPI mode, only Motorola submode (all Motorola modes: 0, 1, 2, 3) is supported and the transmitter should use continuous data frames; i.e. data frames mot seperated by slave deselection. This mode is only applicable to slave functionality. In EZ mode, the slave can read from and write to an addressable memory structure of 32 bytes. In EZ mode, data frames should 8-bit in size and should be transmitted and received with the Most Significant Bit (MSB) first. In UART mode this field should be '0'. Default Value: 0
9	EC_OP_MODE	Internally clocked mode ('0') or externally clocked mode ('1') operation. In internally clocked mode, the serial interface protocols run off the peripheral clock. In externally clocked mode, the serial interface protocols run off the clock as provided by the serial interface. Externally clocked operation mode is only used for synchronous serial interface protocols (SPI and I2C) in slave mode AND EZ mode. In SPI mode, only Motorola submode (all Motorola modes: 0, 1, 2, 3) is supported. The maximum SPI slave, EZ mode bitrate is 48 Mbps (transmission and IO delays outside the IP will degrade the effective bitrate). In UART mode this field should be '0'. Default Value: 0
8	EC_AM_MODE	Internally clocked mode ('0') or externally clocked mode ('1') address matching (I2C) or selection (SPI). In internally clocked mode, the serial interface protocols run off the peripheral clock. In externally clocked mode, the serial interface protocols run off the clock as provided by the serial interface. Externally clocked mode is only used for synchronous serial interface protocols (SPI and I2C) in slave mode. In SPI mode, only Motorola submode (all Motorola modes: 0, 1, 2, 3) is supported. In UART mode this field should be '0'. Default Value: 0

(continued)

3 : 0	OVS	Serial interface bit period oversampling factor expressed in IP clock cycles. Used for SPI and UART functionality. OVS + 1 IP clock cycles constitute a single serial interface clock/bit cycle. The IP clock is provided by the programmable clock IP. This field is NOT used in externally clocked mode. If OVS is odd, the oversampling factor is even and the first and second phase of the interface clock period are the same. If OVS is even, the oversampling factor is odd and the first phase of the interface clock period is 1 peripheral clock cycle longer than the second phase of the interface clock period. In SPI master mode, the valid range is [3, 15]. At an IP frequency of 48 MHz, the maximum IP bit rate is 12 Mbps. The effective system bit rate is dependent on the external SPI slave that we communicate with. If the SPI output clock "spi_clk_out" to SPI MISO input "spi_miso_in" round trip delay is introducing significant delays (multiple "spi_clk_out" cycles), it may be necessary to increase OVS and/or to set SPI_CTRL.LATE_MISO_SAMPLE to '1' to achieve the maximum possible system bit rate. The maximum IP bit rate of 12 Mbps provides an IP centric perspective, assuming ideal (0 ns) IO cell and routing (chip and board) delay. The required IP clock/IF clock ratio increases and the calculated maximum bit rate decreases, when realistic chip and routing delays are taken into account. In SPI slave mode, the OVS field is NOT used. However, there is a frequency requirement for the IP clock wrt. the interface (IF) clock to guarantee functional correct behavior. This requirement is expressed as a ratio: IP clock/IF clock. The ratio is dependent on the setting of RX_CTRL.MEDIAN and the external SPI master's capability to support "late MISO sample" functionality (similar to our SPI master functionality represented by SPI_CTRL.LATE_MISO_SAMPLE): - MEDIAN is '0' and external SPI master has NO "late MISO sample functionality": IP clock/IF clock >= 6. At a IP frequency of 48 MHz, the maximum bit rate is 8 Mbps. - MEDIAN is '0' and external SPI master has "late MISO sample functionality": IP clock/IF clock >= 3. At a IP frequency of 48 MHz, the maximum bit rate is 16 Mbps. - MEDIAN is '1' and external SPI master has NO "late MISO sample functionality": IP clock/IF clock >= 8. At a IP frequency of 48 MHz, the maximum bit rate is 6 Mbps. - MEDIAN is '1' and external SPI master has "late MISO sample functionality": IP clock/IF clock >= 4. At a IP frequency of 48 MHz, the maximum bit rate is 12 Mbps. The maximum bit rates provide an IP centric perspective, assuming ideal (0 ns) IO cell and routing (chip and board) delay. The required IP clock/IF clock ratio increases and the calculated maximum bit rate decreases, when realistic chip and routing delays are taken into account. In UART standard submode (including LIN), the valid range is [7, 15]. In UART SmartCard submode, the valid range is [7, 15]. In UART TX IrDA submode this field indirectly specifies the oversampling. The oversampling determines the interface clock/bit cycle and the width of the pulse. Only normal transmission mode is supported, the pulse is roughly 3/16 of the bit period (for all bit rates). There is only one valid OVS value: - 0: 16 times oversampling. IP clock frequency of 16*115.2 KHz for 115.2 Kbps. IP clock frequency of 16*57.6 KHz for 57.6 Kbps. IP clock frequency of 16*38.4 KHz for 38.4 Kbps. IP clock frequency of 16*19.2 KHz for 19.2 Kbps. IP clock frequency of 16*9.6 KHz for 9.6 Kbps. IP clock frequency of 16*2.4 KHz for 2.4 Kbps. IP clock frequency of 16*1.2 KHz for 1.2 Kbps. - all other values are not used in normal mode.

(continued)

In UART RX IrDA submode (1.2, 2.4, 9.6, 19.2, 38.4, 57.6 and 115.2 Kbps) this field indirectly specifies the oversampling. The oversampling determines the interface clock/bit cycle and the width of the pulse. In normal transmission mode, this pulse is roughly 3/16 of the bit period (for all bit rates). In low power transmission mode, this pulse is potentially smaller (down to 1.62 us typical and 1.41 us minimal) than 3/16 of the bit period (for < 115.2 Kbps bitrates). Pulse widths greater or equal than two IP clock cycles are guaranteed to be detected by the receiver. Pulse widths less than two IP clock cycles and greater or equal than one IP clock cycle may be detected by the receiver. Pulse widths less than one IP clock cycle will not be detected by the receiver. RX_CTRL.MEDIAN should be set to '1' for IrDA receiver functionality. The IP clock (as provided by the programmable clock IP) and the oversampling together determine the IrDA bitrate. Normal mode, OVS field values (with the required IP clock frequency):

- 0: 16 times oversampling.
  IP clock frequency of 16*115.2 KHz for 115.2 Kbps.
  IP clock frequency of 16*57.6 KHz for 57.6 Kbps.
  IP clock frequency of 16*38.4 KHz for 38.4 Kbps.
  IP clock frequency of 16*19.2 KHz for 19.2 Kbps.
  IP clock frequency of 16*9.6 KHz for 9.6 Kbps.
  IP clock frequency of 16*2.4 KHz for 2.4 Kbps.
  IP clock frequency of 16*1.2 KHz for 1.2 Kbps.
- all other values are not used in normal mode.

Low power mode, OVS field values (with the required IP clock frequency):

- 0: 16 times oversampling.
  IP clock frequency of 16*115.2 KHz for 115.2 Kbps.
- 1: 32 times oversampling.
  IP clock frequency of 32*57.6 KHz for 57.6 Kbps.
- 2: 48 times oversampling.
  IP clock frequency of 48*38.4 KHz for 38.4 Kbps.
- 3: 96 times oversampling.
  IP clock frequency of 96*19.2 KHz for 19.2 Kbps.
- 4: 192 times oversampling.
  IP clock frequency of 192*9.6 KHz for 9.6 Kbps.
- 5: 768 times oversampling.
  IP clock frequency of 768*2.4 KHz for 2.4 Kbps.
- 6: 1536 times oversampling.
  IP clock frequency of 1536*1.2 KHz for 1.2 Kbps.
- all other values are not used in low power mode.

Default Value: 15

28.1.81 SCB1_STATUS

Generic status register.

Address: 0x40250004

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							W
Name	None [7:1]							EC_BUSY

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	EC_BUSY	Inidicates whether the externally clocked logic is potentially accessing the EZ memory (this is only possible in EZ mode). This bit can be used by SW to determine whether it is safe to issue a SW access to the EZ memory (without bus wait states (a blocked SW access) or bus errors being generated). Note that the INTR_TX.BLOCKED and INTR_RX.BLOCKED interrupt causes are used to indicate whether a SW access was actually blocked by externally clocked logic. Default Value: Undefined

28.1.82 SCB1_SPI_CTRL

SPI control register.

Address: 0x40250020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		R	R	R	R	R	R
Name	None [7:6]		SCLK_CONTINUOUS	LATE_MISO_SAMPLE	CPOL	CPHA	SELECT_PRECEDE	CONTINU-OUS

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [15:12]				SSEL_POLARITY3	SSEL_POLARITY2	SSEL_POLARITY1	SSEL_POLARITY0

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							LOOPBACK

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None			RW		RW	
HW Access	R	None			R		R	
Name	MASTER_MODE	None [30:28]			SLAVE_SELECT [27:26]		MODE [25:24]	

Bits	Name	Description
31	MASTER_MODE	Master ('1') or slave ('0') mode. In master mode, transmission will commence on availability of data frames in the TX FIFO. In slave mode, when selected and there is no data frame in the TX FIFO, the slave will transmit all '1's. In both master and slave modes, received data frames will be lost if the RX FIFO is full. Default Value: 0
27 : 26	SLAVE_SELECT	Selects one of the four outgoing SPI slave select signals: - 0: Slave 0, SPI_SELECT[0]. - 1: Slave 1, SPI_SELECT[1]. - 2: Slave 2, SPI_SELECT[2]. - 3: Slave 3, SPI_SELECT[3]. Only used in master mode. The IP should be disabled when changes are made to this field. Default Value: 0
25 : 24	MODE	Submode of SPI operation (3: Reserved). Default Value: 3

(continued)

		0x0: SPI_MOTOROLA: SPI Motorola submode. In master mode, when not transmitting data (SELECT is inactive), SCLK is stable at CPOL. In slave mode, when not selected, SCLK is ignored; i.e. it can be either stable or clocking. In master mode, when there is no data to transmit (TX FIFO is empty), SELECT is inactive. **0x1: SPI_TI:** SPI Texas Instruments submode. In master mode, when not transmitting data, SCLK is stable at '0'. In slave mode, when not selected, SCLK is ignored; i.e. it can be either stable or clocking. In master mode, when there is no data to transmit (TX FIFO is empty), SELECT is inactive; i.e. no pulse is generated. **0x2: SPI_NS:** SPI National Semiconducturs submode. In master mode, when not transmitting data, SCLK is stable at '0'. In slave mode, when not selected, SCLK is ignored; i.e. it can be either stable or clocking. In master mode, when there is no data to transmit (TX FIFO is empty), SELECT is inactive.
16	LOOPBACK	Local loopback control (does NOT affect the information on the pins). Only used in master mode. Not used in National Semiconductors submode. '0': the SPI master MISO line "spi_miso_in" is connected to the SPI MISO pin. '1': the SPI master MISO line "spi_miso_in" is connected to the SPI master MOSI line "spi_mosi_out". In other words, in loopback mode the SPI master receives on MISO what it transmits on MOSI. Default Value: 0
11	SSEL_POLARITY3	Slave select polarity. SSEL_POLARITY3 applies to the outgoing SPI slave select signal 3 (master mode). Default Value: 0
10	SSEL_POLARITY2	Slave select polarity. SSEL_POLARITY2 applies to the outgoing SPI slave select signal 2 (master mode). Default Value: 0
9	SSEL_POLARITY1	Slave select polarity. SSEL_POLARITY1 applies to the outgoing SPI slave select signal 1 (master mode). Default Value: 0
8	SSEL_POLARITY0	Slave select polarity. SSEL_POLARITY0 applies to the outgoing SPI slave select signal 0 (master mode) and to the incoming SPI slave select signal (slave mode). For Motorola and National Semiconductors submodes: '0': slave select is low/'0' active. '1': slave select is high/'1' active. For Texas Istruments submode: '0': high/'1' active precede/coincide pulse. '1': low/'0' active precede/coincide pulse. Default Value: 0
5	SCLK_CONTINUOUS	Only applicable in master mode. '0': SCLK is generated, when the SPI master is enabled and data is transmitted. '1': SCLK is generated, when the SPI master is enabled. This mode is useful for slave devices that use SCLK for functional operation other than just SPI functionality. Default Value: 0

(continued)

4	LATE_MISO_SAMPLE	Changes the SCLK edge on which MISO is captured. Only used in master mode. When '0', the default applies (for Motorola as determined by CPOL and CPHA, for Texas Instruments on the falling edge of SCLK and for National Semiconductors on the rising edge of SCLK). When '1', the alternate clock edge is used (which comes half a SPI SCLK period later). Late sampling addresses the round trip delay associated with transmitting SCLK from the master to the slave and transmitting MISO from the slave to the master. Default Value: 0
3	CPOL	Indicates the clock polarity. Only used in SPI Motorola submode. This field, together with the CPHA field, indicates when MOSI data is driven and MISO data is captured: - CPOL is 0: SCLK is 0 when not transmitting data. - CPOL is 1: SCLK is 1 when not transmitting data. Default Value: 0
2	CPHA	Only applicable in SPI Motorola submode. Indicates the clock phase. This field, together with the CPOL field, indicates when MOSI data is driven and MISO data is captured: - Motorola mode 0. CPOL is 0, CPHA is 0: MOSI is driven on a falling edge of SCLK. MISO is captured on a rising edge of SCLK. - Motorola mode 1. CPOL is 0, CPHA is 1: MOSI is driven on a rising edge of SCLK. MISO is captured on a falling edge of SCLK. - Motorola mode 2. CPOL is 1, CPHA is 0: MOSI is driven on a rising edge of SCLK. MISO is captured on a falling edge of SCLK. - Motorola mode 3. CPOL is 1, CPHA is 1: MOSI is driven on a falling edge of SCLK. MISO is captured on a rising edge of SCLK. Default Value: 0
1	SELECT_PRECEDE	Only used in SPI Texas Instruments' submode. When '1', the data frame start indication is a pulse on the SELECT line that precedes the transfer of the first data frame bit. When '0', the data frame start indication is a pulse on the SELECT line that coincides with the transfer of the first data frame bit. Default Value: 0
0	CONTINUOUS	Continuous SPI data transfers enabled ('1') or not ('0'). This field is used in master mode. In slave mode, both continuous and non-continuous SPI data transfers are supported independent of this field. When continuous transfers are enabled individual data frame transfers are not necessarily seperated by slave deselection (as indicated by the level or pulse on the SELECT line): if the TX FIFO has multiple data frames, data frames are send out without slave deselection. When continuous transfers are not enabled individual data frame transfers are always seperated by slave deselection: independent of the availability of TX FIFO data frames, data+G65 frames are send out with slave deselection. Default Value: 0

28.1.83 SCB1_SPI_STATUS

SPI status register.

Address: 0x40250024

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						W	W
Name	None [7:2]						SPI_EC_BUSY	BUS_BUSY

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	CURR_EZ_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	BASE_EZ_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	BASE_EZ_ADDR	SPI base EZ address. Address as provided by a SPI write transfer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable, as clock domain synchronization is not performed in the design. Default Value: Undefined
15 : 8	CURR_EZ_ADDR	SPI current EZ address. Current address pointer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable (during an ongoing transfer when SPI_EC_BUSY is '1'), as clock domain synchronization is not performed in the design. Default Value: Undefined
1	SPI_EC_BUSY	Inidicates whether the externally clocked logic is potentially accessing the EZ memory and/or updating BASE_ADDR or CURR_ADDR (this is only possible in EZ mode). This bit can be used by SW to determine whether BASE_ADDR and CURR_ADDR are reliable. Default Value: Undefined
0	BUS_BUSY	SPI bus is busy. The bus is considered busy ('1') during an ongoing transaction. For Motorola and National submodes, the busy bit is '1', when the slave selection (low active) is activated. For TI submode, the busy bit is '1' from the time the preceding/coinciding slave select (high active) is activated for the first transmitted data frame, till the last MOSI/MISO bit of the last data frame is transmitted. Default Value: Undefined

28.1.84 SCB1_UART_CTRL

UART control register.

Address: 0x40250040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							LOOPBACK

Bits	31	30	29	28	27	26	25	24
SW Access	None						RW	
HW Access	None						R	
Name	None [31:26]						MODE [25:24]	

Bits	Name	Description
25 : 24	MODE	Submode of UART operation (3: Reserved) Default Value: 3 **0x0: UART_STD:** Standard UART submode. **0x1: UART_SMARTCARD:** SmartCard (ISO7816) submode. Support for negative acknowledgement (NACK) on the receiver side and retransmission on the transmitter side. **0x2: UART_IRDA:** Infrared Data Association (IrDA) submode. Return to Zero modulation scheme. In this mode, the oversampling factor should be 16, that is OVS is 15.
16	LOOPBACK	Local loopback control (does NOT affect the information on the pins). When '0', the transmitter TX line "uart_tx_out" is connected to the TX pin and the receiver RX line "uart_rx_in" is connected to the RX pin. When '1', the transmitter TX line "uart_tx_out" is connected to the receiver RX line "uart_rx_in". A similar connections scheme is followed for "uart_rts_out" and "uart_cts_in". This allows a SCB UART transmitter to communicate with its receiver counterpart. Default Value: 0

28.1.85 SCB1_UART_TX_CTRL

UART transmitter control register.

Address: 0x40250044

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	None	RW		
HW Access	None		R	R	None	R		
Name	None [7:6]		PARITY_ENABLED	PARITY	None	STOP_BITS [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							RETRY_ON_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	RETRY_ON_NACK	When '1', a data frame is retransmitted when a negative acknowledgement is received. Only applicable to the SmartCard submode. Default Value: 0
5	PARITY_ENABLED	Parity generation enabled ('1') or not ('0'). Only applicable in standard UART submodes. In SmartCard submode, parity generation is always enabled through hardware. In IrDA submode, parity generation is always disabled through hardware Default Value: 0
4	PARITY	Parity bit. When '0', the transmitter generates an even parity. When '1', the transmitter generates an odd parity. Only applicable in standard UART and SmartCard submodes. Default Value: 0
2 : 0	STOP_BITS	Stop bits. STOP_BITS + 1 is the duration of the stop period in terms of halve bit periods. Valid range is [1, 7]; i.e. a stop period should last at least one bit period. Default Value: 2

28.1.86 SCB1_UART_RX_CTRL

UART receiver control register.

Address: 0x40250048

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	RW	RW	None	RW		
HW Access	None	R	R	R	None	R		
Name	None	POLARITY	PARITY_ENABLED	PARITY	None	STOP_BITS [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW	RW	None	RW	RW	RW
HW Access	None		R	R	None	R	R	R
Name	None [15:14]		SKIP_START	LIN_MODE	None	MP_MODE	DROP_ON_FRAME_ERROR	DROP_ON_PARITY_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				BREAK_WIDTH [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	BREAK_WIDTH	Break width. BREAK_WIDTH + 1 is the minimum width in bit periods of a break. During a break the transmitted/received line value is '0'. This feature is useful for standard UART submode and LIN submode ("break field" detection). Once, the break is detected, the INTR_RX.BREAK_DETECT bit is set to '1'. Note that break detection precedes baud rate detection, which is used to synchronize/refine the receiver clock to the transmitter clock. As a result, break detection operates with an unsynchronized/unrefined receiver clock. Therefore, the receiver's definition of a bit period is imprecise and the setting of this field should take this imprecision into account. The LIN standard also accounts for this imprecision: a LIN start bit followed by 8 data bits allows for up to 9 consecutive '0' bit periods during regular transmission, whereas the LIN break detection should be at least 13 consecutive '0' bit periods. This provides for a margin of 4 bit periods. Therefore, the default value of this field is set to 10, representing a minimal break field with of 10+1 = 11 bit periods; a value in between the 9 consecutive bit periods of a regular transmission and the 13 consecutive bit periods of a break field. This provides for slight imprecisions of the receiver clock wrt. the transmitter clock. There should not be a need to program this field to any value other than its default value. Default Value: 10

(continued)

13	SKIP_START	Only applicable in standard UART submode. When '1', the receiver skips start bit detection for the first received data frame. Instead, it synchronizes on the first received data frame bit, which should be a '1'. This functionality is intended for wake up from DeepSleep when receiving a data frame. The transition from idle ('1') to START ('0') on the RX line is used to wake up the CPU. The transition detection (and the associated wake up functionality) is performed by the GPIO2 IP. The woken up CPU will enable the SCB's UART receiver functionality. Once enabled, it is assumed that the START bit is ongoing (the CPU wakeup and SCB enable time should be less than the START bit period). The SCB will synchronize to a '0' to '1' transition, which indicates the first data frame bit is received (first data frame bit should be '1'). After synchronization to the first data frame bit, the SCB will resume normal UART functionality: subsequent data frames will be synchronized on the receipt of a START bit. Default Value: 0
12	LIN_MODE	Only applicable in standard UART submode. When '1', the receiver performs break detection and baud rate detection on the incoming data. First, break detection counts the amount of bit periods that have a line value of '0'. BREAK_WIDTH specifies the minum required amount of bit periods. Successful break detection sets the INTR_RX.BREAK_DETECT interrupt cause to '1'. Second, baud rate detection counts the amount of peripheral clock periods that are use to receive the synchronization byte (0x55; least significant bit first). The count is available through UART_RX_STATUS.BR_COUNTER. Successful baud rate detection sets the INTR_RX.BAUD_DETECT interrupt cause to '1' (BR_COUNTER is reliable). This functionality is used to synchronize/refine the receiver clock to the transmitter clock. The receiver software can use the BR_COUNTER value to set the right IP clock (from the programmable clock IP) to guarantee successful receipt of the first LIN data frame (Protected Identifier Field) after the synchronization byte. Default Value: 0
10	MP_MODE	Multi-processor mode. When '1', multi-processor mode is enabled. In this mode, RX_CTRL.DATA_WIDTH should indicate a 9-bit data frame. In multi-processor mode, the 9th received bit of a data frame seperates addresses (bit is '1') from data (bit is '0'). A received address is matched with RX_MATCH.DATA and RX_MATCH.MASK. In the case of a match, subsequent received data are sent to the RX FIFO. In the case of NO match, subsequent received data are dropped. Default Value: 0
9	DROP_ON_FRAME_ERROR	Behaviour when an error is detected in a start or stop period. When '0', received data is send to the RX FIFO. When '1', received data is dropped and lost. Default Value: 0
8	DROP_ON_PARITY_ERROR	Behaviour when a parity check fails. When '0', received data is send to the RX FIFO. When '1', received data is dropped and lost. Only applicable in standard UART and SmartCard submodes (negatively acknowledged SmartCard data frames may be dropped with this field). Default Value: 0
6	POLARITY	Inverts incoming RX line signal "uart_rx_in". Inversion is after local loopback. This functionality is intended for IrDA receiver functionality. Default Value: 0
5	PARITY_ENABLED	Parity checking enabled ('1') or not ('0'). Only applicable in standard UART submode. In SmartCard submode, parity checking is always enabled through hardware. In IrDA submode, parity checking is always disabled through hardware. Default Value: 0
4	PARITY	Parity bit. When '0', the receiver expects an even parity. When '1', the receiver expects an odd parity. Only applicable in standard UART and SmartCard submodes. Default Value: 0

(continued)

2 : 0	STOP_BITS	Stop bits. STOP_BITS + 1 is the duration of the stop period in terms of halve bit periods. Valid range is [1, 7]; i.e. a stop period should last at least one bit period. If STOP_BITS is '1', stop bits error detection is NOT performed. If STOP_BITS is in [2, 7], stop bits error detection is performed and the associated interrupt cause INTR_RX.FRAME_ERROR is set to '1' if an error is detected. In other words, the receiver supports data frames with a 1 bit period stop bit sequence, but requires at least 1.5 bit period stop bit sequences to detect errors. This limitation is due to possible transmitter and receiver clock skew that prevents the design from doing reliable stop bit detection for short (1 bit bit period) stop bit sequences. Note that in case of a stop bits error, the successive data frames may get lost as the receiver needs to resynchronize its start bit detection. The amount of lost data frames depends on both the amount of stop bits, the idle ('1') time between data frames and the data frame value. Default Value: 2

28.1.87 SCB1_UART_RX_STATUS

UART receiver status register.

Address: 0x4025004C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	BR_COUNTER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None				R			
HW Access	None				W			
Name	None [15:12]				BR_COUNTER [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11 : 0	BR_COUNTER	Amount of peripheral clock periods that constitute the transmission of a 0x55 data frame (sent least signficant bit first) as determined by the receiver. BR_COUNTER / 8 is the amount of peripheral clock periods that constitute a bit period. This field has valid data when INTR_RX.BAUD_DETECT is set to '1'. Default Value: Undefined

28.1.88 SCB1_UART_FLOW_CTRL

UART flow control register

Address: 0x40250050

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				TRIGGER_LEVEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							RTS_POLARITY

Bits	31	30	29	28	27	26	25	24
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [31:26]						CTS_ENABLED	CTS_POLARITY

Bits	Name	Description
25	CTS_ENABLED	Enable use of CTS input signal "uart_cts_in" by the UART transmitter: '0': Disabled. The UART transmitter ignores "uart_cts_in", and transmits when a data frame is available for transmission in the TX FIFO or the TX shift register. '1': Enabled. The UART transmitter uses "uart_cts_in" to qualify the transmission of data. It transmits when "uart_cts_in" is active and a data frame is available for transmission in the TX FIFO or the TX shift register. If UART_CTRL.LOOPBACK is '1', "uart_cts_in" is connected to "uart_rts_out" in the IP (both signals are subjected to signal polarity changes are indicated by RTS_POLARITY and CTS_POLARITY). Default Value: 0
24	CTS_POLARITY	Polarity of the CTS input signal "uart_cts_in": '0': CTS is low/'0' active; "uart_cts_in" is '0' when active and "uart_cts_in" is '1' when inactive. '1': CTS is high/'1' active; "uart_cts_in" is '1' when active and "uart_cts_in" is '0' when inactive. Default Value: 0

(continued)

16	RTS_POLARITY	Polarity of the RTS output signal "uart_rts_out": '0': RTS is low/'0' active; "uart_rts_out" is '0' when active and "uart_rts_out" is '1' when inactive. '1': RTS is high/'1' active; "uart_rts_out" is '1' when active and "uart_rts_out" is '0' when inactive. During IP reset (Hibernate system power mode), "uart_rts_out" is '1'. This represents an inactive state assuming a low/'0' active polarity. Default Value: 0
3 : 0	TRIGGER_LEVEL	Trigger level. When the receiver FIFO has less entries than the amount of this field, a Ready To Send (RTS) output signal "uart_rts_out" is activated. By setting this field to "0", flow control is effectively SW disabled (may be useful for debug purposes). Default Value: 0

28.1.89 SCB1_I2C_CTRL

I2C control register.

Address: 0x40250060

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	LOW_PHASE_OVS [7:4]				HIGH_PHASE_OVS [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	None	RW	RW
HW Access	R	R	R	R	R	None	R	R
Name	S_NOT_READY_DATA_NACK	S_NOT_READY_ADDR_NACK	S_READY_DATA_ACK	S_READY_ADDR_ACK	S_GENERAL_IGNORE	None	M_NOT_READY_DATA_NACK	M_READY_DATA_ACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							LOOPBACK

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None					
HW Access	R	R	None					
Name	MASTER_MODE	SLAVE_MODE	None [29:24]					

Bits	Name	Description
31	MASTER_MODE	Master mode enabled ('1') or not ('0'). Note that both master and slave modes can be enabled at the same time. This allows the IP to address itself. Default Value: 0
30	SLAVE_MODE	Slave mode enabled ('1') or not ('0'). Default Value: 0
16	LOOPBACK	Local loopback control (does NOT affect the information on the pins). Only applicable in master/slave mode. When '0', the I2C SCL and SDA lines are connected to the I2C SCL and SDA pins. When '1', I2C SCL and SDA lines are routed internally in the peripheral, and as a result unaffected by other I2C devices. This allows a SCB I2C peripheral to address itself. Default Value: 0
15	S_NOT_READY_DATA_NACK	For internally clocked logic only. Only used when: - non EZ mode. Functionality is as follows: - 1: a received data element byte the slave is immediately NACK'd when the receiver FIFO is full. - 0: clock stretching is performed (till the receiver FIFO is no longer full). Default Value: 1

(continued)

14	S_NOT_READY_ADDR_NACK	For internally clocked logic (EC_AM is '0' and EC_OP is '0') on an address match or general call address (and S_GENERAL_IGNORE is '0'). Only used when: - EC_AM is '0', EC_OP is '0' and non EZ mode. Functionality is as follows: - 1: a received (matching) slave address is immediately NACK'd when the receiver FIFO is full. - 0: clock stretching is performed (till the receiver FIFO is no longer full). For externally clocked logic (EC_AM is '1') on an address match or general call address (and S_GENERAL_IGNORE is '0'). Only used when (NOT used when EC_AM is '1' and EC_OP is '1' and address match and EZ mode): - EC_AM is '1' and EC_OP is '0'. - EC_AM is '1' and general call address match. - EC_AM is '1' and non EZ mode. Functionality is as follows: - 1: a received (matching or general) slave address is always immediately NACK'd. There are two possibilities: 1). the internally clocked logic is enabled (we are in Active system power mode) and it handles the rest of the current transfer. In this case the I2C master will not observe the NACK. 2). the internally clocked logic is not enabled (we are in DeepSleep system power mode). In this case the I2C master will observe the NACK and may retry the transfer in the future (which gives the internally clocked logic the time to wake up from DeepSleep system power mode). - 0: clock stretching is performed (till the internally clocked logic takes over). The internally clocked logic will handle the ongoing transfer as soon as it is enabled. Default Value: 1
13	S_READY_DATA_ACK	When '1', a received data element by the slave is immediately ACK'd when the receiver FIFO is not full. In EZ mode, this field should be set to '1'. Default Value: 1
12	S_READY_ADDR_ACK	When '1', a received (matching) slave address is immediately ACK'd when the receiver FIFO is not full. In EZ mode, this field should be set to '1'. Default Value: 1
11	S_GENERAL_IGNORE	When '1', a received general call slave address is immediately NACK'd (no ACK or clock stretching) and treated as a non matching slave address. This is useful for slaves that do not need any data supplied within the general call structure. Default Value: 1
9	M_NOT_READY_DATA_NACK	When '1', a received data element byte the master is immediately NACK'd when the receiver FIFO is full. When '0', clock stretching is used instead (till the receiver FIFO is no longer full). Default Value: 1
8	M_READY_DATA_ACK	When '1', a received data element by the master is immediately ACK'd when the receiver FIFO is not full. Default Value: 1
7 : 4	LOW_PHASE_OVS	Serial I2C interface low phase oversampling factor. LOW_PHASE_OVS + 1 peripheral clock periods constitute the low phase of a bit period. The valid range is [7, 15] with input signal median filtering and [6, 15] without input signal median filtering. The field is only used in master mode. In slave mode, the field is NOT used. However, there is a frequency requirement for the IP clock wrt. the regular (no stretching) interface (IF) low time to guarantee functional correct behavior. With input signal median filtering, the IF low time should be >= 8 IP clock cycles and <= 16 IP clock cycles. Without input signal median filtering, the IF low time should be >= 7 IP clock cycles and <= 16 IP clock cycles. Default Value: 8

(continued)

3 : 0	HIGH_PHASE_OVS	Serial I2C interface high phase oversampling factor. HIGH_PHASE_OVS + 1 peripheral clock periods constitute the high phase of a bit period. The valid range is [5, 15] with input signal median filtering and [4, 15] without input signal median filtering. The field is only used in master mode. In slave mode, the field is NOT used. However, there is a frequency requirement for the IP clock wrt. the regular interface (IF) high time to guarantee functional correct behavior. With input signal median filtering, the IF high time should be >= 6 IP clock cycles and <= 16 IP clock cycles. Without input signal median filtering, the IF high time should be >= 5 IP clock cycles and <= 16 IP clock cycles. Default Value: 8

28.1.90 SCB1_I2C_STATUS

I2C status register.

Address: 0x40250064

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R	R	None		R	R
HW Access	None		W	W	None		W	W
Name	None [7:6]		M_READ	S_READ	None [3:2]		I2C_EC_BUSY	BUS_BUSY

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	CURR_EZ_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	BASE_EZ_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	BASE_EZ_ADDR	I2C slave base EZ address. Address as provided by an I2C write transfer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable, as clock domain synchronization is not performed in the design. Default Value: Undefined
15 : 8	CURR_EZ_ADDR	I2C slave current EZ address. Current address pointer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable (during an ongoing transfer when I2C_EC_BUSY is '1'), as clock domain synchronization is not performed in the design. Default Value: Undefined
5	M_READ	I2C master read transfer ('1') or I2C master write transfer ('0'). When the I2C master is inactive/idle or transmitting START, REPEATED START, STOP or an address, this field is '0''. Default Value: 0
4	S_READ	I2C slave read transfer ('1') or I2C slave write transfer ('0'). When the I2C slave is inactive/idle or receiving START, REPEATED START, STOP or an address, this field is '0''. Default Value: 0

(continued)

1	I2C_EC_BUSY	Inidicates whether the externally clocked logic is potentially accessing the EZ memory and/or updating BASE_ADDR or CURR_ADDR (this is only possible in EZ mode). This bit can be used by SW to determine whether BASE_ADDR and CURR_ADDR are reliable. Default Value: Undefined
0	BUS_BUSY	I2C bus is busy. The bus is considered busy ('1'), from the time a START is detected or from the time the SCL line is '0'. The bus is considered idle ('0'), from the time a STOP is detected. If the IP is disabled, BUS_BUSY is '0'. After enabling the IP, it takes time for the BUS_BUSY to detect a busy bus. This time is the maximum high time of the SCL line. For a 100 kHz interface frequency, this maximum high time may last roughly 5 us (half a bit period). For single master systems, BUS_BUSY does not have to be used to detect an idle bus before a master starts a transfer using I2C_M_CMD.M_START (no bus collisions). For multi-master systems, BUS_BUSY can be used to detect an idle bus before a master starts a transfer using I2C_M_CMD.M_START_ON_IDLE (to prevent bus collisions). Default Value: 0

28.1.91 SCB1_I2C_M_CMD

I2C master command register.

Address: 0x40250068

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			RW1C	RW1C	RW1C	RW1C	RW1C
Name	None [7:5]			M_STOP	M_NACK	M_ACK	M_START_ON_IDLE	M_START

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4	M_STOP	When '1', attempt to transmit a STOP. When this action is performed, the hardware sets this field to '0'. This command has a higher priority than I2C_M_CMD.M_START: in situations where both a STOP and a REPEATED START could be transmitted, M_STOP takes precedence over M_START. Default Value: 0
3	M_NACK	When '1', attempt to transmit a negative acknowledgement (NACK). When this action is performed, the hardware sets this field to '0'. Default Value: 0
2	M_ACK	When '1', attempt to transmit an acknowledgement (ACK). When this action is performed, the hardware sets this field to '0'. Default Value: 0
1	M_START_ON_IDLE	When '1', transmit a START as soon as the bus is idle (I2C_STATUS.BUS_BUSY is '0', note that BUSY has a default value of '0'). For bus idle detection the hardware relies on STOP detection. As a result, bus idle detection is only functional after at least one I2C bus transfer has been detected on the bus (default/reset value of BUSY is '0') . A START is only transmitted when the master state machine is in the default state. When this action is performed, the hardware sets this field to '0'. Default Value: 0

(continued)

0	M_START	When '1', transmit a START or REPEATED START. Whether a START or REPEATED START is transmitted depends on the state of the master state machine. A START is only transmitted when the master state machine is in the default state. A REPEATED START is transmitted when the master state machine is not in the default state, but is working on an ongoing transaction. The REPEATED START can only be transmitted after a NACK or ACK has been received for a transmitted data element or after a NACK has been transmitted for a received data element. When this action is performed, the hardware sets this field to '0'. Default Value: 0

28.1.92 SCB1_I2C_S_CMD

I2C slave command register.

Address: 0x4025006C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						RW1C	RW1C
Name	None [7:2]						S_NACK	S_ACK

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	S_NACK	When '1', attempt to transmit a negative acknowledgement (NACK). When this action is performed, the hardware sets this field to '0'. In EZ mode, this field should be set to '0' (it is only to be used in non EZ mode). This command has a higher priority than I2C_S_CMD.S_ACK, I2C_CTRL.S_READY_ADDR_ACK or I2C_CTRL.S_READY_DATA_ACK. Default Value: 0
0	S_ACK	When '1', attempt to transmit an acknowledgement (ACK). When this action is performed, the hardware sets this field to '0'. In EZ mode, this field should be set to '0' (it is only to be used in non EZ mode). Default Value: 0

28.1.93 SCB1_I2C_CFG

I2C configuration register.

Address: 0x40250070

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	None		RW	
HW Access	None			R	None		R	
Name	None [7:5]			SDA_IN_FILT_SEL	None [3:2]		SDA_IN_FILT_TRIM [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	None		RW	
HW Access	None			R	None		R	
Name	None [15:13]			SCL_IN_FILT_SEL	None [11:10]		SCL_IN_FILT_TRIM [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW		RW		RW	
HW Access	None		R		R		R	
Name	None [23:22]		SDA_OUT_FILT2_TRIM [21:20]		SDA_OUT_FILT1_TRIM [19:18]		SDA_OUT_FILT0_TRIM [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None		RW		None			
HW Access	None		R		None			
Name	None [31:30]		SDA_OUT_FILT_SEL [29:28]		None [27:24]			

Bits	Name	Description
29 : 28	SDA_OUT_FILT_SEL	Selection of cumulative "i2c_sda_out" filter delay: "0": 0 ns. "1": 50 ns (filter 0 enabled). "2": 100 ns (filters 0 and 1 enabled). "3": 150 ns (filters 0, 1 and 2 enabled). Default Value: 0
21 : 20	SDA_OUT_FILT2_TRIM	Trim bits for "i2c_sda_out" 50 ns filter 2. See s8i2cs BROS (001-59539) for more details on the trim bit values. Default Value: 2
19 : 18	SDA_OUT_FILT1_TRIM	Trim bits for "i2c_sda_out" 50 ns filter 1. See s8i2cs BROS (001-59539) for more details on the trim bit values. Default Value: 2
17 : 16	SDA_OUT_FILT0_TRIM	Trim bits for "i2c_sda_out" 50 ns filter 0. See s8i2cs BROS (001-59539) for more details on the trim bit values. Default Value: 2

(continued)

12	SCL_IN_FILT_SEL	Selection of "i2c_scl_in" filter delay: '0': 0 ns. '1: 50 ns (filter enabled). Default Value: 1
9 : 8	SCL_IN_FILT_TRIM	Trim bits for "i2c_scl_in" 50 ns filter. See s8i2cs BROS (001-59539) for more details on the trim bit values. Default Value: 0
4	SDA_IN_FILT_SEL	Selection of "i2c_sda_in" filter delay: '0': 0 ns. '1: 50 ns (filter enabled). Default Value: 1
1 : 0	SDA_IN_FILT_TRIM	Trim bits for "i2c_sda_in" 50 ns filter. See s8i2cs BROS (001-59539) for more details on the trim bit values. Default Value: 3

28.1.94 SCB1_TX_CTRL

Transmitter control register.

Address: 0x40250200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				DATA_WIDTH [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							MSB_FIRST

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	MSB_FIRST	Least significant bit first ('0') or most significant bit first ('1'). For I2C, this field should be '1'. Default Value: 1
3 : 0	DATA_WIDTH	Dataframe width. DATA_WIDTH + 1 is the amount of bits in a transmitted data frame. This number does not include start, parity and stop bits. For UART mode, the valid range is [3, 8]. For SPI, the valid range is [3, 15]. For I2C the only valid value is 7. Default Value: 7

28.1.95 SCB1_TX_FIFO_CTRL

Transmitter FIFO control register.

Address: 0x40250204

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				TRIGGER_LEVEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [23:18]						FREEZE	CLEAR

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
17	FREEZE	When '1', hardware reads from the transmitter FIFO do not remove FIFO entries. Freeze will not advance the TX FIFO read pointer. Default Value: 0
16	CLEAR	When '1', the transmitter FIFO and transmitter shift register are cleared/invalidated. Invalidation will last for as long as this field is '1'. If a quick clear/invalidation is required, the field should be set to '1' and be followed by a set to '0'. If a clear/invalidation is required for an extended time period, the field should be set to '1' during the complete time period. Default Value: 0
3 : 0	TRIGGER_LEVEL	Trigger level. When the transmitter FIFO has less entries than the number of this field, a transmitter trigger event is generated. Default Value: 0

28.1.96 SCB1_TX_FIFO_STATUS

Transmitter FIFO status register.

Address: 0x40250208

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R			
HW Access	None				W			
Name	None [7:5]				USED [4:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	R	None						
HW Access	W	None						
Name	SR_VALID	None [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	None				R			
HW Access	None				W			
Name	None [23:20]				RD_PTR [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None				R			
HW Access	None				W			
Name	None [31:28]				WR_PTR [27:24]			

Bits	Name	Description
27 : 24	WR_PTR	FIFO write pointer: FIFO location at which a new data frame is written. Default Value: 0
19 : 16	RD_PTR	FIFO read pointer: FIFO location from which a data frame is read by the hardware. Default Value: 0
15	SR_VALID	Indicates whether the TX shift registers holds a valid data frame ('1') or not ('0'). The shift register can be considered the top of the TX FIFO (the data frame is not included in the USED field of the TX FIFO). The shift register is a working register and holds the data frame that is currently transmitted (when the protocol state machine is transmitting a data frame) or the data frame that is tranmitted next (when the protocol state machine is not transmitting a data frame). Default Value: 0
4 : 0	USED	Amount of enties in the transmitter FIFO. The value of this field ranges from 0 to FF_DATA_NR. Default Value: 0

28.1.97 SCB1_TX_FIFO_WR

Transmitter FIFO write register.

Address: 0x40250240

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATA	Data frame written into the transmitter FIFO. Behavior is similar to that of a PUSH operation. Note that when CTRL.BYTE_MODE is '1', only DATA[7:0] are used. A write to a full TX FIFO sets INTR_TX.OVERFLOW to '1'. Default Value: 0

28.1.98 SCB1_RX_CTRL

Receiver control register.

Address: 0x40250300

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				DATA_WIDTH [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [15:10]						MEDIAN	MSB_FIRST

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	MEDIAN	Median filter. When '1', a digital 3 taps median filter is performed on input interface lines. This filter should reduce the susceptability to errors. However, its requires higher oversampling values. For UART IrDA submode, this field should always be '1'. Default Value: 0
8	MSB_FIRST	Least significant bit first ('0') or most significant bit first ('1'). For I2C, this field should be '1'. Default Value: 1
3 : 0	DATA_WIDTH	Dataframe width. DATA_WIDTH + 1 is the expected amount of bits in received data frame. This number does not include start, parity and stop bits. For UART mode, the valid range is [3, 8]. For SPI, the valid range is [3, 15]. For I2C the only valid value is 7. In EZ mode (for both SPI and I2C), the only valid value is 7. Default Value: 7

28.1.99 SCB1_RX_FIFO_CTRL

Receiver FIFO control register.

Address: 0x40250304

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				TRIGGER_LEVEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [23:18]						FREEZE	CLEAR

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
17	FREEZE	When '1', hardware writes to the receiver FIFO have no effect. Freeze will not advance the RX FIFO write pointer. Default Value: 0
16	CLEAR	When '1', the receiver FIFO and receiver shift register are cleared/invalidated. Invalidation will last for as long as this field is '1'. If a quick clear/invalidation is required, the field should be set to '1' and be followed by a set to '0'. If a clear/invalidation is required for an extended time period, the field should be set to '1' during the complete time period. Default Value: 0
3 : 0	TRIGGER_LEVEL	Trigger level. When the receiver FIFO has more entries than the number of this field, a receiver trigger event is generated. Default Value: 0

28.1.100 SCB1_RX_FIFO_STATUS

Receiver FIFO status register.

Address: 0x40250308

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R			
HW Access	None				W			
Name	None [7:5]				USED [4:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	R	None						
HW Access	W	None						
Name	SR_VALID	None [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	None				R			
HW Access	None				W			
Name	None [23:20]				RD_PTR [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None				R			
HW Access	None				W			
Name	None [31:28]				WR_PTR [27:24]			

Bits	Name	Description
27 : 24	WR_PTR	FIFO write pointer: FIFO location at which a new data frame is written by the hardware. Default Value: 0
19 : 16	RD_PTR	FIFO read pointer: FIFO location from which a data frame is read. Default Value: 0
15	SR_VALID	Indicates whether the RX shift registers holds a (partial) valid data frame ('1') or not ('0'). The shift register can be considered the bottom of the RX FIFO (the data frame is not included in the USED field of the RX FIFO). The shift register is a working register and holds the data frame that is currently being received (when the protocol state machine is receiving a data frame). Default Value: 0
4 : 0	USED	Amount of enties in the receiver FIFO. The value of this field ranges from 0 to FF_DATA_NR. Default Value: 0

28.1.101 SCB1_RX_MATCH

Slave address and mask register.

Address: 0x40250310

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	MASK [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	MASK	Slave device address mask. This field is a mask that specifies which of the ADDR field bits in the ADDR field take part in the matching of the slave address: MATCH = ((ADDR & MASK) == ("slave address" & MASK)). Default Value: 0
7 : 0	ADDR	Slave device address. In UART multi-processor mode, all 8 bits are used. In I2C slave mode, only bits 7 down to 1 are used. This reflects the organization of the first transmitted byte in a I2C transfer: the first 7 bits represent the address of the addressed slave, and the last 1 bit is a read/write indicator ('0': write, '1': read). Default Value: 0

28.1.102 SCB1_RX_FIFO_RD

Receiver FIFO read register.

Address: 0x40250340

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATA	Data read from the receiver FIFO. Reading a data frame will remove the data frame from the FIFO; i.e. behavior is similar to that of a POP operation. Note that when CTRL.BYTE_MODE is '1', only DATA[7:0] are used. This register has a side effect when read by software: a data frame is removed from the FIFO. This may be undesirable during debug; i.e. a read during debug should NOT have a side effect. To this end, the IP uses the AHB-Lite "hmaster[0]" input signal. When this signal is '1' in the address cycle of a bus transfer, a read transfer will not have a side effect. As a result, a read from this register will not remove a data frame from the FIFO. As a result, a read from this register behaves as a read from the SCB_RX_FIFO_RD_SILENT register. A read from an empty RX FIFO sets INTR_RX.UNDERFLOW to '1'. Default Value: Undefined

28.1.103 SCB1_RX_FIFO_RD_SILENT

Receiver FIFO read register.

Address: 0x40250344

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DATA	Data read from the receiver FIFO. Reading a data frame will NOT remove the data frame from the FIFO; i.e. behavior is similar to that of a PEEK operation. Note that when CTRL.BYTE_MODE is '1', only DATA[7:0] are used. A read from an empty RX FIFO sets INTR_RX.UNDERFLOW to '1'. Default Value: Undefined

28.1.104 SCB1_EZ_DATA0

Memory buffer registers.

Address: 0x40250400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

28.1.105 SCB1_EZ_DATA1

Memory buffer registers.

Address: 0x40250404

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

28.1.106 SCB1_EZ_DATA2

Memory buffer registers.

Address: 0x40250408

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

28.1.107 SCB1_EZ_DATA3

Memory buffer registers.

Address: 0x4025040C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

28.1.108 SCB1_EZ_DATA4

Memory buffer registers.

Address: 0x40250410

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

28.1.109 SCB1_EZ_DATA5

Memory buffer registers.

Address: 0x40250414

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

28.1.110 SCB1_EZ_DATA6

Memory buffer registers.

Address: 0x40250418

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

28.1.111 SCB1_EZ_DATA7

Memory buffer registers.

Address: 0x4025041C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

28.1.112 SCB1_EZ_DATA8

Memory buffer registers.

Address: 0x40250420

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

28.1.113 SCB1_EZ_DATA9

Memory buffer registers.

Address: 0x40250424

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

28.1.114 SCB1_EZ_DATA10

Memory buffer registers.

Address: 0x40250428

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

28.1.115 SCB1_EZ_DATA11

Memory buffer registers.

Address: 0x4025042C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

28.1.116 SCB1_EZ_DATA12

Memory buffer registers.

Address: 0x40250430

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

28.1.117 SCB1_EZ_DATA13

Memory buffer registers.

Address: 0x40250434

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

28.1.118 SCB1_EZ_DATA14

Memory buffer registers.

Address: 0x40250438

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

28.1.119 SCB1_EZ_DATA15

Memory buffer registers.

Address: 0x4025043C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

28.1.120 SCB1_EZ_DATA16

Memory buffer registers.

Address: 0x40250440

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

28.1.121 SCB1_EZ_DATA17

Memory buffer registers.

Address: 0x40250444

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

28.1.122 SCB1_EZ_DATA18

Memory buffer registers.

Address: 0x40250448

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

28.1.123 SCB1_EZ_DATA19

Memory buffer registers.

Address: 0x4025044C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

28.1.124 SCB1_EZ_DATA20

Memory buffer registers.

Address: 0x40250450

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

28.1.125 SCB1_EZ_DATA21

Memory buffer registers.

Address: 0x40250454

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

28.1.126 SCB1_EZ_DATA22

Memory buffer registers.

Address: 0x40250458

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

28.1.127 SCB1_EZ_DATA23

Memory buffer registers.

Address: 0x4025045C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

28.1.128 SCB1_EZ_DATA24

Memory buffer registers.

Address: 0x40250460

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

28.1.129 SCB1_EZ_DATA25

Memory buffer registers.

Address: 0x40250464

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

28.1.130 SCB1_EZ_DATA26

Memory buffer registers.

Address: 0x40250468

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

28.1.131 SCB1_EZ_DATA27

Memory buffer registers.

Address: 0x4025046C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

28.1.132 SCB1_EZ_DATA28

Memory buffer registers.

Address: 0x40250470

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

28.1.133 SCB1_EZ_DATA29

Memory buffer registers.

Address: 0x40250474

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

28.1.134 SCB1_EZ_DATA30

Memory buffer registers.

Address: 0x40250478

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

28.1.135 SCB1_EZ_DATA31

Memory buffer registers.

Address: 0x4025047C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

28.1.136 SCB1_INTR_CAUSE

Active clocked interrupt signal register

Address: 0x40250E00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R	R	R	R	R	R
HW Access	None		W	W	W	W	W	W
Name	None [7:6]		SPI_EC	I2C_EC	RX	TX	S	M

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	SPI_EC	Externally clocked SPI interrupt active ("interrupt_spi_ec"): INTR_SPI_EC_MASKED != 0. Default Value: 0
4	I2C_EC	Externally clock I2C interrupt active ("interrupt_i2c_ec"): INTR_I2C_EC_MASKED != 0. Default Value: 0
3	RX	Receiver interrupt active ("interrupt_rx"): INTR_RX_MASKED != 0. Default Value: 0
2	TX	Transmitter interrupt active ("interrupt_tx"): INTR_TX_MASKED != 0. Default Value: 0
1	S	Slave interrupt active ("interrupt_slave"): INTR_S_MASKED != 0. Default Value: 0
0	M	Master interrupt active ("interrupt_master"): INTR_M_MASKED != 0. Default Value: 0

28.1.137 SCB1_INTR_I2C_EC

Externally clocked I2C interrupt request register

Address: 0x40250E80

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1C	RW1C	RW1C	RW1C
HW Access	None				A	A	A	A
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	STOP detection after a read transfer occurred. Activated on the end of a read transfer (I2C STOP). This event is an indication that a buffer memory location has been read from. Only available for a slave request with an address match, in EZ and CMD_RESP modes, when EC_OP is '1'. Default Value: 0
2	EZ_WRITE_STOP	STOP detection after a write transfer occurred. Activated on the end of a write transfer (I2C STOP). This event is an indication that a buffer memory location has been written to. For EZ mode: a transfer that only writes the base address does NOT activate this event. Only available for a slave request with an address match, in EZ and CMD_RESP modes, when EC_OP is '1'. Default Value: 0
1	EZ_STOP	STOP detection. Activated on the end of a every transfer (I2C STOP). Only available for a slave request with an address match, in EZ and CMD_RESP modes, when EC_OP is '1'. Default Value: 0

(continued)

0	WAKE_UP	Wake up request. Active on incoming slave request (with address match). Only used when EC_AM is '1'. Default Value: 0

28.1.138 SCB1_INTR_I2C_EC_MASK

Externally clocked I2C interrupt mask register

Address: 0x40250E88

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	EZ_WRITE_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	EZ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	WAKE_UP	Mask bit for corresponding bit in interrupt request register. Default Value: 0

28.1.139 SCB1_INTR_I2C_EC_MASKED

Externally clocked I2C interrupt masked register

Address: 0x40250E8C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R	R	R	R
HW Access	None				W	W	W	W
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
2	EZ_WRITE_STOP	Logical and of corresponding request and mask bits. Default Value: 0
1	EZ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
0	WAKE_UP	Logical and of corresponding request and mask bits. Default Value: 0

28.1.140 SCB1_INTR_SPI_EC

Externally clocked SPI interrupt request register

Address: 0x40250EC0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1C	RW1C	RW1C	RW1C
HW Access	None				A	A	A	A
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	STOP detection after a read transfer occurred. Activated on the end of a read transfer (SPI de-selection). This event is an indication that a buffer memory location has been read from. Only used in EZ and CMD_RESP modes and when EC_OP is '1'. Default Value: 0
2	EZ_WRITE_STOP	STOP detection after a write transfer occurred. Activated on the end of a write transfer (SPI de-selection). This event is an indication that a buffer memory location has been written to. For EZ mode: a transfer that only writes the base address does NOT activate this event. Only used in EZ and CMD_RESP modes and when EC_OP is '1'. Default Value: 0
1	EZ_STOP	STOP detection. Activated on the end of a every transfer (SPI deselection). Only available in EZ and CMD_RESP mode and when EC_OP is '1'. Default Value: 0

(continued)

0	WAKE_UP	Wake up request. Active on incoming slave request when externally clocked selection is '1'. Only used when EC_AM is '1'. Default Value: 0

28.1.141 SCB1_INTR_SPI_EC_MASK

Externally clocked SPI interrupt mask register

Address: 0x40250EC8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	EZ_WRITE_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	EZ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	WAKE_UP	Mask bit for corresponding bit in interrupt request register. Default Value: 0

28.1.142 SCB1_INTR_SPI_EC_MASKED

Externally clocked SPI interrupt masked register

Address: 0x40250ECC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R	R	R	R
HW Access	None				W	W	W	W
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
2	EZ_WRITE_STOP	Logical and of corresponding request and mask bits. Default Value: 0
1	EZ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
0	WAKE_UP	Logical and of corresponding request and mask bits. Default Value: 0

28.1.143 SCB1_INTR_M

Master interrupt request register.

Address: 0x40250F00

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW1C	None	RW1C	RW1C	RW1C
HW Access	None			RW1S	None	RW1S	RW1S	RW1S
Name	None [7:5]			I2C_STOP	None	I2C_ACK	I2C_NACK	I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW1C	RW1C
HW Access	None						RW1S	RW1S
Name	None [15:10]						SPI_DONE	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	SPI_DONE	SPI master transfer done event: all data frames in the transmit FIFO are sent and the transmit FIFO is empty. Default Value: 0
8	I2C_BUS_ERROR	I2C master bus error (unexpected detection of START or STOP condition). Default Value: 0
4	I2C_STOP	I2C master STOP. Set to '1', when the master has transmitted a STOP. Default Value: 0
2	I2C_ACK	I2C master acknowledgement. Set to '1', when the master receives a ACK (typically after the master transmitted the slave address or TX data). Default Value: 0
1	I2C_NACK	I2C master negative acknowledgement. Set to '1', when the master receives a NACK (typically after the master transmitted the slave address or TX data). Default Value: 0

(continued)

0	I2C_ARB_LOST	I2C master lost arbitration: the value driven by the master on the SDA line is not the same as the value observed on the SDA line. Default Value: 0

28.1.144 SCB1_INTR_M_SET

Master interrupt set request register

Address: 0x40250F04

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW1S	None	RW1S	RW1S	RW1S
HW Access	None			A	None	A	A	A
Name	None [7:5]			I2C_STOP	None	I2C_ACK	I2C_NACK	I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW1S	RW1S
HW Access	None						A	A
Name	None [15:10]						SPI_DONE	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	SPI_DONE	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
8	I2C_BUS_ERROR	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
4	I2C_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
2	I2C_ACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
1	I2C_NACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	I2C_ARB_LOST	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

28.1.145 SCB1_INTR_M_MASK

Master interrupt mask register.

Address: 0x40250F08

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	None	RW	RW	RW
HW Access	None			R	None	R	R	R
Name	None [7:5]			I2C_STOP	None	I2C_ACK	I2C_NACK	I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [15:10]						SPI_DONE	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	SPI_DONE	Mask bit for corresponding bit in interrupt request register. Default Value: 0
8	I2C_BUS_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
4	I2C_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	I2C_ACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	I2C_NACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	I2C_ARB_LOST	Mask bit for corresponding bit in interrupt request register. Default Value: 0

28.1.146 SCB1_INTR_M_MASKED

Master interrupt masked request register

Address: 0x40250F0C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			R	None	R	R	R
HW Access	None			W	None	W	W	W
Name	None [7:5]			I2C_STOP	None	I2C_ACK	I2C_NACK	I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None						R	R
HW Access	None						W	W
Name	None [15:10]						SPI_DONE	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	SPI_DONE	Logical and of corresponding request and mask bits. Default Value: 0
8	I2C_BUS_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
4	I2C_STOP	Logical and of corresponding request and mask bits. Default Value: 0
2	I2C_ACK	Logical and of corresponding request and mask bits. Default Value: 0
1	I2C_NACK	Logical and of corresponding request and mask bits. Default Value: 0
0	I2C_ARB_LOST	Logical and of corresponding request and mask bits. Default Value: 0

28.1.147 SCB1_INTR_S

Slave interrupt request register.

Address: 0x40250F40

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
Name	I2C_GENERAL	I2C_ADDR_MATCH	I2C_START	I2C_STOP	I2C_WRITE_STOP	I2C_ACK	I2C_NACK	I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW1C	RW1C	RW1C	RW1C
HW Access	None				RW1S	RW1S	RW1S	RW1S
Name	None [15:12]				SPI_BUS_ERROR	SPI_EZ_STOP	SPI_EZ_WRITE_STOP	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	SPI_BUS_ERROR	SPI slave deselected at an unexpected time in the SPI transfer. The Firmware may decide to clear the TX and RX FIFOs in case of this error. Default Value: 0
10	SPI_EZ_STOP	SPI slave deselected after any EZ SPI transfer occurred. Default Value: 0
9	SPI_EZ_WRITE_STOP	SPI slave deselected after a write EZ SPI transfer occurred. Default Value: 0
8	I2C_BUS_ERROR	I2C slave bus error (unexpected detection of START or STOP condition). This should not occur, it represents erroneous I2C bus behavior. In case of a bus error, the I2C slave state machine abort the ongoing transfer. The Firmware may decide to clear the TX and RX FIFOs in case of this error. Default Value: 0

(continued)

7	I2C_GENERAL	I2C slave general call address received. If CTRL.ADDR_ACCEPT, the received address 0x00 (including the R/W bit) is available in the RX FIFO. In the case of externally clocked address matching (CTRL.EC_AM_MODE is '1') and internally clocked operation (CTRL.EC_OP_MODE is '0'), this field is set when the event is detected. Default Value: 0
6	I2C_ADDR_MATCH	I2C slave matching address received. If CTRL.ADDR_ACCEPT, the received address (including the R/W bit) is available in the RX FIFO. In the case of externally clocked address matching (CTRL.EC_AM_MODE is '1') and internally clocked operation (CTRL.EC_OP_MODE is '0'), this field is set when the event is detected. Default Value: 0
5	I2C_START	I2C slave START received. Set to '1', when START or REPEATED START event is detected. In the case of externally clocked address matching (CTRL.EC_AM_MODE is '1') AND clock stretching is performed (till the internally clocked logic takes over) (I2C_CTRL.S_NOT_READY_ADDR_NACK is '0'), this field is NOT set. The Firmware should use INTR_S_EC.WAKE_UP, INTR_S.I2C_ADDR_MATCH and INTR_S.I2C_GENERAL. Default Value: 0
4	I2C_STOP	I2C STOP event for I2C (read or write) transfer intended for this slave (address matching is performed). Set to '1', when STOP or REPEATED START event is detected. The REPEATED START event is included in this interrupt cause such that the I2C transfers separated by a REPEATED START can be distinguished and potentially treated separately by the Firmware. Note that the second I2C transfer (after a REPEATED START) may be to a different slave address. The event is detected on any I2C transfer intended for this slave. Note that a I2C address intended for the slave (address is matching) will result in a I2C_STOP event independent of whether the I2C address is ACK'd or NACK'd. Default Value: 0
3	I2C_WRITE_STOP	I2C STOP event for I2C write transfer intended for this slave (address matching is performed). Set to '1', when STOP or REPEATED START event is detected. The REPEATED START event is included in this interrupt cause such that the I2C transfers separated by a REPEATED START can be distinguished and potentially treated separately by the Firmware. Note that the second I2C transfer (after a REPEATED START) may be to a different slave address. In non EZ mode, the event is detected on any I2C write transfer intended for this slave. Note that a I2C write address intended for the slave (address is matching and a it is a write transfer) will result in a I2C_WRITE_STOP event independent of whether the I2C address is ACK'd or NACK'd. In EZ mode, the event is detected only on I2C write transfers that have EZ data written to the memory structure (an I2C write transfer that only communicates an I2C address and EZ address, will not result in this event being detected). Default Value: 0
2	I2C_ACK	I2C slave acknowledgement received. Set to '1', when the slave receives a ACK (typically after the slave transmitted TX data). Default Value: 0
1	I2C_NACK	I2C slave negative acknowledgement received. Set to '1', when the slave receives a NACK (typically after the slave transmitted TX data). Default Value: 0
0	I2C_ARB_LOST	I2C slave lost arbitration: the value driven on the SDA line is not the same as the value observed on the SDA line (while the SCL line is '1'). This should not occur, it represents erroneous I2C bus behavior. In case of lost arbitration, the I2C slave state machine abort the ongoing transfer. The Firmware may decide to clear the TX and RX FIFOs in case of this error. Default Value: 0

28.1.148 SCB1_INTR_S_SET

Slave interrupt set request register.

Address: 0x40250F44

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	A	A	A	A	A	A	A	A
Name	I2C_GENERAL	I2C_ADDR_MATCH	I2C_START	I2C_STOP	I2C_WRITE_STOP	I2C_ACK	I2C_NACK	I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW1S	RW1S	RW1S	RW1S
HW Access	None				A	A	A	A
Name	None [15:12]				SPI_BUS_ERROR	SPI_EZ_STOP	SPI_EZ_WRITE_STOP	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	SPI_BUS_ERROR	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
10	SPI_EZ_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
9	SPI_EZ_WRITE_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
8	I2C_BUS_ERROR	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
7	I2C_GENERAL	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
6	I2C_ADDR_MATCH	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
5	I2C_START	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

(continued)

4	I2C_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
3	I2C_WRITE_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
2	I2C_ACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
1	I2C_NACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	I2C_ARB_LOST	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

28.1.149 SCB1_INTR_S_MASK

Slave interrupt mask register.

Address: 0x40250F48

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	I2C_GENERAL	I2C_ADDR_MATCH	I2C_START	I2C_STOP	I2C_WRITE_STOP	I2C_ACK	I2C_NACK	I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [15:12]				SPI_BUS_ERROR	SPI_EZ_STOP	SPI_EZ_WRITE_STOP	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	SPI_BUS_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
10	SPI_EZ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
9	SPI_EZ_WRITE_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
8	I2C_BUS_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
7	I2C_GENERAL	Mask bit for corresponding bit in interrupt request register. Default Value: 0
6	I2C_ADDR_MATCH	Mask bit for corresponding bit in interrupt request register. Default Value: 0
5	I2C_START	Mask bit for corresponding bit in interrupt request register. Default Value: 0

(continued)

4	I2C_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
3	I2C_WRITE_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	I2C_ACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	I2C_NACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	I2C_ARB_LOST	Mask bit for corresponding bit in interrupt request register. Default Value: 0

28.1.150 SCB1_INTR_S_MASKED

Slave interrupt masked request register

Address: 0x40250F4C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	I2C_GENERAL	I2C_ADDR_MATCH	I2C_START	I2C_STOP	I2C_WRITE_STOP	I2C_ACK	I2C_NACK	I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None				R	R	R	R
HW Access	None				W	W	W	W
Name	None [15:12]				SPI_BUS_ERROR	SPI_EZ_STOP	SPI_EZ_WRITE_STOP	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	SPI_BUS_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
10	SPI_EZ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
9	SPI_EZ_WRITE_STOP	Logical and of corresponding request and mask bits. Default Value: 0
8	I2C_BUS_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
7	I2C_GENERAL	Logical and of corresponding request and mask bits. Default Value: 0
6	I2C_ADDR_MATCH	Logical and of corresponding request and mask bits. Default Value: 0
5	I2C_START	Logical and of corresponding request and mask bits. Default Value: 0

(continued)

4	I2C_STOP	Logical and of corresponding request and mask bits. Default Value: 0
3	I2C_WRITE_STOP	Logical and of corresponding request and mask bits. Default Value: 0
2	I2C_ACK	Logical and of corresponding request and mask bits. Default Value: 0
1	I2C_NACK	Logical and of corresponding request and mask bits. Default Value: 0
0	I2C_ARB_LOST	Logical and of corresponding request and mask bits. Default Value: 0

28.1.151 SCB1_INTR_TX

Transmitter interrupt request register.

Address: 0x40250F80

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	None		RW1C	RW1C
HW Access	RW1S	RW1S	RW1S	RW1S	None		RW1S	RW1S
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	EMPTY	None [3:2]		NOT_FULL	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW1C	RW1C	RW1C
HW Access	None					RW1S	RW1S	RW1S
Name	None [15:11]					UART_ARB_LOST	UART_DONE	UART_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10	UART_ARB_LOST	UART lost arbitration: the value driven on the TX line is not the same as the value observed on the RX line. This condition event is usefull when transmitter and receiver share a TX/RX line. This is the case in LIN or SmartCard modes. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
9	UART_DONE	UART transmitter done event. This happens when the IP is done transferring all data in the TX FIFO; i.e. EMPTY is '1'. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
8	UART_NACK	UART transmitter received a negative acknowledgement in SmartCard mode. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
7	BLOCKED	AHB-Lite write transfer can not get access to the EZ memory (EZ data access), due to an externally clocked EZ access. This may happen when STATUS.EC_BUSY is '1'. Default Value: 0

(continued)

6	UNDERFLOW	Attempt to read from an empty TX FIFO. This happens when the IP is ready to transfer data and EMPTY is '1'. Only used in FIFO mode. Default Value: 0
5	OVERFLOW	Attempt to write to a full TX FIFO. Only used in FIFO mode. Default Value: 0
4	EMPTY	TX FIFO is empty; i.e. it has 0 entries. Only used in FIFO mode. Default Value: 0
1	NOT_FULL	TX FIFO is not full. Dependent on CTRL.BYTE_MODE: BYTE_MODE is '0': # entries != FF_DATA_NR/2. BYTE_MODE is '1': # entries != FF_DATA_NR. Only used in FIFO mode. Default Value: 0
0	TRIGGER	Less entries in the TX FIFO than the value specified by TX_FIFO_CTRL. Only used in FIFO mode. Default Value: 0

28.1.152 SCB1_INTR_TX_SET

Transmitter interrupt set request register

Address: 0x40250F84

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	RW1S	None		RW1S	RW1S
HW Access	A	A	A	A	None		A	A
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	EMPTY	None [3:2]		NOT_FULL	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW1S	RW1S	RW1S
HW Access	None					A	A	A
Name	None [15:11]					UART_ARB_LOST	UART_DONE	UART_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10	UART_ARB_LOST	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
9	UART_DONE	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
8	UART_NACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
7	BLOCKED	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
6	UNDERFLOW	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
5	OVERFLOW	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
4	EMPTY	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

(continued)

1	NOT_FULL	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	TRIGGER	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

28.1.153 SCB1_INTR_TX_MASK

Transmitter interrupt mask register.

Address: 0x40250F88

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	None		RW	RW
HW Access	R	R	R	R	None		R	R
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	EMPTY	None [3:2]		NOT_FULL	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [15:11]					UART_ARB_LOST	UART_DONE	UART_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10	UART_ARB_LOST	Mask bit for corresponding bit in interrupt request register. Default Value: 0
9	UART_DONE	Mask bit for corresponding bit in interrupt request register. Default Value: 0
8	UART_NACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
7	BLOCKED	Mask bit for corresponding bit in interrupt request register. Default Value: 0
6	UNDERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
5	OVERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
4	EMPTY	Mask bit for corresponding bit in interrupt request register. Default Value: 0

(continued)

1	NOT_FULL	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	TRIGGER	Mask bit for corresponding bit in interrupt request register. Default Value: 0

28.1.154 SCB1_INTR_TX_MASKED

Transmitter interrupt masked request register

Address: 0x40250F8C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	None		R	R
HW Access	W	W	W	W	None		W	W
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	EMPTY	None [3:2]		NOT_FULL	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None					R	R	R
HW Access	None					W	W	W
Name	None [15:11]					UART_ARB_LOST	UART_DONE	UART_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10	UART_ARB_LOST	Logical and of corresponding request and mask bits. Default Value: 0
9	UART_DONE	Logical and of corresponding request and mask bits. Default Value: 0
8	UART_NACK	Logical and of corresponding request and mask bits. Default Value: 0
7	BLOCKED	Logical and of corresponding request and mask bits. Default Value: 0
6	UNDERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
5	OVERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
4	EMPTY	Logical and of corresponding request and mask bits. Default Value: 0

(continued)

1	NOT_FULL	Logical and of corresponding request and mask bits. Default Value: 0
0	TRIGGER	Logical and of corresponding request and mask bits. Default Value: 0

28.1.155 SCB1_INTR_RX

Receiver interrupt request register.

Address: 0x40250FC0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	None	RW1C	RW1C	None	RW1C
HW Access	RW1S	RW1S	RW1S	None	RW1S	RW1S	None	RW1S
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	None	FULL	NOT_EMPTY	None	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW1C	RW1C	RW1C	RW1C
HW Access	None				RW1S	RW1S	RW1S	RW1S
Name	None [15:12]				BREAK_DETECT	BAUD_DETECT	PARITY_ERROR	FRAME_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	BREAK_DETECT	Break detection is successful: the line is '0' for UART_RX_CTRL.BREAK_WIDTH + 1 bit period. Can occur at any time to address unanticipated break fields; i.e. "break-in-data" is supported. This feature is supported for the UART standard and LIN submodes. For the UART standard submodes, ongoing receipt of data frames is NOT affected; i.e. Firmware is ecpected to take the proper action. For the LIN submode, possible ongoing receipt of a data frame is stopped and the (partially) received data frame is dropped and baud rate detection is started. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
10	BAUD_DETECT	LIN baudrate detection is completed. The receiver software uses the UART_RX_STATUS.BR_COUNTER value to set the right IP clock (from the programmable clock IP) to guarantee successful receipt of the first LIN data frame (Protected Identifier Field) after the synchronization byte. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0

(continued)

9	PARITY_ERROR	Parity error in received data frame. Set to '1', when event is detected. Write with '1' to clear bit. If UART_RX_CTL.DROP_ON_PARITY_ERROR is '1', the received frame is dropped. If UART_RX_CTL.DROP_ON_PARITY_ERROR is '0', the received frame is send to the RX FIFO. In SmartCard submode, negatively acknowledged data frames generate a parity error. Note that Firmware can only identify the erroneous data frame in the RX FIFO if it is fast enough to read the data frame before the hardware writes a next data frame into the RX FIFO. Default Value: 0
8	FRAME_ERROR	Frame error in received data frame. Set to '1', when event is detected. Write with '1' to clear bit. This can be either a start or stop bit(s) error: Start bit error: after the detection of the beginning of a start bit period (RX line changes from '1' to '0'), the middle of the start bit period is sampled erroneously (RX line is '1'). Note: a start bit error is detected BEFORE a data frame is received. Stop bit error: the RX line is sampled as '0', but a '1' was expected. Note: a stop bit error may result in failure to receive successive data frame(s). Note: a stop bit error is detected AFTER a data frame is received. A stop bit error is detected after a data frame is received, and the UART_RX_CTL.DROP_ON_FRAME_ERROR field specifies whether the received frame is dropped or send to the RX FIFO. If UART_RX_CTL.DROP_ON_FRAME_ERROR is '1', the received data frame is dropped. If UART_RX_CTL.DROP_ON_FRAME_ERROR is '0', the received data frame is send to the RX FIFO. Note that Firmware can only identify the erroneous data frame in the RX FIFO if it is fast enough to read the data frame before the hardware writes a next data frame into the RX FIFO; i.e. the RX FIFO does not have error flags to tag erroneous data frames. Default Value: 0
7	BLOCKED	AHB-Lite read transfer can not get access to the EZ memory (EZ_DATA accesses), due to an externally clocked EZ access. This may happen when STATUS.EC_BUSY is '1'. Default Value: 0
6	UNDERFLOW	Attempt to read from an empty RX FIFO. Only used in FIFO mode. Default Value: 0
5	OVERFLOW	Attempt to write to a full RX FIFO. Note: in I2C mode, the OVERFLOW is set when a data frame is received and the RX FIFO is full, independent of whether it is ACK'd or NACK'd. Only used in FIFO mode. Default Value: 0
3	FULL	RX FIFO is full. Note that received data frames are lost when the RX FIFO is full. Dependent on CTRL.BYTE_MODET: BYTE_MODE is '0': # entries == FF_DATA_NR/2. BYTE_MODE is '1': # entries == FF_DATA_NR. Only used in FIFO mode. Default Value: 0
2	NOT_EMPTY	RX FIFO is not empty. Only used in FIFO mode. Default Value: 0
0	TRIGGER	More entries in the RX FIFO than the value specified by TRIGGER_LEVEL in SCB_RX_FIFO_CTL. Only used in FIFO mode. Default Value: 0

28.1.156 SCB1_INTR_RX_SET

Receiver interrupt set request register.

Address: 0x40250FC4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	None	RW1S	RW1S	None	RW1S
HW Access	A	A	A	None	A	A	None	A
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	None	FULL	NOT_EMPTY	None	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW1S	RW1S	RW1S	RW1S
HW Access	None				A	A	A	A
Name	None [15:12]				BREAK_DETECT	BAUD_DETECT	PARITY_ERROR	FRAME_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	BREAK_DETECT	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
10	BAUD_DETECT	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
9	PARITY_ERROR	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
8	FRAME_ERROR	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
7	BLOCKED	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
6	UNDERFLOW	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
5	OVERFLOW	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0

(continued)

3	FULL	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
2	NOT_EMPTY	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
0	TRIGGER	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

28.1.157 SCB1_INTR_RX_MASK

Receiver interrupt mask register.

Address: 0x40250FC8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	None	RW	RW	None	RW
HW Access	R	R	R	None	R	R	None	R
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	None	FULL	NOT_EMPTY	None	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [15:12]				BREAK_DETECT	BAUD_DETECT	PARITY_ERROR	FRAME_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	BREAK_DETECT	Mask bit for corresponding bit in interrupt request register. Default Value: 0
10	BAUD_DETECT	Mask bit for corresponding bit in interrupt request register. Default Value: 0
9	PARITY_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
8	FRAME_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
7	BLOCKED	Mask bit for corresponding bit in interrupt request register. Default Value: 0
6	UNDERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
5	OVERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0

(continued)

3	FULL	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	NOT_EMPTY	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	TRIGGER	Mask bit for corresponding bit in interrupt request register. Default Value: 0

28.1.158 SCB1_INTR_RX_MASKED

Receiver interrupt masked request register

Address: 0x40250FCC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	None	R	R	None	R
HW Access	W	W	W	None	W	W	None	W
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	None	FULL	NOT_EMPTY	None	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None				R	R	R	R
HW Access	None				W	W	W	W
Name	None [15:12]				BREAK_DETECT	BAUD_DETECT	PARITY_ERROR	FRAME_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	BREAK_DETECT	Logical and of corresponding request and mask bits. Default Value: 0
10	BAUD_DETECT	Logical and of corresponding request and mask bits. Default Value: 0
9	PARITY_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
8	FRAME_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
7	BLOCKED	Logical and of corresponding request and mask bits. Default Value: 0
6	UNDERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
5	OVERFLOW	Logical and of corresponding request and mask bits. Default Value: 0

(continued)

3	FULL	Logical and of corresponding request and mask bits. Default Value: 0
2	NOT_EMPTY	Logical and of corresponding request and mask bits. Default Value: 0
0	TRIGGER	Logical and of corresponding request and mask bits. Default Value: 0

29 Supervisory Flash (128 KB) Registers

This section discusses the Supervisory Flash (SFLASH) registers for 128 KB devices. It lists all the registers in mapping tables, in address order.

29.1 Register Details

Register Name	Address
SFLASH_PROT_ROW0	0x0FFFF000
SFLASH_PROT_ROW1	0x0FFFF001
SFLASH_PROT_ROW2	0x0FFFF002
SFLASH_PROT_ROW3	0x0FFFF003
SFLASH_PROT_ROW4	0x0FFFF004
SFLASH_PROT_ROW5	0x0FFFF005
SFLASH_PROT_ROW6	0x0FFFF006
SFLASH_PROT_ROW7	0x0FFFF007
SFLASH_PROT_ROW8	0x0FFFF008
SFLASH_PROT_ROW9	0x0FFFF009
SFLASH_PROT_ROW10	0x0FFFF00A
SFLASH_PROT_ROW11	0x0FFFF00B
SFLASH_PROT_ROW12	0x0FFFF00C
SFLASH_PROT_ROW13	0x0FFFF00D
SFLASH_PROT_ROW14	0x0FFFF00E
SFLASH_PROT_ROW15	0x0FFFF00F
SFLASH_PROT_ROW16	0x0FFFF010
SFLASH_PROT_ROW17	0x0FFFF011
SFLASH_PROT_ROW18	0x0FFFF012
SFLASH_PROT_ROW19	0x0FFFF013
SFLASH_PROT_ROW20	0x0FFFF014
SFLASH_PROT_ROW21	0x0FFFF015
SFLASH_PROT_ROW22	0x0FFFF016
SFLASH_PROT_ROW23	0x0FFFF017
SFLASH_PROT_ROW24	0x0FFFF018
SFLASH_PROT_ROW25	0x0FFFF019
SFLASH_PROT_ROW26	0x0FFFF01A

Register Name	Address
SFLASH_PROT_ROW27	0x0FFFF01B
SFLASH_PROT_ROW28	0x0FFFF01C
SFLASH_PROT_ROW29	0x0FFFF01D
SFLASH_PROT_ROW30	0x0FFFF01E
SFLASH_PROT_ROW31	0x0FFFF01F
SFLASH_PROT_ROW32	0x0FFFF020
SFLASH_PROT_ROW33	0x0FFFF021
SFLASH_PROT_ROW34	0x0FFFF022
SFLASH_PROT_ROW35	0x0FFFF023
SFLASH_PROT_ROW36	0x0FFFF024
SFLASH_PROT_ROW37	0x0FFFF025
SFLASH_PROT_ROW38	0x0FFFF026
SFLASH_PROT_ROW39	0x0FFFF027
SFLASH_PROT_ROW40	0x0FFFF028
SFLASH_PROT_ROW41	0x0FFFF029
SFLASH_PROT_ROW42	0x0FFFF02A
SFLASH_PROT_ROW43	0x0FFFF02B
SFLASH_PROT_ROW44	0x0FFFF02C
SFLASH_PROT_ROW45	0x0FFFF02D
SFLASH_PROT_ROW46	0x0FFFF02E
SFLASH_PROT_ROW47	0x0FFFF02F
SFLASH_PROT_ROW48	0x0FFFF030
SFLASH_PROT_ROW49	0x0FFFF031
SFLASH_PROT_ROW50	0x0FFFF032
SFLASH_PROT_ROW51	0x0FFFF033
SFLASH_PROT_ROW52	0x0FFFF034
SFLASH_PROT_ROW53	0x0FFFF035
SFLASH_PROT_ROW54	0x0FFFF036
SFLASH_PROT_ROW55	0x0FFFF037
SFLASH_PROT_ROW56	0x0FFFF038
SFLASH_PROT_ROW57	0x0FFFF039
SFLASH_PROT_ROW58	0x0FFFF03A
SFLASH_PROT_ROW59	0x0FFFF03B
SFLASH_PROT_ROW60	0x0FFFF03C
SFLASH_PROT_ROW61	0x0FFFF03D
SFLASH_PROT_ROW62	0x0FFFF03E
SFLASH_PROT_ROW63	0x0FFFF03F
SFLASH_PROT_PROTECTION	0x0FFFF07F
SFLASH_AV_PAIRS_8B0	0x0FFFF080
SFLASH_AV_PAIRS_8B1	0x0FFFF081
SFLASH_AV_PAIRS_8B2	0x0FFFF082
SFLASH_AV_PAIRS_8B3	0x0FFFF083

Register Name	Address
SFLASH_AV_PAIRS_8B4	0x0FFFF084
SFLASH_AV_PAIRS_8B5	0x0FFFF085
SFLASH_AV_PAIRS_8B6	0x0FFFF086
SFLASH_AV_PAIRS_8B7	0x0FFFF087
SFLASH_AV_PAIRS_8B8	0x0FFFF088
SFLASH_AV_PAIRS_8B9	0x0FFFF089
SFLASH_AV_PAIRS_8B10	0x0FFFF08A
SFLASH_AV_PAIRS_8B11	0x0FFFF08B
SFLASH_AV_PAIRS_8B12	0x0FFFF08C
SFLASH_AV_PAIRS_8B13	0x0FFFF08D
SFLASH_AV_PAIRS_8B14	0x0FFFF08E
SFLASH_AV_PAIRS_8B15	0x0FFFF08F
SFLASH_AV_PAIRS_8B16	0x0FFFF090
SFLASH_AV_PAIRS_8B17	0x0FFFF091
SFLASH_AV_PAIRS_8B18	0x0FFFF092
SFLASH_AV_PAIRS_8B19	0x0FFFF093
SFLASH_AV_PAIRS_8B20	0x0FFFF094
SFLASH_AV_PAIRS_8B21	0x0FFFF095
SFLASH_AV_PAIRS_8B22	0x0FFFF096
SFLASH_AV_PAIRS_8B23	0x0FFFF097
SFLASH_AV_PAIRS_8B24	0x0FFFF098
SFLASH_AV_PAIRS_8B25	0x0FFFF099
SFLASH_AV_PAIRS_8B26	0x0FFFF09A
SFLASH_AV_PAIRS_8B27	0x0FFFF09B
SFLASH_AV_PAIRS_8B28	0x0FFFF09C
SFLASH_AV_PAIRS_8B29	0x0FFFF09D
SFLASH_AV_PAIRS_8B30	0x0FFFF09E
SFLASH_AV_PAIRS_8B31	0x0FFFF09F
SFLASH_AV_PAIRS_8B32	0x0FFFF0A0
SFLASH_AV_PAIRS_8B33	0x0FFFF0A1
SFLASH_AV_PAIRS_8B34	0x0FFFF0A2
SFLASH_AV_PAIRS_8B35	0x0FFFF0A3
SFLASH_AV_PAIRS_8B36	0x0FFFF0A4
SFLASH_AV_PAIRS_8B37	0x0FFFF0A5
SFLASH_AV_PAIRS_8B38	0x0FFFF0A6
SFLASH_AV_PAIRS_8B39	0x0FFFF0A7
SFLASH_AV_PAIRS_8B40	0x0FFFF0A8
SFLASH_AV_PAIRS_8B41	0x0FFFF0A9
SFLASH_AV_PAIRS_8B42	0x0FFFF0AA
SFLASH_AV_PAIRS_8B43	0x0FFFF0AB
SFLASH_AV_PAIRS_8B44	0x0FFFF0AC
SFLASH_AV_PAIRS_8B45	0x0FFFF0AD

Register Name	Address
SFLASH_AV_PAIRS_8B46	0x0FFFF0AE
SFLASH_AV_PAIRS_8B47	0x0FFFF0AF
SFLASH_AV_PAIRS_8B48	0x0FFFF0B0
SFLASH_AV_PAIRS_8B49	0x0FFFF0B1
SFLASH_AV_PAIRS_8B50	0x0FFFF0B2
SFLASH_AV_PAIRS_8B51	0x0FFFF0B3
SFLASH_AV_PAIRS_8B52	0x0FFFF0B4
SFLASH_AV_PAIRS_8B53	0x0FFFF0B5
SFLASH_AV_PAIRS_8B54	0x0FFFF0B6
SFLASH_AV_PAIRS_8B55	0x0FFFF0B7
SFLASH_AV_PAIRS_8B56	0x0FFFF0B8
SFLASH_AV_PAIRS_8B57	0x0FFFF0B9
SFLASH_AV_PAIRS_8B58	0x0FFFF0BA
SFLASH_AV_PAIRS_8B59	0x0FFFF0BB
SFLASH_AV_PAIRS_8B60	0x0FFFF0BC
SFLASH_AV_PAIRS_8B61	0x0FFFF0BD
SFLASH_AV_PAIRS_8B62	0x0FFFF0BE
SFLASH_AV_PAIRS_8B63	0x0FFFF0BF
SFLASH_AV_PAIRS_8B64	0x0FFFF0C0
SFLASH_AV_PAIRS_8B65	0x0FFFF0C1
SFLASH_AV_PAIRS_8B66	0x0FFFF0C2
SFLASH_AV_PAIRS_8B67	0x0FFFF0C3
SFLASH_AV_PAIRS_8B68	0x0FFFF0C4
SFLASH_AV_PAIRS_8B69	0x0FFFF0C5
SFLASH_AV_PAIRS_8B70	0x0FFFF0C6
SFLASH_AV_PAIRS_8B71	0x0FFFF0C7
SFLASH_AV_PAIRS_8B72	0x0FFFF0C8
SFLASH_AV_PAIRS_8B73	0x0FFFF0C9
SFLASH_AV_PAIRS_8B74	0x0FFFF0CA
SFLASH_AV_PAIRS_8B75	0x0FFFF0CB
SFLASH_AV_PAIRS_8B76	0x0FFFF0CC
SFLASH_AV_PAIRS_8B77	0x0FFFF0CD
SFLASH_AV_PAIRS_8B78	0x0FFFF0CE
SFLASH_AV_PAIRS_8B79	0x0FFFF0CF
SFLASH_AV_PAIRS_8B80	0x0FFFF0D0
SFLASH_AV_PAIRS_8B81	0x0FFFF0D1
SFLASH_AV_PAIRS_8B82	0x0FFFF0D2
SFLASH_AV_PAIRS_8B83	0x0FFFF0D3
SFLASH_AV_PAIRS_8B84	0x0FFFF0D4
SFLASH_AV_PAIRS_8B85	0x0FFFF0D5
SFLASH_AV_PAIRS_8B86	0x0FFFF0D6
SFLASH_AV_PAIRS_8B87	0x0FFFF0D7

Register Name	Address
SFLASH_AV_PAIRS_8B88	0x0FFFF0D8
SFLASH_BLESS_BB_BUMP2	0x0FFFF0D8
SFLASH_AV_PAIRS_8B89	0x0FFFF0D9
SFLASH_AV_PAIRS_8B90	0x0FFFF0DA
SFLASH_BLESS_BB_XO	0x0FFFF0DA
SFLASH_AV_PAIRS_8B91	0x0FFFF0DB
SFLASH_AV_PAIRS_8B92	0x0FFFF0DC
SFLASH_BLESS_SY_BUMP1	0x0FFFF0DC
SFLASH_AV_PAIRS_8B93	0x0FFFF0DD
SFLASH_AV_PAIRS_8B94	0x0FFFF0DE
SFLASH_BLESS_LDO	0x0FFFF0DE
SFLASH_AV_PAIRS_8B95	0x0FFFF0DF
SFLASH_AV_PAIRS_8B96	0x0FFFF0E0
SFLASH_AV_PAIRS_8B97	0x0FFFF0E1
SFLASH_AV_PAIRS_8B98	0x0FFFF0E2
SFLASH_AV_PAIRS_8B99	0x0FFFF0E3
SFLASH_AV_PAIRS_8B100	0x0FFFF0E4
SFLASH_AV_PAIRS_8B101	0x0FFFF0E5
SFLASH_AV_PAIRS_8B102	0x0FFFF0E6
SFLASH_AV_PAIRS_8B103	0x0FFFF0E7
SFLASH_AV_PAIRS_8B104	0x0FFFF0E8
SFLASH_AV_PAIRS_8B105	0x0FFFF0E9
SFLASH_AV_PAIRS_8B106	0x0FFFF0EA
SFLASH_AV_PAIRS_8B107	0x0FFFF0EB
SFLASH_AV_PAIRS_8B108	0x0FFFF0EC
SFLASH_AV_PAIRS_8B109	0x0FFFF0ED
SFLASH_AV_PAIRS_8B110	0x0FFFF0EE
SFLASH_AV_PAIRS_8B111	0x0FFFF0EF
SFLASH_AV_PAIRS_8B112	0x0FFFF0F0
SFLASH_AV_PAIRS_8B113	0x0FFFF0F1
SFLASH_AV_PAIRS_8B114	0x0FFFF0F2
SFLASH_AV_PAIRS_8B115	0x0FFFF0F3
SFLASH_AV_PAIRS_8B116	0x0FFFF0F4
SFLASH_AV_PAIRS_8B117	0x0FFFF0F5
SFLASH_AV_PAIRS_8B118	0x0FFFF0F6
SFLASH_AV_PAIRS_8B119	0x0FFFF0F7
SFLASH_AV_PAIRS_8B120	0x0FFFF0F8
SFLASH_AV_PAIRS_8B121	0x0FFFF0F9
SFLASH_AV_PAIRS_8B122	0x0FFFF0FA
SFLASH_AV_PAIRS_8B123	0x0FFFF0FB
SFLASH_AV_PAIRS_8B124	0x0FFFF0FC
SFLASH_AV_PAIRS_8B125	0x0FFFF0FD

Register Name	Address
SFLASH_AV_PAIRS_8B126	0x0FFFF0FE
SFLASH_AV_PAIRS_8B127	0x0FFFF0FF
SFLASH_AV_PAIRS_32B0	0x0FFFF100
SFLASH_AV_PAIRS_32B1	0x0FFFF104
SFLASH_AV_PAIRS_32B2	0x0FFFF108
SFLASH_AV_PAIRS_32B3	0x0FFFF10C
SFLASH_AV_PAIRS_32B4	0x0FFFF110
SFLASH_AV_PAIRS_32B5	0x0FFFF114
SFLASH_AV_PAIRS_32B6	0x0FFFF118
SFLASH_AV_PAIRS_32B7	0x0FFFF11C
SFLASH_AV_PAIRS_32B8	0x0FFFF120
SFLASH_AV_PAIRS_32B9	0x0FFFF124
SFLASH_AV_PAIRS_32B10	0x0FFFF128
SFLASH_AV_PAIRS_32B11	0x0FFFF12C
SFLASH_AV_PAIRS_32B12	0x0FFFF130
SFLASH_AV_PAIRS_32B13	0x0FFFF134
SFLASH_AV_PAIRS_32B14	0x0FFFF138
SFLASH_AV_PAIRS_32B15	0x0FFFF13C
SFLASH_CPUSS_WOUNDING	0x0FFFF140
SFLASH_SILICON_ID	0x0FFFF144
SFLASH_CPUSS_PRIV_RAM	0x0FFFF148
SFLASH_CPUSS_PRIV_ROM_BROM	0x0FFFF14A
SFLASH_CPUSS_PRIV_FLASH	0x0FFFF14C
SFLASH_CPUSS_PRIV_ROM_SROM	0x0FFFF14E
SFLASH_HIB_KEY_DELAY	0x0FFFF150
SFLASH_DPSLP_KEY_DELAY	0x0FFFF152
SFLASH_SWD_CONFIG	0x0FFFF154
SFLASH_INITIAL_SPCIF_TRIM_M1_DAC0	0x0FFFF155
SFLASH_SWD_LISTEN	0x0FFFF158
SFLASH_FLASH_START	0x0FFFF15C
SFLASH_CSD_TRIM1_HVIDAC	0x0FFFF160
SFLASH_CSD_TRIM2_HVIDAC	0x0FFFF161
SFLASH_CSD_TRIM1_CSD	0x0FFFF162
SFLASH_CSD_TRIM2_CSD	0x0FFFF163
SFLASH_SAR_TEMP_MULTIPLIER	0x0FFFF164
SFLASH_SAR_TEMP_OFFSET	0x0FFFF166
SFLASH_SKIP_CHECKSUM	0x0FFFF169
SFLASH_PROT_VIRGINKEY0	0x0FFFF170
SFLASH_PROT_VIRGINKEY1	0x0FFFF171
SFLASH_PROT_VIRGINKEY2	0x0FFFF172
SFLASH_PROT_VIRGINKEY3	0x0FFFF173
SFLASH_PROT_VIRGINKEY4	0x0FFFF174

Register Name	Address
SFLASH_PROT_VIRGINKEY5	0x0FFFF175
SFLASH_PROT_VIRGINKEY6	0x0FFFF176
SFLASH_PROT_VIRGINKEY7	0x0FFFF177
SFLASH_DIE_LOT0	0x0FFFF178
SFLASH_DIE_LOT1	0x0FFFF179
SFLASH_DIE_LOT2	0x0FFFF17A
SFLASH_DIE_WAFER	0x0FFFF17B
SFLASH_DIE_X	0x0FFFF17C
SFLASH_DIE_Y	0x0FFFF17D
SFLASH_DIE_SORT	0x0FFFF17E
SFLASH_DIE_MINOR	0x0FFFF17F
SFLASH_PE_TE_DATA0	0x0FFFF180
SFLASH_PE_TE_DATA1	0x0FFFF181
SFLASH_PE_TE_DATA2	0x0FFFF182
SFLASH_PE_TE_DATA3	0x0FFFF183
SFLASH_PE_TE_DATA4	0x0FFFF184
SFLASH_PE_TE_DATA5	0x0FFFF185
SFLASH_PE_TE_DATA6	0x0FFFF186
SFLASH_PE_TE_DATA7	0x0FFFF187
SFLASH_PE_TE_DATA8	0x0FFFF188
SFLASH_PE_TE_DATA9	0x0FFFF189
SFLASH_PE_TE_DATA10	0x0FFFF18A
SFLASH_PE_TE_DATA11	0x0FFFF18B
SFLASH_PE_TE_DATA12	0x0FFFF18C
SFLASH_PE_TE_DATA13	0x0FFFF18D
SFLASH_PE_TE_DATA14	0x0FFFF18E
SFLASH_PE_TE_DATA15	0x0FFFF18F
SFLASH_PE_TE_DATA16	0x0FFFF190
SFLASH_PE_TE_DATA17	0x0FFFF191
SFLASH_PE_TE_DATA18	0x0FFFF192
SFLASH_PE_TE_DATA19	0x0FFFF193
SFLASH_PE_TE_DATA20	0x0FFFF194
SFLASH_PE_TE_DATA21	0x0FFFF195
SFLASH_PE_TE_DATA22	0x0FFFF196
SFLASH_PE_TE_DATA23	0x0FFFF197
SFLASH_PE_TE_DATA24	0x0FFFF198
SFLASH_PE_TE_DATA25	0x0FFFF199
SFLASH_PE_TE_DATA26	0x0FFFF19A
SFLASH_PE_TE_DATA27	0x0FFFF19B
SFLASH_PE_TE_DATA28	0x0FFFF19C
SFLASH_PE_TE_DATA29	0x0FFFF19D
SFLASH_PE_TE_DATA30	0x0FFFF19E

Register Name	Address
SFLASH_PE_TE_DATA31	0x0FFFF19F
SFLASH_PP	0x0FFFF1A0
SFLASH_E	0x0FFFF1A4
SFLASH_P	0x0FFFF1A8
SFLASH_EA_E	0x0FFFF1AC
SFLASH_EA_P	0x0FFFF1B0
SFLASH_ES_E	0x0FFFF1B4
SFLASH_ES_P_EO	0x0FFFF1B8
SFLASH_E_VCTAT	0x0FFFF1BC
SFLASH_P_VCTAT	0x0FFFF1BD
SFLASH_IMO_MAXF0	0x0FFFF1C0
SFLASH_IMO_ABS0	0x0FFFF1C1
SFLASH_IMO_TMPCO0	0x0FFFF1C2
SFLASH_IMO_MAXF1	0x0FFFF1C3
SFLASH_IMO_ABS1	0x0FFFF1C4
SFLASH_IMO_TMPCO1	0x0FFFF1C5
SFLASH_IMO_MAXF2	0x0FFFF1C6
SFLASH_IMO_ABS2	0x0FFFF1C7
SFLASH_IMO_TMPCO2	0x0FFFF1C8
SFLASH_IMO_MAXF3	0x0FFFF1C9
SFLASH_IMO_ABS3	0x0FFFF1CA
SFLASH_IMO_TMPCO3	0x0FFFF1CB
SFLASH_IMO_ABS4	0x0FFFF1CC
SFLASH_IMO_TMPCO4	0x0FFFF1CD
SFLASH_IMO_TRIM0	0x0FFFF1D0
SFLASH_IMO_TRIM1	0x0FFFF1D1
SFLASH_IMO_TRIM2	0x0FFFF1D2
SFLASH_IMO_TRIM3	0x0FFFF1D3
SFLASH_IMO_TRIM4	0x0FFFF1D4
SFLASH_IMO_TRIM5	0x0FFFF1D5
SFLASH_IMO_TRIM6	0x0FFFF1D6
SFLASH_IMO_TRIM7	0x0FFFF1D7
SFLASH_IMO_TRIM8	0x0FFFF1D8
SFLASH_IMO_TRIM9	0x0FFFF1D9
SFLASH_IMO_TRIM10	0x0FFFF1DA
SFLASH_IMO_TRIM11	0x0FFFF1DB
SFLASH_IMO_TRIM12	0x0FFFF1DC
SFLASH_IMO_TRIM13	0x0FFFF1DD
SFLASH_IMO_TRIM14	0x0FFFF1DE
SFLASH_IMO_TRIM15	0x0FFFF1DF
SFLASH_IMO_TRIM16	0x0FFFF1E0
SFLASH_IMO_TRIM17	0x0FFFF1E1

Register Name	Address
SFLASH_IMO_TRIM18	0x0FFFF1E2
SFLASH_IMO_TRIM19	0x0FFFF1E3
SFLASH_IMO_TRIM20	0x0FFFF1E4
SFLASH_IMO_TRIM21	0x0FFFF1E5
SFLASH_IMO_TRIM22	0x0FFFF1E6
SFLASH_IMO_TRIM23	0x0FFFF1E7
SFLASH_IMO_TRIM24	0x0FFFF1E8
SFLASH_IMO_TRIM25	0x0FFFF1E9
SFLASH_IMO_TRIM26	0x0FFFF1EA
SFLASH_IMO_TRIM27	0x0FFFF1EB
SFLASH_IMO_TRIM28	0x0FFFF1EC
SFLASH_IMO_TRIM29	0x0FFFF1ED
SFLASH_IMO_TRIM30	0x0FFFF1EE
SFLASH_IMO_TRIM31	0x0FFFF1EF
SFLASH_IMO_TRIM32	0x0FFFF1F0
SFLASH_IMO_TRIM33	0x0FFFF1F1
SFLASH_IMO_TRIM34	0x0FFFF1F2
SFLASH_IMO_TRIM35	0x0FFFF1F3
SFLASH_IMO_TRIM36	0x0FFFF1F4
SFLASH_IMO_TRIM37	0x0FFFF1F5
SFLASH_IMO_TRIM38	0x0FFFF1F6
SFLASH_IMO_TRIM39	0x0FFFF1F7
SFLASH_IMO_TRIM40	0x0FFFF1F8
SFLASH_IMO_TRIM41	0x0FFFF1F9
SFLASH_IMO_TRIM42	0x0FFFF1FA
SFLASH_IMO_TRIM43	0x0FFFF1FB
SFLASH_IMO_TRIM44	0x0FFFF1FC
SFLASH_IMO_TRIM45	0x0FFFF1FD
SFLASH_CHECKSUM	0x0FFFF1FE
SFLASH_MACRO_0_FREE_SFLASH0	0x0FFFF200
SFLASH_MACRO_0_FREE_SFLASH1	0x0FFFF201
SFLASH_MACRO_0_FREE_SFLASH2	0x0FFFF202
SFLASH_MACRO_0_FREE_SFLASH3	0x0FFFF203
SFLASH_MACRO_0_FREE_SFLASH4	0x0FFFF204
SFLASH_MACRO_0_FREE_SFLASH5	0x0FFFF205
SFLASH_MACRO_0_FREE_SFLASH6	0x0FFFF206
SFLASH_MACRO_0_FREE_SFLASH7	0x0FFFF207
SFLASH_MACRO_0_FREE_SFLASH8	0x0FFFF208
SFLASH_MACRO_0_FREE_SFLASH9	0x0FFFF209
SFLASH_MACRO_0_FREE_SFLASH10	0x0FFFF20A
SFLASH_MACRO_0_FREE_SFLASH11	0x0FFFF20B
SFLASH_MACRO_0_FREE_SFLASH12	0x0FFFF20C

Register Name	Address
SFLASH_MACRO_0_FREE_SFLASH13	0x0FFFF20D
SFLASH_MACRO_0_FREE_SFLASH14	0x0FFFF20E
SFLASH_MACRO_0_FREE_SFLASH15	0x0FFFF20F
SFLASH_MACRO_0_FREE_SFLASH16	0x0FFFF210
SFLASH_MACRO_0_FREE_SFLASH17	0x0FFFF211
SFLASH_MACRO_0_FREE_SFLASH18	0x0FFFF212
SFLASH_MACRO_0_FREE_SFLASH19	0x0FFFF213
SFLASH_MACRO_0_FREE_SFLASH20	0x0FFFF214
SFLASH_MACRO_0_FREE_SFLASH21	0x0FFFF215
SFLASH_MACRO_0_FREE_SFLASH22	0x0FFFF216
SFLASH_MACRO_0_FREE_SFLASH23	0x0FFFF217
SFLASH_MACRO_0_FREE_SFLASH24	0x0FFFF218
SFLASH_MACRO_0_FREE_SFLASH25	0x0FFFF219
SFLASH_MACRO_0_FREE_SFLASH26	0x0FFFF21A
SFLASH_MACRO_0_FREE_SFLASH27	0x0FFFF21B
SFLASH_MACRO_0_FREE_SFLASH28	0x0FFFF21C
SFLASH_MACRO_0_FREE_SFLASH29	0x0FFFF21D
SFLASH_MACRO_0_FREE_SFLASH30	0x0FFFF21E
SFLASH_MACRO_0_FREE_SFLASH31	0x0FFFF21F
SFLASH_MACRO_0_FREE_SFLASH32	0x0FFFF220
SFLASH_MACRO_0_FREE_SFLASH33	0x0FFFF221
SFLASH_MACRO_0_FREE_SFLASH34	0x0FFFF222
SFLASH_MACRO_0_FREE_SFLASH35	0x0FFFF223
SFLASH_MACRO_0_FREE_SFLASH36	0x0FFFF224
SFLASH_MACRO_0_FREE_SFLASH37	0x0FFFF225
SFLASH_MACRO_0_FREE_SFLASH38	0x0FFFF226
SFLASH_MACRO_0_FREE_SFLASH39	0x0FFFF227
SFLASH_MACRO_0_FREE_SFLASH40	0x0FFFF228
SFLASH_MACRO_0_FREE_SFLASH41	0x0FFFF229
SFLASH_MACRO_0_FREE_SFLASH42	0x0FFFF22A
SFLASH_MACRO_0_FREE_SFLASH43	0x0FFFF22B
SFLASH_MACRO_0_FREE_SFLASH44	0x0FFFF22C
SFLASH_MACRO_0_FREE_SFLASH45	0x0FFFF22D
SFLASH_MACRO_0_FREE_SFLASH46	0x0FFFF22E
SFLASH_MACRO_0_FREE_SFLASH47	0x0FFFF22F
SFLASH_MACRO_0_FREE_SFLASH48	0x0FFFF230
SFLASH_MACRO_0_FREE_SFLASH49	0x0FFFF231
SFLASH_MACRO_0_FREE_SFLASH50	0x0FFFF232
SFLASH_MACRO_0_FREE_SFLASH51	0x0FFFF233
SFLASH_MACRO_0_FREE_SFLASH52	0x0FFFF234
SFLASH_MACRO_0_FREE_SFLASH53	0x0FFFF235
SFLASH_MACRO_0_FREE_SFLASH54	0x0FFFF236

Register Name	Address
SFLASH_MACRO_0_FREE_SFLASH55	0x0FFFF237
SFLASH_MACRO_0_FREE_SFLASH56	0x0FFFF238
SFLASH_MACRO_0_FREE_SFLASH57	0x0FFFF239
SFLASH_MACRO_0_FREE_SFLASH58	0x0FFFF23A
SFLASH_MACRO_0_FREE_SFLASH59	0x0FFFF23B
SFLASH_MACRO_0_FREE_SFLASH60	0x0FFFF23C
SFLASH_MACRO_0_FREE_SFLASH61	0x0FFFF23D
SFLASH_MACRO_0_FREE_SFLASH62	0x0FFFF23E
SFLASH_MACRO_0_FREE_SFLASH63	0x0FFFF23F
SFLASH_MACRO_0_FREE_SFLASH64	0x0FFFF240
SFLASH_MACRO_0_FREE_SFLASH65	0x0FFFF241
SFLASH_MACRO_0_FREE_SFLASH66	0x0FFFF242
SFLASH_MACRO_0_FREE_SFLASH67	0x0FFFF243
SFLASH_MACRO_0_FREE_SFLASH68	0x0FFFF244
SFLASH_MACRO_0_FREE_SFLASH69	0x0FFFF245
SFLASH_MACRO_0_FREE_SFLASH70	0x0FFFF246
SFLASH_MACRO_0_FREE_SFLASH71	0x0FFFF247
SFLASH_MACRO_0_FREE_SFLASH72	0x0FFFF248
SFLASH_MACRO_0_FREE_SFLASH73	0x0FFFF249
SFLASH_MACRO_0_FREE_SFLASH74	0x0FFFF24A
SFLASH_MACRO_0_FREE_SFLASH75	0x0FFFF24B
SFLASH_MACRO_0_FREE_SFLASH76	0x0FFFF24C
SFLASH_MACRO_0_FREE_SFLASH77	0x0FFFF24D
SFLASH_MACRO_0_FREE_SFLASH78	0x0FFFF24E
SFLASH_MACRO_0_FREE_SFLASH79	0x0FFFF24F
SFLASH_MACRO_0_FREE_SFLASH80	0x0FFFF250
SFLASH_MACRO_0_FREE_SFLASH81	0x0FFFF251
SFLASH_MACRO_0_FREE_SFLASH82	0x0FFFF252
SFLASH_MACRO_0_FREE_SFLASH83	0x0FFFF253
SFLASH_MACRO_0_FREE_SFLASH84	0x0FFFF254
SFLASH_MACRO_0_FREE_SFLASH85	0x0FFFF255
SFLASH_MACRO_0_FREE_SFLASH86	0x0FFFF256
SFLASH_MACRO_0_FREE_SFLASH87	0x0FFFF257
SFLASH_MACRO_0_FREE_SFLASH88	0x0FFFF258
SFLASH_MACRO_0_FREE_SFLASH89	0x0FFFF259
SFLASH_MACRO_0_FREE_SFLASH90	0x0FFFF25A
SFLASH_MACRO_0_FREE_SFLASH91	0x0FFFF25B
SFLASH_MACRO_0_FREE_SFLASH92	0x0FFFF25C
SFLASH_MACRO_0_FREE_SFLASH93	0x0FFFF25D
SFLASH_MACRO_0_FREE_SFLASH94	0x0FFFF25E
SFLASH_MACRO_0_FREE_SFLASH95	0x0FFFF25F
SFLASH_MACRO_0_FREE_SFLASH96	0x0FFFF260

Register Name	Address
SFLASH_MACRO_0_FREE_SFLASH97	0x0FFFF261
SFLASH_MACRO_0_FREE_SFLASH98	0x0FFFF262
SFLASH_MACRO_0_FREE_SFLASH99	0x0FFFF263
SFLASH_MACRO_0_FREE_SFLASH100	0x0FFFF264
SFLASH_MACRO_0_FREE_SFLASH101	0x0FFFF265
SFLASH_MACRO_0_FREE_SFLASH102	0x0FFFF266
SFLASH_MACRO_0_FREE_SFLASH103	0x0FFFF267
SFLASH_MACRO_0_FREE_SFLASH104	0x0FFFF268
SFLASH_MACRO_0_FREE_SFLASH105	0x0FFFF269
SFLASH_MACRO_0_FREE_SFLASH106	0x0FFFF26A
SFLASH_MACRO_0_FREE_SFLASH107	0x0FFFF26B
SFLASH_MACRO_0_FREE_SFLASH108	0x0FFFF26C
SFLASH_MACRO_0_FREE_SFLASH109	0x0FFFF26D
SFLASH_MACRO_0_FREE_SFLASH110	0x0FFFF26E
SFLASH_MACRO_0_FREE_SFLASH111	0x0FFFF26F
SFLASH_MACRO_0_FREE_SFLASH112	0x0FFFF270
SFLASH_MACRO_0_FREE_SFLASH113	0x0FFFF271
SFLASH_MACRO_0_FREE_SFLASH114	0x0FFFF272
SFLASH_MACRO_0_FREE_SFLASH115	0x0FFFF273
SFLASH_MACRO_0_FREE_SFLASH116	0x0FFFF274
SFLASH_MACRO_0_FREE_SFLASH117	0x0FFFF275
SFLASH_MACRO_0_FREE_SFLASH118	0x0FFFF276
SFLASH_MACRO_0_FREE_SFLASH119	0x0FFFF277
SFLASH_MACRO_0_FREE_SFLASH120	0x0FFFF278
SFLASH_MACRO_0_FREE_SFLASH121	0x0FFFF279
SFLASH_MACRO_0_FREE_SFLASH122	0x0FFFF27A
SFLASH_MACRO_0_FREE_SFLASH123	0x0FFFF27B
SFLASH_MACRO_0_FREE_SFLASH124	0x0FFFF27C
SFLASH_MACRO_0_FREE_SFLASH125	0x0FFFF27D
SFLASH_MACRO_0_FREE_SFLASH126	0x0FFFF27E
SFLASH_MACRO_0_FREE_SFLASH127	0x0FFFF27F
SFLASH_MACRO_0_FREE_SFLASH128	0x0FFFF280
SFLASH_MACRO_0_FREE_SFLASH129	0x0FFFF281
SFLASH_MACRO_0_FREE_SFLASH130	0x0FFFF282
SFLASH_MACRO_0_FREE_SFLASH131	0x0FFFF283
SFLASH_MACRO_0_FREE_SFLASH132	0x0FFFF284
SFLASH_MACRO_0_FREE_SFLASH133	0x0FFFF285
SFLASH_MACRO_0_FREE_SFLASH134	0x0FFFF286
SFLASH_MACRO_0_FREE_SFLASH135	0x0FFFF287
SFLASH_MACRO_0_FREE_SFLASH136	0x0FFFF288
SFLASH_MACRO_0_FREE_SFLASH137	0x0FFFF289
SFLASH_MACRO_0_FREE_SFLASH138	0x0FFFF28A

Register Name	Address
SFLASH_MACRO_0_FREE_SFLASH139	0x0FFFF28B
SFLASH_MACRO_0_FREE_SFLASH140	0x0FFFF28C
SFLASH_MACRO_0_FREE_SFLASH141	0x0FFFF28D
SFLASH_MACRO_0_FREE_SFLASH142	0x0FFFF28E
SFLASH_MACRO_0_FREE_SFLASH143	0x0FFFF28F
SFLASH_MACRO_0_FREE_SFLASH144	0x0FFFF290
SFLASH_MACRO_0_FREE_SFLASH145	0x0FFFF291
SFLASH_MACRO_0_FREE_SFLASH146	0x0FFFF292
SFLASH_MACRO_0_FREE_SFLASH147	0x0FFFF293
SFLASH_MACRO_0_FREE_SFLASH148	0x0FFFF294
SFLASH_MACRO_0_FREE_SFLASH149	0x0FFFF295
SFLASH_MACRO_0_FREE_SFLASH150	0x0FFFF296
SFLASH_MACRO_0_FREE_SFLASH151	0x0FFFF297
SFLASH_MACRO_0_FREE_SFLASH152	0x0FFFF298
SFLASH_MACRO_0_FREE_SFLASH153	0x0FFFF299
SFLASH_MACRO_0_FREE_SFLASH154	0x0FFFF29A
SFLASH_MACRO_0_FREE_SFLASH155	0x0FFFF29B
SFLASH_MACRO_0_FREE_SFLASH156	0x0FFFF29C
SFLASH_MACRO_0_FREE_SFLASH157	0x0FFFF29D
SFLASH_MACRO_0_FREE_SFLASH158	0x0FFFF29E
SFLASH_MACRO_0_FREE_SFLASH159	0x0FFFF29F
SFLASH_MACRO_0_FREE_SFLASH160	0x0FFFF2A0
SFLASH_MACRO_0_FREE_SFLASH161	0x0FFFF2A1
SFLASH_MACRO_0_FREE_SFLASH162	0x0FFFF2A2
SFLASH_MACRO_0_FREE_SFLASH163	0x0FFFF2A3
SFLASH_MACRO_0_FREE_SFLASH164	0x0FFFF2A4
SFLASH_MACRO_0_FREE_SFLASH165	0x0FFFF2A5
SFLASH_MACRO_0_FREE_SFLASH166	0x0FFFF2A6
SFLASH_MACRO_0_FREE_SFLASH167	0x0FFFF2A7
SFLASH_MACRO_0_FREE_SFLASH168	0x0FFFF2A8
SFLASH_MACRO_0_FREE_SFLASH169	0x0FFFF2A9
SFLASH_MACRO_0_FREE_SFLASH170	0x0FFFF2AA
SFLASH_MACRO_0_FREE_SFLASH171	0x0FFFF2AB
SFLASH_MACRO_0_FREE_SFLASH172	0x0FFFF2AC
SFLASH_MACRO_0_FREE_SFLASH173	0x0FFFF2AD
SFLASH_MACRO_0_FREE_SFLASH174	0x0FFFF2AE
SFLASH_MACRO_0_FREE_SFLASH175	0x0FFFF2AF
SFLASH_MACRO_0_FREE_SFLASH176	0x0FFFF2B0
SFLASH_MACRO_0_FREE_SFLASH177	0x0FFFF2B1
SFLASH_MACRO_0_FREE_SFLASH178	0x0FFFF2B2
SFLASH_MACRO_0_FREE_SFLASH179	0x0FFFF2B3
SFLASH_MACRO_0_FREE_SFLASH180	0x0FFFF2B4

Register Name	Address
SFLASH_MACRO_0_FREE_SFLASH181	0x0FFFF2B5
SFLASH_MACRO_0_FREE_SFLASH182	0x0FFFF2B6
SFLASH_MACRO_0_FREE_SFLASH183	0x0FFFF2B7
SFLASH_MACRO_0_FREE_SFLASH184	0x0FFFF2B8
SFLASH_MACRO_0_FREE_SFLASH185	0x0FFFF2B9
SFLASH_MACRO_0_FREE_SFLASH186	0x0FFFF2BA
SFLASH_MACRO_0_FREE_SFLASH187	0x0FFFF2BB
SFLASH_MACRO_0_FREE_SFLASH188	0x0FFFF2BC
SFLASH_MACRO_0_FREE_SFLASH189	0x0FFFF2BD
SFLASH_MACRO_0_FREE_SFLASH190	0x0FFFF2BE
SFLASH_MACRO_0_FREE_SFLASH191	0x0FFFF2BF
SFLASH_MACRO_0_FREE_SFLASH192	0x0FFFF2C0
SFLASH_MACRO_0_FREE_SFLASH193	0x0FFFF2C1
SFLASH_MACRO_0_FREE_SFLASH194	0x0FFFF2C2
SFLASH_MACRO_0_FREE_SFLASH195	0x0FFFF2C3
SFLASH_MACRO_0_FREE_SFLASH196	0x0FFFF2C4
SFLASH_MACRO_0_FREE_SFLASH197	0x0FFFF2C5
SFLASH_MACRO_0_FREE_SFLASH198	0x0FFFF2C6
SFLASH_MACRO_0_FREE_SFLASH199	0x0FFFF2C7
SFLASH_MACRO_0_FREE_SFLASH200	0x0FFFF2C8
SFLASH_MACRO_0_FREE_SFLASH201	0x0FFFF2C9
SFLASH_MACRO_0_FREE_SFLASH202	0x0FFFF2CA
SFLASH_MACRO_0_FREE_SFLASH203	0x0FFFF2CB
SFLASH_MACRO_0_FREE_SFLASH204	0x0FFFF2CC
SFLASH_MACRO_0_FREE_SFLASH205	0x0FFFF2CD
SFLASH_MACRO_0_FREE_SFLASH206	0x0FFFF2CE
SFLASH_MACRO_0_FREE_SFLASH207	0x0FFFF2CF
SFLASH_MACRO_0_FREE_SFLASH208	0x0FFFF2D0
SFLASH_MACRO_0_FREE_SFLASH209	0x0FFFF2D1
SFLASH_MACRO_0_FREE_SFLASH210	0x0FFFF2D2
SFLASH_MACRO_0_FREE_SFLASH211	0x0FFFF2D3
SFLASH_MACRO_0_FREE_SFLASH212	0x0FFFF2D4
SFLASH_MACRO_0_FREE_SFLASH213	0x0FFFF2D5
SFLASH_MACRO_0_FREE_SFLASH214	0x0FFFF2D6
SFLASH_MACRO_0_FREE_SFLASH215	0x0FFFF2D7
SFLASH_MACRO_0_FREE_SFLASH216	0x0FFFF2D8
SFLASH_MACRO_0_FREE_SFLASH217	0x0FFFF2D9
SFLASH_MACRO_0_FREE_SFLASH218	0x0FFFF2DA
SFLASH_MACRO_0_FREE_SFLASH219	0x0FFFF2DB
SFLASH_MACRO_0_FREE_SFLASH220	0x0FFFF2DC
SFLASH_MACRO_0_FREE_SFLASH221	0x0FFFF2DD
SFLASH_MACRO_0_FREE_SFLASH222	0x0FFFF2DE

Register Name	Address
SFLASH_MACRO_0_FREE_SFLASH223	0x0FFFF2DF
SFLASH_MACRO_0_FREE_SFLASH224	0x0FFFF2E0
SFLASH_MACRO_0_FREE_SFLASH225	0x0FFFF2E1
SFLASH_MACRO_0_FREE_SFLASH226	0x0FFFF2E2
SFLASH_MACRO_0_FREE_SFLASH227	0x0FFFF2E3
SFLASH_MACRO_0_FREE_SFLASH228	0x0FFFF2E4
SFLASH_MACRO_0_FREE_SFLASH229	0x0FFFF2E5
SFLASH_MACRO_0_FREE_SFLASH230	0x0FFFF2E6
SFLASH_MACRO_0_FREE_SFLASH231	0x0FFFF2E7
SFLASH_MACRO_0_FREE_SFLASH232	0x0FFFF2E8
SFLASH_MACRO_0_FREE_SFLASH233	0x0FFFF2E9
SFLASH_MACRO_0_FREE_SFLASH234	0x0FFFF2EA
SFLASH_MACRO_0_FREE_SFLASH235	0x0FFFF2EB
SFLASH_MACRO_0_FREE_SFLASH236	0x0FFFF2EC
SFLASH_MACRO_0_FREE_SFLASH237	0x0FFFF2ED
SFLASH_MACRO_0_FREE_SFLASH238	0x0FFFF2EE
SFLASH_MACRO_0_FREE_SFLASH239	0x0FFFF2EF
SFLASH_MACRO_0_FREE_SFLASH240	0x0FFFF2F0
SFLASH_MACRO_0_FREE_SFLASH241	0x0FFFF2F1
SFLASH_MACRO_0_FREE_SFLASH242	0x0FFFF2F2
SFLASH_MACRO_0_FREE_SFLASH243	0x0FFFF2F3
SFLASH_MACRO_0_FREE_SFLASH244	0x0FFFF2F4
SFLASH_MACRO_0_FREE_SFLASH245	0x0FFFF2F5
SFLASH_MACRO_0_FREE_SFLASH246	0x0FFFF2F6
SFLASH_MACRO_0_FREE_SFLASH247	0x0FFFF2F7
SFLASH_MACRO_0_FREE_SFLASH248	0x0FFFF2F8
SFLASH_MACRO_0_FREE_SFLASH249	0x0FFFF2F9
SFLASH_MACRO_0_FREE_SFLASH250	0x0FFFF2FA
SFLASH_MACRO_0_FREE_SFLASH251	0x0FFFF2FB
SFLASH_MACRO_0_FREE_SFLASH252	0x0FFFF2FC
SFLASH_MACRO_0_FREE_SFLASH253	0x0FFFF2FD
SFLASH_MACRO_0_FREE_SFLASH254	0x0FFFF2FE
SFLASH_MACRO_0_FREE_SFLASH255	0x0FFFF2FF
SFLASH_MACRO_0_FREE_SFLASH256	0x0FFFF300
SFLASH_MACRO_0_FREE_SFLASH257	0x0FFFF301
SFLASH_MACRO_0_FREE_SFLASH258	0x0FFFF302
SFLASH_MACRO_0_FREE_SFLASH259	0x0FFFF303
SFLASH_MACRO_0_FREE_SFLASH260	0x0FFFF304
SFLASH_MACRO_0_FREE_SFLASH261	0x0FFFF305
SFLASH_MACRO_0_FREE_SFLASH262	0x0FFFF306
SFLASH_MACRO_0_FREE_SFLASH263	0x0FFFF307
SFLASH_MACRO_0_FREE_SFLASH264	0x0FFFF308

Register Name	Address
SFLASH_MACRO_0_FREE_SFLASH265	0x0FFFF309
SFLASH_MACRO_0_FREE_SFLASH266	0x0FFFF30A
SFLASH_MACRO_0_FREE_SFLASH267	0x0FFFF30B
SFLASH_MACRO_0_FREE_SFLASH268	0x0FFFF30C
SFLASH_MACRO_0_FREE_SFLASH269	0x0FFFF30D
SFLASH_MACRO_0_FREE_SFLASH270	0x0FFFF30E
SFLASH_MACRO_0_FREE_SFLASH271	0x0FFFF30F
SFLASH_MACRO_0_FREE_SFLASH272	0x0FFFF310
SFLASH_MACRO_0_FREE_SFLASH273	0x0FFFF311
SFLASH_MACRO_0_FREE_SFLASH274	0x0FFFF312
SFLASH_MACRO_0_FREE_SFLASH275	0x0FFFF313
SFLASH_MACRO_0_FREE_SFLASH276	0x0FFFF314
SFLASH_MACRO_0_FREE_SFLASH277	0x0FFFF315
SFLASH_MACRO_0_FREE_SFLASH278	0x0FFFF316
SFLASH_MACRO_0_FREE_SFLASH279	0x0FFFF317
SFLASH_MACRO_0_FREE_SFLASH280	0x0FFFF318
SFLASH_MACRO_0_FREE_SFLASH281	0x0FFFF319
SFLASH_MACRO_0_FREE_SFLASH282	0x0FFFF31A
SFLASH_MACRO_0_FREE_SFLASH283	0x0FFFF31B
SFLASH_MACRO_0_FREE_SFLASH284	0x0FFFF31C
SFLASH_MACRO_0_FREE_SFLASH285	0x0FFFF31D
SFLASH_MACRO_0_FREE_SFLASH286	0x0FFFF31E
SFLASH_MACRO_0_FREE_SFLASH287	0x0FFFF31F
SFLASH_MACRO_0_FREE_SFLASH288	0x0FFFF320
SFLASH_MACRO_0_FREE_SFLASH289	0x0FFFF321
SFLASH_MACRO_0_FREE_SFLASH290	0x0FFFF322
SFLASH_MACRO_0_FREE_SFLASH291	0x0FFFF323
SFLASH_MACRO_0_FREE_SFLASH292	0x0FFFF324
SFLASH_MACRO_0_FREE_SFLASH293	0x0FFFF325
SFLASH_MACRO_0_FREE_SFLASH294	0x0FFFF326
SFLASH_MACRO_0_FREE_SFLASH295	0x0FFFF327
SFLASH_MACRO_0_FREE_SFLASH296	0x0FFFF328
SFLASH_MACRO_0_FREE_SFLASH297	0x0FFFF329
SFLASH_MACRO_0_FREE_SFLASH298	0x0FFFF32A
SFLASH_MACRO_0_FREE_SFLASH299	0x0FFFF32B
SFLASH_MACRO_0_FREE_SFLASH300	0x0FFFF32C
SFLASH_MACRO_0_FREE_SFLASH301	0x0FFFF32D
SFLASH_MACRO_0_FREE_SFLASH302	0x0FFFF32E
SFLASH_MACRO_0_FREE_SFLASH303	0x0FFFF32F
SFLASH_MACRO_0_FREE_SFLASH304	0x0FFFF330
SFLASH_MACRO_0_FREE_SFLASH305	0x0FFFF331
SFLASH_MACRO_0_FREE_SFLASH306	0x0FFFF332

Register Name	Address
SFLASH_MACRO_0_FREE_SFLASH307	0x0FFFF333
SFLASH_MACRO_0_FREE_SFLASH308	0x0FFFF334
SFLASH_MACRO_0_FREE_SFLASH309	0x0FFFF335
SFLASH_MACRO_0_FREE_SFLASH310	0x0FFFF336
SFLASH_MACRO_0_FREE_SFLASH311	0x0FFFF337
SFLASH_MACRO_0_FREE_SFLASH312	0x0FFFF338
SFLASH_MACRO_0_FREE_SFLASH313	0x0FFFF339
SFLASH_MACRO_0_FREE_SFLASH314	0x0FFFF33A
SFLASH_MACRO_0_FREE_SFLASH315	0x0FFFF33B
SFLASH_MACRO_0_FREE_SFLASH316	0x0FFFF33C
SFLASH_MACRO_0_FREE_SFLASH317	0x0FFFF33D
SFLASH_MACRO_0_FREE_SFLASH318	0x0FFFF33E
SFLASH_MACRO_0_FREE_SFLASH319	0x0FFFF33F
SFLASH_MACRO_0_FREE_SFLASH320	0x0FFFF340
SFLASH_MACRO_0_FREE_SFLASH321	0x0FFFF341
SFLASH_MACRO_0_FREE_SFLASH322	0x0FFFF342
SFLASH_MACRO_0_FREE_SFLASH323	0x0FFFF343
SFLASH_MACRO_0_FREE_SFLASH324	0x0FFFF344
SFLASH_MACRO_0_FREE_SFLASH325	0x0FFFF345
SFLASH_MACRO_0_FREE_SFLASH326	0x0FFFF346
SFLASH_MACRO_0_FREE_SFLASH327	0x0FFFF347
SFLASH_MACRO_0_FREE_SFLASH328	0x0FFFF348
SFLASH_MACRO_0_FREE_SFLASH329	0x0FFFF349
SFLASH_MACRO_0_FREE_SFLASH330	0x0FFFF34A
SFLASH_MACRO_0_FREE_SFLASH331	0x0FFFF34B
SFLASH_MACRO_0_FREE_SFLASH332	0x0FFFF34C
SFLASH_MACRO_0_FREE_SFLASH333	0x0FFFF34D
SFLASH_MACRO_0_FREE_SFLASH334	0x0FFFF34E
SFLASH_MACRO_0_FREE_SFLASH335	0x0FFFF34F
SFLASH_MACRO_0_FREE_SFLASH336	0x0FFFF350
SFLASH_MACRO_0_FREE_SFLASH337	0x0FFFF351
SFLASH_MACRO_0_FREE_SFLASH338	0x0FFFF352
SFLASH_MACRO_0_FREE_SFLASH339	0x0FFFF353
SFLASH_MACRO_0_FREE_SFLASH340	0x0FFFF354
SFLASH_MACRO_0_FREE_SFLASH341	0x0FFFF355
SFLASH_MACRO_0_FREE_SFLASH342	0x0FFFF356
SFLASH_MACRO_0_FREE_SFLASH343	0x0FFFF357
SFLASH_MACRO_0_FREE_SFLASH344	0x0FFFF358
SFLASH_MACRO_0_FREE_SFLASH345	0x0FFFF359
SFLASH_MACRO_0_FREE_SFLASH346	0x0FFFF35A
SFLASH_MACRO_0_FREE_SFLASH347	0x0FFFF35B
SFLASH_MACRO_0_FREE_SFLASH348	0x0FFFF35C

Register Name	Address
SFLASH_MACRO_0_FREE_SFLASH349	0x0FFFF35D
SFLASH_MACRO_0_FREE_SFLASH350	0x0FFFF35E
SFLASH_MACRO_0_FREE_SFLASH351	0x0FFFF35F
SFLASH_MACRO_0_FREE_SFLASH352	0x0FFFF360
SFLASH_MACRO_0_FREE_SFLASH353	0x0FFFF361
SFLASH_MACRO_0_FREE_SFLASH354	0x0FFFF362
SFLASH_MACRO_0_FREE_SFLASH355	0x0FFFF363
SFLASH_MACRO_0_FREE_SFLASH356	0x0FFFF364
SFLASH_MACRO_0_FREE_SFLASH357	0x0FFFF365
SFLASH_MACRO_0_FREE_SFLASH358	0x0FFFF366
SFLASH_MACRO_0_FREE_SFLASH359	0x0FFFF367
SFLASH_MACRO_0_FREE_SFLASH360	0x0FFFF368
SFLASH_MACRO_0_FREE_SFLASH361	0x0FFFF369
SFLASH_MACRO_0_FREE_SFLASH362	0x0FFFF36A
SFLASH_MACRO_0_FREE_SFLASH363	0x0FFFF36B
SFLASH_MACRO_0_FREE_SFLASH364	0x0FFFF36C
SFLASH_MACRO_0_FREE_SFLASH365	0x0FFFF36D
SFLASH_MACRO_0_FREE_SFLASH366	0x0FFFF36E
SFLASH_MACRO_0_FREE_SFLASH367	0x0FFFF36F
SFLASH_MACRO_0_FREE_SFLASH368	0x0FFFF370
SFLASH_MACRO_0_FREE_SFLASH369	0x0FFFF371
SFLASH_MACRO_0_FREE_SFLASH370	0x0FFFF372
SFLASH_MACRO_0_FREE_SFLASH371	0x0FFFF373
SFLASH_MACRO_0_FREE_SFLASH372	0x0FFFF374
SFLASH_MACRO_0_FREE_SFLASH373	0x0FFFF375
SFLASH_MACRO_0_FREE_SFLASH374	0x0FFFF376
SFLASH_MACRO_0_FREE_SFLASH375	0x0FFFF377
SFLASH_MACRO_0_FREE_SFLASH376	0x0FFFF378
SFLASH_MACRO_0_FREE_SFLASH377	0x0FFFF379
SFLASH_MACRO_0_FREE_SFLASH378	0x0FFFF37A
SFLASH_MACRO_0_FREE_SFLASH379	0x0FFFF37B
SFLASH_MACRO_0_FREE_SFLASH380	0x0FFFF37C
SFLASH_MACRO_0_FREE_SFLASH381	0x0FFFF37D
SFLASH_MACRO_0_FREE_SFLASH382	0x0FFFF37E
SFLASH_MACRO_0_FREE_SFLASH383	0x0FFFF37F
SFLASH_MACRO_0_FREE_SFLASH384	0x0FFFF380
SFLASH_MACRO_0_FREE_SFLASH385	0x0FFFF381
SFLASH_MACRO_0_FREE_SFLASH386	0x0FFFF382
SFLASH_MACRO_0_FREE_SFLASH387	0x0FFFF383
SFLASH_MACRO_0_FREE_SFLASH388	0x0FFFF384
SFLASH_MACRO_0_FREE_SFLASH389	0x0FFFF385
SFLASH_MACRO_0_FREE_SFLASH390	0x0FFFF386

Register Name	Address
SFLASH_MACRO_0_FREE_SFLASH391	0x0FFFF387
SFLASH_MACRO_0_FREE_SFLASH392	0x0FFFF388
SFLASH_MACRO_0_FREE_SFLASH393	0x0FFFF389
SFLASH_MACRO_0_FREE_SFLASH394	0x0FFFF38A
SFLASH_MACRO_0_FREE_SFLASH395	0x0FFFF38B
SFLASH_MACRO_0_FREE_SFLASH396	0x0FFFF38C
SFLASH_MACRO_0_FREE_SFLASH397	0x0FFFF38D
SFLASH_MACRO_0_FREE_SFLASH398	0x0FFFF38E
SFLASH_MACRO_0_FREE_SFLASH399	0x0FFFF38F
SFLASH_MACRO_0_FREE_SFLASH400	0x0FFFF390
SFLASH_MACRO_0_FREE_SFLASH401	0x0FFFF391
SFLASH_MACRO_0_FREE_SFLASH402	0x0FFFF392
SFLASH_MACRO_0_FREE_SFLASH403	0x0FFFF393
SFLASH_MACRO_0_FREE_SFLASH404	0x0FFFF394
SFLASH_MACRO_0_FREE_SFLASH405	0x0FFFF395
SFLASH_MACRO_0_FREE_SFLASH406	0x0FFFF396
SFLASH_MACRO_0_FREE_SFLASH407	0x0FFFF397
SFLASH_MACRO_0_FREE_SFLASH408	0x0FFFF398
SFLASH_MACRO_0_FREE_SFLASH409	0x0FFFF399
SFLASH_MACRO_0_FREE_SFLASH410	0x0FFFF39A
SFLASH_MACRO_0_FREE_SFLASH411	0x0FFFF39B
SFLASH_MACRO_0_FREE_SFLASH412	0x0FFFF39C
SFLASH_MACRO_0_FREE_SFLASH413	0x0FFFF39D
SFLASH_MACRO_0_FREE_SFLASH414	0x0FFFF39E
SFLASH_MACRO_0_FREE_SFLASH415	0x0FFFF39F
SFLASH_MACRO_0_FREE_SFLASH416	0x0FFFF3A0
SFLASH_MACRO_0_FREE_SFLASH417	0x0FFFF3A1
SFLASH_MACRO_0_FREE_SFLASH418	0x0FFFF3A2
SFLASH_MACRO_0_FREE_SFLASH419	0x0FFFF3A3
SFLASH_MACRO_0_FREE_SFLASH420	0x0FFFF3A4
SFLASH_MACRO_0_FREE_SFLASH421	0x0FFFF3A5
SFLASH_MACRO_0_FREE_SFLASH422	0x0FFFF3A6
SFLASH_MACRO_0_FREE_SFLASH423	0x0FFFF3A7
SFLASH_MACRO_0_FREE_SFLASH424	0x0FFFF3A8
SFLASH_MACRO_0_FREE_SFLASH425	0x0FFFF3A9
SFLASH_MACRO_0_FREE_SFLASH426	0x0FFFF3AA
SFLASH_MACRO_0_FREE_SFLASH427	0x0FFFF3AB
SFLASH_MACRO_0_FREE_SFLASH428	0x0FFFF3AC
SFLASH_MACRO_0_FREE_SFLASH429	0x0FFFF3AD
SFLASH_MACRO_0_FREE_SFLASH430	0x0FFFF3AE
SFLASH_MACRO_0_FREE_SFLASH431	0x0FFFF3AF
SFLASH_MACRO_0_FREE_SFLASH432	0x0FFFF3B0

Register Name	Address
SFLASH_MACRO_0_FREE_SFLASH433	0x0FFFF3B1
SFLASH_MACRO_0_FREE_SFLASH434	0x0FFFF3B2
SFLASH_MACRO_0_FREE_SFLASH435	0x0FFFF3B3
SFLASH_MACRO_0_FREE_SFLASH436	0x0FFFF3B4
SFLASH_MACRO_0_FREE_SFLASH437	0x0FFFF3B5
SFLASH_MACRO_0_FREE_SFLASH438	0x0FFFF3B6
SFLASH_MACRO_0_FREE_SFLASH439	0x0FFFF3B7
SFLASH_MACRO_0_FREE_SFLASH440	0x0FFFF3B8
SFLASH_MACRO_0_FREE_SFLASH441	0x0FFFF3B9
SFLASH_MACRO_0_FREE_SFLASH442	0x0FFFF3BA
SFLASH_MACRO_0_FREE_SFLASH443	0x0FFFF3BB
SFLASH_MACRO_0_FREE_SFLASH444	0x0FFFF3BC
SFLASH_MACRO_0_FREE_SFLASH445	0x0FFFF3BD
SFLASH_MACRO_0_FREE_SFLASH446	0x0FFFF3BE
SFLASH_MACRO_0_FREE_SFLASH447	0x0FFFF3BF
SFLASH_MACRO_0_FREE_SFLASH448	0x0FFFF3C0
SFLASH_MACRO_0_FREE_SFLASH449	0x0FFFF3C1
SFLASH_MACRO_0_FREE_SFLASH450	0x0FFFF3C2
SFLASH_MACRO_0_FREE_SFLASH451	0x0FFFF3C3
SFLASH_MACRO_0_FREE_SFLASH452	0x0FFFF3C4
SFLASH_MACRO_0_FREE_SFLASH453	0x0FFFF3C5
SFLASH_MACRO_0_FREE_SFLASH454	0x0FFFF3C6
SFLASH_MACRO_0_FREE_SFLASH455	0x0FFFF3C7
SFLASH_MACRO_0_FREE_SFLASH456	0x0FFFF3C8
SFLASH_MACRO_0_FREE_SFLASH457	0x0FFFF3C9
SFLASH_MACRO_0_FREE_SFLASH458	0x0FFFF3CA
SFLASH_MACRO_0_FREE_SFLASH459	0x0FFFF3CB
SFLASH_MACRO_0_FREE_SFLASH460	0x0FFFF3CC
SFLASH_MACRO_0_FREE_SFLASH461	0x0FFFF3CD
SFLASH_MACRO_0_FREE_SFLASH462	0x0FFFF3CE
SFLASH_MACRO_0_FREE_SFLASH463	0x0FFFF3CF
SFLASH_MACRO_0_FREE_SFLASH464	0x0FFFF3D0
SFLASH_MACRO_0_FREE_SFLASH465	0x0FFFF3D1
SFLASH_MACRO_0_FREE_SFLASH466	0x0FFFF3D2
SFLASH_MACRO_0_FREE_SFLASH467	0x0FFFF3D3
SFLASH_MACRO_0_FREE_SFLASH468	0x0FFFF3D4
SFLASH_MACRO_0_FREE_SFLASH469	0x0FFFF3D5
SFLASH_MACRO_0_FREE_SFLASH470	0x0FFFF3D6
SFLASH_MACRO_0_FREE_SFLASH471	0x0FFFF3D7
SFLASH_MACRO_0_FREE_SFLASH472	0x0FFFF3D8
SFLASH_MACRO_0_FREE_SFLASH473	0x0FFFF3D9
SFLASH_MACRO_0_FREE_SFLASH474	0x0FFFF3DA

Register Name	Address
SFLASH_MACRO_0_FREE_SFLASH475	0x0FFFF3DB
SFLASH_MACRO_0_FREE_SFLASH476	0x0FFFF3DC
SFLASH_MACRO_0_FREE_SFLASH477	0x0FFFF3DD
SFLASH_MACRO_0_FREE_SFLASH478	0x0FFFF3DE
SFLASH_MACRO_0_FREE_SFLASH479	0x0FFFF3DF
SFLASH_MACRO_0_FREE_SFLASH480	0x0FFFF3E0
SFLASH_MACRO_0_FREE_SFLASH481	0x0FFFF3E1
SFLASH_MACRO_0_FREE_SFLASH482	0x0FFFF3E2
SFLASH_MACRO_0_FREE_SFLASH483	0x0FFFF3E3
SFLASH_MACRO_0_FREE_SFLASH484	0x0FFFF3E4
SFLASH_MACRO_0_FREE_SFLASH485	0x0FFFF3E5
SFLASH_MACRO_0_FREE_SFLASH486	0x0FFFF3E6
SFLASH_MACRO_0_FREE_SFLASH487	0x0FFFF3E7
SFLASH_MACRO_0_FREE_SFLASH488	0x0FFFF3E8
SFLASH_MACRO_0_FREE_SFLASH489	0x0FFFF3E9
SFLASH_MACRO_0_FREE_SFLASH490	0x0FFFF3EA
SFLASH_MACRO_0_FREE_SFLASH491	0x0FFFF3EB
SFLASH_MACRO_0_FREE_SFLASH492	0x0FFFF3EC
SFLASH_MACRO_0_FREE_SFLASH493	0x0FFFF3ED
SFLASH_MACRO_0_FREE_SFLASH494	0x0FFFF3EE
SFLASH_MACRO_0_FREE_SFLASH495	0x0FFFF3EF
SFLASH_MACRO_0_FREE_SFLASH496	0x0FFFF3F0
SFLASH_MACRO_0_FREE_SFLASH497	0x0FFFF3F1
SFLASH_MACRO_0_FREE_SFLASH498	0x0FFFF3F2
SFLASH_MACRO_0_FREE_SFLASH499	0x0FFFF3F3
SFLASH_MACRO_0_FREE_SFLASH500	0x0FFFF3F4
SFLASH_MACRO_0_FREE_SFLASH501	0x0FFFF3F5
SFLASH_MACRO_0_FREE_SFLASH502	0x0FFFF3F6
SFLASH_MACRO_0_FREE_SFLASH503	0x0FFFF3F7
SFLASH_MACRO_0_FREE_SFLASH504	0x0FFFF3F8
SFLASH_MACRO_0_FREE_SFLASH505	0x0FFFF3F9
SFLASH_MACRO_0_FREE_SFLASH506	0x0FFFF3FA
SFLASH_MACRO_0_FREE_SFLASH507	0x0FFFF3FB
SFLASH_MACRO_0_FREE_SFLASH508	0x0FFFF3FC
SFLASH_MACRO_0_FREE_SFLASH509	0x0FFFF3FD
SFLASH_MACRO_0_FREE_SFLASH510	0x0FFFF3FE
SFLASH_MACRO_0_FREE_SFLASH511	0x0FFFF3FF
SFLASH_ALT_PROT_ROW0	0x0FFFF400
SFLASH_ALT_PROT_ROW1	0x0FFFF401
SFLASH_ALT_PROT_ROW2	0x0FFFF402
SFLASH_ALT_PROT_ROW3	0x0FFFF403
SFLASH_ALT_PROT_ROW4	0x0FFFF404

Register Name	Address
SFLASH_ALT_PROT_ROW5	0x0FFFF405
SFLASH_ALT_PROT_ROW6	0x0FFFF406
SFLASH_ALT_PROT_ROW7	0x0FFFF407
SFLASH_ALT_PROT_ROW8	0x0FFFF408
SFLASH_ALT_PROT_ROW9	0x0FFFF409
SFLASH_ALT_PROT_ROW10	0x0FFFF40A
SFLASH_ALT_PROT_ROW11	0x0FFFF40B
SFLASH_ALT_PROT_ROW12	0x0FFFF40C
SFLASH_ALT_PROT_ROW13	0x0FFFF40D
SFLASH_ALT_PROT_ROW14	0x0FFFF40E
SFLASH_ALT_PROT_ROW15	0x0FFFF40F
SFLASH_ALT_PROT_ROW16	0x0FFFF410
SFLASH_ALT_PROT_ROW17	0x0FFFF411
SFLASH_ALT_PROT_ROW18	0x0FFFF412
SFLASH_ALT_PROT_ROW19	0x0FFFF413
SFLASH_ALT_PROT_ROW20	0x0FFFF414
SFLASH_ALT_PROT_ROW21	0x0FFFF415
SFLASH_ALT_PROT_ROW22	0x0FFFF416
SFLASH_ALT_PROT_ROW23	0x0FFFF417
SFLASH_ALT_PROT_ROW24	0x0FFFF418
SFLASH_ALT_PROT_ROW25	0x0FFFF419
SFLASH_ALT_PROT_ROW26	0x0FFFF41A
SFLASH_ALT_PROT_ROW27	0x0FFFF41B
SFLASH_ALT_PROT_ROW28	0x0FFFF41C
SFLASH_ALT_PROT_ROW29	0x0FFFF41D
SFLASH_ALT_PROT_ROW30	0x0FFFF41E
SFLASH_ALT_PROT_ROW31	0x0FFFF41F
SFLASH_ALT_PROT_ROW32	0x0FFFF420
SFLASH_ALT_PROT_ROW33	0x0FFFF421
SFLASH_ALT_PROT_ROW34	0x0FFFF422
SFLASH_ALT_PROT_ROW35	0x0FFFF423
SFLASH_ALT_PROT_ROW36	0x0FFFF424
SFLASH_ALT_PROT_ROW37	0x0FFFF425
SFLASH_ALT_PROT_ROW38	0x0FFFF426
SFLASH_ALT_PROT_ROW39	0x0FFFF427
SFLASH_ALT_PROT_ROW40	0x0FFFF428
SFLASH_ALT_PROT_ROW41	0x0FFFF429
SFLASH_ALT_PROT_ROW42	0x0FFFF42A
SFLASH_ALT_PROT_ROW43	0x0FFFF42B
SFLASH_ALT_PROT_ROW44	0x0FFFF42C
SFLASH_ALT_PROT_ROW45	0x0FFFF42D
SFLASH_ALT_PROT_ROW46	0x0FFFF42E

Register Name	Address
SFLASH_ALT_PROT_ROW47	0x0FFFF42F
SFLASH_ALT_PROT_ROW48	0x0FFFF430
SFLASH_ALT_PROT_ROW49	0x0FFFF431
SFLASH_ALT_PROT_ROW50	0x0FFFF432
SFLASH_ALT_PROT_ROW51	0x0FFFF433
SFLASH_ALT_PROT_ROW52	0x0FFFF434
SFLASH_ALT_PROT_ROW53	0x0FFFF435
SFLASH_ALT_PROT_ROW54	0x0FFFF436
SFLASH_ALT_PROT_ROW55	0x0FFFF437
SFLASH_ALT_PROT_ROW56	0x0FFFF438
SFLASH_ALT_PROT_ROW57	0x0FFFF439
SFLASH_ALT_PROT_ROW58	0x0FFFF43A
SFLASH_ALT_PROT_ROW59	0x0FFFF43B
SFLASH_ALT_PROT_ROW60	0x0FFFF43C
SFLASH_ALT_PROT_ROW61	0x0FFFF43D
SFLASH_ALT_PROT_ROW62	0x0FFFF43E
SFLASH_ALT_PROT_ROW63	0x0FFFF43F
SFLASH_ALT_PROT_ROW64	0x0FFFF440
SFLASH_ALT_PROT_ROW65	0x0FFFF441
SFLASH_ALT_PROT_ROW66	0x0FFFF442
SFLASH_ALT_PROT_ROW67	0x0FFFF443
SFLASH_ALT_PROT_ROW68	0x0FFFF444
SFLASH_ALT_PROT_ROW69	0x0FFFF445
SFLASH_ALT_PROT_ROW70	0x0FFFF446
SFLASH_ALT_PROT_ROW71	0x0FFFF447
SFLASH_ALT_PROT_ROW72	0x0FFFF448
SFLASH_ALT_PROT_ROW73	0x0FFFF449
SFLASH_ALT_PROT_ROW74	0x0FFFF44A
SFLASH_ALT_PROT_ROW75	0x0FFFF44B
SFLASH_ALT_PROT_ROW76	0x0FFFF44C
SFLASH_ALT_PROT_ROW77	0x0FFFF44D
SFLASH_ALT_PROT_ROW78	0x0FFFF44E
SFLASH_ALT_PROT_ROW79	0x0FFFF44F
SFLASH_ALT_PROT_ROW80	0x0FFFF450
SFLASH_ALT_PROT_ROW81	0x0FFFF451
SFLASH_ALT_PROT_ROW82	0x0FFFF452
SFLASH_ALT_PROT_ROW83	0x0FFFF453
SFLASH_ALT_PROT_ROW84	0x0FFFF454
SFLASH_ALT_PROT_ROW85	0x0FFFF455
SFLASH_ALT_PROT_ROW86	0x0FFFF456
SFLASH_ALT_PROT_ROW87	0x0FFFF457
SFLASH_ALT_PROT_ROW88	0x0FFFF458

Register Name	Address
SFLASH_ALT_PROT_ROW89	0x0FFFF459
SFLASH_ALT_PROT_ROW90	0x0FFFF45A
SFLASH_ALT_PROT_ROW91	0x0FFFF45B
SFLASH_ALT_PROT_ROW92	0x0FFFF45C
SFLASH_ALT_PROT_ROW93	0x0FFFF45D
SFLASH_ALT_PROT_ROW94	0x0FFFF45E
SFLASH_ALT_PROT_ROW95	0x0FFFF45F
SFLASH_ALT_PROT_ROW96	0x0FFFF460
SFLASH_ALT_PROT_ROW97	0x0FFFF461
SFLASH_ALT_PROT_ROW98	0x0FFFF462
SFLASH_ALT_PROT_ROW99	0x0FFFF463
SFLASH_ALT_PROT_ROW100	0x0FFFF464
SFLASH_ALT_PROT_ROW101	0x0FFFF465
SFLASH_ALT_PROT_ROW102	0x0FFFF466
SFLASH_ALT_PROT_ROW103	0x0FFFF467
SFLASH_ALT_PROT_ROW104	0x0FFFF468
SFLASH_ALT_PROT_ROW105	0x0FFFF469
SFLASH_ALT_PROT_ROW106	0x0FFFF46A
SFLASH_ALT_PROT_ROW107	0x0FFFF46B
SFLASH_ALT_PROT_ROW108	0x0FFFF46C
SFLASH_ALT_PROT_ROW109	0x0FFFF46D
SFLASH_ALT_PROT_ROW110	0x0FFFF46E
SFLASH_ALT_PROT_ROW111	0x0FFFF46F
SFLASH_ALT_PROT_ROW112	0x0FFFF470
SFLASH_ALT_PROT_ROW113	0x0FFFF471
SFLASH_ALT_PROT_ROW114	0x0FFFF472
SFLASH_ALT_PROT_ROW115	0x0FFFF473
SFLASH_ALT_PROT_ROW116	0x0FFFF474
SFLASH_ALT_PROT_ROW117	0x0FFFF475
SFLASH_ALT_PROT_ROW118	0x0FFFF476
SFLASH_ALT_PROT_ROW119	0x0FFFF477
SFLASH_ALT_PROT_ROW120	0x0FFFF478
SFLASH_ALT_PROT_ROW121	0x0FFFF479
SFLASH_ALT_PROT_ROW122	0x0FFFF47A
SFLASH_ALT_PROT_ROW123	0x0FFFF47B
SFLASH_ALT_PROT_ROW124	0x0FFFF47C
SFLASH_ALT_PROT_ROW125	0x0FFFF47D
SFLASH_ALT_PROT_ROW126	0x0FFFF47E
SFLASH_ALT_PROT_ROW127	0x0FFFF47F
SFLASH_ALT_PROT_ROW128	0x0FFFF480
SFLASH_ALT_PROT_ROW129	0x0FFFF481
SFLASH_ALT_PROT_ROW130	0x0FFFF482

Register Name	Address
SFLASH_ALT_PROT_ROW131	0x0FFFF483
SFLASH_ALT_PROT_ROW132	0x0FFFF484
SFLASH_ALT_PROT_ROW133	0x0FFFF485
SFLASH_ALT_PROT_ROW134	0x0FFFF486
SFLASH_ALT_PROT_ROW135	0x0FFFF487
SFLASH_ALT_PROT_ROW136	0x0FFFF488
SFLASH_ALT_PROT_ROW137	0x0FFFF489
SFLASH_ALT_PROT_ROW138	0x0FFFF48A
SFLASH_ALT_PROT_ROW139	0x0FFFF48B
SFLASH_ALT_PROT_ROW140	0x0FFFF48C
SFLASH_ALT_PROT_ROW141	0x0FFFF48D
SFLASH_ALT_PROT_ROW142	0x0FFFF48E
SFLASH_ALT_PROT_ROW143	0x0FFFF48F
SFLASH_ALT_PROT_ROW144	0x0FFFF490
SFLASH_ALT_PROT_ROW145	0x0FFFF491
SFLASH_ALT_PROT_ROW146	0x0FFFF492
SFLASH_ALT_PROT_ROW147	0x0FFFF493
SFLASH_ALT_PROT_ROW148	0x0FFFF494
SFLASH_ALT_PROT_ROW149	0x0FFFF495
SFLASH_ALT_PROT_ROW150	0x0FFFF496
SFLASH_ALT_PROT_ROW151	0x0FFFF497
SFLASH_ALT_PROT_ROW152	0x0FFFF498
SFLASH_ALT_PROT_ROW153	0x0FFFF499
SFLASH_ALT_PROT_ROW154	0x0FFFF49A
SFLASH_ALT_PROT_ROW155	0x0FFFF49B
SFLASH_ALT_PROT_ROW156	0x0FFFF49C
SFLASH_ALT_PROT_ROW157	0x0FFFF49D
SFLASH_ALT_PROT_ROW158	0x0FFFF49E
SFLASH_ALT_PROT_ROW159	0x0FFFF49F
SFLASH_ALT_PROT_ROW160	0x0FFFF4A0
SFLASH_ALT_PROT_ROW161	0x0FFFF4A1
SFLASH_ALT_PROT_ROW162	0x0FFFF4A2
SFLASH_ALT_PROT_ROW163	0x0FFFF4A3
SFLASH_ALT_PROT_ROW164	0x0FFFF4A4
SFLASH_ALT_PROT_ROW165	0x0FFFF4A5
SFLASH_ALT_PROT_ROW166	0x0FFFF4A6
SFLASH_ALT_PROT_ROW167	0x0FFFF4A7
SFLASH_ALT_PROT_ROW168	0x0FFFF4A8
SFLASH_ALT_PROT_ROW169	0x0FFFF4A9
SFLASH_ALT_PROT_ROW170	0x0FFFF4AA
SFLASH_ALT_PROT_ROW171	0x0FFFF4AB
SFLASH_ALT_PROT_ROW172	0x0FFFF4AC

Register Name	Address
SFLASH_ALT_PROT_ROW173	0x0FFFF4AD
SFLASH_ALT_PROT_ROW174	0x0FFFF4AE
SFLASH_ALT_PROT_ROW175	0x0FFFF4AF
SFLASH_ALT_PROT_ROW176	0x0FFFF4B0
SFLASH_ALT_PROT_ROW177	0x0FFFF4B1
SFLASH_ALT_PROT_ROW178	0x0FFFF4B2
SFLASH_ALT_PROT_ROW179	0x0FFFF4B3
SFLASH_ALT_PROT_ROW180	0x0FFFF4B4
SFLASH_ALT_PROT_ROW181	0x0FFFF4B5
SFLASH_ALT_PROT_ROW182	0x0FFFF4B6
SFLASH_ALT_PROT_ROW183	0x0FFFF4B7
SFLASH_ALT_PROT_ROW184	0x0FFFF4B8
SFLASH_ALT_PROT_ROW185	0x0FFFF4B9
SFLASH_ALT_PROT_ROW186	0x0FFFF4BA
SFLASH_ALT_PROT_ROW187	0x0FFFF4BB
SFLASH_ALT_PROT_ROW188	0x0FFFF4BC
SFLASH_ALT_PROT_ROW189	0x0FFFF4BD
SFLASH_ALT_PROT_ROW190	0x0FFFF4BE
SFLASH_ALT_PROT_ROW191	0x0FFFF4BF
SFLASH_ALT_PROT_ROW192	0x0FFFF4C0
SFLASH_ALT_PROT_ROW193	0x0FFFF4C1
SFLASH_ALT_PROT_ROW194	0x0FFFF4C2
SFLASH_ALT_PROT_ROW195	0x0FFFF4C3
SFLASH_ALT_PROT_ROW196	0x0FFFF4C4
SFLASH_ALT_PROT_ROW197	0x0FFFF4C5
SFLASH_ALT_PROT_ROW198	0x0FFFF4C6
SFLASH_ALT_PROT_ROW199	0x0FFFF4C7
SFLASH_ALT_PROT_ROW200	0x0FFFF4C8
SFLASH_ALT_PROT_ROW201	0x0FFFF4C9
SFLASH_ALT_PROT_ROW202	0x0FFFF4CA
SFLASH_ALT_PROT_ROW203	0x0FFFF4CB
SFLASH_ALT_PROT_ROW204	0x0FFFF4CC
SFLASH_ALT_PROT_ROW205	0x0FFFF4CD
SFLASH_ALT_PROT_ROW206	0x0FFFF4CE
SFLASH_ALT_PROT_ROW207	0x0FFFF4CF
SFLASH_ALT_PROT_ROW208	0x0FFFF4D0
SFLASH_ALT_PROT_ROW209	0x0FFFF4D1
SFLASH_ALT_PROT_ROW210	0x0FFFF4D2
SFLASH_ALT_PROT_ROW211	0x0FFFF4D3
SFLASH_ALT_PROT_ROW212	0x0FFFF4D4
SFLASH_ALT_PROT_ROW213	0x0FFFF4D5
SFLASH_ALT_PROT_ROW214	0x0FFFF4D6

Register Name	Address
SFLASH_ALT_PROT_ROW215	0x0FFFF4D7
SFLASH_ALT_PROT_ROW216	0x0FFFF4D8
SFLASH_ALT_PROT_ROW217	0x0FFFF4D9
SFLASH_ALT_PROT_ROW218	0x0FFFF4DA
SFLASH_ALT_PROT_ROW219	0x0FFFF4DB
SFLASH_ALT_PROT_ROW220	0x0FFFF4DC
SFLASH_ALT_PROT_ROW221	0x0FFFF4DD
SFLASH_ALT_PROT_ROW222	0x0FFFF4DE
SFLASH_ALT_PROT_ROW223	0x0FFFF4DF
SFLASH_ALT_PROT_ROW224	0x0FFFF4E0
SFLASH_ALT_PROT_ROW225	0x0FFFF4E1
SFLASH_ALT_PROT_ROW226	0x0FFFF4E2
SFLASH_ALT_PROT_ROW227	0x0FFFF4E3
SFLASH_ALT_PROT_ROW228	0x0FFFF4E4
SFLASH_ALT_PROT_ROW229	0x0FFFF4E5
SFLASH_ALT_PROT_ROW230	0x0FFFF4E6
SFLASH_ALT_PROT_ROW231	0x0FFFF4E7
SFLASH_ALT_PROT_ROW232	0x0FFFF4E8
SFLASH_ALT_PROT_ROW233	0x0FFFF4E9
SFLASH_ALT_PROT_ROW234	0x0FFFF4EA
SFLASH_ALT_PROT_ROW235	0x0FFFF4EB
SFLASH_ALT_PROT_ROW236	0x0FFFF4EC
SFLASH_ALT_PROT_ROW237	0x0FFFF4ED
SFLASH_ALT_PROT_ROW238	0x0FFFF4EE
SFLASH_ALT_PROT_ROW239	0x0FFFF4EF
SFLASH_ALT_PROT_ROW240	0x0FFFF4F0
SFLASH_ALT_PROT_ROW241	0x0FFFF4F1
SFLASH_ALT_PROT_ROW242	0x0FFFF4F2
SFLASH_ALT_PROT_ROW243	0x0FFFF4F3
SFLASH_ALT_PROT_ROW244	0x0FFFF4F4
SFLASH_ALT_PROT_ROW245	0x0FFFF4F5
SFLASH_ALT_PROT_ROW246	0x0FFFF4F6
SFLASH_ALT_PROT_ROW247	0x0FFFF4F7
SFLASH_ALT_PROT_ROW248	0x0FFFF4F8
SFLASH_ALT_PROT_ROW249	0x0FFFF4F9
SFLASH_ALT_PROT_ROW250	0x0FFFF4FA
SFLASH_ALT_PROT_ROW251	0x0FFFF4FB
SFLASH_ALT_PROT_ROW252	0x0FFFF4FC
SFLASH_ALT_PROT_ROW253	0x0FFFF4FD
SFLASH_ALT_PROT_ROW254	0x0FFFF4FE
SFLASH_ALT_PROT_ROW255	0x0FFFF4FF
SFLASH_ALT_PP	0x0FFFF5A0

Register Name	Address
SFLASH_ALT_E	0x0FFFF5A4
SFLASH_ALT_P	0x0FFFF5A8
SFLASH_ALT_EA_E	0x0FFFF5AC
SFLASH_ALT_EA_P	0x0FFFF5B0
SFLASH_ALT_ES_E	0x0FFFF5B4
SFLASH_ALT_ES_P_EO	0x0FFFF5B8
SFLASH_ALT_E_VCTAT	0x0FFFF5BC
SFLASH_ALT_P_VCTAT	0x0FFFF5BD

29.1.1 SFLASH_PROT_ROW0

Per Page Write Protection

Address: 0x0FFFF000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.2 SFLASH_PROT_ROW1

Per Page Write Protection

Address: 0x0FFFF001

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.3 SFLASH_PROT_ROW2

Per Page Write Protection

Address: 0x0FFFF002

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.4 SFLASH_PROT_ROW3

Per Page Write Protection

Address: 0x0FFFF003

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.5 SFLASH_PROT_ROW4

Per Page Write Protection

Address: 0x0FFFF004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.6 SFLASH_PROT_ROW5

Per Page Write Protection

Address: 0x0FFFF005

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.7 SFLASH_PROT_ROW6

Per Page Write Protection

Address: 0x0FFFF006

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.8 SFLASH_PROT_ROW7

Per Page Write Protection

Address: 0x0FFFF007

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.9 SFLASH_PROT_ROW8

Per Page Write Protection

Address: 0x0FFFF008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.10 SFLASH_PROT_ROW9

Per Page Write Protection

Address: 0x0FFFF009

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.11 SFLASH_PROT_ROW10

Per Page Write Protection

Address: 0x0FFFF00A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.12 SFLASH_PROT_ROW11

Per Page Write Protection

Address: 0x0FFFF00B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.13 SFLASH_PROT_ROW12

Per Page Write Protection

Address: 0x0FFFF00C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.14 SFLASH_PROT_ROW13

Per Page Write Protection

Address: 0x0FFFF00D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.15 SFLASH_PROT_ROW14

Per Page Write Protection

Address: 0x0FFFF00E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.16 SFLASH_PROT_ROW15

Per Page Write Protection

Address: 0x0FFFF00F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.17 SFLASH_PROT_ROW16

Per Page Write Protection

Address: 0x0FFFF010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.18 SFLASH_PROT_ROW17

Per Page Write Protection

Address: 0x0FFFF011

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.19 SFLASH_PROT_ROW18

Per Page Write Protection

Address: 0x0FFFF012

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.20 SFLASH_PROT_ROW19

Per Page Write Protection

Address: 0x0FFFF013

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.21 SFLASH_PROT_ROW20

Per Page Write Protection

Address: 0x0FFFF014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.22 SFLASH_PROT_ROW21

Per Page Write Protection

Address: 0x0FFFF015

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.23 SFLASH_PROT_ROW22

Per Page Write Protection

Address: 0x0FFFF016

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.24 SFLASH_PROT_ROW23

Per Page Write Protection

Address: 0x0FFFF017

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.25 SFLASH_PROT_ROW24

Per Page Write Protection

Address: 0x0FFFF018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.26 SFLASH_PROT_ROW25

Per Page Write Protection

Address: 0x0FFFF019

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.27 SFLASH_PROT_ROW26

Per Page Write Protection

Address: 0x0FFFF01A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.28 SFLASH_PROT_ROW27

Per Page Write Protection

Address: 0x0FFFF01B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.29 SFLASH_PROT_ROW28

Per Page Write Protection

Address: 0x0FFFF01C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.30 SFLASH_PROT_ROW29

Per Page Write Protection

Address: 0x0FFFF01D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.31 SFLASH_PROT_ROW30

Per Page Write Protection

Address: 0x0FFFF01E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.32 SFLASH_PROT_ROW31

Per Page Write Protection

Address: 0x0FFFF01F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.33 SFLASH_PROT_ROW32

Per Page Write Protection

Address: 0x0FFFF020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.34 SFLASH_PROT_ROW33

Per Page Write Protection

Address: 0x0FFFF021

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.35 SFLASH_PROT_ROW34

Per Page Write Protection

Address: 0x0FFFF022

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.36 SFLASH_PROT_ROW35

Per Page Write Protection

Address: 0x0FFFF023

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.37 SFLASH_PROT_ROW36

Per Page Write Protection

Address: 0x0FFFF024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.38 SFLASH_PROT_ROW37

Per Page Write Protection

Address: 0x0FFFF025

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.39 SFLASH_PROT_ROW38

Per Page Write Protection

Address: 0x0FFFF026

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.40 SFLASH_PROT_ROW39

Per Page Write Protection

Address: 0x0FFFF027

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.41 SFLASH_PROT_ROW40

Per Page Write Protection

Address: 0x0FFFF028

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.42 SFLASH_PROT_ROW41

Per Page Write Protection

Address: 0x0FFFF029

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.43 SFLASH_PROT_ROW42

Per Page Write Protection

Address: 0x0FFFF02A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.44 SFLASH_PROT_ROW43

Per Page Write Protection

Address: 0x0FFFF02B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.45 SFLASH_PROT_ROW44

Per Page Write Protection

Address: 0x0FFFF02C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.46 SFLASH_PROT_ROW45

Per Page Write Protection

Address: 0x0FFFF02D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.47 SFLASH_PROT_ROW46

Per Page Write Protection

Address: 0x0FFFF02E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.48 SFLASH_PROT_ROW47

Per Page Write Protection

Address: 0x0FFFF02F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.49 SFLASH_PROT_ROW48

Per Page Write Protection

Address: 0x0FFFF030

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.50 SFLASH_PROT_ROW49

Per Page Write Protection

Address: 0x0FFFF031

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.51 SFLASH_PROT_ROW50

Per Page Write Protection

Address: 0x0FFFF032

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.52 SFLASH_PROT_ROW51

Per Page Write Protection

Address: 0x0FFFF033

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.53 SFLASH_PROT_ROW52

Per Page Write Protection

Address: 0x0FFFF034

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.54 SFLASH_PROT_ROW53

Per Page Write Protection

Address: 0x0FFFF035

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.55 SFLASH_PROT_ROW54

Per Page Write Protection

Address: 0x0FFFF036

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.56 SFLASH_PROT_ROW55

Per Page Write Protection

Address: 0x0FFFF037

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.57 SFLASH_PROT_ROW56

Per Page Write Protection

Address: 0x0FFFF038

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.58 SFLASH_PROT_ROW57

Per Page Write Protection

Address: 0x0FFFF039

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.59 SFLASH_PROT_ROW58

Per Page Write Protection

Address: 0x0FFFF03A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.60 SFLASH_PROT_ROW59

Per Page Write Protection

Address: 0x0FFFF03B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.61 SFLASH_PROT_ROW60

Per Page Write Protection

Address: 0x0FFFF03C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.62 SFLASH_PROT_ROW61

Per Page Write Protection

Address: 0x0FFFF03D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.63 SFLASH_PROT_ROW62

Per Page Write Protection

Address: 0x0FFFF03E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.64 SFLASH_PROT_ROW63

Per Page Write Protection

Address: 0x0FFFF03F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.65 SFLASH_PROT_PROTECTION

Protection Level

Address: 0x0FFFF07F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	
HW Access	None						None	
Name	None [7:2]						PROT_LEVEL [1:0]	

Bits	Name	Description
1 : 0	PROT_LEVEL	Current Protection Mode - note that encoding is different from CPUSS_PROTECTION !! Default Value: X **0x0: OPEN:** System is in OPEN mode **0x1: VIRGIN:** System is in VIRGIN mode **0x2: PROTECTED:** System is in PROTECTED mode **0x3: KILL:** System is in KILL mode

29.1.66 SFLASH_AV_PAIRS_8B0

8b Addr/Value pair Section

Address: 0x0FFFF080

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.67 SFLASH_AV_PAIRS_8B1

8b Addr/Value pair Section

Address: 0x0FFFF081

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.68 SFLASH_AV_PAIRS_8B2

8b Addr/Value pair Section

Address: 0x0FFFF082

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.69 SFLASH_AV_PAIRS_8B3

8b Addr/Value pair Section

Address: 0x0FFFF083

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.70 SFLASH_AV_PAIRS_8B4

8b Addr/Value pair Section

Address: 0x0FFFF084

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.71 SFLASH_AV_PAIRS_8B5

8b Addr/Value pair Section

Address: 0x0FFFF085

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.72 SFLASH_AV_PAIRS_8B6

8b Addr/Value pair Section

Address: 0x0FFFF086

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.73 SFLASH_AV_PAIRS_8B7

8b Addr/Value pair Section

Address: 0x0FFFF087

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.74 SFLASH_AV_PAIRS_8B8

8b Addr/Value pair Section

Address: 0x0FFFF088

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.75 SFLASH_AV_PAIRS_8B9

8b Addr/Value pair Section

Address: 0x0FFFF089

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.76 SFLASH_AV_PAIRS_8B10

8b Addr/Value pair Section

Address: 0x0FFFF08A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.77 SFLASH_AV_PAIRS_8B11

8b Addr/Value pair Section

Address: 0x0FFFF08B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.78 SFLASH_AV_PAIRS_8B12

8b Addr/Value pair Section

Address: 0x0FFFF08C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.79 SFLASH_AV_PAIRS_8B13

8b Addr/Value pair Section

Address: 0x0FFFF08D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.80 SFLASH_AV_PAIRS_8B14

8b Addr/Value pair Section

Address: 0x0FFFF08E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.81 SFLASH_AV_PAIRS_8B15

8b Addr/Value pair Section

Address: 0x0FFFF08F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.82 SFLASH_AV_PAIRS_8B16

8b Addr/Value pair Section

Address: 0x0FFFF090

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.83 SFLASH_AV_PAIRS_8B17

8b Addr/Value pair Section

Address: 0x0FFFF091

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.84 SFLASH_AV_PAIRS_8B18

8b Addr/Value pair Section

Address: 0x0FFFF092

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.85 SFLASH_AV_PAIRS_8B19

8b Addr/Value pair Section

Address: 0x0FFFF093

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.86 SFLASH_AV_PAIRS_8B20

8b Addr/Value pair Section

Address: 0x0FFFF094

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.87 SFLASH_AV_PAIRS_8B21

8b Addr/Value pair Section

Address: 0x0FFFF095

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.88 SFLASH_AV_PAIRS_8B22

8b Addr/Value pair Section

Address: 0x0FFFF096

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.89 SFLASH_AV_PAIRS_8B23

8b Addr/Value pair Section

Address: 0x0FFFF097

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.90 SFLASH_AV_PAIRS_8B24

8b Addr/Value pair Section

Address: 0x0FFFF098

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.91 SFLASH_AV_PAIRS_8B25

8b Addr/Value pair Section

Address: 0x0FFFF099

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.92 SFLASH_AV_PAIRS_8B26

8b Addr/Value pair Section

Address: 0x0FFFF09A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.93 SFLASH_AV_PAIRS_8B27

8b Addr/Value pair Section

Address: 0x0FFFF09B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.94 SFLASH_AV_PAIRS_8B28

8b Addr/Value pair Section

Address: 0x0FFFF09C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.95 SFLASH_AV_PAIRS_8B29

8b Addr/Value pair Section

Address: 0x0FFFF09D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.96 SFLASH_AV_PAIRS_8B30

8b Addr/Value pair Section

Address: 0x0FFFF09E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.97 SFLASH_AV_PAIRS_8B31

8b Addr/Value pair Section

Address: 0x0FFFF09F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.98 SFLASH_AV_PAIRS_8B32

8b Addr/Value pair Section

Address: 0x0FFFF0A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.99 SFLASH_AV_PAIRS_8B33

8b Addr/Value pair Section

Address: 0x0FFFF0A1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.100 SFLASH_AV_PAIRS_8B34

8b Addr/Value pair Section

Address: 0x0FFFF0A2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.101 SFLASH_AV_PAIRS_8B35

8b Addr/Value pair Section

Address: 0x0FFFF0A3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.102 SFLASH_AV_PAIRS_8B36

8b Addr/Value pair Section

Address: 0x0FFFF0A4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.103 SFLASH_AV_PAIRS_8B37

8b Addr/Value pair Section

Address: 0x0FFFF0A5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.104 SFLASH_AV_PAIRS_8B38

8b Addr/Value pair Section

Address: 0x0FFFF0A6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.105 SFLASH_AV_PAIRS_8B39

8b Addr/Value pair Section

Address: 0x0FFFF0A7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.106 SFLASH_AV_PAIRS_8B40

8b Addr/Value pair Section

Address: 0x0FFFF0A8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.107 SFLASH_AV_PAIRS_8B41

8b Addr/Value pair Section

Address: 0x0FFFF0A9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.108 SFLASH_AV_PAIRS_8B42

8b Addr/Value pair Section

Address: 0x0FFFF0AA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.109 SFLASH_AV_PAIRS_8B43

8b Addr/Value pair Section

Address: 0x0FFFF0AB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.110 SFLASH_AV_PAIRS_8B44

8b Addr/Value pair Section

Address: 0x0FFFF0AC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.111 SFLASH_AV_PAIRS_8B45

8b Addr/Value pair Section

Address: 0x0FFFF0AD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.112 SFLASH_AV_PAIRS_8B46

8b Addr/Value pair Section

Address: 0x0FFFF0AE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.113 SFLASH_AV_PAIRS_8B47

8b Addr/Value pair Section

Address: 0x0FFFF0AF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.114 SFLASH_AV_PAIRS_8B48

8b Addr/Value pair Section

Address: 0x0FFFF0B0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.115 SFLASH_AV_PAIRS_8B49

8b Addr/Value pair Section

Address: 0x0FFFF0B1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.116 SFLASH_AV_PAIRS_8B50

8b Addr/Value pair Section

Address: 0x0FFFF0B2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.117 SFLASH_AV_PAIRS_8B51

8b Addr/Value pair Section

Address: 0x0FFFF0B3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.118 SFLASH_AV_PAIRS_8B52

8b Addr/Value pair Section

Address: 0x0FFFF0B4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.119 SFLASH_AV_PAIRS_8B53

8b Addr/Value pair Section

Address: 0x0FFFF0B5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.120 SFLASH_AV_PAIRS_8B54

8b Addr/Value pair Section

Address: 0x0FFFF0B6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.121 SFLASH_AV_PAIRS_8B55

8b Addr/Value pair Section

Address: 0x0FFFF0B7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.122 SFLASH_AV_PAIRS_8B56

8b Addr/Value pair Section

Address: 0x0FFFF0B8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.123 SFLASH_AV_PAIRS_8B57

8b Addr/Value pair Section

Address: 0x0FFFF0B9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.124 SFLASH_AV_PAIRS_8B58

8b Addr/Value pair Section

Address: 0x0FFFF0BA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.125 SFLASH_AV_PAIRS_8B59

8b Addr/Value pair Section

Address: 0x0FFFF0BB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.126 SFLASH_AV_PAIRS_8B60

8b Addr/Value pair Section

Address: 0x0FFFF0BC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.127 SFLASH_AV_PAIRS_8B61

8b Addr/Value pair Section

Address: 0x0FFFF0BD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.128 SFLASH_AV_PAIRS_8B62

8b Addr/Value pair Section

Address: 0x0FFFF0BE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.129 SFLASH_AV_PAIRS_8B63

8b Addr/Value pair Section

Address: 0x0FFFF0BF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.130 SFLASH_AV_PAIRS_8B64

8b Addr/Value pair Section

Address: 0x0FFFF0C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.131 SFLASH_AV_PAIRS_8B65

8b Addr/Value pair Section

Address: 0x0FFFF0C1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.132 SFLASH_AV_PAIRS_8B66

8b Addr/Value pair Section

Address: 0x0FFFF0C2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.133 SFLASH_AV_PAIRS_8B67

8b Addr/Value pair Section

Address: 0x0FFFF0C3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.134 SFLASH_AV_PAIRS_8B68

8b Addr/Value pair Section

Address: 0x0FFFF0C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.135 SFLASH_AV_PAIRS_8B69

8b Addr/Value pair Section

Address: 0x0FFFF0C5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.136 SFLASH_AV_PAIRS_8B70

8b Addr/Value pair Section

Address: 0x0FFFF0C6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.137 SFLASH_AV_PAIRS_8B71

8b Addr/Value pair Section

Address: 0x0FFFF0C7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.138 SFLASH_AV_PAIRS_8B72

8b Addr/Value pair Section

Address: 0x0FFFF0C8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.139 SFLASH_AV_PAIRS_8B73

8b Addr/Value pair Section

Address: 0x0FFFF0C9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.140 SFLASH_AV_PAIRS_8B74

8b Addr/Value pair Section

Address: 0x0FFFF0CA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.141 SFLASH_AV_PAIRS_8B75

8b Addr/Value pair Section

Address: 0x0FFFF0CB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.142 SFLASH_AV_PAIRS_8B76

8b Addr/Value pair Section

Address: 0x0FFFF0CC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.143 SFLASH_AV_PAIRS_8B77

8b Addr/Value pair Section

Address: 0x0FFFF0CD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.144 SFLASH_AV_PAIRS_8B78

8b Addr/Value pair Section

Address: 0x0FFFF0CE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.145 SFLASH_AV_PAIRS_8B79

8b Addr/Value pair Section

Address: 0x0FFFF0CF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.146 SFLASH_AV_PAIRS_8B80

8b Addr/Value pair Section

Address: 0x0FFFF0D0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.147 SFLASH_AV_PAIRS_8B81

8b Addr/Value pair Section

Address: 0x0FFFF0D1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.148 SFLASH_AV_PAIRS_8B82

8b Addr/Value pair Section

Address: 0x0FFFF0D2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.149 SFLASH_AV_PAIRS_8B83

8b Addr/Value pair Section

Address: 0x0FFFF0D3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.150 SFLASH_AV_PAIRS_8B84

8b Addr/Value pair Section

Address: 0x0FFFF0D4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.151 SFLASH_AV_PAIRS_8B85

8b Addr/Value pair Section

Address: 0x0FFFF0D5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.152 SFLASH_AV_PAIRS_8B86

8b Addr/Value pair Section

Address: 0x0FFFF0D6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.153 SFLASH_AV_PAIRS_8B87

8b Addr/Value pair Section

Address: 0x0FFFF0D7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.154 SFLASH_AV_PAIRS_8B88

8b Addr/Value pair Section

Address: 0x0FFFF0D8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.155 SFLASH_BLESS_BB_BUMP2

BLESS Bump bit for LDO BB, TXRX

Address: 0x0FFFF0D8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW			RW				
HW Access	R			R				
Name	V2I [7:5]			V2I_RCAL [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW			RW	
HW Access	R			R			R	
Name	SY_IBIAS [15:13]			VBG_TRIM [12:10]			V2I [9:8]	

Bits	Name	Description
15 : 13	SY_IBIAS	3'b1xx: RCAL current bumped 3'b0xx: BG current bumped. 2'bxx: reperesent current bump 01: +12.5%, 00: 0%, 11: -12.5%, 10:-25% Default Value: 0
12 : 10	VBG_TRIM	3d0: Trims the Bandgap voltage by 0% 3d1: Trims the Bandgap voltage by 1.6% 3d2: Trims the Bandgap voltage by 3.2% 3d3: Trims the Bandgap voltage by 4.8% 3d4: Trims the Bandgap voltage by 6.4% 3d5: Trims the Bandgap voltage by -4.8% 3d6: Trims the Bandgap voltage by -3.2% 3d7: Trims the Bandgap voltage by -1.6% Default Value: 0

(continued)

9 : 5	V2I	Bit[9] 1: Error amp quiescent current is 5u 0: Error amp quiescent current is 10u Bit[8:5] 4d0: Trims the BGR current by 0% 4d1: Trims the BGR current by -2.5% 4d2: Trims the BGR current by -5% 4d3: Trims the BGR current by -7.5% 4d4: Trims the BGR current by -10% 4d5: Trims the BGR current by -12.5% 4d6: Trims the BGR current by -15% 4d7: Trims the BGR current by -17.5% 4d8: Trims the BGR current by 20% 4d9: Trims the BGR current by 17.5% 4d10: Trims the BGR current by 15% 4d11: Trims the BGR current by 12.5% 4d12: Trims the BGR current by 10% 4d13: Trims the BGR current by 7.5% 4d14: Trims the BGR current by 5% 4d15: Trims the BGR current by 2.5% Default Value: 0
4 : 0	V2I_RCAL	Bit[4] 1: Error amp quiescent current is 5u 0: Error amp quiescent current is 10u Bit[3:0] 4d0: Trims the RCAL current by 0% 4d1: Trims the RCAL current by -2.5% 4d2: Trims the RCAL current by -5% 4d3: Trims the RCAL current by -7.5% 4d4: Trims the RCAL current by -10% Default Value: 0

29.1.156 SFLASH_AV_PAIRS_8B89

8b Addr/Value pair Section

Address: 0x0FFFF0D9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.157 SFLASH_AV_PAIRS_8B90

8b Addr/Value pair Section

Address: 0x0FFFF0DA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.158 SFLASH_BLESS_BB_XO

BLESS bump configuration 1

Address: 0x0FFFF0DA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW		RW	RW	RW	RW	RW
HW Access	R	R		R	R	R	R	R
Name	CTRL_VDDL_XO	CTRL_RC_FASTSTART_RES [6:5]		EN_AMPDET_FASTSTART	EN_AMPDET_CURMEAS	EN_CURMEAS	EN_RE_FASTSTART	DIS_XOCORE_SUPFILT

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW		RW			RW	
HW Access	R	R		R			R	
Name	rev_bb_xo	CTRL_RPREF [14:13]		CTRL_VDDL_XB [12:10]			CTRL_VDDL_XO [9:8]	

Bits	Name	Description
15	rev_bb_xo	reserved for feature Default Value: 0
14 : 13	CTRL_RPREF	Controls the reference voltage fed as input to the regulators which generate vdd_xo and vdd_xb. 2d0 : 1.289V 2d0 : 1.227V 2d0 : 1.164V 2d0 : 1.382V Default Value: 0
12 : 10	CTRL_VDDL_XB	Controls the value of supply filter resistance in the inverter chain. This in turn controls the supply voltage at which the inverter chain runs. 3d0 : 1.028k 3d0 : 1.172k 3d0 : 1.367k 3d0 : 1.540k 3d0 : 1.889k 3d0 : 2.055k 3d0 : 0.503k 3d0 : 0.747k Default Value: 0
9 : 7	CTRL_VDDL_XO	Controls the value of supply filter resistance in the xo core. This in turn controls the supply voltage at which the core runs. 3d0 : 0.769k 3d0 : 0.877k 3d0 : 1.023k 3d0 : 1.152k 3d0 : 1.413k 3d0 : 1.537k 3d0 : 0.376k 3d0 : 0.559k Default Value: 0

(continued)

6 : 5	CTRL_RC_FASTSTART_RES	Controls the time constant with which the surge current from rc_faststart block decays down to zero. 2d0 : 387us 2d1 : 309us 2d2 : 232us 2d3 : 464us Default Value: 0
4	EN_AMPDET_FASTSTART	This bit is used to force startup of the vtnbyr circuit in the biasgen_and_reg block of the XO. 1d1 : startup forced 1d0 : Normal startup Default Value: 0
3	EN_AMPDET_CURMEAS	This bit can be used to disable all the caps on both X1 node and X2 node. 1d0 : Caps Enabled 1d1 : Caps disabled. Even when all the caps are disabled, due to finite on/off ratio of the caps, the cap on both X1 and X2 node is still 3.69pF Default Value: 0
2	EN_CURMEAS	This bit is used to force startup of the positive feedback loop in the amplitude detect block of the XO. 1d1 : startup forced 1d0 : Normal startup Default Value: 0
1	EN_RE_FASTSTART	Enables/Disables the RC faststart block in the XO. When enabled, this block provides a surge current at xo startup to reduce the settling time of the XO. 1: RC Fast start in XO is enabled 0: RC Fast start in XO is disabled Default Value: 0
0	DIS_XOCORE_SUPFILT	Enables/Disables the supply filter of the XO core. 1: Disabled 0: Enabled Default Value: 0

29.1.159 SFLASH_AV_PAIRS_8B91

8b Addr/Value pair Section

Address: 0x0FFFF0DB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.160 SFLASH_AV_PAIRS_8B92

8b Addr/Value pair Section

Address: 0x0FFFF0DC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.161 SFLASH_BLESS_SY_BUMP1

BLESS SY bump bits configuration 1

Address: 0x0FFFF0DC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW		RW	RW			
HW Access	R	R		R	R			
Name	LDOLO_FORCE_STARTUP	IBIAS_LOPATH [6:5]		LOFB_POWERSAVE	VCO [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	PDCPLPF [15:12]				LOPATH [11:8]			

Bits	Name	Description
15 : 12	PDCPLPF	Bump for PD CP and LPF blocks.[2:0] is used to get range of -20%to +15% in 5% steps. ICP_BUMP[2:0] ICP 1 0 0 -20% 1 0 1 -15% 1 1 0 -10% 1 1 1 -05% 0 0 0 00% 0 0 1 05% 0 1 0 10% 0 1 1 15%. Default Value: 0
11 : 8	LOPATH	Bump bits for LO path bulk bias. Goes to DIVN/FCAL/LOPATH for bumps. 2 bits for pBulk [3:2] and 2 bits for nBulk[1:0]. bump pbulk 0 0 vddx-380mV 0 1 vddx-320mV 1 0 vddx-440mV 1 1 vddx Default Value: 5
7	LDOLO_FORCE_STARTUP	1: force start-up of the VT/R circuit in VCOLOPATH LCO 0: no force start-up Default Value: 0
6 : 5	IBIAS_LOPATH	bump bits for clkbias in lopath bump clk bias pM clk bias nM 0 0 vddo-vgsp vgsn 0 1 vddlo-vgsp-100m vgsn+100m 1 0 vddlo-vgsp-200m vgsn+200m 1 1 vddlo-vgsp-400m vgsn+400m Default Value: 0

(continued)

4	LOFB_POWERSAVE	1: enable powersave for LOFB buffer 0: disable powersave for LOFB buffer Default Value: 0
3 : 0	VCO	Bump bits for SY VCO block. Rt VCO (2 bits) - sy_bump1_vco [3:2] 00 ~ 50 Ohms 01 ~ 30 Ohms 10 ~ 22 Ohms 11 ~ 16 Ohms and Rb VCO (2 bits) - sy_bump1_vco[1:0] 00 ~ 58 Ohms 01 ~ 39 Ohms 10 ~ 22 Ohms 11 ~ 16 Ohms Default Value: 5

29.1.162 SFLASH_AV_PAIRS_8B93

8b Addr/Value pair Section

Address: 0x0FFFF0DD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.163 SFLASH_AV_PAIRS_8B94

8b Addr/Value pair Section

Address: 0x0FFFF0DE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.164 SFLASH_BLESS_LDO

BLESS bump bit for LDO

Address: 0x0FFFF0DE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW		RW		RW		
HW Access	R	R		R		R		
Name	BUMP_SY_LHV	BUMP_SY_LOPATH [6:5]		BUMP_SY_VCO [4:3]		BUMP_BALUM_HF [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			RW
HW Access	R				R			R
Name	REV_LDO [15:12]				BUMP_SY_FFFB [11:9]			BUMP_SY_LHV

Bits	Name	Description
15 : 12	REV_LDO	received for feature Default Value: 0
11 : 9	BUMP_SY_FFFB	3d0: FF and FB LDO outputs are 1.800V 3d1: FF and FB LDO outputs are 1.846V 3d2: FF and FB LDO outputs are 1.894V 3d3: FF and FB LDO outputs are 1.946V 3d4: FF and FB LDO outputs are 2.000V 3d5: FF and FB LDO outputs are 1.649V 3d6: FF and FB LDO outputs are 1.701V 3d7: FF and FB LDO outputs are 1.756V Default Value: 0
8 : 7	BUMP_SY_LHV	2d0: HV LDO outputs are 1.894V 2d1: HV LDO outputs are 2.000V 2d2: HV LDO outputs are 1.800V 2d3: HV LDO outputs are 1.846V Default Value: 0
6 : 5	BUMP_SY_LOPATH	2d0: LOPATH LDO outputs are 1.762V 2d1: LOPATH LDO outputs are 1.861V 2d2: LOPATH LDO outputs are 1.673V 2d3: LOPATH LDO outputs are 1.716V Default Value: 0
4 : 3	BUMP_SY_VCO	2d0: VCO LDO outputs are 1.413V 2d1: VCO LDO outputs are 1.494V 2d2: VCO LDO outputs are 1.329V 2d3: VCO LDO outputs are 1.371V Default Value: 0

(continued)

2 : 0	BUMP_BALUM_HF	3d0: HF LDO output is 1.800V 3d1: HF LDO output is 1.846V 3d2: HF LDO output is 1.894V 3d3: HF LDO output is 1.946V Default Value: 0

29.1.165 SFLASH_AV_PAIRS_8B95

8b Addr/Value pair Section

Address: 0x0FFFF0DF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.166 SFLASH_AV_PAIRS_8B96

8b Addr/Value pair Section

Address: 0x0FFFF0E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.167 SFLASH_AV_PAIRS_8B97

8b Addr/Value pair Section

Address: 0x0FFFF0E1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.168 SFLASH_AV_PAIRS_8B98

8b Addr/Value pair Section

Address: 0x0FFFF0E2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.169 SFLASH_AV_PAIRS_8B99

8b Addr/Value pair Section

Address: 0x0FFFF0E3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.170 SFLASH_AV_PAIRS_8B100

8b Addr/Value pair Section

Address: 0x0FFFF0E4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.171 SFLASH_AV_PAIRS_8B101

8b Addr/Value pair Section

Address: 0x0FFFF0E5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.172 SFLASH_AV_PAIRS_8B102

8b Addr/Value pair Section

Address: 0x0FFFF0E6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.173 SFLASH_AV_PAIRS_8B103

8b Addr/Value pair Section

Address: 0x0FFFF0E7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.174 SFLASH_AV_PAIRS_8B104

8b Addr/Value pair Section

Address: 0x0FFFF0E8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.175 SFLASH_AV_PAIRS_8B105

8b Addr/Value pair Section

Address: 0x0FFFF0E9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.176 SFLASH_AV_PAIRS_8B106

8b Addr/Value pair Section

Address: 0x0FFFF0EA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.177 SFLASH_AV_PAIRS_8B107

8b Addr/Value pair Section

Address: 0x0FFFF0EB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.178 SFLASH_AV_PAIRS_8B108

8b Addr/Value pair Section

Address: 0x0FFFF0EC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.179 SFLASH_AV_PAIRS_8B109

8b Addr/Value pair Section

Address: 0x0FFFF0ED

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.180 SFLASH_AV_PAIRS_8B110

8b Addr/Value pair Section

Address: 0x0FFFF0EE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.181 SFLASH_AV_PAIRS_8B111

8b Addr/Value pair Section

Address: 0x0FFFF0EF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.182 SFLASH_AV_PAIRS_8B112

8b Addr/Value pair Section

Address: 0x0FFFF0F0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.183 SFLASH_AV_PAIRS_8B113

8b Addr/Value pair Section

Address: 0x0FFFF0F1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.184 SFLASH_AV_PAIRS_8B114

8b Addr/Value pair Section

Address: 0x0FFFF0F2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.185 SFLASH_AV_PAIRS_8B115

8b Addr/Value pair Section

Address: 0x0FFFF0F3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.186 SFLASH_AV_PAIRS_8B116

8b Addr/Value pair Section

Address: 0x0FFFF0F4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.187 SFLASH_AV_PAIRS_8B117

8b Addr/Value pair Section

Address: 0x0FFFF0F5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.188 SFLASH_AV_PAIRS_8B118

8b Addr/Value pair Section

Address: 0x0FFFF0F6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.189 SFLASH_AV_PAIRS_8B119

8b Addr/Value pair Section

Address: 0x0FFFF0F7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.190 SFLASH_AV_PAIRS_8B120

8b Addr/Value pair Section

Address: 0x0FFFF0F8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.191 SFLASH_AV_PAIRS_8B121

8b Addr/Value pair Section

Address: 0x0FFFF0F9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.192 SFLASH_AV_PAIRS_8B122

8b Addr/Value pair Section

Address: 0x0FFFF0FA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.193 SFLASH_AV_PAIRS_8B123

8b Addr/Value pair Section

Address: 0x0FFFF0FB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.194 SFLASH_AV_PAIRS_8B124

8b Addr/Value pair Section

Address: 0x0FFFF0FC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.195 SFLASH_AV_PAIRS_8B125

8b Addr/Value pair Section

Address: 0x0FFFF0FD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.196 SFLASH_AV_PAIRS_8B126

8b Addr/Value pair Section

Address: 0x0FFFF0FE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.197 SFLASH_AV_PAIRS_8B127

8b Addr/Value pair Section

Address: 0x0FFFF0FF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

29.1.198 SFLASH_AV_PAIRS_32B0

32b Addr/Value pair Section

Address: 0x0FFFF100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Address or Value Word Default Value: X

29.1.199 SFLASH_AV_PAIRS_32B1

32b Addr/Value pair Section

Address: 0x0FFFF104

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Address or Value Word Default Value: X

29.1.200 SFLASH_AV_PAIRS_32B2

32b Addr/Value pair Section

Address: 0x0FFFF108

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Address or Value Word Default Value: X

29.1.201 SFLASH_AV_PAIRS_32B3

32b Addr/Value pair Section

Address: 0x0FFFF10C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Address or Value Word Default Value: X

29.1.202 SFLASH_AV_PAIRS_32B4

32b Addr/Value pair Section

Address: 0x0FFFF110

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Address or Value Word Default Value: X

29.1.203 SFLASH_AV_PAIRS_32B5

32b Addr/Value pair Section

Address: 0x0FFFF114

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Address or Value Word Default Value: X

29.1.204 SFLASH_AV_PAIRS_32B6

32b Addr/Value pair Section

Address: 0x0FFFF118

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Address or Value Word Default Value: X

29.1.205 SFLASH_AV_PAIRS_32B7

32b Addr/Value pair Section

Address: 0x0FFFF11C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Address or Value Word Default Value: X

29.1.206 SFLASH_AV_PAIRS_32B8

32b Addr/Value pair Section

Address: 0x0FFFF120

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Address or Value Word Default Value: X

29.1.207 SFLASH_AV_PAIRS_32B9

32b Addr/Value pair Section

Address: 0x0FFFF124

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Address or Value Word Default Value: X

29.1.208 SFLASH_AV_PAIRS_32B10

32b Addr/Value pair Section

Address: 0x0FFFF128

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Address or Value Word Default Value: X

29.1.209 SFLASH_AV_PAIRS_32B11

32b Addr/Value pair Section

Address: 0x0FFFF12C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Address or Value Word Default Value: X

29.1.210 SFLASH_AV_PAIRS_32B12

32b Addr/Value pair Section

Address: 0x0FFFF130

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Address or Value Word Default Value: X

29.1.211 SFLASH_AV_PAIRS_32B13

32b Addr/Value pair Section

Address: 0x0FFFF134

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Address or Value Word Default Value: X

29.1.212 SFLASH_AV_PAIRS_32B14

32b Addr/Value pair Section

Address: 0x0FFFF138

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Address or Value Word Default Value: X

29.1.213 SFLASH_AV_PAIRS_32B15

32b Addr/Value pair Section

Address: 0x0FFFF13C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Address or Value Word Default Value: X

29.1.214 SFLASH_CPUSS_WOUNDING

CPUSS Wounding Register

Address: 0x0FFFF140

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Data to use for register Default Value: X

29.1.215 SFLASH_SILICON_ID

Silicon ID

Address: 0x0FFFF144

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	ID [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	ID	Silicon ID Default Value: X

29.1.216 SFLASH_CPUSS_PRIV_RAM

RAM Privileged Limit

Address: 0x0FFFF148

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	RAM_PROT_LIMIT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							RAM_PROT_LIMIT

Bits	Name	Description
8 : 0	RAM_PROT_LIMIT	Indicates the limit where the privileged area of SRAM starts in increments of 256 Bytes. "0": Entire SRAM is Privileged. "1": First 256 Bytes are User accessable. Any number larger than the size of the SRAM indicates that the entire SRAM is user mode accessible. Default Value: 0

29.1.217 SFLASH_CPUSS_PRIV_ROM_BROM

Boot ROM Privileged Limit

Address: 0x0FFFF14A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	BROM_PROT_LIMIT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 0	BROM_PROT_LIMIT	Indicates the limit where the privileged area of the Boot ROM partition starts in increments of 256 Bytes. "0": Entire Boot ROM is Privileged. "1": First 256 Bytes are User accessable. ... BROM_PROT_LIMIT >= "Boot ROM partition capacity": Entire Boot ROM partition is user mode accessible. Default Value: 0

29.1.218 SFLASH_CPUSS_PRIV_FLASH

Flash Privileged Limit

Address: 0x0FFFF14C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	FLASH_PROT_LIMIT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW		
HW Access	None					R		
Name	None [15:11]					FLASH_PROT_LIMIT [10:8]		

Bits	Name	Description
10 : 0	FLASH_PROT_LIMIT	Indicates the limit where the privileged area of flash starts in increments of 256 Bytes. "0": Entire flash is Privileged. "1": First 256 Bytes are User accessable. Any number larger than the size of the flash indicates that the entire flash is user mode accessible. Note that SuperVisory rows are always User accessable. If FLASH_PROT_LIMIT defines a non-empty privileged area, the boot ROM will assume that a system call table exists at the beginning of the Flash privileged area and use it for all SystemCalls made using SYSREQ. Default Value: 0

29.1.219 SFLASH_CPUSS_PRIV_ROM_SROM

System ROM Privileged Limit

Address: 0x0FFFF14E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SROM_PROT_LIMIT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						SROM_PROT_LIMIT [9:8]	

Bits	Name	Description
9 : 0	SROM_PROT_LIMIT	Indicates the limit where the privileged area of System ROM partition starts in increments of 256 Bytes. The limit is wrt. the start of the ROM memory (start of the Boot ROM partition). SROM_PROT_LIMIT * 256 Byte <= "Boot ROM partition capacity": Entire System ROM is Privileged. SROM_PROT_LIMIT * 256 Byte > "Boot ROM partition capacity": First SROM_PROT_LIMIT * 256 - "Boot ROM partition capacity" Bytes are User accessable. ... SROM_PROT_LIMIT >= "ROM capacity": Entire System ROM is user mode accessible. Default Value: 0

29.1.220 SFLASH_HIB_KEY_DELAY

Hibernate wakeup value for PWR_KEY_DELAY

Address: 0x0FFFF150

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	WAKEUP_HOLDOFF [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						WAKEUP_HOLDOFF [9:8]	

Bits	Name	Description
9 : 0	WAKEUP_HOLDOFF	Delay (in 12MHz IMO clock cycles) to wait for references to settle on wakeup from hibernate/ deepsleep. PBOD is ignored and system does not resume until this delay expires. Note that the same delay on POR is hard-coded. Default Value: X

29.1.221 SFLASH_DPSLP_KEY_DELAY

DeepSleep wakeup value for PWR_KEY_DELAY

Address: 0x0FFFF152

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	WAKEUP_HOLDOFF [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						WAKEUP_HOLDOFF [9:8]	

Bits	Name	Description
9 : 0	WAKEUP_HOLDOFF	Delay (in 12MHz IMO clock cycles) to wait for references to settle on wakeup from hibernate/ deepsleep. PBOD is ignored and system does not resume until this delay expires. Note that the same delay on POR is hard-coded. Default Value: X

29.1.222 SFLASH_SWD_CONFIG

SWD pinout selector (not present in TSG4/TSG5-M)

Address: 0x0FFFF154

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							None
Name	None [7:1]							SWD_SELECT

Bits	Name	Description
0	SWD_SELECT	0: Use Primary SWD location 1: Use Alternate SWD location Default Value: X

29.1.223 SFLASH_INITIAL_SPCIF_TRIM_M1_DAC0

FLASH IDAC trim used during boot

Address: 0x0FFFF155

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW			RW				
HW Access	R			R				
Name	SLOPE [7:5]			IDAC [4:0]				

Bits	Name	Description
7 : 5	SLOPE	See SPCIF_TRIM1 Default Value: 0
4 : 0	IDAC	See SPCIF_TRIM1 Default Value: 0

29.1.224 SFLASH_SWD_LISTEN

Listen Window Length

Address: 0x0FFFF158

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	CYCLES [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	CYCLES [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	CYCLES [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	CYCLES [31:24]							

Bits	Name	Description
31 : 0	CYCLES	Number of clock cycles Default Value: X

29.1.225 SFLASH_FLASH_START

Flash Image Start Address

Address: 0x0FFFF15C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	ADDRESS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	ADDRESS [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	ADDRESS [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	ADDRESS [31:24]							

Bits	Name	Description
31 : 0	ADDRESS	Start Address Default Value: X

29.1.226 SFLASH_CSD_TRIM1_HVIDAC

CSD Trim Data for HVIDAC operation

Address: 0x0FFFF160

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	TRIM8 [7:0]							

Bits	Name	Description
7 : 0	TRIM8	Trim data Default Value: X

29.1.227 SFLASH_CSD_TRIM2_HVIDAC

CSD Trim Data for HVIDAC operation

Address: 0x0FFFF161

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	TRIM8 [7:0]							

Bits	Name	Description
7 : 0	TRIM8	Trim data Default Value: X

29.1.228 SFLASH_CSD_TRIM1_CSD

CSD Trim Data for (normal) CSD operation

Address: 0x0FFFF162

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	TRIM8 [7:0]							

Bits	Name	Description
7 : 0	TRIM8	Trim data Default Value: X

29.1.229 SFLASH_CSD_TRIM2_CSD

CSD Trim Data for (normal) CSD operation

Address: 0x0FFFF163

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	TRIM8 [7:0]							

Bits	Name	Description
7 : 0	TRIM8	Trim data Default Value: X

29.1.230 SFLASH_SAR_TEMP_MULTIPLIER

SAR Temperature Sensor Multiplication Factor

Address: 0x0FFFF164

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	TEMP_MULTIPLIER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	TEMP_MULTIPLIER [15:8]							

Bits	Name	Description
15 : 0	TEMP_MULTIPLIER	Multiplier value for SAR temperature sensor in fixed point 0.16 format. Note: this field exists in products that contain SAR (m0s8sar) only. Default Value: X

29.1.231 SFLASH_SAR_TEMP_OFFSET

SAR Temperature Sensor Offset

Address: 0x0FFFF166

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	TEMP_OFFSET [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	TEMP_OFFSET [15:8]							

Bits	Name	Description
15 : 0	TEMP_OFFSET	Offset value for SAR temperature sensor in fixed point 10.6 format. Note: this field exists in products that contain SAR (m0s8sar) only. Default Value: X

29.1.232 SFLASH_SKIP_CHECKSUM

Checksum Skip Option Register

Address: 0x0FFFF169

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	SKIP [7:0]							

Bits	Name	Description
7 : 0	SKIP	0: Perform checksum check (see CHECKSUM fueld below) 1: Skip checksum check >1: Undefined - do not use Default Value: X

29.1.233 SFLASH_PROT_VIRGINKEY0

Virgin Protection Mode Key

Address: 0x0FFFF170

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	KEY8 [7:0]							

Bits	Name	Description
7 : 0	KEY8	Key Byte Default Value: X

29.1.234 SFLASH_PROT_VIRGINKEY1

Virgin Protection Mode Key

Address: 0x0FFFF171

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	KEY8 [7:0]							

Bits	Name	Description
7 : 0	KEY8	Key Byte Default Value: X

29.1.235 SFLASH_PROT_VIRGINKEY2

Virgin Protection Mode Key

Address: 0x0FFFF172

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	KEY8 [7:0]							

Bits	Name	Description
7 : 0	KEY8	Key Byte Default Value: X

29.1.236 SFLASH_PROT_VIRGINKEY3

Virgin Protection Mode Key

Address: 0x0FFFF173

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	KEY8 [7:0]							

Bits	Name	Description
7 : 0	KEY8	Key Byte Default Value: X

29.1.237 SFLASH_PROT_VIRGINKEY4

Virgin Protection Mode Key

Address: 0x0FFFF174

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	KEY8 [7:0]							

Bits	Name	Description
7 : 0	KEY8	Key Byte Default Value: X

29.1.238 SFLASH_PROT_VIRGINKEY5

Virgin Protection Mode Key

Address: 0x0FFFF175

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	KEY8 [7:0]							

Bits	Name	Description
7 : 0	KEY8	Key Byte Default Value: X

29.1.239 SFLASH_PROT_VIRGINKEY6

Virgin Protection Mode Key

Address: 0x0FFFF176

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	KEY8 [7:0]							

Bits	Name	Description
7 : 0	KEY8	Key Byte Default Value: X

29.1.240 SFLASH_PROT_VIRGINKEY7

Virgin Protection Mode Key

Address: 0x0FFFF177

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	KEY8 [7:0]							

Bits	Name	Description
7 : 0	KEY8	Key Byte Default Value: X

29.1.241 SFLASH_DIE_LOT0

Lot Number (3 bytes)

Address: 0x0FFFF178

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	LOT [7:0]							

Bits	Name	Description
7 : 0	LOT	Lot Number Byte Default Value: X

29.1.242 SFLASH_DIE_LOT1

Lot Number (3 bytes)

Address: 0x0FFFF179

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	LOT [7:0]							

Bits	Name	Description
7 : 0	LOT	Lot Number Byte Default Value: X

29.1.243 SFLASH_DIE_LOT2

Lot Number (3 bytes)

Address: 0x0FFFF17A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	LOT [7:0]							

Bits	Name	Description
7 : 0	LOT	Lot Number Byte Default Value: X

29.1.244 SFLASH_DIE_WAFER

Wafer Number

Address: 0x0FFFF17B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	WAFER [7:0]							

Bits	Name	Description
7 : 0	WAFER	Wafer Number Default Value: X

29.1.245 SFLASH_DIE_X

X Position on Wafer, CRI Pass/Fail Bin

Address: 0x0FFFF17C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	X [7:0]							

Bits	Name	Description
7 : 0	X	X Position Default Value: X

29.1.246 SFLASH_DIE_Y

Y Position on Wafer, CHI Pass/Fail Bin

Address: 0x0FFFF17D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	Y [7:0]							

Bits	Name	Description
7 : 0	Y	Y Position Default Value: X

29.1.247 SFLASH_DIE_SORT

Sort1/2/3 Pass/Fail Bin

Address: 0x0FFFF17E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		None	None	None	None	None	None
Name	None [7:6]		ENG_PASS	CHI_PASS	CRI_PASS	S3_PASS	S2_PASS	S1_PASS

Bits	Name	Description
5	ENG_PASS	ENG Pass Bin Default Value: X
4	CHI_PASS	CHI Pass Bin (1) or 0 (Fail Bin) Default Value: X
3	CRI_PASS	CRI Pass Bin (1) or 0 (Fail Bin) Default Value: X
2	S3_PASS	SORT3 Pass Bin (1) or 0 (Fail Bin) Default Value: X
1	S2_PASS	SORT2 Pass Bin (1) or 0 (Fail Bin) Default Value: X
0	S1_PASS	SORT1 Pass Bin (1) or 0 (Fail Bin) Default Value: X

29.1.248 SFLASH_DIE_MINOR

Minor Revision Number

Address: 0x0FFFF17F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	MINOR [7:0]							

Bits	Name	Description
7 : 0	MINOR	Minor revision number Default Value: X

29.1.249 SFLASH_PE_TE_DATA0

PE/TE Data

Address: 0x0FFFF180

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

29.1.250 SFLASH_PE_TE_DATA1

PE/TE Data

Address: 0x0FFFF181

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

29.1.251 SFLASH_PE_TE_DATA2

PE/TE Data

Address: 0x0FFFF182

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

29.1.252 SFLASH_PE_TE_DATA3

PE/TE Data

Address: 0x0FFFF183

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

29.1.253 SFLASH_PE_TE_DATA4

PE/TE Data

Address: 0x0FFFF184

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

29.1.254 SFLASH_PE_TE_DATA5

PE/TE Data

Address: 0x0FFFF185

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

29.1.255 SFLASH_PE_TE_DATA6

PE/TE Data

Address: 0x0FFFF186

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

29.1.256 SFLASH_PE_TE_DATA7

PE/TE Data

Address: 0x0FFFF187

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

29.1.257 SFLASH_PE_TE_DATA8

PE/TE Data

Address: 0x0FFFF188

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

29.1.258 SFLASH_PE_TE_DATA9

PE/TE Data

Address: 0x0FFFF189

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

29.1.259 SFLASH_PE_TE_DATA10

PE/TE Data

Address: 0x0FFFF18A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

29.1.260 SFLASH_PE_TE_DATA11

PE/TE Data

Address: 0x0FFFF18B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

29.1.261 SFLASH_PE_TE_DATA12

PE/TE Data

Address: 0x0FFFF18C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

29.1.262 SFLASH_PE_TE_DATA13

PE/TE Data

Address: 0x0FFFF18D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

29.1.263 SFLASH_PE_TE_DATA14

PE/TE Data

Address: 0x0FFFF18E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

29.1.264 SFLASH_PE_TE_DATA15

PE/TE Data

Address: 0x0FFFF18F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

29.1.265 SFLASH_PE_TE_DATA16

PE/TE Data

Address: 0x0FFFF190

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

29.1.266 SFLASH_PE_TE_DATA17

PE/TE Data

Address: 0x0FFFF191

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

29.1.267 SFLASH_PE_TE_DATA18

PE/TE Data

Address: 0x0FFFF192

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

29.1.268 SFLASH_PE_TE_DATA19

PE/TE Data

Address: 0x0FFFF193

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

29.1.269 SFLASH_PE_TE_DATA20

PE/TE Data

Address: 0x0FFFF194

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

29.1.270 SFLASH_PE_TE_DATA21

PE/TE Data

Address: 0x0FFFF195

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

29.1.271 SFLASH_PE_TE_DATA22

PE/TE Data

Address: 0x0FFFF196

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

29.1.272 SFLASH_PE_TE_DATA23

PE/TE Data

Address: 0x0FFFF197

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

29.1.273 SFLASH_PE_TE_DATA24

PE/TE Data

Address: 0x0FFFF198

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

29.1.274 SFLASH_PE_TE_DATA25

PE/TE Data

Address: 0x0FFFF199

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

29.1.275 SFLASH_PE_TE_DATA26

PE/TE Data

Address: 0x0FFFF19A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

29.1.276 SFLASH_PE_TE_DATA27

PE/TE Data

Address: 0x0FFFF19B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

29.1.277 SFLASH_PE_TE_DATA28

PE/TE Data

Address: 0x0FFFF19C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

29.1.278 SFLASH_PE_TE_DATA29

PE/TE Data

Address: 0x0FFFF19D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

29.1.279 SFLASH_PE_TE_DATA30

PE/TE Data

Address: 0x0FFFF19E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

29.1.280 SFLASH_PE_TE_DATA31

PE/TE Data

Address: 0x0FFFF19F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

29.1.281 SFLASH_PP

Preprogram Settings

Address: 0x0FFFF1A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	PERIOD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	None				None			
Name	NDAC [31:28]				PDAC [27:24]			

Bits	Name	Description
31 : 28	NDAC	NDAC input. Each increment in NDAC causes an increase of ~0.10V in VNEG Default Value: X
27 : 24	PDAC	PDAC input. Each increment in PDAC causes an increase of ~0.10V in VPOS Default Value: X
23 : 0	PERIOD	Period of timer in clk_spcif_timer ticks. For regular FLASH, clock is 36MHz from dedicated oscillator. For FLASH-Lite, clock is same as clk_hf, which must be set to 48MHz for 48MHz devices and 12MHz for max 16MHz devices Default Value: X

29.1.282 SFLASH_E

Erase Settings

Address: 0x0FFFF1A4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	PERIOD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	None				None			
Name	NDAC [31:28]				PDAC [27:24]			

Bits	Name	Description
31 : 28	NDAC	NDAC input. Each increment in NDAC causes an increase of ~0.10V in VNEG Default Value: X
27 : 24	PDAC	PDAC input. Each increment in PDAC causes an increase of ~0.10V in VPOS Default Value: X
23 : 0	PERIOD	Period of timer in clk_spcif_timer ticks. For regular FLASH, clock is 36MHz from dedicated oscillator. For FLASH-Lite, clock is same as clk_hf, which must be set to 48MHz for 48MHz devices and 12MHz for max 16MHz devices Default Value: X

29.1.283 SFLASH_P

Program Settings

Address: 0x0FFFF1A8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	PERIOD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	None				None			
Name	NDAC [31:28]				PDAC [27:24]			

Bits	Name	Description
31 : 28	NDAC	NDAC input. Each increment in NDAC causes an increase of ~0.10V in VNEG Default Value: X
27 : 24	PDAC	PDAC input. Each increment in PDAC causes an increase of ~0.10V in VPOS Default Value: X
23 : 0	PERIOD	Period of timer in clk_spcif_timer ticks. For regular FLASH, clock is 36MHz from dedicated oscillator. For FLASH-Lite, clock is same as clk_hf, which must be set to 48MHz for 48MHz devices and 12MHz for max 16MHz devices Default Value: X

29.1.284 SFLASH_EA_E

Erase All - Erase Settings

Address: 0x0FFFF1AC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	PERIOD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	None				None			
Name	NDAC [31:28]				PDAC [27:24]			

Bits	Name	Description
31 : 28	NDAC	NDAC input. Each increment in NDAC causes an increase of ~0.10V in VNEG Default Value: X
27 : 24	PDAC	PDAC input. Each increment in PDAC causes an increase of ~0.10V in VPOS Default Value: X
23 : 0	PERIOD	Period of timer in clk_spcif_timer ticks. For regular FLASH, clock is 36MHz from dedicated oscillator. For FLASH-Lite, clock is same as clk_hf, which must be set to 48MHz for 48MHz devices and 12MHz for max 16MHz devices Default Value: X

29.1.285 SFLASH_EA_P

Erase All - Program Settings

Address: 0x0FFFF1B0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	PERIOD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	None				None			
Name	NDAC [31:28]				PDAC [27:24]			

Bits	Name	Description
31 : 28	NDAC	NDAC input. Each increment in NDAC causes an increase of ~0.10V in VNEG Default Value: X
27 : 24	PDAC	PDAC input. Each increment in PDAC causes an increase of ~0.10V in VPOS Default Value: X
23 : 0	PERIOD	Period of timer in clk_spcif_timer ticks. For regular FLASH, clock is 36MHz from dedicated oscillator. For FLASH-Lite, clock is same as clk_hf, which must be set to 48MHz for 48MHz devices and 12MHz for max 16MHz devices Default Value: X

29.1.286 SFLASH_ES_E

Erase Sector - Erase Settings

Address: 0x0FFFF1B4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	PERIOD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	None				None			
Name	NDAC [31:28]				PDAC [27:24]			

Bits	Name	Description
31 : 28	NDAC	NDAC input. Each increment in NDAC causes an increase of ~0.10V in VNEG Default Value: X
27 : 24	PDAC	PDAC input. Each increment in PDAC causes an increase of ~0.10V in VPOS Default Value: X
23 : 0	PERIOD	Period of timer in clk_spcif_timer ticks. For regular FLASH, clock is 36MHz from dedicated oscillator. For FLASH-Lite, clock is same as clk_hf, which must be set to 48MHz for 48MHz devices and 12MHz for max 16MHz devices Default Value: X

29.1.287 SFLASH_ES_P_EO

Erase Sector - Program EO Settings

Address: 0x0FFFF1B8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	PERIOD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	None				None			
Name	NDAC [31:28]				PDAC [27:24]			

Bits	Name	Description
31 : 28	NDAC	NDAC input. Each increment in NDAC causes an increase of ~0.10V in VNEG Default Value: X
27 : 24	PDAC	PDAC input. Each increment in PDAC causes an increase of ~0.10V in VPOS Default Value: X
23 : 0	PERIOD	Period of timer in clk_spcif_timer ticks. For regular FLASH, clock is 36MHz from dedicated oscillator. For FLASH-Lite, clock is same as clk_hf, which must be set to 48MHz for 48MHz devices and 12MHz for max 16MHz devices Default Value: X

29.1.288 SFLASH_E_VCTAT

Bandgap Trim Register

Address: 0x0FFFF1BC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	RW		RW			
HW Access	None	None	None		None			
Name	None	VCTAT_ENABLE	VCTAT_VOLTAGE [5:4]		VCTAT_SLOPE [3:0]			

Bits	Name	Description
6	VCTAT_ENABLE	Enable VCTAT block Default Value: X
5 : 4	VCTAT_VOLTAGE	Output voltage absolute trim Default Value: X
3 : 0	VCTAT_SLOPE	Output slope setting controls. The slope of the voltage with temperature varies from ~0% to ~15% from the value at 55C over the temperature range -40C to 150C based on control signal settings 0 to 15 Default Value: X

29.1.289 SFLASH_P_VCTAT

Bandgap Trim Register

Address: 0x0FFFF1BD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	RW		RW			
HW Access	None	None	None		None			
Name	None	VCTAT_ENABLE	VCTAT_VOLTAGE [5:4]		VCTAT_SLOPE [3:0]			

Bits	Name	Description
6	VCTAT_ENABLE	Enable VCTAT block Default Value: X
5 : 4	VCTAT_VOLTAGE	Output voltage absolute trim Default Value: X
3 : 0	VCTAT_SLOPE	Output slope setting controls. The slope of the voltage with temperature varies from ~0% to ~15% from the value at 55C over the temperature range -40C to 150C based on control signal settings 0 to 15 Default Value: X

29.1.290 SFLASH_IMO_MAXF0

Max frequency for trim pair

Address: 0x0FFFF1C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		None					
Name	None [7:6]		MAXFREQ [5:0]					

Bits	Name	Description
5 : 0	MAXFREQ	Max frequency (3..48) at which IMO_ABS/TMPCO3 is valid (range is IMO_MAXF2+1 .. IMO_MAXF3). Default Value: X

29.1.291 SFLASH_IMO_ABS0

Value for PWR_BG_TRIM4 (ICTAT trim for IMO current reference).

Address: 0x0FFFF1C1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		None					
Name	None [7:6]		ABS_TRIM_IMO [5:0]					

Bits	Name	Description
5 : 0	ABS_TRIM_IMO	IMO-irefgen output current magnitude trim Default Value: X

29.1.292 SFLASH_IMO_TMPCO0

Value for PWR_BG_TRIM5 (ICTAT tempco for IMO current reference).

Address: 0x0FFFF1C2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		None					
Name	None [7:6]		TMPCO_TRIM_IMO [5:0]					

Bits	Name	Description
5 : 0	TMPCO_TRIM_IMO	IMO-irefgen output current temperature co-efficient trim Default Value: X

29.1.293 SFLASH_IMO_MAXF1

Max frequency for trim pair

Address: 0x0FFFF1C3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		None					
Name	None [7:6]		MAXFREQ [5:0]					

Bits	Name	Description
5 : 0	MAXFREQ	Max frequency (3..48) at which IMO_ABS/TMPCO3 is valid (range is IMO_MAXF2+1 .. IMO_MAXF3). Default Value: X

29.1.294 SFLASH_IMO_ABS1

Value for PWR_BG_TRIM4 (ICTAT trim for IMO current reference).

Address: 0x0FFFF1C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		None					
Name	None [7:6]		ABS_TRIM_IMO [5:0]					

Bits	Name	Description
5 : 0	ABS_TRIM_IMO	IMO-irefgen output current magnitude trim Default Value: X

29.1.295 SFLASH_IMO_TMPCO1

Value for PWR_BG_TRIM5 (ICTAT tempco for IMO current reference).

Address: 0x0FFFF1C5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		None					
Name	None [7:6]		TMPCO_TRIM_IMO [5:0]					

Bits	Name	Description
5 : 0	TMPCO_TRIM_IMO	IMO-irefgen output current temperature co-efficient trim Default Value: X

29.1.296 SFLASH_IMO_MAXF2

Max frequency for trim pair

Address: 0x0FFFF1C6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		None					
Name	None [7:6]		MAXFREQ [5:0]					

Bits	Name	Description
5 : 0	MAXFREQ	Max frequency (3..48) at which IMO_ABS/TMPCO3 is valid (range is IMO_MAXF2+1 .. IMO_MAXF3). Default Value: X

29.1.297 SFLASH_IMO_ABS2

Value for PWR_BG_TRIM4 (ICTAT trim for IMO current reference).

Address: 0x0FFFF1C7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		None					
Name	None [7:6]		ABS_TRIM_IMO [5:0]					

Bits	Name	Description
5 : 0	ABS_TRIM_IMO	IMO-irefgen output current magnitude trim Default Value: X

29.1.298 SFLASH_IMO_TMPCO2

Value for PWR_BG_TRIM5 (ICTAT tempco for IMO current reference).

Address: 0x0FFFF1C8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		None					
Name	None [7:6]		TMPCO_TRIM_IMO [5:0]					

Bits	Name	Description
5 : 0	TMPCO_TRIM_IMO	IMO-irefgen output current temperature co-efficient trim Default Value: X

29.1.299 SFLASH_IMO_MAXF3

Max frequency for trim pair

Address: 0x0FFFF1C9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		None					
Name	None [7:6]		MAXFREQ [5:0]					

Bits	Name	Description
5 : 0	MAXFREQ	Max frequency (3..48) at which IMO_ABS/TMPCO3 is valid (range is IMO_MAXF2+1 .. IMO_MAXF3). Default Value: X

29.1.300 SFLASH_IMO_ABS3

Value for PWR_BG_TRIM4 (ICTAT trim for IMO current reference).

Address: 0x0FFFF1CA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		None					
Name	None [7:6]		ABS_TRIM_IMO [5:0]					

Bits	Name	Description
5 : 0	ABS_TRIM_IMO	IMO-irefgen output current magnitude trim Default Value: X

29.1.301 SFLASH_IMO_TMPCO3

Value for PWR_BG_TRIM5 (ICTAT tempco for IMO current reference).

Address: 0x0FFFF1CB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		None					
Name	None [7:6]		TMPCO_TRIM_IMO [5:0]					

Bits	Name	Description
5 : 0	TMPCO_TRIM_IMO	IMO-irefgen output current temperature co-efficient trim Default Value: X

29.1.302 SFLASH_IMO_ABS4

Value for PWR_BG_TRIM4 (ICTAT trim for IMO current reference).

Address: 0x0FFFF1CC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		None					
Name	None [7:6]		ABS_TRIM_IMO [5:0]					

Bits	Name	Description
5 : 0	ABS_TRIM_IMO	IMO-irefgen output current magnitude trim Default Value: X

29.1.303 SFLASH_IMO_TMPCO4

Value for PWR_BG_TRIM5 (ICTAT tempco for IMO current reference).

Address: 0x0FFFF1CD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		None					
Name	None [7:6]		TMPCO_TRIM_IMO [5:0]					

Bits	Name	Description
5 : 0	TMPCO_TRIM_IMO	IMO-irefgen output current temperature co-efficient trim Default Value: X

29.1.304 SFLASH_IMO_TRIM0

IMO Trim Register (SRSSv2)

Address: 0x0FFFF1D0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

29.1.305 SFLASH_IMO_TRIM1

IMO Trim Register (SRSSv2)

Address: 0x0FFFF1D1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

29.1.306 SFLASH_IMO_TRIM2

IMO Trim Register (SRSSv2)

Address: 0x0FFFF1D2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

29.1.307 SFLASH_IMO_TRIM3

IMO Trim Register (SRSSv2)

Address: 0x0FFFF1D3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

29.1.308 SFLASH_IMO_TRIM4

IMO Trim Register (SRSSv2)

Address: 0x0FFFF1D4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

29.1.309 SFLASH_IMO_TRIM5

IMO Trim Register (SRSSv2)

Address: 0x0FFFF1D5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

29.1.310 SFLASH_IMO_TRIM6

IMO Trim Register (SRSSv2)

Address: 0x0FFFF1D6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

29.1.311 SFLASH_IMO_TRIM7

IMO Trim Register (SRSSv2)

Address: 0x0FFFF1D7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

29.1.312 SFLASH_IMO_TRIM8

IMO Trim Register (SRSSv2)

Address: 0x0FFFF1D8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

29.1.313 SFLASH_IMO_TRIM9

IMO Trim Register (SRSSv2)

Address: 0x0FFFF1D9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

29.1.314 SFLASH_IMO_TRIM10

IMO Trim Register (SRSSv2)

Address: 0x0FFFF1DA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

29.1.315 SFLASH_IMO_TRIM11

IMO Trim Register (SRSSv2)

Address: 0x0FFFF1DB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

29.1.316 SFLASH_IMO_TRIM12

IMO Trim Register (SRSSv2)

Address: 0x0FFFF1DC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

29.1.317 SFLASH_IMO_TRIM13

IMO Trim Register (SRSSv2)

Address: 0x0FFFF1DD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

29.1.318 SFLASH_IMO_TRIM14

IMO Trim Register (SRSSv2)

Address: 0x0FFFF1DE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

29.1.319 SFLASH_IMO_TRIM15

IMO Trim Register (SRSSv2)

Address: 0x0FFFF1DF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

29.1.320 SFLASH_IMO_TRIM16

IMO Trim Register (SRSSv2)

Address: 0x0FFFF1E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

29.1.321 SFLASH_IMO_TRIM17

IMO Trim Register (SRSSv2)

Address: 0x0FFFF1E1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

29.1.322 SFLASH_IMO_TRIM18

IMO Trim Register (SRSSv2)

Address: 0x0FFFF1E2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

29.1.323 SFLASH_IMO_TRIM19

IMO Trim Register (SRSSv2)

Address: 0x0FFFF1E3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

29.1.324 SFLASH_IMO_TRIM20

IMO Trim Register (SRSSv2)

Address: 0x0FFFF1E4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

29.1.325 SFLASH_IMO_TRIM21

IMO Trim Register (SRSSv2)

Address: 0x0FFFF1E5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

29.1.326 SFLASH_IMO_TRIM22

IMO Trim Register (SRSSv2)

Address: 0x0FFFF1E6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

29.1.327 SFLASH_IMO_TRIM23

IMO Trim Register (SRSSv2)

Address: 0x0FFFF1E7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

29.1.328 SFLASH_IMO_TRIM24

IMO Trim Register (SRSSv2)

Address: 0x0FFFF1E8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

29.1.329 SFLASH_IMO_TRIM25

IMO Trim Register (SRSSv2)

Address: 0x0FFFF1E9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

29.1.330 SFLASH_IMO_TRIM26

IMO Trim Register (SRSSv2)

Address: 0x0FFFF1EA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

29.1.331 SFLASH_IMO_TRIM27

IMO Trim Register (SRSSv2)

Address: 0x0FFFF1EB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

29.1.332 SFLASH_IMO_TRIM28

IMO Trim Register (SRSSv2)

Address: 0x0FFFF1EC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

29.1.333 SFLASH_IMO_TRIM29

IMO Trim Register (SRSSv2)

Address: 0x0FFFF1ED

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

29.1.334 SFLASH_IMO_TRIM30

IMO Trim Register (SRSSv2)

Address: 0x0FFFF1EE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

29.1.335 SFLASH_IMO_TRIM31

IMO Trim Register (SRSSv2)

Address: 0x0FFFF1EF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

29.1.336 SFLASH_IMO_TRIM32

IMO Trim Register (SRSSv2)

Address: 0x0FFFF1F0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

29.1.337 SFLASH_IMO_TRIM33

IMO Trim Register (SRSSv2)

Address: 0x0FFFF1F1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

29.1.338 SFLASH_IMO_TRIM34

IMO Trim Register (SRSSv2)

Address: 0x0FFFF1F2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

29.1.339 SFLASH_IMO_TRIM35

IMO Trim Register (SRSSv2)

Address: 0x0FFFF1F3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

29.1.340 SFLASH_IMO_TRIM36

IMO Trim Register (SRSSv2)

Address: 0x0FFFF1F4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

29.1.341 SFLASH_IMO_TRIM37

IMO Trim Register (SRSSv2)

Address: 0x0FFFF1F5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

29.1.342 SFLASH_IMO_TRIM38

IMO Trim Register (SRSSv2)

Address: 0x0FFFF1F6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

29.1.343 SFLASH_IMO_TRIM39

IMO Trim Register (SRSSv2)

Address: 0x0FFFF1F7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

29.1.344 SFLASH_IMO_TRIM40

IMO Trim Register (SRSSv2)

Address: 0x0FFFF1F8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

29.1.345 SFLASH_IMO_TRIM41

IMO Trim Register (SRSSv2)

Address: 0x0FFFF1F9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

29.1.346 SFLASH_IMO_TRIM42

IMO Trim Register (SRSSv2)

Address: 0x0FFFF1FA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

29.1.347 SFLASH_IMO_TRIM43

IMO Trim Register (SRSSv2)

Address: 0x0FFFF1FB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

29.1.348 SFLASH_IMO_TRIM44

IMO Trim Register (SRSSv2)

Address: 0x0FFFF1FC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

29.1.349 SFLASH_IMO_TRIM45

IMO Trim Register (SRSSv2)

Address: 0x0FFFF1FD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

29.1.350 SFLASH_CHECKSUM

Boot Checksum

Address: 0x0FFFF1FE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	CHECKSUM [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	CHECKSUM [15:8]							

Bits	Name	Description
15 : 0	CHECKSUM	Checksum of fixed data checked during boot. This checksum covers all of rows 1,2,3 of macro 0 + row 3 of macro 1 (except this checksum, and row 3 of macro 1 only if it exists). Default Value: X

29.1.351 SFLASH_MACRO_0_FREE_SFLASH0

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.352 SFLASH_MACRO_0_FREE_SFLASH1

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF201

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.353 SFLASH_MACRO_0_FREE_SFLASH2

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF202

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.354 SFLASH_MACRO_0_FREE_SFLASH3

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF203

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.355 SFLASH_MACRO_0_FREE_SFLASH4

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF204

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.356 SFLASH_MACRO_0_FREE_SFLASH5

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF205

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.357 SFLASH_MACRO_0_FREE_SFLASH6

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF206

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.358 SFLASH_MACRO_0_FREE_SFLASH7

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF207

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.359 SFLASH_MACRO_0_FREE_SFLASH8

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF208

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.360 SFLASH_MACRO_0_FREE_SFLASH9

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF209

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.361 SFLASH_MACRO_0_FREE_SFLASH10

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF20A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.362 SFLASH_MACRO_0_FREE_SFLASH11

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF20B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.363 SFLASH_MACRO_0_FREE_SFLASH12

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF20C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.364 SFLASH_MACRO_0_FREE_SFLASH13

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF20D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.365 SFLASH_MACRO_0_FREE_SFLASH14

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF20E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.366 SFLASH_MACRO_0_FREE_SFLASH15

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF20F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.367 SFLASH_MACRO_0_FREE_SFLASH16

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF210

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.368 SFLASH_MACRO_0_FREE_SFLASH17

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF211

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.369 SFLASH_MACRO_0_FREE_SFLASH18

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF212

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.370 SFLASH_MACRO_0_FREE_SFLASH19

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF213

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.371 SFLASH_MACRO_0_FREE_SFLASH20

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF214

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.372 SFLASH_MACRO_0_FREE_SFLASH21

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF215

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.373 SFLASH_MACRO_0_FREE_SFLASH22

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF216

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.374 SFLASH_MACRO_0_FREE_SFLASH23

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF217

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.375 SFLASH_MACRO_0_FREE_SFLASH24

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF218

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.376 SFLASH_MACRO_0_FREE_SFLASH25

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF219

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.377 SFLASH_MACRO_0_FREE_SFLASH26

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF21A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.378 SFLASH_MACRO_0_FREE_SFLASH27

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF21B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.379 SFLASH_MACRO_0_FREE_SFLASH28

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF21C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.380 SFLASH_MACRO_0_FREE_SFLASH29

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF21D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.381 SFLASH_MACRO_0_FREE_SFLASH30

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF21E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.382 SFLASH_MACRO_0_FREE_SFLASH31

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF21F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.383 SFLASH_MACRO_0_FREE_SFLASH32

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF220

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.384 SFLASH_MACRO_0_FREE_SFLASH33

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF221

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.385 SFLASH_MACRO_0_FREE_SFLASH34

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF222

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.386 SFLASH_MACRO_0_FREE_SFLASH35

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF223

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.387 SFLASH_MACRO_0_FREE_SFLASH36

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF224

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.388 SFLASH_MACRO_0_FREE_SFLASH37

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF225

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.389 SFLASH_MACRO_0_FREE_SFLASH38

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF226

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.390 SFLASH_MACRO_0_FREE_SFLASH39

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF227

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.391 SFLASH_MACRO_0_FREE_SFLASH40

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF228

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.392 SFLASH_MACRO_0_FREE_SFLASH41

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF229

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.393 SFLASH_MACRO_0_FREE_SFLASH42

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF22A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.394 SFLASH_MACRO_0_FREE_SFLASH43

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF22B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.395 SFLASH_MACRO_0_FREE_SFLASH44

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF22C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.396 SFLASH_MACRO_0_FREE_SFLASH45

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF22D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.397 SFLASH_MACRO_0_FREE_SFLASH46

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF22E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.398 SFLASH_MACRO_0_FREE_SFLASH47

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF22F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.399 SFLASH_MACRO_0_FREE_SFLASH48

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF230

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.400 SFLASH_MACRO_0_FREE_SFLASH49

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF231

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.401 SFLASH_MACRO_0_FREE_SFLASH50

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF232

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.402 SFLASH_MACRO_0_FREE_SFLASH51

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF233

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.403 SFLASH_MACRO_0_FREE_SFLASH52

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF234

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.404 SFLASH_MACRO_0_FREE_SFLASH53

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF235

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.405 SFLASH_MACRO_0_FREE_SFLASH54

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF236

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.406 SFLASH_MACRO_0_FREE_SFLASH55

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF237

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.407 SFLASH_MACRO_0_FREE_SFLASH56

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF238

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.408 SFLASH_MACRO_0_FREE_SFLASH57

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF239

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.409 SFLASH_MACRO_0_FREE_SFLASH58

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF23A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.410 SFLASH_MACRO_0_FREE_SFLASH59

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF23B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.411 SFLASH_MACRO_0_FREE_SFLASH60

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF23C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.412 SFLASH_MACRO_0_FREE_SFLASH61

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF23D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.413 SFLASH_MACRO_0_FREE_SFLASH62

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF23E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.414 SFLASH_MACRO_0_FREE_SFLASH63

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF23F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.415 SFLASH_MACRO_0_FREE_SFLASH64

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF240

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.416 SFLASH_MACRO_0_FREE_SFLASH65

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF241

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.417 SFLASH_MACRO_0_FREE_SFLASH66

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF242

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.418 SFLASH_MACRO_0_FREE_SFLASH67

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF243

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.419 SFLASH_MACRO_0_FREE_SFLASH68

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF244

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.420 SFLASH_MACRO_0_FREE_SFLASH69

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF245

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.421 SFLASH_MACRO_0_FREE_SFLASH70

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF246

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.422 SFLASH_MACRO_0_FREE_SFLASH71

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF247

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.423 SFLASH_MACRO_0_FREE_SFLASH72

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF248

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.424 SFLASH_MACRO_0_FREE_SFLASH73

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF249

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.425 SFLASH_MACRO_0_FREE_SFLASH74

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF24A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.426 SFLASH_MACRO_0_FREE_SFLASH75

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF24B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.427 SFLASH_MACRO_0_FREE_SFLASH76

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF24C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.428 SFLASH_MACRO_0_FREE_SFLASH77

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF24D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.429 SFLASH_MACRO_0_FREE_SFLASH78

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF24E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.430 SFLASH_MACRO_0_FREE_SFLASH79

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF24F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.431 SFLASH_MACRO_0_FREE_SFLASH80

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF250

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.432 SFLASH_MACRO_0_FREE_SFLASH81

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF251

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.433 SFLASH_MACRO_0_FREE_SFLASH82

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF252

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.434 SFLASH_MACRO_0_FREE_SFLASH83

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF253

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.435 SFLASH_MACRO_0_FREE_SFLASH84

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF254

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.436 SFLASH_MACRO_0_FREE_SFLASH85

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF255

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.437 SFLASH_MACRO_0_FREE_SFLASH86

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF256

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.438 SFLASH_MACRO_0_FREE_SFLASH87

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF257

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.439 SFLASH_MACRO_0_FREE_SFLASH88

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF258

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.440 SFLASH_MACRO_0_FREE_SFLASH89

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF259

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.441 SFLASH_MACRO_0_FREE_SFLASH90

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF25A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.442 SFLASH_MACRO_0_FREE_SFLASH91

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF25B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.443 SFLASH_MACRO_0_FREE_SFLASH92

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF25C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.444 SFLASH_MACRO_0_FREE_SFLASH93

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF25D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.445 SFLASH_MACRO_0_FREE_SFLASH94

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF25E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.446 SFLASH_MACRO_0_FREE_SFLASH95

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF25F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.447 SFLASH_MACRO_0_FREE_SFLASH96

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF260

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.448 SFLASH_MACRO_0_FREE_SFLASH97

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF261

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.449 SFLASH_MACRO_0_FREE_SFLASH98

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF262

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.450 SFLASH_MACRO_0_FREE_SFLASH99

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF263

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.451 SFLASH_MACRO_0_FREE_SFLASH100

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF264

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.452 SFLASH_MACRO_0_FREE_SFLASH101

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF265

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.453 SFLASH_MACRO_0_FREE_SFLASH102

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF266

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.454 SFLASH_MACRO_0_FREE_SFLASH103

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF267

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.455 SFLASH_MACRO_0_FREE_SFLASH104

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF268

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.456 SFLASH_MACRO_0_FREE_SFLASH105

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF269

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.457 SFLASH_MACRO_0_FREE_SFLASH106

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF26A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.458 SFLASH_MACRO_0_FREE_SFLASH107

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF26B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.459 SFLASH_MACRO_0_FREE_SFLASH108

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF26C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.460 SFLASH_MACRO_0_FREE_SFLASH109

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF26D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.461 SFLASH_MACRO_0_FREE_SFLASH110

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF26E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.462 SFLASH_MACRO_0_FREE_SFLASH111

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF26F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.463 SFLASH_MACRO_0_FREE_SFLASH112

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF270

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.464 SFLASH_MACRO_0_FREE_SFLASH113

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF271

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.465 SFLASH_MACRO_0_FREE_SFLASH114

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF272

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.466 SFLASH_MACRO_0_FREE_SFLASH115

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF273

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.467 SFLASH_MACRO_0_FREE_SFLASH116

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF274

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.468 SFLASH_MACRO_0_FREE_SFLASH117

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF275

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.469 SFLASH_MACRO_0_FREE_SFLASH118

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF276

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.470 SFLASH_MACRO_0_FREE_SFLASH119

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF277

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.471 SFLASH_MACRO_0_FREE_SFLASH120

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF278

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.472 SFLASH_MACRO_0_FREE_SFLASH121

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF279

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.473 SFLASH_MACRO_0_FREE_SFLASH122

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF27A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.474 SFLASH_MACRO_0_FREE_SFLASH123

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF27B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.475 SFLASH_MACRO_0_FREE_SFLASH124

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF27C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.476 SFLASH_MACRO_0_FREE_SFLASH125

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF27D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.477 SFLASH_MACRO_0_FREE_SFLASH126

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF27E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.478 SFLASH_MACRO_0_FREE_SFLASH127

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF27F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.479 SFLASH_MACRO_0_FREE_SFLASH128

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF280

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.480 SFLASH_MACRO_0_FREE_SFLASH129

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF281

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.481 SFLASH_MACRO_0_FREE_SFLASH130

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF282

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.482 SFLASH_MACRO_0_FREE_SFLASH131

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF283

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.483 SFLASH_MACRO_0_FREE_SFLASH132

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF284

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.484 SFLASH_MACRO_0_FREE_SFLASH133

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF285

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.485 SFLASH_MACRO_0_FREE_SFLASH134

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF286

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.486 SFLASH_MACRO_0_FREE_SFLASH135

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF287

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.487 SFLASH_MACRO_0_FREE_SFLASH136

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF288

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.488 SFLASH_MACRO_0_FREE_SFLASH137

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF289

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.489 SFLASH_MACRO_0_FREE_SFLASH138

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF28A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.490 SFLASH_MACRO_0_FREE_SFLASH139

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF28B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.491 SFLASH_MACRO_0_FREE_SFLASH140

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF28C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.492 SFLASH_MACRO_0_FREE_SFLASH141

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF28D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.493 SFLASH_MACRO_0_FREE_SFLASH142

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF28E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.494 SFLASH_MACRO_0_FREE_SFLASH143

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF28F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.495 SFLASH_MACRO_0_FREE_SFLASH144

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF290

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.496 SFLASH_MACRO_0_FREE_SFLASH145

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF291

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.497 SFLASH_MACRO_0_FREE_SFLASH146

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF292

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.498 SFLASH_MACRO_0_FREE_SFLASH147

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF293

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.499 SFLASH_MACRO_0_FREE_SFLASH148

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF294

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.500 SFLASH_MACRO_0_FREE_SFLASH149

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF295

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.501 SFLASH_MACRO_0_FREE_SFLASH150

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF296

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.502 SFLASH_MACRO_0_FREE_SFLASH151

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF297

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.503 SFLASH_MACRO_0_FREE_SFLASH152

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF298

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.504 SFLASH_MACRO_0_FREE_SFLASH153

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF299

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.505 SFLASH_MACRO_0_FREE_SFLASH154

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF29A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.506 SFLASH_MACRO_0_FREE_SFLASH155

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF29B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.507 SFLASH_MACRO_0_FREE_SFLASH156

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF29C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.508 SFLASH_MACRO_0_FREE_SFLASH157

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF29D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.509 SFLASH_MACRO_0_FREE_SFLASH158

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF29E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.510 SFLASH_MACRO_0_FREE_SFLASH159

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF29F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.511 SFLASH_MACRO_0_FREE_SFLASH160

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.512 SFLASH_MACRO_0_FREE_SFLASH161

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2A1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.513 SFLASH_MACRO_0_FREE_SFLASH162

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2A2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.514 SFLASH_MACRO_0_FREE_SFLASH163

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2A3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.515 SFLASH_MACRO_0_FREE_SFLASH164

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2A4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.516 SFLASH_MACRO_0_FREE_SFLASH165

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2A5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.517 SFLASH_MACRO_0_FREE_SFLASH166

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2A6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.518 SFLASH_MACRO_0_FREE_SFLASH167

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2A7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.519 SFLASH_MACRO_0_FREE_SFLASH168

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2A8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.520 SFLASH_MACRO_0_FREE_SFLASH169

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2A9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.521 SFLASH_MACRO_0_FREE_SFLASH170

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2AA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.522 SFLASH_MACRO_0_FREE_SFLASH171

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2AB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.523 SFLASH_MACRO_0_FREE_SFLASH172

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2AC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.524 SFLASH_MACRO_0_FREE_SFLASH173

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2AD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.525 SFLASH_MACRO_0_FREE_SFLASH174

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2AE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.526 SFLASH_MACRO_0_FREE_SFLASH175

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2AF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.527 SFLASH_MACRO_0_FREE_SFLASH176

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2B0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.528 SFLASH_MACRO_0_FREE_SFLASH177

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2B1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.529 SFLASH_MACRO_0_FREE_SFLASH178

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2B2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.530 SFLASH_MACRO_0_FREE_SFLASH179

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2B3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.531 SFLASH_MACRO_0_FREE_SFLASH180

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2B4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.532 SFLASH_MACRO_0_FREE_SFLASH181

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2B5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.533 SFLASH_MACRO_0_FREE_SFLASH182

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2B6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.534 SFLASH_MACRO_0_FREE_SFLASH183

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2B7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.535 SFLASH_MACRO_0_FREE_SFLASH184

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2B8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.536 SFLASH_MACRO_0_FREE_SFLASH185

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2B9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.537 SFLASH_MACRO_0_FREE_SFLASH186

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2BA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.538 SFLASH_MACRO_0_FREE_SFLASH187

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2BB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.539 SFLASH_MACRO_0_FREE_SFLASH188

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2BC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.540 SFLASH_MACRO_0_FREE_SFLASH189

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2BD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.541 SFLASH_MACRO_0_FREE_SFLASH190

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2BE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.542 SFLASH_MACRO_0_FREE_SFLASH191

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2BF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.543 SFLASH_MACRO_0_FREE_SFLASH192

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.544 SFLASH_MACRO_0_FREE_SFLASH193

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2C1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.545 SFLASH_MACRO_0_FREE_SFLASH194

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2C2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.546 SFLASH_MACRO_0_FREE_SFLASH195

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2C3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.547 SFLASH_MACRO_0_FREE_SFLASH196

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.548 SFLASH_MACRO_0_FREE_SFLASH197

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2C5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.549 SFLASH_MACRO_0_FREE_SFLASH198

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2C6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.550 SFLASH_MACRO_0_FREE_SFLASH199

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2C7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.551 SFLASH_MACRO_0_FREE_SFLASH200

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2C8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.552 SFLASH_MACRO_0_FREE_SFLASH201

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2C9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.553 SFLASH_MACRO_0_FREE_SFLASH202

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2CA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.554 SFLASH_MACRO_0_FREE_SFLASH203

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2CB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.555 SFLASH_MACRO_0_FREE_SFLASH204

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2CC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.556 SFLASH_MACRO_0_FREE_SFLASH205

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2CD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.557 SFLASH_MACRO_0_FREE_SFLASH206

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2CE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.558 SFLASH_MACRO_0_FREE_SFLASH207

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2CF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.559 SFLASH_MACRO_0_FREE_SFLASH208

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2D0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.560 SFLASH_MACRO_0_FREE_SFLASH209

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2D1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.561 SFLASH_MACRO_0_FREE_SFLASH210

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2D2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.562 SFLASH_MACRO_0_FREE_SFLASH211

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2D3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.563 SFLASH_MACRO_0_FREE_SFLASH212

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2D4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.564 SFLASH_MACRO_0_FREE_SFLASH213

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2D5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.565 SFLASH_MACRO_0_FREE_SFLASH214

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2D6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.566 SFLASH_MACRO_0_FREE_SFLASH215

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2D7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.567 SFLASH_MACRO_0_FREE_SFLASH216

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2D8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.568 SFLASH_MACRO_0_FREE_SFLASH217

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2D9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.569 SFLASH_MACRO_0_FREE_SFLASH218

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2DA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.570 SFLASH_MACRO_0_FREE_SFLASH219

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2DB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.571 SFLASH_MACRO_0_FREE_SFLASH220

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2DC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.572 SFLASH_MACRO_0_FREE_SFLASH221

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2DD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.573 SFLASH_MACRO_0_FREE_SFLASH222

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2DE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.574 SFLASH_MACRO_0_FREE_SFLASH223

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2DF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.575 SFLASH_MACRO_0_FREE_SFLASH224

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.576 SFLASH_MACRO_0_FREE_SFLASH225

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2E1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.577 SFLASH_MACRO_0_FREE_SFLASH226

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2E2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.578 SFLASH_MACRO_0_FREE_SFLASH227

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2E3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.579 SFLASH_MACRO_0_FREE_SFLASH228

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2E4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.580 SFLASH_MACRO_0_FREE_SFLASH229

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2E5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.581 SFLASH_MACRO_0_FREE_SFLASH230

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2E6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.582 SFLASH_MACRO_0_FREE_SFLASH231

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2E7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.583 SFLASH_MACRO_0_FREE_SFLASH232

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2E8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.584 SFLASH_MACRO_0_FREE_SFLASH233

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2E9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.585 SFLASH_MACRO_0_FREE_SFLASH234

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2EA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.586 SFLASH_MACRO_0_FREE_SFLASH235

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2EB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.587 SFLASH_MACRO_0_FREE_SFLASH236

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2EC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.588 SFLASH_MACRO_0_FREE_SFLASH237

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2ED

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.589 SFLASH_MACRO_0_FREE_SFLASH238

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2EE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.590 SFLASH_MACRO_0_FREE_SFLASH239

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2EF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.591 SFLASH_MACRO_0_FREE_SFLASH240

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2F0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.592 SFLASH_MACRO_0_FREE_SFLASH241

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2F1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.593 SFLASH_MACRO_0_FREE_SFLASH242

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2F2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.594 SFLASH_MACRO_0_FREE_SFLASH243

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2F3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.595 SFLASH_MACRO_0_FREE_SFLASH244

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2F4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.596 SFLASH_MACRO_0_FREE_SFLASH245

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2F5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.597 SFLASH_MACRO_0_FREE_SFLASH246

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2F6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.598 SFLASH_MACRO_0_FREE_SFLASH247

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2F7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.599 SFLASH_MACRO_0_FREE_SFLASH248

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2F8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.600 SFLASH_MACRO_0_FREE_SFLASH249

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2F9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.601 SFLASH_MACRO_0_FREE_SFLASH250

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2FA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.602 SFLASH_MACRO_0_FREE_SFLASH251

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2FB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.603 SFLASH_MACRO_0_FREE_SFLASH252

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2FC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.604 SFLASH_MACRO_0_FREE_SFLASH253

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2FD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.605 SFLASH_MACRO_0_FREE_SFLASH254

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2FE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.606 SFLASH_MACRO_0_FREE_SFLASH255

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF2FF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.607 SFLASH_MACRO_0_FREE_SFLASH256

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF300

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.608 SFLASH_MACRO_0_FREE_SFLASH257

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF301

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.609 SFLASH_MACRO_0_FREE_SFLASH258

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF302

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.610 SFLASH_MACRO_0_FREE_SFLASH259

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF303

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.611 SFLASH_MACRO_0_FREE_SFLASH260

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF304

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.612 SFLASH_MACRO_0_FREE_SFLASH261

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF305

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.613 SFLASH_MACRO_0_FREE_SFLASH262

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF306

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.614 SFLASH_MACRO_0_FREE_SFLASH263

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF307

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.615 SFLASH_MACRO_0_FREE_SFLASH264

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF308

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.616 SFLASH_MACRO_0_FREE_SFLASH265

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF309

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.617 SFLASH_MACRO_0_FREE_SFLASH266

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF30A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.618 SFLASH_MACRO_0_FREE_SFLASH267

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF30B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.619 SFLASH_MACRO_0_FREE_SFLASH268

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF30C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.620 SFLASH_MACRO_0_FREE_SFLASH269

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF30D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.621 SFLASH_MACRO_0_FREE_SFLASH270

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF30E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.622 SFLASH_MACRO_0_FREE_SFLASH271

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF30F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.623 SFLASH_MACRO_0_FREE_SFLASH272

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF310

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.624 SFLASH_MACRO_0_FREE_SFLASH273

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF311

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.625 SFLASH_MACRO_0_FREE_SFLASH274

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF312

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.626 SFLASH_MACRO_0_FREE_SFLASH275

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF313

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.627 SFLASH_MACRO_0_FREE_SFLASH276

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF314

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.628 SFLASH_MACRO_0_FREE_SFLASH277

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF315

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.629 SFLASH_MACRO_0_FREE_SFLASH278

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF316

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.630 SFLASH_MACRO_0_FREE_SFLASH279

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF317

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.631 SFLASH_MACRO_0_FREE_SFLASH280

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF318

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.632 SFLASH_MACRO_0_FREE_SFLASH281

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF319

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.633 SFLASH_MACRO_0_FREE_SFLASH282

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF31A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.634 SFLASH_MACRO_0_FREE_SFLASH283

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF31B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.635 SFLASH_MACRO_0_FREE_SFLASH284

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF31C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.636 SFLASH_MACRO_0_FREE_SFLASH285

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF31D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.637 SFLASH_MACRO_0_FREE_SFLASH286

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF31E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.638 SFLASH_MACRO_0_FREE_SFLASH287

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF31F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.639 SFLASH_MACRO_0_FREE_SFLASH288

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF320

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.640 SFLASH_MACRO_0_FREE_SFLASH289

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF321

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.641 SFLASH_MACRO_0_FREE_SFLASH290

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF322

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.642 SFLASH_MACRO_0_FREE_SFLASH291

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF323

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.643 SFLASH_MACRO_0_FREE_SFLASH292

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF324

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.644 SFLASH_MACRO_0_FREE_SFLASH293

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF325

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.645 SFLASH_MACRO_0_FREE_SFLASH294

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF326

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.646 SFLASH_MACRO_0_FREE_SFLASH295

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF327

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.647 SFLASH_MACRO_0_FREE_SFLASH296

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF328

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.648 SFLASH_MACRO_0_FREE_SFLASH297

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF329

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.649 SFLASH_MACRO_0_FREE_SFLASH298

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF32A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.650 SFLASH_MACRO_0_FREE_SFLASH299

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF32B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.651 SFLASH_MACRO_0_FREE_SFLASH300

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF32C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.652 SFLASH_MACRO_0_FREE_SFLASH301

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF32D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.653 SFLASH_MACRO_0_FREE_SFLASH302

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF32E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.654 SFLASH_MACRO_0_FREE_SFLASH303

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF32F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.655 SFLASH_MACRO_0_FREE_SFLASH304

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF330

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.656 SFLASH_MACRO_0_FREE_SFLASH305

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF331

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.657 SFLASH_MACRO_0_FREE_SFLASH306

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF332

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.658 SFLASH_MACRO_0_FREE_SFLASH307

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF333

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.659 SFLASH_MACRO_0_FREE_SFLASH308

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF334

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.660 SFLASH_MACRO_0_FREE_SFLASH309

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF335

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.661 SFLASH_MACRO_0_FREE_SFLASH310

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF336

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.662 SFLASH_MACRO_0_FREE_SFLASH311

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF337

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.663 SFLASH_MACRO_0_FREE_SFLASH312

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF338

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.664 SFLASH_MACRO_0_FREE_SFLASH313

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF339

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.665 SFLASH_MACRO_0_FREE_SFLASH314

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF33A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.666 SFLASH_MACRO_0_FREE_SFLASH315

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF33B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.667 SFLASH_MACRO_0_FREE_SFLASH316

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF33C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.668 SFLASH_MACRO_0_FREE_SFLASH317

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF33D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.669 SFLASH_MACRO_0_FREE_SFLASH318

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF33E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.670 SFLASH_MACRO_0_FREE_SFLASH319

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF33F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.671 SFLASH_MACRO_0_FREE_SFLASH320

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF340

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.672 SFLASH_MACRO_0_FREE_SFLASH321

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF341

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.673 SFLASH_MACRO_0_FREE_SFLASH322

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF342

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.674 SFLASH_MACRO_0_FREE_SFLASH323

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF343

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.675 SFLASH_MACRO_0_FREE_SFLASH324

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF344

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.676 SFLASH_MACRO_0_FREE_SFLASH325

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF345

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.677 SFLASH_MACRO_0_FREE_SFLASH326

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF346

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.678 SFLASH_MACRO_0_FREE_SFLASH327

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF347

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.679 SFLASH_MACRO_0_FREE_SFLASH328

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF348

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.680 SFLASH_MACRO_0_FREE_SFLASH329

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF349

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.681 SFLASH_MACRO_0_FREE_SFLASH330

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF34A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.682 SFLASH_MACRO_0_FREE_SFLASH331

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF34B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.683 SFLASH_MACRO_0_FREE_SFLASH332

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF34C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.684 SFLASH_MACRO_0_FREE_SFLASH333

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF34D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.685 SFLASH_MACRO_0_FREE_SFLASH334

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF34E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.686 SFLASH_MACRO_0_FREE_SFLASH335

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF34F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.687 SFLASH_MACRO_0_FREE_SFLASH336

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF350

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.688 SFLASH_MACRO_0_FREE_SFLASH337

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF351

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.689 SFLASH_MACRO_0_FREE_SFLASH338

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF352

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.690 SFLASH_MACRO_0_FREE_SFLASH339

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF353

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.691 SFLASH_MACRO_0_FREE_SFLASH340

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF354

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.692 SFLASH_MACRO_0_FREE_SFLASH341

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF355

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.693 SFLASH_MACRO_0_FREE_SFLASH342

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF356

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.694 SFLASH_MACRO_0_FREE_SFLASH343

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF357

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.695 SFLASH_MACRO_0_FREE_SFLASH344

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF358

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.696 SFLASH_MACRO_0_FREE_SFLASH345

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF359

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.697 SFLASH_MACRO_0_FREE_SFLASH346

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF35A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.698 SFLASH_MACRO_0_FREE_SFLASH347

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF35B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.699 SFLASH_MACRO_0_FREE_SFLASH348

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF35C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.700 SFLASH_MACRO_0_FREE_SFLASH349

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF35D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.701 SFLASH_MACRO_0_FREE_SFLASH350

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF35E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.702 SFLASH_MACRO_0_FREE_SFLASH351

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF35F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.703 SFLASH_MACRO_0_FREE_SFLASH352

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF360

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.704 SFLASH_MACRO_0_FREE_SFLASH353

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF361

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.705 SFLASH_MACRO_0_FREE_SFLASH354

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF362

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.706 SFLASH_MACRO_0_FREE_SFLASH355

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF363

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.707 SFLASH_MACRO_0_FREE_SFLASH356

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF364

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.708 SFLASH_MACRO_0_FREE_SFLASH357

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF365

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.709 SFLASH_MACRO_0_FREE_SFLASH358

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF366

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.710 SFLASH_MACRO_0_FREE_SFLASH359

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF367

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.711 SFLASH_MACRO_0_FREE_SFLASH360

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF368

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.712 SFLASH_MACRO_0_FREE_SFLASH361

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF369

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.713 SFLASH_MACRO_0_FREE_SFLASH362

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF36A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.714 SFLASH_MACRO_0_FREE_SFLASH363

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF36B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.715 SFLASH_MACRO_0_FREE_SFLASH364

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF36C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.716 SFLASH_MACRO_0_FREE_SFLASH365

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF36D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.717 SFLASH_MACRO_0_FREE_SFLASH366

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF36E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.718 SFLASH_MACRO_0_FREE_SFLASH367

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF36F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.719 SFLASH_MACRO_0_FREE_SFLASH368

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF370

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.720 SFLASH_MACRO_0_FREE_SFLASH369

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF371

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.721 SFLASH_MACRO_0_FREE_SFLASH370

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF372

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.722 SFLASH_MACRO_0_FREE_SFLASH371

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF373

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.723 SFLASH_MACRO_0_FREE_SFLASH372

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF374

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.724 SFLASH_MACRO_0_FREE_SFLASH373

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF375

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.725 SFLASH_MACRO_0_FREE_SFLASH374

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF376

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.726 SFLASH_MACRO_0_FREE_SFLASH375

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF377

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.727 SFLASH_MACRO_0_FREE_SFLASH376

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF378

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.728 SFLASH_MACRO_0_FREE_SFLASH377

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF379

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.729 SFLASH_MACRO_0_FREE_SFLASH378

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF37A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.730 SFLASH_MACRO_0_FREE_SFLASH379

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF37B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.731 SFLASH_MACRO_0_FREE_SFLASH380

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF37C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.732 SFLASH_MACRO_0_FREE_SFLASH381

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF37D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.733 SFLASH_MACRO_0_FREE_SFLASH382

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF37E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.734 SFLASH_MACRO_0_FREE_SFLASH383

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF37F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.735 SFLASH_MACRO_0_FREE_SFLASH384

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF380

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.736 SFLASH_MACRO_0_FREE_SFLASH385

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF381

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.737 SFLASH_MACRO_0_FREE_SFLASH386

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF382

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.738 SFLASH_MACRO_0_FREE_SFLASH387

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF383

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.739 SFLASH_MACRO_0_FREE_SFLASH388

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF384

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.740 SFLASH_MACRO_0_FREE_SFLASH389

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF385

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.741 SFLASH_MACRO_0_FREE_SFLASH390

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF386

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.742 SFLASH_MACRO_0_FREE_SFLASH391

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF387

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.743 SFLASH_MACRO_0_FREE_SFLASH392

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF388

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.744 SFLASH_MACRO_0_FREE_SFLASH393

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF389

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.745 SFLASH_MACRO_0_FREE_SFLASH394

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF38A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.746 SFLASH_MACRO_0_FREE_SFLASH395

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF38B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.747 SFLASH_MACRO_0_FREE_SFLASH396

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF38C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.748 SFLASH_MACRO_0_FREE_SFLASH397

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF38D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.749 SFLASH_MACRO_0_FREE_SFLASH398

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF38E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.750 SFLASH_MACRO_0_FREE_SFLASH399

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF38F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.751 SFLASH_MACRO_0_FREE_SFLASH400

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF390

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.752 SFLASH_MACRO_0_FREE_SFLASH401

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF391

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.753 SFLASH_MACRO_0_FREE_SFLASH402

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF392

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.754 SFLASH_MACRO_0_FREE_SFLASH403

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF393

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.755 SFLASH_MACRO_0_FREE_SFLASH404

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF394

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.756 SFLASH_MACRO_0_FREE_SFLASH405

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF395

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.757 SFLASH_MACRO_0_FREE_SFLASH406

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF396

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.758 SFLASH_MACRO_0_FREE_SFLASH407

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF397

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.759 SFLASH_MACRO_0_FREE_SFLASH408

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF398

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.760 SFLASH_MACRO_0_FREE_SFLASH409

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF399

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.761 SFLASH_MACRO_0_FREE_SFLASH410

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF39A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.762 SFLASH_MACRO_0_FREE_SFLASH411

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF39B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.763 SFLASH_MACRO_0_FREE_SFLASH412

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF39C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.764 SFLASH_MACRO_0_FREE_SFLASH413

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF39D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.765 SFLASH_MACRO_0_FREE_SFLASH414

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF39E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.766 SFLASH_MACRO_0_FREE_SFLASH415

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF39F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.767 SFLASH_MACRO_0_FREE_SFLASH416

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.768 SFLASH_MACRO_0_FREE_SFLASH417

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3A1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.769 SFLASH_MACRO_0_FREE_SFLASH418

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3A2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.770 SFLASH_MACRO_0_FREE_SFLASH419

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3A3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.771 SFLASH_MACRO_0_FREE_SFLASH420

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3A4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.772 SFLASH_MACRO_0_FREE_SFLASH421

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3A5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.773 SFLASH_MACRO_0_FREE_SFLASH422

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3A6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.774 SFLASH_MACRO_0_FREE_SFLASH423

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3A7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.775 SFLASH_MACRO_0_FREE_SFLASH424

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3A8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.776 SFLASH_MACRO_0_FREE_SFLASH425

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3A9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.777 SFLASH_MACRO_0_FREE_SFLASH426

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3AA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.778 SFLASH_MACRO_0_FREE_SFLASH427

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3AB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.779 SFLASH_MACRO_0_FREE_SFLASH428

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3AC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.780 SFLASH_MACRO_0_FREE_SFLASH429

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3AD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.781 SFLASH_MACRO_0_FREE_SFLASH430

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3AE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.782 SFLASH_MACRO_0_FREE_SFLASH431

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3AF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.783 SFLASH_MACRO_0_FREE_SFLASH432

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3B0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.784 SFLASH_MACRO_0_FREE_SFLASH433

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3B1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.785 SFLASH_MACRO_0_FREE_SFLASH434

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3B2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.786 SFLASH_MACRO_0_FREE_SFLASH435

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3B3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.787 SFLASH_MACRO_0_FREE_SFLASH436

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3B4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.788 SFLASH_MACRO_0_FREE_SFLASH437

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3B5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.789 SFLASH_MACRO_0_FREE_SFLASH438

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3B6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.790 SFLASH_MACRO_0_FREE_SFLASH439

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3B7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.791 SFLASH_MACRO_0_FREE_SFLASH440

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3B8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.792 SFLASH_MACRO_0_FREE_SFLASH441

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3B9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.793 SFLASH_MACRO_0_FREE_SFLASH442

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3BA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.794 SFLASH_MACRO_0_FREE_SFLASH443

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3BB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.795 SFLASH_MACRO_0_FREE_SFLASH444

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3BC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.796 SFLASH_MACRO_0_FREE_SFLASH445

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3BD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.797 SFLASH_MACRO_0_FREE_SFLASH446

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3BE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.798 SFLASH_MACRO_0_FREE_SFLASH447

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3BF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.799 SFLASH_MACRO_0_FREE_SFLASH448

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.800 SFLASH_MACRO_0_FREE_SFLASH449

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3C1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.801 SFLASH_MACRO_0_FREE_SFLASH450

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3C2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.802 SFLASH_MACRO_0_FREE_SFLASH451

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3C3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.803 SFLASH_MACRO_0_FREE_SFLASH452

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.804 SFLASH_MACRO_0_FREE_SFLASH453

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3C5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.805 SFLASH_MACRO_0_FREE_SFLASH454

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3C6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.806 SFLASH_MACRO_0_FREE_SFLASH455

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3C7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.807 SFLASH_MACRO_0_FREE_SFLASH456

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3C8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.808 SFLASH_MACRO_0_FREE_SFLASH457

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3C9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.809 SFLASH_MACRO_0_FREE_SFLASH458

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3CA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.810 SFLASH_MACRO_0_FREE_SFLASH459

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3CB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.811 SFLASH_MACRO_0_FREE_SFLASH460

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3CC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.812 SFLASH_MACRO_0_FREE_SFLASH461

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3CD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.813 SFLASH_MACRO_0_FREE_SFLASH462

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3CE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.814 SFLASH_MACRO_0_FREE_SFLASH463

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3CF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.815 SFLASH_MACRO_0_FREE_SFLASH464

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3D0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.816 SFLASH_MACRO_0_FREE_SFLASH465

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3D1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.817 SFLASH_MACRO_0_FREE_SFLASH466

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3D2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.818 SFLASH_MACRO_0_FREE_SFLASH467

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3D3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.819 SFLASH_MACRO_0_FREE_SFLASH468

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3D4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.820 SFLASH_MACRO_0_FREE_SFLASH469

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3D5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.821 SFLASH_MACRO_0_FREE_SFLASH470

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3D6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.822 SFLASH_MACRO_0_FREE_SFLASH471

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3D7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.823 SFLASH_MACRO_0_FREE_SFLASH472

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3D8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.824 SFLASH_MACRO_0_FREE_SFLASH473

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3D9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.825 SFLASH_MACRO_0_FREE_SFLASH474

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3DA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.826 SFLASH_MACRO_0_FREE_SFLASH475

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3DB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.827 SFLASH_MACRO_0_FREE_SFLASH476

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3DC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.828 SFLASH_MACRO_0_FREE_SFLASH477

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3DD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.829 SFLASH_MACRO_0_FREE_SFLASH478

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3DE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.830 SFLASH_MACRO_0_FREE_SFLASH479

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3DF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.831 SFLASH_MACRO_0_FREE_SFLASH480

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.832 SFLASH_MACRO_0_FREE_SFLASH481

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3E1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.833 SFLASH_MACRO_0_FREE_SFLASH482

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3E2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.834 SFLASH_MACRO_0_FREE_SFLASH483

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3E3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.835 SFLASH_MACRO_0_FREE_SFLASH484

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3E4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.836 SFLASH_MACRO_0_FREE_SFLASH485

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3E5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.837 SFLASH_MACRO_0_FREE_SFLASH486

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3E6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.838 SFLASH_MACRO_0_FREE_SFLASH487

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3E7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.839 SFLASH_MACRO_0_FREE_SFLASH488

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3E8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.840 SFLASH_MACRO_0_FREE_SFLASH489

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3E9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.841 SFLASH_MACRO_0_FREE_SFLASH490

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3EA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.842 SFLASH_MACRO_0_FREE_SFLASH491

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3EB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.843 SFLASH_MACRO_0_FREE_SFLASH492

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3EC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.844 SFLASH_MACRO_0_FREE_SFLASH493

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3ED

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.845 SFLASH_MACRO_0_FREE_SFLASH494

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3EE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.846 SFLASH_MACRO_0_FREE_SFLASH495

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3EF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.847 SFLASH_MACRO_0_FREE_SFLASH496

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3F0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.848 SFLASH_MACRO_0_FREE_SFLASH497

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3F1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.849 SFLASH_MACRO_0_FREE_SFLASH498

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3F2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.850 SFLASH_MACRO_0_FREE_SFLASH499

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3F3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.851 SFLASH_MACRO_0_FREE_SFLASH500

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3F4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.852 SFLASH_MACRO_0_FREE_SFLASH501

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3F5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.853 SFLASH_MACRO_0_FREE_SFLASH502

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3F6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.854 SFLASH_MACRO_0_FREE_SFLASH503

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3F7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.855 SFLASH_MACRO_0_FREE_SFLASH504

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3F8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.856 SFLASH_MACRO_0_FREE_SFLASH505

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3F9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.857 SFLASH_MACRO_0_FREE_SFLASH506

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3FA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.858 SFLASH_MACRO_0_FREE_SFLASH507

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3FB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.859 SFLASH_MACRO_0_FREE_SFLASH508

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3FC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.860 SFLASH_MACRO_0_FREE_SFLASH509

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3FD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.861 SFLASH_MACRO_0_FREE_SFLASH510

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3FE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.862 SFLASH_MACRO_0_FREE_SFLASH511

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF3FF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

29.1.863 SFLASH_ALT_PROT_ROW0

Per Page Write Protection

Address: 0x0FFFF400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.864 SFLASH_ALT_PROT_ROW1

Per Page Write Protection

Address: 0x0FFFF401

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.865 SFLASH_ALT_PROT_ROW2

Per Page Write Protection

Address: 0x0FFFF402

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.866 SFLASH_ALT_PROT_ROW3

Per Page Write Protection

Address: 0x0FFFF403

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.867 SFLASH_ALT_PROT_ROW4

Per Page Write Protection

Address: 0x0FFFF404

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.868 SFLASH_ALT_PROT_ROW5

Per Page Write Protection

Address: 0x0FFFF405

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.869 SFLASH_ALT_PROT_ROW6

Per Page Write Protection

Address: 0x0FFFF406

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.870 SFLASH_ALT_PROT_ROW7

Per Page Write Protection

Address: 0x0FFFF407

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.871 SFLASH_ALT_PROT_ROW8

Per Page Write Protection

Address: 0x0FFFF408

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.872 SFLASH_ALT_PROT_ROW9

Per Page Write Protection

Address: 0x0FFFF409

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.873 SFLASH_ALT_PROT_ROW10

Per Page Write Protection

Address: 0x0FFFF40A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.874 SFLASH_ALT_PROT_ROW11

Per Page Write Protection

Address: 0x0FFFF40B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.875 SFLASH_ALT_PROT_ROW12

Per Page Write Protection

Address: 0x0FFFF40C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.876 SFLASH_ALT_PROT_ROW13

Per Page Write Protection

Address: 0x0FFFF40D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.877 SFLASH_ALT_PROT_ROW14

Per Page Write Protection

Address: 0x0FFFF40E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.878 SFLASH_ALT_PROT_ROW15

Per Page Write Protection

Address: 0x0FFFF40F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.879 SFLASH_ALT_PROT_ROW16

Per Page Write Protection

Address: 0x0FFFF410

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.880 SFLASH_ALT_PROT_ROW17

Per Page Write Protection

Address: 0x0FFFF411

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.881 SFLASH_ALT_PROT_ROW18

Per Page Write Protection

Address: 0x0FFFF412

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.882 SFLASH_ALT_PROT_ROW19

Per Page Write Protection

Address: 0x0FFFF413

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.883 SFLASH_ALT_PROT_ROW20

Per Page Write Protection

Address: 0x0FFFF414

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.884 SFLASH_ALT_PROT_ROW21

Per Page Write Protection

Address: 0x0FFFF415

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.885 SFLASH_ALT_PROT_ROW22

Per Page Write Protection

Address: 0x0FFFF416

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.886 SFLASH_ALT_PROT_ROW23

Per Page Write Protection

Address: 0x0FFFF417

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.887 SFLASH_ALT_PROT_ROW24

Per Page Write Protection

Address: 0x0FFFF418

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.888 SFLASH_ALT_PROT_ROW25

Per Page Write Protection

Address: 0x0FFFF419

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.889 SFLASH_ALT_PROT_ROW26

Per Page Write Protection

Address: 0x0FFFF41A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.890 SFLASH_ALT_PROT_ROW27

Per Page Write Protection

Address: 0x0FFFF41B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.891 SFLASH_ALT_PROT_ROW28

Per Page Write Protection

Address: 0x0FFFF41C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.892 SFLASH_ALT_PROT_ROW29

Per Page Write Protection

Address: 0x0FFFF41D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.893 SFLASH_ALT_PROT_ROW30

Per Page Write Protection

Address: 0x0FFFF41E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.894 SFLASH_ALT_PROT_ROW31

Per Page Write Protection

Address: 0x0FFFF41F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.895 SFLASH_ALT_PROT_ROW32

Per Page Write Protection

Address: 0x0FFFF420

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.896 SFLASH_ALT_PROT_ROW33

Per Page Write Protection

Address: 0x0FFFF421

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.897 SFLASH_ALT_PROT_ROW34

Per Page Write Protection

Address: 0x0FFFF422

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.898 SFLASH_ALT_PROT_ROW35

Per Page Write Protection

Address: 0x0FFFF423

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.899 SFLASH_ALT_PROT_ROW36

Per Page Write Protection

Address: 0x0FFFF424

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.900 SFLASH_ALT_PROT_ROW37

Per Page Write Protection

Address: 0x0FFFF425

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.901 SFLASH_ALT_PROT_ROW38

Per Page Write Protection

Address: 0x0FFFF426

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.902 SFLASH_ALT_PROT_ROW39

Per Page Write Protection

Address: 0x0FFFF427

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.903 SFLASH_ALT_PROT_ROW40

Per Page Write Protection

Address: 0x0FFFF428

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.904 SFLASH_ALT_PROT_ROW41

Per Page Write Protection

Address: 0x0FFFF429

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.905 SFLASH_ALT_PROT_ROW42

Per Page Write Protection

Address: 0x0FFFF42A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.906 SFLASH_ALT_PROT_ROW43

Per Page Write Protection

Address: 0x0FFFF42B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.907 SFLASH_ALT_PROT_ROW44

Per Page Write Protection

Address: 0x0FFFF42C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.908 SFLASH_ALT_PROT_ROW45

Per Page Write Protection

Address: 0x0FFFF42D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.909 SFLASH_ALT_PROT_ROW46

Per Page Write Protection

Address: 0x0FFFF42E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.910 SFLASH_ALT_PROT_ROW47

Per Page Write Protection

Address: 0x0FFFF42F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.911 SFLASH_ALT_PROT_ROW48

Per Page Write Protection

Address: 0x0FFFF430

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.912 SFLASH_ALT_PROT_ROW49

Per Page Write Protection

Address: 0x0FFFF431

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.913 SFLASH_ALT_PROT_ROW50

Per Page Write Protection

Address: 0x0FFFF432

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.914 SFLASH_ALT_PROT_ROW51

Per Page Write Protection

Address: 0x0FFFF433

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.915 SFLASH_ALT_PROT_ROW52

Per Page Write Protection

Address: 0x0FFFF434

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.916 SFLASH_ALT_PROT_ROW53

Per Page Write Protection

Address: 0x0FFFF435

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.917 SFLASH_ALT_PROT_ROW54

Per Page Write Protection

Address: 0x0FFFF436

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.918 SFLASH_ALT_PROT_ROW55

Per Page Write Protection

Address: 0x0FFFF437

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.919 SFLASH_ALT_PROT_ROW56

Per Page Write Protection

Address: 0x0FFFF438

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.920 SFLASH_ALT_PROT_ROW57

Per Page Write Protection

Address: 0x0FFFF439

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.921 SFLASH_ALT_PROT_ROW58

Per Page Write Protection

Address: 0x0FFFF43A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.922 SFLASH_ALT_PROT_ROW59

Per Page Write Protection

Address: 0x0FFFF43B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.923 SFLASH_ALT_PROT_ROW60

Per Page Write Protection

Address: 0x0FFFF43C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.924 SFLASH_ALT_PROT_ROW61

Per Page Write Protection

Address: 0x0FFFF43D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.925 SFLASH_ALT_PROT_ROW62

Per Page Write Protection

Address: 0x0FFFF43E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.926 SFLASH_ALT_PROT_ROW63

Per Page Write Protection

Address: 0x0FFFF43F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.927 SFLASH_ALT_PROT_ROW64

Per Page Write Protection

Address: 0x0FFFF440

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.928 SFLASH_ALT_PROT_ROW65

Per Page Write Protection

Address: 0x0FFFF441

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.929 SFLASH_ALT_PROT_ROW66

Per Page Write Protection

Address: 0x0FFFF442

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.930 SFLASH_ALT_PROT_ROW67

Per Page Write Protection

Address: 0x0FFFF443

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.931 SFLASH_ALT_PROT_ROW68

Per Page Write Protection

Address: 0x0FFFF444

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.932 SFLASH_ALT_PROT_ROW69

Per Page Write Protection

Address: 0x0FFFF445

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.933 SFLASH_ALT_PROT_ROW70

Per Page Write Protection

Address: 0x0FFFF446

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.934 SFLASH_ALT_PROT_ROW71

Per Page Write Protection

Address: 0x0FFFF447

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.935 SFLASH_ALT_PROT_ROW72

Per Page Write Protection

Address: 0x0FFFF448

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.936 SFLASH_ALT_PROT_ROW73

Per Page Write Protection

Address: 0x0FFFF449

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.937 SFLASH_ALT_PROT_ROW74

Per Page Write Protection

Address: 0x0FFFF44A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.938 SFLASH_ALT_PROT_ROW75

Per Page Write Protection

Address: 0x0FFFF44B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.939 SFLASH_ALT_PROT_ROW76

Per Page Write Protection

Address: 0x0FFFF44C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.940 SFLASH_ALT_PROT_ROW77

Per Page Write Protection

Address: 0x0FFFF44D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.941 SFLASH_ALT_PROT_ROW78

Per Page Write Protection

Address: 0x0FFFF44E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.942 SFLASH_ALT_PROT_ROW79

Per Page Write Protection

Address: 0x0FFFF44F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.943 SFLASH_ALT_PROT_ROW80

Per Page Write Protection

Address: 0x0FFFF450

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.944 SFLASH_ALT_PROT_ROW81

Per Page Write Protection

Address: 0x0FFFF451

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.945 SFLASH_ALT_PROT_ROW82

Per Page Write Protection

Address: 0x0FFFF452

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.946 SFLASH_ALT_PROT_ROW83

Per Page Write Protection

Address: 0x0FFFF453

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.947 SFLASH_ALT_PROT_ROW84

Per Page Write Protection

Address: 0x0FFFF454

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.948 SFLASH_ALT_PROT_ROW85

Per Page Write Protection

Address: 0x0FFFF455

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.949 SFLASH_ALT_PROT_ROW86

Per Page Write Protection

Address: 0x0FFFF456

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.950 SFLASH_ALT_PROT_ROW87

Per Page Write Protection

Address: 0x0FFFF457

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.951 SFLASH_ALT_PROT_ROW88

Per Page Write Protection

Address: 0x0FFFF458

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.952 SFLASH_ALT_PROT_ROW89

Per Page Write Protection

Address: 0x0FFFF459

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.953 SFLASH_ALT_PROT_ROW90

Per Page Write Protection

Address: 0x0FFFF45A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.954 SFLASH_ALT_PROT_ROW91

Per Page Write Protection

Address: 0x0FFFF45B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.955 SFLASH_ALT_PROT_ROW92

Per Page Write Protection

Address: 0x0FFFF45C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.956 SFLASH_ALT_PROT_ROW93

Per Page Write Protection

Address: 0x0FFFF45D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.957 SFLASH_ALT_PROT_ROW94

Per Page Write Protection

Address: 0x0FFFF45E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.958 SFLASH_ALT_PROT_ROW95

Per Page Write Protection

Address: 0x0FFFF45F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.959 SFLASH_ALT_PROT_ROW96

Per Page Write Protection

Address: 0x0FFFF460

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.960 SFLASH_ALT_PROT_ROW97

Per Page Write Protection

Address: 0x0FFFF461

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.961 SFLASH_ALT_PROT_ROW98

Per Page Write Protection

Address: 0x0FFFF462

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.962 SFLASH_ALT_PROT_ROW99

Per Page Write Protection

Address: 0x0FFFF463

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.963 SFLASH_ALT_PROT_ROW100

Per Page Write Protection

Address: 0x0FFFF464

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.964 SFLASH_ALT_PROT_ROW101

Per Page Write Protection

Address: 0x0FFFF465

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.965 SFLASH_ALT_PROT_ROW102

Per Page Write Protection

Address: 0x0FFFF466

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.966 SFLASH_ALT_PROT_ROW103

Per Page Write Protection

Address: 0x0FFFF467

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.967 SFLASH_ALT_PROT_ROW104

Per Page Write Protection

Address: 0x0FFFF468

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.968 SFLASH_ALT_PROT_ROW105

Per Page Write Protection

Address: 0x0FFFF469

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.969 SFLASH_ALT_PROT_ROW106

Per Page Write Protection

Address: 0x0FFFF46A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.970 SFLASH_ALT_PROT_ROW107

Per Page Write Protection

Address: 0x0FFFF46B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.971 SFLASH_ALT_PROT_ROW108

Per Page Write Protection

Address: 0x0FFFF46C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.972 SFLASH_ALT_PROT_ROW109

Per Page Write Protection

Address: 0x0FFFF46D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.973 SFLASH_ALT_PROT_ROW110

Per Page Write Protection

Address: 0x0FFFF46E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.974 SFLASH_ALT_PROT_ROW111

Per Page Write Protection

Address: 0x0FFFF46F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.975 SFLASH_ALT_PROT_ROW112

Per Page Write Protection

Address: 0x0FFFF470

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.976 SFLASH_ALT_PROT_ROW113

Per Page Write Protection

Address: 0x0FFFF471

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.977 SFLASH_ALT_PROT_ROW114

Per Page Write Protection

Address: 0x0FFFF472

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.978 SFLASH_ALT_PROT_ROW115

Per Page Write Protection

Address: 0x0FFFF473

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.979 SFLASH_ALT_PROT_ROW116

Per Page Write Protection

Address: 0x0FFFF474

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.980 SFLASH_ALT_PROT_ROW117

Per Page Write Protection

Address: 0x0FFFF475

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.981 SFLASH_ALT_PROT_ROW118

Per Page Write Protection

Address: 0x0FFFF476

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.982 SFLASH_ALT_PROT_ROW119

Per Page Write Protection

Address: 0x0FFFF477

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.983 SFLASH_ALT_PROT_ROW120

Per Page Write Protection

Address: 0x0FFFF478

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.984 SFLASH_ALT_PROT_ROW121

Per Page Write Protection

Address: 0x0FFFF479

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.985 SFLASH_ALT_PROT_ROW122

Per Page Write Protection

Address: 0x0FFFF47A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.986 SFLASH_ALT_PROT_ROW123

Per Page Write Protection

Address: 0x0FFFF47B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.987 SFLASH_ALT_PROT_ROW124

Per Page Write Protection

Address: 0x0FFFF47C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.988 SFLASH_ALT_PROT_ROW125

Per Page Write Protection

Address: 0x0FFFF47D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.989 SFLASH_ALT_PROT_ROW126

Per Page Write Protection

Address: 0x0FFFF47E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.990 SFLASH_ALT_PROT_ROW127

Per Page Write Protection

Address: 0x0FFFF47F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.991 SFLASH_ALT_PROT_ROW128

Per Page Write Protection

Address: 0x0FFFF480

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.992 SFLASH_ALT_PROT_ROW129

Per Page Write Protection

Address: 0x0FFFF481

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.993 SFLASH_ALT_PROT_ROW130

Per Page Write Protection

Address: 0x0FFFF482

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.994 SFLASH_ALT_PROT_ROW131

Per Page Write Protection

Address: 0x0FFFF483

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.995 SFLASH_ALT_PROT_ROW132

Per Page Write Protection

Address: 0x0FFFF484

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.996 SFLASH_ALT_PROT_ROW133

Per Page Write Protection

Address: 0x0FFFF485

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.997 SFLASH_ALT_PROT_ROW134

Per Page Write Protection

Address: 0x0FFFF486

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.998 SFLASH_ALT_PROT_ROW135

Per Page Write Protection

Address: 0x0FFFF487

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.999 SFLASH_ALT_PROT_ROW136

Per Page Write Protection

Address: 0x0FFFF488

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1000SFLASH_ALT_PROT_ROW137

Per Page Write Protection

Address: 0x0FFFF489

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1001SFLASH_ALT_PROT_ROW138

Per Page Write Protection

Address: 0x0FFFF48A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1002SFLASH_ALT_PROT_ROW139

Per Page Write Protection

Address: 0x0FFFF48B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1003SFLASH_ALT_PROT_ROW140

Per Page Write Protection

Address: 0x0FFFF48C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1004SFLASH_ALT_PROT_ROW141

Per Page Write Protection

Address: 0x0FFFF48D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1005SFLASH_ALT_PROT_ROW142

Per Page Write Protection

Address: 0x0FFFF48E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1006SFLASH_ALT_PROT_ROW143

Per Page Write Protection

Address: 0x0FFFF48F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1007SFLASH_ALT_PROT_ROW144

Per Page Write Protection

Address: 0x0FFFF490

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1008SFLASH_ALT_PROT_ROW145

Per Page Write Protection

Address: 0x0FFFF491

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1009SFLASH_ALT_PROT_ROW146

Per Page Write Protection

Address: 0x0FFFF492

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1010SFLASH_ALT_PROT_ROW147

Per Page Write Protection

Address: 0x0FFFF493

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1011SFLASH_ALT_PROT_ROW148

Per Page Write Protection

Address: 0x0FFFF494

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1012SFLASH_ALT_PROT_ROW149

Per Page Write Protection

Address: 0x0FFFF495

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1013SFLASH_ALT_PROT_ROW150

Per Page Write Protection

Address: 0x0FFFF496

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1014SFLASH_ALT_PROT_ROW151

Per Page Write Protection

Address: 0x0FFFF497

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1015SFLASH_ALT_PROT_ROW152

Per Page Write Protection

Address: 0x0FFFF498

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1016SFLASH_ALT_PROT_ROW153

Per Page Write Protection

Address: 0x0FFFF499

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1017SFLASH_ALT_PROT_ROW154

Per Page Write Protection

Address: 0x0FFFF49A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1018SFLASH_ALT_PROT_ROW155

Per Page Write Protection

Address: 0x0FFFF49B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1019SFLASH_ALT_PROT_ROW156

Per Page Write Protection

Address: 0x0FFFF49C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1020SFLASH_ALT_PROT_ROW157

Per Page Write Protection

Address: 0x0FFFF49D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1021SFLASH_ALT_PROT_ROW158

Per Page Write Protection

Address: 0x0FFFF49E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1022SFLASH_ALT_PROT_ROW159

Per Page Write Protection

Address: 0x0FFFF49F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1023SFLASH_ALT_PROT_ROW160

Per Page Write Protection

Address: 0x0FFFF4A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1024SFLASH_ALT_PROT_ROW161

Per Page Write Protection

Address: 0x0FFFF4A1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1025SFLASH_ALT_PROT_ROW162

Per Page Write Protection

Address: 0x0FFFF4A2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1026SFLASH_ALT_PROT_ROW163

Per Page Write Protection

Address: 0x0FFFF4A3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1027SFLASH_ALT_PROT_ROW164

Per Page Write Protection

Address: 0x0FFFF4A4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1028SFLASH_ALT_PROT_ROW165

Per Page Write Protection

Address: 0x0FFFF4A5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1029SFLASH_ALT_PROT_ROW166

Per Page Write Protection

Address: 0x0FFFF4A6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1030SFLASH_ALT_PROT_ROW167

Per Page Write Protection

Address: 0x0FFFF4A7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1031SFLASH_ALT_PROT_ROW168

Per Page Write Protection

Address: 0x0FFFF4A8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1032SFLASH_ALT_PROT_ROW169

Per Page Write Protection

Address: 0x0FFFF4A9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1033SFLASH_ALT_PROT_ROW170

Per Page Write Protection

Address: 0x0FFFF4AA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1034SFLASH_ALT_PROT_ROW171

Per Page Write Protection

Address: 0x0FFFF4AB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1035SFLASH_ALT_PROT_ROW172

Per Page Write Protection

Address: 0x0FFFF4AC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1036SFLASH_ALT_PROT_ROW173

Per Page Write Protection

Address: 0x0FFFF4AD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1037SFLASH_ALT_PROT_ROW174

Per Page Write Protection

Address: 0x0FFFF4AE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1038SFLASH_ALT_PROT_ROW175

Per Page Write Protection

Address: 0x0FFFF4AF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1039SFLASH_ALT_PROT_ROW176

Per Page Write Protection

Address: 0x0FFFF4B0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1040SFLASH_ALT_PROT_ROW177

Per Page Write Protection

Address: 0x0FFFF4B1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1041SFLASH_ALT_PROT_ROW178

Per Page Write Protection

Address: 0x0FFFF4B2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1042SFLASH_ALT_PROT_ROW179

Per Page Write Protection

Address: 0x0FFFF4B3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1043SFLASH_ALT_PROT_ROW180

Per Page Write Protection

Address: 0x0FFFF4B4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1044SFLASH_ALT_PROT_ROW181

Per Page Write Protection

Address: 0x0FFFF4B5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1045SFLASH_ALT_PROT_ROW182

Per Page Write Protection

Address: 0x0FFFF4B6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1046SFLASH_ALT_PROT_ROW183

Per Page Write Protection

Address: 0x0FFFF4B7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1047SFLASH_ALT_PROT_ROW184

Per Page Write Protection

Address: 0x0FFFF4B8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1048SFLASH_ALT_PROT_ROW185

Per Page Write Protection

Address: 0x0FFFF4B9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1049SFLASH_ALT_PROT_ROW186

Per Page Write Protection

Address: 0x0FFFF4BA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1050SFLASH_ALT_PROT_ROW187

Per Page Write Protection

Address: 0x0FFFF4BB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1051SFLASH_ALT_PROT_ROW188

Per Page Write Protection

Address: 0x0FFFF4BC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1052SFLASH_ALT_PROT_ROW189

Per Page Write Protection

Address: 0x0FFFF4BD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1053SFLASH_ALT_PROT_ROW190

Per Page Write Protection

Address: 0x0FFFF4BE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1054SFLASH_ALT_PROT_ROW191

Per Page Write Protection

Address: 0x0FFFF4BF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1055SFLASH_ALT_PROT_ROW192

Per Page Write Protection

Address: 0x0FFFF4C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1056SFLASH_ALT_PROT_ROW193

Per Page Write Protection

Address: 0x0FFFF4C1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1057SFLASH_ALT_PROT_ROW194

Per Page Write Protection

Address: 0x0FFFF4C2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1058SFLASH_ALT_PROT_ROW195

Per Page Write Protection

Address: 0x0FFFF4C3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1059SFLASH_ALT_PROT_ROW196

Per Page Write Protection

Address: 0x0FFFF4C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1060SFLASH_ALT_PROT_ROW197

Per Page Write Protection

Address: 0x0FFFF4C5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1061SFLASH_ALT_PROT_ROW198

Per Page Write Protection

Address: 0x0FFFF4C6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1062SFLASH_ALT_PROT_ROW199

Per Page Write Protection

Address: 0x0FFFF4C7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1063SFLASH_ALT_PROT_ROW200

Per Page Write Protection

Address: 0x0FFFF4C8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1064SFLASH_ALT_PROT_ROW201

Per Page Write Protection

Address: 0x0FFFF4C9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1065SFLASH_ALT_PROT_ROW202

Per Page Write Protection

Address: 0x0FFFF4CA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1066SFLASH_ALT_PROT_ROW203

Per Page Write Protection

Address: 0x0FFFF4CB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1067SFLASH_ALT_PROT_ROW204

Per Page Write Protection

Address: 0x0FFFF4CC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1068SFLASH_ALT_PROT_ROW205

Per Page Write Protection

Address: 0x0FFFF4CD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1069SFLASH_ALT_PROT_ROW206

Per Page Write Protection

Address: 0x0FFFF4CE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1070SFLASH_ALT_PROT_ROW207

Per Page Write Protection

Address: 0x0FFFF4CF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1071SFLASH_ALT_PROT_ROW208

Per Page Write Protection

Address: 0x0FFFF4D0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1072SFLASH_ALT_PROT_ROW209

Per Page Write Protection

Address: 0x0FFFF4D1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1073SFLASH_ALT_PROT_ROW210

Per Page Write Protection

Address: 0x0FFFF4D2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1074SFLASH_ALT_PROT_ROW211

Per Page Write Protection

Address: 0x0FFFF4D3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1075SFLASH_ALT_PROT_ROW212

Per Page Write Protection

Address: 0x0FFFF4D4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1076SFLASH_ALT_PROT_ROW213

Per Page Write Protection

Address: 0x0FFFF4D5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1077SFLASH_ALT_PROT_ROW214

Per Page Write Protection

Address: 0x0FFFF4D6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1078SFLASH_ALT_PROT_ROW215

Per Page Write Protection

Address: 0x0FFFF4D7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1079SFLASH_ALT_PROT_ROW216

Per Page Write Protection

Address: 0x0FFFF4D8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1080SFLASH_ALT_PROT_ROW217

Per Page Write Protection

Address: 0x0FFFF4D9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1081SFLASH_ALT_PROT_ROW218

Per Page Write Protection

Address: 0x0FFFF4DA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1082SFLASH_ALT_PROT_ROW219

Per Page Write Protection

Address: 0x0FFFF4DB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1083SFLASH_ALT_PROT_ROW220

Per Page Write Protection

Address: 0x0FFFF4DC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1084SFLASH_ALT_PROT_ROW221

Per Page Write Protection

Address: 0x0FFFF4DD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1085SFLASH_ALT_PROT_ROW222

Per Page Write Protection

Address: 0x0FFFF4DE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1086SFLASH_ALT_PROT_ROW223

Per Page Write Protection

Address: 0x0FFFF4DF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1087SFLASH_ALT_PROT_ROW224

Per Page Write Protection

Address: 0x0FFFF4E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1088SFLASH_ALT_PROT_ROW225

Per Page Write Protection

Address: 0x0FFFF4E1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1089SFLASH_ALT_PROT_ROW226

Per Page Write Protection

Address: 0x0FFFF4E2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1090SFLASH_ALT_PROT_ROW227

Per Page Write Protection

Address: 0x0FFFF4E3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1091SFLASH_ALT_PROT_ROW228

Per Page Write Protection

Address: 0x0FFFF4E4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1092SFLASH_ALT_PROT_ROW229

Per Page Write Protection

Address: 0x0FFFF4E5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1093SFLASH_ALT_PROT_ROW230

Per Page Write Protection

Address: 0x0FFFF4E6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1094SFLASH_ALT_PROT_ROW231

Per Page Write Protection

Address: 0x0FFFF4E7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1095SFLASH_ALT_PROT_ROW232

Per Page Write Protection

Address: 0x0FFFF4E8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1096SFLASH_ALT_PROT_ROW233

Per Page Write Protection

Address: 0x0FFFF4E9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1097SFLASH_ALT_PROT_ROW234

Per Page Write Protection

Address: 0x0FFFF4EA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1098SFLASH_ALT_PROT_ROW235

Per Page Write Protection

Address: 0x0FFFF4EB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1099SFLASH_ALT_PROT_ROW236

Per Page Write Protection

Address: 0x0FFFF4EC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1100SFLASH_ALT_PROT_ROW237

Per Page Write Protection

Address: 0x0FFFF4ED

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1101SFLASH_ALT_PROT_ROW238

Per Page Write Protection

Address: 0x0FFFF4EE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1102SFLASH_ALT_PROT_ROW239

Per Page Write Protection

Address: 0x0FFFF4EF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1103SFLASH_ALT_PROT_ROW240

Per Page Write Protection

Address: 0x0FFFF4F0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1104SFLASH_ALT_PROT_ROW241

Per Page Write Protection

Address: 0x0FFFF4F1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1105SFLASH_ALT_PROT_ROW242

Per Page Write Protection

Address: 0x0FFFF4F2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1106SFLASH_ALT_PROT_ROW243

Per Page Write Protection

Address: 0x0FFFF4F3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1107SFLASH_ALT_PROT_ROW244

Per Page Write Protection

Address: 0x0FFFF4F4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1108SFLASH_ALT_PROT_ROW245

Per Page Write Protection

Address: 0x0FFFF4F5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1109SFLASH_ALT_PROT_ROW246

Per Page Write Protection

Address: 0x0FFFF4F6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1110SFLASH_ALT_PROT_ROW247

Per Page Write Protection

Address: 0x0FFFF4F7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1111 SFLASH_ALT_PROT_ROW248

Per Page Write Protection

Address: 0x0FFFF4F8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1112SFLASH_ALT_PROT_ROW249

Per Page Write Protection

Address: 0x0FFFF4F9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1113SFLASH_ALT_PROT_ROW250

Per Page Write Protection

Address: 0x0FFFF4FA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1114SFLASH_ALT_PROT_ROW251

Per Page Write Protection

Address: 0x0FFFF4FB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1115SFLASH_ALT_PROT_ROW252

Per Page Write Protection

Address: 0x0FFFF4FC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1116 SFLASH_ALT_PROT_ROW253

Per Page Write Protection

Address: 0x0FFFF4FD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1117SFLASH_ALT_PROT_ROW254

Per Page Write Protection

Address: 0x0FFFF4FE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1118SFLASH_ALT_PROT_ROW255

Per Page Write Protection

Address: 0x0FFFF4FF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

29.1.1119SFLASH_ALT_PP

Preprogram Settings

Address: 0x0FFFF5A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	PERIOD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	None				None			
Name	NDAC [31:28]				PDAC [27:24]			

Bits	Name	Description
31 : 28	NDAC	NDAC input. Each increment in NDAC causes an increase of ~0.10V in VNEG Default Value: X
27 : 24	PDAC	PDAC input. Each increment in PDAC causes an increase of ~0.10V in VPOS Default Value: X
23 : 0	PERIOD	Period of timer in clk_spcif_timer ticks. For regular FLASH, clock is 36MHz from dedicated oscillator. For FLASH-Lite, clock is same as clk_hf, which must be set to 48MHz for 48MHz devices and 12MHz for max 16MHz devices Default Value: X

29.1.1120SFLASH_ALT_E

Erase Settings

Address: 0x0FFFF5A4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	PERIOD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	None				None			
Name	NDAC [31:28]				PDAC [27:24]			

Bits	Name	Description
31 : 28	NDAC	NDAC input. Each increment in NDAC causes an increase of ~0.10V in VNEG Default Value: X
27 : 24	PDAC	PDAC input. Each increment in PDAC causes an increase of ~0.10V in VPOS Default Value: X
23 : 0	PERIOD	Period of timer in clk_spcif_timer ticks. For regular FLASH, clock is 36MHz from dedicated oscillator. For FLASH-Lite, clock is same as clk_hf, which must be set to 48MHz for 48MHz devices and 12MHz for max 16MHz devices Default Value: X

29.1.1121SFLASH_ALT_P

Program Settings

Address: 0x0FFFF5A8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	PERIOD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	None				None			
Name	NDAC [31:28]				PDAC [27:24]			

Bits	Name	Description
31 : 28	NDAC	NDAC input. Each increment in NDAC causes an increase of ~0.10V in VNEG Default Value: X
27 : 24	PDAC	PDAC input. Each increment in PDAC causes an increase of ~0.10V in VPOS Default Value: X
23 : 0	PERIOD	Period of timer in clk_spcif_timer ticks. For regular FLASH, clock is 36MHz from dedicated oscillator. For FLASH-Lite, clock is same as clk_hf, which must be set to 48MHz for 48MHz devices and 12MHz for max 16MHz devices Default Value: X

29.1.1122SFLASH_ALT_EA_E

Erase All - Erase Settings

Address: 0x0FFFF5AC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	PERIOD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	None				None			
Name	NDAC [31:28]				PDAC [27:24]			

Bits	Name	Description
31 : 28	NDAC	NDAC input. Each increment in NDAC causes an increase of ~0.10V in VNEG Default Value: X
27 : 24	PDAC	PDAC input. Each increment in PDAC causes an increase of ~0.10V in VPOS Default Value: X
23 : 0	PERIOD	Period of timer in clk_spcif_timer ticks. For regular FLASH, clock is 36MHz from dedicated oscillator. For FLASH-Lite, clock is same as clk_hf, which must be set to 48MHz for 48MHz devices and 12MHz for max 16MHz devices Default Value: X

29.1.1123SFLASH_ALT_EA_P

Erase All - Program Settings

Address: 0x0FFFF5B0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	PERIOD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	None				None			
Name	NDAC [31:28]				PDAC [27:24]			

Bits	Name	Description
31 : 28	NDAC	NDAC input. Each increment in NDAC causes an increase of ~0.10V in VNEG Default Value: X
27 : 24	PDAC	PDAC input. Each increment in PDAC causes an increase of ~0.10V in VPOS Default Value: X
23 : 0	PERIOD	Period of timer in clk_spcif_timer ticks. For regular FLASH, clock is 36MHz from dedicated oscillator. For FLASH-Lite, clock is same as clk_hf, which must be set to 48MHz for 48MHz devices and 12MHz for max 16MHz devices Default Value: X

29.1.1124SFLASH_ALT_ES_E

Erase Sector - Erase Settings

Address: 0x0FFFF5B4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	PERIOD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	None				None			
Name	NDAC [31:28]				PDAC [27:24]			

Bits	Name	Description
31 : 28	NDAC	NDAC input. Each increment in NDAC causes an increase of ~0.10V in VNEG Default Value: X
27 : 24	PDAC	PDAC input. Each increment in PDAC causes an increase of ~0.10V in VPOS Default Value: X
23 : 0	PERIOD	Period of timer in clk_spcif_timer ticks. For regular FLASH, clock is 36MHz from dedicated oscillator. For FLASH-Lite, clock is same as clk_hf, which must be set to 48MHz for 48MHz devices and 12MHz for max 16MHz devices Default Value: X

29.1.1125SFLASH_ALT_ES_P_EO

Erase Sector - Program EO Settings

Address: 0x0FFFF5B8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	PERIOD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	None				None			
Name	NDAC [31:28]				PDAC [27:24]			

Bits	Name	Description
31 : 28	NDAC	NDAC input. Each increment in NDAC causes an increase of ~0.10V in VNEG Default Value: X
27 : 24	PDAC	PDAC input. Each increment in PDAC causes an increase of ~0.10V in VPOS Default Value: X
23 : 0	PERIOD	Period of timer in clk_spcif_timer ticks. For regular FLASH, clock is 36MHz from dedicated oscillator. For FLASH-Lite, clock is same as clk_hf, which must be set to 48MHz for 48MHz devices and 12MHz for max 16MHz devices Default Value: X

29.1.1126SFLASH_ALT_E_VCTAT

Bandgap Trim Register

Address: 0x0FFFF5BC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	RW		RW			
HW Access	None	None	None		None			
Name	None	VCTAT_ENABLE	VCTAT_VOLTAGE [5:4]		VCTAT_SLOPE [3:0]			

Bits	Name	Description
6	VCTAT_ENABLE	Enable VCTAT block Default Value: X
5 : 4	VCTAT_VOLTAGE	Output voltage absolute trim Default Value: X
3 : 0	VCTAT_SLOPE	Output slope setting controls. The slope of the voltage with temperature varies from ~0% to ~15% from the value at 55C over the temperature range -40C to 150C based on control signal settings 0 to 15 Default Value: X

29.1.1127SFLASH_ALT_P_VCTAT

Bandgap Trim Register

Address: 0x0FFFF5BD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	RW		RW			
HW Access	None	None	None		None			
Name	None	VCTAT_ENABLE	VCTAT_VOLTAGE [5:4]		VCTAT_SLOPE [3:0]			

Bits	Name	Description
6	VCTAT_ENABLE	Enable VCTAT block Default Value: X
5 : 4	VCTAT_VOLTAGE	Output voltage absolute trim Default Value: X
3 : 0	VCTAT_SLOPE	Output slope setting controls. The slope of the voltage with temperature varies from ~0% to ~15% from the value at 55C over the temperature range -40C to 150C based on control signal settings 0 to 15 Default Value: X

30 Supervisory Flash (256 KB) Registers

This section discusses the Supervisory Flash (SFLASH) registers for 256 KB devices. It lists all the registers in mapping tables, in address order.

30.1 Register Details

Register Name	Address
SFLASH_PROT_ROW0	0x0FFFF000
SFLASH_PROT_ROW1	0x0FFFF001
SFLASH_PROT_ROW2	0x0FFFF002
SFLASH_PROT_ROW3	0x0FFFF003
SFLASH_PROT_ROW4	0x0FFFF004
SFLASH_PROT_ROW5	0x0FFFF005
SFLASH_PROT_ROW6	0x0FFFF006
SFLASH_PROT_ROW7	0x0FFFF007
SFLASH_PROT_ROW8	0x0FFFF008
SFLASH_PROT_ROW9	0x0FFFF009
SFLASH_PROT_ROW10	0x0FFFF00A
SFLASH_PROT_ROW11	0x0FFFF00B
SFLASH_PROT_ROW12	0x0FFFF00C
SFLASH_PROT_ROW13	0x0FFFF00D
SFLASH_PROT_ROW14	0x0FFFF00E
SFLASH_PROT_ROW15	0x0FFFF00F
SFLASH_PROT_ROW16	0x0FFFF010
SFLASH_PROT_ROW17	0x0FFFF011
SFLASH_PROT_ROW18	0x0FFFF012
SFLASH_PROT_ROW19	0x0FFFF013
SFLASH_PROT_ROW20	0x0FFFF014
SFLASH_PROT_ROW21	0x0FFFF015
SFLASH_PROT_ROW22	0x0FFFF016
SFLASH_PROT_ROW23	0x0FFFF017
SFLASH_PROT_ROW24	0x0FFFF018
SFLASH_PROT_ROW25	0x0FFFF019
SFLASH_PROT_ROW26	0x0FFFF01A

Register Name	Address
SFLASH_PROT_ROW27	0x0FFFF01B
SFLASH_PROT_ROW28	0x0FFFF01C
SFLASH_PROT_ROW29	0x0FFFF01D
SFLASH_PROT_ROW30	0x0FFFF01E
SFLASH_PROT_ROW31	0x0FFFF01F
SFLASH_PROT_ROW32	0x0FFFF020
SFLASH_PROT_ROW33	0x0FFFF021
SFLASH_PROT_ROW34	0x0FFFF022
SFLASH_PROT_ROW35	0x0FFFF023
SFLASH_PROT_ROW36	0x0FFFF024
SFLASH_PROT_ROW37	0x0FFFF025
SFLASH_PROT_ROW38	0x0FFFF026
SFLASH_PROT_ROW39	0x0FFFF027
SFLASH_PROT_ROW40	0x0FFFF028
SFLASH_PROT_ROW41	0x0FFFF029
SFLASH_PROT_ROW42	0x0FFFF02A
SFLASH_PROT_ROW43	0x0FFFF02B
SFLASH_PROT_ROW44	0x0FFFF02C
SFLASH_PROT_ROW45	0x0FFFF02D
SFLASH_PROT_ROW46	0x0FFFF02E
SFLASH_PROT_ROW47	0x0FFFF02F
SFLASH_PROT_ROW48	0x0FFFF030
SFLASH_PROT_ROW49	0x0FFFF031
SFLASH_PROT_ROW50	0x0FFFF032
SFLASH_PROT_ROW51	0x0FFFF033
SFLASH_PROT_ROW52	0x0FFFF034
SFLASH_PROT_ROW53	0x0FFFF035
SFLASH_PROT_ROW54	0x0FFFF036
SFLASH_PROT_ROW55	0x0FFFF037
SFLASH_PROT_ROW56	0x0FFFF038
SFLASH_PROT_ROW57	0x0FFFF039
SFLASH_PROT_ROW58	0x0FFFF03A
SFLASH_PROT_ROW59	0x0FFFF03B
SFLASH_PROT_ROW60	0x0FFFF03C
SFLASH_PROT_ROW61	0x0FFFF03D
SFLASH_PROT_ROW62	0x0FFFF03E
SFLASH_PROT_ROW63	0x0FFFF03F
SFLASH_PROT_PROTECTION	0x0FFFF0FF
SFLASH_AV_PAIRS_8B0	0x0FFFF100
SFLASH_AV_PAIRS_8B1	0x0FFFF101
SFLASH_AV_PAIRS_8B2	0x0FFFF102
SFLASH_AV_PAIRS_8B3	0x0FFFF103

Register Name	Address
SFLASH_AV_PAIRS_8B4	0x0FFFF104
SFLASH_AV_PAIRS_8B5	0x0FFFF105
SFLASH_AV_PAIRS_8B6	0x0FFFF106
SFLASH_AV_PAIRS_8B7	0x0FFFF107
SFLASH_AV_PAIRS_8B8	0x0FFFF108
SFLASH_AV_PAIRS_8B9	0x0FFFF109
SFLASH_AV_PAIRS_8B10	0x0FFFF10A
SFLASH_AV_PAIRS_8B11	0x0FFFF10B
SFLASH_AV_PAIRS_8B12	0x0FFFF10C
SFLASH_AV_PAIRS_8B13	0x0FFFF10D
SFLASH_AV_PAIRS_8B14	0x0FFFF10E
SFLASH_AV_PAIRS_8B15	0x0FFFF10F
SFLASH_AV_PAIRS_8B16	0x0FFFF110
SFLASH_AV_PAIRS_8B17	0x0FFFF111
SFLASH_AV_PAIRS_8B18	0x0FFFF112
SFLASH_AV_PAIRS_8B19	0x0FFFF113
SFLASH_AV_PAIRS_8B20	0x0FFFF114
SFLASH_AV_PAIRS_8B21	0x0FFFF115
SFLASH_AV_PAIRS_8B22	0x0FFFF116
SFLASH_AV_PAIRS_8B23	0x0FFFF117
SFLASH_AV_PAIRS_8B24	0x0FFFF118
SFLASH_AV_PAIRS_8B25	0x0FFFF119
SFLASH_AV_PAIRS_8B26	0x0FFFF11A
SFLASH_AV_PAIRS_8B27	0x0FFFF11B
SFLASH_AV_PAIRS_8B28	0x0FFFF11C
SFLASH_AV_PAIRS_8B29	0x0FFFF11D
SFLASH_AV_PAIRS_8B30	0x0FFFF11E
SFLASH_AV_PAIRS_8B31	0x0FFFF11F
SFLASH_AV_PAIRS_8B32	0x0FFFF120
SFLASH_AV_PAIRS_8B33	0x0FFFF121
SFLASH_AV_PAIRS_8B34	0x0FFFF122
SFLASH_AV_PAIRS_8B35	0x0FFFF123
SFLASH_AV_PAIRS_8B36	0x0FFFF124
SFLASH_AV_PAIRS_8B37	0x0FFFF125
SFLASH_AV_PAIRS_8B38	0x0FFFF126
SFLASH_AV_PAIRS_8B39	0x0FFFF127
SFLASH_AV_PAIRS_8B40	0x0FFFF128
SFLASH_AV_PAIRS_8B41	0x0FFFF129
SFLASH_AV_PAIRS_8B42	0x0FFFF12A
SFLASH_AV_PAIRS_8B43	0x0FFFF12B
SFLASH_AV_PAIRS_8B44	0x0FFFF12C
SFLASH_AV_PAIRS_8B45	0x0FFFF12D

Register Name	Address
SFLASH_AV_PAIRS_8B46	0x0FFFF12E
SFLASH_AV_PAIRS_8B47	0x0FFFF12F
SFLASH_AV_PAIRS_8B48	0x0FFFF130
SFLASH_AV_PAIRS_8B49	0x0FFFF131
SFLASH_AV_PAIRS_8B50	0x0FFFF132
SFLASH_AV_PAIRS_8B51	0x0FFFF133
SFLASH_AV_PAIRS_8B52	0x0FFFF134
SFLASH_AV_PAIRS_8B53	0x0FFFF135
SFLASH_AV_PAIRS_8B54	0x0FFFF136
SFLASH_AV_PAIRS_8B55	0x0FFFF137
SFLASH_AV_PAIRS_8B56	0x0FFFF138
SFLASH_AV_PAIRS_8B57	0x0FFFF139
SFLASH_AV_PAIRS_8B58	0x0FFFF13A
SFLASH_AV_PAIRS_8B59	0x0FFFF13B
SFLASH_AV_PAIRS_8B60	0x0FFFF13C
SFLASH_AV_PAIRS_8B61	0x0FFFF13D
SFLASH_AV_PAIRS_8B62	0x0FFFF13E
SFLASH_AV_PAIRS_8B63	0x0FFFF13F
SFLASH_AV_PAIRS_8B64	0x0FFFF140
SFLASH_AV_PAIRS_8B65	0x0FFFF141
SFLASH_AV_PAIRS_8B66	0x0FFFF142
SFLASH_AV_PAIRS_8B67	0x0FFFF143
SFLASH_AV_PAIRS_8B68	0x0FFFF144
SFLASH_AV_PAIRS_8B69	0x0FFFF145
SFLASH_AV_PAIRS_8B70	0x0FFFF146
SFLASH_AV_PAIRS_8B71	0x0FFFF147
SFLASH_AV_PAIRS_8B72	0x0FFFF148
SFLASH_AV_PAIRS_8B73	0x0FFFF149
SFLASH_AV_PAIRS_8B74	0x0FFFF14A
SFLASH_AV_PAIRS_8B75	0x0FFFF14B
SFLASH_AV_PAIRS_8B76	0x0FFFF14C
SFLASH_AV_PAIRS_8B77	0x0FFFF14D
SFLASH_AV_PAIRS_8B78	0x0FFFF14E
SFLASH_AV_PAIRS_8B79	0x0FFFF14F
SFLASH_AV_PAIRS_8B80	0x0FFFF150
SFLASH_AV_PAIRS_8B81	0x0FFFF151
SFLASH_AV_PAIRS_8B82	0x0FFFF152
SFLASH_AV_PAIRS_8B83	0x0FFFF153
SFLASH_AV_PAIRS_8B84	0x0FFFF154
SFLASH_AV_PAIRS_8B85	0x0FFFF155
SFLASH_AV_PAIRS_8B86	0x0FFFF156
SFLASH_AV_PAIRS_8B87	0x0FFFF157

Register Name	Address
SFLASH_BLESS_BB_BUMP2	0x0FFFF158
SFLASH_AV_PAIRS_8B88	0x0FFFF158
SFLASH_AV_PAIRS_8B89	0x0FFFF159
SFLASH_BLESS_BB_XO	0x0FFFF15A
SFLASH_AV_PAIRS_8B90	0x0FFFF15A
SFLASH_AV_PAIRS_8B91	0x0FFFF15B
SFLASH_BLESS_SY_BUMP1	0x0FFFF15C
SFLASH_AV_PAIRS_8B92	0x0FFFF15C
SFLASH_AV_PAIRS_8B93	0x0FFFF15D
SFLASH_BLESS_LDO	0x0FFFF15E
SFLASH_AV_PAIRS_8B94	0x0FFFF15E
SFLASH_AV_PAIRS_8B95	0x0FFFF15F
SFLASH_AV_PAIRS_8B96	0x0FFFF160
SFLASH_AV_PAIRS_8B97	0x0FFFF161
SFLASH_AV_PAIRS_8B98	0x0FFFF162
SFLASH_AV_PAIRS_8B99	0x0FFFF163
SFLASH_AV_PAIRS_8B100	0x0FFFF164
SFLASH_AV_PAIRS_8B101	0x0FFFF165
SFLASH_AV_PAIRS_8B102	0x0FFFF166
SFLASH_AV_PAIRS_8B103	0x0FFFF167
SFLASH_AV_PAIRS_8B104	0x0FFFF168
SFLASH_AV_PAIRS_8B105	0x0FFFF169
SFLASH_AV_PAIRS_8B106	0x0FFFF16A
SFLASH_AV_PAIRS_8B107	0x0FFFF16B
SFLASH_AV_PAIRS_8B108	0x0FFFF16C
SFLASH_AV_PAIRS_8B109	0x0FFFF16D
SFLASH_AV_PAIRS_8B110	0x0FFFF16E
SFLASH_AV_PAIRS_8B111	0x0FFFF16F
SFLASH_AV_PAIRS_8B112	0x0FFFF170
SFLASH_AV_PAIRS_8B113	0x0FFFF171
SFLASH_AV_PAIRS_8B114	0x0FFFF172
SFLASH_AV_PAIRS_8B115	0x0FFFF173
SFLASH_AV_PAIRS_8B116	0x0FFFF174
SFLASH_AV_PAIRS_8B117	0x0FFFF175
SFLASH_AV_PAIRS_8B118	0x0FFFF176
SFLASH_AV_PAIRS_8B119	0x0FFFF177
SFLASH_AV_PAIRS_8B120	0x0FFFF178
SFLASH_AV_PAIRS_8B121	0x0FFFF179
SFLASH_AV_PAIRS_8B122	0x0FFFF17A
SFLASH_AV_PAIRS_8B123	0x0FFFF17B
SFLASH_AV_PAIRS_8B124	0x0FFFF17C
SFLASH_AV_PAIRS_8B125	0x0FFFF17D

Register Name	Address
SFLASH_AV_PAIRS_8B126	0x0FFFF17E
SFLASH_AV_PAIRS_8B127	0x0FFFF17F
SFLASH_AV_PAIRS_32B0	0x0FFFF200
SFLASH_AV_PAIRS_32B1	0x0FFFF204
SFLASH_AV_PAIRS_32B2	0x0FFFF208
SFLASH_AV_PAIRS_32B3	0x0FFFF20C
SFLASH_AV_PAIRS_32B4	0x0FFFF210
SFLASH_AV_PAIRS_32B5	0x0FFFF214
SFLASH_AV_PAIRS_32B6	0x0FFFF218
SFLASH_AV_PAIRS_32B7	0x0FFFF21C
SFLASH_AV_PAIRS_32B8	0x0FFFF220
SFLASH_AV_PAIRS_32B9	0x0FFFF224
SFLASH_AV_PAIRS_32B10	0x0FFFF228
SFLASH_AV_PAIRS_32B11	0x0FFFF22C
SFLASH_AV_PAIRS_32B12	0x0FFFF230
SFLASH_AV_PAIRS_32B13	0x0FFFF234
SFLASH_AV_PAIRS_32B14	0x0FFFF238
SFLASH_AV_PAIRS_32B15	0x0FFFF23C
SFLASH_CPUSS_WOUNDING	0x0FFFF240
SFLASH_SILICON_ID	0x0FFFF244
SFLASH_CPUSS_PRIV_RAM	0x0FFFF248
SFLASH_CPUSS_PRIV_ROM_BROM	0x0FFFF24A
SFLASH_CPUSS_PRIV_FLASH	0x0FFFF24C
SFLASH_CPUSS_PRIV_ROM_SROM	0x0FFFF24E
SFLASH_HIB_KEY_DELAY	0x0FFFF250
SFLASH_DPSLP_KEY_DELAY	0x0FFFF252
SFLASH_SWD_CONFIG	0x0FFFF254
SFLASH_INITIAL_SPCIF_TRIM_M1_DAC0	0x0FFFF255
SFLASH_SWD_LISTEN	0x0FFFF258
SFLASH_FLASH_START	0x0FFFF25C
SFLASH_CSD_TRIM1_HVIDAC	0x0FFFF260
SFLASH_CSD_TRIM2_HVIDAC	0x0FFFF261
SFLASH_CSD_TRIM1_CSD	0x0FFFF262
SFLASH_CSD_TRIM2_CSD	0x0FFFF263
SFLASH_SAR_TEMP_MULTIPLIER	0x0FFFF264
SFLASH_SAR_TEMP_OFFSET	0x0FFFF266
SFLASH_SKIP_CHECKSUM	0x0FFFF269
SFLASH_PROT_VIRGINKEY0	0x0FFFF270
SFLASH_PROT_VIRGINKEY1	0x0FFFF271
SFLASH_PROT_VIRGINKEY2	0x0FFFF272
SFLASH_PROT_VIRGINKEY3	0x0FFFF273
SFLASH_PROT_VIRGINKEY4	0x0FFFF274

Register Name	Address
SFLASH_PROT_VIRGINKEY5	0x0FFFF275
SFLASH_PROT_VIRGINKEY6	0x0FFFF276
SFLASH_PROT_VIRGINKEY7	0x0FFFF277
SFLASH_DIE_LOT0	0x0FFFF278
SFLASH_DIE_LOT1	0x0FFFF279
SFLASH_DIE_LOT2	0x0FFFF27A
SFLASH_DIE_WAFER	0x0FFFF27B
SFLASH_DIE_X	0x0FFFF27C
SFLASH_DIE_Y	0x0FFFF27D
SFLASH_DIE_SORT	0x0FFFF27E
SFLASH_DIE_MINOR	0x0FFFF27F
SFLASH_PE_TE_DATA0	0x0FFFF300
SFLASH_PE_TE_DATA1	0x0FFFF301
SFLASH_PE_TE_DATA2	0x0FFFF302
SFLASH_PE_TE_DATA3	0x0FFFF303
SFLASH_PE_TE_DATA4	0x0FFFF304
SFLASH_PE_TE_DATA5	0x0FFFF305
SFLASH_PE_TE_DATA6	0x0FFFF306
SFLASH_PE_TE_DATA7	0x0FFFF307
SFLASH_PE_TE_DATA8	0x0FFFF308
SFLASH_PE_TE_DATA9	0x0FFFF309
SFLASH_PE_TE_DATA10	0x0FFFF30A
SFLASH_PE_TE_DATA11	0x0FFFF30B
SFLASH_PE_TE_DATA12	0x0FFFF30C
SFLASH_PE_TE_DATA13	0x0FFFF30D
SFLASH_PE_TE_DATA14	0x0FFFF30E
SFLASH_PE_TE_DATA15	0x0FFFF30F
SFLASH_PE_TE_DATA16	0x0FFFF310
SFLASH_PE_TE_DATA17	0x0FFFF311
SFLASH_PE_TE_DATA18	0x0FFFF312
SFLASH_PE_TE_DATA19	0x0FFFF313
SFLASH_PE_TE_DATA20	0x0FFFF314
SFLASH_PE_TE_DATA21	0x0FFFF315
SFLASH_PE_TE_DATA22	0x0FFFF316
SFLASH_PE_TE_DATA23	0x0FFFF317
SFLASH_PE_TE_DATA24	0x0FFFF318
SFLASH_PE_TE_DATA25	0x0FFFF319
SFLASH_PE_TE_DATA26	0x0FFFF31A
SFLASH_PE_TE_DATA27	0x0FFFF31B
SFLASH_PE_TE_DATA28	0x0FFFF31C
SFLASH_PE_TE_DATA29	0x0FFFF31D
SFLASH_PE_TE_DATA30	0x0FFFF31E

Register Name	Address
SFLASH_PE_TE_DATA31	0x0FFFF31F
SFLASH_PP	0x0FFFF320
SFLASH_E	0x0FFFF324
SFLASH_P	0x0FFFF328
SFLASH_EA_E	0x0FFFF32C
SFLASH_EA_P	0x0FFFF330
SFLASH_ES_E	0x0FFFF334
SFLASH_ES_P_EO	0x0FFFF338
SFLASH_E_VCTAT	0x0FFFF33C
SFLASH_P_VCTAT	0x0FFFF33D
SFLASH_IMO_MAXF0	0x0FFFF340
SFLASH_IMO_ABS0	0x0FFFF341
SFLASH_IMO_TMPCO0	0x0FFFF342
SFLASH_IMO_MAXF1	0x0FFFF343
SFLASH_IMO_ABS1	0x0FFFF344
SFLASH_IMO_TMPCO1	0x0FFFF345
SFLASH_IMO_MAXF2	0x0FFFF346
SFLASH_IMO_ABS2	0x0FFFF347
SFLASH_IMO_TMPCO2	0x0FFFF348
SFLASH_IMO_MAXF3	0x0FFFF349
SFLASH_IMO_ABS3	0x0FFFF34A
SFLASH_IMO_TMPCO3	0x0FFFF34B
SFLASH_IMO_ABS4	0x0FFFF34C
SFLASH_IMO_TMPCO4	0x0FFFF34D
SFLASH_IMO_TRIM0	0x0FFFF350
SFLASH_IMO_TRIM1	0x0FFFF351
SFLASH_IMO_TRIM2	0x0FFFF352
SFLASH_IMO_TRIM3	0x0FFFF353
SFLASH_IMO_TRIM4	0x0FFFF354
SFLASH_IMO_TRIM5	0x0FFFF355
SFLASH_IMO_TRIM6	0x0FFFF356
SFLASH_IMO_TRIM7	0x0FFFF357
SFLASH_IMO_TRIM8	0x0FFFF358
SFLASH_IMO_TRIM9	0x0FFFF359
SFLASH_IMO_TRIM10	0x0FFFF35A
SFLASH_IMO_TRIM11	0x0FFFF35B
SFLASH_IMO_TRIM12	0x0FFFF35C
SFLASH_IMO_TRIM13	0x0FFFF35D
SFLASH_IMO_TRIM14	0x0FFFF35E
SFLASH_IMO_TRIM15	0x0FFFF35F
SFLASH_IMO_TRIM16	0x0FFFF360
SFLASH_IMO_TRIM17	0x0FFFF361

Register Name	Address
SFLASH_IMO_TRIM18	0x0FFFF362
SFLASH_IMO_TRIM19	0x0FFFF363
SFLASH_IMO_TRIM20	0x0FFFF364
SFLASH_IMO_TRIM21	0x0FFFF365
SFLASH_IMO_TRIM22	0x0FFFF366
SFLASH_IMO_TRIM23	0x0FFFF367
SFLASH_IMO_TRIM24	0x0FFFF368
SFLASH_IMO_TRIM25	0x0FFFF369
SFLASH_IMO_TRIM26	0x0FFFF36A
SFLASH_IMO_TRIM27	0x0FFFF36B
SFLASH_IMO_TRIM28	0x0FFFF36C
SFLASH_IMO_TRIM29	0x0FFFF36D
SFLASH_IMO_TRIM30	0x0FFFF36E
SFLASH_IMO_TRIM31	0x0FFFF36F
SFLASH_IMO_TRIM32	0x0FFFF370
SFLASH_IMO_TRIM33	0x0FFFF371
SFLASH_IMO_TRIM34	0x0FFFF372
SFLASH_IMO_TRIM35	0x0FFFF373
SFLASH_IMO_TRIM36	0x0FFFF374
SFLASH_IMO_TRIM37	0x0FFFF375
SFLASH_IMO_TRIM38	0x0FFFF376
SFLASH_IMO_TRIM39	0x0FFFF377
SFLASH_IMO_TRIM40	0x0FFFF378
SFLASH_IMO_TRIM41	0x0FFFF379
SFLASH_IMO_TRIM42	0x0FFFF37A
SFLASH_IMO_TRIM43	0x0FFFF37B
SFLASH_IMO_TRIM44	0x0FFFF37C
SFLASH_IMO_TRIM45	0x0FFFF37D
SFLASH_CHECKSUM	0x0FFFF3FE
SFLASH_MACRO_0_FREE_SFLASH0	0x0FFFF400
SFLASH_MACRO_0_FREE_SFLASH1	0x0FFFF401
SFLASH_MACRO_0_FREE_SFLASH2	0x0FFFF402
SFLASH_MACRO_0_FREE_SFLASH3	0x0FFFF403
SFLASH_MACRO_0_FREE_SFLASH4	0x0FFFF404
SFLASH_MACRO_0_FREE_SFLASH5	0x0FFFF405
SFLASH_MACRO_0_FREE_SFLASH6	0x0FFFF406
SFLASH_MACRO_0_FREE_SFLASH7	0x0FFFF407
SFLASH_MACRO_0_FREE_SFLASH8	0x0FFFF408
SFLASH_MACRO_0_FREE_SFLASH9	0x0FFFF409
SFLASH_MACRO_0_FREE_SFLASH10	0x0FFFF40A
SFLASH_MACRO_0_FREE_SFLASH11	0x0FFFF40B
SFLASH_MACRO_0_FREE_SFLASH12	0x0FFFF40C

Register Name	Address
SFLASH_MACRO_0_FREE_SFLASH13	0x0FFFF40D
SFLASH_MACRO_0_FREE_SFLASH14	0x0FFFF40E
SFLASH_MACRO_0_FREE_SFLASH15	0x0FFFF40F
SFLASH_MACRO_0_FREE_SFLASH16	0x0FFFF410
SFLASH_MACRO_0_FREE_SFLASH17	0x0FFFF411
SFLASH_MACRO_0_FREE_SFLASH18	0x0FFFF412
SFLASH_MACRO_0_FREE_SFLASH19	0x0FFFF413
SFLASH_MACRO_0_FREE_SFLASH20	0x0FFFF414
SFLASH_MACRO_0_FREE_SFLASH21	0x0FFFF415
SFLASH_MACRO_0_FREE_SFLASH22	0x0FFFF416
SFLASH_MACRO_0_FREE_SFLASH23	0x0FFFF417
SFLASH_MACRO_0_FREE_SFLASH24	0x0FFFF418
SFLASH_MACRO_0_FREE_SFLASH25	0x0FFFF419
SFLASH_MACRO_0_FREE_SFLASH26	0x0FFFF41A
SFLASH_MACRO_0_FREE_SFLASH27	0x0FFFF41B
SFLASH_MACRO_0_FREE_SFLASH28	0x0FFFF41C
SFLASH_MACRO_0_FREE_SFLASH29	0x0FFFF41D
SFLASH_MACRO_0_FREE_SFLASH30	0x0FFFF41E
SFLASH_MACRO_0_FREE_SFLASH31	0x0FFFF41F
SFLASH_MACRO_0_FREE_SFLASH32	0x0FFFF420
SFLASH_MACRO_0_FREE_SFLASH33	0x0FFFF421
SFLASH_MACRO_0_FREE_SFLASH34	0x0FFFF422
SFLASH_MACRO_0_FREE_SFLASH35	0x0FFFF423
SFLASH_MACRO_0_FREE_SFLASH36	0x0FFFF424
SFLASH_MACRO_0_FREE_SFLASH37	0x0FFFF425
SFLASH_MACRO_0_FREE_SFLASH38	0x0FFFF426
SFLASH_MACRO_0_FREE_SFLASH39	0x0FFFF427
SFLASH_MACRO_0_FREE_SFLASH40	0x0FFFF428
SFLASH_MACRO_0_FREE_SFLASH41	0x0FFFF429
SFLASH_MACRO_0_FREE_SFLASH42	0x0FFFF42A
SFLASH_MACRO_0_FREE_SFLASH43	0x0FFFF42B
SFLASH_MACRO_0_FREE_SFLASH44	0x0FFFF42C
SFLASH_MACRO_0_FREE_SFLASH45	0x0FFFF42D
SFLASH_MACRO_0_FREE_SFLASH46	0x0FFFF42E
SFLASH_MACRO_0_FREE_SFLASH47	0x0FFFF42F
SFLASH_MACRO_0_FREE_SFLASH48	0x0FFFF430
SFLASH_MACRO_0_FREE_SFLASH49	0x0FFFF431
SFLASH_MACRO_0_FREE_SFLASH50	0x0FFFF432
SFLASH_MACRO_0_FREE_SFLASH51	0x0FFFF433
SFLASH_MACRO_0_FREE_SFLASH52	0x0FFFF434
SFLASH_MACRO_0_FREE_SFLASH53	0x0FFFF435
SFLASH_MACRO_0_FREE_SFLASH54	0x0FFFF436

Register Name	Address
SFLASH_MACRO_0_FREE_SFLASH55	0x0FFFF437
SFLASH_MACRO_0_FREE_SFLASH56	0x0FFFF438
SFLASH_MACRO_0_FREE_SFLASH57	0x0FFFF439
SFLASH_MACRO_0_FREE_SFLASH58	0x0FFFF43A
SFLASH_MACRO_0_FREE_SFLASH59	0x0FFFF43B
SFLASH_MACRO_0_FREE_SFLASH60	0x0FFFF43C
SFLASH_MACRO_0_FREE_SFLASH61	0x0FFFF43D
SFLASH_MACRO_0_FREE_SFLASH62	0x0FFFF43E
SFLASH_MACRO_0_FREE_SFLASH63	0x0FFFF43F
SFLASH_MACRO_0_FREE_SFLASH64	0x0FFFF440
SFLASH_MACRO_0_FREE_SFLASH65	0x0FFFF441
SFLASH_MACRO_0_FREE_SFLASH66	0x0FFFF442
SFLASH_MACRO_0_FREE_SFLASH67	0x0FFFF443
SFLASH_MACRO_0_FREE_SFLASH68	0x0FFFF444
SFLASH_MACRO_0_FREE_SFLASH69	0x0FFFF445
SFLASH_MACRO_0_FREE_SFLASH70	0x0FFFF446
SFLASH_MACRO_0_FREE_SFLASH71	0x0FFFF447
SFLASH_MACRO_0_FREE_SFLASH72	0x0FFFF448
SFLASH_MACRO_0_FREE_SFLASH73	0x0FFFF449
SFLASH_MACRO_0_FREE_SFLASH74	0x0FFFF44A
SFLASH_MACRO_0_FREE_SFLASH75	0x0FFFF44B
SFLASH_MACRO_0_FREE_SFLASH76	0x0FFFF44C
SFLASH_MACRO_0_FREE_SFLASH77	0x0FFFF44D
SFLASH_MACRO_0_FREE_SFLASH78	0x0FFFF44E
SFLASH_MACRO_0_FREE_SFLASH79	0x0FFFF44F
SFLASH_MACRO_0_FREE_SFLASH80	0x0FFFF450
SFLASH_MACRO_0_FREE_SFLASH81	0x0FFFF451
SFLASH_MACRO_0_FREE_SFLASH82	0x0FFFF452
SFLASH_MACRO_0_FREE_SFLASH83	0x0FFFF453
SFLASH_MACRO_0_FREE_SFLASH84	0x0FFFF454
SFLASH_MACRO_0_FREE_SFLASH85	0x0FFFF455
SFLASH_MACRO_0_FREE_SFLASH86	0x0FFFF456
SFLASH_MACRO_0_FREE_SFLASH87	0x0FFFF457
SFLASH_MACRO_0_FREE_SFLASH88	0x0FFFF458
SFLASH_MACRO_0_FREE_SFLASH89	0x0FFFF459
SFLASH_MACRO_0_FREE_SFLASH90	0x0FFFF45A
SFLASH_MACRO_0_FREE_SFLASH91	0x0FFFF45B
SFLASH_MACRO_0_FREE_SFLASH92	0x0FFFF45C
SFLASH_MACRO_0_FREE_SFLASH93	0x0FFFF45D
SFLASH_MACRO_0_FREE_SFLASH94	0x0FFFF45E
SFLASH_MACRO_0_FREE_SFLASH95	0x0FFFF45F
SFLASH_MACRO_0_FREE_SFLASH96	0x0FFFF460

Register Name	Address
SFLASH_MACRO_0_FREE_SFLASH97	0x0FFFF461
SFLASH_MACRO_0_FREE_SFLASH98	0x0FFFF462
SFLASH_MACRO_0_FREE_SFLASH99	0x0FFFF463
SFLASH_MACRO_0_FREE_SFLASH100	0x0FFFF464
SFLASH_MACRO_0_FREE_SFLASH101	0x0FFFF465
SFLASH_MACRO_0_FREE_SFLASH102	0x0FFFF466
SFLASH_MACRO_0_FREE_SFLASH103	0x0FFFF467
SFLASH_MACRO_0_FREE_SFLASH104	0x0FFFF468
SFLASH_MACRO_0_FREE_SFLASH105	0x0FFFF469
SFLASH_MACRO_0_FREE_SFLASH106	0x0FFFF46A
SFLASH_MACRO_0_FREE_SFLASH107	0x0FFFF46B
SFLASH_MACRO_0_FREE_SFLASH108	0x0FFFF46C
SFLASH_MACRO_0_FREE_SFLASH109	0x0FFFF46D
SFLASH_MACRO_0_FREE_SFLASH110	0x0FFFF46E
SFLASH_MACRO_0_FREE_SFLASH111	0x0FFFF46F
SFLASH_MACRO_0_FREE_SFLASH112	0x0FFFF470
SFLASH_MACRO_0_FREE_SFLASH113	0x0FFFF471
SFLASH_MACRO_0_FREE_SFLASH114	0x0FFFF472
SFLASH_MACRO_0_FREE_SFLASH115	0x0FFFF473
SFLASH_MACRO_0_FREE_SFLASH116	0x0FFFF474
SFLASH_MACRO_0_FREE_SFLASH117	0x0FFFF475
SFLASH_MACRO_0_FREE_SFLASH118	0x0FFFF476
SFLASH_MACRO_0_FREE_SFLASH119	0x0FFFF477
SFLASH_MACRO_0_FREE_SFLASH120	0x0FFFF478
SFLASH_MACRO_0_FREE_SFLASH121	0x0FFFF479
SFLASH_MACRO_0_FREE_SFLASH122	0x0FFFF47A
SFLASH_MACRO_0_FREE_SFLASH123	0x0FFFF47B
SFLASH_MACRO_0_FREE_SFLASH124	0x0FFFF47C
SFLASH_MACRO_0_FREE_SFLASH125	0x0FFFF47D
SFLASH_MACRO_0_FREE_SFLASH126	0x0FFFF47E
SFLASH_MACRO_0_FREE_SFLASH127	0x0FFFF47F
SFLASH_MACRO_0_FREE_SFLASH128	0x0FFFF480
SFLASH_MACRO_0_FREE_SFLASH129	0x0FFFF481
SFLASH_MACRO_0_FREE_SFLASH130	0x0FFFF482
SFLASH_MACRO_0_FREE_SFLASH131	0x0FFFF483
SFLASH_MACRO_0_FREE_SFLASH132	0x0FFFF484
SFLASH_MACRO_0_FREE_SFLASH133	0x0FFFF485
SFLASH_MACRO_0_FREE_SFLASH134	0x0FFFF486
SFLASH_MACRO_0_FREE_SFLASH135	0x0FFFF487
SFLASH_MACRO_0_FREE_SFLASH136	0x0FFFF488
SFLASH_MACRO_0_FREE_SFLASH137	0x0FFFF489
SFLASH_MACRO_0_FREE_SFLASH138	0x0FFFF48A

Register Name	Address
SFLASH_MACRO_0_FREE_SFLASH139	0x0FFFF48B
SFLASH_MACRO_0_FREE_SFLASH140	0x0FFFF48C
SFLASH_MACRO_0_FREE_SFLASH141	0x0FFFF48D
SFLASH_MACRO_0_FREE_SFLASH142	0x0FFFF48E
SFLASH_MACRO_0_FREE_SFLASH143	0x0FFFF48F
SFLASH_MACRO_0_FREE_SFLASH144	0x0FFFF490
SFLASH_MACRO_0_FREE_SFLASH145	0x0FFFF491
SFLASH_MACRO_0_FREE_SFLASH146	0x0FFFF492
SFLASH_MACRO_0_FREE_SFLASH147	0x0FFFF493
SFLASH_MACRO_0_FREE_SFLASH148	0x0FFFF494
SFLASH_MACRO_0_FREE_SFLASH149	0x0FFFF495
SFLASH_MACRO_0_FREE_SFLASH150	0x0FFFF496
SFLASH_MACRO_0_FREE_SFLASH151	0x0FFFF497
SFLASH_MACRO_0_FREE_SFLASH152	0x0FFFF498
SFLASH_MACRO_0_FREE_SFLASH153	0x0FFFF499
SFLASH_MACRO_0_FREE_SFLASH154	0x0FFFF49A
SFLASH_MACRO_0_FREE_SFLASH155	0x0FFFF49B
SFLASH_MACRO_0_FREE_SFLASH156	0x0FFFF49C
SFLASH_MACRO_0_FREE_SFLASH157	0x0FFFF49D
SFLASH_MACRO_0_FREE_SFLASH158	0x0FFFF49E
SFLASH_MACRO_0_FREE_SFLASH159	0x0FFFF49F
SFLASH_MACRO_0_FREE_SFLASH160	0x0FFFF4A0
SFLASH_MACRO_0_FREE_SFLASH161	0x0FFFF4A1
SFLASH_MACRO_0_FREE_SFLASH162	0x0FFFF4A2
SFLASH_MACRO_0_FREE_SFLASH163	0x0FFFF4A3
SFLASH_MACRO_0_FREE_SFLASH164	0x0FFFF4A4
SFLASH_MACRO_0_FREE_SFLASH165	0x0FFFF4A5
SFLASH_MACRO_0_FREE_SFLASH166	0x0FFFF4A6
SFLASH_MACRO_0_FREE_SFLASH167	0x0FFFF4A7
SFLASH_MACRO_0_FREE_SFLASH168	0x0FFFF4A8
SFLASH_MACRO_0_FREE_SFLASH169	0x0FFFF4A9
SFLASH_MACRO_0_FREE_SFLASH170	0x0FFFF4AA
SFLASH_MACRO_0_FREE_SFLASH171	0x0FFFF4AB
SFLASH_MACRO_0_FREE_SFLASH172	0x0FFFF4AC
SFLASH_MACRO_0_FREE_SFLASH173	0x0FFFF4AD
SFLASH_MACRO_0_FREE_SFLASH174	0x0FFFF4AE
SFLASH_MACRO_0_FREE_SFLASH175	0x0FFFF4AF
SFLASH_MACRO_0_FREE_SFLASH176	0x0FFFF4B0
SFLASH_MACRO_0_FREE_SFLASH177	0x0FFFF4B1
SFLASH_MACRO_0_FREE_SFLASH178	0x0FFFF4B2
SFLASH_MACRO_0_FREE_SFLASH179	0x0FFFF4B3
SFLASH_MACRO_0_FREE_SFLASH180	0x0FFFF4B4

Register Name	Address
SFLASH_MACRO_0_FREE_SFLASH181	0x0FFFF4B5
SFLASH_MACRO_0_FREE_SFLASH182	0x0FFFF4B6
SFLASH_MACRO_0_FREE_SFLASH183	0x0FFFF4B7
SFLASH_MACRO_0_FREE_SFLASH184	0x0FFFF4B8
SFLASH_MACRO_0_FREE_SFLASH185	0x0FFFF4B9
SFLASH_MACRO_0_FREE_SFLASH186	0x0FFFF4BA
SFLASH_MACRO_0_FREE_SFLASH187	0x0FFFF4BB
SFLASH_MACRO_0_FREE_SFLASH188	0x0FFFF4BC
SFLASH_MACRO_0_FREE_SFLASH189	0x0FFFF4BD
SFLASH_MACRO_0_FREE_SFLASH190	0x0FFFF4BE
SFLASH_MACRO_0_FREE_SFLASH191	0x0FFFF4BF
SFLASH_MACRO_0_FREE_SFLASH192	0x0FFFF4C0
SFLASH_MACRO_0_FREE_SFLASH193	0x0FFFF4C1
SFLASH_MACRO_0_FREE_SFLASH194	0x0FFFF4C2
SFLASH_MACRO_0_FREE_SFLASH195	0x0FFFF4C3
SFLASH_MACRO_0_FREE_SFLASH196	0x0FFFF4C4
SFLASH_MACRO_0_FREE_SFLASH197	0x0FFFF4C5
SFLASH_MACRO_0_FREE_SFLASH198	0x0FFFF4C6
SFLASH_MACRO_0_FREE_SFLASH199	0x0FFFF4C7
SFLASH_MACRO_0_FREE_SFLASH200	0x0FFFF4C8
SFLASH_MACRO_0_FREE_SFLASH201	0x0FFFF4C9
SFLASH_MACRO_0_FREE_SFLASH202	0x0FFFF4CA
SFLASH_MACRO_0_FREE_SFLASH203	0x0FFFF4CB
SFLASH_MACRO_0_FREE_SFLASH204	0x0FFFF4CC
SFLASH_MACRO_0_FREE_SFLASH205	0x0FFFF4CD
SFLASH_MACRO_0_FREE_SFLASH206	0x0FFFF4CE
SFLASH_MACRO_0_FREE_SFLASH207	0x0FFFF4CF
SFLASH_MACRO_0_FREE_SFLASH208	0x0FFFF4D0
SFLASH_MACRO_0_FREE_SFLASH209	0x0FFFF4D1
SFLASH_MACRO_0_FREE_SFLASH210	0x0FFFF4D2
SFLASH_MACRO_0_FREE_SFLASH211	0x0FFFF4D3
SFLASH_MACRO_0_FREE_SFLASH212	0x0FFFF4D4
SFLASH_MACRO_0_FREE_SFLASH213	0x0FFFF4D5
SFLASH_MACRO_0_FREE_SFLASH214	0x0FFFF4D6
SFLASH_MACRO_0_FREE_SFLASH215	0x0FFFF4D7
SFLASH_MACRO_0_FREE_SFLASH216	0x0FFFF4D8
SFLASH_MACRO_0_FREE_SFLASH217	0x0FFFF4D9
SFLASH_MACRO_0_FREE_SFLASH218	0x0FFFF4DA
SFLASH_MACRO_0_FREE_SFLASH219	0x0FFFF4DB
SFLASH_MACRO_0_FREE_SFLASH220	0x0FFFF4DC
SFLASH_MACRO_0_FREE_SFLASH221	0x0FFFF4DD
SFLASH_MACRO_0_FREE_SFLASH222	0x0FFFF4DE

Register Name	Address
SFLASH_MACRO_0_FREE_SFLASH223	0x0FFFF4DF
SFLASH_MACRO_0_FREE_SFLASH224	0x0FFFF4E0
SFLASH_MACRO_0_FREE_SFLASH225	0x0FFFF4E1
SFLASH_MACRO_0_FREE_SFLASH226	0x0FFFF4E2
SFLASH_MACRO_0_FREE_SFLASH227	0x0FFFF4E3
SFLASH_MACRO_0_FREE_SFLASH228	0x0FFFF4E4
SFLASH_MACRO_0_FREE_SFLASH229	0x0FFFF4E5
SFLASH_MACRO_0_FREE_SFLASH230	0x0FFFF4E6
SFLASH_MACRO_0_FREE_SFLASH231	0x0FFFF4E7
SFLASH_MACRO_0_FREE_SFLASH232	0x0FFFF4E8
SFLASH_MACRO_0_FREE_SFLASH233	0x0FFFF4E9
SFLASH_MACRO_0_FREE_SFLASH234	0x0FFFF4EA
SFLASH_MACRO_0_FREE_SFLASH235	0x0FFFF4EB
SFLASH_MACRO_0_FREE_SFLASH236	0x0FFFF4EC
SFLASH_MACRO_0_FREE_SFLASH237	0x0FFFF4ED
SFLASH_MACRO_0_FREE_SFLASH238	0x0FFFF4EE
SFLASH_MACRO_0_FREE_SFLASH239	0x0FFFF4EF
SFLASH_MACRO_0_FREE_SFLASH240	0x0FFFF4F0
SFLASH_MACRO_0_FREE_SFLASH241	0x0FFFF4F1
SFLASH_MACRO_0_FREE_SFLASH242	0x0FFFF4F2
SFLASH_MACRO_0_FREE_SFLASH243	0x0FFFF4F3
SFLASH_MACRO_0_FREE_SFLASH244	0x0FFFF4F4
SFLASH_MACRO_0_FREE_SFLASH245	0x0FFFF4F5
SFLASH_MACRO_0_FREE_SFLASH246	0x0FFFF4F6
SFLASH_MACRO_0_FREE_SFLASH247	0x0FFFF4F7
SFLASH_MACRO_0_FREE_SFLASH248	0x0FFFF4F8
SFLASH_MACRO_0_FREE_SFLASH249	0x0FFFF4F9
SFLASH_MACRO_0_FREE_SFLASH250	0x0FFFF4FA
SFLASH_MACRO_0_FREE_SFLASH251	0x0FFFF4FB
SFLASH_MACRO_0_FREE_SFLASH252	0x0FFFF4FC
SFLASH_MACRO_0_FREE_SFLASH253	0x0FFFF4FD
SFLASH_MACRO_0_FREE_SFLASH254	0x0FFFF4FE
SFLASH_MACRO_0_FREE_SFLASH255	0x0FFFF4FF
SFLASH_MACRO_0_FREE_SFLASH256	0x0FFFF500
SFLASH_MACRO_0_FREE_SFLASH257	0x0FFFF501
SFLASH_MACRO_0_FREE_SFLASH258	0x0FFFF502
SFLASH_MACRO_0_FREE_SFLASH259	0x0FFFF503
SFLASH_MACRO_0_FREE_SFLASH260	0x0FFFF504
SFLASH_MACRO_0_FREE_SFLASH261	0x0FFFF505
SFLASH_MACRO_0_FREE_SFLASH262	0x0FFFF506
SFLASH_MACRO_0_FREE_SFLASH263	0x0FFFF507
SFLASH_MACRO_0_FREE_SFLASH264	0x0FFFF508

Register Name	Address
SFLASH_MACRO_0_FREE_SFLASH265	0x0FFFF509
SFLASH_MACRO_0_FREE_SFLASH266	0x0FFFF50A
SFLASH_MACRO_0_FREE_SFLASH267	0x0FFFF50B
SFLASH_MACRO_0_FREE_SFLASH268	0x0FFFF50C
SFLASH_MACRO_0_FREE_SFLASH269	0x0FFFF50D
SFLASH_MACRO_0_FREE_SFLASH270	0x0FFFF50E
SFLASH_MACRO_0_FREE_SFLASH271	0x0FFFF50F
SFLASH_MACRO_0_FREE_SFLASH272	0x0FFFF510
SFLASH_MACRO_0_FREE_SFLASH273	0x0FFFF511
SFLASH_MACRO_0_FREE_SFLASH274	0x0FFFF512
SFLASH_MACRO_0_FREE_SFLASH275	0x0FFFF513
SFLASH_MACRO_0_FREE_SFLASH276	0x0FFFF514
SFLASH_MACRO_0_FREE_SFLASH277	0x0FFFF515
SFLASH_MACRO_0_FREE_SFLASH278	0x0FFFF516
SFLASH_MACRO_0_FREE_SFLASH279	0x0FFFF517
SFLASH_MACRO_0_FREE_SFLASH280	0x0FFFF518
SFLASH_MACRO_0_FREE_SFLASH281	0x0FFFF519
SFLASH_MACRO_0_FREE_SFLASH282	0x0FFFF51A
SFLASH_MACRO_0_FREE_SFLASH283	0x0FFFF51B
SFLASH_MACRO_0_FREE_SFLASH284	0x0FFFF51C
SFLASH_MACRO_0_FREE_SFLASH285	0x0FFFF51D
SFLASH_MACRO_0_FREE_SFLASH286	0x0FFFF51E
SFLASH_MACRO_0_FREE_SFLASH287	0x0FFFF51F
SFLASH_MACRO_0_FREE_SFLASH288	0x0FFFF520
SFLASH_MACRO_0_FREE_SFLASH289	0x0FFFF521
SFLASH_MACRO_0_FREE_SFLASH290	0x0FFFF522
SFLASH_MACRO_0_FREE_SFLASH291	0x0FFFF523
SFLASH_MACRO_0_FREE_SFLASH292	0x0FFFF524
SFLASH_MACRO_0_FREE_SFLASH293	0x0FFFF525
SFLASH_MACRO_0_FREE_SFLASH294	0x0FFFF526
SFLASH_MACRO_0_FREE_SFLASH295	0x0FFFF527
SFLASH_MACRO_0_FREE_SFLASH296	0x0FFFF528
SFLASH_MACRO_0_FREE_SFLASH297	0x0FFFF529
SFLASH_MACRO_0_FREE_SFLASH298	0x0FFFF52A
SFLASH_MACRO_0_FREE_SFLASH299	0x0FFFF52B
SFLASH_MACRO_0_FREE_SFLASH300	0x0FFFF52C
SFLASH_MACRO_0_FREE_SFLASH301	0x0FFFF52D
SFLASH_MACRO_0_FREE_SFLASH302	0x0FFFF52E
SFLASH_MACRO_0_FREE_SFLASH303	0x0FFFF52F
SFLASH_MACRO_0_FREE_SFLASH304	0x0FFFF530
SFLASH_MACRO_0_FREE_SFLASH305	0x0FFFF531
SFLASH_MACRO_0_FREE_SFLASH306	0x0FFFF532

Register Name	Address
SFLASH_MACRO_0_FREE_SFLASH307	0x0FFFF533
SFLASH_MACRO_0_FREE_SFLASH308	0x0FFFF534
SFLASH_MACRO_0_FREE_SFLASH309	0x0FFFF535
SFLASH_MACRO_0_FREE_SFLASH310	0x0FFFF536
SFLASH_MACRO_0_FREE_SFLASH311	0x0FFFF537
SFLASH_MACRO_0_FREE_SFLASH312	0x0FFFF538
SFLASH_MACRO_0_FREE_SFLASH313	0x0FFFF539
SFLASH_MACRO_0_FREE_SFLASH314	0x0FFFF53A
SFLASH_MACRO_0_FREE_SFLASH315	0x0FFFF53B
SFLASH_MACRO_0_FREE_SFLASH316	0x0FFFF53C
SFLASH_MACRO_0_FREE_SFLASH317	0x0FFFF53D
SFLASH_MACRO_0_FREE_SFLASH318	0x0FFFF53E
SFLASH_MACRO_0_FREE_SFLASH319	0x0FFFF53F
SFLASH_MACRO_0_FREE_SFLASH320	0x0FFFF540
SFLASH_MACRO_0_FREE_SFLASH321	0x0FFFF541
SFLASH_MACRO_0_FREE_SFLASH322	0x0FFFF542
SFLASH_MACRO_0_FREE_SFLASH323	0x0FFFF543
SFLASH_MACRO_0_FREE_SFLASH324	0x0FFFF544
SFLASH_MACRO_0_FREE_SFLASH325	0x0FFFF545
SFLASH_MACRO_0_FREE_SFLASH326	0x0FFFF546
SFLASH_MACRO_0_FREE_SFLASH327	0x0FFFF547
SFLASH_MACRO_0_FREE_SFLASH328	0x0FFFF548
SFLASH_MACRO_0_FREE_SFLASH329	0x0FFFF549
SFLASH_MACRO_0_FREE_SFLASH330	0x0FFFF54A
SFLASH_MACRO_0_FREE_SFLASH331	0x0FFFF54B
SFLASH_MACRO_0_FREE_SFLASH332	0x0FFFF54C
SFLASH_MACRO_0_FREE_SFLASH333	0x0FFFF54D
SFLASH_MACRO_0_FREE_SFLASH334	0x0FFFF54E
SFLASH_MACRO_0_FREE_SFLASH335	0x0FFFF54F
SFLASH_MACRO_0_FREE_SFLASH336	0x0FFFF550
SFLASH_MACRO_0_FREE_SFLASH337	0x0FFFF551
SFLASH_MACRO_0_FREE_SFLASH338	0x0FFFF552
SFLASH_MACRO_0_FREE_SFLASH339	0x0FFFF553
SFLASH_MACRO_0_FREE_SFLASH340	0x0FFFF554
SFLASH_MACRO_0_FREE_SFLASH341	0x0FFFF555
SFLASH_MACRO_0_FREE_SFLASH342	0x0FFFF556
SFLASH_MACRO_0_FREE_SFLASH343	0x0FFFF557
SFLASH_MACRO_0_FREE_SFLASH344	0x0FFFF558
SFLASH_MACRO_0_FREE_SFLASH345	0x0FFFF559
SFLASH_MACRO_0_FREE_SFLASH346	0x0FFFF55A
SFLASH_MACRO_0_FREE_SFLASH347	0x0FFFF55B
SFLASH_MACRO_0_FREE_SFLASH348	0x0FFFF55C

Register Name	Address
SFLASH_MACRO_0_FREE_SFLASH349	0x0FFFF55D
SFLASH_MACRO_0_FREE_SFLASH350	0x0FFFF55E
SFLASH_MACRO_0_FREE_SFLASH351	0x0FFFF55F
SFLASH_MACRO_0_FREE_SFLASH352	0x0FFFF560
SFLASH_MACRO_0_FREE_SFLASH353	0x0FFFF561
SFLASH_MACRO_0_FREE_SFLASH354	0x0FFFF562
SFLASH_MACRO_0_FREE_SFLASH355	0x0FFFF563
SFLASH_MACRO_0_FREE_SFLASH356	0x0FFFF564
SFLASH_MACRO_0_FREE_SFLASH357	0x0FFFF565
SFLASH_MACRO_0_FREE_SFLASH358	0x0FFFF566
SFLASH_MACRO_0_FREE_SFLASH359	0x0FFFF567
SFLASH_MACRO_0_FREE_SFLASH360	0x0FFFF568
SFLASH_MACRO_0_FREE_SFLASH361	0x0FFFF569
SFLASH_MACRO_0_FREE_SFLASH362	0x0FFFF56A
SFLASH_MACRO_0_FREE_SFLASH363	0x0FFFF56B
SFLASH_MACRO_0_FREE_SFLASH364	0x0FFFF56C
SFLASH_MACRO_0_FREE_SFLASH365	0x0FFFF56D
SFLASH_MACRO_0_FREE_SFLASH366	0x0FFFF56E
SFLASH_MACRO_0_FREE_SFLASH367	0x0FFFF56F
SFLASH_MACRO_0_FREE_SFLASH368	0x0FFFF570
SFLASH_MACRO_0_FREE_SFLASH369	0x0FFFF571
SFLASH_MACRO_0_FREE_SFLASH370	0x0FFFF572
SFLASH_MACRO_0_FREE_SFLASH371	0x0FFFF573
SFLASH_MACRO_0_FREE_SFLASH372	0x0FFFF574
SFLASH_MACRO_0_FREE_SFLASH373	0x0FFFF575
SFLASH_MACRO_0_FREE_SFLASH374	0x0FFFF576
SFLASH_MACRO_0_FREE_SFLASH375	0x0FFFF577
SFLASH_MACRO_0_FREE_SFLASH376	0x0FFFF578
SFLASH_MACRO_0_FREE_SFLASH377	0x0FFFF579
SFLASH_MACRO_0_FREE_SFLASH378	0x0FFFF57A
SFLASH_MACRO_0_FREE_SFLASH379	0x0FFFF57B
SFLASH_MACRO_0_FREE_SFLASH380	0x0FFFF57C
SFLASH_MACRO_0_FREE_SFLASH381	0x0FFFF57D
SFLASH_MACRO_0_FREE_SFLASH382	0x0FFFF57E
SFLASH_MACRO_0_FREE_SFLASH383	0x0FFFF57F
SFLASH_MACRO_0_FREE_SFLASH384	0x0FFFF580
SFLASH_MACRO_0_FREE_SFLASH385	0x0FFFF581
SFLASH_MACRO_0_FREE_SFLASH386	0x0FFFF582
SFLASH_MACRO_0_FREE_SFLASH387	0x0FFFF583
SFLASH_MACRO_0_FREE_SFLASH388	0x0FFFF584
SFLASH_MACRO_0_FREE_SFLASH389	0x0FFFF585
SFLASH_MACRO_0_FREE_SFLASH390	0x0FFFF586

Register Name	Address
SFLASH_MACRO_0_FREE_SFLASH391	0x0FFFF587
SFLASH_MACRO_0_FREE_SFLASH392	0x0FFFF588
SFLASH_MACRO_0_FREE_SFLASH393	0x0FFFF589
SFLASH_MACRO_0_FREE_SFLASH394	0x0FFFF58A
SFLASH_MACRO_0_FREE_SFLASH395	0x0FFFF58B
SFLASH_MACRO_0_FREE_SFLASH396	0x0FFFF58C
SFLASH_MACRO_0_FREE_SFLASH397	0x0FFFF58D
SFLASH_MACRO_0_FREE_SFLASH398	0x0FFFF58E
SFLASH_MACRO_0_FREE_SFLASH399	0x0FFFF58F
SFLASH_MACRO_0_FREE_SFLASH400	0x0FFFF590
SFLASH_MACRO_0_FREE_SFLASH401	0x0FFFF591
SFLASH_MACRO_0_FREE_SFLASH402	0x0FFFF592
SFLASH_MACRO_0_FREE_SFLASH403	0x0FFFF593
SFLASH_MACRO_0_FREE_SFLASH404	0x0FFFF594
SFLASH_MACRO_0_FREE_SFLASH405	0x0FFFF595
SFLASH_MACRO_0_FREE_SFLASH406	0x0FFFF596
SFLASH_MACRO_0_FREE_SFLASH407	0x0FFFF597
SFLASH_MACRO_0_FREE_SFLASH408	0x0FFFF598
SFLASH_MACRO_0_FREE_SFLASH409	0x0FFFF599
SFLASH_MACRO_0_FREE_SFLASH410	0x0FFFF59A
SFLASH_MACRO_0_FREE_SFLASH411	0x0FFFF59B
SFLASH_MACRO_0_FREE_SFLASH412	0x0FFFF59C
SFLASH_MACRO_0_FREE_SFLASH413	0x0FFFF59D
SFLASH_MACRO_0_FREE_SFLASH414	0x0FFFF59E
SFLASH_MACRO_0_FREE_SFLASH415	0x0FFFF59F
SFLASH_MACRO_0_FREE_SFLASH416	0x0FFFF5A0
SFLASH_MACRO_0_FREE_SFLASH417	0x0FFFF5A1
SFLASH_MACRO_0_FREE_SFLASH418	0x0FFFF5A2
SFLASH_MACRO_0_FREE_SFLASH419	0x0FFFF5A3
SFLASH_MACRO_0_FREE_SFLASH420	0x0FFFF5A4
SFLASH_MACRO_0_FREE_SFLASH421	0x0FFFF5A5
SFLASH_MACRO_0_FREE_SFLASH422	0x0FFFF5A6
SFLASH_MACRO_0_FREE_SFLASH423	0x0FFFF5A7
SFLASH_MACRO_0_FREE_SFLASH424	0x0FFFF5A8
SFLASH_MACRO_0_FREE_SFLASH425	0x0FFFF5A9
SFLASH_MACRO_0_FREE_SFLASH426	0x0FFFF5AA
SFLASH_MACRO_0_FREE_SFLASH427	0x0FFFF5AB
SFLASH_MACRO_0_FREE_SFLASH428	0x0FFFF5AC
SFLASH_MACRO_0_FREE_SFLASH429	0x0FFFF5AD
SFLASH_MACRO_0_FREE_SFLASH430	0x0FFFF5AE
SFLASH_MACRO_0_FREE_SFLASH431	0x0FFFF5AF
SFLASH_MACRO_0_FREE_SFLASH432	0x0FFFF5B0

Register Name	Address
SFLASH_MACRO_0_FREE_SFLASH433	0x0FFFF5B1
SFLASH_MACRO_0_FREE_SFLASH434	0x0FFFF5B2
SFLASH_MACRO_0_FREE_SFLASH435	0x0FFFF5B3
SFLASH_MACRO_0_FREE_SFLASH436	0x0FFFF5B4
SFLASH_MACRO_0_FREE_SFLASH437	0x0FFFF5B5
SFLASH_MACRO_0_FREE_SFLASH438	0x0FFFF5B6
SFLASH_MACRO_0_FREE_SFLASH439	0x0FFFF5B7
SFLASH_MACRO_0_FREE_SFLASH440	0x0FFFF5B8
SFLASH_MACRO_0_FREE_SFLASH441	0x0FFFF5B9
SFLASH_MACRO_0_FREE_SFLASH442	0x0FFFF5BA
SFLASH_MACRO_0_FREE_SFLASH443	0x0FFFF5BB
SFLASH_MACRO_0_FREE_SFLASH444	0x0FFFF5BC
SFLASH_MACRO_0_FREE_SFLASH445	0x0FFFF5BD
SFLASH_MACRO_0_FREE_SFLASH446	0x0FFFF5BE
SFLASH_MACRO_0_FREE_SFLASH447	0x0FFFF5BF
SFLASH_MACRO_0_FREE_SFLASH448	0x0FFFF5C0
SFLASH_MACRO_0_FREE_SFLASH449	0x0FFFF5C1
SFLASH_MACRO_0_FREE_SFLASH450	0x0FFFF5C2
SFLASH_MACRO_0_FREE_SFLASH451	0x0FFFF5C3
SFLASH_MACRO_0_FREE_SFLASH452	0x0FFFF5C4
SFLASH_MACRO_0_FREE_SFLASH453	0x0FFFF5C5
SFLASH_MACRO_0_FREE_SFLASH454	0x0FFFF5C6
SFLASH_MACRO_0_FREE_SFLASH455	0x0FFFF5C7
SFLASH_MACRO_0_FREE_SFLASH456	0x0FFFF5C8
SFLASH_MACRO_0_FREE_SFLASH457	0x0FFFF5C9
SFLASH_MACRO_0_FREE_SFLASH458	0x0FFFF5CA
SFLASH_MACRO_0_FREE_SFLASH459	0x0FFFF5CB
SFLASH_MACRO_0_FREE_SFLASH460	0x0FFFF5CC
SFLASH_MACRO_0_FREE_SFLASH461	0x0FFFF5CD
SFLASH_MACRO_0_FREE_SFLASH462	0x0FFFF5CE
SFLASH_MACRO_0_FREE_SFLASH463	0x0FFFF5CF
SFLASH_MACRO_0_FREE_SFLASH464	0x0FFFF5D0
SFLASH_MACRO_0_FREE_SFLASH465	0x0FFFF5D1
SFLASH_MACRO_0_FREE_SFLASH466	0x0FFFF5D2
SFLASH_MACRO_0_FREE_SFLASH467	0x0FFFF5D3
SFLASH_MACRO_0_FREE_SFLASH468	0x0FFFF5D4
SFLASH_MACRO_0_FREE_SFLASH469	0x0FFFF5D5
SFLASH_MACRO_0_FREE_SFLASH470	0x0FFFF5D6
SFLASH_MACRO_0_FREE_SFLASH471	0x0FFFF5D7
SFLASH_MACRO_0_FREE_SFLASH472	0x0FFFF5D8
SFLASH_MACRO_0_FREE_SFLASH473	0x0FFFF5D9
SFLASH_MACRO_0_FREE_SFLASH474	0x0FFFF5DA

Register Name	Address
SFLASH_MACRO_0_FREE_SFLASH475	0x0FFFF5DB
SFLASH_MACRO_0_FREE_SFLASH476	0x0FFFF5DC
SFLASH_MACRO_0_FREE_SFLASH477	0x0FFFF5DD
SFLASH_MACRO_0_FREE_SFLASH478	0x0FFFF5DE
SFLASH_MACRO_0_FREE_SFLASH479	0x0FFFF5DF
SFLASH_MACRO_0_FREE_SFLASH480	0x0FFFF5E0
SFLASH_MACRO_0_FREE_SFLASH481	0x0FFFF5E1
SFLASH_MACRO_0_FREE_SFLASH482	0x0FFFF5E2
SFLASH_MACRO_0_FREE_SFLASH483	0x0FFFF5E3
SFLASH_MACRO_0_FREE_SFLASH484	0x0FFFF5E4
SFLASH_MACRO_0_FREE_SFLASH485	0x0FFFF5E5
SFLASH_MACRO_0_FREE_SFLASH486	0x0FFFF5E6
SFLASH_MACRO_0_FREE_SFLASH487	0x0FFFF5E7
SFLASH_MACRO_0_FREE_SFLASH488	0x0FFFF5E8
SFLASH_MACRO_0_FREE_SFLASH489	0x0FFFF5E9
SFLASH_MACRO_0_FREE_SFLASH490	0x0FFFF5EA
SFLASH_MACRO_0_FREE_SFLASH491	0x0FFFF5EB
SFLASH_MACRO_0_FREE_SFLASH492	0x0FFFF5EC
SFLASH_MACRO_0_FREE_SFLASH493	0x0FFFF5ED
SFLASH_MACRO_0_FREE_SFLASH494	0x0FFFF5EE
SFLASH_MACRO_0_FREE_SFLASH495	0x0FFFF5EF
SFLASH_MACRO_0_FREE_SFLASH496	0x0FFFF5F0
SFLASH_MACRO_0_FREE_SFLASH497	0x0FFFF5F1
SFLASH_MACRO_0_FREE_SFLASH498	0x0FFFF5F2
SFLASH_MACRO_0_FREE_SFLASH499	0x0FFFF5F3
SFLASH_MACRO_0_FREE_SFLASH500	0x0FFFF5F4
SFLASH_MACRO_0_FREE_SFLASH501	0x0FFFF5F5
SFLASH_MACRO_0_FREE_SFLASH502	0x0FFFF5F6
SFLASH_MACRO_0_FREE_SFLASH503	0x0FFFF5F7
SFLASH_MACRO_0_FREE_SFLASH504	0x0FFFF5F8
SFLASH_MACRO_0_FREE_SFLASH505	0x0FFFF5F9
SFLASH_MACRO_0_FREE_SFLASH506	0x0FFFF5FA
SFLASH_MACRO_0_FREE_SFLASH507	0x0FFFF5FB
SFLASH_MACRO_0_FREE_SFLASH508	0x0FFFF5FC
SFLASH_MACRO_0_FREE_SFLASH509	0x0FFFF5FD
SFLASH_MACRO_0_FREE_SFLASH510	0x0FFFF5FE
SFLASH_MACRO_0_FREE_SFLASH511	0x0FFFF5FF
SFLASH_MACRO_0_FREE_SFLASH512	0x0FFFF600
SFLASH_MACRO_0_FREE_SFLASH513	0x0FFFF601
SFLASH_MACRO_0_FREE_SFLASH514	0x0FFFF602
SFLASH_MACRO_0_FREE_SFLASH515	0x0FFFF603
SFLASH_MACRO_0_FREE_SFLASH516	0x0FFFF604

Register Name	Address
SFLASH_MACRO_0_FREE_SFLASH517	0x0FFFF605
SFLASH_MACRO_0_FREE_SFLASH518	0x0FFFF606
SFLASH_MACRO_0_FREE_SFLASH519	0x0FFFF607
SFLASH_MACRO_0_FREE_SFLASH520	0x0FFFF608
SFLASH_MACRO_0_FREE_SFLASH521	0x0FFFF609
SFLASH_MACRO_0_FREE_SFLASH522	0x0FFFF60A
SFLASH_MACRO_0_FREE_SFLASH523	0x0FFFF60B
SFLASH_MACRO_0_FREE_SFLASH524	0x0FFFF60C
SFLASH_MACRO_0_FREE_SFLASH525	0x0FFFF60D
SFLASH_MACRO_0_FREE_SFLASH526	0x0FFFF60E
SFLASH_MACRO_0_FREE_SFLASH527	0x0FFFF60F
SFLASH_MACRO_0_FREE_SFLASH528	0x0FFFF610
SFLASH_MACRO_0_FREE_SFLASH529	0x0FFFF611
SFLASH_MACRO_0_FREE_SFLASH530	0x0FFFF612
SFLASH_MACRO_0_FREE_SFLASH531	0x0FFFF613
SFLASH_MACRO_0_FREE_SFLASH532	0x0FFFF614
SFLASH_MACRO_0_FREE_SFLASH533	0x0FFFF615
SFLASH_MACRO_0_FREE_SFLASH534	0x0FFFF616
SFLASH_MACRO_0_FREE_SFLASH535	0x0FFFF617
SFLASH_MACRO_0_FREE_SFLASH536	0x0FFFF618
SFLASH_MACRO_0_FREE_SFLASH537	0x0FFFF619
SFLASH_MACRO_0_FREE_SFLASH538	0x0FFFF61A
SFLASH_MACRO_0_FREE_SFLASH539	0x0FFFF61B
SFLASH_MACRO_0_FREE_SFLASH540	0x0FFFF61C
SFLASH_MACRO_0_FREE_SFLASH541	0x0FFFF61D
SFLASH_MACRO_0_FREE_SFLASH542	0x0FFFF61E
SFLASH_MACRO_0_FREE_SFLASH543	0x0FFFF61F
SFLASH_MACRO_0_FREE_SFLASH544	0x0FFFF620
SFLASH_MACRO_0_FREE_SFLASH545	0x0FFFF621
SFLASH_MACRO_0_FREE_SFLASH546	0x0FFFF622
SFLASH_MACRO_0_FREE_SFLASH547	0x0FFFF623
SFLASH_MACRO_0_FREE_SFLASH548	0x0FFFF624
SFLASH_MACRO_0_FREE_SFLASH549	0x0FFFF625
SFLASH_MACRO_0_FREE_SFLASH550	0x0FFFF626
SFLASH_MACRO_0_FREE_SFLASH551	0x0FFFF627
SFLASH_MACRO_0_FREE_SFLASH552	0x0FFFF628
SFLASH_MACRO_0_FREE_SFLASH553	0x0FFFF629
SFLASH_MACRO_0_FREE_SFLASH554	0x0FFFF62A
SFLASH_MACRO_0_FREE_SFLASH555	0x0FFFF62B
SFLASH_MACRO_0_FREE_SFLASH556	0x0FFFF62C
SFLASH_MACRO_0_FREE_SFLASH557	0x0FFFF62D
SFLASH_MACRO_0_FREE_SFLASH558	0x0FFFF62E

Register Name	Address
SFLASH_MACRO_0_FREE_SFLASH559	0x0FFFF62F
SFLASH_MACRO_0_FREE_SFLASH560	0x0FFFF630
SFLASH_MACRO_0_FREE_SFLASH561	0x0FFFF631
SFLASH_MACRO_0_FREE_SFLASH562	0x0FFFF632
SFLASH_MACRO_0_FREE_SFLASH563	0x0FFFF633
SFLASH_MACRO_0_FREE_SFLASH564	0x0FFFF634
SFLASH_MACRO_0_FREE_SFLASH565	0x0FFFF635
SFLASH_MACRO_0_FREE_SFLASH566	0x0FFFF636
SFLASH_MACRO_0_FREE_SFLASH567	0x0FFFF637
SFLASH_MACRO_0_FREE_SFLASH568	0x0FFFF638
SFLASH_MACRO_0_FREE_SFLASH569	0x0FFFF639
SFLASH_MACRO_0_FREE_SFLASH570	0x0FFFF63A
SFLASH_MACRO_0_FREE_SFLASH571	0x0FFFF63B
SFLASH_MACRO_0_FREE_SFLASH572	0x0FFFF63C
SFLASH_MACRO_0_FREE_SFLASH573	0x0FFFF63D
SFLASH_MACRO_0_FREE_SFLASH574	0x0FFFF63E
SFLASH_MACRO_0_FREE_SFLASH575	0x0FFFF63F
SFLASH_MACRO_0_FREE_SFLASH576	0x0FFFF640
SFLASH_MACRO_0_FREE_SFLASH577	0x0FFFF641
SFLASH_MACRO_0_FREE_SFLASH578	0x0FFFF642
SFLASH_MACRO_0_FREE_SFLASH579	0x0FFFF643
SFLASH_MACRO_0_FREE_SFLASH580	0x0FFFF644
SFLASH_MACRO_0_FREE_SFLASH581	0x0FFFF645
SFLASH_MACRO_0_FREE_SFLASH582	0x0FFFF646
SFLASH_MACRO_0_FREE_SFLASH583	0x0FFFF647
SFLASH_MACRO_0_FREE_SFLASH584	0x0FFFF648
SFLASH_MACRO_0_FREE_SFLASH585	0x0FFFF649
SFLASH_MACRO_0_FREE_SFLASH586	0x0FFFF64A
SFLASH_MACRO_0_FREE_SFLASH587	0x0FFFF64B
SFLASH_MACRO_0_FREE_SFLASH588	0x0FFFF64C
SFLASH_MACRO_0_FREE_SFLASH589	0x0FFFF64D
SFLASH_MACRO_0_FREE_SFLASH590	0x0FFFF64E
SFLASH_MACRO_0_FREE_SFLASH591	0x0FFFF64F
SFLASH_MACRO_0_FREE_SFLASH592	0x0FFFF650
SFLASH_MACRO_0_FREE_SFLASH593	0x0FFFF651
SFLASH_MACRO_0_FREE_SFLASH594	0x0FFFF652
SFLASH_MACRO_0_FREE_SFLASH595	0x0FFFF653
SFLASH_MACRO_0_FREE_SFLASH596	0x0FFFF654
SFLASH_MACRO_0_FREE_SFLASH597	0x0FFFF655
SFLASH_MACRO_0_FREE_SFLASH598	0x0FFFF656
SFLASH_MACRO_0_FREE_SFLASH599	0x0FFFF657
SFLASH_MACRO_0_FREE_SFLASH600	0x0FFFF658

Register Name	Address
SFLASH_MACRO_0_FREE_SFLASH601	0x0FFFF659
SFLASH_MACRO_0_FREE_SFLASH602	0x0FFFF65A
SFLASH_MACRO_0_FREE_SFLASH603	0x0FFFF65B
SFLASH_MACRO_0_FREE_SFLASH604	0x0FFFF65C
SFLASH_MACRO_0_FREE_SFLASH605	0x0FFFF65D
SFLASH_MACRO_0_FREE_SFLASH606	0x0FFFF65E
SFLASH_MACRO_0_FREE_SFLASH607	0x0FFFF65F
SFLASH_MACRO_0_FREE_SFLASH608	0x0FFFF660
SFLASH_MACRO_0_FREE_SFLASH609	0x0FFFF661
SFLASH_MACRO_0_FREE_SFLASH610	0x0FFFF662
SFLASH_MACRO_0_FREE_SFLASH611	0x0FFFF663
SFLASH_MACRO_0_FREE_SFLASH612	0x0FFFF664
SFLASH_MACRO_0_FREE_SFLASH613	0x0FFFF665
SFLASH_MACRO_0_FREE_SFLASH614	0x0FFFF666
SFLASH_MACRO_0_FREE_SFLASH615	0x0FFFF667
SFLASH_MACRO_0_FREE_SFLASH616	0x0FFFF668
SFLASH_MACRO_0_FREE_SFLASH617	0x0FFFF669
SFLASH_MACRO_0_FREE_SFLASH618	0x0FFFF66A
SFLASH_MACRO_0_FREE_SFLASH619	0x0FFFF66B
SFLASH_MACRO_0_FREE_SFLASH620	0x0FFFF66C
SFLASH_MACRO_0_FREE_SFLASH621	0x0FFFF66D
SFLASH_MACRO_0_FREE_SFLASH622	0x0FFFF66E
SFLASH_MACRO_0_FREE_SFLASH623	0x0FFFF66F
SFLASH_MACRO_0_FREE_SFLASH624	0x0FFFF670
SFLASH_MACRO_0_FREE_SFLASH625	0x0FFFF671
SFLASH_MACRO_0_FREE_SFLASH626	0x0FFFF672
SFLASH_MACRO_0_FREE_SFLASH627	0x0FFFF673
SFLASH_MACRO_0_FREE_SFLASH628	0x0FFFF674
SFLASH_MACRO_0_FREE_SFLASH629	0x0FFFF675
SFLASH_MACRO_0_FREE_SFLASH630	0x0FFFF676
SFLASH_MACRO_0_FREE_SFLASH631	0x0FFFF677
SFLASH_MACRO_0_FREE_SFLASH632	0x0FFFF678
SFLASH_MACRO_0_FREE_SFLASH633	0x0FFFF679
SFLASH_MACRO_0_FREE_SFLASH634	0x0FFFF67A
SFLASH_MACRO_0_FREE_SFLASH635	0x0FFFF67B
SFLASH_MACRO_0_FREE_SFLASH636	0x0FFFF67C
SFLASH_MACRO_0_FREE_SFLASH637	0x0FFFF67D
SFLASH_MACRO_0_FREE_SFLASH638	0x0FFFF67E
SFLASH_MACRO_0_FREE_SFLASH639	0x0FFFF67F
SFLASH_MACRO_0_FREE_SFLASH640	0x0FFFF680
SFLASH_MACRO_0_FREE_SFLASH641	0x0FFFF681
SFLASH_MACRO_0_FREE_SFLASH642	0x0FFFF682

Register Name	Address
SFLASH_MACRO_0_FREE_SFLASH643	0x0FFFF683
SFLASH_MACRO_0_FREE_SFLASH644	0x0FFFF684
SFLASH_MACRO_0_FREE_SFLASH645	0x0FFFF685
SFLASH_MACRO_0_FREE_SFLASH646	0x0FFFF686
SFLASH_MACRO_0_FREE_SFLASH647	0x0FFFF687
SFLASH_MACRO_0_FREE_SFLASH648	0x0FFFF688
SFLASH_MACRO_0_FREE_SFLASH649	0x0FFFF689
SFLASH_MACRO_0_FREE_SFLASH650	0x0FFFF68A
SFLASH_MACRO_0_FREE_SFLASH651	0x0FFFF68B
SFLASH_MACRO_0_FREE_SFLASH652	0x0FFFF68C
SFLASH_MACRO_0_FREE_SFLASH653	0x0FFFF68D
SFLASH_MACRO_0_FREE_SFLASH654	0x0FFFF68E
SFLASH_MACRO_0_FREE_SFLASH655	0x0FFFF68F
SFLASH_MACRO_0_FREE_SFLASH656	0x0FFFF690
SFLASH_MACRO_0_FREE_SFLASH657	0x0FFFF691
SFLASH_MACRO_0_FREE_SFLASH658	0x0FFFF692
SFLASH_MACRO_0_FREE_SFLASH659	0x0FFFF693
SFLASH_MACRO_0_FREE_SFLASH660	0x0FFFF694
SFLASH_MACRO_0_FREE_SFLASH661	0x0FFFF695
SFLASH_MACRO_0_FREE_SFLASH662	0x0FFFF696
SFLASH_MACRO_0_FREE_SFLASH663	0x0FFFF697
SFLASH_MACRO_0_FREE_SFLASH664	0x0FFFF698
SFLASH_MACRO_0_FREE_SFLASH665	0x0FFFF699
SFLASH_MACRO_0_FREE_SFLASH666	0x0FFFF69A
SFLASH_MACRO_0_FREE_SFLASH667	0x0FFFF69B
SFLASH_MACRO_0_FREE_SFLASH668	0x0FFFF69C
SFLASH_MACRO_0_FREE_SFLASH669	0x0FFFF69D
SFLASH_MACRO_0_FREE_SFLASH670	0x0FFFF69E
SFLASH_MACRO_0_FREE_SFLASH671	0x0FFFF69F
SFLASH_MACRO_0_FREE_SFLASH672	0x0FFFF6A0
SFLASH_MACRO_0_FREE_SFLASH673	0x0FFFF6A1
SFLASH_MACRO_0_FREE_SFLASH674	0x0FFFF6A2
SFLASH_MACRO_0_FREE_SFLASH675	0x0FFFF6A3
SFLASH_MACRO_0_FREE_SFLASH676	0x0FFFF6A4
SFLASH_MACRO_0_FREE_SFLASH677	0x0FFFF6A5
SFLASH_MACRO_0_FREE_SFLASH678	0x0FFFF6A6
SFLASH_MACRO_0_FREE_SFLASH679	0x0FFFF6A7
SFLASH_MACRO_0_FREE_SFLASH680	0x0FFFF6A8
SFLASH_MACRO_0_FREE_SFLASH681	0x0FFFF6A9
SFLASH_MACRO_0_FREE_SFLASH682	0x0FFFF6AA
SFLASH_MACRO_0_FREE_SFLASH683	0x0FFFF6AB
SFLASH_MACRO_0_FREE_SFLASH684	0x0FFFF6AC

Register Name	Address
SFLASH_MACRO_0_FREE_SFLASH685	0x0FFFF6AD
SFLASH_MACRO_0_FREE_SFLASH686	0x0FFFF6AE
SFLASH_MACRO_0_FREE_SFLASH687	0x0FFFF6AF
SFLASH_MACRO_0_FREE_SFLASH688	0x0FFFF6B0
SFLASH_MACRO_0_FREE_SFLASH689	0x0FFFF6B1
SFLASH_MACRO_0_FREE_SFLASH690	0x0FFFF6B2
SFLASH_MACRO_0_FREE_SFLASH691	0x0FFFF6B3
SFLASH_MACRO_0_FREE_SFLASH692	0x0FFFF6B4
SFLASH_MACRO_0_FREE_SFLASH693	0x0FFFF6B5
SFLASH_MACRO_0_FREE_SFLASH694	0x0FFFF6B6
SFLASH_MACRO_0_FREE_SFLASH695	0x0FFFF6B7
SFLASH_MACRO_0_FREE_SFLASH696	0x0FFFF6B8
SFLASH_MACRO_0_FREE_SFLASH697	0x0FFFF6B9
SFLASH_MACRO_0_FREE_SFLASH698	0x0FFFF6BA
SFLASH_MACRO_0_FREE_SFLASH699	0x0FFFF6BB
SFLASH_MACRO_0_FREE_SFLASH700	0x0FFFF6BC
SFLASH_MACRO_0_FREE_SFLASH701	0x0FFFF6BD
SFLASH_MACRO_0_FREE_SFLASH702	0x0FFFF6BE
SFLASH_MACRO_0_FREE_SFLASH703	0x0FFFF6BF
SFLASH_MACRO_0_FREE_SFLASH704	0x0FFFF6C0
SFLASH_MACRO_0_FREE_SFLASH705	0x0FFFF6C1
SFLASH_MACRO_0_FREE_SFLASH706	0x0FFFF6C2
SFLASH_MACRO_0_FREE_SFLASH707	0x0FFFF6C3
SFLASH_MACRO_0_FREE_SFLASH708	0x0FFFF6C4
SFLASH_MACRO_0_FREE_SFLASH709	0x0FFFF6C5
SFLASH_MACRO_0_FREE_SFLASH710	0x0FFFF6C6
SFLASH_MACRO_0_FREE_SFLASH711	0x0FFFF6C7
SFLASH_MACRO_0_FREE_SFLASH712	0x0FFFF6C8
SFLASH_MACRO_0_FREE_SFLASH713	0x0FFFF6C9
SFLASH_MACRO_0_FREE_SFLASH714	0x0FFFF6CA
SFLASH_MACRO_0_FREE_SFLASH715	0x0FFFF6CB
SFLASH_MACRO_0_FREE_SFLASH716	0x0FFFF6CC
SFLASH_MACRO_0_FREE_SFLASH717	0x0FFFF6CD
SFLASH_MACRO_0_FREE_SFLASH718	0x0FFFF6CE
SFLASH_MACRO_0_FREE_SFLASH719	0x0FFFF6CF
SFLASH_MACRO_0_FREE_SFLASH720	0x0FFFF6D0
SFLASH_MACRO_0_FREE_SFLASH721	0x0FFFF6D1
SFLASH_MACRO_0_FREE_SFLASH722	0x0FFFF6D2
SFLASH_MACRO_0_FREE_SFLASH723	0x0FFFF6D3
SFLASH_MACRO_0_FREE_SFLASH724	0x0FFFF6D4
SFLASH_MACRO_0_FREE_SFLASH725	0x0FFFF6D5
SFLASH_MACRO_0_FREE_SFLASH726	0x0FFFF6D6

Register Name	Address
SFLASH_MACRO_0_FREE_SFLASH727	0x0FFFF6D7
SFLASH_MACRO_0_FREE_SFLASH728	0x0FFFF6D8
SFLASH_MACRO_0_FREE_SFLASH729	0x0FFFF6D9
SFLASH_MACRO_0_FREE_SFLASH730	0x0FFFF6DA
SFLASH_MACRO_0_FREE_SFLASH731	0x0FFFF6DB
SFLASH_MACRO_0_FREE_SFLASH732	0x0FFFF6DC
SFLASH_MACRO_0_FREE_SFLASH733	0x0FFFF6DD
SFLASH_MACRO_0_FREE_SFLASH734	0x0FFFF6DE
SFLASH_MACRO_0_FREE_SFLASH735	0x0FFFF6DF
SFLASH_MACRO_0_FREE_SFLASH736	0x0FFFF6E0
SFLASH_MACRO_0_FREE_SFLASH737	0x0FFFF6E1
SFLASH_MACRO_0_FREE_SFLASH738	0x0FFFF6E2
SFLASH_MACRO_0_FREE_SFLASH739	0x0FFFF6E3
SFLASH_MACRO_0_FREE_SFLASH740	0x0FFFF6E4
SFLASH_MACRO_0_FREE_SFLASH741	0x0FFFF6E5
SFLASH_MACRO_0_FREE_SFLASH742	0x0FFFF6E6
SFLASH_MACRO_0_FREE_SFLASH743	0x0FFFF6E7
SFLASH_MACRO_0_FREE_SFLASH744	0x0FFFF6E8
SFLASH_MACRO_0_FREE_SFLASH745	0x0FFFF6E9
SFLASH_MACRO_0_FREE_SFLASH746	0x0FFFF6EA
SFLASH_MACRO_0_FREE_SFLASH747	0x0FFFF6EB
SFLASH_MACRO_0_FREE_SFLASH748	0x0FFFF6EC
SFLASH_MACRO_0_FREE_SFLASH749	0x0FFFF6ED
SFLASH_MACRO_0_FREE_SFLASH750	0x0FFFF6EE
SFLASH_MACRO_0_FREE_SFLASH751	0x0FFFF6EF
SFLASH_MACRO_0_FREE_SFLASH752	0x0FFFF6F0
SFLASH_MACRO_0_FREE_SFLASH753	0x0FFFF6F1
SFLASH_MACRO_0_FREE_SFLASH754	0x0FFFF6F2
SFLASH_MACRO_0_FREE_SFLASH755	0x0FFFF6F3
SFLASH_MACRO_0_FREE_SFLASH756	0x0FFFF6F4
SFLASH_MACRO_0_FREE_SFLASH757	0x0FFFF6F5
SFLASH_MACRO_0_FREE_SFLASH758	0x0FFFF6F6
SFLASH_MACRO_0_FREE_SFLASH759	0x0FFFF6F7
SFLASH_MACRO_0_FREE_SFLASH760	0x0FFFF6F8
SFLASH_MACRO_0_FREE_SFLASH761	0x0FFFF6F9
SFLASH_MACRO_0_FREE_SFLASH762	0x0FFFF6FA
SFLASH_MACRO_0_FREE_SFLASH763	0x0FFFF6FB
SFLASH_MACRO_0_FREE_SFLASH764	0x0FFFF6FC
SFLASH_MACRO_0_FREE_SFLASH765	0x0FFFF6FD
SFLASH_MACRO_0_FREE_SFLASH766	0x0FFFF6FE
SFLASH_MACRO_0_FREE_SFLASH767	0x0FFFF6FF
SFLASH_MACRO_0_FREE_SFLASH768	0x0FFFF700

Register Name	Address
SFLASH_MACRO_0_FREE_SFLASH769	0x0FFFF701
SFLASH_MACRO_0_FREE_SFLASH770	0x0FFFF702
SFLASH_MACRO_0_FREE_SFLASH771	0x0FFFF703
SFLASH_MACRO_0_FREE_SFLASH772	0x0FFFF704
SFLASH_MACRO_0_FREE_SFLASH773	0x0FFFF705
SFLASH_MACRO_0_FREE_SFLASH774	0x0FFFF706
SFLASH_MACRO_0_FREE_SFLASH775	0x0FFFF707
SFLASH_MACRO_0_FREE_SFLASH776	0x0FFFF708
SFLASH_MACRO_0_FREE_SFLASH777	0x0FFFF709
SFLASH_MACRO_0_FREE_SFLASH778	0x0FFFF70A
SFLASH_MACRO_0_FREE_SFLASH779	0x0FFFF70B
SFLASH_MACRO_0_FREE_SFLASH780	0x0FFFF70C
SFLASH_MACRO_0_FREE_SFLASH781	0x0FFFF70D
SFLASH_MACRO_0_FREE_SFLASH782	0x0FFFF70E
SFLASH_MACRO_0_FREE_SFLASH783	0x0FFFF70F
SFLASH_MACRO_0_FREE_SFLASH784	0x0FFFF710
SFLASH_MACRO_0_FREE_SFLASH785	0x0FFFF711
SFLASH_MACRO_0_FREE_SFLASH786	0x0FFFF712
SFLASH_MACRO_0_FREE_SFLASH787	0x0FFFF713
SFLASH_MACRO_0_FREE_SFLASH788	0x0FFFF714
SFLASH_MACRO_0_FREE_SFLASH789	0x0FFFF715
SFLASH_MACRO_0_FREE_SFLASH790	0x0FFFF716
SFLASH_MACRO_0_FREE_SFLASH791	0x0FFFF717
SFLASH_MACRO_0_FREE_SFLASH792	0x0FFFF718
SFLASH_MACRO_0_FREE_SFLASH793	0x0FFFF719
SFLASH_MACRO_0_FREE_SFLASH794	0x0FFFF71A
SFLASH_MACRO_0_FREE_SFLASH795	0x0FFFF71B
SFLASH_MACRO_0_FREE_SFLASH796	0x0FFFF71C
SFLASH_MACRO_0_FREE_SFLASH797	0x0FFFF71D
SFLASH_MACRO_0_FREE_SFLASH798	0x0FFFF71E
SFLASH_MACRO_0_FREE_SFLASH799	0x0FFFF71F
SFLASH_MACRO_0_FREE_SFLASH800	0x0FFFF720
SFLASH_MACRO_0_FREE_SFLASH801	0x0FFFF721
SFLASH_MACRO_0_FREE_SFLASH802	0x0FFFF722
SFLASH_MACRO_0_FREE_SFLASH803	0x0FFFF723
SFLASH_MACRO_0_FREE_SFLASH804	0x0FFFF724
SFLASH_MACRO_0_FREE_SFLASH805	0x0FFFF725
SFLASH_MACRO_0_FREE_SFLASH806	0x0FFFF726
SFLASH_MACRO_0_FREE_SFLASH807	0x0FFFF727
SFLASH_MACRO_0_FREE_SFLASH808	0x0FFFF728
SFLASH_MACRO_0_FREE_SFLASH809	0x0FFFF729
SFLASH_MACRO_0_FREE_SFLASH810	0x0FFFF72A

Register Name	Address
SFLASH_MACRO_0_FREE_SFLASH811	0x0FFFF72B
SFLASH_MACRO_0_FREE_SFLASH812	0x0FFFF72C
SFLASH_MACRO_0_FREE_SFLASH813	0x0FFFF72D
SFLASH_MACRO_0_FREE_SFLASH814	0x0FFFF72E
SFLASH_MACRO_0_FREE_SFLASH815	0x0FFFF72F
SFLASH_MACRO_0_FREE_SFLASH816	0x0FFFF730
SFLASH_MACRO_0_FREE_SFLASH817	0x0FFFF731
SFLASH_MACRO_0_FREE_SFLASH818	0x0FFFF732
SFLASH_MACRO_0_FREE_SFLASH819	0x0FFFF733
SFLASH_MACRO_0_FREE_SFLASH820	0x0FFFF734
SFLASH_MACRO_0_FREE_SFLASH821	0x0FFFF735
SFLASH_MACRO_0_FREE_SFLASH822	0x0FFFF736
SFLASH_MACRO_0_FREE_SFLASH823	0x0FFFF737
SFLASH_MACRO_0_FREE_SFLASH824	0x0FFFF738
SFLASH_MACRO_0_FREE_SFLASH825	0x0FFFF739
SFLASH_MACRO_0_FREE_SFLASH826	0x0FFFF73A
SFLASH_MACRO_0_FREE_SFLASH827	0x0FFFF73B
SFLASH_MACRO_0_FREE_SFLASH828	0x0FFFF73C
SFLASH_MACRO_0_FREE_SFLASH829	0x0FFFF73D
SFLASH_MACRO_0_FREE_SFLASH830	0x0FFFF73E
SFLASH_MACRO_0_FREE_SFLASH831	0x0FFFF73F
SFLASH_MACRO_0_FREE_SFLASH832	0x0FFFF740
SFLASH_MACRO_0_FREE_SFLASH833	0x0FFFF741
SFLASH_MACRO_0_FREE_SFLASH834	0x0FFFF742
SFLASH_MACRO_0_FREE_SFLASH835	0x0FFFF743
SFLASH_MACRO_0_FREE_SFLASH836	0x0FFFF744
SFLASH_MACRO_0_FREE_SFLASH837	0x0FFFF745
SFLASH_MACRO_0_FREE_SFLASH838	0x0FFFF746
SFLASH_MACRO_0_FREE_SFLASH839	0x0FFFF747
SFLASH_MACRO_0_FREE_SFLASH840	0x0FFFF748
SFLASH_MACRO_0_FREE_SFLASH841	0x0FFFF749
SFLASH_MACRO_0_FREE_SFLASH842	0x0FFFF74A
SFLASH_MACRO_0_FREE_SFLASH843	0x0FFFF74B
SFLASH_MACRO_0_FREE_SFLASH844	0x0FFFF74C
SFLASH_MACRO_0_FREE_SFLASH845	0x0FFFF74D
SFLASH_MACRO_0_FREE_SFLASH846	0x0FFFF74E
SFLASH_MACRO_0_FREE_SFLASH847	0x0FFFF74F
SFLASH_MACRO_0_FREE_SFLASH848	0x0FFFF750
SFLASH_MACRO_0_FREE_SFLASH849	0x0FFFF751
SFLASH_MACRO_0_FREE_SFLASH850	0x0FFFF752
SFLASH_MACRO_0_FREE_SFLASH851	0x0FFFF753
SFLASH_MACRO_0_FREE_SFLASH852	0x0FFFF754

Register Name	Address
SFLASH_MACRO_0_FREE_SFLASH853	0x0FFFF755
SFLASH_MACRO_0_FREE_SFLASH854	0x0FFFF756
SFLASH_MACRO_0_FREE_SFLASH855	0x0FFFF757
SFLASH_MACRO_0_FREE_SFLASH856	0x0FFFF758
SFLASH_MACRO_0_FREE_SFLASH857	0x0FFFF759
SFLASH_MACRO_0_FREE_SFLASH858	0x0FFFF75A
SFLASH_MACRO_0_FREE_SFLASH859	0x0FFFF75B
SFLASH_MACRO_0_FREE_SFLASH860	0x0FFFF75C
SFLASH_MACRO_0_FREE_SFLASH861	0x0FFFF75D
SFLASH_MACRO_0_FREE_SFLASH862	0x0FFFF75E
SFLASH_MACRO_0_FREE_SFLASH863	0x0FFFF75F
SFLASH_MACRO_0_FREE_SFLASH864	0x0FFFF760
SFLASH_MACRO_0_FREE_SFLASH865	0x0FFFF761
SFLASH_MACRO_0_FREE_SFLASH866	0x0FFFF762
SFLASH_MACRO_0_FREE_SFLASH867	0x0FFFF763
SFLASH_MACRO_0_FREE_SFLASH868	0x0FFFF764
SFLASH_MACRO_0_FREE_SFLASH869	0x0FFFF765
SFLASH_MACRO_0_FREE_SFLASH870	0x0FFFF766
SFLASH_MACRO_0_FREE_SFLASH871	0x0FFFF767
SFLASH_MACRO_0_FREE_SFLASH872	0x0FFFF768
SFLASH_MACRO_0_FREE_SFLASH873	0x0FFFF769
SFLASH_MACRO_0_FREE_SFLASH874	0x0FFFF76A
SFLASH_MACRO_0_FREE_SFLASH875	0x0FFFF76B
SFLASH_MACRO_0_FREE_SFLASH876	0x0FFFF76C
SFLASH_MACRO_0_FREE_SFLASH877	0x0FFFF76D
SFLASH_MACRO_0_FREE_SFLASH878	0x0FFFF76E
SFLASH_MACRO_0_FREE_SFLASH879	0x0FFFF76F
SFLASH_MACRO_0_FREE_SFLASH880	0x0FFFF770
SFLASH_MACRO_0_FREE_SFLASH881	0x0FFFF771
SFLASH_MACRO_0_FREE_SFLASH882	0x0FFFF772
SFLASH_MACRO_0_FREE_SFLASH883	0x0FFFF773
SFLASH_MACRO_0_FREE_SFLASH884	0x0FFFF774
SFLASH_MACRO_0_FREE_SFLASH885	0x0FFFF775
SFLASH_MACRO_0_FREE_SFLASH886	0x0FFFF776
SFLASH_MACRO_0_FREE_SFLASH887	0x0FFFF777
SFLASH_MACRO_0_FREE_SFLASH888	0x0FFFF778
SFLASH_MACRO_0_FREE_SFLASH889	0x0FFFF779
SFLASH_MACRO_0_FREE_SFLASH890	0x0FFFF77A
SFLASH_MACRO_0_FREE_SFLASH891	0x0FFFF77B
SFLASH_MACRO_0_FREE_SFLASH892	0x0FFFF77C
SFLASH_MACRO_0_FREE_SFLASH893	0x0FFFF77D
SFLASH_MACRO_0_FREE_SFLASH894	0x0FFFF77E

Register Name	Address
SFLASH_MACRO_0_FREE_SFLASH895	0x0FFFF77F
SFLASH_MACRO_0_FREE_SFLASH896	0x0FFFF780
SFLASH_MACRO_0_FREE_SFLASH897	0x0FFFF781
SFLASH_MACRO_0_FREE_SFLASH898	0x0FFFF782
SFLASH_MACRO_0_FREE_SFLASH899	0x0FFFF783
SFLASH_MACRO_0_FREE_SFLASH900	0x0FFFF784
SFLASH_MACRO_0_FREE_SFLASH901	0x0FFFF785
SFLASH_MACRO_0_FREE_SFLASH902	0x0FFFF786
SFLASH_MACRO_0_FREE_SFLASH903	0x0FFFF787
SFLASH_MACRO_0_FREE_SFLASH904	0x0FFFF788
SFLASH_MACRO_0_FREE_SFLASH905	0x0FFFF789
SFLASH_MACRO_0_FREE_SFLASH906	0x0FFFF78A
SFLASH_MACRO_0_FREE_SFLASH907	0x0FFFF78B
SFLASH_MACRO_0_FREE_SFLASH908	0x0FFFF78C
SFLASH_MACRO_0_FREE_SFLASH909	0x0FFFF78D
SFLASH_MACRO_0_FREE_SFLASH910	0x0FFFF78E
SFLASH_MACRO_0_FREE_SFLASH911	0x0FFFF78F
SFLASH_MACRO_0_FREE_SFLASH912	0x0FFFF790
SFLASH_MACRO_0_FREE_SFLASH913	0x0FFFF791
SFLASH_MACRO_0_FREE_SFLASH914	0x0FFFF792
SFLASH_MACRO_0_FREE_SFLASH915	0x0FFFF793
SFLASH_MACRO_0_FREE_SFLASH916	0x0FFFF794
SFLASH_MACRO_0_FREE_SFLASH917	0x0FFFF795
SFLASH_MACRO_0_FREE_SFLASH918	0x0FFFF796
SFLASH_MACRO_0_FREE_SFLASH919	0x0FFFF797
SFLASH_MACRO_0_FREE_SFLASH920	0x0FFFF798
SFLASH_MACRO_0_FREE_SFLASH921	0x0FFFF799
SFLASH_MACRO_0_FREE_SFLASH922	0x0FFFF79A
SFLASH_MACRO_0_FREE_SFLASH923	0x0FFFF79B
SFLASH_MACRO_0_FREE_SFLASH924	0x0FFFF79C
SFLASH_MACRO_0_FREE_SFLASH925	0x0FFFF79D
SFLASH_MACRO_0_FREE_SFLASH926	0x0FFFF79E
SFLASH_MACRO_0_FREE_SFLASH927	0x0FFFF79F
SFLASH_MACRO_0_FREE_SFLASH928	0x0FFFF7A0
SFLASH_MACRO_0_FREE_SFLASH929	0x0FFFF7A1
SFLASH_MACRO_0_FREE_SFLASH930	0x0FFFF7A2
SFLASH_MACRO_0_FREE_SFLASH931	0x0FFFF7A3
SFLASH_MACRO_0_FREE_SFLASH932	0x0FFFF7A4
SFLASH_MACRO_0_FREE_SFLASH933	0x0FFFF7A5
SFLASH_MACRO_0_FREE_SFLASH934	0x0FFFF7A6
SFLASH_MACRO_0_FREE_SFLASH935	0x0FFFF7A7
SFLASH_MACRO_0_FREE_SFLASH936	0x0FFFF7A8

Register Name	Address
SFLASH_MACRO_0_FREE_SFLASH937	0x0FFFF7A9
SFLASH_MACRO_0_FREE_SFLASH938	0x0FFFF7AA
SFLASH_MACRO_0_FREE_SFLASH939	0x0FFFF7AB
SFLASH_MACRO_0_FREE_SFLASH940	0x0FFFF7AC
SFLASH_MACRO_0_FREE_SFLASH941	0x0FFFF7AD
SFLASH_MACRO_0_FREE_SFLASH942	0x0FFFF7AE
SFLASH_MACRO_0_FREE_SFLASH943	0x0FFFF7AF
SFLASH_MACRO_0_FREE_SFLASH944	0x0FFFF7B0
SFLASH_MACRO_0_FREE_SFLASH945	0x0FFFF7B1
SFLASH_MACRO_0_FREE_SFLASH946	0x0FFFF7B2
SFLASH_MACRO_0_FREE_SFLASH947	0x0FFFF7B3
SFLASH_MACRO_0_FREE_SFLASH948	0x0FFFF7B4
SFLASH_MACRO_0_FREE_SFLASH949	0x0FFFF7B5
SFLASH_MACRO_0_FREE_SFLASH950	0x0FFFF7B6
SFLASH_MACRO_0_FREE_SFLASH951	0x0FFFF7B7
SFLASH_MACRO_0_FREE_SFLASH952	0x0FFFF7B8
SFLASH_MACRO_0_FREE_SFLASH953	0x0FFFF7B9
SFLASH_MACRO_0_FREE_SFLASH954	0x0FFFF7BA
SFLASH_MACRO_0_FREE_SFLASH955	0x0FFFF7BB
SFLASH_MACRO_0_FREE_SFLASH956	0x0FFFF7BC
SFLASH_MACRO_0_FREE_SFLASH957	0x0FFFF7BD
SFLASH_MACRO_0_FREE_SFLASH958	0x0FFFF7BE
SFLASH_MACRO_0_FREE_SFLASH959	0x0FFFF7BF
SFLASH_MACRO_0_FREE_SFLASH960	0x0FFFF7C0
SFLASH_MACRO_0_FREE_SFLASH961	0x0FFFF7C1
SFLASH_MACRO_0_FREE_SFLASH962	0x0FFFF7C2
SFLASH_MACRO_0_FREE_SFLASH963	0x0FFFF7C3
SFLASH_MACRO_0_FREE_SFLASH964	0x0FFFF7C4
SFLASH_MACRO_0_FREE_SFLASH965	0x0FFFF7C5
SFLASH_MACRO_0_FREE_SFLASH966	0x0FFFF7C6
SFLASH_MACRO_0_FREE_SFLASH967	0x0FFFF7C7
SFLASH_MACRO_0_FREE_SFLASH968	0x0FFFF7C8
SFLASH_MACRO_0_FREE_SFLASH969	0x0FFFF7C9
SFLASH_MACRO_0_FREE_SFLASH970	0x0FFFF7CA
SFLASH_MACRO_0_FREE_SFLASH971	0x0FFFF7CB
SFLASH_MACRO_0_FREE_SFLASH972	0x0FFFF7CC
SFLASH_MACRO_0_FREE_SFLASH973	0x0FFFF7CD
SFLASH_MACRO_0_FREE_SFLASH974	0x0FFFF7CE
SFLASH_MACRO_0_FREE_SFLASH975	0x0FFFF7CF
SFLASH_MACRO_0_FREE_SFLASH976	0x0FFFF7D0
SFLASH_MACRO_0_FREE_SFLASH977	0x0FFFF7D1
SFLASH_MACRO_0_FREE_SFLASH978	0x0FFFF7D2

Register Name	Address
SFLASH_MACRO_0_FREE_SFLASH979	0x0FFFF7D3
SFLASH_MACRO_0_FREE_SFLASH980	0x0FFFF7D4
SFLASH_MACRO_0_FREE_SFLASH981	0x0FFFF7D5
SFLASH_MACRO_0_FREE_SFLASH982	0x0FFFF7D6
SFLASH_MACRO_0_FREE_SFLASH983	0x0FFFF7D7
SFLASH_MACRO_0_FREE_SFLASH984	0x0FFFF7D8
SFLASH_MACRO_0_FREE_SFLASH985	0x0FFFF7D9
SFLASH_MACRO_0_FREE_SFLASH986	0x0FFFF7DA
SFLASH_MACRO_0_FREE_SFLASH987	0x0FFFF7DB
SFLASH_MACRO_0_FREE_SFLASH988	0x0FFFF7DC
SFLASH_MACRO_0_FREE_SFLASH989	0x0FFFF7DD
SFLASH_MACRO_0_FREE_SFLASH990	0x0FFFF7DE
SFLASH_MACRO_0_FREE_SFLASH991	0x0FFFF7DF
SFLASH_MACRO_0_FREE_SFLASH992	0x0FFFF7E0
SFLASH_MACRO_0_FREE_SFLASH993	0x0FFFF7E1
SFLASH_MACRO_0_FREE_SFLASH994	0x0FFFF7E2
SFLASH_MACRO_0_FREE_SFLASH995	0x0FFFF7E3
SFLASH_MACRO_0_FREE_SFLASH996	0x0FFFF7E4
SFLASH_MACRO_0_FREE_SFLASH997	0x0FFFF7E5
SFLASH_MACRO_0_FREE_SFLASH998	0x0FFFF7E6
SFLASH_MACRO_0_FREE_SFLASH999	0x0FFFF7E7
SFLASH_MACRO_0_FREE_SFLASH1000	0x0FFFF7E8
SFLASH_MACRO_0_FREE_SFLASH1001	0x0FFFF7E9
SFLASH_MACRO_0_FREE_SFLASH1002	0x0FFFF7EA
SFLASH_MACRO_0_FREE_SFLASH1003	0x0FFFF7EB
SFLASH_MACRO_0_FREE_SFLASH1004	0x0FFFF7EC
SFLASH_MACRO_0_FREE_SFLASH1005	0x0FFFF7ED
SFLASH_MACRO_0_FREE_SFLASH1006	0x0FFFF7EE
SFLASH_MACRO_0_FREE_SFLASH1007	0x0FFFF7EF
SFLASH_MACRO_0_FREE_SFLASH1008	0x0FFFF7F0
SFLASH_MACRO_0_FREE_SFLASH1009	0x0FFFF7F1
SFLASH_MACRO_0_FREE_SFLASH1010	0x0FFFF7F2
SFLASH_MACRO_0_FREE_SFLASH1011	0x0FFFF7F3
SFLASH_MACRO_0_FREE_SFLASH1012	0x0FFFF7F4
SFLASH_MACRO_0_FREE_SFLASH1013	0x0FFFF7F5
SFLASH_MACRO_0_FREE_SFLASH1014	0x0FFFF7F6
SFLASH_MACRO_0_FREE_SFLASH1015	0x0FFFF7F7
SFLASH_MACRO_0_FREE_SFLASH1016	0x0FFFF7F8
SFLASH_MACRO_0_FREE_SFLASH1017	0x0FFFF7F9
SFLASH_MACRO_0_FREE_SFLASH1018	0x0FFFF7FA
SFLASH_MACRO_0_FREE_SFLASH1019	0x0FFFF7FB
SFLASH_MACRO_0_FREE_SFLASH1020	0x0FFFF7FC

Register Name	Address
SFLASH_MACRO_0_FREE_SFLASH1021	0x0FFFF7FD
SFLASH_MACRO_0_FREE_SFLASH1022	0x0FFFF7FE
SFLASH_MACRO_0_FREE_SFLASH1023	0x0FFFF7FF
SFLASH_ALT_PROT_ROW0	0x0FFFF800
SFLASH_ALT_PROT_ROW1	0x0FFFF801
SFLASH_ALT_PROT_ROW2	0x0FFFF802
SFLASH_ALT_PROT_ROW3	0x0FFFF803
SFLASH_ALT_PROT_ROW4	0x0FFFF804
SFLASH_ALT_PROT_ROW5	0x0FFFF805
SFLASH_ALT_PROT_ROW6	0x0FFFF806
SFLASH_ALT_PROT_ROW7	0x0FFFF807
SFLASH_ALT_PROT_ROW8	0x0FFFF808
SFLASH_ALT_PROT_ROW9	0x0FFFF809
SFLASH_ALT_PROT_ROW10	0x0FFFF80A
SFLASH_ALT_PROT_ROW11	0x0FFFF80B
SFLASH_ALT_PROT_ROW12	0x0FFFF80C
SFLASH_ALT_PROT_ROW13	0x0FFFF80D
SFLASH_ALT_PROT_ROW14	0x0FFFF80E
SFLASH_ALT_PROT_ROW15	0x0FFFF80F
SFLASH_ALT_PROT_ROW16	0x0FFFF810
SFLASH_ALT_PROT_ROW17	0x0FFFF811
SFLASH_ALT_PROT_ROW18	0x0FFFF812
SFLASH_ALT_PROT_ROW19	0x0FFFF813
SFLASH_ALT_PROT_ROW20	0x0FFFF814
SFLASH_ALT_PROT_ROW21	0x0FFFF815
SFLASH_ALT_PROT_ROW22	0x0FFFF816
SFLASH_ALT_PROT_ROW23	0x0FFFF817
SFLASH_ALT_PROT_ROW24	0x0FFFF818
SFLASH_ALT_PROT_ROW25	0x0FFFF819
SFLASH_ALT_PROT_ROW26	0x0FFFF81A
SFLASH_ALT_PROT_ROW27	0x0FFFF81B
SFLASH_ALT_PROT_ROW28	0x0FFFF81C
SFLASH_ALT_PROT_ROW29	0x0FFFF81D
SFLASH_ALT_PROT_ROW30	0x0FFFF81E
SFLASH_ALT_PROT_ROW31	0x0FFFF81F
SFLASH_ALT_PROT_ROW32	0x0FFFF820
SFLASH_ALT_PROT_ROW33	0x0FFFF821
SFLASH_ALT_PROT_ROW34	0x0FFFF822
SFLASH_ALT_PROT_ROW35	0x0FFFF823
SFLASH_ALT_PROT_ROW36	0x0FFFF824
SFLASH_ALT_PROT_ROW37	0x0FFFF825
SFLASH_ALT_PROT_ROW38	0x0FFFF826

Register Name	Address
SFLASH_ALT_PROT_ROW39	0x0FFFF827
SFLASH_ALT_PROT_ROW40	0x0FFFF828
SFLASH_ALT_PROT_ROW41	0x0FFFF829
SFLASH_ALT_PROT_ROW42	0x0FFFF82A
SFLASH_ALT_PROT_ROW43	0x0FFFF82B
SFLASH_ALT_PROT_ROW44	0x0FFFF82C
SFLASH_ALT_PROT_ROW45	0x0FFFF82D
SFLASH_ALT_PROT_ROW46	0x0FFFF82E
SFLASH_ALT_PROT_ROW47	0x0FFFF82F
SFLASH_ALT_PROT_ROW48	0x0FFFF830
SFLASH_ALT_PROT_ROW49	0x0FFFF831
SFLASH_ALT_PROT_ROW50	0x0FFFF832
SFLASH_ALT_PROT_ROW51	0x0FFFF833
SFLASH_ALT_PROT_ROW52	0x0FFFF834
SFLASH_ALT_PROT_ROW53	0x0FFFF835
SFLASH_ALT_PROT_ROW54	0x0FFFF836
SFLASH_ALT_PROT_ROW55	0x0FFFF837
SFLASH_ALT_PROT_ROW56	0x0FFFF838
SFLASH_ALT_PROT_ROW57	0x0FFFF839
SFLASH_ALT_PROT_ROW58	0x0FFFF83A
SFLASH_ALT_PROT_ROW59	0x0FFFF83B
SFLASH_ALT_PROT_ROW60	0x0FFFF83C
SFLASH_ALT_PROT_ROW61	0x0FFFF83D
SFLASH_ALT_PROT_ROW62	0x0FFFF83E
SFLASH_ALT_PROT_ROW63	0x0FFFF83F
SFLASH_ALT_PROT_ROW64	0x0FFFF840
SFLASH_ALT_PROT_ROW65	0x0FFFF841
SFLASH_ALT_PROT_ROW66	0x0FFFF842
SFLASH_ALT_PROT_ROW67	0x0FFFF843
SFLASH_ALT_PROT_ROW68	0x0FFFF844
SFLASH_ALT_PROT_ROW69	0x0FFFF845
SFLASH_ALT_PROT_ROW70	0x0FFFF846
SFLASH_ALT_PROT_ROW71	0x0FFFF847
SFLASH_ALT_PROT_ROW72	0x0FFFF848
SFLASH_ALT_PROT_ROW73	0x0FFFF849
SFLASH_ALT_PROT_ROW74	0x0FFFF84A
SFLASH_ALT_PROT_ROW75	0x0FFFF84B
SFLASH_ALT_PROT_ROW76	0x0FFFF84C
SFLASH_ALT_PROT_ROW77	0x0FFFF84D
SFLASH_ALT_PROT_ROW78	0x0FFFF84E
SFLASH_ALT_PROT_ROW79	0x0FFFF84F
SFLASH_ALT_PROT_ROW80	0x0FFFF850

Register Name	Address
SFLASH_ALT_PROT_ROW81	0x0FFFF851
SFLASH_ALT_PROT_ROW82	0x0FFFF852
SFLASH_ALT_PROT_ROW83	0x0FFFF853
SFLASH_ALT_PROT_ROW84	0x0FFFF854
SFLASH_ALT_PROT_ROW85	0x0FFFF855
SFLASH_ALT_PROT_ROW86	0x0FFFF856
SFLASH_ALT_PROT_ROW87	0x0FFFF857
SFLASH_ALT_PROT_ROW88	0x0FFFF858
SFLASH_ALT_PROT_ROW89	0x0FFFF859
SFLASH_ALT_PROT_ROW90	0x0FFFF85A
SFLASH_ALT_PROT_ROW91	0x0FFFF85B
SFLASH_ALT_PROT_ROW92	0x0FFFF85C
SFLASH_ALT_PROT_ROW93	0x0FFFF85D
SFLASH_ALT_PROT_ROW94	0x0FFFF85E
SFLASH_ALT_PROT_ROW95	0x0FFFF85F
SFLASH_ALT_PROT_ROW96	0x0FFFF860
SFLASH_ALT_PROT_ROW97	0x0FFFF861
SFLASH_ALT_PROT_ROW98	0x0FFFF862
SFLASH_ALT_PROT_ROW99	0x0FFFF863
SFLASH_ALT_PROT_ROW100	0x0FFFF864
SFLASH_ALT_PROT_ROW101	0x0FFFF865
SFLASH_ALT_PROT_ROW102	0x0FFFF866
SFLASH_ALT_PROT_ROW103	0x0FFFF867
SFLASH_ALT_PROT_ROW104	0x0FFFF868
SFLASH_ALT_PROT_ROW105	0x0FFFF869
SFLASH_ALT_PROT_ROW106	0x0FFFF86A
SFLASH_ALT_PROT_ROW107	0x0FFFF86B
SFLASH_ALT_PROT_ROW108	0x0FFFF86C
SFLASH_ALT_PROT_ROW109	0x0FFFF86D
SFLASH_ALT_PROT_ROW110	0x0FFFF86E
SFLASH_ALT_PROT_ROW111	0x0FFFF86F
SFLASH_ALT_PROT_ROW112	0x0FFFF870
SFLASH_ALT_PROT_ROW113	0x0FFFF871
SFLASH_ALT_PROT_ROW114	0x0FFFF872
SFLASH_ALT_PROT_ROW115	0x0FFFF873
SFLASH_ALT_PROT_ROW116	0x0FFFF874
SFLASH_ALT_PROT_ROW117	0x0FFFF875
SFLASH_ALT_PROT_ROW118	0x0FFFF876
SFLASH_ALT_PROT_ROW119	0x0FFFF877
SFLASH_ALT_PROT_ROW120	0x0FFFF878
SFLASH_ALT_PROT_ROW121	0x0FFFF879
SFLASH_ALT_PROT_ROW122	0x0FFFF87A

Register Name	Address
SFLASH_ALT_PROT_ROW123	0x0FFFF87B
SFLASH_ALT_PROT_ROW124	0x0FFFF87C
SFLASH_ALT_PROT_ROW125	0x0FFFF87D
SFLASH_ALT_PROT_ROW126	0x0FFFF87E
SFLASH_ALT_PROT_ROW127	0x0FFFF87F
SFLASH_ALT_PROT_ROW128	0x0FFFF880
SFLASH_ALT_PROT_ROW129	0x0FFFF881
SFLASH_ALT_PROT_ROW130	0x0FFFF882
SFLASH_ALT_PROT_ROW131	0x0FFFF883
SFLASH_ALT_PROT_ROW132	0x0FFFF884
SFLASH_ALT_PROT_ROW133	0x0FFFF885
SFLASH_ALT_PROT_ROW134	0x0FFFF886
SFLASH_ALT_PROT_ROW135	0x0FFFF887
SFLASH_ALT_PROT_ROW136	0x0FFFF888
SFLASH_ALT_PROT_ROW137	0x0FFFF889
SFLASH_ALT_PROT_ROW138	0x0FFFF88A
SFLASH_ALT_PROT_ROW139	0x0FFFF88B
SFLASH_ALT_PROT_ROW140	0x0FFFF88C
SFLASH_ALT_PROT_ROW141	0x0FFFF88D
SFLASH_ALT_PROT_ROW142	0x0FFFF88E
SFLASH_ALT_PROT_ROW143	0x0FFFF88F
SFLASH_ALT_PROT_ROW144	0x0FFFF890
SFLASH_ALT_PROT_ROW145	0x0FFFF891
SFLASH_ALT_PROT_ROW146	0x0FFFF892
SFLASH_ALT_PROT_ROW147	0x0FFFF893
SFLASH_ALT_PROT_ROW148	0x0FFFF894
SFLASH_ALT_PROT_ROW149	0x0FFFF895
SFLASH_ALT_PROT_ROW150	0x0FFFF896
SFLASH_ALT_PROT_ROW151	0x0FFFF897
SFLASH_ALT_PROT_ROW152	0x0FFFF898
SFLASH_ALT_PROT_ROW153	0x0FFFF899
SFLASH_ALT_PROT_ROW154	0x0FFFF89A
SFLASH_ALT_PROT_ROW155	0x0FFFF89B
SFLASH_ALT_PROT_ROW156	0x0FFFF89C
SFLASH_ALT_PROT_ROW157	0x0FFFF89D
SFLASH_ALT_PROT_ROW158	0x0FFFF89E
SFLASH_ALT_PROT_ROW159	0x0FFFF89F
SFLASH_ALT_PROT_ROW160	0x0FFFF8A0
SFLASH_ALT_PROT_ROW161	0x0FFFF8A1
SFLASH_ALT_PROT_ROW162	0x0FFFF8A2
SFLASH_ALT_PROT_ROW163	0x0FFFF8A3
SFLASH_ALT_PROT_ROW164	0x0FFFF8A4

Register Name	Address
SFLASH_ALT_PROT_ROW165	0x0FFFF8A5
SFLASH_ALT_PROT_ROW166	0x0FFFF8A6
SFLASH_ALT_PROT_ROW167	0x0FFFF8A7
SFLASH_ALT_PROT_ROW168	0x0FFFF8A8
SFLASH_ALT_PROT_ROW169	0x0FFFF8A9
SFLASH_ALT_PROT_ROW170	0x0FFFF8AA
SFLASH_ALT_PROT_ROW171	0x0FFFF8AB
SFLASH_ALT_PROT_ROW172	0x0FFFF8AC
SFLASH_ALT_PROT_ROW173	0x0FFFF8AD
SFLASH_ALT_PROT_ROW174	0x0FFFF8AE
SFLASH_ALT_PROT_ROW175	0x0FFFF8AF
SFLASH_ALT_PROT_ROW176	0x0FFFF8B0
SFLASH_ALT_PROT_ROW177	0x0FFFF8B1
SFLASH_ALT_PROT_ROW178	0x0FFFF8B2
SFLASH_ALT_PROT_ROW179	0x0FFFF8B3
SFLASH_ALT_PROT_ROW180	0x0FFFF8B4
SFLASH_ALT_PROT_ROW181	0x0FFFF8B5
SFLASH_ALT_PROT_ROW182	0x0FFFF8B6
SFLASH_ALT_PROT_ROW183	0x0FFFF8B7
SFLASH_ALT_PROT_ROW184	0x0FFFF8B8
SFLASH_ALT_PROT_ROW185	0x0FFFF8B9
SFLASH_ALT_PROT_ROW186	0x0FFFF8BA
SFLASH_ALT_PROT_ROW187	0x0FFFF8BB
SFLASH_ALT_PROT_ROW188	0x0FFFF8BC
SFLASH_ALT_PROT_ROW189	0x0FFFF8BD
SFLASH_ALT_PROT_ROW190	0x0FFFF8BE
SFLASH_ALT_PROT_ROW191	0x0FFFF8BF
SFLASH_ALT_PROT_ROW192	0x0FFFF8C0
SFLASH_ALT_PROT_ROW193	0x0FFFF8C1
SFLASH_ALT_PROT_ROW194	0x0FFFF8C2
SFLASH_ALT_PROT_ROW195	0x0FFFF8C3
SFLASH_ALT_PROT_ROW196	0x0FFFF8C4
SFLASH_ALT_PROT_ROW197	0x0FFFF8C5
SFLASH_ALT_PROT_ROW198	0x0FFFF8C6
SFLASH_ALT_PROT_ROW199	0x0FFFF8C7
SFLASH_ALT_PROT_ROW200	0x0FFFF8C8
SFLASH_ALT_PROT_ROW201	0x0FFFF8C9
SFLASH_ALT_PROT_ROW202	0x0FFFF8CA
SFLASH_ALT_PROT_ROW203	0x0FFFF8CB
SFLASH_ALT_PROT_ROW204	0x0FFFF8CC
SFLASH_ALT_PROT_ROW205	0x0FFFF8CD
SFLASH_ALT_PROT_ROW206	0x0FFFF8CE

Register Name	Address
SFLASH_ALT_PROT_ROW207	0x0FFFF8CF
SFLASH_ALT_PROT_ROW208	0x0FFFF8D0
SFLASH_ALT_PROT_ROW209	0x0FFFF8D1
SFLASH_ALT_PROT_ROW210	0x0FFFF8D2
SFLASH_ALT_PROT_ROW211	0x0FFFF8D3
SFLASH_ALT_PROT_ROW212	0x0FFFF8D4
SFLASH_ALT_PROT_ROW213	0x0FFFF8D5
SFLASH_ALT_PROT_ROW214	0x0FFFF8D6
SFLASH_ALT_PROT_ROW215	0x0FFFF8D7
SFLASH_ALT_PROT_ROW216	0x0FFFF8D8
SFLASH_ALT_PROT_ROW217	0x0FFFF8D9
SFLASH_ALT_PROT_ROW218	0x0FFFF8DA
SFLASH_ALT_PROT_ROW219	0x0FFFF8DB
SFLASH_ALT_PROT_ROW220	0x0FFFF8DC
SFLASH_ALT_PROT_ROW221	0x0FFFF8DD
SFLASH_ALT_PROT_ROW222	0x0FFFF8DE
SFLASH_ALT_PROT_ROW223	0x0FFFF8DF
SFLASH_ALT_PROT_ROW224	0x0FFFF8E0
SFLASH_ALT_PROT_ROW225	0x0FFFF8E1
SFLASH_ALT_PROT_ROW226	0x0FFFF8E2
SFLASH_ALT_PROT_ROW227	0x0FFFF8E3
SFLASH_ALT_PROT_ROW228	0x0FFFF8E4
SFLASH_ALT_PROT_ROW229	0x0FFFF8E5
SFLASH_ALT_PROT_ROW230	0x0FFFF8E6
SFLASH_ALT_PROT_ROW231	0x0FFFF8E7
SFLASH_ALT_PROT_ROW232	0x0FFFF8E8
SFLASH_ALT_PROT_ROW233	0x0FFFF8E9
SFLASH_ALT_PROT_ROW234	0x0FFFF8EA
SFLASH_ALT_PROT_ROW235	0x0FFFF8EB
SFLASH_ALT_PROT_ROW236	0x0FFFF8EC
SFLASH_ALT_PROT_ROW237	0x0FFFF8ED
SFLASH_ALT_PROT_ROW238	0x0FFFF8EE
SFLASH_ALT_PROT_ROW239	0x0FFFF8EF
SFLASH_ALT_PROT_ROW240	0x0FFFF8F0
SFLASH_ALT_PROT_ROW241	0x0FFFF8F1
SFLASH_ALT_PROT_ROW242	0x0FFFF8F2
SFLASH_ALT_PROT_ROW243	0x0FFFF8F3
SFLASH_ALT_PROT_ROW244	0x0FFFF8F4
SFLASH_ALT_PROT_ROW245	0x0FFFF8F5
SFLASH_ALT_PROT_ROW246	0x0FFFF8F6
SFLASH_ALT_PROT_ROW247	0x0FFFF8F7
SFLASH_ALT_PROT_ROW248	0x0FFFF8F8

Register Name	Address
SFLASH_ALT_PROT_ROW249	0x0FFFF8F9
SFLASH_ALT_PROT_ROW250	0x0FFFF8FA
SFLASH_ALT_PROT_ROW251	0x0FFFF8FB
SFLASH_ALT_PROT_ROW252	0x0FFFF8FC
SFLASH_ALT_PROT_ROW253	0x0FFFF8FD
SFLASH_ALT_PROT_ROW254	0x0FFFF8FE
SFLASH_ALT_PROT_ROW255	0x0FFFF8FF
SFLASH_ALT_PP	0x0FFFFB20
SFLASH_ALT_E	0x0FFFFB24
SFLASH_ALT_P	0x0FFFFB28
SFLASH_ALT_EA_E	0x0FFFFB2C
SFLASH_ALT_EA_P	0x0FFFFB30
SFLASH_ALT_ES_E	0x0FFFFB34
SFLASH_ALT_ES_P_EO	0x0FFFFB38
SFLASH_ALT_E_VCTAT	0x0FFFFB3C
SFLASH_ALT_P_VCTAT	0x0FFFFB3D

30.1.1 SFLASH_PROT_ROW0

Per Page Write Protection

Address: 0x0FFFF000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.2 SFLASH_PROT_ROW1

Per Page Write Protection

Address: 0x0FFFF001

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.3 SFLASH_PROT_ROW2

Per Page Write Protection

Address: 0x0FFFF002

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.4 SFLASH_PROT_ROW3

Per Page Write Protection

Address: 0x0FFFF003

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.5 SFLASH_PROT_ROW4

Per Page Write Protection

Address: 0x0FFFF004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.6 SFLASH_PROT_ROW5

Per Page Write Protection

Address: 0x0FFFF005

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.7 SFLASH_PROT_ROW6

Per Page Write Protection

Address: 0x0FFFF006

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.8 SFLASH_PROT_ROW7

Per Page Write Protection

Address: 0x0FFFF007

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.9 SFLASH_PROT_ROW8

Per Page Write Protection

Address: 0x0FFFF008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.10 SFLASH_PROT_ROW9

Per Page Write Protection

Address: 0x0FFFF009

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.11 SFLASH_PROT_ROW10

Per Page Write Protection

Address: 0x0FFFF00A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.12 SFLASH_PROT_ROW11

Per Page Write Protection

Address: 0x0FFFF00B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.13 SFLASH_PROT_ROW12

Per Page Write Protection

Address: 0x0FFFF00C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.14 SFLASH_PROT_ROW13

Per Page Write Protection

Address: 0x0FFFF00D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.15 SFLASH_PROT_ROW14

Per Page Write Protection

Address: 0x0FFFF00E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.16 SFLASH_PROT_ROW15

Per Page Write Protection

Address: 0x0FFFF00F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.17 SFLASH_PROT_ROW16

Per Page Write Protection

Address: 0x0FFFF010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.18 SFLASH_PROT_ROW17

Per Page Write Protection

Address: 0x0FFFF011

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.19 SFLASH_PROT_ROW18

Per Page Write Protection

Address: 0x0FFFF012

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.20 SFLASH_PROT_ROW19

Per Page Write Protection

Address: 0x0FFFF013

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.21 SFLASH_PROT_ROW20

Per Page Write Protection

Address: 0x0FFFF014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.22 SFLASH_PROT_ROW21

Per Page Write Protection

Address: 0x0FFFF015

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.23 SFLASH_PROT_ROW22

Per Page Write Protection

Address: 0x0FFFF016

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.24 SFLASH_PROT_ROW23

Per Page Write Protection

Address: 0x0FFFF017

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.25 SFLASH_PROT_ROW24

Per Page Write Protection

Address: 0x0FFFF018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.26 SFLASH_PROT_ROW25

Per Page Write Protection

Address: 0x0FFFF019

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.27 SFLASH_PROT_ROW26

Per Page Write Protection

Address: 0x0FFFF01A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.28 SFLASH_PROT_ROW27

Per Page Write Protection

Address: 0x0FFFF01B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.29 SFLASH_PROT_ROW28

Per Page Write Protection

Address: 0x0FFFF01C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.30 SFLASH_PROT_ROW29

Per Page Write Protection

Address: 0x0FFFF01D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.31 SFLASH_PROT_ROW30

Per Page Write Protection

Address: 0x0FFFF01E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.32 SFLASH_PROT_ROW31

Per Page Write Protection

Address: 0x0FFFF01F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.33 SFLASH_PROT_ROW32

Per Page Write Protection

Address: 0x0FFFF020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.34 SFLASH_PROT_ROW33

Per Page Write Protection

Address: 0x0FFFF021

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.35 SFLASH_PROT_ROW34

Per Page Write Protection

Address: 0x0FFFF022

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.36 SFLASH_PROT_ROW35

Per Page Write Protection

Address: 0x0FFFF023

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.37 SFLASH_PROT_ROW36

Per Page Write Protection

Address: 0x0FFFF024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.38 SFLASH_PROT_ROW37

Per Page Write Protection

Address: 0x0FFFF025

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.39 SFLASH_PROT_ROW38

Per Page Write Protection

Address: 0x0FFFF026

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.40 SFLASH_PROT_ROW39

Per Page Write Protection

Address: 0x0FFFF027

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.41 SFLASH_PROT_ROW40

Per Page Write Protection

Address: 0x0FFFF028

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.42 SFLASH_PROT_ROW41

Per Page Write Protection

Address: 0x0FFFF029

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.43 SFLASH_PROT_ROW42

Per Page Write Protection

Address: 0x0FFFF02A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.44 SFLASH_PROT_ROW43

Per Page Write Protection

Address: 0x0FFFF02B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.45 SFLASH_PROT_ROW44

Per Page Write Protection

Address: 0x0FFFF02C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.46 SFLASH_PROT_ROW45

Per Page Write Protection

Address: 0x0FFFF02D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.47 SFLASH_PROT_ROW46

Per Page Write Protection

Address: 0x0FFFF02E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.48 SFLASH_PROT_ROW47

Per Page Write Protection

Address: 0x0FFFF02F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.49 SFLASH_PROT_ROW48

Per Page Write Protection

Address: 0x0FFFF030

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.50 SFLASH_PROT_ROW49

Per Page Write Protection

Address: 0x0FFFF031

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.51 SFLASH_PROT_ROW50

Per Page Write Protection

Address: 0x0FFFF032

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.52 SFLASH_PROT_ROW51

Per Page Write Protection

Address: 0x0FFFF033

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.53 SFLASH_PROT_ROW52

Per Page Write Protection

Address: 0x0FFFF034

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.54 SFLASH_PROT_ROW53

Per Page Write Protection

Address: 0x0FFFF035

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.55 SFLASH_PROT_ROW54

Per Page Write Protection

Address: 0x0FFFF036

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.56 SFLASH_PROT_ROW55

Per Page Write Protection

Address: 0x0FFFF037

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.57 SFLASH_PROT_ROW56

Per Page Write Protection

Address: 0x0FFFF038

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.58 SFLASH_PROT_ROW57

Per Page Write Protection

Address: 0x0FFFF039

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.59 SFLASH_PROT_ROW58

Per Page Write Protection

Address: 0x0FFFF03A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.60 SFLASH_PROT_ROW59

Per Page Write Protection

Address: 0x0FFFF03B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.61 SFLASH_PROT_ROW60

Per Page Write Protection

Address: 0x0FFFF03C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.62 SFLASH_PROT_ROW61

Per Page Write Protection

Address: 0x0FFFF03D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.63 SFLASH_PROT_ROW62

Per Page Write Protection

Address: 0x0FFFF03E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.64 SFLASH_PROT_ROW63

Per Page Write Protection

Address: 0x0FFFF03F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.65 SFLASH_PROT_PROTECTION

Protection Level

Address: 0x0FFFF0FF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	
HW Access	None						None	
Name	None [7:2]						PROT_LEVEL [1:0]	

Bits	Name	Description
1 : 0	PROT_LEVEL	Current Protection Mode - note that encoding is different from CPUSS_PROTECTION !! Default Value: X **0x0: OPEN:** System is in OPEN mode **0x1: VIRGIN:** System is in VIRGIN mode **0x2: PROTECTED:** System is in PROTECTED mode **0x3: KILL:** System is in KILL mode

30.1.66 SFLASH_AV_PAIRS_8B0

8b Addr/Value pair Section

Address: 0x0FFFF100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.67 SFLASH_AV_PAIRS_8B1

8b Addr/Value pair Section

Address: 0x0FFFF101

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.68 SFLASH_AV_PAIRS_8B2

8b Addr/Value pair Section

Address: 0x0FFFF102

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.69 SFLASH_AV_PAIRS_8B3

8b Addr/Value pair Section

Address: 0x0FFFF103

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.70 SFLASH_AV_PAIRS_8B4

8b Addr/Value pair Section

Address: 0x0FFFF104

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.71 SFLASH_AV_PAIRS_8B5

8b Addr/Value pair Section

Address: 0x0FFFF105

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.72 SFLASH_AV_PAIRS_8B6

8b Addr/Value pair Section

Address: 0x0FFFF106

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.73 SFLASH_AV_PAIRS_8B7

8b Addr/Value pair Section

Address: 0x0FFFF107

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.74 SFLASH_AV_PAIRS_8B8

8b Addr/Value pair Section

Address: 0x0FFFF108

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.75 SFLASH_AV_PAIRS_8B9

8b Addr/Value pair Section

Address: 0x0FFFF109

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.76 SFLASH_AV_PAIRS_8B10

8b Addr/Value pair Section

Address: 0x0FFFF10A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.77 SFLASH_AV_PAIRS_8B11

8b Addr/Value pair Section

Address: 0x0FFFF10B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.78 SFLASH_AV_PAIRS_8B12

8b Addr/Value pair Section

Address: 0x0FFFF10C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.79 SFLASH_AV_PAIRS_8B13

8b Addr/Value pair Section

Address: 0x0FFFF10D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.80 SFLASH_AV_PAIRS_8B14

8b Addr/Value pair Section

Address: 0x0FFFF10E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.81 SFLASH_AV_PAIRS_8B15

8b Addr/Value pair Section

Address: 0x0FFFF10F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.82 SFLASH_AV_PAIRS_8B16

8b Addr/Value pair Section

Address: 0x0FFFF110

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.83 SFLASH_AV_PAIRS_8B17

8b Addr/Value pair Section

Address: 0x0FFFF111

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.84 SFLASH_AV_PAIRS_8B18

8b Addr/Value pair Section

Address: 0x0FFFF112

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.85 SFLASH_AV_PAIRS_8B19

8b Addr/Value pair Section

Address: 0x0FFFF113

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.86 SFLASH_AV_PAIRS_8B20

8b Addr/Value pair Section

Address: 0x0FFFF114

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.87 SFLASH_AV_PAIRS_8B21

8b Addr/Value pair Section

Address: 0x0FFFF115

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.88 SFLASH_AV_PAIRS_8B22

8b Addr/Value pair Section

Address: 0x0FFFF116

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.89 SFLASH_AV_PAIRS_8B23

8b Addr/Value pair Section

Address: 0x0FFFF117

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.90 SFLASH_AV_PAIRS_8B24

8b Addr/Value pair Section

Address: 0x0FFFF118

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.91 SFLASH_AV_PAIRS_8B25

8b Addr/Value pair Section

Address: 0x0FFFF119

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.92 SFLASH_AV_PAIRS_8B26

8b Addr/Value pair Section

Address: 0x0FFFF11A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.93 SFLASH_AV_PAIRS_8B27

8b Addr/Value pair Section

Address: 0x0FFFF11B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.94 SFLASH_AV_PAIRS_8B28

8b Addr/Value pair Section

Address: 0x0FFFF11C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.95 SFLASH_AV_PAIRS_8B29

8b Addr/Value pair Section

Address: 0x0FFFF11D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.96 SFLASH_AV_PAIRS_8B30

8b Addr/Value pair Section

Address: 0x0FFFF11E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.97 SFLASH_AV_PAIRS_8B31

8b Addr/Value pair Section

Address: 0x0FFFF11F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.98 SFLASH_AV_PAIRS_8B32

8b Addr/Value pair Section

Address: 0x0FFFF120

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.99 SFLASH_AV_PAIRS_8B33

8b Addr/Value pair Section

Address: 0x0FFFF121

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.100 SFLASH_AV_PAIRS_8B34

8b Addr/Value pair Section

Address: 0x0FFFF122

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.101 SFLASH_AV_PAIRS_8B35

8b Addr/Value pair Section

Address: 0x0FFFF123

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.102 SFLASH_AV_PAIRS_8B36

8b Addr/Value pair Section

Address: 0x0FFFF124

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.103 SFLASH_AV_PAIRS_8B37

8b Addr/Value pair Section

Address: 0x0FFFF125

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.104 SFLASH_AV_PAIRS_8B38

8b Addr/Value pair Section

Address: 0x0FFFF126

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.105 SFLASH_AV_PAIRS_8B39

8b Addr/Value pair Section

Address: 0x0FFFF127

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.106 SFLASH_AV_PAIRS_8B40

8b Addr/Value pair Section

Address: 0x0FFFF128

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.107 SFLASH_AV_PAIRS_8B41

8b Addr/Value pair Section

Address: 0x0FFFF129

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.108 SFLASH_AV_PAIRS_8B42

8b Addr/Value pair Section

Address: 0x0FFFF12A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.109 SFLASH_AV_PAIRS_8B43

8b Addr/Value pair Section

Address: 0x0FFFF12B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.110 SFLASH_AV_PAIRS_8B44

8b Addr/Value pair Section

Address: 0x0FFFF12C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.111 SFLASH_AV_PAIRS_8B45

8b Addr/Value pair Section

Address: 0x0FFFF12D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.112 SFLASH_AV_PAIRS_8B46

8b Addr/Value pair Section

Address: 0x0FFFF12E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.113 SFLASH_AV_PAIRS_8B47

8b Addr/Value pair Section

Address: 0x0FFFF12F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.114 SFLASH_AV_PAIRS_8B48

8b Addr/Value pair Section

Address: 0x0FFFF130

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.115 SFLASH_AV_PAIRS_8B49

8b Addr/Value pair Section

Address: 0x0FFFF131

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.116 SFLASH_AV_PAIRS_8B50

8b Addr/Value pair Section

Address: 0x0FFFF132

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.117 SFLASH_AV_PAIRS_8B51

8b Addr/Value pair Section

Address: 0x0FFFF133

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.118 SFLASH_AV_PAIRS_8B52

8b Addr/Value pair Section

Address: 0x0FFFF134

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.119 SFLASH_AV_PAIRS_8B53

8b Addr/Value pair Section

Address: 0x0FFFF135

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.120 SFLASH_AV_PAIRS_8B54

8b Addr/Value pair Section

Address: 0x0FFFF136

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.121 SFLASH_AV_PAIRS_8B55

8b Addr/Value pair Section

Address: 0x0FFFF137

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.122 SFLASH_AV_PAIRS_8B56

8b Addr/Value pair Section

Address: 0x0FFFF138

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.123 SFLASH_AV_PAIRS_8B57

8b Addr/Value pair Section

Address: 0x0FFFF139

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.124 SFLASH_AV_PAIRS_8B58

8b Addr/Value pair Section

Address: 0x0FFFF13A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.125 SFLASH_AV_PAIRS_8B59

8b Addr/Value pair Section

Address: 0x0FFFF13B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.126 SFLASH_AV_PAIRS_8B60

8b Addr/Value pair Section

Address: 0x0FFFF13C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.127 SFLASH_AV_PAIRS_8B61

8b Addr/Value pair Section

Address: 0x0FFFF13D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.128 SFLASH_AV_PAIRS_8B62

8b Addr/Value pair Section

Address: 0x0FFFF13E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.129 SFLASH_AV_PAIRS_8B63

8b Addr/Value pair Section

Address: 0x0FFFF13F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.130 SFLASH_AV_PAIRS_8B64

8b Addr/Value pair Section

Address: 0x0FFFF140

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.131 SFLASH_AV_PAIRS_8B65

8b Addr/Value pair Section

Address: 0x0FFFF141

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.132 SFLASH_AV_PAIRS_8B66

8b Addr/Value pair Section

Address: 0x0FFFF142

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.133 SFLASH_AV_PAIRS_8B67

8b Addr/Value pair Section

Address: 0x0FFFF143

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.134 SFLASH_AV_PAIRS_8B68

8b Addr/Value pair Section

Address: 0x0FFFF144

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.135 SFLASH_AV_PAIRS_8B69

8b Addr/Value pair Section

Address: 0x0FFFF145

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.136 SFLASH_AV_PAIRS_8B70

8b Addr/Value pair Section

Address: 0x0FFFF146

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.137 SFLASH_AV_PAIRS_8B71

8b Addr/Value pair Section

Address: 0x0FFFF147

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.138 SFLASH_AV_PAIRS_8B72

8b Addr/Value pair Section

Address: 0x0FFFF148

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.139 SFLASH_AV_PAIRS_8B73

8b Addr/Value pair Section

Address: 0x0FFFF149

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.140 SFLASH_AV_PAIRS_8B74

8b Addr/Value pair Section

Address: 0x0FFFF14A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.141 SFLASH_AV_PAIRS_8B75

8b Addr/Value pair Section

Address: 0x0FFFF14B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.142 SFLASH_AV_PAIRS_8B76

8b Addr/Value pair Section

Address: 0x0FFFF14C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.143 SFLASH_AV_PAIRS_8B77

8b Addr/Value pair Section

Address: 0x0FFFF14D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.144 SFLASH_AV_PAIRS_8B78

8b Addr/Value pair Section

Address: 0x0FFFF14E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.145 SFLASH_AV_PAIRS_8B79

8b Addr/Value pair Section

Address: 0x0FFFF14F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.146 SFLASH_AV_PAIRS_8B80

8b Addr/Value pair Section

Address: 0x0FFFF150

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.147 SFLASH_AV_PAIRS_8B81

8b Addr/Value pair Section

Address: 0x0FFFF151

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.148 SFLASH_AV_PAIRS_8B82

8b Addr/Value pair Section

Address: 0x0FFFF152

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.149 SFLASH_AV_PAIRS_8B83

8b Addr/Value pair Section

Address: 0x0FFFF153

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.150 SFLASH_AV_PAIRS_8B84

8b Addr/Value pair Section

Address: 0x0FFFF154

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.151 SFLASH_AV_PAIRS_8B85

8b Addr/Value pair Section

Address: 0x0FFFF155

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.152 SFLASH_AV_PAIRS_8B86

8b Addr/Value pair Section

Address: 0x0FFFF156

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.153 SFLASH_AV_PAIRS_8B87

8b Addr/Value pair Section

Address: 0x0FFFF157

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.154 SFLASH_BLESS_BB_BUMP2

BLESS Bump bit for LDO BB, TXRX

Address: 0x0FFFF158

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW			RW				
HW Access	R			R				
Name	V2I [7:5]			V2I_RCAL [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW			RW	
HW Access	R			R			R	
Name	SY_IBIAS [15:13]			VBG_TRIM [12:10]			V2I [9:8]	

Bits	Name	Description
15 : 13	SY_IBIAS	3'b1xx: RCAL current bumped 3'b0xx: BG current bumped. 2'bxx: reperesent current bump 01: +12.5%, 00: 0%, 11: -12.5%, 10:-25% Default Value: 0
12 : 10	VBG_TRIM	3d0: Trims the Bandgap voltage by 0% 3d1: Trims the Bandgap voltage by 1.6% 3d2: Trims the Bandgap voltage by 3.2% 3d3: Trims the Bandgap voltage by 4.8% 3d4: Trims the Bandgap voltage by 6.4% 3d5: Trims the Bandgap voltage by -4.8% 3d6: Trims the Bandgap voltage by -3.2% 3d7: Trims the Bandgap voltage by -1.6% Default Value: 0

(continued)

9 : 5	V2I	Bit[9] 1: Error amp quiescent current is 5u 0: Error amp quiescent current is 10u Bit[8:5] 4d0: Trims the BGR current by 0% 4d1: Trims the BGR current by -2.5% 4d2: Trims the BGR current by -5% 4d3: Trims the BGR current by -7.5% 4d4: Trims the BGR current by -10% 4d5: Trims the BGR current by -12.5% 4d6: Trims the BGR current by -15% 4d7: Trims the BGR current by -17.5% 4d8: Trims the BGR current by 20% 4d9: Trims the BGR current by 17.5% 4d10: Trims the BGR current by 15% 4d11: Trims the BGR current by 12.5% 4d12: Trims the BGR current by 10% 4d13: Trims the BGR current by 7.5% 4d14: Trims the BGR current by 5% 4d15: Trims the BGR current by 2.5% Default Value: 0
4 : 0	V2I_RCAL	Bit[4] 1: Error amp quiescent current is 5u 0: Error amp quiescent current is 10u Bit[3:0] 4d0: Trims the RCAL current by 0% 4d1: Trims the RCAL current by -2.5% 4d2: Trims the RCAL current by -5% 4d3: Trims the RCAL current by -7.5% 4d4: Trims the RCAL current by -10% Default Value: 0

30.1.155 SFLASH_AV_PAIRS_8B88

8b Addr/Value pair Section

Address: 0x0FFFF158

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.156 SFLASH_AV_PAIRS_8B89

8b Addr/Value pair Section

Address: 0x0FFFF159

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.157 SFLASH_BLESS_BB_XO

BLESS bump configuration 1

Address: 0x0FFFF15A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW		RW	RW	RW	RW	RW
HW Access	R	R		R	R	R	R	R
Name	CTRL_VDDL_XO	CTRL_RC_FASTSTART_RES [6:5]		EN_AMPDET_FASTSTART	EN_AMPDET_CURMEAS	EN_CURMEAS	EN_RE_FASTSTART	DIS_XOCORE_SUPFILT

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW		RW			RW	
HW Access	R	R		R			R	
Name	rev_bb_xo	CTRL_RPREF [14:13]		CTRL_VDDL_XB [12:10]			CTRL_VDDL_XO [9:8]	

Bits	Name	Description
15	rev_bb_xo	reserved for feature Default Value: 0
14 : 13	CTRL_RPREF	Controls the reference voltage fed as input to the regulators which generate vdd_xo and vdd_xb. 2d0 : 1.289V 2d0 : 1.227V 2d0 : 1.164V 2d0 : 1.382V Default Value: 0
12 : 10	CTRL_VDDL_XB	Controls the value of supply filter resistance in the inverter chain. This in turn controls the supply voltage at which the inverter chain runs. 3d0 : 1.028k 3d0 : 1.172k 3d0 : 1.367k 3d0 : 1.540k 3d0 : 1.889k 3d0 : 2.055k 3d0 : 0.503k 3d0 : 0.747k Default Value: 0
9 : 7	CTRL_VDDL_XO	Controls the value of supply filter resistance in the xo core. This in turn controls the supply voltage at which the core runs. 3d0 : 0.769k 3d0 : 0.877k 3d0 : 1.023k 3d0 : 1.152k 3d0 : 1.413k 3d0 : 1.537k 3d0 : 0.376k 3d0 : 0.559k Default Value: 0

(continued)

6 : 5	CTRL_RC_FASTSTART_RES	Controls the time constant with which the surge current from rc_faststart block decays down to zero. 2d0 : 387us 2d1 : 309us 2d2 : 232us 2d3 : 464us Default Value: 0
4	EN_AMPDET_FASTSTART	This bit is used to force startup of the vtnbyr circuit in the biasgen_and_reg block of the XO. 1d1 : startup forced 1d0 : Normal startup Default Value: 0
3	EN_AMPDET_CURMEAS	This bit can be used to disable all the caps on both X1 node and X2 node. 1d0 : Caps Enabled 1d1 : Caps disabled. Even when all the caps are disabled, due to finite on/off ratio of the caps, the cap on both X1 and X2 node is still 3.69pF Default Value: 0
2	EN_CURMEAS	This bit is used to force startup of the positive feedback loop in the amplitude detect block of the XO. 1d1 : startup forced 1d0 : Normal startup Default Value: 0
1	EN_RE_FASTSTART	Enables/Disables the RC faststart block in the XO. When enabled, this block provides a surge current at xo startup to reduce the settling time of the XO. 1: RC Fast start in XO is enabled 0: RC Fast start in XO is disabled Default Value: 0
0	DIS_XOCORE_SUPFILT	Enables/Disables the supply filter of the XO core. 1: Disabled 0: Enabled Default Value: 0

30.1.158 SFLASH_AV_PAIRS_8B90

8b Addr/Value pair Section

Address: 0x0FFFF15A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.159 SFLASH_AV_PAIRS_8B91

8b Addr/Value pair Section

Address: 0x0FFFF15B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.160 SFLASH_BLESS_SY_BUMP1

BLESS SY bump bits configuration 1

Address: 0x0FFFF15C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW		RW	RW			
HW Access	R	R		R	R			
Name	LDOLO_FORCE_STARTUP	IBIAS_LOPATH [6:5]		LOFB_POWERSAVE	VCO [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	PDCPLPF [15:12]				LOPATH [11:8]			

Bits	Name	Description
15 : 12	PDCPLPF	Bump for PD CP and LPF blocks.[2:0] is used to get range of -20%to +15% in 5% steps. ICP_BUMP[2:0] ICP 1 0 0 -20% 1 0 1 -15% 1 1 0 -10% 1 1 1 -05% 0 0 0 00% 0 0 1 05% 0 1 0 10% 0 1 1 15%. Default Value: 0
11 : 8	LOPATH	Bump bits for LO path bulk bias. Goes to DIVN/FCAL/LOPATH for bumps. 2 bits for pBulk [3:2] and 2 bits for nBulk[1:0]. bump pbulk 0 0 vddx-380mV 0 1 vddx-320mV 1 0 vddx-440mV 1 1 vddx Default Value: 5
7	LDOLO_FORCE_STARTUP	1: force start-up of the VT/R circuit in VCOLOPATH LCO 0: no force start-up Default Value: 0
6 : 5	IBIAS_LOPATH	bump bits for clkbias in lopath bump clk bias pM clk bias nM 0 0 vddo-vgsp vgsn 0 1 vddlo-vgsp-100m vgsn+100m 1 0 vddlo-vgsp-200m vgsn+200m 1 1 vddlo-vgsp-400m vgsn+400m Default Value: 0

(continued)

4	LOFB_POWERSAVE	1: enable powersave for LOFB buffer 0: disable powersave for LOFB buffer Default Value: 0
3 : 0	VCO	Bump bits for SY VCO block. Rt VCO (2 bits) - sy_bump1_vco [3:2] 00 ~ 50 Ohms 01 ~ 30 Ohms 10 ~ 22 Ohms 11 ~ 16 Ohms and Rb VCO (2 bits) - sy_bump1_vco[1:0] 00 ~ 58 Ohms 01 ~ 39 Ohms 10 ~ 22 Ohms 11 ~ 16 Ohms Default Value: 5

30.1.161 SFLASH_AV_PAIRS_8B92

8b Addr/Value pair Section

Address: 0x0FFFF15C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.162 SFLASH_AV_PAIRS_8B93

8b Addr/Value pair Section

Address: 0x0FFFF15D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.163 SFLASH_BLESS_LDO

BLESS bump bit for LDO

Address: 0x0FFFF15E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW		RW		RW		
HW Access	R	R		R		R		
Name	BUMP_SY_LHV	BUMP_SY_LOPATH [6:5]		BUMP_SY_VCO [4:3]		BUMP_BALUM_HF [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			RW
HW Access	R				R			R
Name	REV_LDO [15:12]				BUMP_SY_FFFB [11:9]			BUMP_SY_LHV

Bits	Name	Description
15 : 12	REV_LDO	received for feature Default Value: 0
11 : 9	BUMP_SY_FFFB	3d0: FF and FB LDO outputs are 1.800V 3d1: FF and FB LDO outputs are 1.846V 3d2: FF and FB LDO outputs are 1.894V 3d3: FF and FB LDO outputs are 1.946V 3d4: FF and FB LDO outputs are 2.000V 3d5: FF and FB LDO outputs are 1.649V 3d6: FF and FB LDO outputs are 1.701V 3d7: FF and FB LDO outputs are 1.756V Default Value: 0
8 : 7	BUMP_SY_LHV	2d0: HV LDO outputs are 1.894V 2d1: HV LDO outputs are 2.000V 2d2: HV LDO outputs are 1.800V 2d3: HV LDO outputs are 1.846V Default Value: 0
6 : 5	BUMP_SY_LOPATH	2d0: LOPATH LDO outputs are 1.762V 2d1: LOPATH LDO outputs are 1.861V 2d2: LOPATH LDO outputs are 1.673V 2d3: LOPATH LDO outputs are 1.716V Default Value: 0
4 : 3	BUMP_SY_VCO	2d0: VCO LDO outputs are 1.413V 2d1: VCO LDO outputs are 1.494V 2d2: VCO LDO outputs are 1.329V 2d3: VCO LDO outputs are 1.371V Default Value: 0

(continued)

2 : 0	BUMP_BALUM_HF	3d0: HF LDO output is 1.800V 3d1: HF LDO output is 1.846V 3d2: HF LDO output is 1.894V 3d3: HF LDO output is 1.946V Default Value: 0

30.1.164 SFLASH_AV_PAIRS_8B94

8b Addr/Value pair Section

Address: 0x0FFFF15E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.165 SFLASH_AV_PAIRS_8B95

8b Addr/Value pair Section

Address: 0x0FFFF15F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.166 SFLASH_AV_PAIRS_8B96

8b Addr/Value pair Section

Address: 0x0FFFF160

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.167 SFLASH_AV_PAIRS_8B97

8b Addr/Value pair Section

Address: 0x0FFFF161

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.168 SFLASH_AV_PAIRS_8B98

8b Addr/Value pair Section

Address: 0x0FFFF162

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.169 SFLASH_AV_PAIRS_8B99

8b Addr/Value pair Section

Address: 0x0FFFF163

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.170 SFLASH_AV_PAIRS_8B100

8b Addr/Value pair Section

Address: 0x0FFFF164

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.171 SFLASH_AV_PAIRS_8B101

8b Addr/Value pair Section

Address: 0x0FFFF165

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.172 SFLASH_AV_PAIRS_8B102

8b Addr/Value pair Section

Address: 0x0FFFF166

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.173 SFLASH_AV_PAIRS_8B103

8b Addr/Value pair Section

Address: 0x0FFFF167

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.174 SFLASH_AV_PAIRS_8B104

8b Addr/Value pair Section

Address: 0x0FFFF168

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.175 SFLASH_AV_PAIRS_8B105

8b Addr/Value pair Section

Address: 0x0FFFF169

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.176 SFLASH_AV_PAIRS_8B106

8b Addr/Value pair Section

Address: 0x0FFFF16A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.177 SFLASH_AV_PAIRS_8B107

8b Addr/Value pair Section

Address: 0x0FFFF16B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.178 SFLASH_AV_PAIRS_8B108

8b Addr/Value pair Section

Address: 0x0FFFF16C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.179 SFLASH_AV_PAIRS_8B109

8b Addr/Value pair Section

Address: 0x0FFFF16D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.180 SFLASH_AV_PAIRS_8B110

8b Addr/Value pair Section

Address: 0x0FFFF16E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.181 SFLASH_AV_PAIRS_8B111

8b Addr/Value pair Section

Address: 0x0FFFF16F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.182 SFLASH_AV_PAIRS_8B112

8b Addr/Value pair Section

Address: 0x0FFFF170

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.183 SFLASH_AV_PAIRS_8B113

8b Addr/Value pair Section

Address: 0x0FFFF171

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.184 SFLASH_AV_PAIRS_8B114

8b Addr/Value pair Section

Address: 0x0FFFF172

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.185 SFLASH_AV_PAIRS_8B115

8b Addr/Value pair Section

Address: 0x0FFFF173

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.186 SFLASH_AV_PAIRS_8B116

8b Addr/Value pair Section

Address: 0x0FFFF174

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.187 SFLASH_AV_PAIRS_8B117

8b Addr/Value pair Section

Address: 0x0FFFF175

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.188 SFLASH_AV_PAIRS_8B118

8b Addr/Value pair Section

Address: 0x0FFFF176

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.189 SFLASH_AV_PAIRS_8B119

8b Addr/Value pair Section

Address: 0x0FFFF177

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.190 SFLASH_AV_PAIRS_8B120

8b Addr/Value pair Section

Address: 0x0FFFF178

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.191 SFLASH_AV_PAIRS_8B121

8b Addr/Value pair Section

Address: 0x0FFFF179

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.192 SFLASH_AV_PAIRS_8B122

8b Addr/Value pair Section

Address: 0x0FFFF17A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.193 SFLASH_AV_PAIRS_8B123

8b Addr/Value pair Section

Address: 0x0FFFF17B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.194 SFLASH_AV_PAIRS_8B124

8b Addr/Value pair Section

Address: 0x0FFFF17C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.195 SFLASH_AV_PAIRS_8B125

8b Addr/Value pair Section

Address: 0x0FFFF17D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.196 SFLASH_AV_PAIRS_8B126

8b Addr/Value pair Section

Address: 0x0FFFF17E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.197 SFLASH_AV_PAIRS_8B127

8b Addr/Value pair Section

Address: 0x0FFFF17F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Address or Value Byte Default Value: X

30.1.198 SFLASH_AV_PAIRS_32B0

32b Addr/Value pair Section

Address: 0x0FFFF200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Address or Value Word Default Value: X

30.1.199 SFLASH_AV_PAIRS_32B1

32b Addr/Value pair Section

Address: 0x0FFFF204

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Address or Value Word Default Value: X

30.1.200 SFLASH_AV_PAIRS_32B2

32b Addr/Value pair Section

Address: 0x0FFFF208

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Address or Value Word Default Value: X

30.1.201 SFLASH_AV_PAIRS_32B3

32b Addr/Value pair Section

Address: 0x0FFFF20C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Address or Value Word Default Value: X

30.1.202 SFLASH_AV_PAIRS_32B4

32b Addr/Value pair Section

Address: 0x0FFFF210

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Address or Value Word Default Value: X

30.1.203 SFLASH_AV_PAIRS_32B5

32b Addr/Value pair Section

Address: 0x0FFFF214

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Address or Value Word Default Value: X

30.1.204 SFLASH_AV_PAIRS_32B6

32b Addr/Value pair Section

Address: 0x0FFFF218

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Address or Value Word Default Value: X

30.1.205 SFLASH_AV_PAIRS_32B7

32b Addr/Value pair Section

Address: 0x0FFFF21C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Address or Value Word Default Value: X

30.1.206 SFLASH_AV_PAIRS_32B8

32b Addr/Value pair Section

Address: 0x0FFFF220

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Address or Value Word Default Value: X

30.1.207 SFLASH_AV_PAIRS_32B9

32b Addr/Value pair Section

Address: 0x0FFFF224

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Address or Value Word Default Value: X

30.1.208 SFLASH_AV_PAIRS_32B10

32b Addr/Value pair Section

Address: 0x0FFFF228

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Address or Value Word Default Value: X

30.1.209 SFLASH_AV_PAIRS_32B11

32b Addr/Value pair Section

Address: 0x0FFFF22C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Address or Value Word Default Value: X

30.1.210 SFLASH_AV_PAIRS_32B12

32b Addr/Value pair Section

Address: 0x0FFFF230

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Address or Value Word Default Value: X

30.1.211 SFLASH_AV_PAIRS_32B13

32b Addr/Value pair Section

Address: 0x0FFFF234

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Address or Value Word Default Value: X

30.1.212 SFLASH_AV_PAIRS_32B14

32b Addr/Value pair Section

Address: 0x0FFFF238

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Address or Value Word Default Value: X

30.1.213 SFLASH_AV_PAIRS_32B15

32b Addr/Value pair Section

Address: 0x0FFFF23C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Address or Value Word Default Value: X

30.1.214 SFLASH_CPUSS_WOUNDING

CPUSS Wounding Register

Address: 0x0FFFF240

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Data to use for register Default Value: X

30.1.215 SFLASH_SILICON_ID

Silicon ID

Address: 0x0FFFF244

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	ID [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	ID	Silicon ID Default Value: X

30.1.216 SFLASH_CPUSS_PRIV_RAM

RAM Privileged Limit

Address: 0x0FFFF248

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	RAM_PROT_LIMIT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							RAM_PROT_LIMIT

Bits	Name	Description
8 : 0	RAM_PROT_LIMIT	Indicates the limit where the privileged area of SRAM starts in increments of 256 Bytes. "0": Entire SRAM is Privileged. "1": First 256 Bytes are User accessable. Any number larger than the size of the SRAM indicates that the entire SRAM is user mode accessible. Default Value: 0

30.1.217 SFLASH_CPUSS_PRIV_ROM_BROM

Boot ROM Privileged Limit

Address: 0x0FFFF24A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	BROM_PROT_LIMIT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 0	BROM_PROT_LIMIT	Indicates the limit where the privileged area of the Boot ROM partition starts in increments of 256 Bytes. "0": Entire Boot ROM is Privileged. "1": First 256 Bytes are User accessable. ... BROM_PROT_LIMIT >= "Boot ROM partition capacity": Entire Boot ROM partition is user mode accessible. Default Value: 0

30.1.218 SFLASH_CPUSS_PRIV_FLASH

Flash Privileged Limit

Address: 0x0FFFF24C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	FLASH_PROT_LIMIT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW		
HW Access	None					R		
Name	None [15:11]					FLASH_PROT_LIMIT [10:8]		

Bits	Name	Description
10 : 0	FLASH_PROT_LIMIT	Indicates the limit where the privileged area of flash starts in increments of 256 Bytes. "0": Entire flash is Privileged. "1": First 256 Bytes are User accessable. Any number larger than the size of the flash indicates that the entire flash is user mode accessible. Note that SuperVisory rows are always User accessable. If FLASH_PROT_LIMIT defines a non-empty privileged area, the boot ROM will assume that a system call table exists at the beginning of the Flash privileged area and use it for all SystemCalls made using SYSREQ. Default Value: 0

30.1.219 SFLASH_CPUSS_PRIV_ROM_SROM

System ROM Privileged Limit

Address: 0x0FFFF24E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SROM_PROT_LIMIT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						SROM_PROT_LIMIT [9:8]	

Bits	Name	Description
9 : 0	SROM_PROT_LIMIT	Indicates the limit where the privileged area of System ROM partition starts in increments of 256 Bytes. The limit is wrt. the start of the ROM memory (start of the Boot ROM partition). SROM_PROT_LIMIT * 256 Byte <= "Boot ROM partition capacity": Entire System ROM is Privileged. SROM_PROT_LIMIT * 256 Byte > "Boot ROM partition capacity": First SROM_PROT_LIMIT * 256 - "Boot ROM partition capacity" Bytes are User accessable. ... SROM_PROT_LIMIT >= "ROM capacity": Entire System ROM is user mode accessible. Default Value: 0

30.1.220 SFLASH_HIB_KEY_DELAY

Hibernate wakeup value for PWR_KEY_DELAY

Address: 0x0FFFF250

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	WAKEUP_HOLDOFF [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						WAKEUP_HOLDOFF [9:8]	

Bits	Name	Description
9 : 0	WAKEUP_HOLDOFF	Delay (in 12MHz IMO clock cycles) to wait for references to settle on wakeup from hibernate/ deepsleep. PBOD is ignored and system does not resume until this delay expires. Note that the same delay on POR is hard-coded. Default Value: X

30.1.221 SFLASH_DPSLP_KEY_DELAY

DeepSleep wakeup value for PWR_KEY_DELAY

Address: 0x0FFFF252

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	WAKEUP_HOLDOFF [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						WAKEUP_HOLDOFF [9:8]	

Bits	Name	Description
9 : 0	WAKEUP_HOLDOFF	Delay (in 12MHz IMO clock cycles) to wait for references to settle on wakeup from hibernate/ deepsleep. PBOD is ignored and system does not resume until this delay expires. Note that the same delay on POR is hard-coded. Default Value: X

30.1.222 SFLASH_SWD_CONFIG

SWD pinout selector (not present in TSG4/TSG5-M)

Address: 0x0FFFF254

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							None
Name	None [7:1]							SWD_SELECT

Bits	Name	Description
0	SWD_SELECT	0: Use Primary SWD location 1: Use Alternate SWD location Default Value: X

30.1.223 SFLASH_INITIAL_SPCIF_TRIM_M1_DAC0

FLASH IDAC trim used during boot

Address: 0x0FFFF255

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW			RW				
HW Access	R			R				
Name	SLOPE [7:5]			IDAC [4:0]				

Bits	Name	Description
7 : 5	SLOPE	See SPCIF_TRIM1 Default Value: 0
4 : 0	IDAC	See SPCIF_TRIM1 Default Value: 0

30.1.224 SFLASH_SWD_LISTEN

Listen Window Length

Address: 0x0FFFF258

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	CYCLES [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	CYCLES [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	CYCLES [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	CYCLES [31:24]							

Bits	Name	Description
31 : 0	CYCLES	Number of clock cycles Default Value: X

30.1.225 SFLASH_FLASH_START

Flash Image Start Address

Address: 0x0FFFF25C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	ADDRESS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	ADDRESS [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	ADDRESS [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	None							
Name	ADDRESS [31:24]							

Bits	Name	Description
31 : 0	ADDRESS	Start Address Default Value: X

30.1.226 SFLASH_CSD_TRIM1_HVIDAC

CSD Trim Data for HVIDAC operation

Address: 0x0FFFF260

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	TRIM8 [7:0]							

Bits	Name	Description
7 : 0	TRIM8	Trim data Default Value: X

30.1.227 SFLASH_CSD_TRIM2_HVIDAC

CSD Trim Data for HVIDAC operation

Address: 0x0FFFF261

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	TRIM8 [7:0]							

Bits	Name	Description
7 : 0	TRIM8	Trim data Default Value: X

30.1.228 SFLASH_CSD_TRIM1_CSD

CSD Trim Data for (normal) CSD operation

Address: 0x0FFFF262

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	TRIM8 [7:0]							

Bits	Name	Description
7 : 0	TRIM8	Trim data Default Value: X

30.1.229 SFLASH_CSD_TRIM2_CSD

CSD Trim Data for (normal) CSD operation

Address: 0x0FFFF263

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	TRIM8 [7:0]							

Bits	Name	Description
7 : 0	TRIM8	Trim data Default Value: X

30.1.230 SFLASH_SAR_TEMP_MULTIPLIER

SAR Temperature Sensor Multiplication Factor

Address: 0x0FFFF264

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	TEMP_MULTIPLIER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	TEMP_MULTIPLIER [15:8]							

Bits	Name	Description
15 : 0	TEMP_MULTIPLIER	Multiplier value for SAR temperature sensor in fixed point 0.16 format. Note: this field exists in products that contain SAR (m0s8sar) only. Default Value: X

30.1.231 SFLASH_SAR_TEMP_OFFSET

SAR Temperature Sensor Offset

Address: 0x0FFFF266

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	TEMP_OFFSET [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	TEMP_OFFSET [15:8]							

Bits	Name	Description
15 : 0	TEMP_OFFSET	Offset value for SAR temperature sensor in fixed point 10.6 format. Note: this field exists in products that contain SAR (m0s8sar) only. Default Value: X

30.1.232 SFLASH_SKIP_CHECKSUM

Checksum Skip Option Register

Address: 0x0FFFF269

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	SKIP [7:0]							

Bits	Name	Description
7 : 0	SKIP	0: Perform checksum check (see CHECKSUM fueld below) 1: Skip checksum check >1: Undefined - do not use Default Value: X

30.1.233 SFLASH_PROT_VIRGINKEY0

Virgin Protection Mode Key

Address: 0x0FFFF270

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	KEY8 [7:0]							

Bits	Name	Description
7 : 0	KEY8	Key Byte Default Value: X

30.1.234 SFLASH_PROT_VIRGINKEY1

Virgin Protection Mode Key

Address: 0x0FFFF271

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	KEY8 [7:0]							

Bits	Name	Description
7 : 0	KEY8	Key Byte Default Value: X

30.1.235 SFLASH_PROT_VIRGINKEY2

Virgin Protection Mode Key

Address: 0x0FFFF272

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	KEY8 [7:0]							

Bits	Name	Description
7 : 0	KEY8	Key Byte Default Value: X

30.1.236 SFLASH_PROT_VIRGINKEY3

Virgin Protection Mode Key

Address: 0x0FFFF273

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	KEY8 [7:0]							

Bits	Name	Description
7 : 0	KEY8	Key Byte Default Value: X

30.1.237 SFLASH_PROT_VIRGINKEY4

Virgin Protection Mode Key

Address: 0x0FFFF274

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	KEY8 [7:0]							

Bits	Name	Description
7 : 0	KEY8	Key Byte Default Value: X

30.1.238 SFLASH_PROT_VIRGINKEY5

Virgin Protection Mode Key

Address: 0x0FFFF275

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	KEY8 [7:0]							

Bits	Name	Description
7 : 0	KEY8	Key Byte Default Value: X

30.1.239 SFLASH_PROT_VIRGINKEY6

Virgin Protection Mode Key

Address: 0x0FFFF276

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	KEY8 [7:0]							

Bits	Name	Description
7 : 0	KEY8	Key Byte Default Value: X

30.1.240 SFLASH_PROT_VIRGINKEY7

Virgin Protection Mode Key

Address: 0x0FFFF277

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	KEY8 [7:0]							

Bits	Name	Description
7 : 0	KEY8	Key Byte Default Value: X

30.1.241 SFLASH_DIE_LOT0

Lot Number (3 bytes)

Address: 0x0FFFF278

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	LOT [7:0]							

Bits	Name	Description
7 : 0	LOT	Lot Number Byte Default Value: X

30.1.242 SFLASH_DIE_LOT1

Lot Number (3 bytes)

Address: 0x0FFFF279

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	LOT [7:0]							

Bits	Name	Description
7 : 0	LOT	Lot Number Byte Default Value: X

30.1.243 SFLASH_DIE_LOT2

Lot Number (3 bytes)

Address: 0x0FFFF27A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	LOT [7:0]							

Bits	Name	Description
7 : 0	LOT	Lot Number Byte Default Value: X

30.1.244 SFLASH_DIE_WAFER

Wafer Number

Address: 0x0FFFF27B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	WAFER [7:0]							

Bits	Name	Description
7 : 0	WAFER	Wafer Number Default Value: X

30.1.245 SFLASH_DIE_X

X Position on Wafer, CRI Pass/Fail Bin

Address: 0x0FFFF27C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	X [7:0]							

Bits	Name	Description
7 : 0	X	X Position Default Value: X

30.1.246 SFLASH_DIE_Y

Y Position on Wafer, CHI Pass/Fail Bin

Address: 0x0FFFF27D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	Y [7:0]							

Bits	Name	Description
7 : 0	Y	Y Position Default Value: X

30.1.247 SFLASH_DIE_SORT

Sort1/2/3 Pass/Fail Bin

Address: 0x0FFFF27E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		None	None	None	None	None	None
Name	None [7:6]		ENG_PASS	CHI_PASS	CRI_PASS	S3_PASS	S2_PASS	S1_PASS

Bits	Name	Description
5	ENG_PASS	ENG Pass Bin Default Value: X
4	CHI_PASS	CHI Pass Bin (1) or 0 (Fail Bin) Default Value: X
3	CRI_PASS	CRI Pass Bin (1) or 0 (Fail Bin) Default Value: X
2	S3_PASS	SORT3 Pass Bin (1) or 0 (Fail Bin) Default Value: X
1	S2_PASS	SORT2 Pass Bin (1) or 0 (Fail Bin) Default Value: X
0	S1_PASS	SORT1 Pass Bin (1) or 0 (Fail Bin) Default Value: X

30.1.248 SFLASH_DIE_MINOR

Minor Revision Number

Address: 0x0FFFF27F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	MINOR [7:0]							

Bits	Name	Description
7 : 0	MINOR	Minor revision number Default Value: X

30.1.249 SFLASH_PE_TE_DATA0

PE/TE Data

Address: 0x0FFFF300

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

30.1.250 SFLASH_PE_TE_DATA1

PE/TE Data

Address: 0x0FFFF301

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

30.1.251 SFLASH_PE_TE_DATA2

PE/TE Data

Address: 0x0FFFF302

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

30.1.252 SFLASH_PE_TE_DATA3

PE/TE Data

Address: 0x0FFFF303

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

30.1.253 SFLASH_PE_TE_DATA4

PE/TE Data

Address: 0x0FFFF304

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

30.1.254 SFLASH_PE_TE_DATA5

PE/TE Data

Address: 0x0FFFF305

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

30.1.255 SFLASH_PE_TE_DATA6

PE/TE Data

Address: 0x0FFFF306

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

30.1.256 SFLASH_PE_TE_DATA7

PE/TE Data

Address: 0x0FFFF307

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

30.1.257 SFLASH_PE_TE_DATA8

PE/TE Data

Address: 0x0FFFF308

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

30.1.258 SFLASH_PE_TE_DATA9

PE/TE Data

Address: 0x0FFFF309

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

30.1.259 SFLASH_PE_TE_DATA10

PE/TE Data

Address: 0x0FFFF30A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

30.1.260 SFLASH_PE_TE_DATA11

PE/TE Data

Address: 0x0FFFF30B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

30.1.261 SFLASH_PE_TE_DATA12

PE/TE Data

Address: 0x0FFFF30C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

30.1.262 SFLASH_PE_TE_DATA13

PE/TE Data

Address: 0x0FFFF30D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

30.1.263 SFLASH_PE_TE_DATA14

PE/TE Data

Address: 0x0FFFF30E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

30.1.264 SFLASH_PE_TE_DATA15

PE/TE Data

Address: 0x0FFFF30F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

30.1.265 SFLASH_PE_TE_DATA16

PE/TE Data

Address: 0x0FFFF310

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

30.1.266 SFLASH_PE_TE_DATA17

PE/TE Data

Address: 0x0FFFF311

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

30.1.267 SFLASH_PE_TE_DATA18

PE/TE Data

Address: 0x0FFFF312

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

30.1.268 SFLASH_PE_TE_DATA19

PE/TE Data

Address: 0x0FFFF313

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

30.1.269 SFLASH_PE_TE_DATA20

PE/TE Data

Address: 0x0FFFF314

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

30.1.270 SFLASH_PE_TE_DATA21

PE/TE Data

Address: 0x0FFFF315

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

30.1.271 SFLASH_PE_TE_DATA22

PE/TE Data

Address: 0x0FFFF316

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

30.1.272 SFLASH_PE_TE_DATA23

PE/TE Data

Address: 0x0FFFF317

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

30.1.273 SFLASH_PE_TE_DATA24

PE/TE Data

Address: 0x0FFFF318

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

30.1.274 SFLASH_PE_TE_DATA25

PE/TE Data

Address: 0x0FFFF319

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

30.1.275 SFLASH_PE_TE_DATA26

PE/TE Data

Address: 0x0FFFF31A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

30.1.276 SFLASH_PE_TE_DATA27

PE/TE Data

Address: 0x0FFFF31B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

30.1.277 SFLASH_PE_TE_DATA28

PE/TE Data

Address: 0x0FFFF31C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

30.1.278 SFLASH_PE_TE_DATA29

PE/TE Data

Address: 0x0FFFF31D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

30.1.279 SFLASH_PE_TE_DATA30

PE/TE Data

Address: 0x0FFFF31E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

30.1.280 SFLASH_PE_TE_DATA31

PE/TE Data

Address: 0x0FFFF31F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	PE/TE Data Default Value: X

30.1.281 SFLASH_PP

Preprogram Settings

Address: 0x0FFFF320

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	PERIOD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	None				None			
Name	NDAC [31:28]				PDAC [27:24]			

Bits	Name	Description
31 : 28	NDAC	NDAC input. Each increment in NDAC causes an increase of ~0.10V in VNEG Default Value: X
27 : 24	PDAC	PDAC input. Each increment in PDAC causes an increase of ~0.10V in VPOS Default Value: X
23 : 0	PERIOD	Period of timer in clk_spcif_timer ticks. For regular FLASH, clock is 36MHz from dedicated oscillator. For FLASH-Lite, clock is same as clk_hf, which must be set to 48MHz for 48MHz devices and 12MHz for max 16MHz devices Default Value: X

30.1.282 SFLASH_E

Erase Settings

Address: 0x0FFFF324

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	PERIOD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	None				None			
Name	NDAC [31:28]				PDAC [27:24]			

Bits	Name	Description
31 : 28	NDAC	NDAC input. Each increment in NDAC causes an increase of ~0.10V in VNEG Default Value: X
27 : 24	PDAC	PDAC input. Each increment in PDAC causes an increase of ~0.10V in VPOS Default Value: X
23 : 0	PERIOD	Period of timer in clk_spcif_timer ticks. For regular FLASH, clock is 36MHz from dedicated oscillator. For FLASH-Lite, clock is same as clk_hf, which must be set to 48MHz for 48MHz devices and 12MHz for max 16MHz devices Default Value: X

30.1.283 SFLASH_P

Program Settings

Address: 0x0FFFF328

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	PERIOD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	None				None			
Name	NDAC [31:28]				PDAC [27:24]			

Bits	Name	Description
31 : 28	NDAC	NDAC input. Each increment in NDAC causes an increase of ~0.10V in VNEG Default Value: X
27 : 24	PDAC	PDAC input. Each increment in PDAC causes an increase of ~0.10V in VPOS Default Value: X
23 : 0	PERIOD	Period of timer in clk_spcif_timer ticks. For regular FLASH, clock is 36MHz from dedicated oscillator. For FLASH-Lite, clock is same as clk_hf, which must be set to 48MHz for 48MHz devices and 12MHz for max 16MHz devices Default Value: X

30.1.284 SFLASH_EA_E

Erase All - Erase Settings

Address: 0x0FFFF32C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	PERIOD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	None				None			
Name	NDAC [31:28]				PDAC [27:24]			

Bits	Name	Description
31 : 28	NDAC	NDAC input. Each increment in NDAC causes an increase of ~0.10V in VNEG Default Value: X
27 : 24	PDAC	PDAC input. Each increment in PDAC causes an increase of ~0.10V in VPOS Default Value: X
23 : 0	PERIOD	Period of timer in clk_spcif_timer ticks. For regular FLASH, clock is 36MHz from dedicated oscillator. For FLASH-Lite, clock is same as clk_hf, which must be set to 48MHz for 48MHz devices and 12MHz for max 16MHz devices Default Value: X

30.1.285 SFLASH_EA_P

Erase All - Program Settings

Address: 0x0FFFF330

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	PERIOD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	None				None			
Name	NDAC [31:28]				PDAC [27:24]			

Bits	Name	Description
31 : 28	NDAC	NDAC input. Each increment in NDAC causes an increase of ~0.10V in VNEG Default Value: X
27 : 24	PDAC	PDAC input. Each increment in PDAC causes an increase of ~0.10V in VPOS Default Value: X
23 : 0	PERIOD	Period of timer in clk_spcif_timer ticks. For regular FLASH, clock is 36MHz from dedicated oscillator. For FLASH-Lite, clock is same as clk_hf, which must be set to 48MHz for 48MHz devices and 12MHz for max 16MHz devices Default Value: X

30.1.286 SFLASH_ES_E

Erase Sector - Erase Settings

Address: 0x0FFFF334

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	PERIOD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	None				None			
Name	NDAC [31:28]				PDAC [27:24]			

Bits	Name	Description
31 : 28	NDAC	NDAC input. Each increment in NDAC causes an increase of ~0.10V in VNEG Default Value: X
27 : 24	PDAC	PDAC input. Each increment in PDAC causes an increase of ~0.10V in VPOS Default Value: X
23 : 0	PERIOD	Period of timer in clk_spcif_timer ticks. For regular FLASH, clock is 36MHz from dedicated oscillator. For FLASH-Lite, clock is same as clk_hf, which must be set to 48MHz for 48MHz devices and 12MHz for max 16MHz devices Default Value: X

30.1.287 SFLASH_ES_P_EO

Erase Sector - Program EO Settings

Address: 0x0FFFF338

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	PERIOD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	None				None			
Name	NDAC [31:28]				PDAC [27:24]			

Bits	Name	Description
31 : 28	NDAC	NDAC input. Each increment in NDAC causes an increase of ~0.10V in VNEG Default Value: X
27 : 24	PDAC	PDAC input. Each increment in PDAC causes an increase of ~0.10V in VPOS Default Value: X
23 : 0	PERIOD	Period of timer in clk_spcif_timer ticks. For regular FLASH, clock is 36MHz from dedicated oscillator. For FLASH-Lite, clock is same as clk_hf, which must be set to 48MHz for 48MHz devices and 12MHz for max 16MHz devices Default Value: X

30.1.288 SFLASH_E_VCTAT

Bandgap Trim Register

Address: 0x0FFFF33C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	RW		RW			
HW Access	None	None	None		None			
Name	None	VCTAT_ENABLE	VCTAT_VOLTAGE [5:4]		VCTAT_SLOPE [3:0]			

Bits	Name	Description
6	VCTAT_ENABLE	Enable VCTAT block Default Value: X
5 : 4	VCTAT_VOLTAGE	Output voltage absolute trim Default Value: X
3 : 0	VCTAT_SLOPE	Output slope setting controls. The slope of the voltage with temperature varies from ~0% to ~15% from the value at 55C over the temperature range -40C to 150C based on control signal settings 0 to 15 Default Value: X

30.1.289 SFLASH_P_VCTAT

Bandgap Trim Register

Address: 0x0FFFF33D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	RW		RW			
HW Access	None	None	None		None			
Name	None	VCTAT_ENABLE	VCTAT_VOLTAGE [5:4]		VCTAT_SLOPE [3:0]			

Bits	Name	Description
6	VCTAT_ENABLE	Enable VCTAT block Default Value: X
5 : 4	VCTAT_VOLTAGE	Output voltage absolute trim Default Value: X
3 : 0	VCTAT_SLOPE	Output slope setting controls. The slope of the voltage with temperature varies from ~0% to ~15% from the value at 55C over the temperature range -40C to 150C based on control signal settings 0 to 15 Default Value: X

30.1.290 SFLASH_IMO_MAXF0

Max frequency for trim pair

Address: 0x0FFFF340

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		None					
Name	None [7:6]		MAXFREQ [5:0]					

Bits	Name	Description
5 : 0	MAXFREQ	Max frequency (3..48) at which IMO_ABS/TMPCO3 is valid (range is IMO_MAXF2+1 .. IMO_MAXF3). Default Value: X

30.1.291 SFLASH_IMO_ABS0

Value for PWR_BG_TRIM4 (ICTAT trim for IMO current reference).

Address: 0x0FFFF341

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		None					
Name	None [7:6]		ABS_TRIM_IMO [5:0]					

Bits	Name	Description
5 : 0	ABS_TRIM_IMO	IMO-irefgen output current magnitude trim Default Value: X

30.1.292 SFLASH_IMO_TMPCO0

Value for PWR_BG_TRIM5 (ICTAT tempco for IMO current reference).

Address: 0x0FFFF342

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		None					
Name	None [7:6]		TMPCO_TRIM_IMO [5:0]					

Bits	Name	Description
5 : 0	TMPCO_TRIM_IMO	IMO-irefgen output current temperature co-efficient trim Default Value: X

30.1.293 SFLASH_IMO_MAXF1

Max frequency for trim pair

Address: 0x0FFFF343

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		None					
Name	None [7:6]		MAXFREQ [5:0]					

Bits	Name	Description
5 : 0	MAXFREQ	Max frequency (3..48) at which IMO_ABS/TMPCO3 is valid (range is IMO_MAXF2+1 .. IMO_MAXF3). Default Value: X

30.1.294 SFLASH_IMO_ABS1

Value for PWR_BG_TRIM4 (ICTAT trim for IMO current reference).

Address: 0x0FFFF344

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		None					
Name	None [7:6]		ABS_TRIM_IMO [5:0]					

Bits	Name	Description
5 : 0	ABS_TRIM_IMO	IMO-irefgen output current magnitude trim Default Value: X

30.1.295 SFLASH_IMO_TMPCO1

Value for PWR_BG_TRIM5 (ICTAT tempco for IMO current reference).

Address: 0x0FFFF345

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		None					
Name	None [7:6]		TMPCO_TRIM_IMO [5:0]					

Bits	Name	Description
5 : 0	TMPCO_TRIM_IMO	IMO-irefgen output current temperature co-efficient trim Default Value: X

30.1.296 SFLASH_IMO_MAXF2

Max frequency for trim pair

Address: 0x0FFFF346

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		None					
Name	None [7:6]		MAXFREQ [5:0]					

Bits	Name	Description
5 : 0	MAXFREQ	Max frequency (3..48) at which IMO_ABS/TMPCO3 is valid (range is IMO_MAXF2+1 .. IMO_MAXF3). Default Value: X

30.1.297 SFLASH_IMO_ABS2

Value for PWR_BG_TRIM4 (ICTAT trim for IMO current reference).

Address: 0x0FFFF347

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		None					
Name	None [7:6]		ABS_TRIM_IMO [5:0]					

Bits	Name	Description
5 : 0	ABS_TRIM_IMO	IMO-irefgen output current magnitude trim Default Value: X

30.1.298 SFLASH_IMO_TMPCO2

Value for PWR_BG_TRIM5 (ICTAT tempco for IMO current reference).

Address: 0x0FFFF348

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		None					
Name	None [7:6]		TMPCO_TRIM_IMO [5:0]					

Bits	Name	Description
5 : 0	TMPCO_TRIM_IMO	IMO-irefgen output current temperature co-efficient trim Default Value: X

30.1.299 SFLASH_IMO_MAXF3

Max frequency for trim pair

Address: 0x0FFFF349

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		None					
Name	None [7:6]		MAXFREQ [5:0]					

Bits	Name	Description
5 : 0	MAXFREQ	Max frequency (3..48) at which IMO_ABS/TMPCO3 is valid (range is IMO_MAXF2+1 .. IMO_MAXF3). Default Value: X

30.1.300 SFLASH_IMO_ABS3

Value for PWR_BG_TRIM4 (ICTAT trim for IMO current reference).

Address: 0x0FFFF34A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		None					
Name	None [7:6]		ABS_TRIM_IMO [5:0]					

Bits	Name	Description
5 : 0	ABS_TRIM_IMO	IMO-irefgen output current magnitude trim Default Value: X

30.1.301 SFLASH_IMO_TMPCO3

Value for PWR_BG_TRIM5 (ICTAT tempco for IMO current reference).

Address: 0x0FFFF34B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		None					
Name	None [7:6]		TMPCO_TRIM_IMO [5:0]					

Bits	Name	Description
5 : 0	TMPCO_TRIM_IMO	IMO-irefgen output current temperature co-efficient trim Default Value: X

30.1.302 SFLASH_IMO_ABS4

Value for PWR_BG_TRIM4 (ICTAT trim for IMO current reference).

Address: 0x0FFFF34C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		None					
Name	None [7:6]		ABS_TRIM_IMO [5:0]					

Bits	Name	Description
5 : 0	ABS_TRIM_IMO	IMO-irefgen output current magnitude trim Default Value: X

30.1.303 SFLASH_IMO_TMPCO4

Value for PWR_BG_TRIM5 (ICTAT tempco for IMO current reference).

Address: 0x0FFFF34D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		None					
Name	None [7:6]		TMPCO_TRIM_IMO [5:0]					

Bits	Name	Description
5 : 0	TMPCO_TRIM_IMO	IMO-irefgen output current temperature co-efficient trim Default Value: X

30.1.304 SFLASH_IMO_TRIM0

IMO Trim Register (SRSSv2)

Address: 0x0FFFF350

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

30.1.305 SFLASH_IMO_TRIM1

IMO Trim Register (SRSSv2)

Address: 0x0FFFF351

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

30.1.306 SFLASH_IMO_TRIM2

IMO Trim Register (SRSSv2)

Address: 0x0FFFF352

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

30.1.307 SFLASH_IMO_TRIM3

IMO Trim Register (SRSSv2)

Address: 0x0FFFF353

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

30.1.308 SFLASH_IMO_TRIM4

IMO Trim Register (SRSSv2)

Address: 0x0FFFF354

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

30.1.309 SFLASH_IMO_TRIM5

IMO Trim Register (SRSSv2)

Address: 0x0FFFF355

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

30.1.310 SFLASH_IMO_TRIM6

IMO Trim Register (SRSSv2)

Address: 0x0FFFF356

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

30.1.311 SFLASH_IMO_TRIM7

IMO Trim Register (SRSSv2)

Address: 0x0FFFF357

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

30.1.312 SFLASH_IMO_TRIM8

IMO Trim Register (SRSSv2)

Address: 0x0FFFF358

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

30.1.313 SFLASH_IMO_TRIM9

IMO Trim Register (SRSSv2)

Address: 0x0FFFF359

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

30.1.314 SFLASH_IMO_TRIM10

IMO Trim Register (SRSSv2)

Address: 0x0FFFF35A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

30.1.315 SFLASH_IMO_TRIM11

IMO Trim Register (SRSSv2)

Address: 0x0FFFF35B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

30.1.316 SFLASH_IMO_TRIM12

IMO Trim Register (SRSSv2)

Address: 0x0FFFF35C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

30.1.317 SFLASH_IMO_TRIM13

IMO Trim Register (SRSSv2)

Address: 0x0FFFF35D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

30.1.318 SFLASH_IMO_TRIM14

IMO Trim Register (SRSSv2)

Address: 0x0FFFF35E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

30.1.319 SFLASH_IMO_TRIM15

IMO Trim Register (SRSSv2)

Address: 0x0FFFF35F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

30.1.320 SFLASH_IMO_TRIM16

IMO Trim Register (SRSSv2)

Address: 0x0FFFF360

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

30.1.321 SFLASH_IMO_TRIM17

IMO Trim Register (SRSSv2)

Address: 0x0FFFF361

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

30.1.322 SFLASH_IMO_TRIM18

IMO Trim Register (SRSSv2)

Address: 0x0FFFF362

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

30.1.323 SFLASH_IMO_TRIM19

IMO Trim Register (SRSSv2)

Address: 0x0FFFF363

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

30.1.324 SFLASH_IMO_TRIM20

IMO Trim Register (SRSSv2)

Address: 0x0FFFF364

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

30.1.325 SFLASH_IMO_TRIM21

IMO Trim Register (SRSSv2)

Address: 0x0FFFF365

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

30.1.326 SFLASH_IMO_TRIM22

IMO Trim Register (SRSSv2)

Address: 0x0FFFF366

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

30.1.327 SFLASH_IMO_TRIM23

IMO Trim Register (SRSSv2)

Address: 0x0FFFF367

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

30.1.328 SFLASH_IMO_TRIM24

IMO Trim Register (SRSSv2)

Address: 0x0FFFF368

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

30.1.329 SFLASH_IMO_TRIM25

IMO Trim Register (SRSSv2)

Address: 0x0FFFF369

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

30.1.330 SFLASH_IMO_TRIM26

IMO Trim Register (SRSSv2)

Address: 0x0FFFF36A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

30.1.331 SFLASH_IMO_TRIM27

IMO Trim Register (SRSSv2)

Address: 0x0FFFF36B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

30.1.332 SFLASH_IMO_TRIM28

IMO Trim Register (SRSSv2)

Address: 0x0FFFF36C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

30.1.333 SFLASH_IMO_TRIM29

IMO Trim Register (SRSSv2)

Address: 0x0FFFF36D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

30.1.334 SFLASH_IMO_TRIM30

IMO Trim Register (SRSSv2)

Address: 0x0FFFF36E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

30.1.335 SFLASH_IMO_TRIM31

IMO Trim Register (SRSSv2)

Address: 0x0FFFF36F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

30.1.336 SFLASH_IMO_TRIM32

IMO Trim Register (SRSSv2)

Address: 0x0FFFF370

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

30.1.337 SFLASH_IMO_TRIM33

IMO Trim Register (SRSSv2)

Address: 0x0FFFF371

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

30.1.338 SFLASH_IMO_TRIM34

IMO Trim Register (SRSSv2)

Address: 0x0FFFF372

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

30.1.339 SFLASH_IMO_TRIM35

IMO Trim Register (SRSSv2)

Address: 0x0FFFF373

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

30.1.340 SFLASH_IMO_TRIM36

IMO Trim Register (SRSSv2)

Address: 0x0FFFF374

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

30.1.341 SFLASH_IMO_TRIM37

IMO Trim Register (SRSSv2)

Address: 0x0FFFF375

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

30.1.342 SFLASH_IMO_TRIM38

IMO Trim Register (SRSSv2)

Address: 0x0FFFF376

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

30.1.343 SFLASH_IMO_TRIM39

IMO Trim Register (SRSSv2)

Address: 0x0FFFF377

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

30.1.344 SFLASH_IMO_TRIM40

IMO Trim Register (SRSSv2)

Address: 0x0FFFF378

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

30.1.345 SFLASH_IMO_TRIM41

IMO Trim Register (SRSSv2)

Address: 0x0FFFF379

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

30.1.346 SFLASH_IMO_TRIM42

IMO Trim Register (SRSSv2)

Address: 0x0FFFF37A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

30.1.347 SFLASH_IMO_TRIM43

IMO Trim Register (SRSSv2)

Address: 0x0FFFF37B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

30.1.348 SFLASH_IMO_TRIM44

IMO Trim Register (SRSSv2)

Address: 0x0FFFF37C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

30.1.349 SFLASH_IMO_TRIM45

IMO Trim Register (SRSSv2)

Address: 0x0FFFF37D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

30.1.350 SFLASH_CHECKSUM

Boot Checksum

Address: 0x0FFFF3FE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	CHECKSUM [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	CHECKSUM [15:8]							

Bits	Name	Description
15 : 0	CHECKSUM	Checksum of fixed data checked during boot. This checksum covers all of rows 1,2,3 of macro 0 + row 3 of macro 1 (except this checksum, and row 3 of macro 1 only if it exists). Default Value: X

30.1.351 SFLASH_MACRO_0_FREE_SFLASH0

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.352 SFLASH_MACRO_0_FREE_SFLASH1

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF401

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.353 SFLASH_MACRO_0_FREE_SFLASH2

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF402

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.354 SFLASH_MACRO_0_FREE_SFLASH3

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF403

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.355 SFLASH_MACRO_0_FREE_SFLASH4

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF404

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.356 SFLASH_MACRO_0_FREE_SFLASH5

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF405

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.357 SFLASH_MACRO_0_FREE_SFLASH6

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF406

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.358 SFLASH_MACRO_0_FREE_SFLASH7

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF407

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.359 SFLASH_MACRO_0_FREE_SFLASH8

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF408

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.360 SFLASH_MACRO_0_FREE_SFLASH9

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF409

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.361 SFLASH_MACRO_0_FREE_SFLASH10

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF40A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.362 SFLASH_MACRO_0_FREE_SFLASH11

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF40B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.363 SFLASH_MACRO_0_FREE_SFLASH12

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF40C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.364 SFLASH_MACRO_0_FREE_SFLASH13

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF40D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.365 SFLASH_MACRO_0_FREE_SFLASH14

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF40E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.366 SFLASH_MACRO_0_FREE_SFLASH15

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF40F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.367 SFLASH_MACRO_0_FREE_SFLASH16

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF410

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.368 SFLASH_MACRO_0_FREE_SFLASH17

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF411

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.369 SFLASH_MACRO_0_FREE_SFLASH18

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF412

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.370 SFLASH_MACRO_0_FREE_SFLASH19

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF413

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.371 SFLASH_MACRO_0_FREE_SFLASH20

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF414

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.372 SFLASH_MACRO_0_FREE_SFLASH21

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF415

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.373 SFLASH_MACRO_0_FREE_SFLASH22

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF416

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.374 SFLASH_MACRO_0_FREE_SFLASH23

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF417

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.375 SFLASH_MACRO_0_FREE_SFLASH24

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF418

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.376 SFLASH_MACRO_0_FREE_SFLASH25

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF419

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.377 SFLASH_MACRO_0_FREE_SFLASH26

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF41A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.378 SFLASH_MACRO_0_FREE_SFLASH27

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF41B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.379 SFLASH_MACRO_0_FREE_SFLASH28

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF41C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.380 SFLASH_MACRO_0_FREE_SFLASH29

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF41D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.381 SFLASH_MACRO_0_FREE_SFLASH30

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF41E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.382 SFLASH_MACRO_0_FREE_SFLASH31

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF41F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.383 SFLASH_MACRO_0_FREE_SFLASH32

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF420

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.384 SFLASH_MACRO_0_FREE_SFLASH33

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF421

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.385 SFLASH_MACRO_0_FREE_SFLASH34

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF422

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.386 SFLASH_MACRO_0_FREE_SFLASH35

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF423

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.387 SFLASH_MACRO_0_FREE_SFLASH36

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF424

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.388 SFLASH_MACRO_0_FREE_SFLASH37

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF425

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.389 SFLASH_MACRO_0_FREE_SFLASH38

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF426

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.390 SFLASH_MACRO_0_FREE_SFLASH39

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF427

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.391 SFLASH_MACRO_0_FREE_SFLASH40

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF428

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.392 SFLASH_MACRO_0_FREE_SFLASH41

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF429

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.393 SFLASH_MACRO_0_FREE_SFLASH42

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF42A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.394 SFLASH_MACRO_0_FREE_SFLASH43

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF42B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.395 SFLASH_MACRO_0_FREE_SFLASH44

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF42C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.396 SFLASH_MACRO_0_FREE_SFLASH45

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF42D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.397 SFLASH_MACRO_0_FREE_SFLASH46

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF42E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.398 SFLASH_MACRO_0_FREE_SFLASH47

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF42F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.399 SFLASH_MACRO_0_FREE_SFLASH48

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF430

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.400 SFLASH_MACRO_0_FREE_SFLASH49

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF431

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.401 SFLASH_MACRO_0_FREE_SFLASH50

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF432

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.402 SFLASH_MACRO_0_FREE_SFLASH51

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF433

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.403 SFLASH_MACRO_0_FREE_SFLASH52

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF434

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.404 SFLASH_MACRO_0_FREE_SFLASH53

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF435

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.405 SFLASH_MACRO_0_FREE_SFLASH54

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF436

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.406 SFLASH_MACRO_0_FREE_SFLASH55

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF437

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.407 SFLASH_MACRO_0_FREE_SFLASH56

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF438

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.408 SFLASH_MACRO_0_FREE_SFLASH57

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF439

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.409 SFLASH_MACRO_0_FREE_SFLASH58

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF43A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.410 SFLASH_MACRO_0_FREE_SFLASH59

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF43B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.411 SFLASH_MACRO_0_FREE_SFLASH60

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF43C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.412 SFLASH_MACRO_0_FREE_SFLASH61

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF43D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.413 SFLASH_MACRO_0_FREE_SFLASH62

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF43E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.414 SFLASH_MACRO_0_FREE_SFLASH63

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF43F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.415 SFLASH_MACRO_0_FREE_SFLASH64

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF440

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.416 SFLASH_MACRO_0_FREE_SFLASH65

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF441

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.417 SFLASH_MACRO_0_FREE_SFLASH66

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF442

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.418 SFLASH_MACRO_0_FREE_SFLASH67

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF443

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.419 SFLASH_MACRO_0_FREE_SFLASH68

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF444

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.420 SFLASH_MACRO_0_FREE_SFLASH69

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF445

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.421 SFLASH_MACRO_0_FREE_SFLASH70

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF446

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.422 SFLASH_MACRO_0_FREE_SFLASH71

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF447

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.423 SFLASH_MACRO_0_FREE_SFLASH72

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF448

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.424 SFLASH_MACRO_0_FREE_SFLASH73

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF449

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.425 SFLASH_MACRO_0_FREE_SFLASH74

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF44A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.426 SFLASH_MACRO_0_FREE_SFLASH75

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF44B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.427 SFLASH_MACRO_0_FREE_SFLASH76

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF44C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.428 SFLASH_MACRO_0_FREE_SFLASH77

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF44D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.429 SFLASH_MACRO_0_FREE_SFLASH78

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF44E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.430 SFLASH_MACRO_0_FREE_SFLASH79

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF44F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.431 SFLASH_MACRO_0_FREE_SFLASH80

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF450

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.432 SFLASH_MACRO_0_FREE_SFLASH81

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF451

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.433 SFLASH_MACRO_0_FREE_SFLASH82

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF452

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.434 SFLASH_MACRO_0_FREE_SFLASH83

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF453

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.435 SFLASH_MACRO_0_FREE_SFLASH84

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF454

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.436 SFLASH_MACRO_0_FREE_SFLASH85

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF455

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.437 SFLASH_MACRO_0_FREE_SFLASH86

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF456

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.438 SFLASH_MACRO_0_FREE_SFLASH87

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF457

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.439 SFLASH_MACRO_0_FREE_SFLASH88

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF458

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.440 SFLASH_MACRO_0_FREE_SFLASH89

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF459

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.441 SFLASH_MACRO_0_FREE_SFLASH90

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF45A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.442 SFLASH_MACRO_0_FREE_SFLASH91

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF45B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.443 SFLASH_MACRO_0_FREE_SFLASH92

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF45C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.444 SFLASH_MACRO_0_FREE_SFLASH93

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF45D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.445 SFLASH_MACRO_0_FREE_SFLASH94

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF45E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.446 SFLASH_MACRO_0_FREE_SFLASH95

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF45F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.447 SFLASH_MACRO_0_FREE_SFLASH96

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF460

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.448 SFLASH_MACRO_0_FREE_SFLASH97

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF461

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.449 SFLASH_MACRO_0_FREE_SFLASH98

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF462

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.450 SFLASH_MACRO_0_FREE_SFLASH99

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF463

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.451 SFLASH_MACRO_0_FREE_SFLASH100

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF464

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.452 SFLASH_MACRO_0_FREE_SFLASH101

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF465

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.453 SFLASH_MACRO_0_FREE_SFLASH102

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF466

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.454 SFLASH_MACRO_0_FREE_SFLASH103

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF467

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.455 SFLASH_MACRO_0_FREE_SFLASH104

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF468

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.456 SFLASH_MACRO_0_FREE_SFLASH105

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF469

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.457 SFLASH_MACRO_0_FREE_SFLASH106

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF46A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.458 SFLASH_MACRO_0_FREE_SFLASH107

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF46B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.459 SFLASH_MACRO_0_FREE_SFLASH108

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF46C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.460 SFLASH_MACRO_0_FREE_SFLASH109

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF46D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.461 SFLASH_MACRO_0_FREE_SFLASH110

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF46E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.462 SFLASH_MACRO_0_FREE_SFLASH111

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF46F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.463 SFLASH_MACRO_0_FREE_SFLASH112

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF470

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.464 SFLASH_MACRO_0_FREE_SFLASH113

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF471

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.465 SFLASH_MACRO_0_FREE_SFLASH114

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF472

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.466 SFLASH_MACRO_0_FREE_SFLASH115

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF473

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.467 SFLASH_MACRO_0_FREE_SFLASH116

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF474

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.468 SFLASH_MACRO_0_FREE_SFLASH117

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF475

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.469 SFLASH_MACRO_0_FREE_SFLASH118

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF476

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.470 SFLASH_MACRO_0_FREE_SFLASH119

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF477

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.471 SFLASH_MACRO_0_FREE_SFLASH120

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF478

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.472 SFLASH_MACRO_0_FREE_SFLASH121

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF479

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.473 SFLASH_MACRO_0_FREE_SFLASH122

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF47A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.474 SFLASH_MACRO_0_FREE_SFLASH123

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF47B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.475 SFLASH_MACRO_0_FREE_SFLASH124

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF47C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.476 SFLASH_MACRO_0_FREE_SFLASH125

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF47D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.477 SFLASH_MACRO_0_FREE_SFLASH126

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF47E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.478 SFLASH_MACRO_0_FREE_SFLASH127

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF47F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.479 SFLASH_MACRO_0_FREE_SFLASH128

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF480

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.480 SFLASH_MACRO_0_FREE_SFLASH129

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF481

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.481 SFLASH_MACRO_0_FREE_SFLASH130

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF482

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.482 SFLASH_MACRO_0_FREE_SFLASH131

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF483

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.483 SFLASH_MACRO_0_FREE_SFLASH132

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF484

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.484 SFLASH_MACRO_0_FREE_SFLASH133

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF485

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.485 SFLASH_MACRO_0_FREE_SFLASH134

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF486

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.486 SFLASH_MACRO_0_FREE_SFLASH135

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF487

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.487 SFLASH_MACRO_0_FREE_SFLASH136

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF488

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.488 SFLASH_MACRO_0_FREE_SFLASH137

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF489

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.489 SFLASH_MACRO_0_FREE_SFLASH138

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF48A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.490 SFLASH_MACRO_0_FREE_SFLASH139

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF48B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.491 SFLASH_MACRO_0_FREE_SFLASH140

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF48C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.492 SFLASH_MACRO_0_FREE_SFLASH141

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF48D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.493 SFLASH_MACRO_0_FREE_SFLASH142

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF48E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.494 SFLASH_MACRO_0_FREE_SFLASH143

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF48F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.495 SFLASH_MACRO_0_FREE_SFLASH144

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF490

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.496 SFLASH_MACRO_0_FREE_SFLASH145

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF491

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.497 SFLASH_MACRO_0_FREE_SFLASH146

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF492

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.498 SFLASH_MACRO_0_FREE_SFLASH147

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF493

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.499 SFLASH_MACRO_0_FREE_SFLASH148

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF494

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.500 SFLASH_MACRO_0_FREE_SFLASH149

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF495

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.501 SFLASH_MACRO_0_FREE_SFLASH150

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF496

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.502 SFLASH_MACRO_0_FREE_SFLASH151

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF497

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.503 SFLASH_MACRO_0_FREE_SFLASH152

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF498

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.504 SFLASH_MACRO_0_FREE_SFLASH153

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF499

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.505 SFLASH_MACRO_0_FREE_SFLASH154

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF49A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.506 SFLASH_MACRO_0_FREE_SFLASH155

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF49B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.507 SFLASH_MACRO_0_FREE_SFLASH156

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF49C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.508 SFLASH_MACRO_0_FREE_SFLASH157

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF49D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.509 SFLASH_MACRO_0_FREE_SFLASH158

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF49E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.510 SFLASH_MACRO_0_FREE_SFLASH159

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF49F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.511 SFLASH_MACRO_0_FREE_SFLASH160

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.512 SFLASH_MACRO_0_FREE_SFLASH161

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4A1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.513 SFLASH_MACRO_0_FREE_SFLASH162

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4A2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.514 SFLASH_MACRO_0_FREE_SFLASH163

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4A3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.515 SFLASH_MACRO_0_FREE_SFLASH164

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4A4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.516 SFLASH_MACRO_0_FREE_SFLASH165

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4A5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.517 SFLASH_MACRO_0_FREE_SFLASH166

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4A6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.518 SFLASH_MACRO_0_FREE_SFLASH167

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4A7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.519 SFLASH_MACRO_0_FREE_SFLASH168

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4A8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.520 SFLASH_MACRO_0_FREE_SFLASH169

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4A9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.521 SFLASH_MACRO_0_FREE_SFLASH170

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4AA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.522 SFLASH_MACRO_0_FREE_SFLASH171

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4AB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.523 SFLASH_MACRO_0_FREE_SFLASH172

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4AC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.524 SFLASH_MACRO_0_FREE_SFLASH173

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4AD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.525 SFLASH_MACRO_0_FREE_SFLASH174

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4AE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.526 SFLASH_MACRO_0_FREE_SFLASH175

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4AF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.527 SFLASH_MACRO_0_FREE_SFLASH176

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4B0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.528 SFLASH_MACRO_0_FREE_SFLASH177

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4B1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.529 SFLASH_MACRO_0_FREE_SFLASH178

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4B2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.530 SFLASH_MACRO_0_FREE_SFLASH179

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4B3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.531 SFLASH_MACRO_0_FREE_SFLASH180

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4B4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.532 SFLASH_MACRO_0_FREE_SFLASH181

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4B5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.533 SFLASH_MACRO_0_FREE_SFLASH182

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4B6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.534 SFLASH_MACRO_0_FREE_SFLASH183

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4B7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.535 SFLASH_MACRO_0_FREE_SFLASH184

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4B8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.536 SFLASH_MACRO_0_FREE_SFLASH185

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4B9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.537 SFLASH_MACRO_0_FREE_SFLASH186

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4BA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.538 SFLASH_MACRO_0_FREE_SFLASH187

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4BB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.539 SFLASH_MACRO_0_FREE_SFLASH188

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4BC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.540 SFLASH_MACRO_0_FREE_SFLASH189

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4BD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.541 SFLASH_MACRO_0_FREE_SFLASH190

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4BE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.542 SFLASH_MACRO_0_FREE_SFLASH191

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4BF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.543 SFLASH_MACRO_0_FREE_SFLASH192

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.544 SFLASH_MACRO_0_FREE_SFLASH193

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4C1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.545 SFLASH_MACRO_0_FREE_SFLASH194

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4C2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.546 SFLASH_MACRO_0_FREE_SFLASH195

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4C3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.547 SFLASH_MACRO_0_FREE_SFLASH196

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.548 SFLASH_MACRO_0_FREE_SFLASH197

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4C5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.549 SFLASH_MACRO_0_FREE_SFLASH198

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4C6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.550 SFLASH_MACRO_0_FREE_SFLASH199

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4C7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.551 SFLASH_MACRO_0_FREE_SFLASH200

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4C8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.552 SFLASH_MACRO_0_FREE_SFLASH201

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4C9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.553 SFLASH_MACRO_0_FREE_SFLASH202

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4CA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.554 SFLASH_MACRO_0_FREE_SFLASH203

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4CB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.555 SFLASH_MACRO_0_FREE_SFLASH204

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4CC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.556 SFLASH_MACRO_0_FREE_SFLASH205

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4CD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.557 SFLASH_MACRO_0_FREE_SFLASH206

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4CE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.558 SFLASH_MACRO_0_FREE_SFLASH207

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4CF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.559 SFLASH_MACRO_0_FREE_SFLASH208

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4D0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.560 SFLASH_MACRO_0_FREE_SFLASH209

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4D1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.561 SFLASH_MACRO_0_FREE_SFLASH210

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4D2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.562 SFLASH_MACRO_0_FREE_SFLASH211

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4D3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.563 SFLASH_MACRO_0_FREE_SFLASH212

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4D4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.564 SFLASH_MACRO_0_FREE_SFLASH213

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4D5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.565 SFLASH_MACRO_0_FREE_SFLASH214

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4D6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.566 SFLASH_MACRO_0_FREE_SFLASH215

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4D7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.567 SFLASH_MACRO_0_FREE_SFLASH216

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4D8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.568 SFLASH_MACRO_0_FREE_SFLASH217

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4D9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.569 SFLASH_MACRO_0_FREE_SFLASH218

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4DA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.570 SFLASH_MACRO_0_FREE_SFLASH219

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4DB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.571 SFLASH_MACRO_0_FREE_SFLASH220

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4DC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.572 SFLASH_MACRO_0_FREE_SFLASH221

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4DD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.573 SFLASH_MACRO_0_FREE_SFLASH222

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4DE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.574 SFLASH_MACRO_0_FREE_SFLASH223

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4DF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.575 SFLASH_MACRO_0_FREE_SFLASH224

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.576 SFLASH_MACRO_0_FREE_SFLASH225

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4E1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.577 SFLASH_MACRO_0_FREE_SFLASH226

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4E2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.578 SFLASH_MACRO_0_FREE_SFLASH227

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4E3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.579 SFLASH_MACRO_0_FREE_SFLASH228

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4E4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.580 SFLASH_MACRO_0_FREE_SFLASH229

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4E5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.581 SFLASH_MACRO_0_FREE_SFLASH230

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4E6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.582 SFLASH_MACRO_0_FREE_SFLASH231

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4E7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.583 SFLASH_MACRO_0_FREE_SFLASH232

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4E8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.584 SFLASH_MACRO_0_FREE_SFLASH233

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4E9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.585 SFLASH_MACRO_0_FREE_SFLASH234

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4EA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.586 SFLASH_MACRO_0_FREE_SFLASH235

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4EB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.587 SFLASH_MACRO_0_FREE_SFLASH236

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4EC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.588 SFLASH_MACRO_0_FREE_SFLASH237

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4ED

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.589 SFLASH_MACRO_0_FREE_SFLASH238

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4EE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.590 SFLASH_MACRO_0_FREE_SFLASH239

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4EF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.591 SFLASH_MACRO_0_FREE_SFLASH240

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4F0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.592 SFLASH_MACRO_0_FREE_SFLASH241

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4F1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.593 SFLASH_MACRO_0_FREE_SFLASH242

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4F2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.594 SFLASH_MACRO_0_FREE_SFLASH243

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4F3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.595 SFLASH_MACRO_0_FREE_SFLASH244

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4F4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.596 SFLASH_MACRO_0_FREE_SFLASH245

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4F5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.597 SFLASH_MACRO_0_FREE_SFLASH246

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4F6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.598 SFLASH_MACRO_0_FREE_SFLASH247

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4F7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.599 SFLASH_MACRO_0_FREE_SFLASH248

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4F8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.600 SFLASH_MACRO_0_FREE_SFLASH249

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4F9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.601 SFLASH_MACRO_0_FREE_SFLASH250

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4FA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.602 SFLASH_MACRO_0_FREE_SFLASH251

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4FB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.603 SFLASH_MACRO_0_FREE_SFLASH252

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4FC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.604 SFLASH_MACRO_0_FREE_SFLASH253

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4FD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.605 SFLASH_MACRO_0_FREE_SFLASH254

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4FE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.606 SFLASH_MACRO_0_FREE_SFLASH255

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF4FF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.607 SFLASH_MACRO_0_FREE_SFLASH256

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF500

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.608 SFLASH_MACRO_0_FREE_SFLASH257

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF501

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.609 SFLASH_MACRO_0_FREE_SFLASH258

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF502

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.610 SFLASH_MACRO_0_FREE_SFLASH259

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF503

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.611 SFLASH_MACRO_0_FREE_SFLASH260

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF504

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.612 SFLASH_MACRO_0_FREE_SFLASH261

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF505

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.613 SFLASH_MACRO_0_FREE_SFLASH262

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF506

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.614 SFLASH_MACRO_0_FREE_SFLASH263

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF507

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.615 SFLASH_MACRO_0_FREE_SFLASH264

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF508

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.616 SFLASH_MACRO_0_FREE_SFLASH265

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF509

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.617 SFLASH_MACRO_0_FREE_SFLASH266

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF50A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.618 SFLASH_MACRO_0_FREE_SFLASH267

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF50B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.619 SFLASH_MACRO_0_FREE_SFLASH268

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF50C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.620 SFLASH_MACRO_0_FREE_SFLASH269

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF50D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.621 SFLASH_MACRO_0_FREE_SFLASH270

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF50E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.622 SFLASH_MACRO_0_FREE_SFLASH271

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF50F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.623 SFLASH_MACRO_0_FREE_SFLASH272

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF510

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.624 SFLASH_MACRO_0_FREE_SFLASH273

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF511

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.625 SFLASH_MACRO_0_FREE_SFLASH274

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF512

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.626 SFLASH_MACRO_0_FREE_SFLASH275

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF513

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.627 SFLASH_MACRO_0_FREE_SFLASH276

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF514

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.628 SFLASH_MACRO_0_FREE_SFLASH277

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF515

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.629 SFLASH_MACRO_0_FREE_SFLASH278

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF516

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.630 SFLASH_MACRO_0_FREE_SFLASH279

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF517

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.631 SFLASH_MACRO_0_FREE_SFLASH280

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF518

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.632 SFLASH_MACRO_0_FREE_SFLASH281

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF519

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.633 SFLASH_MACRO_0_FREE_SFLASH282

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF51A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.634 SFLASH_MACRO_0_FREE_SFLASH283

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF51B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.635 SFLASH_MACRO_0_FREE_SFLASH284

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF51C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.636 SFLASH_MACRO_0_FREE_SFLASH285

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF51D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.637 SFLASH_MACRO_0_FREE_SFLASH286

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF51E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.638 SFLASH_MACRO_0_FREE_SFLASH287

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF51F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.639 SFLASH_MACRO_0_FREE_SFLASH288

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF520

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.640 SFLASH_MACRO_0_FREE_SFLASH289

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF521

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.641 SFLASH_MACRO_0_FREE_SFLASH290

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF522

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.642 SFLASH_MACRO_0_FREE_SFLASH291

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF523

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.643 SFLASH_MACRO_0_FREE_SFLASH292

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF524

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.644 SFLASH_MACRO_0_FREE_SFLASH293

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF525

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.645 SFLASH_MACRO_0_FREE_SFLASH294

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF526

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.646 SFLASH_MACRO_0_FREE_SFLASH295

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF527

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.647 SFLASH_MACRO_0_FREE_SFLASH296

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF528

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.648 SFLASH_MACRO_0_FREE_SFLASH297

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF529

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.649 SFLASH_MACRO_0_FREE_SFLASH298

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF52A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.650 SFLASH_MACRO_0_FREE_SFLASH299

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF52B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.651 SFLASH_MACRO_0_FREE_SFLASH300

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF52C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.652 SFLASH_MACRO_0_FREE_SFLASH301

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF52D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.653 SFLASH_MACRO_0_FREE_SFLASH302

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF52E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.654 SFLASH_MACRO_0_FREE_SFLASH303

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF52F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.655 SFLASH_MACRO_0_FREE_SFLASH304

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF530

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.656 SFLASH_MACRO_0_FREE_SFLASH305

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF531

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.657 SFLASH_MACRO_0_FREE_SFLASH306

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF532

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.658 SFLASH_MACRO_0_FREE_SFLASH307

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF533

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.659 SFLASH_MACRO_0_FREE_SFLASH308

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF534

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.660 SFLASH_MACRO_0_FREE_SFLASH309

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF535

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.661 SFLASH_MACRO_0_FREE_SFLASH310

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF536

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.662 SFLASH_MACRO_0_FREE_SFLASH311

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF537

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.663 SFLASH_MACRO_0_FREE_SFLASH312

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF538

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.664 SFLASH_MACRO_0_FREE_SFLASH313

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF539

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.665 SFLASH_MACRO_0_FREE_SFLASH314

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF53A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.666 SFLASH_MACRO_0_FREE_SFLASH315

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF53B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.667 SFLASH_MACRO_0_FREE_SFLASH316

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF53C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.668 SFLASH_MACRO_0_FREE_SFLASH317

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF53D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.669 SFLASH_MACRO_0_FREE_SFLASH318

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF53E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.670 SFLASH_MACRO_0_FREE_SFLASH319

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF53F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.671 SFLASH_MACRO_0_FREE_SFLASH320

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF540

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.672 SFLASH_MACRO_0_FREE_SFLASH321

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF541

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.673 SFLASH_MACRO_0_FREE_SFLASH322

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF542

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.674 SFLASH_MACRO_0_FREE_SFLASH323

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF543

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.675 SFLASH_MACRO_0_FREE_SFLASH324

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF544

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.676 SFLASH_MACRO_0_FREE_SFLASH325

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF545

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.677 SFLASH_MACRO_0_FREE_SFLASH326

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF546

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.678 SFLASH_MACRO_0_FREE_SFLASH327

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF547

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.679 SFLASH_MACRO_0_FREE_SFLASH328

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF548

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.680 SFLASH_MACRO_0_FREE_SFLASH329

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF549

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.681 SFLASH_MACRO_0_FREE_SFLASH330

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF54A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.682 SFLASH_MACRO_0_FREE_SFLASH331

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF54B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.683 SFLASH_MACRO_0_FREE_SFLASH332

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF54C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.684 SFLASH_MACRO_0_FREE_SFLASH333

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF54D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.685 SFLASH_MACRO_0_FREE_SFLASH334

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF54E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.686 SFLASH_MACRO_0_FREE_SFLASH335

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF54F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.687 SFLASH_MACRO_0_FREE_SFLASH336

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF550

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.688 SFLASH_MACRO_0_FREE_SFLASH337

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF551

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.689 SFLASH_MACRO_0_FREE_SFLASH338

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF552

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.690 SFLASH_MACRO_0_FREE_SFLASH339

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF553

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.691 SFLASH_MACRO_0_FREE_SFLASH340

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF554

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.692 SFLASH_MACRO_0_FREE_SFLASH341

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF555

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.693 SFLASH_MACRO_0_FREE_SFLASH342

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF556

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.694 SFLASH_MACRO_0_FREE_SFLASH343

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF557

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.695 SFLASH_MACRO_0_FREE_SFLASH344

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF558

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.696 SFLASH_MACRO_0_FREE_SFLASH345

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF559

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.697 SFLASH_MACRO_0_FREE_SFLASH346

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF55A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.698 SFLASH_MACRO_0_FREE_SFLASH347

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF55B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.699 SFLASH_MACRO_0_FREE_SFLASH348

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF55C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.700 SFLASH_MACRO_0_FREE_SFLASH349

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF55D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.701 SFLASH_MACRO_0_FREE_SFLASH350

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF55E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.702 SFLASH_MACRO_0_FREE_SFLASH351

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF55F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.703 SFLASH_MACRO_0_FREE_SFLASH352

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF560

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.704 SFLASH_MACRO_0_FREE_SFLASH353

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF561

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.705 SFLASH_MACRO_0_FREE_SFLASH354

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF562

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.706 SFLASH_MACRO_0_FREE_SFLASH355

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF563

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.707 SFLASH_MACRO_0_FREE_SFLASH356

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF564

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.708 SFLASH_MACRO_0_FREE_SFLASH357

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF565

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.709 SFLASH_MACRO_0_FREE_SFLASH358

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF566

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.710 SFLASH_MACRO_0_FREE_SFLASH359

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF567

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.711 SFLASH_MACRO_0_FREE_SFLASH360

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF568

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.712 SFLASH_MACRO_0_FREE_SFLASH361

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF569

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.713 SFLASH_MACRO_0_FREE_SFLASH362

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF56A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.714 SFLASH_MACRO_0_FREE_SFLASH363

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF56B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.715 SFLASH_MACRO_0_FREE_SFLASH364

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF56C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.716 SFLASH_MACRO_0_FREE_SFLASH365

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF56D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.717 SFLASH_MACRO_0_FREE_SFLASH366

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF56E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.718 SFLASH_MACRO_0_FREE_SFLASH367

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF56F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.719 SFLASH_MACRO_0_FREE_SFLASH368

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF570

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.720 SFLASH_MACRO_0_FREE_SFLASH369

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF571

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.721 SFLASH_MACRO_0_FREE_SFLASH370

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF572

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.722 SFLASH_MACRO_0_FREE_SFLASH371

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF573

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.723 SFLASH_MACRO_0_FREE_SFLASH372

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF574

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.724 SFLASH_MACRO_0_FREE_SFLASH373

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF575

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.725 SFLASH_MACRO_0_FREE_SFLASH374

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF576

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.726 SFLASH_MACRO_0_FREE_SFLASH375

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF577

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.727 SFLASH_MACRO_0_FREE_SFLASH376

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF578

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.728 SFLASH_MACRO_0_FREE_SFLASH377

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF579

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.729 SFLASH_MACRO_0_FREE_SFLASH378

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF57A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.730 SFLASH_MACRO_0_FREE_SFLASH379

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF57B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.731 SFLASH_MACRO_0_FREE_SFLASH380

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF57C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.732 SFLASH_MACRO_0_FREE_SFLASH381

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF57D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.733 SFLASH_MACRO_0_FREE_SFLASH382

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF57E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.734 SFLASH_MACRO_0_FREE_SFLASH383

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF57F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.735 SFLASH_MACRO_0_FREE_SFLASH384

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF580

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.736 SFLASH_MACRO_0_FREE_SFLASH385

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF581

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.737 SFLASH_MACRO_0_FREE_SFLASH386

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF582

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.738 SFLASH_MACRO_0_FREE_SFLASH387

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF583

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.739 SFLASH_MACRO_0_FREE_SFLASH388

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF584

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.740 SFLASH_MACRO_0_FREE_SFLASH389

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF585

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.741 SFLASH_MACRO_0_FREE_SFLASH390

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF586

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.742 SFLASH_MACRO_0_FREE_SFLASH391

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF587

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.743 SFLASH_MACRO_0_FREE_SFLASH392

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF588

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.744 SFLASH_MACRO_0_FREE_SFLASH393

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF589

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.745 SFLASH_MACRO_0_FREE_SFLASH394

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF58A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.746 SFLASH_MACRO_0_FREE_SFLASH395

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF58B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.747 SFLASH_MACRO_0_FREE_SFLASH396

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF58C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.748 SFLASH_MACRO_0_FREE_SFLASH397

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF58D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.749 SFLASH_MACRO_0_FREE_SFLASH398

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF58E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.750 SFLASH_MACRO_0_FREE_SFLASH399

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF58F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.751 SFLASH_MACRO_0_FREE_SFLASH400

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF590

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.752 SFLASH_MACRO_0_FREE_SFLASH401

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF591

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.753 SFLASH_MACRO_0_FREE_SFLASH402

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF592

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.754 SFLASH_MACRO_0_FREE_SFLASH403

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF593

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.755 SFLASH_MACRO_0_FREE_SFLASH404

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF594

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.756 SFLASH_MACRO_0_FREE_SFLASH405

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF595

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.757 SFLASH_MACRO_0_FREE_SFLASH406

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF596

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.758 SFLASH_MACRO_0_FREE_SFLASH407

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF597

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.759 SFLASH_MACRO_0_FREE_SFLASH408

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF598

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.760 SFLASH_MACRO_0_FREE_SFLASH409

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF599

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.761 SFLASH_MACRO_0_FREE_SFLASH410

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF59A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.762 SFLASH_MACRO_0_FREE_SFLASH411

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF59B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.763 SFLASH_MACRO_0_FREE_SFLASH412

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF59C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.764 SFLASH_MACRO_0_FREE_SFLASH413

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF59D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.765 SFLASH_MACRO_0_FREE_SFLASH414

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF59E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.766 SFLASH_MACRO_0_FREE_SFLASH415

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF59F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.767 SFLASH_MACRO_0_FREE_SFLASH416

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.768 SFLASH_MACRO_0_FREE_SFLASH417

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5A1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.769 SFLASH_MACRO_0_FREE_SFLASH418

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5A2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.770 SFLASH_MACRO_0_FREE_SFLASH419

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5A3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.771 SFLASH_MACRO_0_FREE_SFLASH420

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5A4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.772 SFLASH_MACRO_0_FREE_SFLASH421

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5A5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.773 SFLASH_MACRO_0_FREE_SFLASH422

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5A6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.774 SFLASH_MACRO_0_FREE_SFLASH423

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5A7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.775 SFLASH_MACRO_0_FREE_SFLASH424

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5A8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.776 SFLASH_MACRO_0_FREE_SFLASH425

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5A9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.777 SFLASH_MACRO_0_FREE_SFLASH426

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5AA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.778 SFLASH_MACRO_0_FREE_SFLASH427

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5AB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.779 SFLASH_MACRO_0_FREE_SFLASH428

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5AC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.780 SFLASH_MACRO_0_FREE_SFLASH429

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5AD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.781 SFLASH_MACRO_0_FREE_SFLASH430

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5AE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.782 SFLASH_MACRO_0_FREE_SFLASH431

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5AF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.783 SFLASH_MACRO_0_FREE_SFLASH432

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5B0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.784 SFLASH_MACRO_0_FREE_SFLASH433

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5B1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.785 SFLASH_MACRO_0_FREE_SFLASH434

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5B2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.786 SFLASH_MACRO_0_FREE_SFLASH435

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5B3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.787 SFLASH_MACRO_0_FREE_SFLASH436

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5B4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.788 SFLASH_MACRO_0_FREE_SFLASH437

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5B5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.789 SFLASH_MACRO_0_FREE_SFLASH438

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5B6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.790 SFLASH_MACRO_0_FREE_SFLASH439

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5B7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.791 SFLASH_MACRO_0_FREE_SFLASH440

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5B8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.792 SFLASH_MACRO_0_FREE_SFLASH441

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5B9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.793 SFLASH_MACRO_0_FREE_SFLASH442

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5BA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.794 SFLASH_MACRO_0_FREE_SFLASH443

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5BB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.795 SFLASH_MACRO_0_FREE_SFLASH444

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5BC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.796 SFLASH_MACRO_0_FREE_SFLASH445

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5BD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.797 SFLASH_MACRO_0_FREE_SFLASH446

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5BE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.798 SFLASH_MACRO_0_FREE_SFLASH447

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5BF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.799 SFLASH_MACRO_0_FREE_SFLASH448

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.800 SFLASH_MACRO_0_FREE_SFLASH449

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5C1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.801 SFLASH_MACRO_0_FREE_SFLASH450

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5C2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.802 SFLASH_MACRO_0_FREE_SFLASH451

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5C3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.803 SFLASH_MACRO_0_FREE_SFLASH452

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.804 SFLASH_MACRO_0_FREE_SFLASH453

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5C5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.805 SFLASH_MACRO_0_FREE_SFLASH454

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5C6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.806 SFLASH_MACRO_0_FREE_SFLASH455

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5C7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.807 SFLASH_MACRO_0_FREE_SFLASH456

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5C8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.808 SFLASH_MACRO_0_FREE_SFLASH457

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5C9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.809 SFLASH_MACRO_0_FREE_SFLASH458

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5CA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.810 SFLASH_MACRO_0_FREE_SFLASH459

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5CB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.811 SFLASH_MACRO_0_FREE_SFLASH460

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5CC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.812 SFLASH_MACRO_0_FREE_SFLASH461

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5CD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.813 SFLASH_MACRO_0_FREE_SFLASH462

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5CE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.814 SFLASH_MACRO_0_FREE_SFLASH463

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5CF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.815 SFLASH_MACRO_0_FREE_SFLASH464

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5D0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.816 SFLASH_MACRO_0_FREE_SFLASH465

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5D1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.817 SFLASH_MACRO_0_FREE_SFLASH466

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5D2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.818 SFLASH_MACRO_0_FREE_SFLASH467

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5D3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.819 SFLASH_MACRO_0_FREE_SFLASH468

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5D4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.820 SFLASH_MACRO_0_FREE_SFLASH469

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5D5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.821 SFLASH_MACRO_0_FREE_SFLASH470

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5D6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.822 SFLASH_MACRO_0_FREE_SFLASH471

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5D7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.823 SFLASH_MACRO_0_FREE_SFLASH472

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5D8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.824 SFLASH_MACRO_0_FREE_SFLASH473

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5D9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.825 SFLASH_MACRO_0_FREE_SFLASH474

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5DA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.826 SFLASH_MACRO_0_FREE_SFLASH475

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5DB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.827 SFLASH_MACRO_0_FREE_SFLASH476

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5DC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.828 SFLASH_MACRO_0_FREE_SFLASH477

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5DD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.829 SFLASH_MACRO_0_FREE_SFLASH478

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5DE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.830 SFLASH_MACRO_0_FREE_SFLASH479

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5DF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.831 SFLASH_MACRO_0_FREE_SFLASH480

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.832 SFLASH_MACRO_0_FREE_SFLASH481

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5E1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.833 SFLASH_MACRO_0_FREE_SFLASH482

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5E2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.834 SFLASH_MACRO_0_FREE_SFLASH483

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5E3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.835 SFLASH_MACRO_0_FREE_SFLASH484

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5E4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.836 SFLASH_MACRO_0_FREE_SFLASH485

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5E5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.837 SFLASH_MACRO_0_FREE_SFLASH486

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5E6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.838 SFLASH_MACRO_0_FREE_SFLASH487

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5E7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.839 SFLASH_MACRO_0_FREE_SFLASH488

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5E8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.840 SFLASH_MACRO_0_FREE_SFLASH489

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5E9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.841 SFLASH_MACRO_0_FREE_SFLASH490

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5EA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.842 SFLASH_MACRO_0_FREE_SFLASH491

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5EB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.843 SFLASH_MACRO_0_FREE_SFLASH492

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5EC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.844 SFLASH_MACRO_0_FREE_SFLASH493

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5ED

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.845 SFLASH_MACRO_0_FREE_SFLASH494

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5EE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.846 SFLASH_MACRO_0_FREE_SFLASH495

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5EF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.847 SFLASH_MACRO_0_FREE_SFLASH496

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5F0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.848 SFLASH_MACRO_0_FREE_SFLASH497

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5F1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.849 SFLASH_MACRO_0_FREE_SFLASH498

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5F2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.850 SFLASH_MACRO_0_FREE_SFLASH499

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5F3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.851 SFLASH_MACRO_0_FREE_SFLASH500

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5F4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.852 SFLASH_MACRO_0_FREE_SFLASH501

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5F5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.853 SFLASH_MACRO_0_FREE_SFLASH502

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5F6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.854 SFLASH_MACRO_0_FREE_SFLASH503

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5F7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.855 SFLASH_MACRO_0_FREE_SFLASH504

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5F8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.856 SFLASH_MACRO_0_FREE_SFLASH505

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5F9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.857 SFLASH_MACRO_0_FREE_SFLASH506

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5FA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.858 SFLASH_MACRO_0_FREE_SFLASH507

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5FB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.859 SFLASH_MACRO_0_FREE_SFLASH508

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5FC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.860 SFLASH_MACRO_0_FREE_SFLASH509

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5FD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.861 SFLASH_MACRO_0_FREE_SFLASH510

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5FE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.862 SFLASH_MACRO_0_FREE_SFLASH511

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF5FF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.863 SFLASH_MACRO_0_FREE_SFLASH512

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF600

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.864 SFLASH_MACRO_0_FREE_SFLASH513

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF601

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.865 SFLASH_MACRO_0_FREE_SFLASH514

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF602

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.866 SFLASH_MACRO_0_FREE_SFLASH515

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF603

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.867 SFLASH_MACRO_0_FREE_SFLASH516

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF604

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.868 SFLASH_MACRO_0_FREE_SFLASH517

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF605

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.869 SFLASH_MACRO_0_FREE_SFLASH518

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF606

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.870 SFLASH_MACRO_0_FREE_SFLASH519

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF607

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.871 SFLASH_MACRO_0_FREE_SFLASH520

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF608

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.872 SFLASH_MACRO_0_FREE_SFLASH521

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF609

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.873 SFLASH_MACRO_0_FREE_SFLASH522

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF60A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.874 SFLASH_MACRO_0_FREE_SFLASH523

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF60B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.875 SFLASH_MACRO_0_FREE_SFLASH524

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF60C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.876 SFLASH_MACRO_0_FREE_SFLASH525

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF60D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.877 SFLASH_MACRO_0_FREE_SFLASH526

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF60E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.878 SFLASH_MACRO_0_FREE_SFLASH527

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF60F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.879 SFLASH_MACRO_0_FREE_SFLASH528

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF610

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.880 SFLASH_MACRO_0_FREE_SFLASH529

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF611

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.881 SFLASH_MACRO_0_FREE_SFLASH530

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF612

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.882 SFLASH_MACRO_0_FREE_SFLASH531

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF613

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.883 SFLASH_MACRO_0_FREE_SFLASH532

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF614

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.884 SFLASH_MACRO_0_FREE_SFLASH533

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF615

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.885 SFLASH_MACRO_0_FREE_SFLASH534

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF616

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.886 SFLASH_MACRO_0_FREE_SFLASH535

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF617

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.887 SFLASH_MACRO_0_FREE_SFLASH536

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF618

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.888 SFLASH_MACRO_0_FREE_SFLASH537

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF619

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.889 SFLASH_MACRO_0_FREE_SFLASH538

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF61A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.890 SFLASH_MACRO_0_FREE_SFLASH539

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF61B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.891 SFLASH_MACRO_0_FREE_SFLASH540

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF61C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.892 SFLASH_MACRO_0_FREE_SFLASH541

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF61D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.893 SFLASH_MACRO_0_FREE_SFLASH542

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF61E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.894 SFLASH_MACRO_0_FREE_SFLASH543

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF61F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.895 SFLASH_MACRO_0_FREE_SFLASH544

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF620

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.896 SFLASH_MACRO_0_FREE_SFLASH545

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF621

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.897 SFLASH_MACRO_0_FREE_SFLASH546

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF622

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.898 SFLASH_MACRO_0_FREE_SFLASH547

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF623

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.899 SFLASH_MACRO_0_FREE_SFLASH548

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF624

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.900 SFLASH_MACRO_0_FREE_SFLASH549

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF625

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.901 SFLASH_MACRO_0_FREE_SFLASH550

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF626

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.902 SFLASH_MACRO_0_FREE_SFLASH551

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF627

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.903 SFLASH_MACRO_0_FREE_SFLASH552

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF628

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.904 SFLASH_MACRO_0_FREE_SFLASH553

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF629

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.905 SFLASH_MACRO_0_FREE_SFLASH554

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF62A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.906 SFLASH_MACRO_0_FREE_SFLASH555

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF62B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.907 SFLASH_MACRO_0_FREE_SFLASH556

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF62C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.908 SFLASH_MACRO_0_FREE_SFLASH557

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF62D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.909 SFLASH_MACRO_0_FREE_SFLASH558

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF62E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.910 SFLASH_MACRO_0_FREE_SFLASH559

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF62F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.911 SFLASH_MACRO_0_FREE_SFLASH560

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF630

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.912 SFLASH_MACRO_0_FREE_SFLASH561

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF631

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.913 SFLASH_MACRO_0_FREE_SFLASH562

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF632

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.914 SFLASH_MACRO_0_FREE_SFLASH563

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF633

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.915 SFLASH_MACRO_0_FREE_SFLASH564

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF634

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.916 SFLASH_MACRO_0_FREE_SFLASH565

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF635

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.917 SFLASH_MACRO_0_FREE_SFLASH566

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF636

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.918 SFLASH_MACRO_0_FREE_SFLASH567

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF637

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.919 SFLASH_MACRO_0_FREE_SFLASH568

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF638

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.920 SFLASH_MACRO_0_FREE_SFLASH569

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF639

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.921 SFLASH_MACRO_0_FREE_SFLASH570

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF63A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.922 SFLASH_MACRO_0_FREE_SFLASH571

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF63B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.923 SFLASH_MACRO_0_FREE_SFLASH572

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF63C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.924 SFLASH_MACRO_0_FREE_SFLASH573

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF63D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.925 SFLASH_MACRO_0_FREE_SFLASH574

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF63E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.926 SFLASH_MACRO_0_FREE_SFLASH575

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF63F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.927 SFLASH_MACRO_0_FREE_SFLASH576

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF640

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.928 SFLASH_MACRO_0_FREE_SFLASH577

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF641

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.929 SFLASH_MACRO_0_FREE_SFLASH578

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF642

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.930 SFLASH_MACRO_0_FREE_SFLASH579

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF643

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.931 SFLASH_MACRO_0_FREE_SFLASH580

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF644

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.932 SFLASH_MACRO_0_FREE_SFLASH581

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF645

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.933 SFLASH_MACRO_0_FREE_SFLASH582

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF646

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.934 SFLASH_MACRO_0_FREE_SFLASH583

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF647

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.935 SFLASH_MACRO_0_FREE_SFLASH584

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF648

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.936 SFLASH_MACRO_0_FREE_SFLASH585

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF649

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.937 SFLASH_MACRO_0_FREE_SFLASH586

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF64A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.938 SFLASH_MACRO_0_FREE_SFLASH587

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF64B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.939 SFLASH_MACRO_0_FREE_SFLASH588

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF64C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.940 SFLASH_MACRO_0_FREE_SFLASH589

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF64D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.941 SFLASH_MACRO_0_FREE_SFLASH590

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF64E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.942 SFLASH_MACRO_0_FREE_SFLASH591

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF64F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.943 SFLASH_MACRO_0_FREE_SFLASH592

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF650

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.944 SFLASH_MACRO_0_FREE_SFLASH593

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF651

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.945 SFLASH_MACRO_0_FREE_SFLASH594

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF652

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.946 SFLASH_MACRO_0_FREE_SFLASH595

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF653

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.947 SFLASH_MACRO_0_FREE_SFLASH596

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF654

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.948 SFLASH_MACRO_0_FREE_SFLASH597

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF655

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.949 SFLASH_MACRO_0_FREE_SFLASH598

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF656

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.950 SFLASH_MACRO_0_FREE_SFLASH599

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF657

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.951 SFLASH_MACRO_0_FREE_SFLASH600

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF658

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.952 SFLASH_MACRO_0_FREE_SFLASH601

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF659

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.953 SFLASH_MACRO_0_FREE_SFLASH602

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF65A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.954 SFLASH_MACRO_0_FREE_SFLASH603

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF65B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.955 SFLASH_MACRO_0_FREE_SFLASH604

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF65C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.956 SFLASH_MACRO_0_FREE_SFLASH605

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF65D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.957 SFLASH_MACRO_0_FREE_SFLASH606

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF65E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.958 SFLASH_MACRO_0_FREE_SFLASH607

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF65F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.959 SFLASH_MACRO_0_FREE_SFLASH608

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF660

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.960 SFLASH_MACRO_0_FREE_SFLASH609

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF661

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.961 SFLASH_MACRO_0_FREE_SFLASH610

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF662

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.962 SFLASH_MACRO_0_FREE_SFLASH611

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF663

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.963 SFLASH_MACRO_0_FREE_SFLASH612

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF664

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.964 SFLASH_MACRO_0_FREE_SFLASH613

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF665

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.965 SFLASH_MACRO_0_FREE_SFLASH614

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF666

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.966 SFLASH_MACRO_0_FREE_SFLASH615

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF667

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.967 SFLASH_MACRO_0_FREE_SFLASH616

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF668

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.968 SFLASH_MACRO_0_FREE_SFLASH617

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF669

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.969 SFLASH_MACRO_0_FREE_SFLASH618

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF66A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.970 SFLASH_MACRO_0_FREE_SFLASH619

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF66B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.971 SFLASH_MACRO_0_FREE_SFLASH620

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF66C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.972 SFLASH_MACRO_0_FREE_SFLASH621

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF66D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.973 SFLASH_MACRO_0_FREE_SFLASH622

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF66E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.974 SFLASH_MACRO_0_FREE_SFLASH623

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF66F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.975 SFLASH_MACRO_0_FREE_SFLASH624

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF670

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.976 SFLASH_MACRO_0_FREE_SFLASH625

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF671

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.977 SFLASH_MACRO_0_FREE_SFLASH626

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF672

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.978 SFLASH_MACRO_0_FREE_SFLASH627

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF673

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.979 SFLASH_MACRO_0_FREE_SFLASH628

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF674

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.980 SFLASH_MACRO_0_FREE_SFLASH629

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF675

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.981 SFLASH_MACRO_0_FREE_SFLASH630

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF676

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.982 SFLASH_MACRO_0_FREE_SFLASH631

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF677

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.983 SFLASH_MACRO_0_FREE_SFLASH632

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF678

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.984 SFLASH_MACRO_0_FREE_SFLASH633

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF679

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.985 SFLASH_MACRO_0_FREE_SFLASH634

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF67A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.986 SFLASH_MACRO_0_FREE_SFLASH635

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF67B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.987 SFLASH_MACRO_0_FREE_SFLASH636

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF67C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.988 SFLASH_MACRO_0_FREE_SFLASH637

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF67D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.989 SFLASH_MACRO_0_FREE_SFLASH638

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF67E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.990 SFLASH_MACRO_0_FREE_SFLASH639

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF67F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.991 SFLASH_MACRO_0_FREE_SFLASH640

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF680

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.992 SFLASH_MACRO_0_FREE_SFLASH641

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF681

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.993 SFLASH_MACRO_0_FREE_SFLASH642

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF682

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.994 SFLASH_MACRO_0_FREE_SFLASH643

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF683

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.995 SFLASH_MACRO_0_FREE_SFLASH644

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF684

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.996 SFLASH_MACRO_0_FREE_SFLASH645

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF685

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.997 SFLASH_MACRO_0_FREE_SFLASH646

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF686

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.998 SFLASH_MACRO_0_FREE_SFLASH647

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF687

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.999 SFLASH_MACRO_0_FREE_SFLASH648

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF688

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1000SFLASH_MACRO_0_FREE_SFLASH649

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF689

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1001SFLASH_MACRO_0_FREE_SFLASH650

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF68A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1002SFLASH_MACRO_0_FREE_SFLASH651

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF68B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1003SFLASH_MACRO_0_FREE_SFLASH652

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF68C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1004SFLASH_MACRO_0_FREE_SFLASH653

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF68D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1005SFLASH_MACRO_0_FREE_SFLASH654

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF68E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1006SFLASH_MACRO_0_FREE_SFLASH655

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF68F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1007SFLASH_MACRO_0_FREE_SFLASH656

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF690

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1008SFLASH_MACRO_0_FREE_SFLASH657

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF691

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1009SFLASH_MACRO_0_FREE_SFLASH658

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF692

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1010SFLASH_MACRO_0_FREE_SFLASH659

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF693

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1011SFLASH_MACRO_0_FREE_SFLASH660

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF694

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1012SFLASH_MACRO_0_FREE_SFLASH661

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF695

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1013SFLASH_MACRO_0_FREE_SFLASH662

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF696

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1014SFLASH_MACRO_0_FREE_SFLASH663

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF697

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1015SFLASH_MACRO_0_FREE_SFLASH664

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF698

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1016SFLASH_MACRO_0_FREE_SFLASH665

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF699

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1017SFLASH_MACRO_0_FREE_SFLASH666

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF69A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1018SFLASH_MACRO_0_FREE_SFLASH667

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF69B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1019SFLASH_MACRO_0_FREE_SFLASH668

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF69C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1020SFLASH_MACRO_0_FREE_SFLASH669

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF69D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1021SFLASH_MACRO_0_FREE_SFLASH670

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF69E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1022SFLASH_MACRO_0_FREE_SFLASH671

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF69F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1023SFLASH_MACRO_0_FREE_SFLASH672

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1024SFLASH_MACRO_0_FREE_SFLASH673

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6A1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1025SFLASH_MACRO_0_FREE_SFLASH674

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6A2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1026SFLASH_MACRO_0_FREE_SFLASH675

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6A3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1027SFLASH_MACRO_0_FREE_SFLASH676

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6A4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1028SFLASH_MACRO_0_FREE_SFLASH677

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6A5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1029SFLASH_MACRO_0_FREE_SFLASH678

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6A6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1030SFLASH_MACRO_0_FREE_SFLASH679

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6A7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1031SFLASH_MACRO_0_FREE_SFLASH680

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6A8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1032SFLASH_MACRO_0_FREE_SFLASH681

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6A9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1033SFLASH_MACRO_0_FREE_SFLASH682

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6AA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1034SFLASH_MACRO_0_FREE_SFLASH683

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6AB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1035SFLASH_MACRO_0_FREE_SFLASH684

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6AC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1036SFLASH_MACRO_0_FREE_SFLASH685

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6AD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1037SFLASH_MACRO_0_FREE_SFLASH686

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6AE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1038SFLASH_MACRO_0_FREE_SFLASH687

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6AF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1039SFLASH_MACRO_0_FREE_SFLASH688

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6B0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1040SFLASH_MACRO_0_FREE_SFLASH689

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6B1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1041SFLASH_MACRO_0_FREE_SFLASH690

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6B2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1042SFLASH_MACRO_0_FREE_SFLASH691

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6B3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1043SFLASH_MACRO_0_FREE_SFLASH692

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6B4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1044SFLASH_MACRO_0_FREE_SFLASH693

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6B5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1045SFLASH_MACRO_0_FREE_SFLASH694

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6B6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1046SFLASH_MACRO_0_FREE_SFLASH695

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6B7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1047SFLASH_MACRO_0_FREE_SFLASH696

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6B8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1048SFLASH_MACRO_0_FREE_SFLASH697

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6B9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1049SFLASH_MACRO_0_FREE_SFLASH698

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6BA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1050SFLASH_MACRO_0_FREE_SFLASH699

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6BB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1051SFLASH_MACRO_0_FREE_SFLASH700

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6BC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1052SFLASH_MACRO_0_FREE_SFLASH701

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6BD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1053SFLASH_MACRO_0_FREE_SFLASH702

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6BE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1054SFLASH_MACRO_0_FREE_SFLASH703

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6BF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1055SFLASH_MACRO_0_FREE_SFLASH704

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1056SFLASH_MACRO_0_FREE_SFLASH705

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6C1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1057SFLASH_MACRO_0_FREE_SFLASH706

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6C2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1058SFLASH_MACRO_0_FREE_SFLASH707

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6C3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1059SFLASH_MACRO_0_FREE_SFLASH708

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1060SFLASH_MACRO_0_FREE_SFLASH709

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6C5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1061SFLASH_MACRO_0_FREE_SFLASH710

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6C6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1062SFLASH_MACRO_0_FREE_SFLASH711

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6C7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1063SFLASH_MACRO_0_FREE_SFLASH712

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6C8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1064SFLASH_MACRO_0_FREE_SFLASH713

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6C9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1065SFLASH_MACRO_0_FREE_SFLASH714

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6CA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1066SFLASH_MACRO_0_FREE_SFLASH715

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6CB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1067SFLASH_MACRO_0_FREE_SFLASH716

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6CC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1068SFLASH_MACRO_0_FREE_SFLASH717

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6CD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1069SFLASH_MACRO_0_FREE_SFLASH718

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6CE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1070SFLASH_MACRO_0_FREE_SFLASH719

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6CF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1071SFLASH_MACRO_0_FREE_SFLASH720

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6D0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1072SFLASH_MACRO_0_FREE_SFLASH721

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6D1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1073SFLASH_MACRO_0_FREE_SFLASH722

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6D2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1074SFLASH_MACRO_0_FREE_SFLASH723

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6D3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1075SFLASH_MACRO_0_FREE_SFLASH724

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6D4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1076SFLASH_MACRO_0_FREE_SFLASH725

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6D5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1077SFLASH_MACRO_0_FREE_SFLASH726

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6D6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1078SFLASH_MACRO_0_FREE_SFLASH727

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6D7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1079SFLASH_MACRO_0_FREE_SFLASH728

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6D8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1080SFLASH_MACRO_0_FREE_SFLASH729

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6D9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1081SFLASH_MACRO_0_FREE_SFLASH730

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6DA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1082SFLASH_MACRO_0_FREE_SFLASH731

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6DB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1083SFLASH_MACRO_0_FREE_SFLASH732

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6DC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1084SFLASH_MACRO_0_FREE_SFLASH733

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6DD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1085SFLASH_MACRO_0_FREE_SFLASH734

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6DE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1086SFLASH_MACRO_0_FREE_SFLASH735

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6DF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1087SFLASH_MACRO_0_FREE_SFLASH736

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1088SFLASH_MACRO_0_FREE_SFLASH737

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6E1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1089SFLASH_MACRO_0_FREE_SFLASH738

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6E2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1090SFLASH_MACRO_0_FREE_SFLASH739

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6E3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1091SFLASH_MACRO_0_FREE_SFLASH740

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6E4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1092SFLASH_MACRO_0_FREE_SFLASH741

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6E5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1093SFLASH_MACRO_0_FREE_SFLASH742

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6E6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1094SFLASH_MACRO_0_FREE_SFLASH743

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6E7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1095SFLASH_MACRO_0_FREE_SFLASH744

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6E8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1096SFLASH_MACRO_0_FREE_SFLASH745

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6E9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1097SFLASH_MACRO_0_FREE_SFLASH746

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6EA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1098SFLASH_MACRO_0_FREE_SFLASH747

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6EB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1099SFLASH_MACRO_0_FREE_SFLASH748

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6EC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1100SFLASH_MACRO_0_FREE_SFLASH749

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6ED

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1101SFLASH_MACRO_0_FREE_SFLASH750

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6EE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1102SFLASH_MACRO_0_FREE_SFLASH751

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6EF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1103SFLASH_MACRO_0_FREE_SFLASH752

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6F0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1104SFLASH_MACRO_0_FREE_SFLASH753

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6F1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1105SFLASH_MACRO_0_FREE_SFLASH754

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6F2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1106SFLASH_MACRO_0_FREE_SFLASH755

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6F3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1107SFLASH_MACRO_0_FREE_SFLASH756

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6F4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1108SFLASH_MACRO_0_FREE_SFLASH757

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6F5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1109SFLASH_MACRO_0_FREE_SFLASH758

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6F6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1110SFLASH_MACRO_0_FREE_SFLASH759

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6F7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1111 SFLASH_MACRO_0_FREE_SFLASH760

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6F8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1112SFLASH_MACRO_0_FREE_SFLASH761

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6F9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1113SFLASH_MACRO_0_FREE_SFLASH762

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6FA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1114SFLASH_MACRO_0_FREE_SFLASH763

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6FB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1115SFLASH_MACRO_0_FREE_SFLASH764

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6FC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1116SFLASH_MACRO_0_FREE_SFLASH765

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6FD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1117SFLASH_MACRO_0_FREE_SFLASH766

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6FE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1118SFLASH_MACRO_0_FREE_SFLASH767

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF6FF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1119SFLASH_MACRO_0_FREE_SFLASH768

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF700

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1120SFLASH_MACRO_0_FREE_SFLASH769

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF701

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1121SFLASH_MACRO_0_FREE_SFLASH770

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF702

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1122SFLASH_MACRO_0_FREE_SFLASH771

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF703

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1123SFLASH_MACRO_0_FREE_SFLASH772

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF704

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1124SFLASH_MACRO_0_FREE_SFLASH773

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF705

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1125SFLASH_MACRO_0_FREE_SFLASH774

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF706

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1126SFLASH_MACRO_0_FREE_SFLASH775

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF707

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1127SFLASH_MACRO_0_FREE_SFLASH776

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF708

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1128SFLASH_MACRO_0_FREE_SFLASH777

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF709

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1129SFLASH_MACRO_0_FREE_SFLASH778

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF70A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1130SFLASH_MACRO_0_FREE_SFLASH779

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF70B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1131SFLASH_MACRO_0_FREE_SFLASH780

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF70C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1132SFLASH_MACRO_0_FREE_SFLASH781

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF70D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1133SFLASH_MACRO_0_FREE_SFLASH782

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF70E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1134SFLASH_MACRO_0_FREE_SFLASH783

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF70F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1135SFLASH_MACRO_0_FREE_SFLASH784

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF710

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1136SFLASH_MACRO_0_FREE_SFLASH785

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF711

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1137SFLASH_MACRO_0_FREE_SFLASH786

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF712

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1138SFLASH_MACRO_0_FREE_SFLASH787

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF713

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1139SFLASH_MACRO_0_FREE_SFLASH788

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF714

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1140SFLASH_MACRO_0_FREE_SFLASH789

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF715

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1141SFLASH_MACRO_0_FREE_SFLASH790

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF716

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1142SFLASH_MACRO_0_FREE_SFLASH791

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF717

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1143SFLASH_MACRO_0_FREE_SFLASH792

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF718

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1144SFLASH_MACRO_0_FREE_SFLASH793

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF719

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1145SFLASH_MACRO_0_FREE_SFLASH794

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF71A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1146SFLASH_MACRO_0_FREE_SFLASH795

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF71B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1147SFLASH_MACRO_0_FREE_SFLASH796

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF71C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1148SFLASH_MACRO_0_FREE_SFLASH797

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF71D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1149SFLASH_MACRO_0_FREE_SFLASH798

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF71E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1150SFLASH_MACRO_0_FREE_SFLASH799

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF71F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1151SFLASH_MACRO_0_FREE_SFLASH800

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF720

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1152SFLASH_MACRO_0_FREE_SFLASH801

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF721

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1153SFLASH_MACRO_0_FREE_SFLASH802

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF722

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1154SFLASH_MACRO_0_FREE_SFLASH803

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF723

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1155SFLASH_MACRO_0_FREE_SFLASH804

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF724

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1156SFLASH_MACRO_0_FREE_SFLASH805

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF725

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1157SFLASH_MACRO_0_FREE_SFLASH806

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF726

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1158SFLASH_MACRO_0_FREE_SFLASH807

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF727

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1159SFLASH_MACRO_0_FREE_SFLASH808

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF728

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1160SFLASH_MACRO_0_FREE_SFLASH809

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF729

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1161SFLASH_MACRO_0_FREE_SFLASH810

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF72A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1162SFLASH_MACRO_0_FREE_SFLASH811

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF72B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1163SFLASH_MACRO_0_FREE_SFLASH812

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF72C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1164SFLASH_MACRO_0_FREE_SFLASH813

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF72D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1165SFLASH_MACRO_0_FREE_SFLASH814

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF72E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1166SFLASH_MACRO_0_FREE_SFLASH815

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF72F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1167SFLASH_MACRO_0_FREE_SFLASH816

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF730

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1168SFLASH_MACRO_0_FREE_SFLASH817

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF731

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1169SFLASH_MACRO_0_FREE_SFLASH818

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF732

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1170SFLASH_MACRO_0_FREE_SFLASH819

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF733

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1171SFLASH_MACRO_0_FREE_SFLASH820

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF734

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1172SFLASH_MACRO_0_FREE_SFLASH821

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF735

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1173SFLASH_MACRO_0_FREE_SFLASH822

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF736

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1174SFLASH_MACRO_0_FREE_SFLASH823

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF737

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1175SFLASH_MACRO_0_FREE_SFLASH824

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF738

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1176SFLASH_MACRO_0_FREE_SFLASH825

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF739

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1177SFLASH_MACRO_0_FREE_SFLASH826

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF73A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1178SFLASH_MACRO_0_FREE_SFLASH827

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF73B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1179SFLASH_MACRO_0_FREE_SFLASH828

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF73C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1180SFLASH_MACRO_0_FREE_SFLASH829

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF73D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1181SFLASH_MACRO_0_FREE_SFLASH830

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF73E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1182SFLASH_MACRO_0_FREE_SFLASH831

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF73F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1183SFLASH_MACRO_0_FREE_SFLASH832

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF740

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1184SFLASH_MACRO_0_FREE_SFLASH833

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF741

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1185SFLASH_MACRO_0_FREE_SFLASH834

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF742

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1186SFLASH_MACRO_0_FREE_SFLASH835

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF743

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1187SFLASH_MACRO_0_FREE_SFLASH836

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF744

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1188SFLASH_MACRO_0_FREE_SFLASH837

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF745

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1189SFLASH_MACRO_0_FREE_SFLASH838

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF746

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1190SFLASH_MACRO_0_FREE_SFLASH839

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF747

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1191SFLASH_MACRO_0_FREE_SFLASH840

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF748

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1192SFLASH_MACRO_0_FREE_SFLASH841

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF749

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1193SFLASH_MACRO_0_FREE_SFLASH842

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF74A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1194SFLASH_MACRO_0_FREE_SFLASH843

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF74B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1195SFLASH_MACRO_0_FREE_SFLASH844

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF74C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1196SFLASH_MACRO_0_FREE_SFLASH845

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF74D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1197SFLASH_MACRO_0_FREE_SFLASH846

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF74E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1198SFLASH_MACRO_0_FREE_SFLASH847

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF74F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1199SFLASH_MACRO_0_FREE_SFLASH848

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF750

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1200SFLASH_MACRO_0_FREE_SFLASH849

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF751

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1201SFLASH_MACRO_0_FREE_SFLASH850

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF752

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1202SFLASH_MACRO_0_FREE_SFLASH851

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF753

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1203SFLASH_MACRO_0_FREE_SFLASH852

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF754

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1204SFLASH_MACRO_0_FREE_SFLASH853

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF755

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1205SFLASH_MACRO_0_FREE_SFLASH854

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF756

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1206SFLASH_MACRO_0_FREE_SFLASH855

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF757

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1207SFLASH_MACRO_0_FREE_SFLASH856

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF758

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1208SFLASH_MACRO_0_FREE_SFLASH857

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF759

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1209SFLASH_MACRO_0_FREE_SFLASH858

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF75A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1210SFLASH_MACRO_0_FREE_SFLASH859

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF75B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1211SFLASH_MACRO_0_FREE_SFLASH860

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF75C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1212SFLASH_MACRO_0_FREE_SFLASH861

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF75D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1213SFLASH_MACRO_0_FREE_SFLASH862

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF75E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1214SFLASH_MACRO_0_FREE_SFLASH863

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF75F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1215SFLASH_MACRO_0_FREE_SFLASH864

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF760

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1216SFLASH_MACRO_0_FREE_SFLASH865

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF761

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1217SFLASH_MACRO_0_FREE_SFLASH866

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF762

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1218SFLASH_MACRO_0_FREE_SFLASH867

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF763

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1219SFLASH_MACRO_0_FREE_SFLASH868

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF764

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1220SFLASH_MACRO_0_FREE_SFLASH869

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF765

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1221SFLASH_MACRO_0_FREE_SFLASH870

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF766

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1222SFLASH_MACRO_0_FREE_SFLASH871

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF767

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1223SFLASH_MACRO_0_FREE_SFLASH872

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF768

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1224SFLASH_MACRO_0_FREE_SFLASH873

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF769

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1225SFLASH_MACRO_0_FREE_SFLASH874

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF76A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1226SFLASH_MACRO_0_FREE_SFLASH875

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF76B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1227SFLASH_MACRO_0_FREE_SFLASH876

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF76C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1228SFLASH_MACRO_0_FREE_SFLASH877

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF76D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1229SFLASH_MACRO_0_FREE_SFLASH878

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF76E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1230SFLASH_MACRO_0_FREE_SFLASH879

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF76F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1231SFLASH_MACRO_0_FREE_SFLASH880

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF770

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1232SFLASH_MACRO_0_FREE_SFLASH881

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF771

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1233SFLASH_MACRO_0_FREE_SFLASH882

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF772

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1234SFLASH_MACRO_0_FREE_SFLASH883

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF773

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1235SFLASH_MACRO_0_FREE_SFLASH884

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF774

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1236SFLASH_MACRO_0_FREE_SFLASH885

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF775

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1237SFLASH_MACRO_0_FREE_SFLASH886

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF776

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1238SFLASH_MACRO_0_FREE_SFLASH887

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF777

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1239SFLASH_MACRO_0_FREE_SFLASH888

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF778

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1240SFLASH_MACRO_0_FREE_SFLASH889

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF779

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1241SFLASH_MACRO_0_FREE_SFLASH890

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF77A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1242SFLASH_MACRO_0_FREE_SFLASH891

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF77B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1243SFLASH_MACRO_0_FREE_SFLASH892

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF77C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1244SFLASH_MACRO_0_FREE_SFLASH893

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF77D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1245SFLASH_MACRO_0_FREE_SFLASH894

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF77E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1246SFLASH_MACRO_0_FREE_SFLASH895

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF77F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1247SFLASH_MACRO_0_FREE_SFLASH896

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF780

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1248SFLASH_MACRO_0_FREE_SFLASH897

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF781

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1249SFLASH_MACRO_0_FREE_SFLASH898

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF782

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1250SFLASH_MACRO_0_FREE_SFLASH899

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF783

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1251SFLASH_MACRO_0_FREE_SFLASH900

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF784

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1252SFLASH_MACRO_0_FREE_SFLASH901

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF785

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1253SFLASH_MACRO_0_FREE_SFLASH902

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF786

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1254SFLASH_MACRO_0_FREE_SFLASH903

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF787

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1255SFLASH_MACRO_0_FREE_SFLASH904

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF788

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1256SFLASH_MACRO_0_FREE_SFLASH905

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF789

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1257SFLASH_MACRO_0_FREE_SFLASH906

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF78A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1258SFLASH_MACRO_0_FREE_SFLASH907

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF78B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1259SFLASH_MACRO_0_FREE_SFLASH908

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF78C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1260SFLASH_MACRO_0_FREE_SFLASH909

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF78D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1261SFLASH_MACRO_0_FREE_SFLASH910

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF78E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1262SFLASH_MACRO_0_FREE_SFLASH911

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF78F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1263SFLASH_MACRO_0_FREE_SFLASH912

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF790

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1264SFLASH_MACRO_0_FREE_SFLASH913

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF791

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1265SFLASH_MACRO_0_FREE_SFLASH914

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF792

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1266SFLASH_MACRO_0_FREE_SFLASH915

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF793

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1267SFLASH_MACRO_0_FREE_SFLASH916

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF794

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1268SFLASH_MACRO_0_FREE_SFLASH917

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF795

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1269SFLASH_MACRO_0_FREE_SFLASH918

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF796

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1270SFLASH_MACRO_0_FREE_SFLASH919

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF797

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1271SFLASH_MACRO_0_FREE_SFLASH920

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF798

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1272SFLASH_MACRO_0_FREE_SFLASH921

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF799

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1273SFLASH_MACRO_0_FREE_SFLASH922

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF79A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1274SFLASH_MACRO_0_FREE_SFLASH923

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF79B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1275SFLASH_MACRO_0_FREE_SFLASH924

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF79C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1276SFLASH_MACRO_0_FREE_SFLASH925

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF79D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1277SFLASH_MACRO_0_FREE_SFLASH926

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF79E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1278SFLASH_MACRO_0_FREE_SFLASH927

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF79F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1279SFLASH_MACRO_0_FREE_SFLASH928

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1280SFLASH_MACRO_0_FREE_SFLASH929

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7A1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1281SFLASH_MACRO_0_FREE_SFLASH930

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7A2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1282SFLASH_MACRO_0_FREE_SFLASH931

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7A3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1283SFLASH_MACRO_0_FREE_SFLASH932

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7A4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1284SFLASH_MACRO_0_FREE_SFLASH933

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7A5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1285SFLASH_MACRO_0_FREE_SFLASH934

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7A6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1286SFLASH_MACRO_0_FREE_SFLASH935

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7A7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1287SFLASH_MACRO_0_FREE_SFLASH936

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7A8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1288SFLASH_MACRO_0_FREE_SFLASH937

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7A9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1289SFLASH_MACRO_0_FREE_SFLASH938

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7AA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1290SFLASH_MACRO_0_FREE_SFLASH939

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7AB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1291SFLASH_MACRO_0_FREE_SFLASH940

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7AC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1292SFLASH_MACRO_0_FREE_SFLASH941

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7AD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1293SFLASH_MACRO_0_FREE_SFLASH942

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7AE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1294SFLASH_MACRO_0_FREE_SFLASH943

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7AF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1295SFLASH_MACRO_0_FREE_SFLASH944

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7B0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1296SFLASH_MACRO_0_FREE_SFLASH945

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7B1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1297SFLASH_MACRO_0_FREE_SFLASH946

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7B2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1298SFLASH_MACRO_0_FREE_SFLASH947

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7B3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1299SFLASH_MACRO_0_FREE_SFLASH948

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7B4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1300SFLASH_MACRO_0_FREE_SFLASH949

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7B5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1301SFLASH_MACRO_0_FREE_SFLASH950

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7B6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1302SFLASH_MACRO_0_FREE_SFLASH951

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7B7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1303SFLASH_MACRO_0_FREE_SFLASH952

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7B8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1304SFLASH_MACRO_0_FREE_SFLASH953

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7B9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1305SFLASH_MACRO_0_FREE_SFLASH954

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7BA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1306SFLASH_MACRO_0_FREE_SFLASH955

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7BB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1307SFLASH_MACRO_0_FREE_SFLASH956

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7BC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1308SFLASH_MACRO_0_FREE_SFLASH957

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7BD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1309SFLASH_MACRO_0_FREE_SFLASH958

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7BE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1310SFLASH_MACRO_0_FREE_SFLASH959

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7BF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1311SFLASH_MACRO_0_FREE_SFLASH960

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1312SFLASH_MACRO_0_FREE_SFLASH961

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7C1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1313SFLASH_MACRO_0_FREE_SFLASH962

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7C2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1314SFLASH_MACRO_0_FREE_SFLASH963

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7C3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1315SFLASH_MACRO_0_FREE_SFLASH964

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1316SFLASH_MACRO_0_FREE_SFLASH965

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7C5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1317SFLASH_MACRO_0_FREE_SFLASH966

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7C6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1318SFLASH_MACRO_0_FREE_SFLASH967

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7C7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1319SFLASH_MACRO_0_FREE_SFLASH968

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7C8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1320SFLASH_MACRO_0_FREE_SFLASH969

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7C9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1321SFLASH_MACRO_0_FREE_SFLASH970

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7CA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1322SFLASH_MACRO_0_FREE_SFLASH971

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7CB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1323SFLASH_MACRO_0_FREE_SFLASH972

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7CC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1324SFLASH_MACRO_0_FREE_SFLASH973

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7CD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1325SFLASH_MACRO_0_FREE_SFLASH974

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7CE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1326SFLASH_MACRO_0_FREE_SFLASH975

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7CF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1327SFLASH_MACRO_0_FREE_SFLASH976

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7D0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1328SFLASH_MACRO_0_FREE_SFLASH977

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7D1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1329SFLASH_MACRO_0_FREE_SFLASH978

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7D2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1330SFLASH_MACRO_0_FREE_SFLASH979

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7D3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1331SFLASH_MACRO_0_FREE_SFLASH980

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7D4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1332SFLASH_MACRO_0_FREE_SFLASH981

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7D5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1333SFLASH_MACRO_0_FREE_SFLASH982

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7D6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1334SFLASH_MACRO_0_FREE_SFLASH983

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7D7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1335SFLASH_MACRO_0_FREE_SFLASH984

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7D8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1336SFLASH_MACRO_0_FREE_SFLASH985

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7D9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1337SFLASH_MACRO_0_FREE_SFLASH986

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7DA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1338SFLASH_MACRO_0_FREE_SFLASH987

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7DB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1339SFLASH_MACRO_0_FREE_SFLASH988

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7DC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1340SFLASH_MACRO_0_FREE_SFLASH989

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7DD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1341SFLASH_MACRO_0_FREE_SFLASH990

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7DE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1342SFLASH_MACRO_0_FREE_SFLASH991

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7DF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1343SFLASH_MACRO_0_FREE_SFLASH992

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1344SFLASH_MACRO_0_FREE_SFLASH993

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7E1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1345SFLASH_MACRO_0_FREE_SFLASH994

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7E2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1346SFLASH_MACRO_0_FREE_SFLASH995

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7E3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1347SFLASH_MACRO_0_FREE_SFLASH996

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7E4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1348SFLASH_MACRO_0_FREE_SFLASH997

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7E5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1349SFLASH_MACRO_0_FREE_SFLASH998

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7E6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1350SFLASH_MACRO_0_FREE_SFLASH999

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7E7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1351SFLASH_MACRO_0_FREE_SFLASH1000

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7E8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1352SFLASH_MACRO_0_FREE_SFLASH1001

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7E9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1353SFLASH_MACRO_0_FREE_SFLASH1002

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7EA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1354SFLASH_MACRO_0_FREE_SFLASH1003

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7EB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1355SFLASH_MACRO_0_FREE_SFLASH1004

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7EC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1356SFLASH_MACRO_0_FREE_SFLASH1005

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7ED

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1357SFLASH_MACRO_0_FREE_SFLASH1006

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7EE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1358SFLASH_MACRO_0_FREE_SFLASH1007

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7EF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1359SFLASH_MACRO_0_FREE_SFLASH1008

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7F0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1360SFLASH_MACRO_0_FREE_SFLASH1009

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7F1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1361SFLASH_MACRO_0_FREE_SFLASH1010

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7F2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1362SFLASH_MACRO_0_FREE_SFLASH1011

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7F3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1363SFLASH_MACRO_0_FREE_SFLASH1012

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7F4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1364SFLASH_MACRO_0_FREE_SFLASH1013

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7F5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1365SFLASH_MACRO_0_FREE_SFLASH1014

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7F6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1366SFLASH_MACRO_0_FREE_SFLASH1015

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7F7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1367SFLASH_MACRO_0_FREE_SFLASH1016

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7F8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1368SFLASH_MACRO_0_FREE_SFLASH1017

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7F9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1369SFLASH_MACRO_0_FREE_SFLASH1018

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7FA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1370SFLASH_MACRO_0_FREE_SFLASH1019

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7FB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1371SFLASH_MACRO_0_FREE_SFLASH1020

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7FC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1372SFLASH_MACRO_0_FREE_SFLASH1021

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7FD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1373SFLASH_MACRO_0_FREE_SFLASH1022

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7FE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1374SFLASH_MACRO_0_FREE_SFLASH1023

Uncommitted Supervisorly Flash in Macro 0

Address: 0x0FFFF7FF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	BYTE_MEM [7:0]							

Bits	Name	Description
7 : 0	BYTE_MEM	Uncommited storage byte in Supervisory Flash Default Value: X

30.1.1375SFLASH_ALT_PROT_ROW0

Per Page Write Protection

Address: 0x0FFFF800

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1376SFLASH_ALT_PROT_ROW1

Per Page Write Protection

Address: 0x0FFFF801

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1377SFLASH_ALT_PROT_ROW2

Per Page Write Protection

Address: 0x0FFFF802

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1378SFLASH_ALT_PROT_ROW3

Per Page Write Protection

Address: 0x0FFFF803

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1379SFLASH_ALT_PROT_ROW4

Per Page Write Protection

Address: 0x0FFFF804

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1380SFLASH_ALT_PROT_ROW5

Per Page Write Protection

Address: 0x0FFFF805

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1381SFLASH_ALT_PROT_ROW6

Per Page Write Protection

Address: 0x0FFFF806

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1382SFLASH_ALT_PROT_ROW7

Per Page Write Protection

Address: 0x0FFFF807

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1383SFLASH_ALT_PROT_ROW8

Per Page Write Protection

Address: 0x0FFFF808

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1384SFLASH_ALT_PROT_ROW9

Per Page Write Protection

Address: 0x0FFFF809

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1385SFLASH_ALT_PROT_ROW10

Per Page Write Protection

Address: 0x0FFFF80A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1386SFLASH_ALT_PROT_ROW11

Per Page Write Protection

Address: 0x0FFFF80B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1387SFLASH_ALT_PROT_ROW12

Per Page Write Protection

Address: 0x0FFFF80C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1388SFLASH_ALT_PROT_ROW13

Per Page Write Protection

Address: 0x0FFFF80D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1389SFLASH_ALT_PROT_ROW14

Per Page Write Protection

Address: 0x0FFFF80E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1390SFLASH_ALT_PROT_ROW15

Per Page Write Protection

Address: 0x0FFFF80F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1391SFLASH_ALT_PROT_ROW16

Per Page Write Protection

Address: 0x0FFFF810

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1392SFLASH_ALT_PROT_ROW17

Per Page Write Protection

Address: 0x0FFFF811

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1393SFLASH_ALT_PROT_ROW18

Per Page Write Protection

Address: 0x0FFFF812

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1394SFLASH_ALT_PROT_ROW19

Per Page Write Protection

Address: 0x0FFFF813

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1395SFLASH_ALT_PROT_ROW20

Per Page Write Protection

Address: 0x0FFFF814

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1396SFLASH_ALT_PROT_ROW21

Per Page Write Protection

Address: 0x0FFFF815

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1397SFLASH_ALT_PROT_ROW22

Per Page Write Protection

Address: 0x0FFFF816

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1398SFLASH_ALT_PROT_ROW23

Per Page Write Protection

Address: 0x0FFFF817

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1399SFLASH_ALT_PROT_ROW24

Per Page Write Protection

Address: 0x0FFFF818

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1400SFLASH_ALT_PROT_ROW25

Per Page Write Protection

Address: 0x0FFFF819

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1401SFLASH_ALT_PROT_ROW26

Per Page Write Protection

Address: 0x0FFFF81A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1402SFLASH_ALT_PROT_ROW27

Per Page Write Protection

Address: 0x0FFFF81B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1403SFLASH_ALT_PROT_ROW28

Per Page Write Protection

Address: 0x0FFFF81C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1404SFLASH_ALT_PROT_ROW29

Per Page Write Protection

Address: 0x0FFFF81D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1405SFLASH_ALT_PROT_ROW30

Per Page Write Protection

Address: 0x0FFFF81E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1406SFLASH_ALT_PROT_ROW31

Per Page Write Protection

Address: 0x0FFFF81F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1407SFLASH_ALT_PROT_ROW32

Per Page Write Protection

Address: 0x0FFFF820

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1408SFLASH_ALT_PROT_ROW33

Per Page Write Protection

Address: 0x0FFFF821

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1409SFLASH_ALT_PROT_ROW34

Per Page Write Protection

Address: 0x0FFFF822

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1410SFLASH_ALT_PROT_ROW35

Per Page Write Protection

Address: 0x0FFFF823

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1411SFLASH_ALT_PROT_ROW36

Per Page Write Protection

Address: 0x0FFFF824

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1412SFLASH_ALT_PROT_ROW37

Per Page Write Protection

Address: 0x0FFFF825

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1413SFLASH_ALT_PROT_ROW38

Per Page Write Protection

Address: 0x0FFFF826

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1414SFLASH_ALT_PROT_ROW39

Per Page Write Protection

Address: 0x0FFFF827

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1415SFLASH_ALT_PROT_ROW40

Per Page Write Protection

Address: 0x0FFFF828

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1416SFLASH_ALT_PROT_ROW41

Per Page Write Protection

Address: 0x0FFFF829

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1417SFLASH_ALT_PROT_ROW42

Per Page Write Protection

Address: 0x0FFFF82A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1418SFLASH_ALT_PROT_ROW43

Per Page Write Protection

Address: 0x0FFFF82B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1419SFLASH_ALT_PROT_ROW44

Per Page Write Protection

Address: 0x0FFFF82C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1420SFLASH_ALT_PROT_ROW45

Per Page Write Protection

Address: 0x0FFFF82D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1421SFLASH_ALT_PROT_ROW46

Per Page Write Protection

Address: 0x0FFFF82E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1422SFLASH_ALT_PROT_ROW47

Per Page Write Protection

Address: 0x0FFFF82F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1423SFLASH_ALT_PROT_ROW48

Per Page Write Protection

Address: 0x0FFFF830

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1424SFLASH_ALT_PROT_ROW49

Per Page Write Protection

Address: 0x0FFFF831

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1425SFLASH_ALT_PROT_ROW50

Per Page Write Protection

Address: 0x0FFFF832

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1426SFLASH_ALT_PROT_ROW51

Per Page Write Protection

Address: 0x0FFFF833

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1427SFLASH_ALT_PROT_ROW52

Per Page Write Protection

Address: 0x0FFFF834

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1428SFLASH_ALT_PROT_ROW53

Per Page Write Protection

Address: 0x0FFFF835

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1429SFLASH_ALT_PROT_ROW54

Per Page Write Protection

Address: 0x0FFFF836

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1430SFLASH_ALT_PROT_ROW55

Per Page Write Protection

Address: 0x0FFFF837

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1431SFLASH_ALT_PROT_ROW56

Per Page Write Protection

Address: 0x0FFFF838

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1432SFLASH_ALT_PROT_ROW57

Per Page Write Protection

Address: 0x0FFFF839

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1433SFLASH_ALT_PROT_ROW58

Per Page Write Protection

Address: 0x0FFFF83A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1434SFLASH_ALT_PROT_ROW59

Per Page Write Protection

Address: 0x0FFFF83B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1435SFLASH_ALT_PROT_ROW60

Per Page Write Protection

Address: 0x0FFFF83C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1436SFLASH_ALT_PROT_ROW61

Per Page Write Protection

Address: 0x0FFFF83D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1437SFLASH_ALT_PROT_ROW62

Per Page Write Protection

Address: 0x0FFFF83E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1438SFLASH_ALT_PROT_ROW63

Per Page Write Protection

Address: 0x0FFFF83F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1439SFLASH_ALT_PROT_ROW64

Per Page Write Protection

Address: 0x0FFFF840

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1440SFLASH_ALT_PROT_ROW65

Per Page Write Protection

Address: 0x0FFFF841

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1441SFLASH_ALT_PROT_ROW66

Per Page Write Protection

Address: 0x0FFFF842

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1442SFLASH_ALT_PROT_ROW67

Per Page Write Protection

Address: 0x0FFFF843

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1443SFLASH_ALT_PROT_ROW68

Per Page Write Protection

Address: 0x0FFFF844

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1444SFLASH_ALT_PROT_ROW69

Per Page Write Protection

Address: 0x0FFFF845

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1445SFLASH_ALT_PROT_ROW70

Per Page Write Protection

Address: 0x0FFFF846

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1446SFLASH_ALT_PROT_ROW71

Per Page Write Protection

Address: 0x0FFFF847

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1447SFLASH_ALT_PROT_ROW72

Per Page Write Protection

Address: 0x0FFFF848

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1448SFLASH_ALT_PROT_ROW73

Per Page Write Protection

Address: 0x0FFFF849

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1449SFLASH_ALT_PROT_ROW74

Per Page Write Protection

Address: 0x0FFFF84A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1450SFLASH_ALT_PROT_ROW75

Per Page Write Protection

Address: 0x0FFFF84B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1451SFLASH_ALT_PROT_ROW76

Per Page Write Protection

Address: 0x0FFFF84C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1452SFLASH_ALT_PROT_ROW77

Per Page Write Protection

Address: 0x0FFFF84D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1453SFLASH_ALT_PROT_ROW78

Per Page Write Protection

Address: 0x0FFFF84E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1454SFLASH_ALT_PROT_ROW79

Per Page Write Protection

Address: 0x0FFFF84F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1455SFLASH_ALT_PROT_ROW80

Per Page Write Protection

Address: 0x0FFFF850

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1456SFLASH_ALT_PROT_ROW81

Per Page Write Protection

Address: 0x0FFFF851

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1457SFLASH_ALT_PROT_ROW82

Per Page Write Protection

Address: 0x0FFFF852

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1458SFLASH_ALT_PROT_ROW83

Per Page Write Protection

Address: 0x0FFFF853

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1459SFLASH_ALT_PROT_ROW84

Per Page Write Protection

Address: 0x0FFFF854

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1460SFLASH_ALT_PROT_ROW85

Per Page Write Protection

Address: 0x0FFFF855

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1461SFLASH_ALT_PROT_ROW86

Per Page Write Protection

Address: 0x0FFFF856

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1462SFLASH_ALT_PROT_ROW87

Per Page Write Protection

Address: 0x0FFFF857

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1463SFLASH_ALT_PROT_ROW88

Per Page Write Protection

Address: 0x0FFFF858

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1464SFLASH_ALT_PROT_ROW89

Per Page Write Protection

Address: 0x0FFFF859

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1465SFLASH_ALT_PROT_ROW90

Per Page Write Protection

Address: 0x0FFFF85A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1466SFLASH_ALT_PROT_ROW91

Per Page Write Protection

Address: 0x0FFFF85B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1467SFLASH_ALT_PROT_ROW92

Per Page Write Protection

Address: 0x0FFFF85C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1468SFLASH_ALT_PROT_ROW93

Per Page Write Protection

Address: 0x0FFFF85D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1469SFLASH_ALT_PROT_ROW94

Per Page Write Protection

Address: 0x0FFFF85E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1470SFLASH_ALT_PROT_ROW95

Per Page Write Protection

Address: 0x0FFFF85F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1471SFLASH_ALT_PROT_ROW96

Per Page Write Protection

Address: 0x0FFFF860

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1472SFLASH_ALT_PROT_ROW97

Per Page Write Protection

Address: 0x0FFFF861

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1473SFLASH_ALT_PROT_ROW98

Per Page Write Protection

Address: 0x0FFFF862

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1474SFLASH_ALT_PROT_ROW99

Per Page Write Protection

Address: 0x0FFFF863

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1475SFLASH_ALT_PROT_ROW100

Per Page Write Protection

Address: 0x0FFFF864

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1476SFLASH_ALT_PROT_ROW101

Per Page Write Protection

Address: 0x0FFFF865

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1477SFLASH_ALT_PROT_ROW102

Per Page Write Protection

Address: 0x0FFFF866

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1478SFLASH_ALT_PROT_ROW103

Per Page Write Protection

Address: 0x0FFFF867

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1479SFLASH_ALT_PROT_ROW104

Per Page Write Protection

Address: 0x0FFFF868

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1480SFLASH_ALT_PROT_ROW105

Per Page Write Protection

Address: 0x0FFFF869

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1481SFLASH_ALT_PROT_ROW106

Per Page Write Protection

Address: 0x0FFFF86A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1482SFLASH_ALT_PROT_ROW107

Per Page Write Protection

Address: 0x0FFFF86B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1483SFLASH_ALT_PROT_ROW108

Per Page Write Protection

Address: 0x0FFFF86C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1484SFLASH_ALT_PROT_ROW109

Per Page Write Protection

Address: 0x0FFFF86D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1485SFLASH_ALT_PROT_ROW110

Per Page Write Protection

Address: 0x0FFFF86E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1486SFLASH_ALT_PROT_ROW111

Per Page Write Protection

Address: 0x0FFFF86F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1487SFLASH_ALT_PROT_ROW112

Per Page Write Protection

Address: 0x0FFFF870

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1488SFLASH_ALT_PROT_ROW113

Per Page Write Protection

Address: 0x0FFFF871

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1489SFLASH_ALT_PROT_ROW114

Per Page Write Protection

Address: 0x0FFFF872

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1490SFLASH_ALT_PROT_ROW115

Per Page Write Protection

Address: 0x0FFFF873

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1491SFLASH_ALT_PROT_ROW116

Per Page Write Protection

Address: 0x0FFFF874

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1492SFLASH_ALT_PROT_ROW117

Per Page Write Protection

Address: 0x0FFFF875

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1493SFLASH_ALT_PROT_ROW118

Per Page Write Protection

Address: 0x0FFFF876

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1494SFLASH_ALT_PROT_ROW119

Per Page Write Protection

Address: 0x0FFFF877

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1495SFLASH_ALT_PROT_ROW120

Per Page Write Protection

Address: 0x0FFFF878

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1496SFLASH_ALT_PROT_ROW121

Per Page Write Protection

Address: 0x0FFFF879

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1497SFLASH_ALT_PROT_ROW122

Per Page Write Protection

Address: 0x0FFFF87A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1498SFLASH_ALT_PROT_ROW123

Per Page Write Protection

Address: 0x0FFFF87B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1499SFLASH_ALT_PROT_ROW124

Per Page Write Protection

Address: 0x0FFFF87C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1500SFLASH_ALT_PROT_ROW125

Per Page Write Protection

Address: 0x0FFFF87D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1501SFLASH_ALT_PROT_ROW126

Per Page Write Protection

Address: 0x0FFFF87E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1502SFLASH_ALT_PROT_ROW127

Per Page Write Protection

Address: 0x0FFFF87F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1503SFLASH_ALT_PROT_ROW128

Per Page Write Protection

Address: 0x0FFFF880

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1504SFLASH_ALT_PROT_ROW129

Per Page Write Protection

Address: 0x0FFFF881

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1505SFLASH_ALT_PROT_ROW130

Per Page Write Protection

Address: 0x0FFFF882

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1506SFLASH_ALT_PROT_ROW131

Per Page Write Protection

Address: 0x0FFFF883

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1507SFLASH_ALT_PROT_ROW132

Per Page Write Protection

Address: 0x0FFFF884

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1508SFLASH_ALT_PROT_ROW133

Per Page Write Protection

Address: 0x0FFFF885

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1509SFLASH_ALT_PROT_ROW134

Per Page Write Protection

Address: 0x0FFFF886

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1510SFLASH_ALT_PROT_ROW135

Per Page Write Protection

Address: 0x0FFFF887

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1511SFLASH_ALT_PROT_ROW136

Per Page Write Protection

Address: 0x0FFFF888

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1512SFLASH_ALT_PROT_ROW137

Per Page Write Protection

Address: 0x0FFFF889

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1513SFLASH_ALT_PROT_ROW138

Per Page Write Protection

Address: 0x0FFFF88A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1514SFLASH_ALT_PROT_ROW139

Per Page Write Protection

Address: 0x0FFFF88B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1515SFLASH_ALT_PROT_ROW140

Per Page Write Protection

Address: 0x0FFFF88C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1516SFLASH_ALT_PROT_ROW141

Per Page Write Protection

Address: 0x0FFFF88D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1517SFLASH_ALT_PROT_ROW142

Per Page Write Protection

Address: 0x0FFFF88E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1518SFLASH_ALT_PROT_ROW143

Per Page Write Protection

Address: 0x0FFFF88F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1519SFLASH_ALT_PROT_ROW144

Per Page Write Protection

Address: 0x0FFFF890

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1520SFLASH_ALT_PROT_ROW145

Per Page Write Protection

Address: 0x0FFFF891

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1521SFLASH_ALT_PROT_ROW146

Per Page Write Protection

Address: 0x0FFFF892

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1522SFLASH_ALT_PROT_ROW147

Per Page Write Protection

Address: 0x0FFFF893

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1523SFLASH_ALT_PROT_ROW148

Per Page Write Protection

Address: 0x0FFFF894

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1524SFLASH_ALT_PROT_ROW149

Per Page Write Protection

Address: 0x0FFFF895

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1525SFLASH_ALT_PROT_ROW150

Per Page Write Protection

Address: 0x0FFFF896

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1526SFLASH_ALT_PROT_ROW151

Per Page Write Protection

Address: 0x0FFFF897

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1527SFLASH_ALT_PROT_ROW152

Per Page Write Protection

Address: 0x0FFFF898

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1528SFLASH_ALT_PROT_ROW153

Per Page Write Protection

Address: 0x0FFFF899

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1529SFLASH_ALT_PROT_ROW154

Per Page Write Protection

Address: 0x0FFFF89A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1530SFLASH_ALT_PROT_ROW155

Per Page Write Protection

Address: 0x0FFFF89B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1531SFLASH_ALT_PROT_ROW156

Per Page Write Protection

Address: 0x0FFFF89C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1532SFLASH_ALT_PROT_ROW157

Per Page Write Protection

Address: 0x0FFFF89D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1533SFLASH_ALT_PROT_ROW158

Per Page Write Protection

Address: 0x0FFFF89E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1534SFLASH_ALT_PROT_ROW159

Per Page Write Protection

Address: 0x0FFFF89F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1535SFLASH_ALT_PROT_ROW160

Per Page Write Protection

Address: 0x0FFFF8A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1536SFLASH_ALT_PROT_ROW161

Per Page Write Protection

Address: 0x0FFFF8A1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1537SFLASH_ALT_PROT_ROW162

Per Page Write Protection

Address: 0x0FFFF8A2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1538SFLASH_ALT_PROT_ROW163

Per Page Write Protection

Address: 0x0FFFF8A3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1539SFLASH_ALT_PROT_ROW164

Per Page Write Protection

Address: 0x0FFFF8A4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1540SFLASH_ALT_PROT_ROW165

Per Page Write Protection

Address: 0x0FFFF8A5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1541SFLASH_ALT_PROT_ROW166

Per Page Write Protection

Address: 0x0FFFF8A6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1542SFLASH_ALT_PROT_ROW167

Per Page Write Protection

Address: 0x0FFFF8A7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1543SFLASH_ALT_PROT_ROW168

Per Page Write Protection

Address: 0x0FFFF8A8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1544SFLASH_ALT_PROT_ROW169

Per Page Write Protection

Address: 0x0FFFF8A9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1545SFLASH_ALT_PROT_ROW170

Per Page Write Protection

Address: 0x0FFFF8AA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1546SFLASH_ALT_PROT_ROW171

Per Page Write Protection

Address: 0x0FFFF8AB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1547SFLASH_ALT_PROT_ROW172

Per Page Write Protection

Address: 0x0FFFF8AC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1548SFLASH_ALT_PROT_ROW173

Per Page Write Protection

Address: 0x0FFFF8AD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1549SFLASH_ALT_PROT_ROW174

Per Page Write Protection

Address: 0x0FFFF8AE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1550SFLASH_ALT_PROT_ROW175

Per Page Write Protection

Address: 0x0FFFF8AF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1551SFLASH_ALT_PROT_ROW176

Per Page Write Protection

Address: 0x0FFFF8B0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1552SFLASH_ALT_PROT_ROW177

Per Page Write Protection

Address: 0x0FFFF8B1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1553SFLASH_ALT_PROT_ROW178

Per Page Write Protection

Address: 0x0FFFF8B2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1554SFLASH_ALT_PROT_ROW179

Per Page Write Protection

Address: 0x0FFFF8B3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1555SFLASH_ALT_PROT_ROW180

Per Page Write Protection

Address: 0x0FFFF8B4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1556SFLASH_ALT_PROT_ROW181

Per Page Write Protection

Address: 0x0FFFF8B5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1557SFLASH_ALT_PROT_ROW182

Per Page Write Protection

Address: 0x0FFFF8B6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1558SFLASH_ALT_PROT_ROW183

Per Page Write Protection

Address: 0x0FFFF8B7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1559SFLASH_ALT_PROT_ROW184

Per Page Write Protection

Address: 0x0FFFF8B8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1560SFLASH_ALT_PROT_ROW185

Per Page Write Protection

Address: 0x0FFFF8B9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1561SFLASH_ALT_PROT_ROW186

Per Page Write Protection

Address: 0x0FFFF8BA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1562SFLASH_ALT_PROT_ROW187

Per Page Write Protection

Address: 0x0FFFF8BB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1563SFLASH_ALT_PROT_ROW188

Per Page Write Protection

Address: 0x0FFFF8BC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1564SFLASH_ALT_PROT_ROW189

Per Page Write Protection

Address: 0x0FFFF8BD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1565SFLASH_ALT_PROT_ROW190

Per Page Write Protection

Address: 0x0FFFF8BE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1566SFLASH_ALT_PROT_ROW191

Per Page Write Protection

Address: 0x0FFFF8BF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1567SFLASH_ALT_PROT_ROW192

Per Page Write Protection

Address: 0x0FFFF8C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1568SFLASH_ALT_PROT_ROW193

Per Page Write Protection

Address: 0x0FFFF8C1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1569SFLASH_ALT_PROT_ROW194

Per Page Write Protection

Address: 0x0FFFF8C2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1570SFLASH_ALT_PROT_ROW195

Per Page Write Protection

Address: 0x0FFFF8C3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1571SFLASH_ALT_PROT_ROW196

Per Page Write Protection

Address: 0x0FFFF8C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1572SFLASH_ALT_PROT_ROW197

Per Page Write Protection

Address: 0x0FFFF8C5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1573SFLASH_ALT_PROT_ROW198

Per Page Write Protection

Address: 0x0FFFF8C6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1574SFLASH_ALT_PROT_ROW199

Per Page Write Protection

Address: 0x0FFFF8C7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1575SFLASH_ALT_PROT_ROW200

Per Page Write Protection

Address: 0x0FFFF8C8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1576SFLASH_ALT_PROT_ROW201

Per Page Write Protection

Address: 0x0FFFF8C9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1577SFLASH_ALT_PROT_ROW202

Per Page Write Protection

Address: 0x0FFFF8CA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1578SFLASH_ALT_PROT_ROW203

Per Page Write Protection

Address: 0x0FFFF8CB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1579SFLASH_ALT_PROT_ROW204

Per Page Write Protection

Address: 0x0FFFF8CC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1580SFLASH_ALT_PROT_ROW205

Per Page Write Protection

Address: 0x0FFFF8CD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1581SFLASH_ALT_PROT_ROW206

Per Page Write Protection

Address: 0x0FFFF8CE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1582SFLASH_ALT_PROT_ROW207

Per Page Write Protection

Address: 0x0FFFF8CF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1583SFLASH_ALT_PROT_ROW208

Per Page Write Protection

Address: 0x0FFFF8D0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1584SFLASH_ALT_PROT_ROW209

Per Page Write Protection

Address: 0x0FFFF8D1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1585SFLASH_ALT_PROT_ROW210

Per Page Write Protection

Address: 0x0FFFF8D2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1586SFLASH_ALT_PROT_ROW211

Per Page Write Protection

Address: 0x0FFFF8D3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1587SFLASH_ALT_PROT_ROW212

Per Page Write Protection

Address: 0x0FFFF8D4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1588SFLASH_ALT_PROT_ROW213

Per Page Write Protection

Address: 0x0FFFF8D5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1589SFLASH_ALT_PROT_ROW214

Per Page Write Protection

Address: 0x0FFFF8D6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1590SFLASH_ALT_PROT_ROW215

Per Page Write Protection

Address: 0x0FFFF8D7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1591SFLASH_ALT_PROT_ROW216

Per Page Write Protection

Address: 0x0FFFF8D8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1592SFLASH_ALT_PROT_ROW217

Per Page Write Protection

Address: 0x0FFFF8D9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1593SFLASH_ALT_PROT_ROW218

Per Page Write Protection

Address: 0x0FFFF8DA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1594SFLASH_ALT_PROT_ROW219

Per Page Write Protection

Address: 0x0FFFF8DB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1595SFLASH_ALT_PROT_ROW220

Per Page Write Protection

Address: 0x0FFFF8DC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1596SFLASH_ALT_PROT_ROW221

Per Page Write Protection

Address: 0x0FFFF8DD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1597SFLASH_ALT_PROT_ROW222

Per Page Write Protection

Address: 0x0FFFF8DE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1598SFLASH_ALT_PROT_ROW223

Per Page Write Protection

Address: 0x0FFFF8DF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1599SFLASH_ALT_PROT_ROW224

Per Page Write Protection

Address: 0x0FFFF8E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1600SFLASH_ALT_PROT_ROW225

Per Page Write Protection

Address: 0x0FFFF8E1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1601SFLASH_ALT_PROT_ROW226

Per Page Write Protection

Address: 0x0FFFF8E2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1602SFLASH_ALT_PROT_ROW227

Per Page Write Protection

Address: 0x0FFFF8E3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1603SFLASH_ALT_PROT_ROW228

Per Page Write Protection

Address: 0x0FFFF8E4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1604SFLASH_ALT_PROT_ROW229

Per Page Write Protection

Address: 0x0FFFF8E5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1605SFLASH_ALT_PROT_ROW230

Per Page Write Protection

Address: 0x0FFFF8E6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1606SFLASH_ALT_PROT_ROW231

Per Page Write Protection

Address: 0x0FFFF8E7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1607SFLASH_ALT_PROT_ROW232

Per Page Write Protection

Address: 0x0FFFF8E8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1608SFLASH_ALT_PROT_ROW233

Per Page Write Protection

Address: 0x0FFFF8E9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1609SFLASH_ALT_PROT_ROW234

Per Page Write Protection

Address: 0x0FFFF8EA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1610SFLASH_ALT_PROT_ROW235

Per Page Write Protection

Address: 0x0FFFF8EB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1611SFLASH_ALT_PROT_ROW236

Per Page Write Protection

Address: 0x0FFFF8EC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1612SFLASH_ALT_PROT_ROW237

Per Page Write Protection

Address: 0x0FFFF8ED

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1613SFLASH_ALT_PROT_ROW238

Per Page Write Protection

Address: 0x0FFFF8EE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1614SFLASH_ALT_PROT_ROW239

Per Page Write Protection

Address: 0x0FFFF8EF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1615SFLASH_ALT_PROT_ROW240

Per Page Write Protection

Address: 0x0FFFF8F0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1616SFLASH_ALT_PROT_ROW241

Per Page Write Protection

Address: 0x0FFFF8F1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1617SFLASH_ALT_PROT_ROW242

Per Page Write Protection

Address: 0x0FFFF8F2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1618SFLASH_ALT_PROT_ROW243

Per Page Write Protection

Address: 0x0FFFF8F3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1619SFLASH_ALT_PROT_ROW244

Per Page Write Protection

Address: 0x0FFFF8F4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1620SFLASH_ALT_PROT_ROW245

Per Page Write Protection

Address: 0x0FFFF8F5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1621SFLASH_ALT_PROT_ROW246

Per Page Write Protection

Address: 0x0FFFF8F6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1622SFLASH_ALT_PROT_ROW247

Per Page Write Protection

Address: 0x0FFFF8F7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1623SFLASH_ALT_PROT_ROW248

Per Page Write Protection

Address: 0x0FFFF8F8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1624SFLASH_ALT_PROT_ROW249

Per Page Write Protection

Address: 0x0FFFF8F9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1625SFLASH_ALT_PROT_ROW250

Per Page Write Protection

Address: 0x0FFFF8FA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1626SFLASH_ALT_PROT_ROW251

Per Page Write Protection

Address: 0x0FFFF8FB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1627SFLASH_ALT_PROT_ROW252

Per Page Write Protection

Address: 0x0FFFF8FC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1628SFLASH_ALT_PROT_ROW253

Per Page Write Protection

Address: 0x0FFFF8FD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1629SFLASH_ALT_PROT_ROW254

Per Page Write Protection

Address: 0x0FFFF8FE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1630SFLASH_ALT_PROT_ROW255

Per Page Write Protection

Address: 0x0FFFF8FF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	DATA8 [7:0]							

Bits	Name	Description
7 : 0	DATA8	Protection Data (1b per page) Default Value: X

30.1.1631SFLASH_ALT_PP

Preprogram Settings

Address: 0x0FFFFB20

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	PERIOD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	None				None			
Name	NDAC [31:28]				PDAC [27:24]			

Bits	Name	Description
31 : 28	NDAC	NDAC input. Each increment in NDAC causes an increase of ~0.10V in VNEG Default Value: X
27 : 24	PDAC	PDAC input. Each increment in PDAC causes an increase of ~0.10V in VPOS Default Value: X
23 : 0	PERIOD	Period of timer in clk_spcif_timer ticks. For regular FLASH, clock is 36MHz from dedicated oscillator. For FLASH-Lite, clock is same as clk_hf, which must be set to 48MHz for 48MHz devices and 12MHz for max 16MHz devices Default Value: X

30.1.1632SFLASH_ALT_E

Erase Settings

Address: 0x0FFFFB24

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	PERIOD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	None				None			
Name	NDAC [31:28]				PDAC [27:24]			

Bits	Name	Description
31 : 28	NDAC	NDAC input. Each increment in NDAC causes an increase of ~0.10V in VNEG Default Value: X
27 : 24	PDAC	PDAC input. Each increment in PDAC causes an increase of ~0.10V in VPOS Default Value: X
23 : 0	PERIOD	Period of timer in clk_spcif_timer ticks. For regular FLASH, clock is 36MHz from dedicated oscillator. For FLASH-Lite, clock is same as clk_hf, which must be set to 48MHz for 48MHz devices and 12MHz for max 16MHz devices Default Value: X

30.1.1633SFLASH_ALT_P

Program Settings

Address: 0x0FFFFB28

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	PERIOD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	None				None			
Name	NDAC [31:28]				PDAC [27:24]			

Bits	Name	Description
31 : 28	NDAC	NDAC input. Each increment in NDAC causes an increase of ~0.10V in VNEG Default Value: X
27 : 24	PDAC	PDAC input. Each increment in PDAC causes an increase of ~0.10V in VPOS Default Value: X
23 : 0	PERIOD	Period of timer in clk_spcif_timer ticks. For regular FLASH, clock is 36MHz from dedicated oscillator. For FLASH-Lite, clock is same as clk_hf, which must be set to 48MHz for 48MHz devices and 12MHz for max 16MHz devices Default Value: X

30.1.1634SFLASH_ALT_EA_E

Erase All - Erase Settings

Address: 0x0FFFFB2C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	PERIOD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	None				None			
Name	NDAC [31:28]				PDAC [27:24]			

Bits	Name	Description
31 : 28	NDAC	NDAC input. Each increment in NDAC causes an increase of ~0.10V in VNEG Default Value: X
27 : 24	PDAC	PDAC input. Each increment in PDAC causes an increase of ~0.10V in VPOS Default Value: X
23 : 0	PERIOD	Period of timer in clk_spcif_timer ticks. For regular FLASH, clock is 36MHz from dedicated oscillator. For FLASH-Lite, clock is same as clk_hf, which must be set to 48MHz for 48MHz devices and 12MHz for max 16MHz devices Default Value: X

30.1.1635SFLASH_ALT_EA_P

Erase All - Program Settings

Address: 0x0FFFFB30

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	PERIOD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	None				None			
Name	NDAC [31:28]				PDAC [27:24]			

Bits	Name	Description
31 : 28	NDAC	NDAC input. Each increment in NDAC causes an increase of ~0.10V in VNEG Default Value: X
27 : 24	PDAC	PDAC input. Each increment in PDAC causes an increase of ~0.10V in VPOS Default Value: X
23 : 0	PERIOD	Period of timer in clk_spcif_timer ticks. For regular FLASH, clock is 36MHz from dedicated oscillator. For FLASH-Lite, clock is same as clk_hf, which must be set to 48MHz for 48MHz devices and 12MHz for max 16MHz devices Default Value: X

30.1.1636SFLASH_ALT_ES_E

Erase Sector - Erase Settings

Address: 0x0FFFFB34

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	PERIOD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	None				None			
Name	NDAC [31:28]				PDAC [27:24]			

Bits	Name	Description
31 : 28	NDAC	NDAC input. Each increment in NDAC causes an increase of ~0.10V in VNEG Default Value: X
27 : 24	PDAC	PDAC input. Each increment in PDAC causes an increase of ~0.10V in VPOS Default Value: X
23 : 0	PERIOD	Period of timer in clk_spcif_timer ticks. For regular FLASH, clock is 36MHz from dedicated oscillator. For FLASH-Lite, clock is same as clk_hf, which must be set to 48MHz for 48MHz devices and 12MHz for max 16MHz devices Default Value: X

30.1.1637SFLASH_ALT_ES_P_EO

Erase Sector - Program EO Settings

Address: 0x0FFFFB38

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	None							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	None							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	None							
Name	PERIOD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	None				None			
Name	NDAC [31:28]				PDAC [27:24]			

Bits	Name	Description
31 : 28	NDAC	NDAC input. Each increment in NDAC causes an increase of ~0.10V in VNEG Default Value: X
27 : 24	PDAC	PDAC input. Each increment in PDAC causes an increase of ~0.10V in VPOS Default Value: X
23 : 0	PERIOD	Period of timer in clk_spcif_timer ticks. For regular FLASH, clock is 36MHz from dedicated oscillator. For FLASH-Lite, clock is same as clk_hf, which must be set to 48MHz for 48MHz devices and 12MHz for max 16MHz devices Default Value: X

30.1.1638SFLASH_ALT_E_VCTAT

Bandgap Trim Register

Address: 0x0FFFFB3C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	RW		RW			
HW Access	None	None	None		None			
Name	None	VCTAT_ENABLE	VCTAT_VOLTAGE [5:4]		VCTAT_SLOPE [3:0]			

Bits	Name	Description
6	VCTAT_ENABLE	Enable VCTAT block Default Value: X
5 : 4	VCTAT_VOLTAGE	Output voltage absolute trim Default Value: X
3 : 0	VCTAT_SLOPE	Output slope setting controls. The slope of the voltage with temperature varies from ~0% to ~15% from the value at 55C over the temperature range -40C to 150C based on control signal settings 0 to 15 Default Value: X

30.1.1639SFLASH_ALT_P_VCTAT

Bandgap Trim Register

Address: 0x0FFFFB3D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	RW		RW			
HW Access	None	None	None		None			
Name	None	VCTAT_ENABLE	VCTAT_VOLTAGE [5:4]		VCTAT_SLOPE [3:0]			

Bits	Name	Description
6	VCTAT_ENABLE	Enable VCTAT block Default Value: X
5 : 4	VCTAT_VOLTAGE	Output voltage absolute trim Default Value: X
3 : 0	VCTAT_SLOPE	Output slope setting controls. The slope of the voltage with temperature varies from ~0% to ~15% from the value at 55C over the temperature range -40C to 150C based on control signal settings 0 to 15 Default Value: X

31 SPC Interface (SPCIF) Registers

This section discusses the SPCIF registers. It lists all the registers in mapping tables, in address order.

31.1 Register Details

Register Name	Address
SPCIF_GEOMETRY	0x40110000
SPCIF_INTR	0x401107F0
SPCIF_INTR_SET	0x401107F4
SPCIF_INTR_MASK	0x401107F8
SPCIF_INTR_MASKED	0x401107FC

31.1.1 SPCIF_GEOMETRY

Flash/NVL geometry information

Address: 0x40110000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	FLASH [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	FLASH [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R		R		R			
HW Access	W		W		W			
Name	FLASH_ROW [23:22]		NUM_FLASH [21:20]		SFLASH [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW	R						
HW Access	None	W						
Name	DE_CPD_LP	NVL [30:24]						

Bits	Name	Description
31	DE_CPD_LP	0': SRAM busy wait loop has not been copied. '1': Busy wait loop has been written into SRAM. Default Value: 0
30 : 24	NVL	NVLatch size in Byte multiples (chip dependent): "0": 0 Bytes "1": 1 Byte ... "127": 127 Bytes Default Value: Undefined

(continued)

23 : 22	FLASH_ROW	Page size in 64 Byte multiples (chip dependent): "0": 64 byte "1": 128 byte "2": 192 byte "3": 256 byte The page size is used to detemine the number of Bytes in a page for Flash page based operations (e.g. PGM_PAGE). Note: the field name FLASH_ROW is misleading, as this field specifies the number of Bytes in a page, rather than the number of Bytes in a row. In a single plane flash macro architecture, a page consists of a single row. However, in a multi plane flash macro architecture, a page consists of multiple rows from different planes. Default Value: Undefined
21 : 20	NUM_FLASH	Number of flash macros (chip dependent): "0": 1 flash macro "1": 2 flash macros "2": 3 flash macros "3": 4 flash macros Default Value: Undefined
19 : 16	SFLASH	Supervisory flash capacity in 256 Byte multiples (chip dependent). If multiple flash macros are present, this field provides the supervisory flash capacity of all flash macros together: "0": 256 Bytes. "1": 2*256 Bytes. ... "15": 16*256 Bytes. Default Value: Undefined
15 : 0	FLASH	Regular flash capacity in 256 Byte multiples (chip dependent). If multiple flash macros are present, this field provides the flash capacity of all flash macros together: "0": 256 Bytes. "1": 2*256 Bytes. ... "65535": 65536*256 Bytes. Default Value: Undefined

31.1.2 SPCIF_INTR

SPCIF interrupt request register

Address: 0x401107F0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1C
HW Access	None							RW1S
Name	None [7:1]							TIMER

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	TIMER	Timer counter value reaches "0". Set to '1', when event is detected. Write INTR field with '1', to clear bit. Write INTR_SET field with '1', to set bit. Default Value: 0

31.1.3 SPCIF_INTR_SET

SPCIF interrupt set request register

Address: 0x401107F4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1S
HW Access	None							A
Name	None [7:1]							TIMER

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	TIMER	Write INTR_SET field with '1' to set corresponding INTR field. Default Value: 0

31.1.4 SPCIF_INTR_MASK

SPCIF interrupt mask register

Address: 0x401107F8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							TIMER

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	TIMER	Mask for corresponding field in INTR register. Default Value: 0

31.1.5 SPCIF_INTR_MASKED

SPCIF interrupt masked request register

Address: 0x401107FC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							W
Name	None [7:1]							TIMER

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	TIMER	Logical and of corresponding request and mask fields. Default Value: 0

32 TCPWM Registers

This section discusses the TCPWM registers. It lists all the registers in mapping tables, in address order.

32.1 Register Details

Register Name	Address
TCPWM_CTRL	0x40200000
TCPWM_CMD	0x40200008
TCPWM_INTR_CAUSE	0x4020000C

32.1.1 TCPWM_CTRL

TCPWM control register 0.

Address: 0x40200000

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				COUNTER_ENABLED [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	COUNTER_ENABLED	Counter enables for counters 0 up to CNT_NR-1. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_CTRL0, TR_CTRL1, and TR_CTRL2 register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_overflow", "tr_underflow" and "tr_compare_match"). - the counter's line outputs ("line_out" and "line_compl_out"). Default Value: 0

32.1.2 TCPWM_CMD

TCPWM command register.

Address: 0x40200008

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1S			
HW Access	None				RW1C			
Name	None [7:4]				COUNTER_CAPTURE [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW1S			
HW Access	None				RW1C			
Name	None [15:12]				COUNTER_RELOAD [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW1S			
HW Access	None				RW1C			
Name	None [23:20]				COUNTER_STOP [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None				RW1S			
HW Access	None				RW1C			
Name	None [31:28]				COUNTER_START [27:24]			

Bits	Name	Description
27 : 24	COUNTER_START	Counters SW start trigger. For HW behavior, see COUNTER_CAPTURE field. Default Value: 0
19 : 16	COUNTER_STOP	Counters SW stop trigger. For HW behavior, see COUNTER_CAPTURE field. Default Value: 0
11 : 8	COUNTER_RELOAD	Counters SW reload trigger. For HW behavior, see COUNTER_CAPTURE field. Default Value: 0
3 : 0	COUNTER_CAPTURE	Counters SW capture trigger. When written with '1', a capture trigger is generated and the HW sets the field to '0' when the SW trigger has taken effect. It should be noted that the HW operates on the counter frequency. If the counter is disabled through CTRL.COUNTER_ENABLED, the field is immediately set to '0'. Default Value: 0

32.1.3 TCPWM_INTR_CAUSE

TCPWM Counter interrupt cause register.

Address: 0x4020000C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R			
HW Access	None				W			
Name	None [7:4]				COUNTER_INT [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	COUNTER_INT	Counters interrupt signal active. If the counter is disabled through CTRL.COUNTER_ENABLED, the associated interrupt field is immediately set to '0'. Default Value: 0

33 Test (TST) Registers

This section discusses the TST registers. It lists all the registers in mapping tables, in address order.

33.1 Register Details

Register Name	Address
TST_MODE	0x40030014

33.1.1 TST_MODE

Test Mode Control Register

Address: 0x40030014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					R	None	
HW Access	None					RW	None	
Name	None [7:3]					SWD_CONNECTED	None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	R	None					
HW Access	R	RW	None					
Name	TEST_MODE	POR_BYPASS	None [29:24]					

Bits	Name	Description
31	TEST_MODE	0: Normal operation mode 1: Test mode (any test mode) Setting this bit will prevent BootROM from yielding execution to Flash image. Default Value: 0
30	POR_BYPASS	This bit is set during POR bypass mode. When this bit is set, the BootROM will not yield execution to the FLASH image (same function as setting TEST_MODE bit below). Default Value: 0
2	SWD_CONNECTED	0: SWD not active 1: SWD activated (Line Reset & Connect sequence passed) (Note: this bit replaces TST_CTRL.SWD_CONNECTED) Default Value: 0

34 UDB Interface (UDBIF) Registers

This section discusses the UDBIF registers. It lists all the registers in mapping tables, in address order.

34.1 Register Details

Register Name	Address
UDB_UDBIF_BANK_CTL	0x400F7000
UDB_UDBIF_WAIT_CFG	0x400F7001
UDB_UDBIF_INT_CLK_CTL	0x400F701C

34.1.1 UDB_UDBIF_BANK_CTL

Bank Control

Address: 0x400F7000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	None		RW	RW	RW	RW	RW
HW Access	R	None		R	R	R	R	R
Name	GLBL_WR	None [6:5]		PIPE	LOCK	BANK_EN	ROUTE_EN	DIS_COR

Bits	Name	Description
7	GLBL_WR	UDB Array Global Writing Option Default Value: 0 **0x0: DISABLE:** Global Writes disabled **0x1: ENABLE:** Global Writes enabled
4	PIPE	Pipelining Control Default Value: 0 **0x0: BYPASS:** Pipelining bypassed **0x1: PIPELINED:** Pipelining enabled
3	LOCK	UDB Array Configuration Locking Default Value: 0 **0x0: MUTABLE:** UDB Array configuration is writable **0x1: LOCKED:** UDB Array configuration is locked
2	BANK_EN	Enable Bank Default Value: 0 **0x0: DISABLE:** Bank disabled **0x1: ENABLE:** Bank enabled
1	ROUTE_EN	Enable Routing Default Value: 0 **0x0: DISABLE:** Routing disabled **0x1: ENABLE:** Routing enabled
0	DIS_COR	Selection of Clear-On-Read Default Value: 0

(continued)

0x0: NORMAL:
Clear-On-Read enabled

0x1: DISABLE:
Clear-On-Read disabled

34.1.2 UDB_UDBIF_WAIT_CFG

Wait States Configuration

Address: 0x400F7001

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	WR_WRK_WAIT [7:6]		RD_WRK_WAIT [5:4]		WR_CFG_WAIT [3:2]		RD_CFG_WAIT [1:0]	

Bits	Name	Description
7 : 6	WR_WRK_WAIT	Write Work Wait States Default Value: 0 **0x0: ONE_WAIT:** 1 wait states **0x1: TWO_WAITS:** 2 wait states **0x2: THREE_WAITS:** 3 wait states **0x3: ZERO_WAITS:** 0 wait state
5 : 4	RD_WRK_WAIT	Read Work Wait States Default Value: 0 **0x0: ONE_WAIT:** 1 wait states **0x1: TWO_WAITS:** 2 wait states **0x2: THREE_WAITS:** 3 wait states **0x3: ZERO_WAITS:** 0 wait state
3 : 2	WR_CFG_WAIT	Write Configuration Wait States Default Value: 0 **0x0: ONE_WAIT:** 1 wait states **0x1: TWO_WAITS:** 2 wait states **0x2: THREE_WAITS:** 3 wait states **0x3: ZERO_WAITS:** 0 wait state
1 : 0	RD_CFG_WAIT	Read Configuration Wait States Default Value: 0

(continued)

0x0: FIVE_WAITS:
5 wait states

0x1: FOUR_WAITS:
4 wait states

0x2: THREE_WAITS:
3 wait states

0x3: ONE_WAIT:
1 wait state

34.1.3 UDB_UDBIF_INT_CLK_CTL

Interrupt Synchronizer Clock Control

Address: 0x400F701C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							EN_HFCLK

Bits	Name	Description
0	EN_HFCLK	This bit enables the interrupt synchronizer in the UDB interface. It needs to be set whenever UDB/DSI interrupts are used. Disabling the interrupt synchronizer saves power in Active/Sleep mode. Default Value: 0

35 UDB Registers

This section discusses the UDB registers. It lists all the registers in mapping tables, in address order.

35.1 Register Details

Register Name	Address
UDB_INT_CFG	0x400F8000

35.1.1 UDB_INT_CFG

UDB Subsystem Interrupt Configuration

Address: 0x400F8000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	INT_MODE_CFG [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	INT_MODE_CFG	Interrupt Mode; bit position corresponds to interrupt Default Value: 0 **0x0: LEVEL:** Level **0x1: PULSE:** Pulse

36 Single UDB (UDBSNG) Registers

This section discusses the UDBSNG registers. It lists all the registers in mapping tables, in address order.

36.1 Register Details

Register Name	Address
UDB_P0_U0_PLD_IT0	0x400F3000
UDB_P0_U0_PLD_IT1	0x400F3004
UDB_P0_U0_PLD_IT2	0x400F3008
UDB_P0_U0_PLD_IT3	0x400F300C
UDB_P0_U0_PLD_IT4	0x400F3010
UDB_P0_U0_PLD_IT5	0x400F3014
UDB_P0_U0_PLD_IT6	0x400F3018
UDB_P0_U0_PLD_IT7	0x400F301C
UDB_P0_U0_PLD_IT8	0x400F3020
UDB_P0_U0_PLD_IT9	0x400F3024
UDB_P0_U0_PLD_IT10	0x400F3028
UDB_P0_U0_PLD_IT11	0x400F302C
UDB_P0_U0_PLD_ORT0	0x400F3030
UDB_P0_U0_PLD_ORT1	0x400F3032
UDB_P0_U0_PLD_ORT2	0x400F3034
UDB_P0_U0_PLD_ORT3	0x400F3036
UDB_P0_U0_PLD_MC_CFG_CEN_CONST	0x400F3038
UDB_P0_U0_PLD_MC_CFG_XORFB	0x400F303A
UDB_P0_U0_PLD_MC_SET_RESET	0x400F303C
UDB_P0_U0_PLD_MC_CFG_BYPASS	0x400F303E
UDB_P0_U0_CFG0	0x400F3040
UDB_P0_U0_CFG1	0x400F3041
UDB_P0_U0_CFG2	0x400F3042
UDB_P0_U0_CFG3	0x400F3043
UDB_P0_U0_CFG4	0x400F3044
UDB_P0_U0_CFG5	0x400F3045
UDB_P0_U0_CFG6	0x400F3046

Register Name	Address
UDB_P0_U0_CFG7	0x400F3047
UDB_P0_U0_CFG8	0x400F3048
UDB_P0_U0_CFG9	0x400F3049
UDB_P0_U0_CFG10	0x400F304A
UDB_P0_U0_CFG11	0x400F304B
UDB_P0_U0_CFG12	0x400F304C
UDB_P0_U0_CFG13	0x400F304D
UDB_P0_U0_CFG14	0x400F304E
UDB_P0_U0_CFG15	0x400F304F
UDB_P0_U0_CFG16	0x400F3050
UDB_P0_U0_CFG17	0x400F3051
UDB_P0_U0_CFG18	0x400F3052
UDB_P0_U0_CFG19	0x400F3053
UDB_P0_U0_CFG20	0x400F3054
UDB_P0_U0_CFG21	0x400F3055
UDB_P0_U0_CFG22	0x400F3056
UDB_P0_U0_CFG23	0x400F3057
UDB_P0_U0_CFG24	0x400F3058
UDB_P0_U0_CFG25	0x400F3059
UDB_P0_U0_CFG26	0x400F305A
UDB_P0_U0_CFG27	0x400F305B
UDB_P0_U0_CFG28	0x400F305C
UDB_P0_U0_CFG29	0x400F305D
UDB_P0_U0_CFG30	0x400F305E
UDB_P0_U0_CFG31	0x400F305F
UDB_P0_U0_DCFG0	0x400F3060
UDB_P0_U0_DCFG1	0x400F3062
UDB_P0_U0_DCFG2	0x400F3064
UDB_P0_U0_DCFG3	0x400F3066
UDB_P0_U0_DCFG4	0x400F3068
UDB_P0_U0_DCFG5	0x400F306A
UDB_P0_U0_DCFG6	0x400F306C
UDB_P0_U0_DCFG7	0x400F306E
UDB_P0_U1_PLD_IT0	0x400F3080
UDB_P0_U1_PLD_IT1	0x400F3084
UDB_P0_U1_PLD_IT2	0x400F3088
UDB_P0_U1_PLD_IT3	0x400F308C
UDB_P0_U1_PLD_IT4	0x400F3090
UDB_P0_U1_PLD_IT5	0x400F3094
UDB_P0_U1_PLD_IT6	0x400F3098
UDB_P0_U1_PLD_IT7	0x400F309C
UDB_P0_U1_PLD_IT8	0x400F30A0

Register Name	Address
UDB_P0_U1_PLD_IT9	0x400F30A4
UDB_P0_U1_PLD_IT10	0x400F30A8
UDB_P0_U1_PLD_IT11	0x400F30AC
UDB_P0_U1_PLD_ORT0	0x400F30B0
UDB_P0_U1_PLD_ORT1	0x400F30B2
UDB_P0_U1_PLD_ORT2	0x400F30B4
UDB_P0_U1_PLD_ORT3	0x400F30B6
UDB_P0_U1_PLD_MC_CFG_CEN_CONST	0x400F30B8
UDB_P0_U1_PLD_MC_CFG_XORFB	0x400F30BA
UDB_P0_U1_PLD_MC_SET_RESET	0x400F30BC
UDB_P0_U1_PLD_MC_CFG_BYPASS	0x400F30BE
UDB_P0_U1_CFG0	0x400F30C0
UDB_P0_U1_CFG1	0x400F30C1
UDB_P0_U1_CFG2	0x400F30C2
UDB_P0_U1_CFG3	0x400F30C3
UDB_P0_U1_CFG4	0x400F30C4
UDB_P0_U1_CFG5	0x400F30C5
UDB_P0_U1_CFG6	0x400F30C6
UDB_P0_U1_CFG7	0x400F30C7
UDB_P0_U1_CFG8	0x400F30C8
UDB_P0_U1_CFG9	0x400F30C9
UDB_P0_U1_CFG10	0x400F30CA
UDB_P0_U1_CFG11	0x400F30CB
UDB_P0_U1_CFG12	0x400F30CC
UDB_P0_U1_CFG13	0x400F30CD
UDB_P0_U1_CFG14	0x400F30CE
UDB_P0_U1_CFG15	0x400F30CF
UDB_P0_U1_CFG16	0x400F30D0
UDB_P0_U1_CFG17	0x400F30D1
UDB_P0_U1_CFG18	0x400F30D2
UDB_P0_U1_CFG19	0x400F30D3
UDB_P0_U1_CFG20	0x400F30D4
UDB_P0_U1_CFG21	0x400F30D5
UDB_P0_U1_CFG22	0x400F30D6
UDB_P0_U1_CFG23	0x400F30D7
UDB_P0_U1_CFG24	0x400F30D8
UDB_P0_U1_CFG25	0x400F30D9
UDB_P0_U1_CFG26	0x400F30DA
UDB_P0_U1_CFG27	0x400F30DB
UDB_P0_U1_CFG28	0x400F30DC
UDB_P0_U1_CFG29	0x400F30DD
UDB_P0_U1_CFG30	0x400F30DE

Register Name	Address
UDB_P0_U1_CFG31	0x400F30DF
UDB_P0_U1_DCFG0	0x400F30E0
UDB_P0_U1_DCFG1	0x400F30E2
UDB_P0_U1_DCFG2	0x400F30E4
UDB_P0_U1_DCFG3	0x400F30E6
UDB_P0_U1_DCFG4	0x400F30E8
UDB_P0_U1_DCFG5	0x400F30EA
UDB_P0_U1_DCFG6	0x400F30EC
UDB_P0_U1_DCFG7	0x400F30EE
UDB_P1_U0_PLD_IT0	0x400F3200
UDB_P1_U0_PLD_IT1	0x400F3204
UDB_P1_U0_PLD_IT2	0x400F3208
UDB_P1_U0_PLD_IT3	0x400F320C
UDB_P1_U0_PLD_IT4	0x400F3210
UDB_P1_U0_PLD_IT5	0x400F3214
UDB_P1_U0_PLD_IT6	0x400F3218
UDB_P1_U0_PLD_IT7	0x400F321C
UDB_P1_U0_PLD_IT8	0x400F3220
UDB_P1_U0_PLD_IT9	0x400F3224
UDB_P1_U0_PLD_IT10	0x400F3228
UDB_P1_U0_PLD_IT11	0x400F322C
UDB_P1_U0_PLD_ORT0	0x400F3230
UDB_P1_U0_PLD_ORT1	0x400F3232
UDB_P1_U0_PLD_ORT2	0x400F3234
UDB_P1_U0_PLD_ORT3	0x400F3236
UDB_P1_U0_PLD_MC_CFG_CEN_CONST	0x400F3238
UDB_P1_U0_PLD_MC_CFG_XORFB	0x400F323A
UDB_P1_U0_PLD_MC_SET_RESET	0x400F323C
UDB_P1_U0_PLD_MC_CFG_BYPASS	0x400F323E
UDB_P1_U0_CFG0	0x400F3240
UDB_P1_U0_CFG1	0x400F3241
UDB_P1_U0_CFG2	0x400F3242
UDB_P1_U0_CFG3	0x400F3243
UDB_P1_U0_CFG4	0x400F3244
UDB_P1_U0_CFG5	0x400F3245
UDB_P1_U0_CFG6	0x400F3246
UDB_P1_U0_CFG7	0x400F3247
UDB_P1_U0_CFG8	0x400F3248
UDB_P1_U0_CFG9	0x400F3249
UDB_P1_U0_CFG10	0x400F324A
UDB_P1_U0_CFG11	0x400F324B
UDB_P1_U0_CFG12	0x400F324C

Register Name	Address
UDB_P1_U0_CFG13	0x400F324D
UDB_P1_U0_CFG14	0x400F324E
UDB_P1_U0_CFG15	0x400F324F
UDB_P1_U0_CFG16	0x400F3250
UDB_P1_U0_CFG17	0x400F3251
UDB_P1_U0_CFG18	0x400F3252
UDB_P1_U0_CFG19	0x400F3253
UDB_P1_U0_CFG20	0x400F3254
UDB_P1_U0_CFG21	0x400F3255
UDB_P1_U0_CFG22	0x400F3256
UDB_P1_U0_CFG23	0x400F3257
UDB_P1_U0_CFG24	0x400F3258
UDB_P1_U0_CFG25	0x400F3259
UDB_P1_U0_CFG26	0x400F325A
UDB_P1_U0_CFG27	0x400F325B
UDB_P1_U0_CFG28	0x400F325C
UDB_P1_U0_CFG29	0x400F325D
UDB_P1_U0_CFG30	0x400F325E
UDB_P1_U0_CFG31	0x400F325F
UDB_P1_U0_DCFG0	0x400F3260
UDB_P1_U0_DCFG1	0x400F3262
UDB_P1_U0_DCFG2	0x400F3264
UDB_P1_U0_DCFG3	0x400F3266
UDB_P1_U0_DCFG4	0x400F3268
UDB_P1_U0_DCFG5	0x400F326A
UDB_P1_U0_DCFG6	0x400F326C
UDB_P1_U0_DCFG7	0x400F326E
UDB_P1_U1_PLD_IT0	0x400F3280
UDB_P1_U1_PLD_IT1	0x400F3284
UDB_P1_U1_PLD_IT2	0x400F3288
UDB_P1_U1_PLD_IT3	0x400F328C
UDB_P1_U1_PLD_IT4	0x400F3290
UDB_P1_U1_PLD_IT5	0x400F3294
UDB_P1_U1_PLD_IT6	0x400F3298
UDB_P1_U1_PLD_IT7	0x400F329C
UDB_P1_U1_PLD_IT8	0x400F32A0
UDB_P1_U1_PLD_IT9	0x400F32A4
UDB_P1_U1_PLD_IT10	0x400F32A8
UDB_P1_U1_PLD_IT11	0x400F32AC
UDB_P1_U1_PLD_ORT0	0x400F32B0
UDB_P1_U1_PLD_ORT1	0x400F32B2
UDB_P1_U1_PLD_ORT2	0x400F32B4

Register Name	Address
UDB_P1_U1_PLD_ORT3	0x400F32B6
UDB_P1_U1_PLD_MC_CFG_CEN_CONST	0x400F32B8
UDB_P1_U1_PLD_MC_CFG_XORFB	0x400F32BA
UDB_P1_U1_PLD_MC_SET_RESET	0x400F32BC
UDB_P1_U1_PLD_MC_CFG_BYPASS	0x400F32BE
UDB_P1_U1_CFG0	0x400F32C0
UDB_P1_U1_CFG1	0x400F32C1
UDB_P1_U1_CFG2	0x400F32C2
UDB_P1_U1_CFG3	0x400F32C3
UDB_P1_U1_CFG4	0x400F32C4
UDB_P1_U1_CFG5	0x400F32C5
UDB_P1_U1_CFG6	0x400F32C6
UDB_P1_U1_CFG7	0x400F32C7
UDB_P1_U1_CFG8	0x400F32C8
UDB_P1_U1_CFG9	0x400F32C9
UDB_P1_U1_CFG10	0x400F32CA
UDB_P1_U1_CFG11	0x400F32CB
UDB_P1_U1_CFG12	0x400F32CC
UDB_P1_U1_CFG13	0x400F32CD
UDB_P1_U1_CFG14	0x400F32CE
UDB_P1_U1_CFG15	0x400F32CF
UDB_P1_U1_CFG16	0x400F32D0
UDB_P1_U1_CFG17	0x400F32D1
UDB_P1_U1_CFG18	0x400F32D2
UDB_P1_U1_CFG19	0x400F32D3
UDB_P1_U1_CFG20	0x400F32D4
UDB_P1_U1_CFG21	0x400F32D5
UDB_P1_U1_CFG22	0x400F32D6
UDB_P1_U1_CFG23	0x400F32D7
UDB_P1_U1_CFG24	0x400F32D8
UDB_P1_U1_CFG25	0x400F32D9
UDB_P1_U1_CFG26	0x400F32DA
UDB_P1_U1_CFG27	0x400F32DB
UDB_P1_U1_CFG28	0x400F32DC
UDB_P1_U1_CFG29	0x400F32DD
UDB_P1_U1_CFG30	0x400F32DE
UDB_P1_U1_CFG31	0x400F32DF
UDB_P1_U1_DCFG0	0x400F32E0
UDB_P1_U1_DCFG1	0x400F32E2
UDB_P1_U1_DCFG2	0x400F32E4
UDB_P1_U1_DCFG3	0x400F32E6
UDB_P1_U1_DCFG4	0x400F32E8

Register Name	Address
UDB_P1_U1_DCFG5	0x400F32EA
UDB_P1_U1_DCFG6	0x400F32EC
UDB_P1_U1_DCFG7	0x400F32EE

36.1.1 UDB_P0_U0_PLD_IT0

PLD Input Terms

Address: 0x400F3000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Bits	Name	Description
31	PLD1_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X

(continued)

25	PLD1_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
22	PLD0_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X

(continued)

3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X

36.1.2 UDB_P0_U0_PLD_IT1

PLD Input Terms

Address: 0x400F3004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Bits	Name	Description
31	PLD1_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X

(continued)

25	PLD1_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
22	PLD0_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X

(continued)

3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X

36.1.3 UDB_P0_U0_PLD_IT2

PLD Input Terms

Address: 0x400F3008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Bits	Name	Description
31	PLD1_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X

(continued)

25	PLD1_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
22	PLD0_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X

(continued)

3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X

36.1.4 UDB_P0_U0_PLD_IT3

PLD Input Terms

Address: 0x400F300C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Bits	Name	Description
31	PLD1_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X

(continued)

25	PLD1_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
22	PLD0_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X

(continued)

3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X

36.1.5 UDB_P0_U0_PLD_IT4

PLD Input Terms

Address: 0x400F3010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Bits	Name	Description
31	PLD1_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X

(continued)

25	PLD1_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
22	PLD0_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X

(continued)

3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X

36.1.6 UDB_P0_U0_PLD_IT5

PLD Input Terms

Address: 0x400F3014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Bits	Name	Description
31	PLD1_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X

(continued)

25	PLD1_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
22	PLD0_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X

(continued)

3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X

36.1.7 UDB_P0_U0_PLD_IT6

PLD Input Terms

Address: 0x400F3018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Bits	Name	Description
31	PLD1_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X

(continued)

25	PLD1_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
22	PLD0_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X

(continued)

3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X

36.1.8 UDB_P0_U0_PLD_IT7

PLD Input Terms

Address: 0x400F301C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Bits	Name	Description
31	PLD1_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X

(continued)

25	PLD1_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
22	PLD0_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X

(continued)

3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X

36.1.9 UDB_P0_U0_PLD_IT8

PLD Input Terms

Address: 0x400F3020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Bits	Name	Description
31	PLD1_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X

(continued)

25	PLD1_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
22	PLD0_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X

(continued)

3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X

36.1.10 UDB_P0_U0_PLD_IT9

PLD Input Terms

Address: 0x400F3024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Bits	Name	Description
31	PLD1_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X

(continued)

25	PLD1_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
22	PLD0_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X

(continued)

3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X

36.1.11 UDB_P0_U0_PLD_IT10

PLD Input Terms

Address: 0x400F3028

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Bits	Name	Description
31	PLD1_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X

(continued)

25	PLD1_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
22	PLD0_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X

(continued)

3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X

36.1.12 UDB_P0_U0_PLD_IT11

PLD Input Terms

Address: 0x400F302C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Bits	Name	Description
31	PLD1_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X

(continued)

25	PLD1_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
22	PLD0_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X

(continued)

3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X

36.1.13 UDB_P0_U0_PLD_ORT0

PLD OR Terms

Address: 0x400F3030

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ORT_PTx_7	PLD0_ORT_PTx_6	PLD0_ORT_PTx_5	PLD0_ORT_PTx_4	PLD0_ORT_PTx_3	PLD0_ORT_PTx_2	PLD0_ORT_PTx_1	PLD0_ORT_PTx_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ORT_PTx_7	PLD1_ORT_PTx_6	PLD1_ORT_PTx_5	PLD1_ORT_PTx_4	PLD1_ORT_PTx_3	PLD1_ORT_PTx_2	PLD1_ORT_PTx_1	PLD1_ORT_PTx_0

Bits	Name	Description
15	PLD1_ORT_PTx_7	OR term. Bit position corresponds to product term. Default Value: X
14	PLD1_ORT_PTx_6	OR term. Bit position corresponds to product term. Default Value: X
13	PLD1_ORT_PTx_5	OR term. Bit position corresponds to product term. Default Value: X
12	PLD1_ORT_PTx_4	OR term. Bit position corresponds to product term. Default Value: X
11	PLD1_ORT_PTx_3	OR term. Bit position corresponds to product term. Default Value: X
10	PLD1_ORT_PTx_2	OR term. Bit position corresponds to product term. Default Value: X
9	PLD1_ORT_PTx_1	OR term. Bit position corresponds to product term. Default Value: X
8	PLD1_ORT_PTx_0	OR term. Bit position corresponds to product term. Default Value: X
7	PLD0_ORT_PTx_7	OR term. Bit position corresponds to product term. Default Value: X
6	PLD0_ORT_PTx_6	OR term. Bit position corresponds to product term. Default Value: X
5	PLD0_ORT_PTx_5	OR term. Bit position corresponds to product term. Default Value: X
4	PLD0_ORT_PTx_4	OR term. Bit position corresponds to product term. Default Value: X

(continued)

3	PLD0_ORT_PTx_3	OR term. Bit position corresponds to product term. Default Value: X
2	PLD0_ORT_PTx_2	OR term. Bit position corresponds to product term. Default Value: X
1	PLD0_ORT_PTx_1	OR term. Bit position corresponds to product term. Default Value: X
0	PLD0_ORT_PTx_0	OR term. Bit position corresponds to product term. Default Value: X

36.1.14 UDB_P0_U0_PLD_ORT1

PLD OR Terms

Address: 0x400F3032

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ORT_PTx_7	PLD0_ORT_PTx_6	PLD0_ORT_PTx_5	PLD0_ORT_PTx_4	PLD0_ORT_PTx_3	PLD0_ORT_PTx_2	PLD0_ORT_PTx_1	PLD0_ORT_PTx_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ORT_PTx_7	PLD1_ORT_PTx_6	PLD1_ORT_PTx_5	PLD1_ORT_PTx_4	PLD1_ORT_PTx_3	PLD1_ORT_PTx_2	PLD1_ORT_PTx_1	PLD1_ORT_PTx_0

Bits	Name	Description
15	PLD1_ORT_PTx_7	OR term. Bit position corresponds to product term. Default Value: X
14	PLD1_ORT_PTx_6	OR term. Bit position corresponds to product term. Default Value: X
13	PLD1_ORT_PTx_5	OR term. Bit position corresponds to product term. Default Value: X
12	PLD1_ORT_PTx_4	OR term. Bit position corresponds to product term. Default Value: X
11	PLD1_ORT_PTx_3	OR term. Bit position corresponds to product term. Default Value: X
10	PLD1_ORT_PTx_2	OR term. Bit position corresponds to product term. Default Value: X
9	PLD1_ORT_PTx_1	OR term. Bit position corresponds to product term. Default Value: X
8	PLD1_ORT_PTx_0	OR term. Bit position corresponds to product term. Default Value: X
7	PLD0_ORT_PTx_7	OR term. Bit position corresponds to product term. Default Value: X
6	PLD0_ORT_PTx_6	OR term. Bit position corresponds to product term. Default Value: X
5	PLD0_ORT_PTx_5	OR term. Bit position corresponds to product term. Default Value: X
4	PLD0_ORT_PTx_4	OR term. Bit position corresponds to product term. Default Value: X

(continued)

3	PLD0_ORT_PTx_3	OR term. Bit position corresponds to product term. Default Value: X
2	PLD0_ORT_PTx_2	OR term. Bit position corresponds to product term. Default Value: X
1	PLD0_ORT_PTx_1	OR term. Bit position corresponds to product term. Default Value: X
0	PLD0_ORT_PTx_0	OR term. Bit position corresponds to product term. Default Value: X

36.1.15 UDB_P0_U0_PLD_ORT2

PLD OR Terms

Address: 0x400F3034

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ORT_PTx_7	PLD0_ORT_PTx_6	PLD0_ORT_PTx_5	PLD0_ORT_PTx_4	PLD0_ORT_PTx_3	PLD0_ORT_PTx_2	PLD0_ORT_PTx_1	PLD0_ORT_PTx_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ORT_PTx_7	PLD1_ORT_PTx_6	PLD1_ORT_PTx_5	PLD1_ORT_PTx_4	PLD1_ORT_PTx_3	PLD1_ORT_PTx_2	PLD1_ORT_PTx_1	PLD1_ORT_PTx_0

Bits	Name	Description
15	PLD1_ORT_PTx_7	OR term. Bit position corresponds to product term. Default Value: X
14	PLD1_ORT_PTx_6	OR term. Bit position corresponds to product term. Default Value: X
13	PLD1_ORT_PTx_5	OR term. Bit position corresponds to product term. Default Value: X
12	PLD1_ORT_PTx_4	OR term. Bit position corresponds to product term. Default Value: X
11	PLD1_ORT_PTx_3	OR term. Bit position corresponds to product term. Default Value: X
10	PLD1_ORT_PTx_2	OR term. Bit position corresponds to product term. Default Value: X
9	PLD1_ORT_PTx_1	OR term. Bit position corresponds to product term. Default Value: X
8	PLD1_ORT_PTx_0	OR term. Bit position corresponds to product term. Default Value: X
7	PLD0_ORT_PTx_7	OR term. Bit position corresponds to product term. Default Value: X
6	PLD0_ORT_PTx_6	OR term. Bit position corresponds to product term. Default Value: X
5	PLD0_ORT_PTx_5	OR term. Bit position corresponds to product term. Default Value: X
4	PLD0_ORT_PTx_4	OR term. Bit position corresponds to product term. Default Value: X

(continued)

3	PLD0_ORT_PTx_3	OR term. Bit position corresponds to product term. Default Value: X
2	PLD0_ORT_PTx_2	OR term. Bit position corresponds to product term. Default Value: X
1	PLD0_ORT_PTx_1	OR term. Bit position corresponds to product term. Default Value: X
0	PLD0_ORT_PTx_0	OR term. Bit position corresponds to product term. Default Value: X

36.1.16 UDB_P0_U0_PLD_ORT3

PLD OR Terms

Address: 0x400F3036

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ORT_PTx_7	PLD0_ORT_PTx_6	PLD0_ORT_PTx_5	PLD0_ORT_PTx_4	PLD0_ORT_PTx_3	PLD0_ORT_PTx_2	PLD0_ORT_PTx_1	PLD0_ORT_PTx_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ORT_PTx_7	PLD1_ORT_PTx_6	PLD1_ORT_PTx_5	PLD1_ORT_PTx_4	PLD1_ORT_PTx_3	PLD1_ORT_PTx_2	PLD1_ORT_PTx_1	PLD1_ORT_PTx_0

Bits	Name	Description
15	PLD1_ORT_PTx_7	OR term. Bit position corresponds to product term. Default Value: X
14	PLD1_ORT_PTx_6	OR term. Bit position corresponds to product term. Default Value: X
13	PLD1_ORT_PTx_5	OR term. Bit position corresponds to product term. Default Value: X
12	PLD1_ORT_PTx_4	OR term. Bit position corresponds to product term. Default Value: X
11	PLD1_ORT_PTx_3	OR term. Bit position corresponds to product term. Default Value: X
10	PLD1_ORT_PTx_2	OR term. Bit position corresponds to product term. Default Value: X
9	PLD1_ORT_PTx_1	OR term. Bit position corresponds to product term. Default Value: X
8	PLD1_ORT_PTx_0	OR term. Bit position corresponds to product term. Default Value: X
7	PLD0_ORT_PTx_7	OR term. Bit position corresponds to product term. Default Value: X
6	PLD0_ORT_PTx_6	OR term. Bit position corresponds to product term. Default Value: X
5	PLD0_ORT_PTx_5	OR term. Bit position corresponds to product term. Default Value: X
4	PLD0_ORT_PTx_4	OR term. Bit position corresponds to product term. Default Value: X

(continued)

3	PLD0_ORT_PTx_3	OR term. Bit position corresponds to product term. Default Value: X
2	PLD0_ORT_PTx_2	OR term. Bit position corresponds to product term. Default Value: X
1	PLD0_ORT_PTx_1	OR term. Bit position corresponds to product term. Default Value: X
0	PLD0_ORT_PTx_0	OR term. Bit position corresponds to product term. Default Value: X

36.1.17 UDB_P0_U0_PLD_MC_CFG_CEN_CONST

Macrocell configuration for Carry Enable and Constant

Address: 0x400F3038

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_MC3_DFF_C	PLD0_MC3_CEN	PLD0_MC2_DFF_C	PLD0_MC2_CEN	PLD0_MC1_DFF_C	PLD0_MC1_CEN	PLD0_MC0_DFF_C	PLD0_MC0_CEN

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_MC3_DFF_C	PLD1_MC3_CEN	PLD1_MC2_DFF_C	PLD1_MC2_CEN	PLD1_MC1_DFF_C	PLD1_MC1_CEN	PLD1_MC0_DFF_C	PLD1_MC0_CEN

Bits	Name	Description
15	PLD1_MC3_DFF_C	DFF Constant Default Value: X **0x0: NOINV:** DFF non-inverted **0x1: INVERTED:** DFF inverted
14	PLD1_MC3_CEN	Carry enable Default Value: X **0x0: DISABLE:** Disabled **0x1: ENABLE:** Enabled
13	PLD1_MC2_DFF_C	DFF Constant Default Value: X **0x0: NOINV:** DFF non-inverted **0x1: INVERTED:** DFF inverted
12	PLD1_MC2_CEN	Carry enable Default Value: X **0x0: DISABLE:** Disabled **0x1: ENABLE:** Enabled

(continued)

11	PLD1_MC1_DFF_C	DFF Constant Default Value: X **0x0: NOINV:** DFF non-inverted **0x1: INVERTED:** DFF inverted
10	PLD1_MC1_CEN	Carry enable Default Value: X **0x0: DISABLE:** Disabled **0x1: ENABLE:** Enabled
9	PLD1_MC0_DFF_C	DFF Constant Default Value: X **0x0: NOINV:** DFF non-inverted **0x1: INVERTED:** DFF inverted
8	PLD1_MC0_CEN	Carry enable Default Value: X **0x0: DISABLE:** Disabled **0x1: ENABLE:** Enabled
7	PLD0_MC3_DFF_C	DFF Constant Default Value: X **0x0: NOINV:** DFF non-inverted **0x1: INVERTED:** DFF inverted
6	PLD0_MC3_CEN	Carry enable Default Value: X **0x0: DISABLE:** Disabled **0x1: ENABLE:** Enabled
5	PLD0_MC2_DFF_C	DFF Constant Default Value: X **0x0: NOINV:** DFF non-inverted **0x1: INVERTED:** DFF inverted
4	PLD0_MC2_CEN	Carry enable Default Value: X

(continued)

		0x0: DISABLE: Disabled **0x1: ENABLE:** Enabled
3	PLD0_MC1_DFF_C	DFF Constant Default Value: X **0x0: NOINV:** DFF non-inverted **0x1: INVERTED:** DFF inverted
2	PLD0_MC1_CEN	Carry enable Default Value: X **0x0: DISABLE:** Disabled **0x1: ENABLE:** Enabled
1	PLD0_MC0_DFF_C	DFF Constant Default Value: X **0x0: NOINV:** DFF non-inverted **0x1: INVERTED:** DFF inverted
0	PLD0_MC0_CEN	Carry enable Default Value: X **0x0: DISABLE:** Disabled **0x1: ENABLE:** Enabled

36.1.18 UDB_P0_U0_PLD_MC_CFG_XORFB

PLD Macro cell XOR feedback

Address: 0x400F303A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	PLD0_MC3_XORFB [7:6]		PLD0_MC2_XORFB [5:4]		PLD0_MC1_XORFB [3:2]		PLD0_MC0_XORFB [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	PLD1_MC3_XORFB [15:14]		PLD1_MC2_XORFB [13:12]		PLD1_MC1_XORFB [11:10]		PLD1_MC0_XORFB [9:8]	

Bits	Name	Description
15 : 14	PLD1_MC3_XORFB	XOR feedback Default Value: X **0x0: DFF:** DFF **0x1: CARRY:** Carry **0x2: TFF_H:** TFF on high **0x3: TFF_L:** TFF on low
13 : 12	PLD1_MC2_XORFB	XOR feedback Default Value: X **0x0: DFF:** DFF **0x1: CARRY:** Carry **0x2: TFF_H:** TFF on high **0x3: TFF_L:** TFF on low
11 : 10	PLD1_MC1_XORFB	XOR feedback Default Value: X **0x0: DFF:** DFF **0x1: CARRY:** Carry

(continued)

		0x2: TFF_H: TFF on high
		0x3: TFF_L: TFF on low
9 : 8	PLD1_MC0_XORFB	XOR feedback Default Value: X
		0x0: DFF: DFF
		0x1: CARRY: Carry
		0x2: TFF_H: TFF on high
		0x3: TFF_L: TFF on low
7 : 6	PLD0_MC3_XORFB	XOR feedback Default Value: X
		0x0: DFF: DFF
		0x1: CARRY: Carry
		0x2: TFF_H: TFF on high
		0x3: TFF_L: TFF on low
5 : 4	PLD0_MC2_XORFB	XOR feedback Default Value: X
		0x0: DFF: DFF
		0x1: CARRY: Carry
		0x2: TFF_H: TFF on high
		0x3: TFF_L: TFF on low
3 : 2	PLD0_MC1_XORFB	XOR feedback Default Value: X
		0x0: DFF: DFF
		0x1: CARRY: Carry
		0x2: TFF_H: TFF on high
		0x3: TFF_L: TFF on low

(continued)

1 : 0	PLD0_MC0_XORFB	XOR feedback Default Value: X **0x0: DFF:** DFF **0x1: CARRY:** Carry **0x2: TFF_H:** TFF on high **0x3: TFF_L:** TFF on low

36.1.19 UDB_P0_U0_PLD_MC_SET_RESET

PLD Macro cell Set Reset Selection

Address: 0x400F303C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_MC3_RESET_SEL	PLD0_MC3_SET_SEL	PLD0_MC2_RESET_SEL	PLD0_MC2_SET_SEL	PLD0_MC1_RESET_SEL	PLD0_MC1_SET_SEL	PLD0_MC0_RESET_SEL	PLD0_MC0_SET_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_MC3_RESET_SEL	PLD1_MC3_SET_SEL	PLD1_MC2_RESET_SEL	PLD1_MC2_SET_SEL	PLD1_MC1_RESET_SEL	PLD1_MC1_SET_SEL	PLD1_MC0_RESET_SEL	PLD1_MC0_SET_SEL

Bits	Name	Description
15	PLD1_MC3_RESET_SEL	Reset select enable Default Value: X **0x0: DISABLE:** Reset not used **0x1: ENABLE:** Reset enabled
14	PLD1_MC3_SET_SEL	Set select enable Default Value: X **0x0: DISABLE:** Set not used **0x1: ENABLE:** Set enabled
13	PLD1_MC2_RESET_SEL	Reset select enable Default Value: X **0x0: DISABLE:** Reset not used **0x1: ENABLE:** Reset enabled
12	PLD1_MC2_SET_SEL	Set select enable Default Value: X **0x0: DISABLE:** Set not used **0x1: ENABLE:** Set enabled

(continued)

11	PLD1_MC1_RESET_SEL	Reset select enable Default Value: X **0x0: DISABLE:** Reset not used **0x1: ENABLE:** Reset enabled
10	PLD1_MC1_SET_SEL	Set select enable Default Value: X **0x0: DISABLE:** Set not used **0x1: ENABLE:** Set enabled
9	PLD1_MC0_RESET_SEL	Reset select enable Default Value: X **0x0: DISABLE:** Reset not used **0x1: ENABLE:** Reset enabled
8	PLD1_MC0_SET_SEL	Set select enable Default Value: X **0x0: DISABLE:** Set not used **0x1: ENABLE:** Set enabled
7	PLD0_MC3_RESET_SEL	Reset select enable Default Value: X **0x0: DISABLE:** Reset not used **0x1: ENABLE:** Reset enabled
6	PLD0_MC3_SET_SEL	Set select enable Default Value: X **0x0: DISABLE:** Set not used **0x1: ENABLE:** Set enabled
5	PLD0_MC2_RESET_SEL	Reset select enable Default Value: X **0x0: DISABLE:** Reset not used **0x1: ENABLE:** Reset enabled
4	PLD0_MC2_SET_SEL	Set select enable Default Value: X

(continued)

		0x0: DISABLE: Set not used **0x1: ENABLE:** Set enabled
3	PLD0_MC1_RESET_SEL	Reset select enable Default Value: X **0x0: DISABLE:** Reset not used **0x1: ENABLE:** Reset enabled
2	PLD0_MC1_SET_SEL	Set select enable Default Value: X **0x0: DISABLE:** Set not used **0x1: ENABLE:** Set enabled
1	PLD0_MC0_RESET_SEL	Reset select enable Default Value: X **0x0: DISABLE:** Reset not used **0x1: ENABLE:** Reset enabled
0	PLD0_MC0_SET_SEL	Set select enable Default Value: X **0x0: DISABLE:** Set not used **0x1: ENABLE:** Set enabled

36.1.20 UDB_P0_U0_PLD_MC_CFG_BYPASS

PLD Macro cell Bypass control

Address: 0x400F303E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	NC7	PLD0_MC3_BYPASS	NC5	PLD0_MC2_BYPASS	NC3	PLD0_MC1_BYPASS	NC1	PLD0_MC0_BYPASS

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	NC15	PLD1_MC3_BYPASS	NC13	PLD1_MC2_BYPASS	NC11	PLD1_MC1_BYPASS	NC9	PLD1_MC0_BYPASS

Bits	Name	Description
15	NC15	Spare register bit Default Value: X
14	PLD1_MC3_BYPASS	Bypass selection Default Value: X **0x0: REGISTER:** Registered output **0x1: COMBINATIONAL:** Combinational output
13	NC13	Spare register bit Default Value: X
12	PLD1_MC2_BYPASS	Bypass selection Default Value: X **0x0: REGISTER:** Registered output **0x1: COMBINATIONAL:** Combinational output
11	NC11	Spare register bit Default Value: X
10	PLD1_MC1_BYPASS	Bypass selection Default Value: X **0x0: REGISTER:** Registered output **0x1: COMBINATIONAL:** Combinational output

(continued)

9	NC9	Spare register bit Default Value: X
8	PLD1_MC0_BYPASS	Bypass selection Default Value: X **0x0: REGISTER:** Registered output **0x1: COMBINATIONAL:** Combinational output
7	NC7	Spare register bit Default Value: X
6	PLD0_MC3_BYPASS	Bypass selection Default Value: X **0x0: REGISTER:** Registered output **0x1: COMBINATIONAL:** Combinational output
5	NC5	Spare register bit Default Value: X
4	PLD0_MC2_BYPASS	Bypass selection Default Value: X **0x0: REGISTER:** Registered output **0x1: COMBINATIONAL:** Combinational output
3	NC3	Spare register bit Default Value: X
2	PLD0_MC1_BYPASS	Bypass selection Default Value: X **0x0: REGISTER:** Registered output **0x1: COMBINATIONAL:** Combinational output
1	NC1	Spare register bit Default Value: X
0	PLD0_MC0_BYPASS	Bypass selection Default Value: X **0x0: REGISTER:** Registered output **0x1: COMBINATIONAL:** Combinational output

36.1.21 UDB_P0_U0_CFG0

Datapath Input Selection - RAD1 RAD0. Address bits 0 and 1 to the dynamic configuration RAM

Address: 0x400F3040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	RAD1 [6:4]			None	RAD0 [2:0]		

Bits	Name	Description
6 : 4	RAD1	Datapath Permutable Input Mux Default Value: 0 **0x0: OFF:** Input off **0x1: DP_IN0:** Set to dp_in[0] **0x2: DP_IN1:** Set to dp_in[1] **0x3: DP_IN2:** Set to dp_in[2] **0x4: DP_IN3:** Set to dp_in[3] **0x5: DP_IN4:** Set to dp_in[4] **0x6: DP_IN5:** Set to dp_in[5] **0x7: RESERVED:** Reserved
2 : 0	RAD0	Datapath Permutable Input Mux Default Value: 0 **0x0: OFF:** Input off **0x1: DP_IN0:** Set to dp_in[0] **0x2: DP_IN1:** Set to dp_in[1] **0x3: DP_IN2:** Set to dp_in[2] **0x4: DP_IN3:** Set to dp_in[3] **0x5: DP_IN4:** Set to dp_in[4]

(continued)

0x6: DP_IN5:
Set to dp_in[5]

0x7: RESERVED:
Reserved

36.1.22 UDB_P0_U0_CFG1

Datapath Input Selection - RAD2. Address bit 2 to the dynamic configuration RAM

Address: 0x400F3041

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW		
HW Access	R	R	R	R	R	R		
Name	DP_RTE_BYPASS4	DP_RTE_BYPASS3	DP_RTE_BYPASS2	DP_RTE_BYPASS1	DP_RTE_BYPASS0	RAD2 [2:0]		

Bits	Name	Description
7	DP_RTE_BYPASS4	DP_In bypass control Default Value: 0 **0x0: DP_IN4_ROUTE:** Use dp_in[4] **0x1: DP_IN4_BYPASS:** Use dp_out[4] as input via bypass
6	DP_RTE_BYPASS3	DP_In bypass control Default Value: 0 **0x0: DP_IN3_ROUTE:** Use dp_in[3] **0x1: DP_IN3_BYPASS:** Use dp_out[3] as input via bypass
5	DP_RTE_BYPASS2	DP_In bypass control Default Value: 0 **0x0: DP_IN2_ROUTE:** Use dp_in[2] **0x1: DP_IN2_BYPASS:** Use dp_out[2] as input via bypass
4	DP_RTE_BYPASS1	DP_In bypass control Default Value: 0 **0x0: DP_IN1_ROUTE:** Use dp_in[1] **0x1: DP_IN1_BYPASS:** Use dp_out[1] as input via bypass
3	DP_RTE_BYPASS0	DP_In bypass control Default Value: 0 **0x0: DP_IN0_ROUTE:** Use dp_in[0] **0x1: DP_IN0_BYPASS:** Use dp_out[0] as input via bypass

(continued)

2 : 0	RAD2	Datapath Permutable Input Mux Default Value: 0 **0x0: OFF:** Input off **0x1: DP_IN0:** Set to dp_in[0] **0x2: DP_IN1:** Set to dp_in[1] **0x3: DP_IN2:** Set to dp_in[2] **0x4: DP_IN3:** Set to dp_in[3] **0x5: DP_IN4:** Set to dp_in[4] **0x6: DP_IN5:** Set to dp_in[5] **0x7: RESERVED:** Reserved

36.1.23 UDB_P0_U0_CFG2

Datapath Input Selection - F1_LD, F0_LD.

Address: 0x400F3042

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW			RW	RW		
HW Access	R	R			R	R		
Name	NC7	F1_LD [6:4]			DP_RTE_BYPASS5	F0_LD [2:0]		

Bits	Name	Description
7	NC7	Spare register bit Default Value: 0
6 : 4	F1_LD	Datapath Permutable Input Mux Default Value: 0 **0x0: OFF:** Input off **0x1: DP_IN0:** Set to dp_in[0] **0x2: DP_IN1:** Set to dp_in[1] **0x3: DP_IN2:** Set to dp_in[2] **0x4: DP_IN3:** Set to dp_in[3] **0x5: DP_IN4:** Set to dp_in[4] **0x6: DP_IN5:** Set to dp_in[5] **0x7: RESERVED:** Reserved
3	DP_RTE_BYPASS5	DP_In bypass control Default Value: 0 **0x0: DP_IN5_ROUTE:** Use dp_in[5] **0x1: DP_IN5_BYPASS:** Use dp_out[5] via bypass
2 : 0	F0_LD	Datapath Permutable Input Mux Default Value: 0 **0x0: OFF:** Input off

(continued)

0x1: DP_IN0:
Set to dp_in[0]

0x2: DP_IN1:
Set to dp_in[1]

0x3: DP_IN2:
Set to dp_in[2]

0x4: DP_IN3:
Set to dp_in[3]

0x5: DP_IN4:
Set to dp_in[4]

0x6: DP_IN5:
Set to dp_in[5]

0x7: RESERVED:
Reserved

36.1.24 UDB_P0_U0_CFG3

Datapath Input Selection - D1_LD, D0_LD.

Address: 0x400F3043

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	D1_LD [6:4]			None	D0_LD [2:0]		

Bits	Name	Description
6 : 4	D1_LD	Datapath Permutable Input Mux Default Value: 0 **0x0: OFF:** Input off **0x1: DP_IN0:** Set to dp_in[0] **0x2: DP_IN1:** Set to dp_in[1] **0x3: DP_IN2:** Set to dp_in[2] **0x4: DP_IN3:** Set to dp_in[3] **0x5: DP_IN4:** Set to dp_in[4] **0x6: DP_IN5:** Set to dp_in[5] **0x7: RESERVED:** Reserved
2 : 0	D0_LD	Datapath Permutable Input Mux Default Value: 0 **0x0: OFF:** Input off **0x1: DP_IN0:** Set to dp_in[0] **0x2: DP_IN1:** Set to dp_in[1] **0x3: DP_IN2:** Set to dp_in[2] **0x4: DP_IN3:** Set to dp_in[3] **0x5: DP_IN4:** Set to dp_in[4]

(continued)

0x6: DP_IN5:
Set to dp_in[5]

0x7: RESERVED:
Reserved

36.1.25 UDB_P0_U0_CFG4

Datapath Input Selection - CI_MUX SI_MUX.

Address: 0x400F3044

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	CI_MUX [6:4]			None	SI_MUX [2:0]		

Bits	Name	Description
6 : 4	CI_MUX	Datapath Permutable Input Mux Default Value: 0 **0x0: OFF:** Input off **0x1: DP_IN0:** Set to dp_in[0] **0x2: DP_IN1:** Set to dp_in[1] **0x3: DP_IN2:** Set to dp_in[2] **0x4: DP_IN3:** Set to dp_in[3] **0x5: DP_IN4:** Set to dp_in[4] **0x6: DP_IN5:** Set to dp_in[5] **0x7: RESERVED:** Reserved
2 : 0	SI_MUX	Datapath Permutable Input Mux Default Value: 0 **0x0: OFF:** Input off **0x1: DP_IN0:** Set to dp_in[0] **0x2: DP_IN1:** Set to dp_in[1] **0x3: DP_IN2:** Set to dp_in[2] **0x4: DP_IN3:** Set to dp_in[3] **0x5: DP_IN4:** Set to dp_in[4]

(continued)

0x6: DP_IN5:
Set to dp_in[5]

0x7: RESERVED:
Reserved

36.1.26 UDB_P0_U0_CFG5

Datapath Output Selection for OUT1 OUT0

Address: 0x400F3045

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	OUT1 [7:4]				OUT0 [3:0]			

Bits	Name	Description
7 : 4	OUT1	Datapath Permutable Output Mux Default Value: 0 **0x0: CE0:** Comparator 0 equal **0x1: CL0:** Comparator 0 less than **0x2: Z0:** Accumulator 0 zero detect **0x3: FF0:** Accumulator 0 ones detect **0x4: CE1:** Comparator 1 equal **0x5: CL1:** Comparator 1 less than **0x6: Z1:** Accumulator 1 zero detect **0x7: FF1:** Accumulator 1 ones detect **0x8: OV_MSB:** Overflow of MSB **0x9: CO_MSB:** Carry out of MSB **0xa: CMSBO:** CRC MSB **0xb: SO:** Shift out **0xc: F0_BLK_STAT:** FIFO 0 block status defined by direction **0xd: F1_BLK_STAT:** FIFO 1 block status defined by direction **0xe: F0_BUS_STAT:** FIFO 0 bus status defined by direction and level

(continued)

		0xf: F1_BUS_STAT: FIFO 1 bus status defined by direction and level
3 : 0	OUT0	Datapath Permutable Output Mux Default Value: 0 **0x0: CE0:** Comparator 0 equal **0x1: CL0:** Comparator 0 less than **0x2: Z0:** Accumulator 0 zero detect **0x3: FF0:** Accumulator 0 ones detect **0x4: CE1:** Comparator 1 equal **0x5: CL1:** Comparator 1 less than **0x6: Z1:** Accumulator 1 zero detect **0x7: FF1:** Accumulator 1 ones detect **0x8: OV_MSB:** Overflow of MSB **0x9: CO_MSB:** Carry out of MSB **0xa: CMSBO:** CRC MSB **0xb: SO:** Shift out **0xc: F0_BLK_STAT:** FIFO 0 block status defined by direction **0xd: F1_BLK_STAT:** FIFO 1 block status defined by direction **0xe: F0_BUS_STAT:** FIFO 0 bus status defined by direction and level **0xf: F1_BUS_STAT:** FIFO 1 bus status defined by direction and level

36.1.27 UDB_P0_U0_CFG6

Datapath Output Selection for OUT3 OUT2

Address: 0x400F3046

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	OUT3 [7:4]				OUT2 [3:0]			

Bits	Name	Description
7 : 4	OUT3	Datapath Permutable Output Mux Default Value: 0 **0x0: CE0:** Comparator 0 equal **0x1: CL0:** Comparator 0 less than **0x2: Z0:** Accumulator 0 zero detect **0x3: FF0:** Accumulator 0 ones detect **0x4: CE1:** Comparator 1 equal **0x5: CL1:** Comparator 1 less than **0x6: Z1:** Accumulator 1 zero detect **0x7: FF1:** Accumulator 1 ones detect **0x8: OV_MSB:** Overflow of MSB **0x9: CO_MSB:** Carry out of MSB **0xa: CMSBO:** CRC MSB **0xb: SO:** Shift out **0xc: F0_BLK_STAT:** FIFO 0 block status defined by direction **0xd: F1_BLK_STAT:** FIFO 1 block status defined by direction **0xe: F0_BUS_STAT:** FIFO 0 bus status defined by direction and level

(continued)

		0xf: F1_BUS_STAT: FIFO 1 bus status defined by direction and level
3 : 0	OUT2	Datapath Permutable Output Mux Default Value: 0 **0x0: CE0:** Comparator 0 equal **0x1: CL0:** Comparator 0 less than **0x2: Z0:** Accumulator 0 zero detect **0x3: FF0:** Accumulator 0 ones detect **0x4: CE1:** Comparator 1 equal **0x5: CL1:** Comparator 1 less than **0x6: Z1:** Accumulator 1 zero detect **0x7: FF1:** Accumulator 1 ones detect **0x8: OV_MSB:** Overflow of MSB **0x9: CO_MSB:** Carry out of MSB **0xa: CMSBO:** CRC MSB **0xb: SO:** Shift out **0xc: F0_BLK_STAT:** FIFO 0 block status defined by direction **0xd: F1_BLK_STAT:** FIFO 1 block status defined by direction **0xe: F0_BUS_STAT:** FIFO 0 bus status defined by direction and level **0xf: F1_BUS_STAT:** FIFO 1 bus status defined by direction and level

36.1.28 UDB_P0_U0_CFG7

Datapath Output Selection for OUT5 OUT4

Address: 0x400F3047

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	OUT5 [7:4]				OUT4 [3:0]			

Bits	Name	Description
7 : 4	OUT5	Datapath Permutable Output Mux Default Value: 0 **0x0: CE0:** Comparator 0 equal **0x1: CL0:** Comparator 0 less than **0x2: Z0:** Accumulator 0 zero detect **0x3: FF0:** Accumulator 0 ones detect **0x4: CE1:** Comparator 1 equal **0x5: CL1:** Comparator 1 less than **0x6: Z1:** Accumulator 1 zero detect **0x7: FF1:** Accumulator 1 ones detect **0x8: OV_MSB:** Overflow of MSB **0x9: CO_MSB:** Carry out of MSB **0xa: CMSBO:** CRC MSB **0xb: SO:** Shift out **0xc: F0_BLK_STAT:** FIFO 0 block status defined by direction **0xd: F1_BLK_STAT:** FIFO 1 block status defined by direction **0xe: F0_BUS_STAT:** FIFO 0 bus status defined by direction and level

(continued)

		0xf: F1_BUS_STAT: FIFO 1 bus status defined by direction and level
3 : 0	OUT4	Datapath Permutable Output Mux Default Value: 0 **0x0: CE0:** Comparator 0 equal **0x1: CL0:** Comparator 0 less than **0x2: Z0:** Accumulator 0 zero detect **0x3: FF0:** Accumulator 0 ones detect **0x4: CE1:** Comparator 1 equal **0x5: CL1:** Comparator 1 less than **0x6: Z1:** Accumulator 1 zero detect **0x7: FF1:** Accumulator 1 ones detect **0x8: OV_MSB:** Overflow of MSB **0x9: CO_MSB:** Carry out of MSB **0xa: CMSBO:** CRC MSB **0xb: SO:** Shift out **0xc: F0_BLK_STAT:** FIFO 0 block status defined by direction **0xd: F1_BLK_STAT:** FIFO 1 block status defined by direction **0xe: F0_BUS_STAT:** FIFO 0 bus status defined by direction and level **0xf: F1_BUS_STAT:** FIFO 1 bus status defined by direction and level

36.1.29 UDB_P0_U0_CFG8

Datapath Output Synchronization Option

Address: 0x400F3048

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW					
HW Access	R	R	R					
Name	NC7	NC6	OUT_SYNC [5:0]					

Bits	Name	Description
7	NC7	Spare register bit Default Value: 0
6	NC6	Spare register bit Default Value: 0
5 : 0	OUT_SYNC	Datapath Output Synchronization. Each datapath output can be registered (default,0), or combinational (1) Default Value: 0 **0x0: REGISTERED:** registered **0x1: COMBINATIONAL:** combinational

36.1.30 UDB_P0_U0_CFG9

Datapath ALU Mask

Address: 0x400F3049

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	AMASK [7:0]							

Bits	Name	Description
7 : 0	AMASK	Datapath ALU Mask. The mask value in this register is applied to the output of the Datapath ALU result before the result is stored. The AMASK_EN bit (CFG12) must be set for the mask to be operational. Default Value: 0

36.1.31 UDB_P0_U0_CFG10

Datapath Compare 0 Mask

Address: 0x400F304A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CMASK0 [7:0]							

Bits	Name	Description
7 : 0	CMASK0	Datapath Compare 0 Mask. The mask value in this register is applied to the output of the Accumulator 0 before it is used for comparison in Compare block 0. The CMASK0_EN bit (CFG12) must be set for the mask to be operational. Default Value: 0

36.1.32 UDB_P0_U0_CFG11

Datapath Compare 1 Mask

Address: 0x400F304B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CMASK0 [7:0]							

Bits	Name	Description
7 : 0	CMASK0	Datapath Compare 1 Mask. The mask value in this register is applied to the selected Compare 1 block input (Accumulator 0 or Accumulator 1) before it is used for comparison. The CMASK1_EN bit (CFG12) must be set for the mask to be operational. Default Value: 0

36.1.33 UDB_P0_U0_CFG12

Datapath mask enables and shift in configuration

Address: 0x400F304C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW		RW	
HW Access	R	R	R	R	R		R	
Name	CMASK1_EN	CMASK0_EN	AMASK_EN	DEF_SI	SI_SELB [3:2]		SI_SELA [1:0]	

Bits	Name	Description
7	CMASK1_EN	Datapath mask enable Default Value: 0 **0x0: DISABLE:** Masking disabled **0x1: ENABLE:** Masking enabled
6	CMASK0_EN	Datapath mask enable Default Value: 0 **0x0: DISABLE:** Masking disabled **0x1: ENABLE:** Masking enabled
5	AMASK_EN	Datapath mask enable Default Value: 0 **0x0: DISABLE:** Masking disabled **0x1: ENABLE:** Masking enabled
4	DEF_SI	Datapath default shift value Default Value: 0 **0x0: DEFAULT_0:** Default shift is 0 **0x1: DEFAULT_1:** Default shift is 1
3 : 2	SI_SELB	Datapath shift in source select Default Value: 0 **0x0: DEFAULT:** Default value specified in default shift field **0x1: REGISTERED:** Shift in is the shift out registered from previous cycle

(continued)

		0x2: ROUTE: Shift in is selected from datapath routing input **0x3: CHAIN:** Shift in is chained from the previous datapath
1 : 0	SI_SELA	Datapath shift in source select Default Value: 0 **0x0: DEFAULT:** Default value specified in default shift field **0x1: REGISTERED:** Shift in is the shift out registered from previous cycle **0x2: ROUTE:** Shift in is selected from datapath routing input **0x3: CHAIN:** Shift in is chained from the previous datapath

36.1.34 UDB_P0_U0_CFG13

Datapath carry in and compare configuration

Address: 0x400F304D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	CMP_SELB [7:6]		CMP_SELA [5:4]		CI_SELB [3:2]		CI_SELA [1:0]	

Bits	Name	Description
7 : 6	CMP_SELB	Datapath compare select Default Value: 0 **0x0: A1_D1:** Compare A1 to D1 **0x1: A1_A0:** Compare A1 to A0 **0x2: A0_D1:** Compare A0 to D1 **0x3: A0_A0:** Compare A0 to A0
5 : 4	CMP_SELA	Datapath compare select Default Value: 0 **0x0: A1_D1:** Compare A1 to D1 **0x1: A1_A0:** Compare A1 to A0 **0x2: A0_D1:** Compare A0 to D1 **0x3: A0_A0:** Compare A0 to A0
3 : 2	CI_SELB	Datapath carry in source select Default Value: 0 **0x0: DEFAULT:** Default arithmetic mode **0x1: REGISTERED:** Carry in is the carry out registered from previous cycle **0x2: ROUTE:** Carry in is selected from datapath routing input **0x3: CHAIN:** Carry in is chained from the previous datapath
1 : 0	CI_SELA	Datapath carry in source select Default Value: 0

(continued)

0x0: DEFAULT:
Default arithmetic mode

0x1: REGISTERED:
Carry in is the carry out registered from previous cycle

0x2: ROUTE:
Carry in is selected from datapath routing input

0x3: CHAIN:
Carry in is chained from the previous datapath

36.1.35 UDB_P0_U0_CFG14

Datapath chaining and MSB configuration

Address: 0x400F304E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW			RW	RW	RW	RW
HW Access	R	R			R	R	R	R
Name	MSB_EN	MSB_SEL [6:4]			CHAIN_CMSB	CHAIN_FB	CHAIN1	CHAIN0

Bits	Name	Description
7	MSB_EN	Datapath MSB selection enable Default Value: 0 **0x0: DISABLE:** MSB selection is disabled, MSB is bit 7 **0x1: ENABLE:** MSB selection is controlled by MSB_SEL
6 : 4	MSB_SEL	Datapath MSB Selection Default Value: 0 **0x0: BIT0:** MSB is bit 0 **0x1: BIT1:** MSB is bit 1 **0x2: BIT2:** MSB is bit 2 **0x3: BIT3:** MSB is bit 3 **0x4: BIT4:** MSB is bit 4 **0x5: BIT5:** MSB is bit 5 **0x6: BIT6:** MSB is bit 6 **0x7: BIT7:** MSB is bit 7 - equivalent to MSB_EN=0
3	CHAIN_CMSB	Datapath CRC MSB chaining enable Default Value: 0 **0x0: DISABLE:** CRC MSB is not chained **0x1: ENABLE:** CRC MSB is chained from the next (MSB) datapath

(continued)

2	CHAIN_FB	Datapath CRC feedback chaining enable Default Value: 0 **0x0: DISABLE:** CRC feedback is not chained **0x1: ENABLE:** CRC feedback is chained from the previous (LSB) datapath
1	CHAIN1	Datapath condition chaining enable Default Value: 0 **0x0: DISABLE:** Conditions are not chained **0x1: ENABLE:** Conditions are chained from the previous (LSB) datapath
0	CHAIN0	Datapath condition chaining enable Default Value: 0 **0x0: DISABLE:** Conditions are not chained **0x1: ENABLE:** Conditions are chained from the previous (LSB) datapath

36.1.36 UDB_P0_U0_CFG15

Datapath FIFO, shift and parallel input control

Address: 0x400F304F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW		RW	
HW Access	R	R	R	R	R		R	
Name	PI_SEL	SHIFT_SEL	PI_DYN	MSB_SI	F1_INSEL [3:2]		F0_INSEL [1:0]	

Bits	Name	Description
7	PI_SEL	Datapath parallel input selection Default Value: 0 **0x0: NORMAL:** Normal operation, ALU source is from accumulator selection **0x1: PARALLEL:** ALU source A input is from the parallel data input
6	SHIFT_SEL	Datapath shift out selection Default Value: 0 **0x0: SOL_MSB:** Routed shift out is shift out left (sol_msb) **0x1: SOR:** Routed shift out is shift out right (sor)
5	PI_DYN	Enable for dynamic control of parallel data input (PI) mux. Default Value: 0 **0x0: DISABLE:** Parallel input mux select is only controlled by static configuration (PI_SEL). **0x1: ENABLE:** Parallel input mux to the Datapath is controlled by CFB_EN field in Datapath Dynamic RAM. When this mode is enabled, the CFB_EN usage for CRC/PRS functionality is disabled.
4	MSB_SI	Arithmetic shift right operation shift in selection Default Value: 0 **0x0: DEFAULT:** Shift in default value (when SI_SELA and/or SI_SELB == 0) **0x1: MSB:** Override default and shift in MSB value
3 : 2	F1_INSEL	Datapath FIFO Configuration Default Value: 0 **0x0: INPUT:** Input Mode: Write source is the system bus; read destination is corresponding data register or accumulator **0x1: OUTPUT_A0:** Output Mode: Write source is A0, read destination is the system bus

(continued)

		0x2: OUTPUT_A1: Output Mode: Write source is A1, read destination is the system bus **0x3: OUTPUT_ALU:** Output Mode: Write source is the ALU output, read destination is the system bus
1 : 0	F0_INSEL	Datapath FIFO Configuration Default Value: 0 **0x0: INPUT:** Input Mode: Write source is the system bus; read destination is corresponding data register or accumulator **0x1: OUTPUT_A0:** Output Mode: Write source is A0, read destination is the system bus **0x2: OUTPUT_A1:** Output Mode: Write source is A1, read destination is the system bus **0x3: OUTPUT_ALU:** Output Mode: Write source is the ALU output, read destination is the system bus

36.1.37 UDB_P0_U0_CFG16

Datapath FIFO and register access configuration control

Address: 0x400F3050

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	F1_CK_INV	F0_CK_INV	FIFO_FAST	FIFO_CAP	FIFO_EDGE	FIFO_ASYNC	EXT_CRCPRS	WRK16_CONCAT

Bits	Name	Description
7	F1_CK_INV	FIFO Clock Invert. When this bit is set, the polarity of the clock for the given FIFO will be inverted, with respect to the polarity of the selected Datapath clock. Default Value: 0 **0x0: NORMAL:** FIFO clock is the same polarity as the Datapath clock. **0x1: INVERT:** FIFO clock is inverted with respect to the Datapath clock.
6	F0_CK_INV	FIFO Clock Invert. When this bit is set, the polarity of the clock for the given FIFO will be inverted, with respect to the polarity of the selected Datapath clock. Default Value: 0 **0x0: NORMAL:** FIFO clock is the same polarity as the Datapath clock. **0x1: INVERT:** FIFO clock is inverted with respect to the Datapath clock.
5	FIFO_FAST	FIFO Fast Mode. When this bit is set, the FIFO write logic is clocked by the application bus clock. Lowers the latency of capture timing, at the expense of additional power. Default Value: 0 **0x0: DISABLE:** FIFO is clocked with selected Datapath clock. **0x1: ENABLE:** FIFO is clocked with application bus clock. Master and quadrant bus clock gating must be enabled.
4	FIFO_CAP	FIFO Software Capture Mode. When this bit is set, a read of A0 or A1 triggers a capture into F0 or F1 respectively. This function follows the chaining configuration. All accumulators in the chain from a given block to the MS block in the chain are capture Default Value: 0 **0x0: DISABLE:** FIFO capture is disabled. **0x1: ENABLE:** FIFO capture is enabled (FIFO must be in output mode). A read of A0 or A1 will write into F0 or F1.
3	FIFO_EDGE	Edge/level sensitive FIFO write control (Fx_LD). Only applies to FIFO configured in output mode Default Value: 0

(continued)

		0x0: LEVEL: FIFO write from accumulators/ALU is level sensitive. FIFO write occurs on a clock edge whenever the write control is sampled high on that edge. **0x1: EDGE:** FIFO write from accumulators/ALU is edge sensitive. FIFO write occurs on a clock edge folloing a 0 to 1 transition on the write control. The write control must be negated for at least one full cycle of the FIFO clock for a subsequent transition to be dete
2	FIFO_ASYNC	Asynchronous FIFO clocking support Default Value: 0 **0x0: DISABLE:** FIFO clocks are synchronous **0x1: ENABLE:** FIFO clocks are asynchronous
1	EXT_CRCPRS	External CRC/PRS mode Default Value: 0 **0x0: INTERNAL:** Internal CRC/PRS routing **0x1: EXTERNAL:** External CRC/PRS routing
0	WRK16_CONCAT	Datapath register access mode Default Value: 0 **0x0: DEFAULT:** 16-bit default access mode: selects registers in two consecutive UDBs in chaining order **0x1: CONCATENATE:** 16-bit concat access mode: selects concatenated registers in a single UDB

36.1.38 UDB_P0_U0_CFG17

Datapath FIFO control

Address: 0x400F3051

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [7:5]			FIFO_ADD_SYNC	NC3	NC2	F1_DYN	F0_DYN

Bits	Name	Description
4	FIFO_ADD_SYNC	Adds an additional sync flip-flop to FIFO block status. Default Value: 0 **0x0: DISABLE:** Compatible Mode: FIFO block status sync configuration is 'none' (FIFO_ASYNC = 0) and 1 sync flip-flop (FIFO_ASYNC = 1) **0x1: ENABLE:** Add Sync Mode: FIFO block status sync configuration 1 sync flip-flop (FIFO_ASYNC = 0) and 2 sync flip-flops (FIFO_ASYNC = 1)
3	NC3	Spare register bit Default Value: 0
2	NC2	Spare register bit Default Value: 0
1	F1_DYN	Default Value: 0 **0x0: STATIC:** Default. FIFO direction is static and controlled by the associated Fx_INSEL bits (CFG15). **0x1: DYNAMIC:** The associated FIFO direction is dynamically controlled by the associated 'dx_load' Datapath input signal. When the 'dx_load' signal is '0', the access is internal, where the FIFO is both a source for the Datapath, and a destination for the Datapath (dest
0	F0_DYN	When this bit is set, the associated FIFO configuration may be dynamically controlled. Default Value: 0 **0x0: STATIC:** Default. FIFO direction is static and controlled by the associated Fx_INSEL bits (CFG15). **0x1: DYNAMIC:** The associated FIFO direction is dynamically controlled by the associated 'dx_load' Datapath input signal. When the 'dx_load' signal is '0', the access is internal, where the FIFO is both a source for the Datapath, and a destination for the Datapath (dest

36.1.39 UDB_P0_U0_CFG18

Control Register Mode 0 (used in conjunction with Control Register Mode 1)

Address: 0x400F3052

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CTL_MD0 [7:0]							

Bits	Name	Description
7 : 0	CTL_MD0	CTL_MD1 and CTL_MD0 are concatenated to form an encoding for the mode of each control bit in the control register. Default Value: 0 **0x0: DIRECT:** The value written to that bit drives directly into the routing. **0x1: SYNC:** The value written is resampled by the selected SC clock. The resampled value is driven into the routing. **0x2: DOUBLE_SYNC:** The value written is doubly synced by the selected SC clock. The synched value is driven into the routing. **0x3: PULSE:** The value written is resampled and a synchronous pulse is generated and driven into the routing based on the selected SC clock. At the end of the generated pulse, the control register bit is automatically reset.

36.1.40 UDB_P0_U0_CFG19

Control Register Mode 1 (used in conjunction with Control Register Mode 0)

Address: 0x400F3053

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CTL_MD1 [7:0]							

Bits	Name	Description
7 : 0	CTL_MD1	CTL_MD1 and CTL_MD0 are concatenated to form an encoding for the mode of each control bit in the control register. Default Value: 0 **0x0: DIRECT:** The value written to that bit drives directly into the routing. **0x1: SYNC:** The value written is resampled by the selected SC clock. The resampled value is driven into the routing. **0x2: DOUBLE_SYNC:** The value written is doubly synced by the selected SC clock. The synched value is driven into the routing. **0x3: PULSE:** The value written is resampled and a synchronous pulse is generated and driven into the routing based on the selected SC clock. At the end of the generated pulse, the control register bit is automatically reset.

36.1.41 UDB_P0_U0_CFG20

Status Register input mode selection

Address: 0x400F3054

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	STAT_MD [7:0]							

Bits	Name	Description
7 : 0	STAT_MD	Mode selection for each bit of the status register. A '0' is transparent mode, where internal routing is read idrectly by CPU firmware. A '1' is sticky-clear-on-read mode, where once the given bit is set, it will stay set until the CPU reads the bit. Default Value: 0

36.1.42 UDB_P0_U0_CFG21

Spare register bits

Address: 0x400F3055

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						NC1	NC0

Bits	Name	Description
1	NC1	Spare register bit Default Value: 0
0	NC0	Spare register bit Default Value: 0

36.1.43 UDB_P0_U0_CFG22

SC block configuration control

Address: 0x400F3056

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW	RW	RW	
HW Access	None			R	R	R	R	
Name	None [7:5]			SC_EXT_RES	SC_SYNC_MD	SC_INT_MD	SC_OUT_CTL [1:0]	

Bits	Name	Description
4	SC_EXT_RES	Control register external reset operation. This bit supports autonomous usage of the control register, where a routed reset should clear the writable input registers. By default this is off because the CPU writable register can be cleared in firmware. Default Value: 0 **0x0: DISABLED:** When a routed reset is applied to the control register, only embedded state (sampling registers) are cleared **0x1: ENABLED:** When a routed reset is applied to the control register, all state is cleared, including the CPU writable control bits.
3	SC_SYNC_MD	SC Sync Mode - controls when the status register operates as a 4-bit double synchronizer module Default Value: 0 **0x0: NORMAL:** Normal Mode - Status register operation **0x1: SYNC_MODE:** Sync Mode - Routing inputs sc_in[3:0] are the 4 sync inputs, and connections sc_io[3:0] operate as the sync outputs
2	SC_INT_MD	SC Interrupt Mode - controls when the UDB driving an interrupt generated from the masked OR reduction of status bits 6 to 0 Default Value: 0 **0x0: NORMAL:** Normal Mode - Routing connection sc_io[3] is a normal input to the status register **0x1: INT_MODE:** Interrupt Mode - Routing connection sc_io[3] operates as the UDB interrupt output
1 : 0	SC_OUT_CTL	Selects the output source for the Status and Control routing connections Default Value: 0 **0x0: CONTROL:** Control out, 8-bits of control are driven to the routing connections **0x1: PARALLEL:** Datapath parallel output, 8-bits of datapath parallel output data are driven to the routing connections

(continued)

0x2: COUNTER:
Counter out, 7-bits of count and 1 bit (MSB) of terminal count are driven to the routing connections

0x3: RESERVED:
Reserved

36.1.44 UDB_P0_U0_CFG23

Counter Control

Address: 0x400F3057

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	RW	RW	RW		RW	
HW Access	None	R	R	R	R		R	
Name	None	ALT_CNT	ROUTE_EN	ROUTE_LD	CNT_EN_SEL [3:2]		CNT_LD_SEL [1:0]	

Bits	Name	Description
6	ALT_CNT	Configure the alternate operating mode of the counter Default Value: 0 **0x0: DEFAULT_MODE:** Default counter operating mode **0x1: ALT_MODE:** Alternate counter operating mode
5	ROUTE_EN	Configure the counter enable signal for routing input Default Value: 0 **0x0: DISABLE:** Routed EN signal is not used. EN signal is only controlled by firmware CNT START (ACTL register) **0x1: ROUTED:** Routed EN signal is used, CNT START must be set
4	ROUTE_LD	Configure the counter load signal for routing input Default Value: 0 **0x0: DISABLE:** Routed LD signal is not used **0x1: ROUTED:** Routed LD signal is used
3 : 2	CNT_EN_SEL	Selects the routing inputs for the counter enable signal Default Value: 0 **0x0: SC_IN4:** sc_io_in[0] **0x1: SC_IN5:** sc_io_in[1] **0x2: SC_IN6:** sc_io_in[2] **0x3: SC_IO:** sc_io_in[3]
1 : 0	CNT_LD_SEL	Selects the routing inputs for the counter load signal Default Value: 0

(continued)

0x0: SC_IN0:
sc_in[0]

0x1: SC_IN1:
sc_in[1]

0x2: SC_IN2:
sc_in[2]

0x3: SC_IN3:
sc_in[3]

36.1.45 UDB_P0_U0_CFG24

PLD0 Clock and Reset control

Address: 0x400F3058

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW		RW	
HW Access	R	R	R	R	R		R	
Name	RC_RES_SEL1	RC_RES_SEL0_OR_FRES	RC_INV	RC_EN_INV	RC_EN_MODE [3:2]		RC_EN_SEL [1:0]	

Bits	Name	Description
7	RC_RES_SEL1	Configures the routed reset for the associated UDB component block. The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES = '0' - This bit is not used. When ALT RES = '1' - The bits {RC_SEL1,RC_SEL0_OR_FRES} select the RC routing for routed reset control according to the following: 00 : rc_in [0] 01 : rc_in [1] 10 : rc_in [2] 11 : rc_in [3] Default Value: 0
6	RC_RES_SEL0_OR_FRES	Configures the routed or firmware reset for the associated UDB component block. The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES = '0' - This bit is a firmware reset. When ALT RES = '1' - The bits {RC_SEL1,RC_SEL0_OR_FRES} select the RC routing for routed reset control according to the following: 00 : rc_in [0] 01 : rc_in [1] 10 : rc_in [2] 11 : rc_in [3] Default Value: 0
5	RC_INV	Optionally inverts the clock selection for the associated UDB component block. Default Value: 0 **0x0: NOINV:** Non-inverted **0x1: INVERT:** Inverted
4	RC_EN_INV	Optionally inverts the clock enable selection for the associated UDB component blocks. Default Value: 0 **0x0: NOINV:** Non-inverted **0x1: INVERT:** Inverted
3 : 2	RC_EN_MODE	Selects the operating mode for the clock to the associated UDB component block. Default Value: 0

(continued)

		0x0: OFF: Always off **0x1: ON:** Always on **0x2: POSEDGE:** Positive edge **0x3: LEVEL:** Level sensitive
1 : 0	RC_EN_SEL	Selects channel route for enable control to the associated UDB component block Default Value: 0 **0x0: RC_IN0:** rc_in[0] **0x1: RC_IN1:** rc_in[1] **0x2: RC_IN2:** rc_in[2] **0x3: RC_IN3:** rc_in[3]

36.1.46 UDB_P0_U0_CFG25

PLD1 Clock and Reset control

Address: 0x400F3059

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW		RW	
HW Access	R	R	R	R	R		R	
Name	RC_RES_SEL1	RC_RES_SEL0_OR_FRES	RC_INV	RC_EN_INV	RC_EN_MODE [3:2]		RC_EN_SEL [1:0]	

Bits	Name	Description
7	RC_RES_SEL1	Configures the routed reset for the associated UDB component block. The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES = '0' - This bit is not used. When ALT RES = '1' - The bits {RC_SEL1,RC_SEL0_OR_FRES} select the RC routing for routed reset control according to the following: 00 : rc_in [0] 01 : rc_in [1] 10 : rc_in [2] 11 : rc_in [3] Default Value: 0
6	RC_RES_SEL0_OR_FRES	Configures the routed or firmware reset for the associated UDB component block. The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES = '0' - This bit is a firmware reset. When ALT RES = '1' - The bits {RC_SEL1,RC_SEL0_OR_FRES} select the RC routing for routed reset control according to the following: 00 : rc_in [0] 01 : rc_in [1] 10 : rc_in [2] 11 : rc_in [3] Default Value: 0
5	RC_INV	Optionally inverts the clock selection for the associated UDB component block. Default Value: 0 **0x0: NOINV:** Non-inverted **0x1: INVERT:** Inverted
4	RC_EN_INV	Optionally inverts the clock enable selection for the associated UDB component blocks. Default Value: 0 **0x0: NOINV:** Non-inverted **0x1: INVERT:** Inverted
3 : 2	RC_EN_MODE	Selects the operating mode for the clock to the associated UDB component block. Default Value: 0

(continued)

		0x0: OFF: Always off **0x1: ON:** Always on **0x2: POSEDGE:** Positive edge **0x3: LEVEL:** Level sensitive
1 : 0	RC_EN_SEL	Selects channel route for enable control to the associated UDB component block Default Value: 0 **0x0: RC_IN0:** rc_in[0] **0x1: RC_IN1:** rc_in[1] **0x2: RC_IN2:** rc_in[2] **0x3: RC_IN3:** rc_in[3]

36.1.47 UDB_P0_U0_CFG26

Datapath Clock and Reset control

Address: 0x400F305A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW		RW	
HW Access	R	R	R	R	R		R	
Name	RC_RES_SEL1	RC_RES_SEL0_OR_FRES	RC_INV	RC_EN_INV	RC_EN_MODE [3:2]		RC_EN_SEL [1:0]	

Bits	Name	Description
7	RC_RES_SEL1	Configures the routed reset for the associated UDB component block. The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES = '0' - This bit is not used. When ALT RES = '1' - The bits {RC_SEL1,RC_SEL0_OR_FRES} select the RC routing for routed reset control according to the following: 00 : rc_in [0] 01 : rc_in [1] 10 : rc_in [2] 11 : rc_in [3] Default Value: 0
6	RC_RES_SEL0_OR_FRES	Configures the routed or firmware reset for the associated UDB component block. The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES = '0' - This bit is a firmware reset. When ALT RES = '1' - The bits {RC_SEL1,RC_SEL0_OR_FRES} select the RC routing for routed reset control according to the following: 00 : rc_in [0] 01 : rc_in [1] 10 : rc_in [2] 11 : rc_in [3] Default Value: 0
5	RC_INV	Optionally inverts the clock selection for the associated UDB component block. Default Value: 0 **0x0: NOINV:** Non-inverted **0x1: INVERT:** Inverted
4	RC_EN_INV	Optionally inverts the clock enable selection for the associated UDB component blocks. Default Value: 0 **0x0: NOINV:** Non-inverted **0x1: INVERT:** Inverted
3 : 2	RC_EN_MODE	Selects the operating mode for the clock to the associated UDB component block. Default Value: 0

(continued)

		0x0: OFF: Always off **0x1: ON:** Always on **0x2: POSEDGE:** Positive edge **0x3: LEVEL:** Level sensitive
1 : 0	RC_EN_SEL	Selects channel route for enable control to the associated UDB component block Default Value: 0 **0x0: RC_IN0:** rc_in[0] **0x1: RC_IN1:** rc_in[1] **0x2: RC_IN2:** rc_in[2] **0x3: RC_IN3:** rc_in[3]

36.1.48 UDB_P0_U0_CFG27

Status/Control Clock and Reset control

Address: 0x400F305B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW		RW	
HW Access	R	R	R	R	R		R	
Name	RC_RES_SEL1	RC_RES_SEL0_OR_FRES	RC_INV	RC_EN_INV	RC_EN_MODE [3:2]		RC_EN_SEL [1:0]	

Bits	Name	Description
7	RC_RES_SEL1	Configures the routed reset for the associated UDB component block. The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES = '0' - This bit is not used. When ALT RES = '1' - The bits {RC_SEL1,RC_SEL0_OR_FRES} select the RC routing for routed reset control according to the following: 00 : rc_in [0] 01 : rc_in [1] 10 : rc_in [2] 11 : rc_in [3] Default Value: 0
6	RC_RES_SEL0_OR_FRES	Configures the routed or firmware reset for the associated UDB component block. The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES = '0' - This bit is a firmware reset. When ALT RES = '1' - The bits {RC_SEL1,RC_SEL0_OR_FRES} select the RC routing for routed reset control according to the following: 00 : rc_in [0] 01 : rc_in [1] 10 : rc_in [2] 11 : rc_in [3] Default Value: 0
5	RC_INV	Optionally inverts the clock selection for the associated UDB component block. Default Value: 0 **0x0: NOINV:** Non-inverted **0x1: INVERT:** Inverted
4	RC_EN_INV	Optionally inverts the clock enable selection for the associated UDB component blocks. Default Value: 0 **0x0: NOINV:** Non-inverted **0x1: INVERT:** Inverted
3 : 2	RC_EN_MODE	Selects the operating mode for the clock to the associated UDB component block. Default Value: 0

(continued)

		0x0: OFF: Always off **0x1: ON:** Always on **0x2: POSEDGE:** Positive edge **0x3: LEVEL:** Level sensitive
1 : 0	RC_EN_SEL	Selects channel route for enable control to the associated UDB component block Default Value: 0 **0x0: RC_IN0:** rc_in[0] **0x1: RC_IN1:** rc_in[1] **0x2: RC_IN2:** rc_in[2] **0x3: RC_IN3:** rc_in[3]

36.1.49 UDB_P0_U0_CFG28

Clock Selection for PLD1 and PLD0

Address: 0x400F305C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PLD1_CK_SEL [7:4]				PLD0_CK_SEL [3:0]			

Bits	Name	Description
7 : 4	PLD1_CK_SEL	Clock selection registers Default Value: 0 **0x0: GCLK0:** gclk[0] **0x1: GCLK1:** gclk[1] **0x2: GCLK2:** gclk[2] **0x3: GCLK3:** gclk[3] **0x4: GCLK4:** gclk[4] **0x5: GCLK5:** gclk[5] **0x6: GCLK6:** gclk[6] **0x7: GCLK7:** gclk[7] **0x8: EXT_CLK:** ext_clk **0x9: SYSCLK:** sysclk
3 : 0	PLD0_CK_SEL	Clock selection registers Default Value: 0 **0x0: GCLK0:** gclk[0] **0x1: GCLK1:** gclk[1] **0x2: GCLK2:** gclk[2] **0x3: GCLK3:** gclk[3]

(continued)

0x4: GCLK4:
gclk[4]

0x5: GCLK5:
gclk[5]

0x6: GCLK6:
gclk[6]

0x7: GCLK7:
gclk[7]

0x8: EXT_CLK:
ext_clk

0x9: SYSCLK:
sysclk

36.1.50 UDB_P0_U0_CFG29

Clock Selection for Datapath, Status and Control

Address: 0x400F305D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	SC_CK_SEL [7:4]				DP_CK_SEL [3:0]			

Bits	Name	Description
7 : 4	SC_CK_SEL	Clock selection registers Default Value: 0 **0x0: GCLK0:** gclk[0] **0x1: GCLK1:** gclk[1] **0x2: GCLK2:** gclk[2] **0x3: GCLK3:** gclk[3] **0x4: GCLK4:** gclk[4] **0x5: GCLK5:** gclk[5] **0x6: GCLK6:** gclk[6] **0x7: GCLK7:** gclk[7] **0x8: EXT_CLK:** ext_clk **0x9: SYSCLK:** sysclk
3 : 0	DP_CK_SEL	Clock selection registers Default Value: 0 **0x0: GCLK0:** gclk[0] **0x1: GCLK1:** gclk[1] **0x2: GCLK2:** gclk[2] **0x3: GCLK3:** gclk[3]

(continued)

0x4: GCLK4:
gclk[4]

0x5: GCLK5:
gclk[5]

0x6: GCLK6:
gclk[6]

0x7: GCLK7:
gclk[7]

0x8: EXT_CLK:
ext_clk

0x9: SYSCLK:
sysclk

36.1.51 UDB_P0_U0_CFG30

Reset control

Address: 0x400F305E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	None	RW	RW	RW	RW	
HW Access	R	R	None	R	R	R	R	
Name	SC_RES_POL	DP_RES_POL	None	GUDB_WR	EN_RES_CNTCTL	RES_POL	RES_SEL [1:0]	

Bits	Name	Description
7	SC_RES_POL	Only valid when ALT RES (CFG31) is '1'. This bit controls the polarity of the selected SC routed reset. Default Value: 0 **0x0: NOINV:** Routed reset to the Status and Control block is true polarity. **0x1: INVERT:** Routed reset to the Status and Control block is inverted polarity.
6	DP_RES_POL	Only valid when ALT RES (CFG31) is '1'. This bit controls the polarity of the selected Datapath routed reset. Default Value: 0 **0x0: NOINV:** Routed reset to the Datapath block is true polarity. **0x1: INVERT:** Routed reset to the Datapath block is inverted polarity.
4	GUDB_WR	Enable global write operation for the configuration and working registers in this UDB. When this bit is set, the UDB ID select decoding is bypassed. Default Value: 0 **0x0: DISABLE:** Global UDB configuration/working register write is disabled **0x1: ENABLE:** Global UDB configuration/working register write is enabled
3	EN_RES_CNTCTL	This bit gates the routed reset to the counter/control register. By default, the operation is compatible, i.e., it only applies to the counter. However, if the updated control regisiter modes are used (sync mode, pulse mode, or the ext res bit) then the routed reset applies to the control register also. Default Value: 0 **0x0: DISABLE:** Routed reset is not applied to counter/control register **0x1: ENABLE:** Routed reset is applied to the counter/control register

(continued)

2	RES_POL	The meaning of this bit depends on the value of the ALT RES bit in CFG31. When ALT RES is '0' (compatible mode), this bit sets the polarity of the routed reset. When ALT RES is '1', this bit is unused. Default Value: 0 **0x0: NEGATED:** Polarity of the routed reset is true. **0x1: ASSERTED:** Polarity of the routed reset is inverted.
1 : 0	RES_SEL	The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES is '0' (compatible mode), this 2 bit field selects the RC routing input for the compatible reset scheme. When the ALT RES bit is '1', these bits are not used. Default Value: 0 **0x0: RC_IN0:** rc_in[0] **0x1: RC_IN1:** rc_in[1] **0x2: RC_IN2:** rc_in[2] **0x3: RC_IN3:** rc_in[3]

36.1.52 UDB_P0_U0_CFG31

Reset control

Address: 0x400F305F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW		RW	RW	RW	RW
HW Access	R	R	R		R	R	R	R
Name	PLD1_RES_POL	PLD0_RES_POL	EXT_CK_SEL [5:4]		EN_RES_DP	EN_RES_STAT	EXT_SYNC	ALT_RES

Bits	Name	Description
7	PLD1_RES_POL	Not connected. NOTE: There is only one routed reset available to both PLDs in the UDB. When ALT RES is '1', PLD0 RES SEL controls the polarity of the routed reset for both PLDs. Default Value: 0 **0x0: NOINV:** Not Used **0x1: INVERT:** Not Used
6	PLD0_RES_POL	The meaning of this bit depends on the value of ALT RES. When ALT RES (CFG31) is '1', this bit controls the polarity of the selected PLD0 routed reset. NOTE: There is only one routed reset available to both PLDs in the UDB. When ALT RES is '1', PLD0 RES SEL controls the polarity of the routed reset for both PLDs. Default Value: 0 **0x0: NOINV:** Routed reset to the PLD0/PLD1 block is true polarity. **0x1: INVERT:** Routed reset to the PLD0/PLD1 block is inverted polarity.
5 : 4	EXT_CK_SEL	External clock selection Default Value: 0 **0x0: RC_IN0:** rc_in[0] **0x1: RC_IN1:** rc_in[1] **0x2: RC_IN2:** rc_in[2] **0x3: RC_IN3:** rc_in[3]
3	EN_RES_DP	Only valid when ALT RES (CFG31) is '1'. This bit gates the routed reset to the Datapath block. Default Value: 0 **0x0: DISABLE:** Routed reset to the Datapath block is gated off. **0x1: ENABLE:** Routed reset to the Datapath block is on. ALT RES must be '1' and routed reset must be selected in CFG26

(continued)

2	EN_RES_STAT	Only valid when ALT RES (CFG31) is '1'. This bit gates the routed reset to the status register. Default Value: 0 **0x0: NEGATED:** Status register routed reset is gated off **0x1: ASSERTED:** Status register routed reset is on
1	EXT_SYNC	Enable synchronization of selected external clock Default Value: 0 **0x0: DISABLE:** Selected external clock input is not synchronized **0x1: ENABLE:** Selected external clock input is synchronized
0	ALT_RES	This bit toggles between two reset configurations. When this bit is '0', one routed reset is shared by all components in this UDB (compatible mode). When this bit is a 1, each block can select a unique routed reset from the available RC inputs. Default Value: 0 **0x0: COMPATIBLE:** All UDB blocks share a common routed reset. **0x1: ALTERNATE:** Each UDB component block can select and control its individual routed reset.

36.1.53 UDB_P0_U0_DCFG0

Dynamic Configuration RAM

Address: 0x400F3060

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW	RW	RW	RW
HW Access	R		R		R	R	R	R
Name	A0_WR_SRC [7:6]		A1_WR_SRC [5:4]		CFB_EN	CI_SEL	SI_SEL	CMP_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW	RW		RW	
HW Access	R			R	R		R	
Name	FUNC [15:13]			SRC_A	SRC_B [11:10]		SHIFT [9:8]	

Bits	Name	Description
15 : 13	FUNC	Dynamic ALU function selection Default Value: X **0x0: PASS:** Pass **0x1: INC_A:** Increment source A **0x2: DEC_A:** Decrement source A **0x3: ADD:** Add **0x4: SUB:** Subtract **0x5: XOR:** Bitwise XOR **0x6: AND:** Bitwise AND **0x7: OR:** Bitwise OR
12	SRC_A	Dynamic ALU source A selection Default Value: X **0x0: A0:** Configuration A **0x1: A1:** Configuration B
11 : 10	SRC_B	Dynamic ALU source B selection Default Value: X

(continued)

		0x0: D0: ALU source B is D0 **0x1: D1:** ALU source B is D1 **0x2: A0:** ALU source B is A0 **0x3: A1:** ALU source B is A1
9 : 8	SHIFT	Dynamic shift selection Default Value: X **0x0: NOSHIFT:** No shift **0x1: LEFT:** Left Shift **0x2: RIGHT:** Right Shift **0x3: SWAP:** Nibble swap
7 : 6	A0_WR_SRC	Dynamic A0 write source selection Default Value: X **0x0: NOWRITE:** no value written to A0 **0x1: ALU:** ALU output written to A0 **0x2: D0:** D1 value written to A0 **0x3: F0:** F1 value written to A0
5 : 4	A1_WR_SRC	Dynamic A1 write source selection Default Value: X **0x0: NOWRITE:** no value written to A1 **0x1: ALU:** ALU output written to A1 **0x2: D1:** D1 value written to A1 **0x3: F1:** F1 value written to A1
3	CFB_EN	Dynamic CRC feedback selection Default Value: X **0x0: DISABLE:** CRC feedback disabled **0x1: ENABLE:** CRC feedback enabled

(continued)

2	CI_SEL	Dynamic carry in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
1	SI_SEL	Dynamic shift in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
0	CMP_SEL	Dynamic compare selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B

36.1.54 UDB_P0_U0_DCFG1

Dynamic Configuration RAM

Address: 0x400F3062

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW	RW	RW	RW
HW Access	R		R		R	R	R	R
Name	A0_WR_SRC [7:6]		A1_WR_SRC [5:4]		CFB_EN	CI_SEL	SI_SEL	CMP_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW	RW		RW	
HW Access	R			R	R		R	
Name	FUNC [15:13]			SRC_A	SRC_B [11:10]		SHIFT [9:8]	

Bits	Name	Description
15 : 13	FUNC	Dynamic ALU function selection Default Value: X **0x0: PASS:** Pass **0x1: INC_A:** Increment source A **0x2: DEC_A:** Decrement source A **0x3: ADD:** Add **0x4: SUB:** Subtract **0x5: XOR:** Bitwise XOR **0x6: AND:** Bitwise AND **0x7: OR:** Bitwise OR
12	SRC_A	Dynamic ALU source A selection Default Value: X **0x0: A0:** Configuration A **0x1: A1:** Configuration B
11 : 10	SRC_B	Dynamic ALU source B selection Default Value: X

(continued)

		0x0: D0: ALU source B is D0 **0x1: D1:** ALU source B is D1 **0x2: A0:** ALU source B is A0 **0x3: A1:** ALU source B is A1
9 : 8	SHIFT	Dynamic shift selection Default Value: X **0x0: NOSHIFT:** No shift **0x1: LEFT:** Left Shift **0x2: RIGHT:** Right Shift **0x3: SWAP:** Nibble swap
7 : 6	A0_WR_SRC	Dynamic A0 write source selection Default Value: X **0x0: NOWRITE:** no value written to A0 **0x1: ALU:** ALU output written to A0 **0x2: D0:** D1 value written to A0 **0x3: F0:** F1 value written to A0
5 : 4	A1_WR_SRC	Dynamic A1 write source selection Default Value: X **0x0: NOWRITE:** no value written to A1 **0x1: ALU:** ALU output written to A1 **0x2: D1:** D1 value written to A1 **0x3: F1:** F1 value written to A1
3	CFB_EN	Dynamic CRC feedback selection Default Value: X **0x0: DISABLE:** CRC feedback disabled **0x1: ENABLE:** CRC feedback enabled

(continued)

2	CI_SEL	Dynamic carry in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
1	SI_SEL	Dynamic shift in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
0	CMP_SEL	Dynamic compare selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B

36.1.55 UDB_P0_U0_DCFG2

Dynamic Configuration RAM

Address: 0x400F3064

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW	RW	RW	RW
HW Access	R		R		R	R	R	R
Name	A0_WR_SRC [7:6]		A1_WR_SRC [5:4]		CFB_EN	CI_SEL	SI_SEL	CMP_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW	RW		RW	
HW Access	R			R	R		R	
Name	FUNC [15:13]			SRC_A	SRC_B [11:10]		SHIFT [9:8]	

Bits	Name	Description
15 : 13	FUNC	Dynamic ALU function selection Default Value: X **0x0: PASS:** Pass **0x1: INC_A:** Increment source A **0x2: DEC_A:** Decrement source A **0x3: ADD:** Add **0x4: SUB:** Subtract **0x5: XOR:** Bitwise XOR **0x6: AND:** Bitwise AND **0x7: OR:** Bitwise OR
12	SRC_A	Dynamic ALU source A selection Default Value: X **0x0: A0:** Configuration A **0x1: A1:** Configuration B
11 : 10	SRC_B	Dynamic ALU source B selection Default Value: X

(continued)

		0x0: D0: ALU source B is D0 **0x1: D1:** ALU source B is D1 **0x2: A0:** ALU source B is A0 **0x3: A1:** ALU source B is A1
9 : 8	SHIFT	Dynamic shift selection Default Value: X **0x0: NOSHIFT:** No shift **0x1: LEFT:** Left Shift **0x2: RIGHT:** Right Shift **0x3: SWAP:** Nibble swap
7 : 6	A0_WR_SRC	Dynamic A0 write source selection Default Value: X **0x0: NOWRITE:** no value written to A0 **0x1: ALU:** ALU output written to A0 **0x2: D0:** D1 value written to A0 **0x3: F0:** F1 value written to A0
5 : 4	A1_WR_SRC	Dynamic A1 write source selection Default Value: X **0x0: NOWRITE:** no value written to A1 **0x1: ALU:** ALU output written to A1 **0x2: D1:** D1 value written to A1 **0x3: F1:** F1 value written to A1
3	CFB_EN	Dynamic CRC feedback selection Default Value: X **0x0: DISABLE:** CRC feedback disabled **0x1: ENABLE:** CRC feedback enabled

(continued)

2	CI_SEL	Dynamic carry in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
1	SI_SEL	Dynamic shift in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
0	CMP_SEL	Dynamic compare selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B

36.1.56 UDB_P0_U0_DCFG3

Dynamic Configuration RAM

Address: 0x400F3066

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW	RW	RW	RW
HW Access	R		R		R	R	R	R
Name	A0_WR_SRC [7:6]		A1_WR_SRC [5:4]		CFB_EN	CI_SEL	SI_SEL	CMP_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW	RW		RW	
HW Access	R			R	R		R	
Name	FUNC [15:13]			SRC_A	SRC_B [11:10]		SHIFT [9:8]	

Bits	Name	Description
15 : 13	FUNC	Dynamic ALU function selection Default Value: X **0x0: PASS:** Pass **0x1: INC_A:** Increment source A **0x2: DEC_A:** Decrement source A **0x3: ADD:** Add **0x4: SUB:** Subtract **0x5: XOR:** Bitwise XOR **0x6: AND:** Bitwise AND **0x7: OR:** Bitwise OR
12	SRC_A	Dynamic ALU source A selection Default Value: X **0x0: A0:** Configuration A **0x1: A1:** Configuration B
11 : 10	SRC_B	Dynamic ALU source B selection Default Value: X

(continued)

		0x0: D0: ALU source B is D0 **0x1: D1:** ALU source B is D1 **0x2: A0:** ALU source B is A0 **0x3: A1:** ALU source B is A1
9 : 8	SHIFT	Dynamic shift selection Default Value: X **0x0: NOSHIFT:** No shift **0x1: LEFT:** Left Shift **0x2: RIGHT:** Right Shift **0x3: SWAP:** Nibble swap
7 : 6	A0_WR_SRC	Dynamic A0 write source selection Default Value: X **0x0: NOWRITE:** no value written to A0 **0x1: ALU:** ALU output written to A0 **0x2: D0:** D1 value written to A0 **0x3: F0:** F1 value written to A0
5 : 4	A1_WR_SRC	Dynamic A1 write source selection Default Value: X **0x0: NOWRITE:** no value written to A1 **0x1: ALU:** ALU output written to A1 **0x2: D1:** D1 value written to A1 **0x3: F1:** F1 value written to A1
3	CFB_EN	Dynamic CRC feedback selection Default Value: X **0x0: DISABLE:** CRC feedback disabled **0x1: ENABLE:** CRC feedback enabled

(continued)

2	CI_SEL	Dynamic carry in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
1	SI_SEL	Dynamic shift in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
0	CMP_SEL	Dynamic compare selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B

36.1.57 UDB_P0_U0_DCFG4

Dynamic Configuration RAM

Address: 0x400F3068

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW	RW	RW	RW
HW Access	R		R		R	R	R	R
Name	A0_WR_SRC [7:6]		A1_WR_SRC [5:4]		CFB_EN	CI_SEL	SI_SEL	CMP_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW	RW		RW	
HW Access	R			R	R		R	
Name	FUNC [15:13]			SRC_A	SRC_B [11:10]		SHIFT [9:8]	

Bits	Name	Description
15 : 13	FUNC	Dynamic ALU function selection Default Value: X **0x0: PASS:** Pass **0x1: INC_A:** Increment source A **0x2: DEC_A:** Decrement source A **0x3: ADD:** Add **0x4: SUB:** Subtract **0x5: XOR:** Bitwise XOR **0x6: AND:** Bitwise AND **0x7: OR:** Bitwise OR
12	SRC_A	Dynamic ALU source A selection Default Value: X **0x0: A0:** Configuration A **0x1: A1:** Configuration B
11 : 10	SRC_B	Dynamic ALU source B selection Default Value: X

(continued)

		0x0: D0: ALU source B is D0 **0x1: D1:** ALU source B is D1 **0x2: A0:** ALU source B is A0 **0x3: A1:** ALU source B is A1
9 : 8	SHIFT	Dynamic shift selection Default Value: X **0x0: NOSHIFT:** No shift **0x1: LEFT:** Left Shift **0x2: RIGHT:** Right Shift **0x3: SWAP:** Nibble swap
7 : 6	A0_WR_SRC	Dynamic A0 write source selection Default Value: X **0x0: NOWRITE:** no value written to A0 **0x1: ALU:** ALU output written to A0 **0x2: D0:** D1 value written to A0 **0x3: F0:** F1 value written to A0
5 : 4	A1_WR_SRC	Dynamic A1 write source selection Default Value: X **0x0: NOWRITE:** no value written to A1 **0x1: ALU:** ALU output written to A1 **0x2: D1:** D1 value written to A1 **0x3: F1:** F1 value written to A1
3	CFB_EN	Dynamic CRC feedback selection Default Value: X **0x0: DISABLE:** CRC feedback disabled **0x1: ENABLE:** CRC feedback enabled

(continued)

2	CI_SEL	Dynamic carry in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
1	SI_SEL	Dynamic shift in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
0	CMP_SEL	Dynamic compare selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B

36.1.58 UDB_P0_U0_DCFG5

Dynamic Configuration RAM

Address: 0x400F306A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW	RW	RW	RW
HW Access	R		R		R	R	R	R
Name	A0_WR_SRC [7:6]		A1_WR_SRC [5:4]		CFB_EN	CI_SEL	SI_SEL	CMP_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW	RW		RW	
HW Access	R			R	R		R	
Name	FUNC [15:13]			SRC_A	SRC_B [11:10]		SHIFT [9:8]	

Bits	Name	Description
15 : 13	FUNC	Dynamic ALU function selection Default Value: X **0x0: PASS:** Pass **0x1: INC_A:** Increment source A **0x2: DEC_A:** Decrement source A **0x3: ADD:** Add **0x4: SUB:** Subtract **0x5: XOR:** Bitwise XOR **0x6: AND:** Bitwise AND **0x7: OR:** Bitwise OR
12	SRC_A	Dynamic ALU source A selection Default Value: X **0x0: A0:** Configuration A **0x1: A1:** Configuration B
11 : 10	SRC_B	Dynamic ALU source B selection Default Value: X

(continued)

		0x0: D0: ALU source B is D0 **0x1: D1:** ALU source B is D1 **0x2: A0:** ALU source B is A0 **0x3: A1:** ALU source B is A1
9 : 8	SHIFT	Dynamic shift selection Default Value: X **0x0: NOSHIFT:** No shift **0x1: LEFT:** Left Shift **0x2: RIGHT:** Right Shift **0x3: SWAP:** Nibble swap
7 : 6	A0_WR_SRC	Dynamic A0 write source selection Default Value: X **0x0: NOWRITE:** no value written to A0 **0x1: ALU:** ALU output written to A0 **0x2: D0:** D1 value written to A0 **0x3: F0:** F1 value written to A0
5 : 4	A1_WR_SRC	Dynamic A1 write source selection Default Value: X **0x0: NOWRITE:** no value written to A1 **0x1: ALU:** ALU output written to A1 **0x2: D1:** D1 value written to A1 **0x3: F1:** F1 value written to A1
3	CFB_EN	Dynamic CRC feedback selection Default Value: X **0x0: DISABLE:** CRC feedback disabled **0x1: ENABLE:** CRC feedback enabled

(continued)

2	CI_SEL	Dynamic carry in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
1	SI_SEL	Dynamic shift in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
0	CMP_SEL	Dynamic compare selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B

36.1.59 UDB_P0_U0_DCFG6

Dynamic Configuration RAM

Address: 0x400F306C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW	RW	RW	RW
HW Access	R		R		R	R	R	R
Name	A0_WR_SRC [7:6]		A1_WR_SRC [5:4]		CFB_EN	CI_SEL	SI_SEL	CMP_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW	RW		RW	
HW Access	R			R	R		R	
Name	FUNC [15:13]			SRC_A	SRC_B [11:10]		SHIFT [9:8]	

Bits	Name	Description
15 : 13	FUNC	Dynamic ALU function selection Default Value: X **0x0: PASS:** Pass **0x1: INC_A:** Increment source A **0x2: DEC_A:** Decrement source A **0x3: ADD:** Add **0x4: SUB:** Subtract **0x5: XOR:** Bitwise XOR **0x6: AND:** Bitwise AND **0x7: OR:** Bitwise OR
12	SRC_A	Dynamic ALU source A selection Default Value: X **0x0: A0:** Configuration A **0x1: A1:** Configuration B
11 : 10	SRC_B	Dynamic ALU source B selection Default Value: X

(continued)

		0x0: D0: ALU source B is D0 **0x1: D1:** ALU source B is D1 **0x2: A0:** ALU source B is A0 **0x3: A1:** ALU source B is A1
9 : 8	SHIFT	Dynamic shift selection Default Value: X **0x0: NOSHIFT:** No shift **0x1: LEFT:** Left Shift **0x2: RIGHT:** Right Shift **0x3: SWAP:** Nibble swap
7 : 6	A0_WR_SRC	Dynamic A0 write source selection Default Value: X **0x0: NOWRITE:** no value written to A0 **0x1: ALU:** ALU output written to A0 **0x2: D0:** D1 value written to A0 **0x3: F0:** F1 value written to A0
5 : 4	A1_WR_SRC	Dynamic A1 write source selection Default Value: X **0x0: NOWRITE:** no value written to A1 **0x1: ALU:** ALU output written to A1 **0x2: D1:** D1 value written to A1 **0x3: F1:** F1 value written to A1
3	CFB_EN	Dynamic CRC feedback selection Default Value: X **0x0: DISABLE:** CRC feedback disabled **0x1: ENABLE:** CRC feedback enabled

(continued)

2	CI_SEL	Dynamic carry in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
1	SI_SEL	Dynamic shift in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
0	CMP_SEL	Dynamic compare selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B

36.1.60 UDB_P0_U0_DCFG7

Dynamic Configuration RAM

Address: 0x400F306E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW	RW	RW	RW
HW Access	R		R		R	R	R	R
Name	A0_WR_SRC [7:6]		A1_WR_SRC [5:4]		CFB_EN	CI_SEL	SI_SEL	CMP_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW	RW		RW	
HW Access	R			R	R		R	
Name	FUNC [15:13]			SRC_A	SRC_B [11:10]		SHIFT [9:8]	

Bits	Name	Description
15 : 13	FUNC	Dynamic ALU function selection Default Value: X **0x0: PASS:** Pass **0x1: INC_A:** Increment source A **0x2: DEC_A:** Decrement source A **0x3: ADD:** Add **0x4: SUB:** Subtract **0x5: XOR:** Bitwise XOR **0x6: AND:** Bitwise AND **0x7: OR:** Bitwise OR
12	SRC_A	Dynamic ALU source A selection Default Value: X **0x0: A0:** Configuration A **0x1: A1:** Configuration B
11 : 10	SRC_B	Dynamic ALU source B selection Default Value: X

(continued)

		0x0: D0: ALU source B is D0 **0x1: D1:** ALU source B is D1 **0x2: A0:** ALU source B is A0 **0x3: A1:** ALU source B is A1
9 : 8	SHIFT	Dynamic shift selection Default Value: X **0x0: NOSHIFT:** No shift **0x1: LEFT:** Left Shift **0x2: RIGHT:** Right Shift **0x3: SWAP:** Nibble swap
7 : 6	A0_WR_SRC	Dynamic A0 write source selection Default Value: X **0x0: NOWRITE:** no value written to A0 **0x1: ALU:** ALU output written to A0 **0x2: D0:** D1 value written to A0 **0x3: F0:** F1 value written to A0
5 : 4	A1_WR_SRC	Dynamic A1 write source selection Default Value: X **0x0: NOWRITE:** no value written to A1 **0x1: ALU:** ALU output written to A1 **0x2: D1:** D1 value written to A1 **0x3: F1:** F1 value written to A1
3	CFB_EN	Dynamic CRC feedback selection Default Value: X **0x0: DISABLE:** CRC feedback disabled **0x1: ENABLE:** CRC feedback enabled

(continued)

2	CI_SEL	Dynamic carry in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
1	SI_SEL	Dynamic shift in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
0	CMP_SEL	Dynamic compare selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B

36.1.61 UDB_P0_U1_PLD_IT0

PLD Input Terms

Address: 0x400F3080

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Bits	Name	Description
31	PLD1_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X

(continued)

25	PLD1_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
22	PLD0_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X

(continued)

3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X

36.1.62 UDB_P0_U1_PLD_IT1

PLD Input Terms

Address: 0x400F3084

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Bits	Name	Description
31	PLD1_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X

(continued)

25	PLD1_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
22	PLD0_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X

(continued)

3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X

36.1.63 UDB_P0_U1_PLD_IT2

PLD Input Terms

Address: 0x400F3088

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Bits	Name	Description
31	PLD1_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X

(continued)

25	PLD1_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
22	PLD0_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X

(continued)

3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X

36.1.64 UDB_P0_U1_PLD_IT3

PLD Input Terms

Address: 0x400F308C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Bits	Name	Description
31	PLD1_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X

(continued)

25	PLD1_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
22	PLD0_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X

(continued)

3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X

36.1.65 UDB_P0_U1_PLD_IT4

PLD Input Terms

Address: 0x400F3090

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Bits	Name	Description
31	PLD1_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X

(continued)

25	PLD1_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
22	PLD0_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X

(continued)

3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X

36.1.66 UDB_P0_U1_PLD_IT5

PLD Input Terms

Address: 0x400F3094

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Bits	Name	Description
31	PLD1_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X

(continued)

25	PLD1_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
22	PLD0_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X

(continued)

3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X

36.1.67 UDB_P0_U1_PLD_IT6

PLD Input Terms

Address: 0x400F3098

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Bits	Name	Description
31	PLD1_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X

(continued)

25	PLD1_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
22	PLD0_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X

(continued)

3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X

36.1.68 UDB_P0_U1_PLD_IT7

PLD Input Terms

Address: 0x400F309C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Bits	Name	Description
31	PLD1_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X

(continued)

25	PLD1_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
22	PLD0_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X

(continued)

3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X

36.1.69 UDB_P0_U1_PLD_IT8

PLD Input Terms

Address: 0x400F30A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Bits	Name	Description
31	PLD1_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X

(continued)

25	PLD1_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
22	PLD0_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X

(continued)

3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X

36.1.70 UDB_P0_U1_PLD_IT9

PLD Input Terms

Address: 0x400F30A4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Bits	Name	Description
31	PLD1_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X

(continued)

25	PLD1_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
22	PLD0_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X

(continued)

3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X

36.1.71 UDB_P0_U1_PLD_IT10

PLD Input Terms

Address: 0x400F30A8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Bits	Name	Description
31	PLD1_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X

(continued)

25	PLD1_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
22	PLD0_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X

(continued)

3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X

36.1.72 UDB_P0_U1_PLD_IT11

PLD Input Terms

Address: 0x400F30AC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Bits	Name	Description
31	PLD1_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X

(continued)

25	PLD1_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
22	PLD0_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X

(continued)

3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X

36.1.73 UDB_P0_U1_PLD_ORT0

PLD OR Terms

Address: 0x400F30B0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ORT_PTx_7	PLD0_ORT_PTx_6	PLD0_ORT_PTx_5	PLD0_ORT_PTx_4	PLD0_ORT_PTx_3	PLD0_ORT_PTx_2	PLD0_ORT_PTx_1	PLD0_ORT_PTx_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ORT_PTx_7	PLD1_ORT_PTx_6	PLD1_ORT_PTx_5	PLD1_ORT_PTx_4	PLD1_ORT_PTx_3	PLD1_ORT_PTx_2	PLD1_ORT_PTx_1	PLD1_ORT_PTx_0

Bits	Name	Description
15	PLD1_ORT_PTx_7	OR term. Bit position corresponds to product term. Default Value: X
14	PLD1_ORT_PTx_6	OR term. Bit position corresponds to product term. Default Value: X
13	PLD1_ORT_PTx_5	OR term. Bit position corresponds to product term. Default Value: X
12	PLD1_ORT_PTx_4	OR term. Bit position corresponds to product term. Default Value: X
11	PLD1_ORT_PTx_3	OR term. Bit position corresponds to product term. Default Value: X
10	PLD1_ORT_PTx_2	OR term. Bit position corresponds to product term. Default Value: X
9	PLD1_ORT_PTx_1	OR term. Bit position corresponds to product term. Default Value: X
8	PLD1_ORT_PTx_0	OR term. Bit position corresponds to product term. Default Value: X
7	PLD0_ORT_PTx_7	OR term. Bit position corresponds to product term. Default Value: X
6	PLD0_ORT_PTx_6	OR term. Bit position corresponds to product term. Default Value: X
5	PLD0_ORT_PTx_5	OR term. Bit position corresponds to product term. Default Value: X
4	PLD0_ORT_PTx_4	OR term. Bit position corresponds to product term. Default Value: X

(continued)

3	PLD0_ORT_PTx_3	OR term. Bit position corresponds to product term. Default Value: X
2	PLD0_ORT_PTx_2	OR term. Bit position corresponds to product term. Default Value: X
1	PLD0_ORT_PTx_1	OR term. Bit position corresponds to product term. Default Value: X
0	PLD0_ORT_PTx_0	OR term. Bit position corresponds to product term. Default Value: X

36.1.74 UDB_P0_U1_PLD_ORT1

PLD OR Terms

Address: 0x400F30B2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ORT_PTx_7	PLD0_ORT_PTx_6	PLD0_ORT_PTx_5	PLD0_ORT_PTx_4	PLD0_ORT_PTx_3	PLD0_ORT_PTx_2	PLD0_ORT_PTx_1	PLD0_ORT_PTx_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ORT_PTx_7	PLD1_ORT_PTx_6	PLD1_ORT_PTx_5	PLD1_ORT_PTx_4	PLD1_ORT_PTx_3	PLD1_ORT_PTx_2	PLD1_ORT_PTx_1	PLD1_ORT_PTx_0

Bits	Name	Description
15	PLD1_ORT_PTx_7	OR term. Bit position corresponds to product term. Default Value: X
14	PLD1_ORT_PTx_6	OR term. Bit position corresponds to product term. Default Value: X
13	PLD1_ORT_PTx_5	OR term. Bit position corresponds to product term. Default Value: X
12	PLD1_ORT_PTx_4	OR term. Bit position corresponds to product term. Default Value: X
11	PLD1_ORT_PTx_3	OR term. Bit position corresponds to product term. Default Value: X
10	PLD1_ORT_PTx_2	OR term. Bit position corresponds to product term. Default Value: X
9	PLD1_ORT_PTx_1	OR term. Bit position corresponds to product term. Default Value: X
8	PLD1_ORT_PTx_0	OR term. Bit position corresponds to product term. Default Value: X
7	PLD0_ORT_PTx_7	OR term. Bit position corresponds to product term. Default Value: X
6	PLD0_ORT_PTx_6	OR term. Bit position corresponds to product term. Default Value: X
5	PLD0_ORT_PTx_5	OR term. Bit position corresponds to product term. Default Value: X
4	PLD0_ORT_PTx_4	OR term. Bit position corresponds to product term. Default Value: X

(continued)

3	PLD0_ORT_PTx_3	OR term. Bit position corresponds to product term. Default Value: X
2	PLD0_ORT_PTx_2	OR term. Bit position corresponds to product term. Default Value: X
1	PLD0_ORT_PTx_1	OR term. Bit position corresponds to product term. Default Value: X
0	PLD0_ORT_PTx_0	OR term. Bit position corresponds to product term. Default Value: X

36.1.75 UDB_P0_U1_PLD_ORT2

PLD OR Terms

Address: 0x400F30B4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ORT_PTx_7	PLD0_ORT_PTx_6	PLD0_ORT_PTx_5	PLD0_ORT_PTx_4	PLD0_ORT_PTx_3	PLD0_ORT_PTx_2	PLD0_ORT_PTx_1	PLD0_ORT_PTx_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ORT_PTx_7	PLD1_ORT_PTx_6	PLD1_ORT_PTx_5	PLD1_ORT_PTx_4	PLD1_ORT_PTx_3	PLD1_ORT_PTx_2	PLD1_ORT_PTx_1	PLD1_ORT_PTx_0

Bits	Name	Description
15	PLD1_ORT_PTx_7	OR term. Bit position corresponds to product term. Default Value: X
14	PLD1_ORT_PTx_6	OR term. Bit position corresponds to product term. Default Value: X
13	PLD1_ORT_PTx_5	OR term. Bit position corresponds to product term. Default Value: X
12	PLD1_ORT_PTx_4	OR term. Bit position corresponds to product term. Default Value: X
11	PLD1_ORT_PTx_3	OR term. Bit position corresponds to product term. Default Value: X
10	PLD1_ORT_PTx_2	OR term. Bit position corresponds to product term. Default Value: X
9	PLD1_ORT_PTx_1	OR term. Bit position corresponds to product term. Default Value: X
8	PLD1_ORT_PTx_0	OR term. Bit position corresponds to product term. Default Value: X
7	PLD0_ORT_PTx_7	OR term. Bit position corresponds to product term. Default Value: X
6	PLD0_ORT_PTx_6	OR term. Bit position corresponds to product term. Default Value: X
5	PLD0_ORT_PTx_5	OR term. Bit position corresponds to product term. Default Value: X
4	PLD0_ORT_PTx_4	OR term. Bit position corresponds to product term. Default Value: X

(continued)

3	PLD0_ORT_PTx_3	OR term. Bit position corresponds to product term. Default Value: X
2	PLD0_ORT_PTx_2	OR term. Bit position corresponds to product term. Default Value: X
1	PLD0_ORT_PTx_1	OR term. Bit position corresponds to product term. Default Value: X
0	PLD0_ORT_PTx_0	OR term. Bit position corresponds to product term. Default Value: X

36.1.76 UDB_P0_U1_PLD_ORT3

PLD OR Terms

Address: 0x400F30B6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ORT_PTx_7	PLD0_ORT_PTx_6	PLD0_ORT_PTx_5	PLD0_ORT_PTx_4	PLD0_ORT_PTx_3	PLD0_ORT_PTx_2	PLD0_ORT_PTx_1	PLD0_ORT_PTx_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ORT_PTx_7	PLD1_ORT_PTx_6	PLD1_ORT_PTx_5	PLD1_ORT_PTx_4	PLD1_ORT_PTx_3	PLD1_ORT_PTx_2	PLD1_ORT_PTx_1	PLD1_ORT_PTx_0

Bits	Name	Description
15	PLD1_ORT_PTx_7	OR term. Bit position corresponds to product term. Default Value: X
14	PLD1_ORT_PTx_6	OR term. Bit position corresponds to product term. Default Value: X
13	PLD1_ORT_PTx_5	OR term. Bit position corresponds to product term. Default Value: X
12	PLD1_ORT_PTx_4	OR term. Bit position corresponds to product term. Default Value: X
11	PLD1_ORT_PTx_3	OR term. Bit position corresponds to product term. Default Value: X
10	PLD1_ORT_PTx_2	OR term. Bit position corresponds to product term. Default Value: X
9	PLD1_ORT_PTx_1	OR term. Bit position corresponds to product term. Default Value: X
8	PLD1_ORT_PTx_0	OR term. Bit position corresponds to product term. Default Value: X
7	PLD0_ORT_PTx_7	OR term. Bit position corresponds to product term. Default Value: X
6	PLD0_ORT_PTx_6	OR term. Bit position corresponds to product term. Default Value: X
5	PLD0_ORT_PTx_5	OR term. Bit position corresponds to product term. Default Value: X
4	PLD0_ORT_PTx_4	OR term. Bit position corresponds to product term. Default Value: X

(continued)

3	PLD0_ORT_PTx_3	OR term. Bit position corresponds to product term. Default Value: X
2	PLD0_ORT_PTx_2	OR term. Bit position corresponds to product term. Default Value: X
1	PLD0_ORT_PTx_1	OR term. Bit position corresponds to product term. Default Value: X
0	PLD0_ORT_PTx_0	OR term. Bit position corresponds to product term. Default Value: X

36.1.77 UDB_P0_U1_PLD_MC_CFG_CEN_CONST

Macrocell configuration for Carry Enable and Constant

Address: 0x400F30B8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_MC3_DFF_C	PLD0_MC3_CEN	PLD0_MC2_DFF_C	PLD0_MC2_CEN	PLD0_MC1_DFF_C	PLD0_MC1_CEN	PLD0_MC0_DFF_C	PLD0_MC0_CEN

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_MC3_DFF_C	PLD1_MC3_CEN	PLD1_MC2_DFF_C	PLD1_MC2_CEN	PLD1_MC1_DFF_C	PLD1_MC1_CEN	PLD1_MC0_DFF_C	PLD1_MC0_CEN

Bits	Name	Description
15	PLD1_MC3_DFF_C	DFF Constant Default Value: X **0x0: NOINV:** DFF non-inverted **0x1: INVERTED:** DFF inverted
14	PLD1_MC3_CEN	Carry enable Default Value: X **0x0: DISABLE:** Disabled **0x1: ENABLE:** Enabled
13	PLD1_MC2_DFF_C	DFF Constant Default Value: X **0x0: NOINV:** DFF non-inverted **0x1: INVERTED:** DFF inverted
12	PLD1_MC2_CEN	Carry enable Default Value: X **0x0: DISABLE:** Disabled **0x1: ENABLE:** Enabled

(continued)

11	PLD1_MC1_DFF_C	DFF Constant Default Value: X **0x0: NOINV:** DFF non-inverted **0x1: INVERTED:** DFF inverted
10	PLD1_MC1_CEN	Carry enable Default Value: X **0x0: DISABLE:** Disabled **0x1: ENABLE:** Enabled
9	PLD1_MC0_DFF_C	DFF Constant Default Value: X **0x0: NOINV:** DFF non-inverted **0x1: INVERTED:** DFF inverted
8	PLD1_MC0_CEN	Carry enable Default Value: X **0x0: DISABLE:** Disabled **0x1: ENABLE:** Enabled
7	PLD0_MC3_DFF_C	DFF Constant Default Value: X **0x0: NOINV:** DFF non-inverted **0x1: INVERTED:** DFF inverted
6	PLD0_MC3_CEN	Carry enable Default Value: X **0x0: DISABLE:** Disabled **0x1: ENABLE:** Enabled
5	PLD0_MC2_DFF_C	DFF Constant Default Value: X **0x0: NOINV:** DFF non-inverted **0x1: INVERTED:** DFF inverted
4	PLD0_MC2_CEN	Carry enable Default Value: X

(continued)

		0x0: DISABLE: Disabled **0x1: ENABLE:** Enabled
3	PLD0_MC1_DFF_C	DFF Constant Default Value: X **0x0: NOINV:** DFF non-inverted **0x1: INVERTED:** DFF inverted
2	PLD0_MC1_CEN	Carry enable Default Value: X **0x0: DISABLE:** Disabled **0x1: ENABLE:** Enabled
1	PLD0_MC0_DFF_C	DFF Constant Default Value: X **0x0: NOINV:** DFF non-inverted **0x1: INVERTED:** DFF inverted
0	PLD0_MC0_CEN	Carry enable Default Value: X **0x0: DISABLE:** Disabled **0x1: ENABLE:** Enabled

36.1.78 UDB_P0_U1_PLD_MC_CFG_XORFB

PLD Macro cell XOR feedback

Address: 0x400F30BA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	PLD0_MC3_XORFB [7:6]		PLD0_MC2_XORFB [5:4]		PLD0_MC1_XORFB [3:2]		PLD0_MC0_XORFB [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	PLD1_MC3_XORFB [15:14]		PLD1_MC2_XORFB [13:12]		PLD1_MC1_XORFB [11:10]		PLD1_MC0_XORFB [9:8]	

Bits	Name	Description
15 : 14	PLD1_MC3_XORFB	XOR feedback Default Value: X **0x0: DFF:** DFF **0x1: CARRY:** Carry **0x2: TFF_H:** TFF on high **0x3: TFF_L:** TFF on low
13 : 12	PLD1_MC2_XORFB	XOR feedback Default Value: X **0x0: DFF:** DFF **0x1: CARRY:** Carry **0x2: TFF_H:** TFF on high **0x3: TFF_L:** TFF on low
11 : 10	PLD1_MC1_XORFB	XOR feedback Default Value: X **0x0: DFF:** DFF **0x1: CARRY:** Carry

(continued)

		0x2: TFF_H: TFF on high **0x3: TFF_L:** TFF on low
9 : 8	PLD1_MC0_XORFB	XOR feedback Default Value: X **0x0: DFF:** DFF **0x1: CARRY:** Carry **0x2: TFF_H:** TFF on high **0x3: TFF_L:** TFF on low
7 : 6	PLD0_MC3_XORFB	XOR feedback Default Value: X **0x0: DFF:** DFF **0x1: CARRY:** Carry **0x2: TFF_H:** TFF on high **0x3: TFF_L:** TFF on low
5 : 4	PLD0_MC2_XORFB	XOR feedback Default Value: X **0x0: DFF:** DFF **0x1: CARRY:** Carry **0x2: TFF_H:** TFF on high **0x3: TFF_L:** TFF on low
3 : 2	PLD0_MC1_XORFB	XOR feedback Default Value: X **0x0: DFF:** DFF **0x1: CARRY:** Carry **0x2: TFF_H:** TFF on high **0x3: TFF_L:** TFF on low

(continued)

1 : 0	PLD0_MC0_XORFB	XOR feedback Default Value: X **0x0: DFF:** DFF **0x1: CARRY:** Carry **0x2: TFF_H:** TFF on high **0x3: TFF_L:** TFF on low

36.1.79 UDB_P0_U1_PLD_MC_SET_RESET

PLD Macro cell Set Reset Selection

Address: 0x400F30BC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_MC3_RESET_SEL	PLD0_MC3_SET_SEL	PLD0_MC2_RESET_SEL	PLD0_MC2_SET_SEL	PLD0_MC1_RESET_SEL	PLD0_MC1_SET_SEL	PLD0_MC0_RESET_SEL	PLD0_MC0_SET_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_MC3_RESET_SEL	PLD1_MC3_SET_SEL	PLD1_MC2_RESET_SEL	PLD1_MC2_SET_SEL	PLD1_MC1_RESET_SEL	PLD1_MC1_SET_SEL	PLD1_MC0_RESET_SEL	PLD1_MC0_SET_SEL

Bits	Name	Description
15	PLD1_MC3_RESET_SEL	Reset select enable Default Value: X **0x0: DISABLE:** Reset not used **0x1: ENABLE:** Reset enabled
14	PLD1_MC3_SET_SEL	Set select enable Default Value: X **0x0: DISABLE:** Set not used **0x1: ENABLE:** Set enabled
13	PLD1_MC2_RESET_SEL	Reset select enable Default Value: X **0x0: DISABLE:** Reset not used **0x1: ENABLE:** Reset enabled
12	PLD1_MC2_SET_SEL	Set select enable Default Value: X **0x0: DISABLE:** Set not used **0x1: ENABLE:** Set enabled

(continued)

11	PLD1_MC1_RESET_SEL	Reset select enable Default Value: X **0x0: DISABLE:** Reset not used **0x1: ENABLE:** Reset enabled
10	PLD1_MC1_SET_SEL	Set select enable Default Value: X **0x0: DISABLE:** Set not used **0x1: ENABLE:** Set enabled
9	PLD1_MC0_RESET_SEL	Reset select enable Default Value: X **0x0: DISABLE:** Reset not used **0x1: ENABLE:** Reset enabled
8	PLD1_MC0_SET_SEL	Set select enable Default Value: X **0x0: DISABLE:** Set not used **0x1: ENABLE:** Set enabled
7	PLD0_MC3_RESET_SEL	Reset select enable Default Value: X **0x0: DISABLE:** Reset not used **0x1: ENABLE:** Reset enabled
6	PLD0_MC3_SET_SEL	Set select enable Default Value: X **0x0: DISABLE:** Set not used **0x1: ENABLE:** Set enabled
5	PLD0_MC2_RESET_SEL	Reset select enable Default Value: X **0x0: DISABLE:** Reset not used **0x1: ENABLE:** Reset enabled
4	PLD0_MC2_SET_SEL	Set select enable Default Value: X

(continued)

		0x0: DISABLE: Set not used **0x1: ENABLE:** Set enabled
3	PLD0_MC1_RESET_SEL	Reset select enable Default Value: X **0x0: DISABLE:** Reset not used **0x1: ENABLE:** Reset enabled
2	PLD0_MC1_SET_SEL	Set select enable Default Value: X **0x0: DISABLE:** Set not used **0x1: ENABLE:** Set enabled
1	PLD0_MC0_RESET_SEL	Reset select enable Default Value: X **0x0: DISABLE:** Reset not used **0x1: ENABLE:** Reset enabled
0	PLD0_MC0_SET_SEL	Set select enable Default Value: X **0x0: DISABLE:** Set not used **0x1: ENABLE:** Set enabled

36.1.80 UDB_P0_U1_PLD_MC_CFG_BYPASS

PLD Macro cell Bypass control

Address: 0x400F30BE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	NC7	PLD0_MC3_BYPASS	NC5	PLD0_MC2_BYPASS	NC3	PLD0_MC1_BYPASS	NC1	PLD0_MC0_BYPASS

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	NC15	PLD1_MC3_BYPASS	NC13	PLD1_MC2_BYPASS	NC11	PLD1_MC1_BYPASS	NC9	PLD1_MC0_BYPASS

Bits	Name	Description
15	NC15	Spare register bit Default Value: X
14	PLD1_MC3_BYPASS	Bypass selection Default Value: X **0x0: REGISTER:** Registered output **0x1: COMBINATIONAL:** Combinational output
13	NC13	Spare register bit Default Value: X
12	PLD1_MC2_BYPASS	Bypass selection Default Value: X **0x0: REGISTER:** Registered output **0x1: COMBINATIONAL:** Combinational output
11	NC11	Spare register bit Default Value: X
10	PLD1_MC1_BYPASS	Bypass selection Default Value: X **0x0: REGISTER:** Registered output **0x1: COMBINATIONAL:** Combinational output

(continued)

9	NC9	Spare register bit Default Value: X
8	PLD1_MC0_BYPASS	Bypass selection Default Value: X **0x0: REGISTER:** Registered output **0x1: COMBINATIONAL:** Combinational output
7	NC7	Spare register bit Default Value: X
6	PLD0_MC3_BYPASS	Bypass selection Default Value: X **0x0: REGISTER:** Registered output **0x1: COMBINATIONAL:** Combinational output
5	NC5	Spare register bit Default Value: X
4	PLD0_MC2_BYPASS	Bypass selection Default Value: X **0x0: REGISTER:** Registered output **0x1: COMBINATIONAL:** Combinational output
3	NC3	Spare register bit Default Value: X
2	PLD0_MC1_BYPASS	Bypass selection Default Value: X **0x0: REGISTER:** Registered output **0x1: COMBINATIONAL:** Combinational output
1	NC1	Spare register bit Default Value: X
0	PLD0_MC0_BYPASS	Bypass selection Default Value: X **0x0: REGISTER:** Registered output **0x1: COMBINATIONAL:** Combinational output

36.1.81 UDB_P0_U1_CFG0

Datapath Input Selection - RAD1 RAD0. Address bits 0 and 1 to the dynamic configuration RAM

Address: 0x400F30C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	RAD1 [6:4]			None	RAD0 [2:0]		

Bits	Name	Description
6 : 4	RAD1	Datapath Permutable Input Mux Default Value: 0 **0x0: OFF:** Input off **0x1: DP_IN0:** Set to dp_in[0] **0x2: DP_IN1:** Set to dp_in[1] **0x3: DP_IN2:** Set to dp_in[2] **0x4: DP_IN3:** Set to dp_in[3] **0x5: DP_IN4:** Set to dp_in[4] **0x6: DP_IN5:** Set to dp_in[5] **0x7: RESERVED:** Reserved
2 : 0	RAD0	Datapath Permutable Input Mux Default Value: 0 **0x0: OFF:** Input off **0x1: DP_IN0:** Set to dp_in[0] **0x2: DP_IN1:** Set to dp_in[1] **0x3: DP_IN2:** Set to dp_in[2] **0x4: DP_IN3:** Set to dp_in[3] **0x5: DP_IN4:** Set to dp_in[4]

(continued)

0x6: DP_IN5:
Set to dp_in[5]

0x7: RESERVED:
Reserved

36.1.82 UDB_P0_U1_CFG1

Datapath Input Selection - RAD2. Address bit 2 to the dynamic configuration RAM

Address: 0x400F30C1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW		
HW Access	R	R	R	R	R	R		
Name	DP_RTE_BYPASS4	DP_RTE_BYPASS3	DP_RTE_BYPASS2	DP_RTE_BYPASS1	DP_RTE_BYPASS0	RAD2 [2:0]		

Bits	Name	Description
7	DP_RTE_BYPASS4	DP_In bypass control Default Value: 0 **0x0: DP_IN4_ROUTE:** Use dp_in[4] **0x1: DP_IN4_BYPASS:** Use dp_out[4] as input via bypass
6	DP_RTE_BYPASS3	DP_In bypass control Default Value: 0 **0x0: DP_IN3_ROUTE:** Use dp_in[3] **0x1: DP_IN3_BYPASS:** Use dp_out[3] as input via bypass
5	DP_RTE_BYPASS2	DP_In bypass control Default Value: 0 **0x0: DP_IN2_ROUTE:** Use dp_in[2] **0x1: DP_IN2_BYPASS:** Use dp_out[2] as input via bypass
4	DP_RTE_BYPASS1	DP_In bypass control Default Value: 0 **0x0: DP_IN1_ROUTE:** Use dp_in[1] **0x1: DP_IN1_BYPASS:** Use dp_out[1] as input via bypass
3	DP_RTE_BYPASS0	DP_In bypass control Default Value: 0 **0x0: DP_IN0_ROUTE:** Use dp_in[0] **0x1: DP_IN0_BYPASS:** Use dp_out[0] as input via bypass

(continued)

2 : 0	RAD2	Datapath Permutable Input Mux Default Value: 0 **0x0: OFF:** Input off **0x1: DP_IN0:** Set to dp_in[0] **0x2: DP_IN1:** Set to dp_in[1] **0x3: DP_IN2:** Set to dp_in[2] **0x4: DP_IN3:** Set to dp_in[3] **0x5: DP_IN4:** Set to dp_in[4] **0x6: DP_IN5:** Set to dp_in[5] **0x7: RESERVED:** Reserved

36.1.83 UDB_P0_U1_CFG2

Datapath Input Selection - F1_LD, F0_LD.

Address: 0x400F30C2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW			RW	RW		
HW Access	R	R			R	R		
Name	NC7	F1_LD [6:4]			DP_RTE_BYPASS5	F0_LD [2:0]		

Bits	Name	Description
7	NC7	Spare register bit Default Value: 0
6 : 4	F1_LD	Datapath Permutable Input Mux Default Value: 0 **0x0: OFF:** Input off **0x1: DP_IN0:** Set to dp_in[0] **0x2: DP_IN1:** Set to dp_in[1] **0x3: DP_IN2:** Set to dp_in[2] **0x4: DP_IN3:** Set to dp_in[3] **0x5: DP_IN4:** Set to dp_in[4] **0x6: DP_IN5:** Set to dp_in[5] **0x7: RESERVED:** Reserved
3	DP_RTE_BYPASS5	DP_In bypass control Default Value: 0 **0x0: DP_IN5_ROUTE:** Use dp_in[5] **0x1: DP_IN5_BYPASS:** Use dp_out[5] via bypass
2 : 0	F0_LD	Datapath Permutable Input Mux Default Value: 0 **0x0: OFF:** Input off

(continued)

0x1: DP_IN0:
Set to dp_in[0]

0x2: DP_IN1:
Set to dp_in[1]

0x3: DP_IN2:
Set to dp_in[2]

0x4: DP_IN3:
Set to dp_in[3]

0x5: DP_IN4:
Set to dp_in[4]

0x6: DP_IN5:
Set to dp_in[5]

0x7: RESERVED:
Reserved

36.1.84 UDB_P0_U1_CFG3

Datapath Input Selection - D1_LD, D0_LD.

Address: 0x400F30C3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	D1_LD [6:4]			None	D0_LD [2:0]		

Bits	Name	Description
6 : 4	D1_LD	Datapath Permutable Input Mux Default Value: 0 **0x0: OFF:** Input off **0x1: DP_IN0:** Set to dp_in[0] **0x2: DP_IN1:** Set to dp_in[1] **0x3: DP_IN2:** Set to dp_in[2] **0x4: DP_IN3:** Set to dp_in[3] **0x5: DP_IN4:** Set to dp_in[4] **0x6: DP_IN5:** Set to dp_in[5] **0x7: RESERVED:** Reserved
2 : 0	D0_LD	Datapath Permutable Input Mux Default Value: 0 **0x0: OFF:** Input off **0x1: DP_IN0:** Set to dp_in[0] **0x2: DP_IN1:** Set to dp_in[1] **0x3: DP_IN2:** Set to dp_in[2] **0x4: DP_IN3:** Set to dp_in[3] **0x5: DP_IN4:** Set to dp_in[4]

(continued)

0x6: DP_IN5:
Set to dp_in[5]

0x7: RESERVED:
Reserved

36.1.85 UDB_P0_U1_CFG4

Datapath Input Selection - CI_MUX SI_MUX.

Address: 0x400F30C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	CI_MUX [6:4]			None	SI_MUX [2:0]		

Bits	Name	Description
6 : 4	CI_MUX	Datapath Permutable Input Mux Default Value: 0 **0x0: OFF:** Input off **0x1: DP_IN0:** Set to dp_in[0] **0x2: DP_IN1:** Set to dp_in[1] **0x3: DP_IN2:** Set to dp_in[2] **0x4: DP_IN3:** Set to dp_in[3] **0x5: DP_IN4:** Set to dp_in[4] **0x6: DP_IN5:** Set to dp_in[5] **0x7: RESERVED:** Reserved
2 : 0	SI_MUX	Datapath Permutable Input Mux Default Value: 0 **0x0: OFF:** Input off **0x1: DP_IN0:** Set to dp_in[0] **0x2: DP_IN1:** Set to dp_in[1] **0x3: DP_IN2:** Set to dp_in[2] **0x4: DP_IN3:** Set to dp_in[3] **0x5: DP_IN4:** Set to dp_in[4]

(continued)

0x6: DP_IN5:
Set to dp_in[5]

0x7: RESERVED:
Reserved

36.1.86 UDB_P0_U1_CFG5

Datapath Output Selection for OUT1 OUT0

Address: 0x400F30C5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	OUT1 [7:4]				OUT0 [3:0]			

Bits	Name	Description
7 : 4	OUT1	Datapath Permutable Output Mux Default Value: 0 **0x0: CE0:** Comparator 0 equal **0x1: CL0:** Comparator 0 less than **0x2: Z0:** Accumulator 0 zero detect **0x3: FF0:** Accumulator 0 ones detect **0x4: CE1:** Comparator 1 equal **0x5: CL1:** Comparator 1 less than **0x6: Z1:** Accumulator 1 zero detect **0x7: FF1:** Accumulator 1 ones detect **0x8: OV_MSB:** Overflow of MSB **0x9: CO_MSB:** Carry out of MSB **0xa: CMSBO:** CRC MSB **0xb: SO:** Shift out **0xc: F0_BLK_STAT:** FIFO 0 block status defined by direction **0xd: F1_BLK_STAT:** FIFO 1 block status defined by direction **0xe: F0_BUS_STAT:** FIFO 0 bus status defined by direction and level

(continued)

		0xf: F1_BUS_STAT: FIFO 1 bus status defined by direction and level
3 : 0	OUT0	Datapath Permutable Output Mux Default Value: 0 **0x0: CE0:** Comparator 0 equal **0x1: CL0:** Comparator 0 less than **0x2: Z0:** Accumulator 0 zero detect **0x3: FF0:** Accumulator 0 ones detect **0x4: CE1:** Comparator 1 equal **0x5: CL1:** Comparator 1 less than **0x6: Z1:** Accumulator 1 zero detect **0x7: FF1:** Accumulator 1 ones detect **0x8: OV_MSB:** Overflow of MSB **0x9: CO_MSB:** Carry out of MSB **0xa: CMSBO:** CRC MSB **0xb: SO:** Shift out **0xc: F0_BLK_STAT:** FIFO 0 block status defined by direction **0xd: F1_BLK_STAT:** FIFO 1 block status defined by direction **0xe: F0_BUS_STAT:** FIFO 0 bus status defined by direction and level **0xf: F1_BUS_STAT:** FIFO 1 bus status defined by direction and level

36.1.87 UDB_P0_U1_CFG6

Datapath Output Selection for OUT3 OUT2

Address: 0x400F30C6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	OUT3 [7:4]				OUT2 [3:0]			

Bits	Name	Description
7 : 4	OUT3	Datapath Permutable Output Mux Default Value: 0 **0x0: CE0:** Comparator 0 equal **0x1: CL0:** Comparator 0 less than **0x2: Z0:** Accumulator 0 zero detect **0x3: FF0:** Accumulator 0 ones detect **0x4: CE1:** Comparator 1 equal **0x5: CL1:** Comparator 1 less than **0x6: Z1:** Accumulator 1 zero detect **0x7: FF1:** Accumulator 1 ones detect **0x8: OV_MSB:** Overflow of MSB **0x9: CO_MSB:** Carry out of MSB **0xa: CMSBO:** CRC MSB **0xb: SO:** Shift out **0xc: F0_BLK_STAT:** FIFO 0 block status defined by direction **0xd: F1_BLK_STAT:** FIFO 1 block status defined by direction **0xe: F0_BUS_STAT:** FIFO 0 bus status defined by direction and level

(continued)

		0xf: F1_BUS_STAT: FIFO 1 bus status defined by direction and level
3 : 0	OUT2	Datapath Permutable Output Mux Default Value: 0 **0x0: CE0:** Comparator 0 equal **0x1: CL0:** Comparator 0 less than **0x2: Z0:** Accumulator 0 zero detect **0x3: FF0:** Accumulator 0 ones detect **0x4: CE1:** Comparator 1 equal **0x5: CL1:** Comparator 1 less than **0x6: Z1:** Accumulator 1 zero detect **0x7: FF1:** Accumulator 1 ones detect **0x8: OV_MSB:** Overflow of MSB **0x9: CO_MSB:** Carry out of MSB **0xa: CMSBO:** CRC MSB **0xb: SO:** Shift out **0xc: F0_BLK_STAT:** FIFO 0 block status defined by direction **0xd: F1_BLK_STAT:** FIFO 1 block status defined by direction **0xe: F0_BUS_STAT:** FIFO 0 bus status defined by direction and level **0xf: F1_BUS_STAT:** FIFO 1 bus status defined by direction and level

36.1.88 UDB_P0_U1_CFG7

Datapath Output Selection for OUT5 OUT4

Address: 0x400F30C7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	OUT5 [7:4]				OUT4 [3:0]			

Bits	Name	Description
7 : 4	OUT5	Datapath Permutable Output Mux Default Value: 0 **0x0: CE0:** Comparator 0 equal **0x1: CL0:** Comparator 0 less than **0x2: Z0:** Accumulator 0 zero detect **0x3: FF0:** Accumulator 0 ones detect **0x4: CE1:** Comparator 1 equal **0x5: CL1:** Comparator 1 less than **0x6: Z1:** Accumulator 1 zero detect **0x7: FF1:** Accumulator 1 ones detect **0x8: OV_MSB:** Overflow of MSB **0x9: CO_MSB:** Carry out of MSB **0xa: CMSBO:** CRC MSB **0xb: SO:** Shift out **0xc: F0_BLK_STAT:** FIFO 0 block status defined by direction **0xd: F1_BLK_STAT:** FIFO 1 block status defined by direction **0xe: F0_BUS_STAT:** FIFO 0 bus status defined by direction and level

(continued)

		0xf: F1_BUS_STAT: FIFO 1 bus status defined by direction and level
3 : 0	OUT4	Datapath Permutable Output Mux Default Value: 0 **0x0: CE0:** Comparator 0 equal **0x1: CL0:** Comparator 0 less than **0x2: Z0:** Accumulator 0 zero detect **0x3: FF0:** Accumulator 0 ones detect **0x4: CE1:** Comparator 1 equal **0x5: CL1:** Comparator 1 less than **0x6: Z1:** Accumulator 1 zero detect **0x7: FF1:** Accumulator 1 ones detect **0x8: OV_MSB:** Overflow of MSB **0x9: CO_MSB:** Carry out of MSB **0xa: CMSBO:** CRC MSB **0xb: SO:** Shift out **0xc: F0_BLK_STAT:** FIFO 0 block status defined by direction **0xd: F1_BLK_STAT:** FIFO 1 block status defined by direction **0xe: F0_BUS_STAT:** FIFO 0 bus status defined by direction and level **0xf: F1_BUS_STAT:** FIFO 1 bus status defined by direction and level

36.1.89 UDB_P0_U1_CFG8

Datapath Output Synchronization Option

Address: 0x400F30C8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW					
HW Access	R	R	R					
Name	NC7	NC6	OUT_SYNC [5:0]					

Bits	Name	Description
7	NC7	Spare register bit Default Value: 0
6	NC6	Spare register bit Default Value: 0
5 : 0	OUT_SYNC	Datapath Output Synchronization. Each datapath output can be registered (default,0), or combinational (1) Default Value: 0 **0x0: REGISTERED:** registered **0x1: COMBINATIONAL:** combinational

36.1.90 UDB_P0_U1_CFG9

Datapath ALU Mask

Address: 0x400F30C9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	AMASK [7:0]							

Bits	Name	Description
7 : 0	AMASK	Datapath ALU Mask. The mask value in this register is applied to the output of the Datapath ALU result before the result is stored. The AMASK_EN bit (CFG12) must be set for the mask to be operational. Default Value: 0

36.1.91 UDB_P0_U1_CFG10

Datapath Compare 0 Mask

Address: 0x400F30CA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CMASK0 [7:0]							

Bits	Name	Description
7 : 0	CMASK0	Datapath Compare 0 Mask. The mask value in this register is applied to the output of the Accumulator 0 before it is used for comparison in Compare block 0. The CMASK0_EN bit (CFG12) must be set for the mask to be operational. Default Value: 0

36.1.92 UDB_P0_U1_CFG11

Datapath Compare 1 Mask

Address: 0x400F30CB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CMASK0 [7:0]							

Bits	Name	Description
7 : 0	CMASK0	Datapath Compare 1 Mask. The mask value in this register is applied to the selected Compare 1 block input (Accumulator 0 or Accumulator 1) before it is used for comparison. The CMASK1_EN bit (CFG12) must be set for the mask to be operational. Default Value: 0

36.1.93 UDB_P0_U1_CFG12

Datapath mask enables and shift in configuration

Address: 0x400F30CC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW		RW	
HW Access	R	R	R	R	R		R	
Name	CMASK1_EN	CMASK0_EN	AMASK_EN	DEF_SI	SI_SELB [3:2]		SI_SELA [1:0]	

Bits	Name	Description
7	CMASK1_EN	Datapath mask enable Default Value: 0 **0x0: DISABLE:** Masking disabled **0x1: ENABLE:** Masking enabled
6	CMASK0_EN	Datapath mask enable Default Value: 0 **0x0: DISABLE:** Masking disabled **0x1: ENABLE:** Masking enabled
5	AMASK_EN	Datapath mask enable Default Value: 0 **0x0: DISABLE:** Masking disabled **0x1: ENABLE:** Masking enabled
4	DEF_SI	Datapath default shift value Default Value: 0 **0x0: DEFAULT_0:** Default shift is 0 **0x1: DEFAULT_1:** Default shift is 1
3 : 2	SI_SELB	Datapath shift in source select Default Value: 0 **0x0: DEFAULT:** Default value specified in default shift field **0x1: REGISTERED:** Shift in is the shift out registered from previous cycle

(continued)

		0x2: ROUTE: Shift in is selected from datapath routing input **0x3: CHAIN:** Shift in is chained from the previous datapath
1 : 0	SI_SELA	Datapath shift in source select Default Value: 0 **0x0: DEFAULT:** Default value specified in default shift field **0x1: REGISTERED:** Shift in is the shift out registered from previous cycle **0x2: ROUTE:** Shift in is selected from datapath routing input **0x3: CHAIN:** Shift in is chained from the previous datapath

36.1.94 UDB_P0_U1_CFG13

Datapath carry in and compare configuration

Address: 0x400F30CD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	CMP_SELB [7:6]		CMP_SELA [5:4]		CI_SELB [3:2]		CI_SELA [1:0]	

Bits	Name	Description
7 : 6	CMP_SELB	Datapath compare select Default Value: 0 **0x0: A1_D1:** Compare A1 to D1 **0x1: A1_A0:** Compare A1 to A0 **0x2: A0_D1:** Compare A0 to D1 **0x3: A0_A0:** Compare A0 to A0
5 : 4	CMP_SELA	Datapath compare select Default Value: 0 **0x0: A1_D1:** Compare A1 to D1 **0x1: A1_A0:** Compare A1 to A0 **0x2: A0_D1:** Compare A0 to D1 **0x3: A0_A0:** Compare A0 to A0
3 : 2	CI_SELB	Datapath carry in source select Default Value: 0 **0x0: DEFAULT:** Default arithmetic mode **0x1: REGISTERED:** Carry in is the carry out registered from previous cycle **0x2: ROUTE:** Carry in is selected from datapath routing input **0x3: CHAIN:** Carry in is chained from the previous datapath
1 : 0	CI_SELA	Datapath carry in source select Default Value: 0

(continued)

0x0: DEFAULT:
Default arithmetic mode

0x1: REGISTERED:
Carry in is the carry out registered from previous cycle

0x2: ROUTE:
Carry in is selected from datapath routing input

0x3: CHAIN:
Carry in is chained from the previous datapath

36.1.95 UDB_P0_U1_CFG14

Datapath chaining and MSB configuration

Address: 0x400F30CE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW			RW	RW	RW	RW
HW Access	R	R			R	R	R	R
Name	MSB_EN	MSB_SEL [6:4]			CHAIN_CMSB	CHAIN_FB	CHAIN1	CHAIN0

Bits	Name	Description
7	MSB_EN	Datapath MSB selection enable Default Value: 0 **0x0: DISABLE:** MSB selection is disabled, MSB is bit 7 **0x1: ENABLE:** MSB selection is controlled by MSB_SEL
6 : 4	MSB_SEL	Datapath MSB Selection Default Value: 0 **0x0: BIT0:** MSB is bit 0 **0x1: BIT1:** MSB is bit 1 **0x2: BIT2:** MSB is bit 2 **0x3: BIT3:** MSB is bit 3 **0x4: BIT4:** MSB is bit 4 **0x5: BIT5:** MSB is bit 5 **0x6: BIT6:** MSB is bit 6 **0x7: BIT7:** MSB is bit 7 - equivalent to MSB_EN=0
3	CHAIN_CMSB	Datapath CRC MSB chaining enable Default Value: 0 **0x0: DISABLE:** CRC MSB is not chained **0x1: ENABLE:** CRC MSB is chained from the next (MSB) datapath

(continued)

2	CHAIN_FB	Datapath CRC feedback chaining enable Default Value: 0 **0x0: DISABLE:** CRC feedback is not chained **0x1: ENABLE:** CRC feedback is chained from the previous (LSB) datapath
1	CHAIN1	Datapath condition chaining enable Default Value: 0 **0x0: DISABLE:** Conditions are not chained **0x1: ENABLE:** Conditions are chained from the previous (LSB) datapath
0	CHAIN0	Datapath condition chaining enable Default Value: 0 **0x0: DISABLE:** Conditions are not chained **0x1: ENABLE:** Conditions are chained from the previous (LSB) datapath

36.1.96 UDB_P0_U1_CFG15

Datapath FIFO, shift and parallel input control

Address: 0x400F30CF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW		RW	
HW Access	R	R	R	R	R		R	
Name	PI_SEL	SHIFT_SEL	PI_DYN	MSB_SI	F1_INSEL [3:2]		F0_INSEL [1:0]	

Bits	Name	Description
7	PI_SEL	Datapath parallel input selection Default Value: 0 **0x0: NORMAL:** Normal operation, ALU source is from accumulator selection **0x1: PARALLEL:** ALU source A input is from the parallel data input
6	SHIFT_SEL	Datapath shift out selection Default Value: 0 **0x0: SOL_MSB:** Routed shift out is shift out left (sol_msb) **0x1: SOR:** Routed shift out is shift out right (sor)
5	PI_DYN	Enable for dynamic control of parallel data input (PI) mux. Default Value: 0 **0x0: DISABLE:** Parallel input mux select is only controlled by static configuration (PI_SEL). **0x1: ENABLE:** Parallel input mux to the Datapath is controlled by CFB_EN field in Datapath Dynamic RAM. When this mode is enabled, the CFB_EN usage for CRC/PRS functionality is disabled.
4	MSB_SI	Arithmetic shift right operation shift in selection Default Value: 0 **0x0: DEFAULT:** Shift in default value (when SI_SELA and/or SI_SELB == 0) **0x1: MSB:** Override default and shift in MSB value
3 : 2	F1_INSEL	Datapath FIFO Configuration Default Value: 0 **0x0: INPUT:** Input Mode: Write source is the system bus; read destination is corresponding data register or accumulator **0x1: OUTPUT_A0:** Output Mode: Write source is A0, read destination is the system bus

(continued)

		0x2: OUTPUT_A1: Output Mode: Write source is A1, read destination is the system bus **0x3: OUTPUT_ALU:** Output Mode: Write source is the ALU output, read destination is the system bus
1 : 0	F0_INSEL	Datapath FIFO Configuration Default Value: 0 **0x0: INPUT:** Input Mode: Write source is the system bus; read destination is corresponding data register or accumulator **0x1: OUTPUT_A0:** Output Mode: Write source is A0, read destination is the system bus **0x2: OUTPUT_A1:** Output Mode: Write source is A1, read destination is the system bus **0x3: OUTPUT_ALU:** Output Mode: Write source is the ALU output, read destination is the system bus

36.1.97 UDB_P0_U1_CFG16

Datapath FIFO and register access configuration control

Address: 0x400F30D0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	F1_CK_INV	F0_CK_INV	FIFO_FAST	FIFO_CAP	FIFO_EDGE	FIFO_ASYNC	EXT_CRCPRS	WRK16_CONCAT

Bits	Name	Description
7	F1_CK_INV	FIFO Clock Invert. When this bit is set, the polarity of the clock for the given FIFO will be inverted, with respect to the polarity of the selected Datapath clock. Default Value: 0 **0x0: NORMAL:** FIFO clock is the same polarity as the Datapath clock. **0x1: INVERT:** FIFO clock is inverted with respect to the Datapath clock.
6	F0_CK_INV	FIFO Clock Invert. When this bit is set, the polarity of the clock for the given FIFO will be inverted, with respect to the polarity of the selected Datapath clock. Default Value: 0 **0x0: NORMAL:** FIFO clock is the same polarity as the Datapath clock. **0x1: INVERT:** FIFO clock is inverted with respect to the Datapath clock.
5	FIFO_FAST	FIFO Fast Mode. When this bit is set, the FIFO write logic is clocked by the application bus clock. Lowers the latency of capture timing, at the expense of additional power. Default Value: 0 **0x0: DISABLE:** FIFO is clocked with selected Datapath clock. **0x1: ENABLE:** FIFO is clocked with application bus clock. Master and quadrant bus clock gating must be enabled.
4	FIFO_CAP	FIFO Software Capture Mode. When this bit is set, a read of A0 or A1 triggers a capture into F0 or F1 respectively. This function follows the chaining configuration. All accumulators in the chain from a given block to the MS block in the chain are capture Default Value: 0 **0x0: DISABLE:** FIFO capture is disabled. **0x1: ENABLE:** FIFO capture is enabled (FIFO must be in output mode). A read of A0 or A1 will write into F0 or F1.
3	FIFO_EDGE	Edge/level sensitive FIFO write control (Fx_LD). Only applies to FIFO configured in output mode Default Value: 0

(continued)

		0x0: LEVEL: FIFO write from accumulators/ALU is level sensitive. FIFO write occurs on a clock edge whenever the write control is sampled high on that edge. **0x1: EDGE:** FIFO write from accumulators/ALU is edge sensitive. FIFO write occurs on a clock edge folloing a 0 to 1 transition on the write control. The write control must be negated for at least one full cycle of the FIFO clock for a subsequent transition to be dete
2	FIFO_ASYNC	Asynchronous FIFO clocking support Default Value: 0 **0x0: DISABLE:** FIFO clocks are synchronous **0x1: ENABLE:** FIFO clocks are asynchronous
1	EXT_CRCPRS	External CRC/PRS mode Default Value: 0 **0x0: INTERNAL:** Internal CRC/PRS routing **0x1: EXTERNAL:** External CRC/PRS routing
0	WRK16_CONCAT	Datapath register access mode Default Value: 0 **0x0: DEFAULT:** 16-bit default access mode: selects registers in two consecutive UDBs in chaining order **0x1: CONCATENATE:** 16-bit concat access mode: selects concatenated registers in a single UDB

36.1.98 UDB_P0_U1_CFG17

Datapath FIFO control

Address: 0x400F30D1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [7:5]			FIFO_ADD_SYNC	NC3	NC2	F1_DYN	F0_DYN

Bits	Name	Description
4	FIFO_ADD_SYNC	Adds an additional sync flip-flop to FIFO block status. Default Value: 0 **0x0: DISABLE:** Compatible Mode: FIFO block status sync configuration is 'none' (FIFO_ASYNC = 0) and 1 sync flip-flop (FIFO_ASYNC = 1) **0x1: ENABLE:** Add Sync Mode: FIFO block status sync configuration 1 sync flip-flop (FIFO_ASYNC = 0) and 2 sync flip-flops (FIFO_ASYNC = 1)
3	NC3	Spare register bit Default Value: 0
2	NC2	Spare register bit Default Value: 0
1	F1_DYN	Default Value: 0 **0x0: STATIC:** Default. FIFO direction is static and controlled by the associated Fx_INSEL bits (CFG15). **0x1: DYNAMIC:** The associated FIFO direction is dynamically controlled by the associated 'dx_load' Datapath input signal. When the 'dx_load' signal is '0', the access is internal, where the FIFO is both a source for the Datapath, and a destination for the Datapath (dest
0	F0_DYN	When this bit is set, the associated FIFO configuration may be dynamically controlled. Default Value: 0 **0x0: STATIC:** Default. FIFO direction is static and controlled by the associated Fx_INSEL bits (CFG15). **0x1: DYNAMIC:** The associated FIFO direction is dynamically controlled by the associated 'dx_load' Datapath input signal. When the 'dx_load' signal is '0', the access is internal, where the FIFO is both a source for the Datapath, and a destination for the Datapath (dest

36.1.99 UDB_P0_U1_CFG18

Control Register Mode 0 (used in conjunction with Control Register Mode 1)

Address: 0x400F30D2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CTL_MD0 [7:0]							

Bits	Name	Description
7 : 0	CTL_MD0	CTL_MD1 and CTL_MD0 are concatenated to form an encoding for the mode of each control bit in the control register. Default Value: 0 **0x0: DIRECT:** The value written to that bit drives directly into the routing. **0x1: SYNC:** The value written is resampled by the selected SC clock. The resampled value is driven into the routing. **0x2: DOUBLE_SYNC:** The value written is doubly synced by the selected SC clock. The synched value is driven into the routing. **0x3: PULSE:** The value written is resampled and a synchronous pulse is generated and driven into the routing based on the selected SC clock. At the end of the generated pulse, the control register bit is automatically reset.

36.1.100 UDB_P0_U1_CFG19

Control Register Mode 1 (used in conjunction with Control Register Mode 0)

Address: 0x400F30D3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CTL_MD1 [7:0]							

Bits	Name	Description
7 : 0	CTL_MD1	CTL_MD1 and CTL_MD0 are concatenated to form an encoding for the mode of each control bit in the control register. Default Value: 0 **0x0: DIRECT:** The value written to that bit drives directly into the routing. **0x1: SYNC:** The value written is resampled by the selected SC clock. The resampled value is driven into the routing. **0x2: DOUBLE_SYNC:** The value written is doubly synced by the selected SC clock. The synched value is driven into the routing. **0x3: PULSE:** The value written is resampled and a synchronous pulse is generated and driven into the routing based on the selected SC clock. At the end of the generated pulse, the control register bit is automatically reset.

36.1.101 UDB_P0_U1_CFG20

Status Register input mode selection

Address: 0x400F30D4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	STAT_MD [7:0]							

Bits	Name	Description
7 : 0	STAT_MD	Mode selection for each bit of the status register. A '0' is transparent mode, where internal routing is read idrectly by CPU firmware. A '1' is sticky-clear-on-read mode, where once the given bit is set, it will stay set until the CPU reads the bit. Default Value: 0

36.1.102 UDB_P0_U1_CFG21

Spare register bits

Address: 0x400F30D5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						NC1	NC0

Bits	Name	Description
1	NC1	Spare register bit Default Value: 0
0	NC0	Spare register bit Default Value: 0

36.1.103 UDB_P0_U1_CFG22

SC block configuration control

Address: 0x400F30D6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW	RW	RW	
HW Access	None			R	R	R	R	
Name	None [7:5]			SC_EXT_RES	SC_SYNC_MD	SC_INT_MD	SC_OUT_CTL [1:0]	

Bits	Name	Description
4	SC_EXT_RES	Control register external reset operation. This bit supports autonomous usage of the control register, where a routed reset should clear the writable input registers. By default this is off because the CPU writable register can be cleared in firmware. Default Value: 0 **0x0: DISABLED:** When a routed reset is applied to the control register, only embedded state (sampling registers) are cleared **0x1: ENABLED:** When a routed reset is applied to the control register, all state is cleared, including the CPU writable control bits.
3	SC_SYNC_MD	SC Sync Mode - controls when the status register operates as a 4-bit double synchronizer module Default Value: 0 **0x0: NORMAL:** Normal Mode - Status register operation **0x1: SYNC_MODE:** Sync Mode - Routing inputs sc_in[3:0] are the 4 sync inputs, and connections sc_io[3:0] operate as the sync outputs
2	SC_INT_MD	SC Interrupt Mode - controls when the UDB driving an interrupt generated from the masked OR reduction of status bits 6 to 0 Default Value: 0 **0x0: NORMAL:** Normal Mode - Routing connection sc_io[3] is a normal input to the status register **0x1: INT_MODE:** Interrupt Mode - Routing connection sc_io[3] operates as the UDB interrupt output
1 : 0	SC_OUT_CTL	Selects the output source for the Status and Control routing connections Default Value: 0 **0x0: CONTROL:** Control out, 8-bits of control are driven to the routing connections **0x1: PARALLEL:** Datapath parallel output, 8-bits of datapath parallel output data are driven to the routing connections

(continued)

0x2: COUNTER:
Counter out, 7-bits of count and 1 bit (MSB) of terminal count are driven to the routing connections

0x3: RESERVED:
Reserved

36.1.104 UDB_P0_U1_CFG23

Counter Control

Address: 0x400F30D7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	RW	RW	RW		RW	
HW Access	None	R	R	R	R		R	
Name	None	ALT_CNT	ROUTE_EN	ROUTE_LD	CNT_EN_SEL [3:2]		CNT_LD_SEL [1:0]	

Bits	Name	Description
6	ALT_CNT	Configure the alternate operating mode of the counter Default Value: 0 **0x0: DEFAULT_MODE:** Default counter operating mode **0x1: ALT_MODE:** Alternate counter operating mode
5	ROUTE_EN	Configure the counter enable signal for routing input Default Value: 0 **0x0: DISABLE:** Routed EN signal is not used. EN signal is only controlled by firmware CNT START (ACTL register) **0x1: ROUTED:** Routed EN signal is used, CNT START must be set
4	ROUTE_LD	Configure the counter load signal for routing input Default Value: 0 **0x0: DISABLE:** Routed LD signal is not used **0x1: ROUTED:** Routed LD signal is used
3 : 2	CNT_EN_SEL	Selects the routing inputs for the counter enable signal Default Value: 0 **0x0: SC_IN4:** sc_io_in[0] **0x1: SC_IN5:** sc_io_in[1] **0x2: SC_IN6:** sc_io_in[2] **0x3: SC_IO:** sc_io_in[3]
1 : 0	CNT_LD_SEL	Selects the routing inputs for the counter load signal Default Value: 0

(continued)

0x0: SC_IN0:
sc_in[0]

0x1: SC_IN1:
sc_in[1]

0x2: SC_IN2:
sc_in[2]

0x3: SC_IN3:
sc_in[3]

36.1.105 UDB_P0_U1_CFG24

PLD0 Clock and Reset control

Address: 0x400F30D8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW		RW	
HW Access	R	R	R	R	R		R	
Name	RC_RES_SEL1	RC_RES_SEL0_OR_FRES	RC_INV	RC_EN_INV	RC_EN_MODE [3:2]		RC_EN_SEL [1:0]	

Bits	Name	Description
7	RC_RES_SEL1	Configures the routed reset for the associated UDB component block. The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES = '0' - This bit is not used. When ALT RES = '1' - The bits {RC_SEL1,RC_SEL0_OR_FRES} select the RC routing for routed reset control according to the following: 00 : rc_in [0] 01 : rc_in [1] 10 : rc_in [2] 11 : rc_in [3] Default Value: 0
6	RC_RES_SEL0_OR_FRES	Configures the routed or firmware reset for the associated UDB component block. The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES = '0' - This bit is a firmware reset. When ALT RES = '1' - The bits {RC_SEL1,RC_SEL0_OR_FRES} select the RC routing for routed reset control according to the following: 00 : rc_in [0] 01 : rc_in [1] 10 : rc_in [2] 11 : rc_in [3] Default Value: 0
5	RC_INV	Optionally inverts the clock selection for the associated UDB component block. Default Value: 0 **0x0: NOINV:** Non-inverted **0x1: INVERT:** Inverted
4	RC_EN_INV	Optionally inverts the clock enable selection for the associated UDB component blocks. Default Value: 0 **0x0: NOINV:** Non-inverted **0x1: INVERT:** Inverted
3 : 2	RC_EN_MODE	Selects the operating mode for the clock to the associated UDB component block. Default Value: 0

(continued)

		0x0: OFF: Always off **0x1: ON:** Always on **0x2: POSEDGE:** Positive edge **0x3: LEVEL:** Level sensitive
1 : 0	RC_EN_SEL	Selects channel route for enable control to the associated UDB component block Default Value: 0 **0x0: RC_IN0:** rc_in[0] **0x1: RC_IN1:** rc_in[1] **0x2: RC_IN2:** rc_in[2] **0x3: RC_IN3:** rc_in[3]

36.1.106 UDB_P0_U1_CFG25

PLD1 Clock and Reset control

Address: 0x400F30D9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW		RW	
HW Access	R	R	R	R	R		R	
Name	RC_RES_SEL1	RC_RES_SEL0_OR_FRES	RC_INV	RC_EN_INV	RC_EN_MODE [3:2]		RC_EN_SEL [1:0]	

Bits	Name	Description
7	RC_RES_SEL1	Configures the routed reset for the associated UDB component block. The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES = '0' - This bit is not used. When ALT RES = '1' - The bits {RC_SEL1,RC_SEL0_OR_FRES} select the RC routing for routed reset control according to the following: 00 : rc_in [0] 01 : rc_in [1] 10 : rc_in [2] 11 : rc_in [3] Default Value: 0
6	RC_RES_SEL0_OR_FRES	Configures the routed or firmware reset for the associated UDB component block. The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES = '0' - This bit is a firmware reset. When ALT RES = '1' - The bits {RC_SEL1,RC_SEL0_OR_FRES} select the RC routing for routed reset control according to the following: 00 : rc_in [0] 01 : rc_in [1] 10 : rc_in [2] 11 : rc_in [3] Default Value: 0
5	RC_INV	Optionally inverts the clock selection for the associated UDB component block. Default Value: 0 **0x0: NOINV:** Non-inverted **0x1: INVERT:** Inverted
4	RC_EN_INV	Optionally inverts the clock enable selection for the associated UDB component blocks. Default Value: 0 **0x0: NOINV:** Non-inverted **0x1: INVERT:** Inverted
3 : 2	RC_EN_MODE	Selects the operating mode for the clock to the associated UDB component block. Default Value: 0

(continued)

		0x0: OFF: Always off **0x1: ON:** Always on **0x2: POSEDGE:** Positive edge **0x3: LEVEL:** Level sensitive
1 : 0	RC_EN_SEL	Selects channel route for enable control to the associated UDB component block Default Value: 0 **0x0: RC_IN0:** rc_in[0] **0x1: RC_IN1:** rc_in[1] **0x2: RC_IN2:** rc_in[2] **0x3: RC_IN3:** rc_in[3]

36.1.107 UDB_P0_U1_CFG26

Datapath Clock and Reset control

Address: 0x400F30DA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW		RW	
HW Access	R	R	R	R	R		R	
Name	RC_RES_SEL1	RC_RES_SEL0_OR_FRES	RC_INV	RC_EN_INV	RC_EN_MODE [3:2]		RC_EN_SEL [1:0]	

Bits	Name	Description
7	RC_RES_SEL1	Configures the routed reset for the associated UDB component block. The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES = '0' - This bit is not used. When ALT RES = '1' - The bits {RC_SEL1,RC_SEL0_OR_FRES} select the RC routing for routed reset control according to the following: 00 : rc_in [0] 01 : rc_in [1] 10 : rc_in [2] 11 : rc_in [3] Default Value: 0
6	RC_RES_SEL0_OR_FRES	Configures the routed or firmware reset for the associated UDB component block. The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES = '0' - This bit is a firmware reset. When ALT RES = '1' - The bits {RC_SEL1,RC_SEL0_OR_FRES} select the RC routing for routed reset control according to the following: 00 : rc_in [0] 01 : rc_in [1] 10 : rc_in [2] 11 : rc_in [3] Default Value: 0
5	RC_INV	Optionally inverts the clock selection for the associated UDB component block. Default Value: 0 **0x0: NOINV:** Non-inverted **0x1: INVERT:** Inverted
4	RC_EN_INV	Optionally inverts the clock enable selection for the associated UDB component blocks. Default Value: 0 **0x0: NOINV:** Non-inverted **0x1: INVERT:** Inverted
3 : 2	RC_EN_MODE	Selects the operating mode for the clock to the associated UDB component block. Default Value: 0

(continued)

		0x0: OFF: Always off **0x1: ON:** Always on **0x2: POSEDGE:** Positive edge **0x3: LEVEL:** Level sensitive
1 : 0	RC_EN_SEL	Selects channel route for enable control to the associated UDB component block Default Value: 0 **0x0: RC_IN0:** rc_in[0] **0x1: RC_IN1:** rc_in[1] **0x2: RC_IN2:** rc_in[2] **0x3: RC_IN3:** rc_in[3]

36.1.108 UDB_P0_U1_CFG27

Status/Control Clock and Reset control

Address: 0x400F30DB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW		RW	
HW Access	R	R	R	R	R		R	
Name	RC_RES_SEL1	RC_RES_SEL0_OR_FRES	RC_INV	RC_EN_INV	RC_EN_MODE [3:2]		RC_EN_SEL [1:0]	

Bits	Name	Description
7	RC_RES_SEL1	Configures the routed reset for the associated UDB component block. The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES = '0' - This bit is not used. When ALT RES = '1' - The bits {RC_SEL1,RC_SEL0_OR_FRES} select the RC routing for routed reset control according to the following: 00 : rc_in [0] 01 : rc_in [1] 10 : rc_in [2] 11 : rc_in [3] Default Value: 0
6	RC_RES_SEL0_OR_FRES	Configures the routed or firmware reset for the associated UDB component block. The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES = '0' - This bit is a firmware reset. When ALT RES = '1' - The bits {RC_SEL1,RC_SEL0_OR_FRES} select the RC routing for routed reset control according to the following: 00 : rc_in [0] 01 : rc_in [1] 10 : rc_in [2] 11 : rc_in [3] Default Value: 0
5	RC_INV	Optionally inverts the clock selection for the associated UDB component block. Default Value: 0 **0x0: NOINV:** Non-inverted **0x1: INVERT:** Inverted
4	RC_EN_INV	Optionally inverts the clock enable selection for the associated UDB component blocks. Default Value: 0 **0x0: NOINV:** Non-inverted **0x1: INVERT:** Inverted
3 : 2	RC_EN_MODE	Selects the operating mode for the clock to the associated UDB component block. Default Value: 0

(continued)

		0x0: OFF: Always off **0x1: ON:** Always on **0x2: POSEDGE:** Positive edge **0x3: LEVEL:** Level sensitive
1 : 0	RC_EN_SEL	Selects channel route for enable control to the associated UDB component block Default Value: 0 **0x0: RC_IN0:** rc_in[0] **0x1: RC_IN1:** rc_in[1] **0x2: RC_IN2:** rc_in[2] **0x3: RC_IN3:** rc_in[3]

36.1.109 UDB_P0_U1_CFG28

Clock Selection for PLD1 and PLD0

Address: 0x400F30DC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PLD1_CK_SEL [7:4]				PLD0_CK_SEL [3:0]			

Bits	Name	Description
7 : 4	PLD1_CK_SEL	Clock selection registers Default Value: 0 **0x0: GCLK0:** gclk[0] **0x1: GCLK1:** gclk[1] **0x2: GCLK2:** gclk[2] **0x3: GCLK3:** gclk[3] **0x4: GCLK4:** gclk[4] **0x5: GCLK5:** gclk[5] **0x6: GCLK6:** gclk[6] **0x7: GCLK7:** gclk[7] **0x8: EXT_CLK:** ext_clk **0x9: SYSCLK:** sysclk
3 : 0	PLD0_CK_SEL	Clock selection registers Default Value: 0 **0x0: GCLK0:** gclk[0] **0x1: GCLK1:** gclk[1] **0x2: GCLK2:** gclk[2] **0x3: GCLK3:** gclk[3]

(continued)

0x4: GCLK4:
gclk[4]

0x5: GCLK5:
gclk[5]

0x6: GCLK6:
gclk[6]

0x7: GCLK7:
gclk[7]

0x8: EXT_CLK:
ext_clk

0x9: SYSCLK:
sysclk

36.1.110 UDB_P0_U1_CFG29

Clock Selection for Datapath, Status and Control

Address: 0x400F30DD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	SC_CK_SEL [7:4]				DP_CK_SEL [3:0]			

Bits	Name	Description
7 : 4	SC_CK_SEL	Clock selection registers Default Value: 0 **0x0: GCLK0:** gclk[0] **0x1: GCLK1:** gclk[1] **0x2: GCLK2:** gclk[2] **0x3: GCLK3:** gclk[3] **0x4: GCLK4:** gclk[4] **0x5: GCLK5:** gclk[5] **0x6: GCLK6:** gclk[6] **0x7: GCLK7:** gclk[7] **0x8: EXT_CLK:** ext_clk **0x9: SYSCLK:** sysclk
3 : 0	DP_CK_SEL	Clock selection registers Default Value: 0 **0x0: GCLK0:** gclk[0] **0x1: GCLK1:** gclk[1] **0x2: GCLK2:** gclk[2] **0x3: GCLK3:** gclk[3]

(continued)

0x4: GCLK4:
gclk[4]

0x5: GCLK5:
gclk[5]

0x6: GCLK6:
gclk[6]

0x7: GCLK7:
gclk[7]

0x8: EXT_CLK:
ext_clk

0x9: SYSCLK:
sysclk

36.1.111 UDB_P0_U1_CFG30

Reset control

Address: 0x400F30DE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	None	RW	RW	RW	RW	
HW Access	R	R	None	R	R	R	R	
Name	SC_RES_POL	DP_RES_POL	None	GUDB_WR	EN_RES_CNTCTL	RES_POL	RES_SEL [1:0]	

Bits	Name	Description
7	SC_RES_POL	Only valid when ALT RES (CFG31) is '1'. This bit controls the polarity of the selected SC routed reset. Default Value: 0 **0x0: NOINV:** Routed reset to the Status and Control block is true polarity. **0x1: INVERT:** Routed reset to the Status and Control block is inverted polarity.
6	DP_RES_POL	Only valid when ALT RES (CFG31) is '1'. This bit controls the polarity of the selected Datapath routed reset. Default Value: 0 **0x0: NOINV:** Routed reset to the Datapath block is true polarity. **0x1: INVERT:** Routed reset to the Datapath block is inverted polarity.
4	GUDB_WR	Enable global write operation for the configuration and working registers in this UDB. When this bit is set, the UDB ID select decoding is bypassed. Default Value: 0 **0x0: DISABLE:** Global UDB configuration/working register write is disabled **0x1: ENABLE:** Global UDB configuration/working register write is enabled
3	EN_RES_CNTCTL	This bit gates the routed reset to the counter/control register. By default, the operation is compatible, i.e., it only applies to the counter. However, if the updated control regisiter modes are used (sync mode, pulse mode, or the ext res bit) then the routed reset applies to the control register also. Default Value: 0 **0x0: DISABLE:** Routed reset is not applied to counter/control register **0x1: ENABLE:** Routed reset is applied to the counter/control register

(continued)

2	RES_POL	The meaning of this bit depends on the value of the ALT RES bit in CFG31. When ALT RES is '0' (compatible mode), this bit sets the polarity of the routed reset. When ALT RES is '1', this bit is unused. Default Value: 0 **0x0: NEGATED:** Polarity of the routed reset is true. **0x1: ASSERTED:** Polarity of the routed reset is inverted.
1 : 0	RES_SEL	The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES is '0' (compatible mode), this 2 bit field selects the RC routing input for the compatible reset scheme. When the ALT RES bit is '1', these bits are not used. Default Value: 0 **0x0: RC_IN0:** rc_in[0] **0x1: RC_IN1:** rc_in[1] **0x2: RC_IN2:** rc_in[2] **0x3: RC_IN3:** rc_in[3]

36.1.112 UDB_P0_U1_CFG31

Reset control

Address: 0x400F30DF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW		RW	RW	RW	RW
HW Access	R	R	R		R	R	R	R
Name	PLD1_RES_POL	PLD0_RES_POL	EXT_CK_SEL [5:4]		EN_RES_DP	EN_RES_STAT	EXT_SYNC	ALT_RES

Bits	Name	Description
7	PLD1_RES_POL	Not connected. NOTE: There is only one routed reset available to both PLDs in the UDB. When ALT RES is '1', PLD0 RES SEL controls the polarity of the routed reset for both PLDs. Default Value: 0 **0x0: NOINV:** Not Used **0x1: INVERT:** Not Used
6	PLD0_RES_POL	The meaning of this bit depends on the value of ALT RES. When ALT RES (CFG31) is '1', this bit controls the polarity of the selected PLD0 routed reset. NOTE: There is only one routed reset available to both PLDs in the UDB. When ALT RES is '1', PLD0 RES SEL controls the polarity of the routed reset for both PLDs. Default Value: 0 **0x0: NOINV:** Routed reset to the PLD0/PLD1 block is true polarity. **0x1: INVERT:** Routed reset to the PLD0/PLD1 block is inverted polarity.
5 : 4	EXT_CK_SEL	External clock selection Default Value: 0 **0x0: RC_IN0:** rc_in[0] **0x1: RC_IN1:** rc_in[1] **0x2: RC_IN2:** rc_in[2] **0x3: RC_IN3:** rc_in[3]
3	EN_RES_DP	Only valid when ALT RES (CFG31) is '1'. This bit gates the routed reset to the Datapath block. Default Value: 0 **0x0: DISABLE:** Routed reset to the Datapath block is gated off. **0x1: ENABLE:** Routed reset to the Datapath block is on. ALT RES must be '1' and routed reset must be selected in CFG26

(continued)

2	EN_RES_STAT	Only valid when ALT RES (CFG31) is '1'. This bit gates the routed reset to the status register. Default Value: 0 **0x0: NEGATED:** Status register routed reset is gated off **0x1: ASSERTED:** Status register routed reset is on
1	EXT_SYNC	Enable synchronization of selected external clock Default Value: 0 **0x0: DISABLE:** Selected external clock input is not synchronized **0x1: ENABLE:** Selected external clock input is synchronized
0	ALT_RES	This bit toggles between two reset configurations. When this bit is '0', one routed reset is shared by all components in this UDB (compatible mode). When this bit is a 1, each block can select a unique routed reset from the available RC inputs. Default Value: 0 **0x0: COMPATIBLE:** All UDB blocks share a common routed reset. **0x1: ALTERNATE:** Each UDB component block can select and control its individual routed reset.

36.1.113 UDB_P0_U1_DCFG0

Dynamic Configuration RAM

Address: 0x400F30E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW	RW	RW	RW
HW Access	R		R		R	R	R	R
Name	A0_WR_SRC [7:6]		A1_WR_SRC [5:4]		CFB_EN	CI_SEL	SI_SEL	CMP_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW	RW		RW	
HW Access	R			R	R		R	
Name	FUNC [15:13]			SRC_A	SRC_B [11:10]		SHIFT [9:8]	

Bits	Name	Description
15 : 13	FUNC	Dynamic ALU function selection Default Value: X **0x0: PASS:** Pass **0x1: INC_A:** Increment source A **0x2: DEC_A:** Decrement source A **0x3: ADD:** Add **0x4: SUB:** Subtract **0x5: XOR:** Bitwise XOR **0x6: AND:** Bitwise AND **0x7: OR:** Bitwise OR
12	SRC_A	Dynamic ALU source A selection Default Value: X **0x0: A0:** Configuration A **0x1: A1:** Configuration B
11 : 10	SRC_B	Dynamic ALU source B selection Default Value: X

(continued)

		0x0: D0: ALU source B is D0 **0x1: D1:** ALU source B is D1 **0x2: A0:** ALU source B is A0 **0x3: A1:** ALU source B is A1
9 : 8	SHIFT	Dynamic shift selection Default Value: X **0x0: NOSHIFT:** No shift **0x1: LEFT:** Left Shift **0x2: RIGHT:** Right Shift **0x3: SWAP:** Nibble swap
7 : 6	A0_WR_SRC	Dynamic A0 write source selection Default Value: X **0x0: NOWRITE:** no value written to A0 **0x1: ALU:** ALU output written to A0 **0x2: D0:** D1 value written to A0 **0x3: F0:** F1 value written to A0
5 : 4	A1_WR_SRC	Dynamic A1 write source selection Default Value: X **0x0: NOWRITE:** no value written to A1 **0x1: ALU:** ALU output written to A1 **0x2: D1:** D1 value written to A1 **0x3: F1:** F1 value written to A1
3	CFB_EN	Dynamic CRC feedback selection Default Value: X **0x0: DISABLE:** CRC feedback disabled **0x1: ENABLE:** CRC feedback enabled

(continued)

2	CI_SEL	Dynamic carry in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
1	SI_SEL	Dynamic shift in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
0	CMP_SEL	Dynamic compare selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B

36.1.114 UDB_P0_U1_DCFG1

Dynamic Configuration RAM

Address: 0x400F30E2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW	RW	RW	RW
HW Access	R		R		R	R	R	R
Name	A0_WR_SRC [7:6]		A1_WR_SRC [5:4]		CFB_EN	CI_SEL	SI_SEL	CMP_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW	RW		RW	
HW Access	R			R	R		R	
Name	FUNC [15:13]			SRC_A	SRC_B [11:10]		SHIFT [9:8]	

Bits	Name	Description
15 : 13	FUNC	Dynamic ALU function selection Default Value: X **0x0: PASS:** Pass **0x1: INC_A:** Increment source A **0x2: DEC_A:** Decrement source A **0x3: ADD:** Add **0x4: SUB:** Subtract **0x5: XOR:** Bitwise XOR **0x6: AND:** Bitwise AND **0x7: OR:** Bitwise OR
12	SRC_A	Dynamic ALU source A selection Default Value: X **0x0: A0:** Configuration A **0x1: A1:** Configuration B
11 : 10	SRC_B	Dynamic ALU source B selection Default Value: X

(continued)

		0x0: D0: ALU source B is D0 **0x1: D1:** ALU source B is D1 **0x2: A0:** ALU source B is A0 **0x3: A1:** ALU source B is A1
9 : 8	SHIFT	Dynamic shift selection Default Value: X **0x0: NOSHIFT:** No shift **0x1: LEFT:** Left Shift **0x2: RIGHT:** Right Shift **0x3: SWAP:** Nibble swap
7 : 6	A0_WR_SRC	Dynamic A0 write source selection Default Value: X **0x0: NOWRITE:** no value written to A0 **0x1: ALU:** ALU output written to A0 **0x2: D0:** D1 value written to A0 **0x3: F0:** F1 value written to A0
5 : 4	A1_WR_SRC	Dynamic A1 write source selection Default Value: X **0x0: NOWRITE:** no value written to A1 **0x1: ALU:** ALU output written to A1 **0x2: D1:** D1 value written to A1 **0x3: F1:** F1 value written to A1
3	CFB_EN	Dynamic CRC feedback selection Default Value: X **0x0: DISABLE:** CRC feedback disabled **0x1: ENABLE:** CRC feedback enabled

(continued)

2	CI_SEL	Dynamic carry in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
1	SI_SEL	Dynamic shift in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
0	CMP_SEL	Dynamic compare selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B

36.1.115 UDB_P0_U1_DCFG2

Dynamic Configuration RAM

Address: 0x400F30E4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW	RW	RW	RW
HW Access	R		R		R	R	R	R
Name	A0_WR_SRC [7:6]		A1_WR_SRC [5:4]		CFB_EN	CI_SEL	SI_SEL	CMP_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW	RW		RW	
HW Access	R			R	R		R	
Name	FUNC [15:13]			SRC_A	SRC_B [11:10]		SHIFT [9:8]	

Bits	Name	Description
15 : 13	FUNC	Dynamic ALU function selection Default Value: X **0x0: PASS:** Pass **0x1: INC_A:** Increment source A **0x2: DEC_A:** Decrement source A **0x3: ADD:** Add **0x4: SUB:** Subtract **0x5: XOR:** Bitwise XOR **0x6: AND:** Bitwise AND **0x7: OR:** Bitwise OR
12	SRC_A	Dynamic ALU source A selection Default Value: X **0x0: A0:** Configuration A **0x1: A1:** Configuration B
11 : 10	SRC_B	Dynamic ALU source B selection Default Value: X

(continued)

		0x0: D0: ALU source B is D0 **0x1: D1:** ALU source B is D1 **0x2: A0:** ALU source B is A0 **0x3: A1:** ALU source B is A1
9 : 8	SHIFT	Dynamic shift selection Default Value: X **0x0: NOSHIFT:** No shift **0x1: LEFT:** Left Shift **0x2: RIGHT:** Right Shift **0x3: SWAP:** Nibble swap
7 : 6	A0_WR_SRC	Dynamic A0 write source selection Default Value: X **0x0: NOWRITE:** no value written to A0 **0x1: ALU:** ALU output written to A0 **0x2: D0:** D1 value written to A0 **0x3: F0:** F1 value written to A0
5 : 4	A1_WR_SRC	Dynamic A1 write source selection Default Value: X **0x0: NOWRITE:** no value written to A1 **0x1: ALU:** ALU output written to A1 **0x2: D1:** D1 value written to A1 **0x3: F1:** F1 value written to A1
3	CFB_EN	Dynamic CRC feedback selection Default Value: X **0x0: DISABLE:** CRC feedback disabled **0x1: ENABLE:** CRC feedback enabled

(continued)

2	CI_SEL	Dynamic carry in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
1	SI_SEL	Dynamic shift in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
0	CMP_SEL	Dynamic compare selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B

36.1.116 UDB_P0_U1_DCFG3

Dynamic Configuration RAM

Address: 0x400F30E6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW	RW	RW	RW
HW Access	R		R		R	R	R	R
Name	A0_WR_SRC [7:6]		A1_WR_SRC [5:4]		CFB_EN	CI_SEL	SI_SEL	CMP_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW	RW		RW	
HW Access	R			R	R		R	
Name	FUNC [15:13]			SRC_A	SRC_B [11:10]		SHIFT [9:8]	

Bits	Name	Description
15 : 13	FUNC	Dynamic ALU function selection Default Value: X **0x0: PASS:** Pass **0x1: INC_A:** Increment source A **0x2: DEC_A:** Decrement source A **0x3: ADD:** Add **0x4: SUB:** Subtract **0x5: XOR:** Bitwise XOR **0x6: AND:** Bitwise AND **0x7: OR:** Bitwise OR
12	SRC_A	Dynamic ALU source A selection Default Value: X **0x0: A0:** Configuration A **0x1: A1:** Configuration B
11 : 10	SRC_B	Dynamic ALU source B selection Default Value: X

(continued)

		0x0: D0: ALU source B is D0 **0x1: D1:** ALU source B is D1 **0x2: A0:** ALU source B is A0 **0x3: A1:** ALU source B is A1
9 : 8	SHIFT	Dynamic shift selection Default Value: X **0x0: NOSHIFT:** No shift **0x1: LEFT:** Left Shift **0x2: RIGHT:** Right Shift **0x3: SWAP:** Nibble swap
7 : 6	A0_WR_SRC	Dynamic A0 write source selection Default Value: X **0x0: NOWRITE:** no value written to A0 **0x1: ALU:** ALU output written to A0 **0x2: D0:** D1 value written to A0 **0x3: F0:** F1 value written to A0
5 : 4	A1_WR_SRC	Dynamic A1 write source selection Default Value: X **0x0: NOWRITE:** no value written to A1 **0x1: ALU:** ALU output written to A1 **0x2: D1:** D1 value written to A1 **0x3: F1:** F1 value written to A1
3	CFB_EN	Dynamic CRC feedback selection Default Value: X **0x0: DISABLE:** CRC feedback disabled **0x1: ENABLE:** CRC feedback enabled

(continued)

2	CI_SEL	Dynamic carry in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
1	SI_SEL	Dynamic shift in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
0	CMP_SEL	Dynamic compare selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B

36.1.117 UDB_P0_U1_DCFG4

Dynamic Configuration RAM

Address: 0x400F30E8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW	RW	RW	RW
HW Access	R		R		R	R	R	R
Name	A0_WR_SRC [7:6]		A1_WR_SRC [5:4]		CFB_EN	CI_SEL	SI_SEL	CMP_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW	RW		RW	
HW Access	R			R	R		R	
Name	FUNC [15:13]			SRC_A	SRC_B [11:10]		SHIFT [9:8]	

Bits	Name	Description
15 : 13	FUNC	Dynamic ALU function selection Default Value: X **0x0: PASS:** Pass **0x1: INC_A:** Increment source A **0x2: DEC_A:** Decrement source A **0x3: ADD:** Add **0x4: SUB:** Subtract **0x5: XOR:** Bitwise XOR **0x6: AND:** Bitwise AND **0x7: OR:** Bitwise OR
12	SRC_A	Dynamic ALU source A selection Default Value: X **0x0: A0:** Configuration A **0x1: A1:** Configuration B
11 : 10	SRC_B	Dynamic ALU source B selection Default Value: X

(continued)

		0x0: D0: ALU source B is D0 **0x1: D1:** ALU source B is D1 **0x2: A0:** ALU source B is A0 **0x3: A1:** ALU source B is A1
9 : 8	SHIFT	Dynamic shift selection Default Value: X **0x0: NOSHIFT:** No shift **0x1: LEFT:** Left Shift **0x2: RIGHT:** Right Shift **0x3: SWAP:** Nibble swap
7 : 6	A0_WR_SRC	Dynamic A0 write source selection Default Value: X **0x0: NOWRITE:** no value written to A0 **0x1: ALU:** ALU output written to A0 **0x2: D0:** D1 value written to A0 **0x3: F0:** F1 value written to A0
5 : 4	A1_WR_SRC	Dynamic A1 write source selection Default Value: X **0x0: NOWRITE:** no value written to A1 **0x1: ALU:** ALU output written to A1 **0x2: D1:** D1 value written to A1 **0x3: F1:** F1 value written to A1
3	CFB_EN	Dynamic CRC feedback selection Default Value: X **0x0: DISABLE:** CRC feedback disabled **0x1: ENABLE:** CRC feedback enabled

(continued)

2	CI_SEL	Dynamic carry in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
1	SI_SEL	Dynamic shift in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
0	CMP_SEL	Dynamic compare selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B

36.1.118 UDB_P0_U1_DCFG5

Dynamic Configuration RAM

Address: 0x400F30EA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW	RW	RW	RW
HW Access	R		R		R	R	R	R
Name	A0_WR_SRC [7:6]		A1_WR_SRC [5:4]		CFB_EN	CI_SEL	SI_SEL	CMP_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW	RW		RW	
HW Access	R			R	R		R	
Name	FUNC [15:13]			SRC_A	SRC_B [11:10]		SHIFT [9:8]	

Bits	Name	Description
15 : 13	FUNC	Dynamic ALU function selection Default Value: X **0x0: PASS:** Pass **0x1: INC_A:** Increment source A **0x2: DEC_A:** Decrement source A **0x3: ADD:** Add **0x4: SUB:** Subtract **0x5: XOR:** Bitwise XOR **0x6: AND:** Bitwise AND **0x7: OR:** Bitwise OR
12	SRC_A	Dynamic ALU source A selection Default Value: X **0x0: A0:** Configuration A **0x1: A1:** Configuration B
11 : 10	SRC_B	Dynamic ALU source B selection Default Value: X

(continued)

		0x0: D0: ALU source B is D0 **0x1: D1:** ALU source B is D1 **0x2: A0:** ALU source B is A0 **0x3: A1:** ALU source B is A1
9 : 8	SHIFT	Dynamic shift selection Default Value: X **0x0: NOSHIFT:** No shift **0x1: LEFT:** Left Shift **0x2: RIGHT:** Right Shift **0x3: SWAP:** Nibble swap
7 : 6	A0_WR_SRC	Dynamic A0 write source selection Default Value: X **0x0: NOWRITE:** no value written to A0 **0x1: ALU:** ALU output written to A0 **0x2: D0:** D1 value written to A0 **0x3: F0:** F1 value written to A0
5 : 4	A1_WR_SRC	Dynamic A1 write source selection Default Value: X **0x0: NOWRITE:** no value written to A1 **0x1: ALU:** ALU output written to A1 **0x2: D1:** D1 value written to A1 **0x3: F1:** F1 value written to A1
3	CFB_EN	Dynamic CRC feedback selection Default Value: X **0x0: DISABLE:** CRC feedback disabled **0x1: ENABLE:** CRC feedback enabled

(continued)

2	CI_SEL	Dynamic carry in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
1	SI_SEL	Dynamic shift in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
0	CMP_SEL	Dynamic compare selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B

36.1.119 UDB_P0_U1_DCFG6

Dynamic Configuration RAM

Address: 0x400F30EC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW	RW	RW	RW
HW Access	R		R		R	R	R	R
Name	A0_WR_SRC [7:6]		A1_WR_SRC [5:4]		CFB_EN	CI_SEL	SI_SEL	CMP_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW	RW		RW	
HW Access	R			R	R		R	
Name	FUNC [15:13]			SRC_A	SRC_B [11:10]		SHIFT [9:8]	

Bits	Name	Description
15 : 13	FUNC	Dynamic ALU function selection Default Value: X **0x0: PASS:** Pass **0x1: INC_A:** Increment source A **0x2: DEC_A:** Decrement source A **0x3: ADD:** Add **0x4: SUB:** Subtract **0x5: XOR:** Bitwise XOR **0x6: AND:** Bitwise AND **0x7: OR:** Bitwise OR
12	SRC_A	Dynamic ALU source A selection Default Value: X **0x0: A0:** Configuration A **0x1: A1:** Configuration B
11 : 10	SRC_B	Dynamic ALU source B selection Default Value: X

(continued)

		0x0: D0: ALU source B is D0 **0x1: D1:** ALU source B is D1 **0x2: A0:** ALU source B is A0 **0x3: A1:** ALU source B is A1
9 : 8	SHIFT	Dynamic shift selection Default Value: X **0x0: NOSHIFT:** No shift **0x1: LEFT:** Left Shift **0x2: RIGHT:** Right Shift **0x3: SWAP:** Nibble swap
7 : 6	A0_WR_SRC	Dynamic A0 write source selection Default Value: X **0x0: NOWRITE:** no value written to A0 **0x1: ALU:** ALU output written to A0 **0x2: D0:** D1 value written to A0 **0x3: F0:** F1 value written to A0
5 : 4	A1_WR_SRC	Dynamic A1 write source selection Default Value: X **0x0: NOWRITE:** no value written to A1 **0x1: ALU:** ALU output written to A1 **0x2: D1:** D1 value written to A1 **0x3: F1:** F1 value written to A1
3	CFB_EN	Dynamic CRC feedback selection Default Value: X **0x0: DISABLE:** CRC feedback disabled **0x1: ENABLE:** CRC feedback enabled

(continued)

2	CI_SEL	Dynamic carry in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
1	SI_SEL	Dynamic shift in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
0	CMP_SEL	Dynamic compare selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B

36.1.120 UDB_P0_U1_DCFG7

Dynamic Configuration RAM

Address: 0x400F30EE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW	RW	RW	RW
HW Access	R		R		R	R	R	R
Name	A0_WR_SRC [7:6]		A1_WR_SRC [5:4]		CFB_EN	CI_SEL	SI_SEL	CMP_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW	RW		RW	
HW Access	R			R	R		R	
Name	FUNC [15:13]			SRC_A	SRC_B [11:10]		SHIFT [9:8]	

Bits	Name	Description
15 : 13	FUNC	Dynamic ALU function selection Default Value: X **0x0: PASS:** Pass **0x1: INC_A:** Increment source A **0x2: DEC_A:** Decrement source A **0x3: ADD:** Add **0x4: SUB:** Subtract **0x5: XOR:** Bitwise XOR **0x6: AND:** Bitwise AND **0x7: OR:** Bitwise OR
12	SRC_A	Dynamic ALU source A selection Default Value: X **0x0: A0:** Configuration A **0x1: A1:** Configuration B
11 : 10	SRC_B	Dynamic ALU source B selection Default Value: X

(continued)

		0x0: D0: ALU source B is D0 **0x1: D1:** ALU source B is D1 **0x2: A0:** ALU source B is A0 **0x3: A1:** ALU source B is A1
9 : 8	SHIFT	Dynamic shift selection Default Value: X **0x0: NOSHIFT:** No shift **0x1: LEFT:** Left Shift **0x2: RIGHT:** Right Shift **0x3: SWAP:** Nibble swap
7 : 6	A0_WR_SRC	Dynamic A0 write source selection Default Value: X **0x0: NOWRITE:** no value written to A0 **0x1: ALU:** ALU output written to A0 **0x2: D0:** D1 value written to A0 **0x3: F0:** F1 value written to A0
5 : 4	A1_WR_SRC	Dynamic A1 write source selection Default Value: X **0x0: NOWRITE:** no value written to A1 **0x1: ALU:** ALU output written to A1 **0x2: D1:** D1 value written to A1 **0x3: F1:** F1 value written to A1
3	CFB_EN	Dynamic CRC feedback selection Default Value: X **0x0: DISABLE:** CRC feedback disabled **0x1: ENABLE:** CRC feedback enabled

(continued)

2	CI_SEL	Dynamic carry in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
1	SI_SEL	Dynamic shift in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
0	CMP_SEL	Dynamic compare selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B

36.1.121 UDB_P1_U0_PLD_IT0

PLD Input Terms

Address: 0x400F3200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Bits	Name	Description
31	PLD1_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X

(continued)

25	PLD1_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
22	PLD0_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X

(continued)

3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X

36.1.122 UDB_P1_U0_PLD_IT1

PLD Input Terms

Address: 0x400F3204

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Bits	Name	Description
31	PLD1_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X

(continued)

25	PLD1_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
22	PLD0_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X

(continued)

3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X

36.1.123 UDB_P1_U0_PLD_IT2

PLD Input Terms

Address: 0x400F3208

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Bits	Name	Description
31	PLD1_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X

(continued)

25	PLD1_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
22	PLD0_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X

(continued)

3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X

36.1.124 UDB_P1_U0_PLD_IT3

PLD Input Terms

Address: 0x400F320C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Bits	Name	Description
31	PLD1_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X

(continued)

25	PLD1_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
22	PLD0_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X

(continued)

3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X

36.1.125 UDB_P1_U0_PLD_IT4

PLD Input Terms

Address: 0x400F3210

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Bits	Name	Description
31	PLD1_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X

(continued)

25	PLD1_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
22	PLD0_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X

(continued)

3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X

36.1.126 UDB_P1_U0_PLD_IT5

PLD Input Terms

Address: 0x400F3214

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Bits	Name	Description
31	PLD1_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X

(continued)

25	PLD1_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
22	PLD0_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X

(continued)

3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X

36.1.127 UDB_P1_U0_PLD_IT6

PLD Input Terms

Address: 0x400F3218

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Bits	Name	Description
31	PLD1_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X

(continued)

25	PLD1_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
22	PLD0_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X

(continued)

3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X

36.1.128 UDB_P1_U0_PLD_IT7

PLD Input Terms

Address: 0x400F321C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Bits	Name	Description
31	PLD1_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X

(continued)

25	PLD1_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
22	PLD0_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X

(continued)

3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X

36.1.129 UDB_P1_U0_PLD_IT8

PLD Input Terms

Address: 0x400F3220

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Bits	Name	Description
31	PLD1_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X

(continued)

25	PLD1_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
22	PLD0_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X

(continued)

3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X

36.1.130 UDB_P1_U0_PLD_IT9

PLD Input Terms

Address: 0x400F3224

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Bits	Name	Description
31	PLD1_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X

(continued)

25	PLD1_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
22	PLD0_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X

(continued)

3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X

36.1.131 UDB_P1_U0_PLD_IT10

PLD Input Terms

Address: 0x400F3228

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Bits	Name	Description
31	PLD1_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X

(continued)

25	PLD1_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
22	PLD0_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X

(continued)

3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X

36.1.132 UDB_P1_U0_PLD_IT11

PLD Input Terms

Address: 0x400F322C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Bits	Name	Description
31	PLD1_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X

(continued)

25	PLD1_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
22	PLD0_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X

(continued)

3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X

36.1.133 UDB_P1_U0_PLD_ORT0

PLD OR Terms

Address: 0x400F3230

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ORT_PTx_7	PLD0_ORT_PTx_6	PLD0_ORT_PTx_5	PLD0_ORT_PTx_4	PLD0_ORT_PTx_3	PLD0_ORT_PTx_2	PLD0_ORT_PTx_1	PLD0_ORT_PTx_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ORT_PTx_7	PLD1_ORT_PTx_6	PLD1_ORT_PTx_5	PLD1_ORT_PTx_4	PLD1_ORT_PTx_3	PLD1_ORT_PTx_2	PLD1_ORT_PTx_1	PLD1_ORT_PTx_0

Bits	Name	Description
15	PLD1_ORT_PTx_7	OR term. Bit position corresponds to product term. Default Value: X
14	PLD1_ORT_PTx_6	OR term. Bit position corresponds to product term. Default Value: X
13	PLD1_ORT_PTx_5	OR term. Bit position corresponds to product term. Default Value: X
12	PLD1_ORT_PTx_4	OR term. Bit position corresponds to product term. Default Value: X
11	PLD1_ORT_PTx_3	OR term. Bit position corresponds to product term. Default Value: X
10	PLD1_ORT_PTx_2	OR term. Bit position corresponds to product term. Default Value: X
9	PLD1_ORT_PTx_1	OR term. Bit position corresponds to product term. Default Value: X
8	PLD1_ORT_PTx_0	OR term. Bit position corresponds to product term. Default Value: X
7	PLD0_ORT_PTx_7	OR term. Bit position corresponds to product term. Default Value: X
6	PLD0_ORT_PTx_6	OR term. Bit position corresponds to product term. Default Value: X
5	PLD0_ORT_PTx_5	OR term. Bit position corresponds to product term. Default Value: X
4	PLD0_ORT_PTx_4	OR term. Bit position corresponds to product term. Default Value: X

(continued)

3	PLD0_ORT_PTx_3	OR term. Bit position corresponds to product term. Default Value: X
2	PLD0_ORT_PTx_2	OR term. Bit position corresponds to product term. Default Value: X
1	PLD0_ORT_PTx_1	OR term. Bit position corresponds to product term. Default Value: X
0	PLD0_ORT_PTx_0	OR term. Bit position corresponds to product term. Default Value: X

36.1.134 UDB_P1_U0_PLD_ORT1

PLD OR Terms

Address: 0x400F3232

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ORT_PTx_7	PLD0_ORT_PTx_6	PLD0_ORT_PTx_5	PLD0_ORT_PTx_4	PLD0_ORT_PTx_3	PLD0_ORT_PTx_2	PLD0_ORT_PTx_1	PLD0_ORT_PTx_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ORT_PTx_7	PLD1_ORT_PTx_6	PLD1_ORT_PTx_5	PLD1_ORT_PTx_4	PLD1_ORT_PTx_3	PLD1_ORT_PTx_2	PLD1_ORT_PTx_1	PLD1_ORT_PTx_0

Bits	Name	Description
15	PLD1_ORT_PTx_7	OR term. Bit position corresponds to product term. Default Value: X
14	PLD1_ORT_PTx_6	OR term. Bit position corresponds to product term. Default Value: X
13	PLD1_ORT_PTx_5	OR term. Bit position corresponds to product term. Default Value: X
12	PLD1_ORT_PTx_4	OR term. Bit position corresponds to product term. Default Value: X
11	PLD1_ORT_PTx_3	OR term. Bit position corresponds to product term. Default Value: X
10	PLD1_ORT_PTx_2	OR term. Bit position corresponds to product term. Default Value: X
9	PLD1_ORT_PTx_1	OR term. Bit position corresponds to product term. Default Value: X
8	PLD1_ORT_PTx_0	OR term. Bit position corresponds to product term. Default Value: X
7	PLD0_ORT_PTx_7	OR term. Bit position corresponds to product term. Default Value: X
6	PLD0_ORT_PTx_6	OR term. Bit position corresponds to product term. Default Value: X
5	PLD0_ORT_PTx_5	OR term. Bit position corresponds to product term. Default Value: X
4	PLD0_ORT_PTx_4	OR term. Bit position corresponds to product term. Default Value: X

(continued)

3	PLD0_ORT_PTx_3	OR term. Bit position corresponds to product term. Default Value: X
2	PLD0_ORT_PTx_2	OR term. Bit position corresponds to product term. Default Value: X
1	PLD0_ORT_PTx_1	OR term. Bit position corresponds to product term. Default Value: X
0	PLD0_ORT_PTx_0	OR term. Bit position corresponds to product term. Default Value: X

36.1.135 UDB_P1_U0_PLD_ORT2

PLD OR Terms

Address: 0x400F3234

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ORT_PTx_7	PLD0_ORT_PTx_6	PLD0_ORT_PTx_5	PLD0_ORT_PTx_4	PLD0_ORT_PTx_3	PLD0_ORT_PTx_2	PLD0_ORT_PTx_1	PLD0_ORT_PTx_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ORT_PTx_7	PLD1_ORT_PTx_6	PLD1_ORT_PTx_5	PLD1_ORT_PTx_4	PLD1_ORT_PTx_3	PLD1_ORT_PTx_2	PLD1_ORT_PTx_1	PLD1_ORT_PTx_0

Bits	Name	Description
15	PLD1_ORT_PTx_7	OR term. Bit position corresponds to product term. Default Value: X
14	PLD1_ORT_PTx_6	OR term. Bit position corresponds to product term. Default Value: X
13	PLD1_ORT_PTx_5	OR term. Bit position corresponds to product term. Default Value: X
12	PLD1_ORT_PTx_4	OR term. Bit position corresponds to product term. Default Value: X
11	PLD1_ORT_PTx_3	OR term. Bit position corresponds to product term. Default Value: X
10	PLD1_ORT_PTx_2	OR term. Bit position corresponds to product term. Default Value: X
9	PLD1_ORT_PTx_1	OR term. Bit position corresponds to product term. Default Value: X
8	PLD1_ORT_PTx_0	OR term. Bit position corresponds to product term. Default Value: X
7	PLD0_ORT_PTx_7	OR term. Bit position corresponds to product term. Default Value: X
6	PLD0_ORT_PTx_6	OR term. Bit position corresponds to product term. Default Value: X
5	PLD0_ORT_PTx_5	OR term. Bit position corresponds to product term. Default Value: X
4	PLD0_ORT_PTx_4	OR term. Bit position corresponds to product term. Default Value: X

(continued)

3	PLD0_ORT_PTx_3	OR term. Bit position corresponds to product term. Default Value: X
2	PLD0_ORT_PTx_2	OR term. Bit position corresponds to product term. Default Value: X
1	PLD0_ORT_PTx_1	OR term. Bit position corresponds to product term. Default Value: X
0	PLD0_ORT_PTx_0	OR term. Bit position corresponds to product term. Default Value: X

36.1.136 UDB_P1_U0_PLD_ORT3

PLD OR Terms

Address: 0x400F3236

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ORT_PTx_7	PLD0_ORT_PTx_6	PLD0_ORT_PTx_5	PLD0_ORT_PTx_4	PLD0_ORT_PTx_3	PLD0_ORT_PTx_2	PLD0_ORT_PTx_1	PLD0_ORT_PTx_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ORT_PTx_7	PLD1_ORT_PTx_6	PLD1_ORT_PTx_5	PLD1_ORT_PTx_4	PLD1_ORT_PTx_3	PLD1_ORT_PTx_2	PLD1_ORT_PTx_1	PLD1_ORT_PTx_0

Bits	Name	Description
15	PLD1_ORT_PTx_7	OR term. Bit position corresponds to product term. Default Value: X
14	PLD1_ORT_PTx_6	OR term. Bit position corresponds to product term. Default Value: X
13	PLD1_ORT_PTx_5	OR term. Bit position corresponds to product term. Default Value: X
12	PLD1_ORT_PTx_4	OR term. Bit position corresponds to product term. Default Value: X
11	PLD1_ORT_PTx_3	OR term. Bit position corresponds to product term. Default Value: X
10	PLD1_ORT_PTx_2	OR term. Bit position corresponds to product term. Default Value: X
9	PLD1_ORT_PTx_1	OR term. Bit position corresponds to product term. Default Value: X
8	PLD1_ORT_PTx_0	OR term. Bit position corresponds to product term. Default Value: X
7	PLD0_ORT_PTx_7	OR term. Bit position corresponds to product term. Default Value: X
6	PLD0_ORT_PTx_6	OR term. Bit position corresponds to product term. Default Value: X
5	PLD0_ORT_PTx_5	OR term. Bit position corresponds to product term. Default Value: X
4	PLD0_ORT_PTx_4	OR term. Bit position corresponds to product term. Default Value: X

(continued)

3	PLD0_ORT_PTx_3	OR term. Bit position corresponds to product term. Default Value: X
2	PLD0_ORT_PTx_2	OR term. Bit position corresponds to product term. Default Value: X
1	PLD0_ORT_PTx_1	OR term. Bit position corresponds to product term. Default Value: X
0	PLD0_ORT_PTx_0	OR term. Bit position corresponds to product term. Default Value: X

36.1.137 UDB_P1_U0_PLD_MC_CFG_CEN_CONST

Macrocell configuration for Carry Enable and Constant

Address: 0x400F3238

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_MC3_DFF_C	PLD0_MC3_CEN	PLD0_MC2_DFF_C	PLD0_MC2_CEN	PLD0_MC1_DFF_C	PLD0_MC1_CEN	PLD0_MC0_DFF_C	PLD0_MC0_CEN

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_MC3_DFF_C	PLD1_MC3_CEN	PLD1_MC2_DFF_C	PLD1_MC2_CEN	PLD1_MC1_DFF_C	PLD1_MC1_CEN	PLD1_MC0_DFF_C	PLD1_MC0_CEN

Bits	Name	Description
15	PLD1_MC3_DFF_C	DFF Constant Default Value: X **0x0: NOINV:** DFF non-inverted **0x1: INVERTED:** DFF inverted
14	PLD1_MC3_CEN	Carry enable Default Value: X **0x0: DISABLE:** Disabled **0x1: ENABLE:** Enabled
13	PLD1_MC2_DFF_C	DFF Constant Default Value: X **0x0: NOINV:** DFF non-inverted **0x1: INVERTED:** DFF inverted
12	PLD1_MC2_CEN	Carry enable Default Value: X **0x0: DISABLE:** Disabled **0x1: ENABLE:** Enabled

(continued)

11	PLD1_MC1_DFF_C	DFF Constant Default Value: X **0x0: NOINV:** DFF non-inverted **0x1: INVERTED:** DFF inverted
10	PLD1_MC1_CEN	Carry enable Default Value: X **0x0: DISABLE:** Disabled **0x1: ENABLE:** Enabled
9	PLD1_MC0_DFF_C	DFF Constant Default Value: X **0x0: NOINV:** DFF non-inverted **0x1: INVERTED:** DFF inverted
8	PLD1_MC0_CEN	Carry enable Default Value: X **0x0: DISABLE:** Disabled **0x1: ENABLE:** Enabled
7	PLD0_MC3_DFF_C	DFF Constant Default Value: X **0x0: NOINV:** DFF non-inverted **0x1: INVERTED:** DFF inverted
6	PLD0_MC3_CEN	Carry enable Default Value: X **0x0: DISABLE:** Disabled **0x1: ENABLE:** Enabled
5	PLD0_MC2_DFF_C	DFF Constant Default Value: X **0x0: NOINV:** DFF non-inverted **0x1: INVERTED:** DFF inverted
4	PLD0_MC2_CEN	Carry enable Default Value: X

(continued)

		0x0: DISABLE: Disabled **0x1: ENABLE:** Enabled
3	PLD0_MC1_DFF_C	DFF Constant Default Value: X **0x0: NOINV:** DFF non-inverted **0x1: INVERTED:** DFF inverted
2	PLD0_MC1_CEN	Carry enable Default Value: X **0x0: DISABLE:** Disabled **0x1: ENABLE:** Enabled
1	PLD0_MC0_DFF_C	DFF Constant Default Value: X **0x0: NOINV:** DFF non-inverted **0x1: INVERTED:** DFF inverted
0	PLD0_MC0_CEN	Carry enable Default Value: X **0x0: DISABLE:** Disabled **0x1: ENABLE:** Enabled

36.1.138 UDB_P1_U0_PLD_MC_CFG_XORFB

PLD Macro cell XOR feedback

Address: 0x400F323A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	PLD0_MC3_XORFB [7:6]		PLD0_MC2_XORFB [5:4]		PLD0_MC1_XORFB [3:2]		PLD0_MC0_XORFB [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	PLD1_MC3_XORFB [15:14]		PLD1_MC2_XORFB [13:12]		PLD1_MC1_XORFB [11:10]		PLD1_MC0_XORFB [9:8]	

Bits	Name	Description
15 : 14	PLD1_MC3_XORFB	XOR feedback Default Value: X **0x0: DFF:** DFF **0x1: CARRY:** Carry **0x2: TFF_H:** TFF on high **0x3: TFF_L:** TFF on low
13 : 12	PLD1_MC2_XORFB	XOR feedback Default Value: X **0x0: DFF:** DFF **0x1: CARRY:** Carry **0x2: TFF_H:** TFF on high **0x3: TFF_L:** TFF on low
11 : 10	PLD1_MC1_XORFB	XOR feedback Default Value: X **0x0: DFF:** DFF **0x1: CARRY:** Carry

(continued)

		0x2: TFF_H: TFF on high **0x3: TFF_L:** TFF on low
9 : 8	PLD1_MC0_XORFB	XOR feedback Default Value: X **0x0: DFF:** DFF **0x1: CARRY:** Carry **0x2: TFF_H:** TFF on high **0x3: TFF_L:** TFF on low
7 : 6	PLD0_MC3_XORFB	XOR feedback Default Value: X **0x0: DFF:** DFF **0x1: CARRY:** Carry **0x2: TFF_H:** TFF on high **0x3: TFF_L:** TFF on low
5 : 4	PLD0_MC2_XORFB	XOR feedback Default Value: X **0x0: DFF:** DFF **0x1: CARRY:** Carry **0x2: TFF_H:** TFF on high **0x3: TFF_L:** TFF on low
3 : 2	PLD0_MC1_XORFB	XOR feedback Default Value: X **0x0: DFF:** DFF **0x1: CARRY:** Carry **0x2: TFF_H:** TFF on high **0x3: TFF_L:** TFF on low

(continued)

1 : 0	PLD0_MC0_XORFB	XOR feedback Default Value: X **0x0: DFF:** DFF **0x1: CARRY:** Carry **0x2: TFF_H:** TFF on high **0x3: TFF_L:** TFF on low

36.1.139 UDB_P1_U0_PLD_MC_SET_RESET

PLD Macro cell Set Reset Selection

Address: 0x400F323C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_MC3_RESET_SEL	PLD0_MC3_SET_SEL	PLD0_MC2_RESET_SEL	PLD0_MC2_SET_SEL	PLD0_MC1_RESET_SEL	PLD0_MC1_SET_SEL	PLD0_MC0_RESET_SEL	PLD0_MC0_SET_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_MC3_RESET_SEL	PLD1_MC3_SET_SEL	PLD1_MC2_RESET_SEL	PLD1_MC2_SET_SEL	PLD1_MC1_RESET_SEL	PLD1_MC1_SET_SEL	PLD1_MC0_RESET_SEL	PLD1_MC0_SET_SEL

Bits	Name	Description
15	PLD1_MC3_RESET_SEL	Reset select enable Default Value: X **0x0: DISABLE:** Reset not used **0x1: ENABLE:** Reset enabled
14	PLD1_MC3_SET_SEL	Set select enable Default Value: X **0x0: DISABLE:** Set not used **0x1: ENABLE:** Set enabled
13	PLD1_MC2_RESET_SEL	Reset select enable Default Value: X **0x0: DISABLE:** Reset not used **0x1: ENABLE:** Reset enabled
12	PLD1_MC2_SET_SEL	Set select enable Default Value: X **0x0: DISABLE:** Set not used **0x1: ENABLE:** Set enabled

(continued)

11	PLD1_MC1_RESET_SEL	Reset select enable Default Value: X **0x0: DISABLE:** Reset not used **0x1: ENABLE:** Reset enabled
10	PLD1_MC1_SET_SEL	Set select enable Default Value: X **0x0: DISABLE:** Set not used **0x1: ENABLE:** Set enabled
9	PLD1_MC0_RESET_SEL	Reset select enable Default Value: X **0x0: DISABLE:** Reset not used **0x1: ENABLE:** Reset enabled
8	PLD1_MC0_SET_SEL	Set select enable Default Value: X **0x0: DISABLE:** Set not used **0x1: ENABLE:** Set enabled
7	PLD0_MC3_RESET_SEL	Reset select enable Default Value: X **0x0: DISABLE:** Reset not used **0x1: ENABLE:** Reset enabled
6	PLD0_MC3_SET_SEL	Set select enable Default Value: X **0x0: DISABLE:** Set not used **0x1: ENABLE:** Set enabled
5	PLD0_MC2_RESET_SEL	Reset select enable Default Value: X **0x0: DISABLE:** Reset not used **0x1: ENABLE:** Reset enabled
4	PLD0_MC2_SET_SEL	Set select enable Default Value: X

(continued)

		0x0: DISABLE: Set not used **0x1: ENABLE:** Set enabled
3	PLD0_MC1_RESET_SEL	Reset select enable Default Value: X **0x0: DISABLE:** Reset not used **0x1: ENABLE:** Reset enabled
2	PLD0_MC1_SET_SEL	Set select enable Default Value: X **0x0: DISABLE:** Set not used **0x1: ENABLE:** Set enabled
1	PLD0_MC0_RESET_SEL	Reset select enable Default Value: X **0x0: DISABLE:** Reset not used **0x1: ENABLE:** Reset enabled
0	PLD0_MC0_SET_SEL	Set select enable Default Value: X **0x0: DISABLE:** Set not used **0x1: ENABLE:** Set enabled

36.1.140 UDB_P1_U0_PLD_MC_CFG_BYPASS

PLD Macro cell Bypass control

Address: 0x400F323E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	NC7	PLD0_MC3_BYPASS	NC5	PLD0_MC2_BYPASS	NC3	PLD0_MC1_BYPASS	NC1	PLD0_MC0_BYPASS

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	NC15	PLD1_MC3_BYPASS	NC13	PLD1_MC2_BYPASS	NC11	PLD1_MC1_BYPASS	NC9	PLD1_MC0_BYPASS

Bits	Name	Description
15	NC15	Spare register bit Default Value: X
14	PLD1_MC3_BYPASS	Bypass selection Default Value: X **0x0: REGISTER:** Registered output **0x1: COMBINATIONAL:** Combinational output
13	NC13	Spare register bit Default Value: X
12	PLD1_MC2_BYPASS	Bypass selection Default Value: X **0x0: REGISTER:** Registered output **0x1: COMBINATIONAL:** Combinational output
11	NC11	Spare register bit Default Value: X
10	PLD1_MC1_BYPASS	Bypass selection Default Value: X **0x0: REGISTER:** Registered output **0x1: COMBINATIONAL:** Combinational output

(continued)

9	NC9	Spare register bit Default Value: X
8	PLD1_MC0_BYPASS	Bypass selection Default Value: X **0x0: REGISTER:** Registered output **0x1: COMBINATIONAL:** Combinational output
7	NC7	Spare register bit Default Value: X
6	PLD0_MC3_BYPASS	Bypass selection Default Value: X **0x0: REGISTER:** Registered output **0x1: COMBINATIONAL:** Combinational output
5	NC5	Spare register bit Default Value: X
4	PLD0_MC2_BYPASS	Bypass selection Default Value: X **0x0: REGISTER:** Registered output **0x1: COMBINATIONAL:** Combinational output
3	NC3	Spare register bit Default Value: X
2	PLD0_MC1_BYPASS	Bypass selection Default Value: X **0x0: REGISTER:** Registered output **0x1: COMBINATIONAL:** Combinational output
1	NC1	Spare register bit Default Value: X
0	PLD0_MC0_BYPASS	Bypass selection Default Value: X **0x0: REGISTER:** Registered output **0x1: COMBINATIONAL:** Combinational output

36.1.141 UDB_P1_U0_CFG0

Datapath Input Selection - RAD1 RAD0. Address bits 0 and 1 to the dynamic configuration RAM

Address: 0x400F3240

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	RAD1 [6:4]			None	RAD0 [2:0]		

Bits	Name	Description
6 : 4	RAD1	Datapath Permutable Input Mux Default Value: 0 **0x0: OFF:** Input off **0x1: DP_IN0:** Set to dp_in[0] **0x2: DP_IN1:** Set to dp_in[1] **0x3: DP_IN2:** Set to dp_in[2] **0x4: DP_IN3:** Set to dp_in[3] **0x5: DP_IN4:** Set to dp_in[4] **0x6: DP_IN5:** Set to dp_in[5] **0x7: RESERVED:** Reserved
2 : 0	RAD0	Datapath Permutable Input Mux Default Value: 0 **0x0: OFF:** Input off **0x1: DP_IN0:** Set to dp_in[0] **0x2: DP_IN1:** Set to dp_in[1] **0x3: DP_IN2:** Set to dp_in[2] **0x4: DP_IN3:** Set to dp_in[3] **0x5: DP_IN4:** Set to dp_in[4]

(continued)

0x6: DP_IN5:
Set to dp_in[5]

0x7: RESERVED:
Reserved

36.1.142 UDB_P1_U0_CFG1

Datapath Input Selection - RAD2. Address bit 2 to the dynamic configuration RAM

Address: 0x400F3241

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW		
HW Access	R	R	R	R	R	R		
Name	DP_RTE_BYPASS4	DP_RTE_BYPASS3	DP_RTE_BYPASS2	DP_RTE_BYPASS1	DP_RTE_BYPASS0	RAD2 [2:0]		

Bits	Name	Description
7	DP_RTE_BYPASS4	DP_In bypass control Default Value: 0 **0x0: DP_IN4_ROUTE:** Use dp_in[4] **0x1: DP_IN4_BYPASS:** Use dp_out[4] as input via bypass
6	DP_RTE_BYPASS3	DP_In bypass control Default Value: 0 **0x0: DP_IN3_ROUTE:** Use dp_in[3] **0x1: DP_IN3_BYPASS:** Use dp_out[3] as input via bypass
5	DP_RTE_BYPASS2	DP_In bypass control Default Value: 0 **0x0: DP_IN2_ROUTE:** Use dp_in[2] **0x1: DP_IN2_BYPASS:** Use dp_out[2] as input via bypass
4	DP_RTE_BYPASS1	DP_In bypass control Default Value: 0 **0x0: DP_IN1_ROUTE:** Use dp_in[1] **0x1: DP_IN1_BYPASS:** Use dp_out[1] as input via bypass
3	DP_RTE_BYPASS0	DP_In bypass control Default Value: 0 **0x0: DP_IN0_ROUTE:** Use dp_in[0] **0x1: DP_IN0_BYPASS:** Use dp_out[0] as input via bypass

(continued)

2 : 0	RAD2	Datapath Permutable Input Mux Default Value: 0 **0x0: OFF:** Input off **0x1: DP_IN0:** Set to dp_in[0] **0x2: DP_IN1:** Set to dp_in[1] **0x3: DP_IN2:** Set to dp_in[2] **0x4: DP_IN3:** Set to dp_in[3] **0x5: DP_IN4:** Set to dp_in[4] **0x6: DP_IN5:** Set to dp_in[5] **0x7: RESERVED:** Reserved

36.1.143 UDB_P1_U0_CFG2

Datapath Input Selection - F1_LD, F0_LD.

Address: 0x400F3242

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW			RW	RW		
HW Access	R	R			R	R		
Name	NC7	F1_LD [6:4]			DP_RTE_BYPASS5	F0_LD [2:0]		

Bits	Name	Description
7	NC7	Spare register bit Default Value: 0
6 : 4	F1_LD	Datapath Permutable Input Mux Default Value: 0 **0x0: OFF:** Input off **0x1: DP_IN0:** Set to dp_in[0] **0x2: DP_IN1:** Set to dp_in[1] **0x3: DP_IN2:** Set to dp_in[2] **0x4: DP_IN3:** Set to dp_in[3] **0x5: DP_IN4:** Set to dp_in[4] **0x6: DP_IN5:** Set to dp_in[5] **0x7: RESERVED:** Reserved
3	DP_RTE_BYPASS5	DP_In bypass control Default Value: 0 **0x0: DP_IN5_ROUTE:** Use dp_in[5] **0x1: DP_IN5_BYPASS:** Use dp_out[5] via bypass
2 : 0	F0_LD	Datapath Permutable Input Mux Default Value: 0 **0x0: OFF:** Input off

(continued)

0x1: DP_IN0:
Set to dp_in[0]

0x2: DP_IN1:
Set to dp_in[1]

0x3: DP_IN2:
Set to dp_in[2]

0x4: DP_IN3:
Set to dp_in[3]

0x5: DP_IN4:
Set to dp_in[4]

0x6: DP_IN5:
Set to dp_in[5]

0x7: RESERVED:
Reserved

36.1.144 UDB_P1_U0_CFG3

Datapath Input Selection - D1_LD, D0_LD.

Address: 0x400F3243

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	D1_LD [6:4]			None	D0_LD [2:0]		

Bits	Name	Description
6 : 4	D1_LD	Datapath Permutable Input Mux Default Value: 0 **0x0: OFF:** Input off **0x1: DP_IN0:** Set to dp_in[0] **0x2: DP_IN1:** Set to dp_in[1] **0x3: DP_IN2:** Set to dp_in[2] **0x4: DP_IN3:** Set to dp_in[3] **0x5: DP_IN4:** Set to dp_in[4] **0x6: DP_IN5:** Set to dp_in[5] **0x7: RESERVED:** Reserved
2 : 0	D0_LD	Datapath Permutable Input Mux Default Value: 0 **0x0: OFF:** Input off **0x1: DP_IN0:** Set to dp_in[0] **0x2: DP_IN1:** Set to dp_in[1] **0x3: DP_IN2:** Set to dp_in[2] **0x4: DP_IN3:** Set to dp_in[3] **0x5: DP_IN4:** Set to dp_in[4]

(continued)

0x6: DP_IN5:
Set to dp_in[5]

0x7: RESERVED:
Reserved

36.1.145 UDB_P1_U0_CFG4

Datapath Input Selection - CI_MUX SI_MUX.

Address: 0x400F3244

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	CI_MUX [6:4]			None	SI_MUX [2:0]		

Bits	Name	Description
6 : 4	CI_MUX	Datapath Permutable Input Mux Default Value: 0 **0x0: OFF:** Input off **0x1: DP_IN0:** Set to dp_in[0] **0x2: DP_IN1:** Set to dp_in[1] **0x3: DP_IN2:** Set to dp_in[2] **0x4: DP_IN3:** Set to dp_in[3] **0x5: DP_IN4:** Set to dp_in[4] **0x6: DP_IN5:** Set to dp_in[5] **0x7: RESERVED:** Reserved
2 : 0	SI_MUX	Datapath Permutable Input Mux Default Value: 0 **0x0: OFF:** Input off **0x1: DP_IN0:** Set to dp_in[0] **0x2: DP_IN1:** Set to dp_in[1] **0x3: DP_IN2:** Set to dp_in[2] **0x4: DP_IN3:** Set to dp_in[3] **0x5: DP_IN4:** Set to dp_in[4]

(continued)

0x6: DP_IN5:
Set to dp_in[5]

0x7: RESERVED:
Reserved

36.1.146 UDB_P1_U0_CFG5

Datapath Output Selection for OUT1 OUT0

Address: 0x400F3245

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	OUT1 [7:4]				OUT0 [3:0]			

Bits	Name	Description
7 : 4	OUT1	Datapath Permutable Output Mux Default Value: 0 **0x0: CE0:** Comparator 0 equal **0x1: CL0:** Comparator 0 less than **0x2: Z0:** Accumulator 0 zero detect **0x3: FF0:** Accumulator 0 ones detect **0x4: CE1:** Comparator 1 equal **0x5: CL1:** Comparator 1 less than **0x6: Z1:** Accumulator 1 zero detect **0x7: FF1:** Accumulator 1 ones detect **0x8: OV_MSB:** Overflow of MSB **0x9: CO_MSB:** Carry out of MSB **0xa: CMSBO:** CRC MSB **0xb: SO:** Shift out **0xc: F0_BLK_STAT:** FIFO 0 block status defined by direction **0xd: F1_BLK_STAT:** FIFO 1 block status defined by direction **0xe: F0_BUS_STAT:** FIFO 0 bus status defined by direction and level

(continued)

		0xf: F1_BUS_STAT: FIFO 1 bus status defined by direction and level
3 : 0	OUT0	Datapath Permutable Output Mux Default Value: 0 **0x0: CE0:** Comparator 0 equal **0x1: CL0:** Comparator 0 less than **0x2: Z0:** Accumulator 0 zero detect **0x3: FF0:** Accumulator 0 ones detect **0x4: CE1:** Comparator 1 equal **0x5: CL1:** Comparator 1 less than **0x6: Z1:** Accumulator 1 zero detect **0x7: FF1:** Accumulator 1 ones detect **0x8: OV_MSB:** Overflow of MSB **0x9: CO_MSB:** Carry out of MSB **0xa: CMSBO:** CRC MSB **0xb: SO:** Shift out **0xc: F0_BLK_STAT:** FIFO 0 block status defined by direction **0xd: F1_BLK_STAT:** FIFO 1 block status defined by direction **0xe: F0_BUS_STAT:** FIFO 0 bus status defined by direction and level **0xf: F1_BUS_STAT:** FIFO 1 bus status defined by direction and level

36.1.147 UDB_P1_U0_CFG6

Datapath Output Selection for OUT3 OUT2

Address: 0x400F3246

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	OUT3 [7:4]				OUT2 [3:0]			

Bits	Name	Description
7 : 4	OUT3	Datapath Permutable Output Mux Default Value: 0 **0x0: CE0:** Comparator 0 equal **0x1: CL0:** Comparator 0 less than **0x2: Z0:** Accumulator 0 zero detect **0x3: FF0:** Accumulator 0 ones detect **0x4: CE1:** Comparator 1 equal **0x5: CL1:** Comparator 1 less than **0x6: Z1:** Accumulator 1 zero detect **0x7: FF1:** Accumulator 1 ones detect **0x8: OV_MSB:** Overflow of MSB **0x9: CO_MSB:** Carry out of MSB **0xa: CMSBO:** CRC MSB **0xb: SO:** Shift out **0xc: F0_BLK_STAT:** FIFO 0 block status defined by direction **0xd: F1_BLK_STAT:** FIFO 1 block status defined by direction **0xe: F0_BUS_STAT:** FIFO 0 bus status defined by direction and level

(continued)

		0xf: F1_BUS_STAT: FIFO 1 bus status defined by direction and level
3 : 0	OUT2	Datapath Permutable Output Mux Default Value: 0 **0x0: CE0:** Comparator 0 equal **0x1: CL0:** Comparator 0 less than **0x2: Z0:** Accumulator 0 zero detect **0x3: FF0:** Accumulator 0 ones detect **0x4: CE1:** Comparator 1 equal **0x5: CL1:** Comparator 1 less than **0x6: Z1:** Accumulator 1 zero detect **0x7: FF1:** Accumulator 1 ones detect **0x8: OV_MSB:** Overflow of MSB **0x9: CO_MSB:** Carry out of MSB **0xa: CMSBO:** CRC MSB **0xb: SO:** Shift out **0xc: F0_BLK_STAT:** FIFO 0 block status defined by direction **0xd: F1_BLK_STAT:** FIFO 1 block status defined by direction **0xe: F0_BUS_STAT:** FIFO 0 bus status defined by direction and level **0xf: F1_BUS_STAT:** FIFO 1 bus status defined by direction and level

36.1.148 UDB_P1_U0_CFG7

Datapath Output Selection for OUT5 OUT4

Address: 0x400F3247

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	OUT5 [7:4]				OUT4 [3:0]			

Bits	Name	Description
7 : 4	OUT5	Datapath Permutable Output Mux Default Value: 0 **0x0: CE0:** Comparator 0 equal **0x1: CL0:** Comparator 0 less than **0x2: Z0:** Accumulator 0 zero detect **0x3: FF0:** Accumulator 0 ones detect **0x4: CE1:** Comparator 1 equal **0x5: CL1:** Comparator 1 less than **0x6: Z1:** Accumulator 1 zero detect **0x7: FF1:** Accumulator 1 ones detect **0x8: OV_MSB:** Overflow of MSB **0x9: CO_MSB:** Carry out of MSB **0xa: CMSBO:** CRC MSB **0xb: SO:** Shift out **0xc: F0_BLK_STAT:** FIFO 0 block status defined by direction **0xd: F1_BLK_STAT:** FIFO 1 block status defined by direction **0xe: F0_BUS_STAT:** FIFO 0 bus status defined by direction and level

(continued)

		0xf: F1_BUS_STAT: FIFO 1 bus status defined by direction and level
3 : 0	OUT4	Datapath Permutable Output Mux Default Value: 0 **0x0: CE0:** Comparator 0 equal **0x1: CL0:** Comparator 0 less than **0x2: Z0:** Accumulator 0 zero detect **0x3: FF0:** Accumulator 0 ones detect **0x4: CE1:** Comparator 1 equal **0x5: CL1:** Comparator 1 less than **0x6: Z1:** Accumulator 1 zero detect **0x7: FF1:** Accumulator 1 ones detect **0x8: OV_MSB:** Overflow of MSB **0x9: CO_MSB:** Carry out of MSB **0xa: CMSBO:** CRC MSB **0xb: SO:** Shift out **0xc: F0_BLK_STAT:** FIFO 0 block status defined by direction **0xd: F1_BLK_STAT:** FIFO 1 block status defined by direction **0xe: F0_BUS_STAT:** FIFO 0 bus status defined by direction and level **0xf: F1_BUS_STAT:** FIFO 1 bus status defined by direction and level

36.1.149 UDB_P1_U0_CFG8

Datapath Output Synchronization Option

Address: 0x400F3248

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW					
HW Access	R	R	R					
Name	NC7	NC6	OUT_SYNC [5:0]					

Bits	Name	Description
7	NC7	Spare register bit Default Value: 0
6	NC6	Spare register bit Default Value: 0
5 : 0	OUT_SYNC	Datapath Output Synchronization. Each datapath output can be registered (default,0), or combinational (1) Default Value: 0 **0x0: REGISTERED:** registered **0x1: COMBINATIONAL:** combinational

36.1.150 UDB_P1_U0_CFG9

Datapath ALU Mask

Address: 0x400F3249

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	AMASK [7:0]							

Bits	Name	Description
7 : 0	AMASK	Datapath ALU Mask. The mask value in this register is applied to the output of the Datapath ALU result before the result is stored. The AMASK_EN bit (CFG12) must be set for the mask to be operational. Default Value: 0

36.1.151 UDB_P1_U0_CFG10

Datapath Compare 0 Mask

Address: 0x400F324A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CMASK0 [7:0]							

Bits	Name	Description
7 : 0	CMASK0	Datapath Compare 0 Mask. The mask value in this register is applied to the output of the Accumulator 0 before it is used for comparison in Compare block 0. The CMASK0_EN bit (CFG12) must be set for the mask to be operational. Default Value: 0

36.1.152 UDB_P1_U0_CFG11

Datapath Compare 1 Mask

Address: 0x400F324B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CMASK0 [7:0]							

Bits	Name	Description
7 : 0	CMASK0	Datapath Compare 1 Mask. The mask value in this register is applied to the selected Compare 1 block input (Accumulator 0 or Accumulator 1) before it is used for comparison. The CMASK1_EN bit (CFG12) must be set for the mask to be operational. Default Value: 0

36.1.153 UDB_P1_U0_CFG12

Datapath mask enables and shift in configuration

Address: 0x400F324C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW		RW	
HW Access	R	R	R	R	R		R	
Name	CMASK1_EN	CMASK0_EN	AMASK_EN	DEF_SI	SI_SELB [3:2]		SI_SELA [1:0]	

Bits	Name	Description
7	CMASK1_EN	Datapath mask enable Default Value: 0 **0x0: DISABLE:** Masking disabled **0x1: ENABLE:** Masking enabled
6	CMASK0_EN	Datapath mask enable Default Value: 0 **0x0: DISABLE:** Masking disabled **0x1: ENABLE:** Masking enabled
5	AMASK_EN	Datapath mask enable Default Value: 0 **0x0: DISABLE:** Masking disabled **0x1: ENABLE:** Masking enabled
4	DEF_SI	Datapath default shift value Default Value: 0 **0x0: DEFAULT_0:** Default shift is 0 **0x1: DEFAULT_1:** Default shift is 1
3 : 2	SI_SELB	Datapath shift in source select Default Value: 0 **0x0: DEFAULT:** Default value specified in default shift field **0x1: REGISTERED:** Shift in is the shift out registered from previous cycle

(continued)

		0x2: ROUTE: Shift in is selected from datapath routing input **0x3: CHAIN:** Shift in is chained from the previous datapath
1 : 0	SI_SELA	Datapath shift in source select Default Value: 0 **0x0: DEFAULT:** Default value specified in default shift field **0x1: REGISTERED:** Shift in is the shift out registered from previous cycle **0x2: ROUTE:** Shift in is selected from datapath routing input **0x3: CHAIN:** Shift in is chained from the previous datapath

36.1.154 UDB_P1_U0_CFG13

Datapath carry in and compare configuration

Address: 0x400F324D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	CMP_SELB [7:6]		CMP_SELA [5:4]		CI_SELB [3:2]		CI_SELA [1:0]	

Bits	Name	Description
7 : 6	CMP_SELB	Datapath compare select Default Value: 0 **0x0: A1_D1:** Compare A1 to D1 **0x1: A1_A0:** Compare A1 to A0 **0x2: A0_D1:** Compare A0 to D1 **0x3: A0_A0:** Compare A0 to A0
5 : 4	CMP_SELA	Datapath compare select Default Value: 0 **0x0: A1_D1:** Compare A1 to D1 **0x1: A1_A0:** Compare A1 to A0 **0x2: A0_D1:** Compare A0 to D1 **0x3: A0_A0:** Compare A0 to A0
3 : 2	CI_SELB	Datapath carry in source select Default Value: 0 **0x0: DEFAULT:** Default arithmetic mode **0x1: REGISTERED:** Carry in is the carry out registered from previous cycle **0x2: ROUTE:** Carry in is selected from datapath routing input **0x3: CHAIN:** Carry in is chained from the previous datapath
1 : 0	CI_SELA	Datapath carry in source select Default Value: 0

(continued)

0x0: DEFAULT:
Default arithmetic mode

0x1: REGISTERED:
Carry in is the carry out registered from previous cycle

0x2: ROUTE:
Carry in is selected from datapath routing input

0x3: CHAIN:
Carry in is chained from the previous datapath

36.1.155 UDB_P1_U0_CFG14

Datapath chaining and MSB configuration

Address: 0x400F324E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW			RW	RW	RW	RW
HW Access	R	R			R	R	R	R
Name	MSB_EN	MSB_SEL [6:4]			CHAIN_CMSB	CHAIN_FB	CHAIN1	CHAIN0

Bits	Name	Description
7	MSB_EN	Datapath MSB selection enable Default Value: 0 **0x0: DISABLE:** MSB selection is disabled, MSB is bit 7 **0x1: ENABLE:** MSB selection is controlled by MSB_SEL
6 : 4	MSB_SEL	Datapath MSB Selection Default Value: 0 **0x0: BIT0:** MSB is bit 0 **0x1: BIT1:** MSB is bit 1 **0x2: BIT2:** MSB is bit 2 **0x3: BIT3:** MSB is bit 3 **0x4: BIT4:** MSB is bit 4 **0x5: BIT5:** MSB is bit 5 **0x6: BIT6:** MSB is bit 6 **0x7: BIT7:** MSB is bit 7 - equivalent to MSB_EN=0
3	CHAIN_CMSB	Datapath CRC MSB chaining enable Default Value: 0 **0x0: DISABLE:** CRC MSB is not chained **0x1: ENABLE:** CRC MSB is chained from the next (MSB) datapath

(continued)

2	CHAIN_FB	Datapath CRC feedback chaining enable Default Value: 0 **0x0: DISABLE:** CRC feedback is not chained **0x1: ENABLE:** CRC feedback is chained from the previous (LSB) datapath
1	CHAIN1	Datapath condition chaining enable Default Value: 0 **0x0: DISABLE:** Conditions are not chained **0x1: ENABLE:** Conditions are chained from the previous (LSB) datapath
0	CHAIN0	Datapath condition chaining enable Default Value: 0 **0x0: DISABLE:** Conditions are not chained **0x1: ENABLE:** Conditions are chained from the previous (LSB) datapath

36.1.156 UDB_P1_U0_CFG15

Datapath FIFO, shift and parallel input control

Address: 0x400F324F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW		RW	
HW Access	R	R	R	R	R		R	
Name	PI_SEL	SHIFT_SEL	PI_DYN	MSB_SI	F1_INSEL [3:2]		F0_INSEL [1:0]	

Bits	Name	Description
7	PI_SEL	Datapath parallel input selection Default Value: 0 **0x0: NORMAL:** Normal operation, ALU source is from accumulator selection **0x1: PARALLEL:** ALU source A input is from the parallel data input
6	SHIFT_SEL	Datapath shift out selection Default Value: 0 **0x0: SOL_MSB:** Routed shift out is shift out left (sol_msb) **0x1: SOR:** Routed shift out is shift out right (sor)
5	PI_DYN	Enable for dynamic control of parallel data input (PI) mux. Default Value: 0 **0x0: DISABLE:** Parallel input mux select is only controlled by static configuration (PI_SEL). **0x1: ENABLE:** Parallel input mux to the Datapath is controlled by CFB_EN field in Datapath Dynamic RAM. When this mode is enabled, the CFB_EN usage for CRC/PRS functionality is disabled.
4	MSB_SI	Arithmetic shift right operation shift in selection Default Value: 0 **0x0: DEFAULT:** Shift in default value (when SI_SELA and/or SI_SELB == 0) **0x1: MSB:** Override default and shift in MSB value
3 : 2	F1_INSEL	Datapath FIFO Configuration Default Value: 0 **0x0: INPUT:** Input Mode: Write source is the system bus; read destination is corresponding data register or accumulator **0x1: OUTPUT_A0:** Output Mode: Write source is A0, read destination is the system bus

(continued)

		0x2: OUTPUT_A1: Output Mode: Write source is A1, read destination is the system bus **0x3: OUTPUT_ALU:** Output Mode: Write source is the ALU output, read destination is the system bus
1 : 0	F0_INSEL	Datapath FIFO Configuration Default Value: 0 **0x0: INPUT:** Input Mode: Write source is the system bus; read destination is corresponding data register or accumulator **0x1: OUTPUT_A0:** Output Mode: Write source is A0, read destination is the system bus **0x2: OUTPUT_A1:** Output Mode: Write source is A1, read destination is the system bus **0x3: OUTPUT_ALU:** Output Mode: Write source is the ALU output, read destination is the system bus

36.1.157 UDB_P1_U0_CFG16

Datapath FIFO and register access configuration control

Address: 0x400F3250

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	F1_CK_INV	F0_CK_INV	FIFO_FAST	FIFO_CAP	FIFO_EDGE	FIFO_ASYNC	EXT_CRCPRS	WRK16_CONCAT

Bits	Name	Description
7	F1_CK_INV	FIFO Clock Invert. When this bit is set, the polarity of the clock for the given FIFO will be inverted, with respect to the polarity of the selected Datapath clock. Default Value: 0 **0x0: NORMAL:** FIFO clock is the same polarity as the Datapath clock. **0x1: INVERT:** FIFO clock is inverted with respect to the Datapath clock.
6	F0_CK_INV	FIFO Clock Invert. When this bit is set, the polarity of the clock for the given FIFO will be inverted, with respect to the polarity of the selected Datapath clock. Default Value: 0 **0x0: NORMAL:** FIFO clock is the same polarity as the Datapath clock. **0x1: INVERT:** FIFO clock is inverted with respect to the Datapath clock.
5	FIFO_FAST	FIFO Fast Mode. When this bit is set, the FIFO write logic is clocked by the application bus clock. Lowers the latency of capture timing, at the expense of additional power. Default Value: 0 **0x0: DISABLE:** FIFO is clocked with selected Datapath clock. **0x1: ENABLE:** FIFO is clocked with application bus clock. Master and quadrant bus clock gating must be enabled.
4	FIFO_CAP	FIFO Software Capture Mode. When this bit is set, a read of A0 or A1 triggers a capture into F0 or F1 respectively. This function follows the chaining configuration. All accumulators in the chain from a given block to the MS block in the chain are capture Default Value: 0 **0x0: DISABLE:** FIFO capture is disabled. **0x1: ENABLE:** FIFO capture is enabled (FIFO must be in output mode). A read of A0 or A1 will write into F0 or F1.
3	FIFO_EDGE	Edge/level sensitive FIFO write control (Fx_LD). Only applies to FIFO configured in output mode Default Value: 0

(continued)

		0x0: LEVEL: FIFO write from accumulators/ALU is level sensitive. FIFO write occurs on a clock edge whenever the write control is sampled high on that edge. **0x1: EDGE:** FIFO write from accumulators/ALU is edge sensitive. FIFO write occurs on a clock edge folloing a 0 to 1 transition on the write control. The write control must be negated for at least one full cycle of the FIFO clock for a subsequent transition to be dete
2	FIFO_ASYNC	Asynchronous FIFO clocking support Default Value: 0 **0x0: DISABLE:** FIFO clocks are synchronous **0x1: ENABLE:** FIFO clocks are asynchronous
1	EXT_CRCPRS	External CRC/PRS mode Default Value: 0 **0x0: INTERNAL:** Internal CRC/PRS routing **0x1: EXTERNAL:** External CRC/PRS routing
0	WRK16_CONCAT	Datapath register access mode Default Value: 0 **0x0: DEFAULT:** 16-bit default access mode: selects registers in two consecutive UDBs in chaining order **0x1: CONCATENATE:** 16-bit concat access mode: selects concatenated registers in a single UDB

36.1.158 UDB_P1_U0_CFG17

Datapath FIFO control

Address: 0x400F3251

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [7:5]			FIFO_ADD_SYNC	NC3	NC2	F1_DYN	F0_DYN

Bits	Name	Description
4	FIFO_ADD_SYNC	Adds an additional sync flip-flop to FIFO block status. Default Value: 0 **0x0: DISABLE:** Compatible Mode: FIFO block status sync configuration is 'none' (FIFO_ASYNC = 0) and 1 sync flip-flop (FIFO_ASYNC = 1) **0x1: ENABLE:** Add Sync Mode: FIFO block status sync configuration 1 sync flip-flop (FIFO_ASYNC = 0) and 2 sync flip-flops (FIFO_ASYNC = 1)
3	NC3	Spare register bit Default Value: 0
2	NC2	Spare register bit Default Value: 0
1	F1_DYN	Default Value: 0 **0x0: STATIC:** Default. FIFO direction is static and controlled by the associated Fx_INSEL bits (CFG15). **0x1: DYNAMIC:** The associated FIFO direction is dynamically controlled by the associated 'dx_load' Datapath input signal. When the 'dx_load' signal is '0', the access is internal, where the FIFO is both a source for the Datapath, and a destination for the Datapath (dest
0	F0_DYN	When this bit is set, the associated FIFO configuration may be dynamically controlled. Default Value: 0 **0x0: STATIC:** Default. FIFO direction is static and controlled by the associated Fx_INSEL bits (CFG15). **0x1: DYNAMIC:** The associated FIFO direction is dynamically controlled by the associated 'dx_load' Datapath input signal. When the 'dx_load' signal is '0', the access is internal, where the FIFO is both a source for the Datapath, and a destination for the Datapath (dest

36.1.159 UDB_P1_U0_CFG18

Control Register Mode 0 (used in conjunction with Control Register Mode 1)

Address: 0x400F3252

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CTL_MD0 [7:0]							

Bits	Name	Description
7 : 0	CTL_MD0	CTL_MD1 and CTL_MD0 are concatenated to form an encoding for the mode of each control bit in the control register. Default Value: 0 **0x0: DIRECT:** The value written to that bit drives directly into the routing. **0x1: SYNC:** The value written is resampled by the selected SC clock. The resampled value is driven into the routing. **0x2: DOUBLE_SYNC:** The value written is doubly synced by the selected SC clock. The synched value is driven into the routing. **0x3: PULSE:** The value written is resampled and a synchronous pulse is generated and driven into the routing based on the selected SC clock. At the end of the generated pulse, the control register bit is automatically reset.

36.1.160 UDB_P1_U0_CFG19

Control Register Mode 1 (used in conjunction with Control Register Mode 0)

Address: 0x400F3253

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CTL_MD1 [7:0]							

Bits	Name	Description
7 : 0	CTL_MD1	CTL_MD1 and CTL_MD0 are concatenated to form an encoding for the mode of each control bit in the control register. Default Value: 0 **0x0: DIRECT:** The value written to that bit drives directly into the routing. **0x1: SYNC:** The value written is resampled by the selected SC clock. The resampled value is driven into the routing. **0x2: DOUBLE_SYNC:** The value written is doubly synced by the selected SC clock. The synched value is driven into the routing. **0x3: PULSE:** The value written is resampled and a synchronous pulse is generated and driven into the routing based on the selected SC clock. At the end of the generated pulse, the control register bit is automatically reset.

36.1.161 UDB_P1_U0_CFG20

Status Register input mode selection

Address: 0x400F3254

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	STAT_MD [7:0]							

Bits	Name	Description
7 : 0	STAT_MD	Mode selection for each bit of the status register. A '0' is transparent mode, where internal routing is read idrectly by CPU firmware. A '1' is sticky-clear-on-read mode, where once the given bit is set, it will stay set until the CPU reads the bit. Default Value: 0

36.1.162 UDB_P1_U0_CFG21

Spare register bits

Address: 0x400F3255

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						NC1	NC0

Bits	Name	Description
1	NC1	Spare register bit Default Value: 0
0	NC0	Spare register bit Default Value: 0

36.1.163 UDB_P1_U0_CFG22

SC block configuration control

Address: 0x400F3256

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW	RW	RW	
HW Access	None			R	R	R	R	
Name	None [7:5]			SC_EXT_RES	SC_SYNC_MD	SC_INT_MD	SC_OUT_CTL [1:0]	

Bits	Name	Description
4	SC_EXT_RES	Control register external reset operation. This bit supports autonomous usage of the control register, where a routed reset should clear the writable input registers. By default this is off because the CPU writable register can be cleared in firmware. Default Value: 0 **0x0: DISABLED:** When a routed reset is applied to the control register, only embedded state (sampling registers) are cleared **0x1: ENABLED:** When a routed reset is applied to the control register, all state is cleared, including the CPU writable control bits.
3	SC_SYNC_MD	SC Sync Mode - controls when the status register operates as a 4-bit double synchronizer module Default Value: 0 **0x0: NORMAL:** Normal Mode - Status register operation **0x1: SYNC_MODE:** Sync Mode - Routing inputs sc_in[3:0] are the 4 sync inputs, and connections sc_io[3:0] operate as the sync outputs
2	SC_INT_MD	SC Interrupt Mode - controls when the UDB driving an interrupt generated from the masked OR reduction of status bits 6 to 0 Default Value: 0 **0x0: NORMAL:** Normal Mode - Routing connection sc_io[3] is a normal input to the status register **0x1: INT_MODE:** Interrupt Mode - Routing connection sc_io[3] operates as the UDB interrupt output
1 : 0	SC_OUT_CTL	Selects the output source for the Status and Control routing connections Default Value: 0 **0x0: CONTROL:** Control out, 8-bits of control are driven to the routing connections **0x1: PARALLEL:** Datapath parallel output, 8-bits of datapath parallel output data are driven to the routing connections

(continued)

0x2: COUNTER:
Counter out, 7-bits of count and 1 bit (MSB) of terminal count are driven to the routing connections

0x3: RESERVED:
Reserved

36.1.164 UDB_P1_U0_CFG23

Counter Control

Address: 0x400F3257

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	RW	RW	RW		RW	
HW Access	None	R	R	R	R		R	
Name	None	ALT_CNT	ROUTE_EN	ROUTE_LD	CNT_EN_SEL [3:2]		CNT_LD_SEL [1:0]	

Bits	Name	Description
6	ALT_CNT	Configure the alternate operating mode of the counter Default Value: 0 **0x0: DEFAULT_MODE:** Default counter operating mode **0x1: ALT_MODE:** Alternate counter operating mode
5	ROUTE_EN	Configure the counter enable signal for routing input Default Value: 0 **0x0: DISABLE:** Routed EN signal is not used. EN signal is only controlled by firmware CNT START (ACTL register) **0x1: ROUTED:** Routed EN signal is used, CNT START must be set
4	ROUTE_LD	Configure the counter load signal for routing input Default Value: 0 **0x0: DISABLE:** Routed LD signal is not used **0x1: ROUTED:** Routed LD signal is used
3 : 2	CNT_EN_SEL	Selects the routing inputs for the counter enable signal Default Value: 0 **0x0: SC_IN4:** sc_io_in[0] **0x1: SC_IN5:** sc_io_in[1] **0x2: SC_IN6:** sc_io_in[2] **0x3: SC_IO:** sc_io_in[3]
1 : 0	CNT_LD_SEL	Selects the routing inputs for the counter load signal Default Value: 0

(continued)

0x0: SC_IN0:
sc_in[0]

0x1: SC_IN1:
sc_in[1]

0x2: SC_IN2:
sc_in[2]

0x3: SC_IN3:
sc_in[3]

36.1.165 UDB_P1_U0_CFG24

PLD0 Clock and Reset control

Address: 0x400F3258

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW		RW	
HW Access	R	R	R	R	R		R	
Name	RC_RES_SEL1	RC_RES_SEL0_OR_FRES	RC_INV	RC_EN_INV	RC_EN_MODE [3:2]		RC_EN_SEL [1:0]	

Bits	Name	Description
7	RC_RES_SEL1	Configures the routed reset for the associated UDB component block. The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES = '0' - This bit is not used. When ALT RES = '1' - The bits {RC_SEL1,RC_SEL0_OR_FRES} select the RC routing for routed reset control according to the following: 00 : rc_in [0] 01 : rc_in [1] 10 : rc_in [2] 11 : rc_in [3] Default Value: 0
6	RC_RES_SEL0_OR_FRES	Configures the routed or firmware reset for the associated UDB component block. The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES = '0' - This bit is a firmware reset. When ALT RES = '1' - The bits {RC_SEL1,RC_SEL0_OR_FRES} select the RC routing for routed reset control according to the following: 00 : rc_in [0] 01 : rc_in [1] 10 : rc_in [2] 11 : rc_in [3] Default Value: 0
5	RC_INV	Optionally inverts the clock selection for the associated UDB component block. Default Value: 0 **0x0: NOINV:** Non-inverted **0x1: INVERT:** Inverted
4	RC_EN_INV	Optionally inverts the clock enable selection for the associated UDB component blocks. Default Value: 0 **0x0: NOINV:** Non-inverted **0x1: INVERT:** Inverted
3 : 2	RC_EN_MODE	Selects the operating mode for the clock to the associated UDB component block. Default Value: 0

(continued)

		0x0: OFF: Always off **0x1: ON:** Always on **0x2: POSEDGE:** Positive edge **0x3: LEVEL:** Level sensitive
1 : 0	RC_EN_SEL	Selects channel route for enable control to the associated UDB component block Default Value: 0 **0x0: RC_IN0:** rc_in[0] **0x1: RC_IN1:** rc_in[1] **0x2: RC_IN2:** rc_in[2] **0x3: RC_IN3:** rc_in[3]

36.1.166 UDB_P1_U0_CFG25

PLD1 Clock and Reset control

Address: 0x400F3259

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW		RW	
HW Access	R	R	R	R	R		R	
Name	RC_RES_SEL1	RC_RES_SEL0_OR_FRES	RC_INV	RC_EN_INV	RC_EN_MODE [3:2]		RC_EN_SEL [1:0]	

Bits	Name	Description
7	RC_RES_SEL1	Configures the routed reset for the associated UDB component block. The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES = '0' - This bit is not used. When ALT RES = '1' - The bits {RC_SEL1,RC_SEL0_OR_FRES} select the RC routing for routed reset control according to the following: 00 : rc_in [0] 01 : rc_in [1] 10 : rc_in [2] 11 : rc_in [3] Default Value: 0
6	RC_RES_SEL0_OR_FRES	Configures the routed or firmware reset for the associated UDB component block. The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES = '0' - This bit is a firmware reset. When ALT RES = '1' - The bits {RC_SEL1,RC_SEL0_OR_FRES} select the RC routing for routed reset control according to the following: 00 : rc_in [0] 01 : rc_in [1] 10 : rc_in [2] 11 : rc_in [3] Default Value: 0
5	RC_INV	Optionally inverts the clock selection for the associated UDB component block. Default Value: 0 **0x0: NOINV:** Non-inverted **0x1: INVERT:** Inverted
4	RC_EN_INV	Optionally inverts the clock enable selection for the associated UDB component blocks. Default Value: 0 **0x0: NOINV:** Non-inverted **0x1: INVERT:** Inverted
3 : 2	RC_EN_MODE	Selects the operating mode for the clock to the associated UDB component block. Default Value: 0

(continued)

		0x0: OFF: Always off **0x1: ON:** Always on **0x2: POSEDGE:** Positive edge **0x3: LEVEL:** Level sensitive
1 : 0	RC_EN_SEL	Selects channel route for enable control to the associated UDB component block Default Value: 0 **0x0: RC_IN0:** rc_in[0] **0x1: RC_IN1:** rc_in[1] **0x2: RC_IN2:** rc_in[2] **0x3: RC_IN3:** rc_in[3]

36.1.167 UDB_P1_U0_CFG26

Datapath Clock and Reset control

Address: 0x400F325A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW		RW	
HW Access	R	R	R	R	R		R	
Name	RC_RES_SEL1	RC_RES_SEL0_OR_FRES	RC_INV	RC_EN_INV	RC_EN_MODE [3:2]		RC_EN_SEL [1:0]	

Bits	Name	Description
7	RC_RES_SEL1	Configures the routed reset for the associated UDB component block. The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES = '0' - This bit is not used. When ALT RES = '1' - The bits {RC_SEL1,RC_SEL0_OR_FRES} select the RC routing for routed reset control according to the following: 00 : rc_in [0] 01 : rc_in [1] 10 : rc_in [2] 11 : rc_in [3] Default Value: 0
6	RC_RES_SEL0_OR_FRES	Configures the routed or firmware reset for the associated UDB component block. The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES = '0' - This bit is a firmware reset. When ALT RES = '1' - The bits {RC_SEL1,RC_SEL0_OR_FRES} select the RC routing for routed reset control according to the following: 00 : rc_in [0] 01 : rc_in [1] 10 : rc_in [2] 11 : rc_in [3] Default Value: 0
5	RC_INV	Optionally inverts the clock selection for the associated UDB component block. Default Value: 0 **0x0: NOINV:** Non-inverted **0x1: INVERT:** Inverted
4	RC_EN_INV	Optionally inverts the clock enable selection for the associated UDB component blocks. Default Value: 0 **0x0: NOINV:** Non-inverted **0x1: INVERT:** Inverted
3 : 2	RC_EN_MODE	Selects the operating mode for the clock to the associated UDB component block. Default Value: 0

(continued)

		0x0: OFF: Always off **0x1: ON:** Always on **0x2: POSEDGE:** Positive edge **0x3: LEVEL:** Level sensitive
1 : 0	RC_EN_SEL	Selects channel route for enable control to the associated UDB component block Default Value: 0 **0x0: RC_IN0:** rc_in[0] **0x1: RC_IN1:** rc_in[1] **0x2: RC_IN2:** rc_in[2] **0x3: RC_IN3:** rc_in[3]

36.1.168 UDB_P1_U0_CFG27

Status/Control Clock and Reset control

Address: 0x400F325B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW		RW	
HW Access	R	R	R	R	R		R	
Name	RC_RES_SEL1	RC_RES_SEL0_OR_FRES	RC_INV	RC_EN_INV	RC_EN_MODE [3:2]		RC_EN_SEL [1:0]	

Bits	Name	Description
7	RC_RES_SEL1	Configures the routed reset for the associated UDB component block. The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES = '0' - This bit is not used. When ALT RES = '1' - The bits {RC_SEL1,RC_SEL0_OR_FRES} select the RC routing for routed reset control according to the following: 00 : rc_in [0] 01 : rc_in [1] 10 : rc_in [2] 11 : rc_in [3] Default Value: 0
6	RC_RES_SEL0_OR_FRES	Configures the routed or firmware reset for the associated UDB component block. The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES = '0' - This bit is a firmware reset. When ALT RES = '1' - The bits {RC_SEL1,RC_SEL0_OR_FRES} select the RC routing for routed reset control according to the following: 00 : rc_in [0] 01 : rc_in [1] 10 : rc_in [2] 11 : rc_in [3] Default Value: 0
5	RC_INV	Optionally inverts the clock selection for the associated UDB component block. Default Value: 0 **0x0: NOINV:** Non-inverted **0x1: INVERT:** Inverted
4	RC_EN_INV	Optionally inverts the clock enable selection for the associated UDB component blocks. Default Value: 0 **0x0: NOINV:** Non-inverted **0x1: INVERT:** Inverted
3 : 2	RC_EN_MODE	Selects the operating mode for the clock to the associated UDB component block. Default Value: 0

(continued)

		0x0: OFF: Always off **0x1: ON:** Always on **0x2: POSEDGE:** Positive edge **0x3: LEVEL:** Level sensitive
1 : 0	RC_EN_SEL	Selects channel route for enable control to the associated UDB component block Default Value: 0 **0x0: RC_IN0:** rc_in[0] **0x1: RC_IN1:** rc_in[1] **0x2: RC_IN2:** rc_in[2] **0x3: RC_IN3:** rc_in[3]

36.1.169 UDB_P1_U0_CFG28

Clock Selection for PLD1 and PLD0

Address: 0x400F325C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PLD1_CK_SEL [7:4]				PLD0_CK_SEL [3:0]			

Bits	Name	Description
7 : 4	PLD1_CK_SEL	Clock selection registers Default Value: 0 **0x0: GCLK0:** gclk[0] **0x1: GCLK1:** gclk[1] **0x2: GCLK2:** gclk[2] **0x3: GCLK3:** gclk[3] **0x4: GCLK4:** gclk[4] **0x5: GCLK5:** gclk[5] **0x6: GCLK6:** gclk[6] **0x7: GCLK7:** gclk[7] **0x8: EXT_CLK:** ext_clk **0x9: SYSCLK:** sysclk
3 : 0	PLD0_CK_SEL	Clock selection registers Default Value: 0 **0x0: GCLK0:** gclk[0] **0x1: GCLK1:** gclk[1] **0x2: GCLK2:** gclk[2] **0x3: GCLK3:** gclk[3]

(continued)

0x4: GCLK4:
gclk[4]

0x5: GCLK5:
gclk[5]

0x6: GCLK6:
gclk[6]

0x7: GCLK7:
gclk[7]

0x8: EXT_CLK:
ext_clk

0x9: SYSCLK:
sysclk

36.1.170 UDB_P1_U0_CFG29

Clock Selection for Datapath, Status and Control

Address: 0x400F325D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	SC_CK_SEL [7:4]				DP_CK_SEL [3:0]			

Bits	Name	Description
7 : 4	SC_CK_SEL	Clock selection registers Default Value: 0 **0x0: GCLK0:** gclk[0] **0x1: GCLK1:** gclk[1] **0x2: GCLK2:** gclk[2] **0x3: GCLK3:** gclk[3] **0x4: GCLK4:** gclk[4] **0x5: GCLK5:** gclk[5] **0x6: GCLK6:** gclk[6] **0x7: GCLK7:** gclk[7] **0x8: EXT_CLK:** ext_clk **0x9: SYSCLK:** sysclk
3 : 0	DP_CK_SEL	Clock selection registers Default Value: 0 **0x0: GCLK0:** gclk[0] **0x1: GCLK1:** gclk[1] **0x2: GCLK2:** gclk[2] **0x3: GCLK3:** gclk[3]

(continued)

0x4: GCLK4:
gclk[4]

0x5: GCLK5:
gclk[5]

0x6: GCLK6:
gclk[6]

0x7: GCLK7:
gclk[7]

0x8: EXT_CLK:
ext_clk

0x9: SYSCLK:
sysclk

36.1.171 UDB_P1_U0_CFG30

Reset control

Address: 0x400F325E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	None	RW	RW	RW	RW	
HW Access	R	R	None	R	R	R	R	
Name	SC_RES_POL	DP_RES_POL	None	GUDB_WR	EN_RES_CNTCTL	RES_POL	RES_SEL [1:0]	

Bits	Name	Description
7	SC_RES_POL	Only valid when ALT RES (CFG31) is '1'. This bit controls the polarity of the selected SC routed reset. Default Value: 0 **0x0: NOINV:** Routed reset to the Status and Control block is true polarity. **0x1: INVERT:** Routed reset to the Status and Control block is inverted polarity.
6	DP_RES_POL	Only valid when ALT RES (CFG31) is '1'. This bit controls the polarity of the selected Datapath routed reset. Default Value: 0 **0x0: NOINV:** Routed reset to the Datapath block is true polarity. **0x1: INVERT:** Routed reset to the Datapath block is inverted polarity.
4	GUDB_WR	Enable global write operation for the configuration and working registers in this UDB. When this bit is set, the UDB ID select decoding is bypassed. Default Value: 0 **0x0: DISABLE:** Global UDB configuration/working register write is disabled **0x1: ENABLE:** Global UDB configuration/working register write is enabled
3	EN_RES_CNTCTL	This bit gates the routed reset to the counter/control register. By default, the operation is compatible, i.e., it only applies to the counter. However, if the updated control regisiter modes are used (sync mode, pulse mode, or the ext res bit) then the routed reset applies to the control register also. Default Value: 0 **0x0: DISABLE:** Routed reset is not applied to counter/control register **0x1: ENABLE:** Routed reset is applied to the counter/control register

(continued)

2	RES_POL	The meaning of this bit depends on the value of the ALT RES bit in CFG31. When ALT RES is '0' (compatible mode), this bit sets the polarity of the routed reset. When ALT RES is '1', this bit is unused. Default Value: 0 **0x0: NEGATED:** Polarity of the routed reset is true. **0x1: ASSERTED:** Polarity of the routed reset is inverted.
1 : 0	RES_SEL	The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES is '0' (compatible mode), this 2 bit field selects the RC routing input for the compatible reset scheme. When the ALT RES bit is '1', these bits are not used. Default Value: 0 **0x0: RC_IN0:** rc_in[0] **0x1: RC_IN1:** rc_in[1] **0x2: RC_IN2:** rc_in[2] **0x3: RC_IN3:** rc_in[3]

36.1.172 UDB_P1_U0_CFG31

Reset control

Address: 0x400F325F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW		RW	RW	RW	RW
HW Access	R	R	R		R	R	R	R
Name	PLD1_RES_POL	PLD0_RES_POL	EXT_CK_SEL [5:4]		EN_RES_DP	EN_RES_STAT	EXT_SYNC	ALT_RES

Bits	Name	Description
7	PLD1_RES_POL	Not connected. NOTE: There is only one routed reset available to both PLDs in the UDB. When ALT RES is '1', PLD0 RES SEL controls the polarity of the routed reset for both PLDs. Default Value: 0 **0x0: NOINV:** Not Used **0x1: INVERT:** Not Used
6	PLD0_RES_POL	The meaning of this bit depends on the value of ALT RES. When ALT RES (CFG31) is '1', this bit controls the polarity of the selected PLD0 routed reset. NOTE: There is only one routed reset available to both PLDs in the UDB. When ALT RES is '1', PLD0 RES SEL controls the polarity of the routed reset for both PLDs. Default Value: 0 **0x0: NOINV:** Routed reset to the PLD0/PLD1 block is true polarity. **0x1: INVERT:** Routed reset to the PLD0/PLD1 block is inverted polarity.
5 : 4	EXT_CK_SEL	External clock selection Default Value: 0 **0x0: RC_IN0:** rc_in[0] **0x1: RC_IN1:** rc_in[1] **0x2: RC_IN2:** rc_in[2] **0x3: RC_IN3:** rc_in[3]
3	EN_RES_DP	Only valid when ALT RES (CFG31) is '1'. This bit gates the routed reset to the Datapath block. Default Value: 0 **0x0: DISABLE:** Routed reset to the Datapath block is gated off. **0x1: ENABLE:** Routed reset to the Datapath block is on. ALT RES must be '1' and routed reset must be selected in CFG26

(continued)

2	EN_RES_STAT	Only valid when ALT RES (CFG31) is '1'. This bit gates the routed reset to the status register. Default Value: 0 **0x0: NEGATED:** Status register routed reset is gated off **0x1: ASSERTED:** Status register routed reset is on
1	EXT_SYNC	Enable synchronization of selected external clock Default Value: 0 **0x0: DISABLE:** Selected external clock input is not synchronized **0x1: ENABLE:** Selected external clock input is synchronized
0	ALT_RES	This bit toggles between two reset configurations. When this bit is '0', one routed reset is shared by all components in this UDB (compatible mode). When this bit is a 1, each block can select a unique routed reset from the available RC inputs. Default Value: 0 **0x0: COMPATIBLE:** All UDB blocks share a common routed reset. **0x1: ALTERNATE:** Each UDB component block can select and control its individual routed reset.

36.1.173 UDB_P1_U0_DCFG0

Dynamic Configuration RAM

Address: 0x400F3260

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW	RW	RW	RW
HW Access	R		R		R	R	R	R
Name	A0_WR_SRC [7:6]		A1_WR_SRC [5:4]		CFB_EN	CI_SEL	SI_SEL	CMP_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW	RW		RW	
HW Access	R			R	R		R	
Name	FUNC [15:13]			SRC_A	SRC_B [11:10]		SHIFT [9:8]	

Bits	Name	Description
15 : 13	FUNC	Dynamic ALU function selection Default Value: X **0x0: PASS:** Pass **0x1: INC_A:** Increment source A **0x2: DEC_A:** Decrement source A **0x3: ADD:** Add **0x4: SUB:** Subtract **0x5: XOR:** Bitwise XOR **0x6: AND:** Bitwise AND **0x7: OR:** Bitwise OR
12	SRC_A	Dynamic ALU source A selection Default Value: X **0x0: A0:** Configuration A **0x1: A1:** Configuration B
11 : 10	SRC_B	Dynamic ALU source B selection Default Value: X

(continued)

		0x0: D0: ALU source B is D0 **0x1: D1:** ALU source B is D1 **0x2: A0:** ALU source B is A0 **0x3: A1:** ALU source B is A1
9 : 8	SHIFT	Dynamic shift selection Default Value: X **0x0: NOSHIFT:** No shift **0x1: LEFT:** Left Shift **0x2: RIGHT:** Right Shift **0x3: SWAP:** Nibble swap
7 : 6	A0_WR_SRC	Dynamic A0 write source selection Default Value: X **0x0: NOWRITE:** no value written to A0 **0x1: ALU:** ALU output written to A0 **0x2: D0:** D1 value written to A0 **0x3: F0:** F1 value written to A0
5 : 4	A1_WR_SRC	Dynamic A1 write source selection Default Value: X **0x0: NOWRITE:** no value written to A1 **0x1: ALU:** ALU output written to A1 **0x2: D1:** D1 value written to A1 **0x3: F1:** F1 value written to A1
3	CFB_EN	Dynamic CRC feedback selection Default Value: X **0x0: DISABLE:** CRC feedback disabled **0x1: ENABLE:** CRC feedback enabled

(continued)

2	CI_SEL	Dynamic carry in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
1	SI_SEL	Dynamic shift in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
0	CMP_SEL	Dynamic compare selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B

36.1.174 UDB_P1_U0_DCFG1

Dynamic Configuration RAM

Address: 0x400F3262

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW	RW	RW	RW
HW Access	R		R		R	R	R	R
Name	A0_WR_SRC [7:6]		A1_WR_SRC [5:4]		CFB_EN	CI_SEL	SI_SEL	CMP_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW	RW		RW	
HW Access	R			R	R		R	
Name	FUNC [15:13]			SRC_A	SRC_B [11:10]		SHIFT [9:8]	

Bits	Name	Description
15 : 13	FUNC	Dynamic ALU function selection Default Value: X **0x0: PASS:** Pass **0x1: INC_A:** Increment source A **0x2: DEC_A:** Decrement source A **0x3: ADD:** Add **0x4: SUB:** Subtract **0x5: XOR:** Bitwise XOR **0x6: AND:** Bitwise AND **0x7: OR:** Bitwise OR
12	SRC_A	Dynamic ALU source A selection Default Value: X **0x0: A0:** Configuration A **0x1: A1:** Configuration B
11 : 10	SRC_B	Dynamic ALU source B selection Default Value: X

(continued)

		0x0: D0: ALU source B is D0 **0x1: D1:** ALU source B is D1 **0x2: A0:** ALU source B is A0 **0x3: A1:** ALU source B is A1
9 : 8	SHIFT	Dynamic shift selection Default Value: X **0x0: NOSHIFT:** No shift **0x1: LEFT:** Left Shift **0x2: RIGHT:** Right Shift **0x3: SWAP:** Nibble swap
7 : 6	A0_WR_SRC	Dynamic A0 write source selection Default Value: X **0x0: NOWRITE:** no value written to A0 **0x1: ALU:** ALU output written to A0 **0x2: D0:** D1 value written to A0 **0x3: F0:** F1 value written to A0
5 : 4	A1_WR_SRC	Dynamic A1 write source selection Default Value: X **0x0: NOWRITE:** no value written to A1 **0x1: ALU:** ALU output written to A1 **0x2: D1:** D1 value written to A1 **0x3: F1:** F1 value written to A1
3	CFB_EN	Dynamic CRC feedback selection Default Value: X **0x0: DISABLE:** CRC feedback disabled **0x1: ENABLE:** CRC feedback enabled

(continued)

2	CI_SEL	Dynamic carry in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
1	SI_SEL	Dynamic shift in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
0	CMP_SEL	Dynamic compare selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B

36.1.175 UDB_P1_U0_DCFG2

Dynamic Configuration RAM

Address: 0x400F3264

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW	RW	RW	RW
HW Access	R		R		R	R	R	R
Name	A0_WR_SRC [7:6]		A1_WR_SRC [5:4]		CFB_EN	CI_SEL	SI_SEL	CMP_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW	RW		RW	
HW Access	R			R	R		R	
Name	FUNC [15:13]			SRC_A	SRC_B [11:10]		SHIFT [9:8]	

Bits	Name	Description
15 : 13	FUNC	Dynamic ALU function selection Default Value: X **0x0: PASS:** Pass **0x1: INC_A:** Increment source A **0x2: DEC_A:** Decrement source A **0x3: ADD:** Add **0x4: SUB:** Subtract **0x5: XOR:** Bitwise XOR **0x6: AND:** Bitwise AND **0x7: OR:** Bitwise OR
12	SRC_A	Dynamic ALU source A selection Default Value: X **0x0: A0:** Configuration A **0x1: A1:** Configuration B
11 : 10	SRC_B	Dynamic ALU source B selection Default Value: X

(continued)

		0x0: D0: ALU source B is D0 **0x1: D1:** ALU source B is D1 **0x2: A0:** ALU source B is A0 **0x3: A1:** ALU source B is A1
9 : 8	SHIFT	Dynamic shift selection Default Value: X **0x0: NOSHIFT:** No shift **0x1: LEFT:** Left Shift **0x2: RIGHT:** Right Shift **0x3: SWAP:** Nibble swap
7 : 6	A0_WR_SRC	Dynamic A0 write source selection Default Value: X **0x0: NOWRITE:** no value written to A0 **0x1: ALU:** ALU output written to A0 **0x2: D0:** D1 value written to A0 **0x3: F0:** F1 value written to A0
5 : 4	A1_WR_SRC	Dynamic A1 write source selection Default Value: X **0x0: NOWRITE:** no value written to A1 **0x1: ALU:** ALU output written to A1 **0x2: D1:** D1 value written to A1 **0x3: F1:** F1 value written to A1
3	CFB_EN	Dynamic CRC feedback selection Default Value: X **0x0: DISABLE:** CRC feedback disabled **0x1: ENABLE:** CRC feedback enabled

(continued)

2	CI_SEL	Dynamic carry in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
1	SI_SEL	Dynamic shift in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
0	CMP_SEL	Dynamic compare selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B

36.1.176 UDB_P1_U0_DCFG3

Dynamic Configuration RAM

Address: 0x400F3266

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW	RW	RW	RW
HW Access	R		R		R	R	R	R
Name	A0_WR_SRC [7:6]		A1_WR_SRC [5:4]		CFB_EN	CI_SEL	SI_SEL	CMP_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW	RW		RW	
HW Access	R			R	R		R	
Name	FUNC [15:13]			SRC_A	SRC_B [11:10]		SHIFT [9:8]	

Bits	Name	Description
15 : 13	FUNC	Dynamic ALU function selection Default Value: X **0x0: PASS:** Pass **0x1: INC_A:** Increment source A **0x2: DEC_A:** Decrement source A **0x3: ADD:** Add **0x4: SUB:** Subtract **0x5: XOR:** Bitwise XOR **0x6: AND:** Bitwise AND **0x7: OR:** Bitwise OR
12	SRC_A	Dynamic ALU source A selection Default Value: X **0x0: A0:** Configuration A **0x1: A1:** Configuration B
11 : 10	SRC_B	Dynamic ALU source B selection Default Value: X

(continued)

		0x0: D0: ALU source B is D0 **0x1: D1:** ALU source B is D1 **0x2: A0:** ALU source B is A0 **0x3: A1:** ALU source B is A1
9 : 8	SHIFT	Dynamic shift selection Default Value: X **0x0: NOSHIFT:** No shift **0x1: LEFT:** Left Shift **0x2: RIGHT:** Right Shift **0x3: SWAP:** Nibble swap
7 : 6	A0_WR_SRC	Dynamic A0 write source selection Default Value: X **0x0: NOWRITE:** no value written to A0 **0x1: ALU:** ALU output written to A0 **0x2: D0:** D1 value written to A0 **0x3: F0:** F1 value written to A0
5 : 4	A1_WR_SRC	Dynamic A1 write source selection Default Value: X **0x0: NOWRITE:** no value written to A1 **0x1: ALU:** ALU output written to A1 **0x2: D1:** D1 value written to A1 **0x3: F1:** F1 value written to A1
3	CFB_EN	Dynamic CRC feedback selection Default Value: X **0x0: DISABLE:** CRC feedback disabled **0x1: ENABLE:** CRC feedback enabled

(continued)

2	CI_SEL	Dynamic carry in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
1	SI_SEL	Dynamic shift in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
0	CMP_SEL	Dynamic compare selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B

36.1.177 UDB_P1_U0_DCFG4

Dynamic Configuration RAM

Address: 0x400F3268

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW	RW	RW	RW
HW Access	R		R		R	R	R	R
Name	A0_WR_SRC [7:6]		A1_WR_SRC [5:4]		CFB_EN	CI_SEL	SI_SEL	CMP_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW	RW		RW	
HW Access	R			R	R		R	
Name	FUNC [15:13]			SRC_A	SRC_B [11:10]		SHIFT [9:8]	

Bits	Name	Description
15 : 13	FUNC	Dynamic ALU function selection Default Value: X **0x0: PASS:** Pass **0x1: INC_A:** Increment source A **0x2: DEC_A:** Decrement source A **0x3: ADD:** Add **0x4: SUB:** Subtract **0x5: XOR:** Bitwise XOR **0x6: AND:** Bitwise AND **0x7: OR:** Bitwise OR
12	SRC_A	Dynamic ALU source A selection Default Value: X **0x0: A0:** Configuration A **0x1: A1:** Configuration B
11 : 10	SRC_B	Dynamic ALU source B selection Default Value: X

(continued)

		0x0: D0: ALU source B is D0 **0x1: D1:** ALU source B is D1 **0x2: A0:** ALU source B is A0 **0x3: A1:** ALU source B is A1
9 : 8	SHIFT	Dynamic shift selection Default Value: X **0x0: NOSHIFT:** No shift **0x1: LEFT:** Left Shift **0x2: RIGHT:** Right Shift **0x3: SWAP:** Nibble swap
7 : 6	A0_WR_SRC	Dynamic A0 write source selection Default Value: X **0x0: NOWRITE:** no value written to A0 **0x1: ALU:** ALU output written to A0 **0x2: D0:** D1 value written to A0 **0x3: F0:** F1 value written to A0
5 : 4	A1_WR_SRC	Dynamic A1 write source selection Default Value: X **0x0: NOWRITE:** no value written to A1 **0x1: ALU:** ALU output written to A1 **0x2: D1:** D1 value written to A1 **0x3: F1:** F1 value written to A1
3	CFB_EN	Dynamic CRC feedback selection Default Value: X **0x0: DISABLE:** CRC feedback disabled **0x1: ENABLE:** CRC feedback enabled

(continued)

2	CI_SEL	Dynamic carry in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
1	SI_SEL	Dynamic shift in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
0	CMP_SEL	Dynamic compare selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B

36.1.178 UDB_P1_U0_DCFG5

Dynamic Configuration RAM

Address: 0x400F326A

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW	RW	RW	RW
HW Access	R		R		R	R	R	R
Name	A0_WR_SRC [7:6]		A1_WR_SRC [5:4]		CFB_EN	CI_SEL	SI_SEL	CMP_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW	RW		RW	
HW Access	R			R	R		R	
Name	FUNC [15:13]			SRC_A	SRC_B [11:10]		SHIFT [9:8]	

Bits	Name	Description
15 : 13	FUNC	Dynamic ALU function selection Default Value: X **0x0: PASS:** Pass **0x1: INC_A:** Increment source A **0x2: DEC_A:** Decrement source A **0x3: ADD:** Add **0x4: SUB:** Subtract **0x5: XOR:** Bitwise XOR **0x6: AND:** Bitwise AND **0x7: OR:** Bitwise OR
12	SRC_A	Dynamic ALU source A selection Default Value: X **0x0: A0:** Configuration A **0x1: A1:** Configuration B
11 : 10	SRC_B	Dynamic ALU source B selection Default Value: X

(continued)

		0x0: D0: ALU source B is D0 **0x1: D1:** ALU source B is D1 **0x2: A0:** ALU source B is A0 **0x3: A1:** ALU source B is A1
9 : 8	SHIFT	Dynamic shift selection Default Value: X **0x0: NOSHIFT:** No shift **0x1: LEFT:** Left Shift **0x2: RIGHT:** Right Shift **0x3: SWAP:** Nibble swap
7 : 6	A0_WR_SRC	Dynamic A0 write source selection Default Value: X **0x0: NOWRITE:** no value written to A0 **0x1: ALU:** ALU output written to A0 **0x2: D0:** D1 value written to A0 **0x3: F0:** F1 value written to A0
5 : 4	A1_WR_SRC	Dynamic A1 write source selection Default Value: X **0x0: NOWRITE:** no value written to A1 **0x1: ALU:** ALU output written to A1 **0x2: D1:** D1 value written to A1 **0x3: F1:** F1 value written to A1
3	CFB_EN	Dynamic CRC feedback selection Default Value: X **0x0: DISABLE:** CRC feedback disabled **0x1: ENABLE:** CRC feedback enabled

(continued)

2	CI_SEL	Dynamic carry in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
1	SI_SEL	Dynamic shift in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
0	CMP_SEL	Dynamic compare selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B

36.1.179 UDB_P1_U0_DCFG6

Dynamic Configuration RAM

Address: 0x400F326C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW	RW	RW	RW
HW Access	R		R		R	R	R	R
Name	A0_WR_SRC [7:6]		A1_WR_SRC [5:4]		CFB_EN	CI_SEL	SI_SEL	CMP_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW	RW		RW	
HW Access	R			R	R		R	
Name	FUNC [15:13]			SRC_A	SRC_B [11:10]		SHIFT [9:8]	

Bits	Name	Description
15 : 13	FUNC	Dynamic ALU function selection Default Value: X **0x0: PASS:** Pass **0x1: INC_A:** Increment source A **0x2: DEC_A:** Decrement source A **0x3: ADD:** Add **0x4: SUB:** Subtract **0x5: XOR:** Bitwise XOR **0x6: AND:** Bitwise AND **0x7: OR:** Bitwise OR
12	SRC_A	Dynamic ALU source A selection Default Value: X **0x0: A0:** Configuration A **0x1: A1:** Configuration B
11 : 10	SRC_B	Dynamic ALU source B selection Default Value: X

(continued)

		0x0: D0: ALU source B is D0 **0x1: D1:** ALU source B is D1 **0x2: A0:** ALU source B is A0 **0x3: A1:** ALU source B is A1
9 : 8	SHIFT	Dynamic shift selection Default Value: X **0x0: NOSHIFT:** No shift **0x1: LEFT:** Left Shift **0x2: RIGHT:** Right Shift **0x3: SWAP:** Nibble swap
7 : 6	A0_WR_SRC	Dynamic A0 write source selection Default Value: X **0x0: NOWRITE:** no value written to A0 **0x1: ALU:** ALU output written to A0 **0x2: D0:** D1 value written to A0 **0x3: F0:** F1 value written to A0
5 : 4	A1_WR_SRC	Dynamic A1 write source selection Default Value: X **0x0: NOWRITE:** no value written to A1 **0x1: ALU:** ALU output written to A1 **0x2: D1:** D1 value written to A1 **0x3: F1:** F1 value written to A1
3	CFB_EN	Dynamic CRC feedback selection Default Value: X **0x0: DISABLE:** CRC feedback disabled **0x1: ENABLE:** CRC feedback enabled

(continued)

2	CI_SEL	Dynamic carry in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
1	SI_SEL	Dynamic shift in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
0	CMP_SEL	Dynamic compare selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B

36.1.180 UDB_P1_U0_DCFG7

Dynamic Configuration RAM

Address: 0x400F326E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW	RW	RW	RW
HW Access	R		R		R	R	R	R
Name	A0_WR_SRC [7:6]		A1_WR_SRC [5:4]		CFB_EN	CI_SEL	SI_SEL	CMP_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW	RW		RW	
HW Access	R			R	R		R	
Name	FUNC [15:13]			SRC_A	SRC_B [11:10]		SHIFT [9:8]	

Bits	Name	Description
15 : 13	FUNC	Dynamic ALU function selection Default Value: X **0x0: PASS:** Pass **0x1: INC_A:** Increment source A **0x2: DEC_A:** Decrement source A **0x3: ADD:** Add **0x4: SUB:** Subtract **0x5: XOR:** Bitwise XOR **0x6: AND:** Bitwise AND **0x7: OR:** Bitwise OR
12	SRC_A	Dynamic ALU source A selection Default Value: X **0x0: A0:** Configuration A **0x1: A1:** Configuration B
11 : 10	SRC_B	Dynamic ALU source B selection Default Value: X

(continued)

		0x0: D0: ALU source B is D0 **0x1: D1:** ALU source B is D1 **0x2: A0:** ALU source B is A0 **0x3: A1:** ALU source B is A1
9 : 8	SHIFT	Dynamic shift selection Default Value: X **0x0: NOSHIFT:** No shift **0x1: LEFT:** Left Shift **0x2: RIGHT:** Right Shift **0x3: SWAP:** Nibble swap
7 : 6	A0_WR_SRC	Dynamic A0 write source selection Default Value: X **0x0: NOWRITE:** no value written to A0 **0x1: ALU:** ALU output written to A0 **0x2: D0:** D1 value written to A0 **0x3: F0:** F1 value written to A0
5 : 4	A1_WR_SRC	Dynamic A1 write source selection Default Value: X **0x0: NOWRITE:** no value written to A1 **0x1: ALU:** ALU output written to A1 **0x2: D1:** D1 value written to A1 **0x3: F1:** F1 value written to A1
3	CFB_EN	Dynamic CRC feedback selection Default Value: X **0x0: DISABLE:** CRC feedback disabled **0x1: ENABLE:** CRC feedback enabled

(continued)

2	CI_SEL	Dynamic carry in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
1	SI_SEL	Dynamic shift in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
0	CMP_SEL	Dynamic compare selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B

36.1.181 UDB_P1_U1_PLD_IT0

PLD Input Terms

Address: 0x400F3280

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Bits	Name	Description
31	PLD1_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X

(continued)

25	PLD1_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
22	PLD0_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X

(continued)

3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X

36.1.182 UDB_P1_U1_PLD_IT1

PLD Input Terms

Address: 0x400F3284

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Bits	Name	Description
31	PLD1_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X

(continued)

25	PLD1_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
22	PLD0_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X

(continued)

3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X

36.1.183 UDB_P1_U1_PLD_IT2

PLD Input Terms

Address: 0x400F3288

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Bits	Name	Description
31	PLD1_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X

(continued)

25	PLD1_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
22	PLD0_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X

(continued)

3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X

36.1.184 UDB_P1_U1_PLD_IT3

PLD Input Terms

Address: 0x400F328C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Bits	Name	Description
31	PLD1_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X

(continued)

25	PLD1_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
22	PLD0_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X

(continued)

3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X

36.1.185 UDB_P1_U1_PLD_IT4

PLD Input Terms

Address: 0x400F3290

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Bits	Name	Description
31	PLD1_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X

(continued)

25	PLD1_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
22	PLD0_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X

(continued)

3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X

36.1.186 UDB_P1_U1_PLD_IT5

PLD Input Terms

Address: 0x400F3294

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Bits	Name	Description
31	PLD1_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X

(continued)

25	PLD1_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
22	PLD0_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X

(continued)

3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X

36.1.187 UDB_P1_U1_PLD_IT6

PLD Input Terms

Address: 0x400F3298

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Bits	Name	Description
31	PLD1_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X

(continued)

25	PLD1_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
22	PLD0_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X

(continued)

3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X

36.1.188 UDB_P1_U1_PLD_IT7

PLD Input Terms

Address: 0x400F329C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Bits	Name	Description
31	PLD1_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X

(continued)

25	PLD1_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
22	PLD0_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X

(continued)

3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X

36.1.189 UDB_P1_U1_PLD_IT8

PLD Input Terms

Address: 0x400F32A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Bits	Name	Description
31	PLD1_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X

(continued)

25	PLD1_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
22	PLD0_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X

(continued)

3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X

36.1.190 UDB_P1_U1_PLD_IT9

PLD Input Terms

Address: 0x400F32A4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Bits	Name	Description
31	PLD1_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X

(continued)

25	PLD1_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
22	PLD0_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X

(continued)

3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X

36.1.191 UDB_P1_U1_PLD_IT10

PLD Input Terms

Address: 0x400F32A8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Bits	Name	Description
31	PLD1_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X

(continued)

25	PLD1_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
22	PLD0_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X

(continued)

3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X

36.1.192 UDB_P1_U1_PLD_IT11

PLD Input Terms

Address: 0x400F32AC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxC_7	PLD0_ITxC_6	PLD0_ITxC_5	PLD0_ITxC_4	PLD0_ITxC_3	PLD0_ITxC_2	PLD0_ITxC_1	PLD0_ITxC_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxC_7	PLD1_ITxC_6	PLD1_ITxC_5	PLD1_ITxC_4	PLD1_ITxC_3	PLD1_ITxC_2	PLD1_ITxC_1	PLD1_ITxC_0

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ITxT_7	PLD0_ITxT_6	PLD0_ITxT_5	PLD0_ITxT_4	PLD0_ITxT_3	PLD0_ITxT_2	PLD0_ITxT_1	PLD0_ITxT_0

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ITxT_7	PLD1_ITxT_6	PLD1_ITxT_5	PLD1_ITxT_4	PLD1_ITxT_3	PLD1_ITxT_2	PLD1_ITxT_1	PLD1_ITxT_0

Bits	Name	Description
31	PLD1_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
30	PLD1_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
29	PLD1_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
28	PLD1_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
27	PLD1_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
26	PLD1_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X

(continued)

25	PLD1_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
24	PLD1_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
23	PLD0_ITxT_7	True input term. Bit position corresponds to product term. Default Value: X
22	PLD0_ITxT_6	True input term. Bit position corresponds to product term. Default Value: X
21	PLD0_ITxT_5	True input term. Bit position corresponds to product term. Default Value: X
20	PLD0_ITxT_4	True input term. Bit position corresponds to product term. Default Value: X
19	PLD0_ITxT_3	True input term. Bit position corresponds to product term. Default Value: X
18	PLD0_ITxT_2	True input term. Bit position corresponds to product term. Default Value: X
17	PLD0_ITxT_1	True input term. Bit position corresponds to product term. Default Value: X
16	PLD0_ITxT_0	True input term. Bit position corresponds to product term. Default Value: X
15	PLD1_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
14	PLD1_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
13	PLD1_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
12	PLD1_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X
11	PLD1_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
10	PLD1_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
9	PLD1_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
8	PLD1_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X
7	PLD0_ITxC_7	Complement input term. Bit position corresponds to product term Default Value: X
6	PLD0_ITxC_6	Complement input term. Bit position corresponds to product term Default Value: X
5	PLD0_ITxC_5	Complement input term. Bit position corresponds to product term Default Value: X
4	PLD0_ITxC_4	Complement input term. Bit position corresponds to product term Default Value: X

(continued)

3	PLD0_ITxC_3	Complement input term. Bit position corresponds to product term Default Value: X
2	PLD0_ITxC_2	Complement input term. Bit position corresponds to product term Default Value: X
1	PLD0_ITxC_1	Complement input term. Bit position corresponds to product term Default Value: X
0	PLD0_ITxC_0	Complement input term. Bit position corresponds to product term Default Value: X

36.1.193 UDB_P1_U1_PLD_ORT0

PLD OR Terms

Address: 0x400F32B0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ORT_PTx_7	PLD0_ORT_PTx_6	PLD0_ORT_PTx_5	PLD0_ORT_PTx_4	PLD0_ORT_PTx_3	PLD0_ORT_PTx_2	PLD0_ORT_PTx_1	PLD0_ORT_PTx_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ORT_PTx_7	PLD1_ORT_PTx_6	PLD1_ORT_PTx_5	PLD1_ORT_PTx_4	PLD1_ORT_PTx_3	PLD1_ORT_PTx_2	PLD1_ORT_PTx_1	PLD1_ORT_PTx_0

Bits	Name	Description
15	PLD1_ORT_PTx_7	OR term. Bit position corresponds to product term. Default Value: X
14	PLD1_ORT_PTx_6	OR term. Bit position corresponds to product term. Default Value: X
13	PLD1_ORT_PTx_5	OR term. Bit position corresponds to product term. Default Value: X
12	PLD1_ORT_PTx_4	OR term. Bit position corresponds to product term. Default Value: X
11	PLD1_ORT_PTx_3	OR term. Bit position corresponds to product term. Default Value: X
10	PLD1_ORT_PTx_2	OR term. Bit position corresponds to product term. Default Value: X
9	PLD1_ORT_PTx_1	OR term. Bit position corresponds to product term. Default Value: X
8	PLD1_ORT_PTx_0	OR term. Bit position corresponds to product term. Default Value: X
7	PLD0_ORT_PTx_7	OR term. Bit position corresponds to product term. Default Value: X
6	PLD0_ORT_PTx_6	OR term. Bit position corresponds to product term. Default Value: X
5	PLD0_ORT_PTx_5	OR term. Bit position corresponds to product term. Default Value: X
4	PLD0_ORT_PTx_4	OR term. Bit position corresponds to product term. Default Value: X

(continued)

3	PLD0_ORT_PTx_3	OR term. Bit position corresponds to product term. Default Value: X
2	PLD0_ORT_PTx_2	OR term. Bit position corresponds to product term. Default Value: X
1	PLD0_ORT_PTx_1	OR term. Bit position corresponds to product term. Default Value: X
0	PLD0_ORT_PTx_0	OR term. Bit position corresponds to product term. Default Value: X

36.1.194 UDB_P1_U1_PLD_ORT1

PLD OR Terms

Address: 0x400F32B2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ORT_PTx_7	PLD0_ORT_PTx_6	PLD0_ORT_PTx_5	PLD0_ORT_PTx_4	PLD0_ORT_PTx_3	PLD0_ORT_PTx_2	PLD0_ORT_PTx_1	PLD0_ORT_PTx_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ORT_PTx_7	PLD1_ORT_PTx_6	PLD1_ORT_PTx_5	PLD1_ORT_PTx_4	PLD1_ORT_PTx_3	PLD1_ORT_PTx_2	PLD1_ORT_PTx_1	PLD1_ORT_PTx_0

Bits	Name	Description
15	PLD1_ORT_PTx_7	OR term. Bit position corresponds to product term. Default Value: X
14	PLD1_ORT_PTx_6	OR term. Bit position corresponds to product term. Default Value: X
13	PLD1_ORT_PTx_5	OR term. Bit position corresponds to product term. Default Value: X
12	PLD1_ORT_PTx_4	OR term. Bit position corresponds to product term. Default Value: X
11	PLD1_ORT_PTx_3	OR term. Bit position corresponds to product term. Default Value: X
10	PLD1_ORT_PTx_2	OR term. Bit position corresponds to product term. Default Value: X
9	PLD1_ORT_PTx_1	OR term. Bit position corresponds to product term. Default Value: X
8	PLD1_ORT_PTx_0	OR term. Bit position corresponds to product term. Default Value: X
7	PLD0_ORT_PTx_7	OR term. Bit position corresponds to product term. Default Value: X
6	PLD0_ORT_PTx_6	OR term. Bit position corresponds to product term. Default Value: X
5	PLD0_ORT_PTx_5	OR term. Bit position corresponds to product term. Default Value: X
4	PLD0_ORT_PTx_4	OR term. Bit position corresponds to product term. Default Value: X

(continued)

3	PLD0_ORT_PTx_3	OR term. Bit position corresponds to product term. Default Value: X
2	PLD0_ORT_PTx_2	OR term. Bit position corresponds to product term. Default Value: X
1	PLD0_ORT_PTx_1	OR term. Bit position corresponds to product term. Default Value: X
0	PLD0_ORT_PTx_0	OR term. Bit position corresponds to product term. Default Value: X

36.1.195 UDB_P1_U1_PLD_ORT2

PLD OR Terms

Address: 0x400F32B4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ORT_PTx_7	PLD0_ORT_PTx_6	PLD0_ORT_PTx_5	PLD0_ORT_PTx_4	PLD0_ORT_PTx_3	PLD0_ORT_PTx_2	PLD0_ORT_PTx_1	PLD0_ORT_PTx_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ORT_PTx_7	PLD1_ORT_PTx_6	PLD1_ORT_PTx_5	PLD1_ORT_PTx_4	PLD1_ORT_PTx_3	PLD1_ORT_PTx_2	PLD1_ORT_PTx_1	PLD1_ORT_PTx_0

Bits	Name	Description
15	PLD1_ORT_PTx_7	OR term. Bit position corresponds to product term. Default Value: X
14	PLD1_ORT_PTx_6	OR term. Bit position corresponds to product term. Default Value: X
13	PLD1_ORT_PTx_5	OR term. Bit position corresponds to product term. Default Value: X
12	PLD1_ORT_PTx_4	OR term. Bit position corresponds to product term. Default Value: X
11	PLD1_ORT_PTx_3	OR term. Bit position corresponds to product term. Default Value: X
10	PLD1_ORT_PTx_2	OR term. Bit position corresponds to product term. Default Value: X
9	PLD1_ORT_PTx_1	OR term. Bit position corresponds to product term. Default Value: X
8	PLD1_ORT_PTx_0	OR term. Bit position corresponds to product term. Default Value: X
7	PLD0_ORT_PTx_7	OR term. Bit position corresponds to product term. Default Value: X
6	PLD0_ORT_PTx_6	OR term. Bit position corresponds to product term. Default Value: X
5	PLD0_ORT_PTx_5	OR term. Bit position corresponds to product term. Default Value: X
4	PLD0_ORT_PTx_4	OR term. Bit position corresponds to product term. Default Value: X

(continued)

3	PLD0_ORT_PTx_3	OR term. Bit position corresponds to product term. Default Value: X
2	PLD0_ORT_PTx_2	OR term. Bit position corresponds to product term. Default Value: X
1	PLD0_ORT_PTx_1	OR term. Bit position corresponds to product term. Default Value: X
0	PLD0_ORT_PTx_0	OR term. Bit position corresponds to product term. Default Value: X

36.1.196 UDB_P1_U1_PLD_ORT3

PLD OR Terms

Address: 0x400F32B6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_ORT_PTx_7	PLD0_ORT_PTx_6	PLD0_ORT_PTx_5	PLD0_ORT_PTx_4	PLD0_ORT_PTx_3	PLD0_ORT_PTx_2	PLD0_ORT_PTx_1	PLD0_ORT_PTx_0

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_ORT_PTx_7	PLD1_ORT_PTx_6	PLD1_ORT_PTx_5	PLD1_ORT_PTx_4	PLD1_ORT_PTx_3	PLD1_ORT_PTx_2	PLD1_ORT_PTx_1	PLD1_ORT_PTx_0

Bits	Name	Description
15	PLD1_ORT_PTx_7	OR term. Bit position corresponds to product term. Default Value: X
14	PLD1_ORT_PTx_6	OR term. Bit position corresponds to product term. Default Value: X
13	PLD1_ORT_PTx_5	OR term. Bit position corresponds to product term. Default Value: X
12	PLD1_ORT_PTx_4	OR term. Bit position corresponds to product term. Default Value: X
11	PLD1_ORT_PTx_3	OR term. Bit position corresponds to product term. Default Value: X
10	PLD1_ORT_PTx_2	OR term. Bit position corresponds to product term. Default Value: X
9	PLD1_ORT_PTx_1	OR term. Bit position corresponds to product term. Default Value: X
8	PLD1_ORT_PTx_0	OR term. Bit position corresponds to product term. Default Value: X
7	PLD0_ORT_PTx_7	OR term. Bit position corresponds to product term. Default Value: X
6	PLD0_ORT_PTx_6	OR term. Bit position corresponds to product term. Default Value: X
5	PLD0_ORT_PTx_5	OR term. Bit position corresponds to product term. Default Value: X
4	PLD0_ORT_PTx_4	OR term. Bit position corresponds to product term. Default Value: X

(continued)

3	PLD0_ORT_PTx_3	OR term. Bit position corresponds to product term. Default Value: X
2	PLD0_ORT_PTx_2	OR term. Bit position corresponds to product term. Default Value: X
1	PLD0_ORT_PTx_1	OR term. Bit position corresponds to product term. Default Value: X
0	PLD0_ORT_PTx_0	OR term. Bit position corresponds to product term. Default Value: X

36.1.197 UDB_P1_U1_PLD_MC_CFG_CEN_CONST

Macrocell configuration for Carry Enable and Constant

Address: 0x400F32B8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_MC3_DFF_C	PLD0_MC3_CEN	PLD0_MC2_DFF_C	PLD0_MC2_CEN	PLD0_MC1_DFF_C	PLD0_MC1_CEN	PLD0_MC0_DFF_C	PLD0_MC0_CEN

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_MC3_DFF_C	PLD1_MC3_CEN	PLD1_MC2_DFF_C	PLD1_MC2_CEN	PLD1_MC1_DFF_C	PLD1_MC1_CEN	PLD1_MC0_DFF_C	PLD1_MC0_CEN

Bits	Name	Description
15	PLD1_MC3_DFF_C	DFF Constant Default Value: X **0x0: NOINV:** DFF non-inverted **0x1: INVERTED:** DFF inverted
14	PLD1_MC3_CEN	Carry enable Default Value: X **0x0: DISABLE:** Disabled **0x1: ENABLE:** Enabled
13	PLD1_MC2_DFF_C	DFF Constant Default Value: X **0x0: NOINV:** DFF non-inverted **0x1: INVERTED:** DFF inverted
12	PLD1_MC2_CEN	Carry enable Default Value: X **0x0: DISABLE:** Disabled **0x1: ENABLE:** Enabled

(continued)

11	PLD1_MC1_DFF_C	DFF Constant Default Value: X **0x0: NOINV:** DFF non-inverted **0x1: INVERTED:** DFF inverted
10	PLD1_MC1_CEN	Carry enable Default Value: X **0x0: DISABLE:** Disabled **0x1: ENABLE:** Enabled
9	PLD1_MC0_DFF_C	DFF Constant Default Value: X **0x0: NOINV:** DFF non-inverted **0x1: INVERTED:** DFF inverted
8	PLD1_MC0_CEN	Carry enable Default Value: X **0x0: DISABLE:** Disabled **0x1: ENABLE:** Enabled
7	PLD0_MC3_DFF_C	DFF Constant Default Value: X **0x0: NOINV:** DFF non-inverted **0x1: INVERTED:** DFF inverted
6	PLD0_MC3_CEN	Carry enable Default Value: X **0x0: DISABLE:** Disabled **0x1: ENABLE:** Enabled
5	PLD0_MC2_DFF_C	DFF Constant Default Value: X **0x0: NOINV:** DFF non-inverted **0x1: INVERTED:** DFF inverted
4	PLD0_MC2_CEN	Carry enable Default Value: X

(continued)

		0x0: DISABLE: Disabled **0x1: ENABLE:** Enabled
3	PLD0_MC1_DFF_C	DFF Constant Default Value: X **0x0: NOINV:** DFF non-inverted **0x1: INVERTED:** DFF inverted
2	PLD0_MC1_CEN	Carry enable Default Value: X **0x0: DISABLE:** Disabled **0x1: ENABLE:** Enabled
1	PLD0_MC0_DFF_C	DFF Constant Default Value: X **0x0: NOINV:** DFF non-inverted **0x1: INVERTED:** DFF inverted
0	PLD0_MC0_CEN	Carry enable Default Value: X **0x0: DISABLE:** Disabled **0x1: ENABLE:** Enabled

36.1.198 UDB_P1_U1_PLD_MC_CFG_XORFB

PLD Macro cell XOR feedback

Address: 0x400F32BA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	PLD0_MC3_XORFB [7:6]		PLD0_MC2_XORFB [5:4]		PLD0_MC1_XORFB [3:2]		PLD0_MC0_XORFB [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	PLD1_MC3_XORFB [15:14]		PLD1_MC2_XORFB [13:12]		PLD1_MC1_XORFB [11:10]		PLD1_MC0_XORFB [9:8]	

Bits	Name	Description
15 : 14	PLD1_MC3_XORFB	XOR feedback Default Value: X **0x0: DFF:** DFF **0x1: CARRY:** Carry **0x2: TFF_H:** TFF on high **0x3: TFF_L:** TFF on low
13 : 12	PLD1_MC2_XORFB	XOR feedback Default Value: X **0x0: DFF:** DFF **0x1: CARRY:** Carry **0x2: TFF_H:** TFF on high **0x3: TFF_L:** TFF on low
11 : 10	PLD1_MC1_XORFB	XOR feedback Default Value: X **0x0: DFF:** DFF **0x1: CARRY:** Carry

(continued)

		0x2: TFF_H: TFF on high
		0x3: TFF_L: TFF on low
9 : 8	PLD1_MC0_XORFB	XOR feedback Default Value: X
		0x0: DFF: DFF
		0x1: CARRY: Carry
		0x2: TFF_H: TFF on high
		0x3: TFF_L: TFF on low
7 : 6	PLD0_MC3_XORFB	XOR feedback Default Value: X
		0x0: DFF: DFF
		0x1: CARRY: Carry
		0x2: TFF_H: TFF on high
		0x3: TFF_L: TFF on low
5 : 4	PLD0_MC2_XORFB	XOR feedback Default Value: X
		0x0: DFF: DFF
		0x1: CARRY: Carry
		0x2: TFF_H: TFF on high
		0x3: TFF_L: TFF on low
3 : 2	PLD0_MC1_XORFB	XOR feedback Default Value: X
		0x0: DFF: DFF
		0x1: CARRY: Carry
		0x2: TFF_H: TFF on high
		0x3: TFF_L: TFF on low

(continued)

1 : 0	PLD0_MC0_XORFB	XOR feedback Default Value: X **0x0: DFF:** DFF **0x1: CARRY:** Carry **0x2: TFF_H:** TFF on high **0x3: TFF_L:** TFF on low

36.1.199 UDB_P1_U1_PLD_MC_SET_RESET

PLD Macro cell Set Reset Selection

Address: 0x400F32BC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD0_MC3_RESET_SEL	PLD0_MC3_SET_SEL	PLD0_MC2_RESET_SEL	PLD0_MC2_SET_SEL	PLD0_MC1_RESET_SEL	PLD0_MC1_SET_SEL	PLD0_MC0_RESET_SEL	PLD0_MC0_SET_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	PLD1_MC3_RESET_SEL	PLD1_MC3_SET_SEL	PLD1_MC2_RESET_SEL	PLD1_MC2_SET_SEL	PLD1_MC1_RESET_SEL	PLD1_MC1_SET_SEL	PLD1_MC0_RESET_SEL	PLD1_MC0_SET_SEL

Bits	Name	Description
15	PLD1_MC3_RESET_SEL	Reset select enable Default Value: X **0x0: DISABLE:** Reset not used **0x1: ENABLE:** Reset enabled
14	PLD1_MC3_SET_SEL	Set select enable Default Value: X **0x0: DISABLE:** Set not used **0x1: ENABLE:** Set enabled
13	PLD1_MC2_RESET_SEL	Reset select enable Default Value: X **0x0: DISABLE:** Reset not used **0x1: ENABLE:** Reset enabled
12	PLD1_MC2_SET_SEL	Set select enable Default Value: X **0x0: DISABLE:** Set not used **0x1: ENABLE:** Set enabled

(continued)

11	PLD1_MC1_RESET_SEL	Reset select enable Default Value: X **0x0: DISABLE:** Reset not used **0x1: ENABLE:** Reset enabled
10	PLD1_MC1_SET_SEL	Set select enable Default Value: X **0x0: DISABLE:** Set not used **0x1: ENABLE:** Set enabled
9	PLD1_MC0_RESET_SEL	Reset select enable Default Value: X **0x0: DISABLE:** Reset not used **0x1: ENABLE:** Reset enabled
8	PLD1_MC0_SET_SEL	Set select enable Default Value: X **0x0: DISABLE:** Set not used **0x1: ENABLE:** Set enabled
7	PLD0_MC3_RESET_SEL	Reset select enable Default Value: X **0x0: DISABLE:** Reset not used **0x1: ENABLE:** Reset enabled
6	PLD0_MC3_SET_SEL	Set select enable Default Value: X **0x0: DISABLE:** Set not used **0x1: ENABLE:** Set enabled
5	PLD0_MC2_RESET_SEL	Reset select enable Default Value: X **0x0: DISABLE:** Reset not used **0x1: ENABLE:** Reset enabled
4	PLD0_MC2_SET_SEL	Set select enable Default Value: X

(continued)

		0x0: DISABLE: Set not used **0x1: ENABLE:** Set enabled
3	PLD0_MC1_RESET_SEL	Reset select enable Default Value: X **0x0: DISABLE:** Reset not used **0x1: ENABLE:** Reset enabled
2	PLD0_MC1_SET_SEL	Set select enable Default Value: X **0x0: DISABLE:** Set not used **0x1: ENABLE:** Set enabled
1	PLD0_MC0_RESET_SEL	Reset select enable Default Value: X **0x0: DISABLE:** Reset not used **0x1: ENABLE:** Reset enabled
0	PLD0_MC0_SET_SEL	Set select enable Default Value: X **0x0: DISABLE:** Set not used **0x1: ENABLE:** Set enabled

36.1.200 UDB_P1_U1_PLD_MC_CFG_BYPASS

PLD Macro cell Bypass control

Address: 0x400F32BE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	NC7	PLD0_MC3_BYPASS	NC5	PLD0_MC2_BYPASS	NC3	PLD0_MC1_BYPASS	NC1	PLD0_MC0_BYPASS

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	NC15	PLD1_MC3_BYPASS	NC13	PLD1_MC2_BYPASS	NC11	PLD1_MC1_BYPASS	NC9	PLD1_MC0_BYPASS

Bits	Name	Description
15	NC15	Spare register bit Default Value: X
14	PLD1_MC3_BYPASS	Bypass selection Default Value: X **0x0: REGISTER:** Registered output **0x1: COMBINATIONAL:** Combinational output
13	NC13	Spare register bit Default Value: X
12	PLD1_MC2_BYPASS	Bypass selection Default Value: X **0x0: REGISTER:** Registered output **0x1: COMBINATIONAL:** Combinational output
11	NC11	Spare register bit Default Value: X
10	PLD1_MC1_BYPASS	Bypass selection Default Value: X **0x0: REGISTER:** Registered output **0x1: COMBINATIONAL:** Combinational output

(continued)

9	NC9	Spare register bit Default Value: X
8	PLD1_MC0_BYPASS	Bypass selection Default Value: X **0x0: REGISTER:** Registered output **0x1: COMBINATIONAL:** Combinational output
7	NC7	Spare register bit Default Value: X
6	PLD0_MC3_BYPASS	Bypass selection Default Value: X **0x0: REGISTER:** Registered output **0x1: COMBINATIONAL:** Combinational output
5	NC5	Spare register bit Default Value: X
4	PLD0_MC2_BYPASS	Bypass selection Default Value: X **0x0: REGISTER:** Registered output **0x1: COMBINATIONAL:** Combinational output
3	NC3	Spare register bit Default Value: X
2	PLD0_MC1_BYPASS	Bypass selection Default Value: X **0x0: REGISTER:** Registered output **0x1: COMBINATIONAL:** Combinational output
1	NC1	Spare register bit Default Value: X
0	PLD0_MC0_BYPASS	Bypass selection Default Value: X **0x0: REGISTER:** Registered output **0x1: COMBINATIONAL:** Combinational output

36.1.201 UDB_P1_U1_CFG0

Datapath Input Selection - RAD1 RAD0. Address bits 0 and 1 to the dynamic configuration RAM

Address: 0x400F32C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	RAD1 [6:4]			None	RAD0 [2:0]		

Bits	Name	Description
6 : 4	RAD1	Datapath Permutable Input Mux Default Value: 0 **0x0: OFF:** Input off **0x1: DP_IN0:** Set to dp_in[0] **0x2: DP_IN1:** Set to dp_in[1] **0x3: DP_IN2:** Set to dp_in[2] **0x4: DP_IN3:** Set to dp_in[3] **0x5: DP_IN4:** Set to dp_in[4] **0x6: DP_IN5:** Set to dp_in[5] **0x7: RESERVED:** Reserved
2 : 0	RAD0	Datapath Permutable Input Mux Default Value: 0 **0x0: OFF:** Input off **0x1: DP_IN0:** Set to dp_in[0] **0x2: DP_IN1:** Set to dp_in[1] **0x3: DP_IN2:** Set to dp_in[2] **0x4: DP_IN3:** Set to dp_in[3] **0x5: DP_IN4:** Set to dp_in[4]

(continued)

0x6: DP_IN5:
Set to dp_in[5]

0x7: RESERVED:
Reserved

36.1.202 UDB_P1_U1_CFG1

Datapath Input Selection - RAD2. Address bit 2 to the dynamic configuration RAM

Address: 0x400F32C1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW		
HW Access	R	R	R	R	R	R		
Name	DP_RTE_BYPASS4	DP_RTE_BYPASS3	DP_RTE_BYPASS2	DP_RTE_BYPASS1	DP_RTE_BYPASS0	RAD2 [2:0]		

Bits	Name	Description
7	DP_RTE_BYPASS4	DP_In bypass control Default Value: 0 **0x0: DP_IN4_ROUTE:** Use dp_in[4] **0x1: DP_IN4_BYPASS:** Use dp_out[4] as input via bypass
6	DP_RTE_BYPASS3	DP_In bypass control Default Value: 0 **0x0: DP_IN3_ROUTE:** Use dp_in[3] **0x1: DP_IN3_BYPASS:** Use dp_out[3] as input via bypass
5	DP_RTE_BYPASS2	DP_In bypass control Default Value: 0 **0x0: DP_IN2_ROUTE:** Use dp_in[2] **0x1: DP_IN2_BYPASS:** Use dp_out[2] as input via bypass
4	DP_RTE_BYPASS1	DP_In bypass control Default Value: 0 **0x0: DP_IN1_ROUTE:** Use dp_in[1] **0x1: DP_IN1_BYPASS:** Use dp_out[1] as input via bypass
3	DP_RTE_BYPASS0	DP_In bypass control Default Value: 0 **0x0: DP_IN0_ROUTE:** Use dp_in[0] **0x1: DP_IN0_BYPASS:** Use dp_out[0] as input via bypass

(continued)

2 : 0	RAD2	Datapath Permutable Input Mux Default Value: 0 **0x0: OFF:** Input off **0x1: DP_IN0:** Set to dp_in[0] **0x2: DP_IN1:** Set to dp_in[1] **0x3: DP_IN2:** Set to dp_in[2] **0x4: DP_IN3:** Set to dp_in[3] **0x5: DP_IN4:** Set to dp_in[4] **0x6: DP_IN5:** Set to dp_in[5] **0x7: RESERVED:** Reserved

36.1.203 UDB_P1_U1_CFG2

Datapath Input Selection - F1_LD, F0_LD.

Address: 0x400F32C2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW			RW	RW		
HW Access	R	R			R	R		
Name	NC7	F1_LD [6:4]			DP_RTE_BYPASS5	F0_LD [2:0]		

Bits	Name	Description
7	NC7	Spare register bit Default Value: 0
6 : 4	F1_LD	Datapath Permutable Input Mux Default Value: 0 **0x0: OFF:** Input off **0x1: DP_IN0:** Set to dp_in[0] **0x2: DP_IN1:** Set to dp_in[1] **0x3: DP_IN2:** Set to dp_in[2] **0x4: DP_IN3:** Set to dp_in[3] **0x5: DP_IN4:** Set to dp_in[4] **0x6: DP_IN5:** Set to dp_in[5] **0x7: RESERVED:** Reserved
3	DP_RTE_BYPASS5	DP_In bypass control Default Value: 0 **0x0: DP_IN5_ROUTE:** Use dp_in[5] **0x1: DP_IN5_BYPASS:** Use dp_out[5] via bypass
2 : 0	F0_LD	Datapath Permutable Input Mux Default Value: 0 **0x0: OFF:** Input off

(continued)

0x1: DP_IN0:
Set to dp_in[0]

0x2: DP_IN1:
Set to dp_in[1]

0x3: DP_IN2:
Set to dp_in[2]

0x4: DP_IN3:
Set to dp_in[3]

0x5: DP_IN4:
Set to dp_in[4]

0x6: DP_IN5:
Set to dp_in[5]

0x7: RESERVED:
Reserved

36.1.204 UDB_P1_U1_CFG3

Datapath Input Selection - D1_LD, D0_LD.

Address: 0x400F32C3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	D1_LD [6:4]			None	D0_LD [2:0]		

Bits	Name	Description
6 : 4	D1_LD	Datapath Permutable Input Mux Default Value: 0 **0x0: OFF:** Input off **0x1: DP_IN0:** Set to dp_in[0] **0x2: DP_IN1:** Set to dp_in[1] **0x3: DP_IN2:** Set to dp_in[2] **0x4: DP_IN3:** Set to dp_in[3] **0x5: DP_IN4:** Set to dp_in[4] **0x6: DP_IN5:** Set to dp_in[5] **0x7: RESERVED:** Reserved
2 : 0	D0_LD	Datapath Permutable Input Mux Default Value: 0 **0x0: OFF:** Input off **0x1: DP_IN0:** Set to dp_in[0] **0x2: DP_IN1:** Set to dp_in[1] **0x3: DP_IN2:** Set to dp_in[2] **0x4: DP_IN3:** Set to dp_in[3] **0x5: DP_IN4:** Set to dp_in[4]

(continued)

0x6: DP_IN5:
Set to dp_in[5]

0x7: RESERVED:
Reserved

36.1.205 UDB_P1_U1_CFG4

Datapath Input Selection - CI_MUX SI_MUX.

Address: 0x400F32C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	CI_MUX [6:4]			None	SI_MUX [2:0]		

Bits	Name	Description
6 : 4	CI_MUX	Datapath Permutable Input Mux Default Value: 0 **0x0: OFF:** Input off **0x1: DP_IN0:** Set to dp_in[0] **0x2: DP_IN1:** Set to dp_in[1] **0x3: DP_IN2:** Set to dp_in[2] **0x4: DP_IN3:** Set to dp_in[3] **0x5: DP_IN4:** Set to dp_in[4] **0x6: DP_IN5:** Set to dp_in[5] **0x7: RESERVED:** Reserved
2 : 0	SI_MUX	Datapath Permutable Input Mux Default Value: 0 **0x0: OFF:** Input off **0x1: DP_IN0:** Set to dp_in[0] **0x2: DP_IN1:** Set to dp_in[1] **0x3: DP_IN2:** Set to dp_in[2] **0x4: DP_IN3:** Set to dp_in[3] **0x5: DP_IN4:** Set to dp_in[4]

(continued)

0x6: DP_IN5:
Set to dp_in[5]

0x7: RESERVED:
Reserved

36.1.206 UDB_P1_U1_CFG5

Datapath Output Selection for OUT1 OUT0

Address: 0x400F32C5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	OUT1 [7:4]				OUT0 [3:0]			

Bits	Name	Description
7 : 4	OUT1	Datapath Permutable Output Mux Default Value: 0 **0x0: CE0:** Comparator 0 equal **0x1: CL0:** Comparator 0 less than **0x2: Z0:** Accumulator 0 zero detect **0x3: FF0:** Accumulator 0 ones detect **0x4: CE1:** Comparator 1 equal **0x5: CL1:** Comparator 1 less than **0x6: Z1:** Accumulator 1 zero detect **0x7: FF1:** Accumulator 1 ones detect **0x8: OV_MSB:** Overflow of MSB **0x9: CO_MSB:** Carry out of MSB **0xa: CMSBO:** CRC MSB **0xb: SO:** Shift out **0xc: F0_BLK_STAT:** FIFO 0 block status defined by direction **0xd: F1_BLK_STAT:** FIFO 1 block status defined by direction **0xe: F0_BUS_STAT:** FIFO 0 bus status defined by direction and level

(continued)

		0xf: F1_BUS_STAT: FIFO 1 bus status defined by direction and level
3 : 0	OUT0	Datapath Permutable Output Mux Default Value: 0 **0x0: CE0:** Comparator 0 equal **0x1: CL0:** Comparator 0 less than **0x2: Z0:** Accumulator 0 zero detect **0x3: FF0:** Accumulator 0 ones detect **0x4: CE1:** Comparator 1 equal **0x5: CL1:** Comparator 1 less than **0x6: Z1:** Accumulator 1 zero detect **0x7: FF1:** Accumulator 1 ones detect **0x8: OV_MSB:** Overflow of MSB **0x9: CO_MSB:** Carry out of MSB **0xa: CMSBO:** CRC MSB **0xb: SO:** Shift out **0xc: F0_BLK_STAT:** FIFO 0 block status defined by direction **0xd: F1_BLK_STAT:** FIFO 1 block status defined by direction **0xe: F0_BUS_STAT:** FIFO 0 bus status defined by direction and level **0xf: F1_BUS_STAT:** FIFO 1 bus status defined by direction and level

36.1.207 UDB_P1_U1_CFG6

Datapath Output Selection for OUT3 OUT2

Address: 0x400F32C6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	OUT3 [7:4]				OUT2 [3:0]			

Bits	Name	Description
7 : 4	OUT3	Datapath Permutable Output Mux Default Value: 0 **0x0: CE0:** Comparator 0 equal **0x1: CL0:** Comparator 0 less than **0x2: Z0:** Accumulator 0 zero detect **0x3: FF0:** Accumulator 0 ones detect **0x4: CE1:** Comparator 1 equal **0x5: CL1:** Comparator 1 less than **0x6: Z1:** Accumulator 1 zero detect **0x7: FF1:** Accumulator 1 ones detect **0x8: OV_MSB:** Overflow of MSB **0x9: CO_MSB:** Carry out of MSB **0xa: CMSBO:** CRC MSB **0xb: SO:** Shift out **0xc: F0_BLK_STAT:** FIFO 0 block status defined by direction **0xd: F1_BLK_STAT:** FIFO 1 block status defined by direction **0xe: F0_BUS_STAT:** FIFO 0 bus status defined by direction and level

(continued)

		0xf: F1_BUS_STAT: FIFO 1 bus status defined by direction and level
3 : 0	OUT2	Datapath Permutable Output Mux Default Value: 0 **0x0: CE0:** Comparator 0 equal **0x1: CL0:** Comparator 0 less than **0x2: Z0:** Accumulator 0 zero detect **0x3: FF0:** Accumulator 0 ones detect **0x4: CE1:** Comparator 1 equal **0x5: CL1:** Comparator 1 less than **0x6: Z1:** Accumulator 1 zero detect **0x7: FF1:** Accumulator 1 ones detect **0x8: OV_MSB:** Overflow of MSB **0x9: CO_MSB:** Carry out of MSB **0xa: CMSBO:** CRC MSB **0xb: SO:** Shift out **0xc: F0_BLK_STAT:** FIFO 0 block status defined by direction **0xd: F1_BLK_STAT:** FIFO 1 block status defined by direction **0xe: F0_BUS_STAT:** FIFO 0 bus status defined by direction and level **0xf: F1_BUS_STAT:** FIFO 1 bus status defined by direction and level

36.1.208 UDB_P1_U1_CFG7

Datapath Output Selection for OUT5 OUT4

Address: 0x400F32C7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	OUT5 [7:4]				OUT4 [3:0]			

Bits	Name	Description
7 : 4	OUT5	Datapath Permutable Output Mux Default Value: 0 **0x0: CE0:** Comparator 0 equal **0x1: CL0:** Comparator 0 less than **0x2: Z0:** Accumulator 0 zero detect **0x3: FF0:** Accumulator 0 ones detect **0x4: CE1:** Comparator 1 equal **0x5: CL1:** Comparator 1 less than **0x6: Z1:** Accumulator 1 zero detect **0x7: FF1:** Accumulator 1 ones detect **0x8: OV_MSB:** Overflow of MSB **0x9: CO_MSB:** Carry out of MSB **0xa: CMSBO:** CRC MSB **0xb: SO:** Shift out **0xc: F0_BLK_STAT:** FIFO 0 block status defined by direction **0xd: F1_BLK_STAT:** FIFO 1 block status defined by direction **0xe: F0_BUS_STAT:** FIFO 0 bus status defined by direction and level

(continued)

		0xf: F1_BUS_STAT: FIFO 1 bus status defined by direction and level
3 : 0	OUT4	Datapath Permutable Output Mux Default Value: 0 **0x0: CE0:** Comparator 0 equal **0x1: CL0:** Comparator 0 less than **0x2: Z0:** Accumulator 0 zero detect **0x3: FF0:** Accumulator 0 ones detect **0x4: CE1:** Comparator 1 equal **0x5: CL1:** Comparator 1 less than **0x6: Z1:** Accumulator 1 zero detect **0x7: FF1:** Accumulator 1 ones detect **0x8: OV_MSB:** Overflow of MSB **0x9: CO_MSB:** Carry out of MSB **0xa: CMSBO:** CRC MSB **0xb: SO:** Shift out **0xc: F0_BLK_STAT:** FIFO 0 block status defined by direction **0xd: F1_BLK_STAT:** FIFO 1 block status defined by direction **0xe: F0_BUS_STAT:** FIFO 0 bus status defined by direction and level **0xf: F1_BUS_STAT:** FIFO 1 bus status defined by direction and level

36.1.209 UDB_P1_U1_CFG8

Datapath Output Synchronization Option

Address: 0x400F32C8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW					
HW Access	R	R	R					
Name	NC7	NC6	OUT_SYNC [5:0]					

Bits	Name	Description
7	NC7	Spare register bit Default Value: 0
6	NC6	Spare register bit Default Value: 0
5 : 0	OUT_SYNC	Datapath Output Synchronization. Each datapath output can be registered (default,0), or combinational (1) Default Value: 0 **0x0: REGISTERED:** registered **0x1: COMBINATIONAL:** combinational

36.1.210 UDB_P1_U1_CFG9

Datapath ALU Mask

Address: 0x400F32C9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	AMASK [7:0]							

Bits	Name	Description
7 : 0	AMASK	Datapath ALU Mask. The mask value in this register is applied to the output of the Datapath ALU result before the result is stored. The AMASK_EN bit (CFG12) must be set for the mask to be operational. Default Value: 0

36.1.211 UDB_P1_U1_CFG10

Datapath Compare 0 Mask

Address: 0x400F32CA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CMASK0 [7:0]							

Bits	Name	Description
7 : 0	CMASK0	Datapath Compare 0 Mask. The mask value in this register is applied to the output of the Accumulator 0 before it is used for comparison in Compare block 0. The CMASK0_EN bit (CFG12) must be set for the mask to be operational. Default Value: 0

36.1.212 UDB_P1_U1_CFG11

Datapath Compare 1 Mask

Address: 0x400F32CB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CMASK0 [7:0]							

Bits	Name	Description
7 : 0	CMASK0	Datapath Compare 1 Mask. The mask value in this register is applied to the selected Compare 1 block input (Accumulator 0 or Accumulator 1) before it is used for comparison. The CMASK1_EN bit (CFG12) must be set for the mask to be operational. Default Value: 0

36.1.213 UDB_P1_U1_CFG12

Datapath mask enables and shift in configuration

Address: 0x400F32CC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW		RW	
HW Access	R	R	R	R	R		R	
Name	CMASK1_EN	CMASK0_EN	AMASK_EN	DEF_SI	SI_SELB [3:2]		SI_SELA [1:0]	

Bits	Name	Description
7	CMASK1_EN	Datapath mask enable Default Value: 0 **0x0: DISABLE:** Masking disabled **0x1: ENABLE:** Masking enabled
6	CMASK0_EN	Datapath mask enable Default Value: 0 **0x0: DISABLE:** Masking disabled **0x1: ENABLE:** Masking enabled
5	AMASK_EN	Datapath mask enable Default Value: 0 **0x0: DISABLE:** Masking disabled **0x1: ENABLE:** Masking enabled
4	DEF_SI	Datapath default shift value Default Value: 0 **0x0: DEFAULT_0:** Default shift is 0 **0x1: DEFAULT_1:** Default shift is 1
3 : 2	SI_SELB	Datapath shift in source select Default Value: 0 **0x0: DEFAULT:** Default value specified in default shift field **0x1: REGISTERED:** Shift in is the shift out registered from previous cycle

(continued)

		0x2: ROUTE: Shift in is selected from datapath routing input **0x3: CHAIN:** Shift in is chained from the previous datapath
1 : 0	SI_SELA	Datapath shift in source select Default Value: 0 **0x0: DEFAULT:** Default value specified in default shift field **0x1: REGISTERED:** Shift in is the shift out registered from previous cycle **0x2: ROUTE:** Shift in is selected from datapath routing input **0x3: CHAIN:** Shift in is chained from the previous datapath

36.1.214 UDB_P1_U1_CFG13

Datapath carry in and compare configuration

Address: 0x400F32CD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	CMP_SELB [7:6]		CMP_SELA [5:4]		CI_SELB [3:2]		CI_SELA [1:0]	

Bits	Name	Description
7 : 6	CMP_SELB	Datapath compare select Default Value: 0 **0x0: A1_D1:** Compare A1 to D1 **0x1: A1_A0:** Compare A1 to A0 **0x2: A0_D1:** Compare A0 to D1 **0x3: A0_A0:** Compare A0 to A0
5 : 4	CMP_SELA	Datapath compare select Default Value: 0 **0x0: A1_D1:** Compare A1 to D1 **0x1: A1_A0:** Compare A1 to A0 **0x2: A0_D1:** Compare A0 to D1 **0x3: A0_A0:** Compare A0 to A0
3 : 2	CI_SELB	Datapath carry in source select Default Value: 0 **0x0: DEFAULT:** Default arithmetic mode **0x1: REGISTERED:** Carry in is the carry out registered from previous cycle **0x2: ROUTE:** Carry in is selected from datapath routing input **0x3: CHAIN:** Carry in is chained from the previous datapath
1 : 0	CI_SELA	Datapath carry in source select Default Value: 0

(continued)

0x0: DEFAULT:
Default arithmetic mode

0x1: REGISTERED:
Carry in is the carry out registered from previous cycle

0x2: ROUTE:
Carry in is selected from datapath routing input

0x3: CHAIN:
Carry in is chained from the previous datapath

36.1.215 UDB_P1_U1_CFG14

Datapath chaining and MSB configuration

Address: 0x400F32CE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW			RW	RW	RW	RW
HW Access	R	R			R	R	R	R
Name	MSB_EN	MSB_SEL [6:4]			CHAIN_CMSB	CHAIN_FB	CHAIN1	CHAIN0

Bits	Name	Description
7	MSB_EN	Datapath MSB selection enable Default Value: 0 **0x0: DISABLE:** MSB selection is disabled, MSB is bit 7 **0x1: ENABLE:** MSB selection is controlled by MSB_SEL
6 : 4	MSB_SEL	Datapath MSB Selection Default Value: 0 **0x0: BIT0:** MSB is bit 0 **0x1: BIT1:** MSB is bit 1 **0x2: BIT2:** MSB is bit 2 **0x3: BIT3:** MSB is bit 3 **0x4: BIT4:** MSB is bit 4 **0x5: BIT5:** MSB is bit 5 **0x6: BIT6:** MSB is bit 6 **0x7: BIT7:** MSB is bit 7 - equivalent to MSB_EN=0
3	CHAIN_CMSB	Datapath CRC MSB chaining enable Default Value: 0 **0x0: DISABLE:** CRC MSB is not chained **0x1: ENABLE:** CRC MSB is chained from the next (MSB) datapath

(continued)

2	CHAIN_FB	Datapath CRC feedback chaining enable Default Value: 0 **0x0: DISABLE:** CRC feedback is not chained **0x1: ENABLE:** CRC feedback is chained from the previous (LSB) datapath
1	CHAIN1	Datapath condition chaining enable Default Value: 0 **0x0: DISABLE:** Conditions are not chained **0x1: ENABLE:** Conditions are chained from the previous (LSB) datapath
0	CHAIN0	Datapath condition chaining enable Default Value: 0 **0x0: DISABLE:** Conditions are not chained **0x1: ENABLE:** Conditions are chained from the previous (LSB) datapath

36.1.216 UDB_P1_U1_CFG15

Datapath FIFO, shift and parallel input control

Address: 0x400F32CF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW		RW	
HW Access	R	R	R	R	R		R	
Name	PI_SEL	SHIFT_SEL	PI_DYN	MSB_SI	F1_INSEL [3:2]		F0_INSEL [1:0]	

Bits	Name	Description
7	PI_SEL	Datapath parallel input selection Default Value: 0 **0x0: NORMAL:** Normal operation, ALU source is from accumulator selection **0x1: PARALLEL:** ALU source A input is from the parallel data input
6	SHIFT_SEL	Datapath shift out selection Default Value: 0 **0x0: SOL_MSB:** Routed shift out is shift out left (sol_msb) **0x1: SOR:** Routed shift out is shift out right (sor)
5	PI_DYN	Enable for dynamic control of parallel data input (PI) mux. Default Value: 0 **0x0: DISABLE:** Parallel input mux select is only controlled by static configuration (PI_SEL). **0x1: ENABLE:** Parallel input mux to the Datapath is controlled by CFB_EN field in Datapath Dynamic RAM. When this mode is enabled, the CFB_EN usage for CRC/PRS functionality is disabled.
4	MSB_SI	Arithmetic shift right operation shift in selection Default Value: 0 **0x0: DEFAULT:** Shift in default value (when SI_SELA and/or SI_SELB == 0) **0x1: MSB:** Override default and shift in MSB value
3 : 2	F1_INSEL	Datapath FIFO Configuration Default Value: 0 **0x0: INPUT:** Input Mode: Write source is the system bus; read destination is corresponding data register or accumulator **0x1: OUTPUT_A0:** Output Mode: Write source is A0, read destination is the system bus

(continued)

		0x2: OUTPUT_A1: Output Mode: Write source is A1, read destination is the system bus **0x3: OUTPUT_ALU:** Output Mode: Write source is the ALU output, read destination is the system bus
1 : 0	F0_INSEL	Datapath FIFO Configuration Default Value: 0 **0x0: INPUT:** Input Mode: Write source is the system bus; read destination is corresponding data register or accumulator **0x1: OUTPUT_A0:** Output Mode: Write source is A0, read destination is the system bus **0x2: OUTPUT_A1:** Output Mode: Write source is A1, read destination is the system bus **0x3: OUTPUT_ALU:** Output Mode: Write source is the ALU output, read destination is the system bus

36.1.217 UDB_P1_U1_CFG16

Datapath FIFO and register access configuration control

Address: 0x400F32D0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	F1_CK_INV	F0_CK_INV	FIFO_FAST	FIFO_CAP	FIFO_EDGE	FIFO_ASYNC	EXT_CRCPRS	WRK16_CONCAT

Bits	Name	Description
7	F1_CK_INV	FIFO Clock Invert. When this bit is set, the polarity of the clock for the given FIFO will be inverted, with respect to the polarity of the selected Datapath clock. Default Value: 0 **0x0: NORMAL:** FIFO clock is the same polarity as the Datapath clock. **0x1: INVERT:** FIFO clock is inverted with respect to the Datapath clock.
6	F0_CK_INV	FIFO Clock Invert. When this bit is set, the polarity of the clock for the given FIFO will be inverted, with respect to the polarity of the selected Datapath clock. Default Value: 0 **0x0: NORMAL:** FIFO clock is the same polarity as the Datapath clock. **0x1: INVERT:** FIFO clock is inverted with respect to the Datapath clock.
5	FIFO_FAST	FIFO Fast Mode. When this bit is set, the FIFO write logic is clocked by the application bus clock. Lowers the latency of capture timing, at the expense of additional power. Default Value: 0 **0x0: DISABLE:** FIFO is clocked with selected Datapath clock. **0x1: ENABLE:** FIFO is clocked with application bus clock. Master and quadrant bus clock gating must be enabled.
4	FIFO_CAP	FIFO Software Capture Mode. When this bit is set, a read of A0 or A1 triggers a capture into F0 or F1 respectively. This function follows the chaining configuration. All accumulators in the chain from a given block to the MS block in the chain are capture Default Value: 0 **0x0: DISABLE:** FIFO capture is disabled. **0x1: ENABLE:** FIFO capture is enabled (FIFO must be in output mode). A read of A0 or A1 will write into F0 or F1.
3	FIFO_EDGE	Edge/level sensitive FIFO write control (Fx_LD). Only applies to FIFO configured in output mode Default Value: 0

(continued)

		0x0: LEVEL: FIFO write from accumulators/ALU is level sensitive. FIFO write occurs on a clock edge whenever the write control is sampled high on that edge. **0x1: EDGE:** FIFO write from accumulators/ALU is edge sensitive. FIFO write occurs on a clock edge folloing a 0 to 1 transition on the write control. The write control must be negated for at least one full cycle of the FIFO clock for a subsequent transition to be dete
2	FIFO_ASYNC	Asynchronous FIFO clocking support Default Value: 0 **0x0: DISABLE:** FIFO clocks are synchronous **0x1: ENABLE:** FIFO clocks are asynchronous
1	EXT_CRCPRS	External CRC/PRS mode Default Value: 0 **0x0: INTERNAL:** Internal CRC/PRS routing **0x1: EXTERNAL:** External CRC/PRS routing
0	WRK16_CONCAT	Datapath register access mode Default Value: 0 **0x0: DEFAULT:** 16-bit default access mode: selects registers in two consecutive UDBs in chaining order **0x1: CONCATENATE:** 16-bit concat access mode: selects concatenated registers in a single UDB

36.1.218 UDB_P1_U1_CFG17

Datapath FIFO control

Address: 0x400F32D1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			R	R	R	R	R
Name	None [7:5]			FIFO_ADD_SYNC	NC3	NC2	F1_DYN	F0_DYN

Bits	Name	Description
4	FIFO_ADD_SYNC	Adds an additional sync flip-flop to FIFO block status. Default Value: 0 **0x0: DISABLE:** Compatible Mode: FIFO block status sync configuration is 'none' (FIFO_ASYNC = 0) and 1 sync flip-flop (FIFO_ASYNC = 1) **0x1: ENABLE:** Add Sync Mode: FIFO block status sync configuration 1 sync flip-flop (FIFO_ASYNC = 0) and 2 sync flip-flops (FIFO_ASYNC = 1)
3	NC3	Spare register bit Default Value: 0
2	NC2	Spare register bit Default Value: 0
1	F1_DYN	Default Value: 0 **0x0: STATIC:** Default. FIFO direction is static and controlled by the associated Fx_INSEL bits (CFG15). **0x1: DYNAMIC:** The associated FIFO direction is dynamically controlled by the associated 'dx_load' Datapath input signal. When the 'dx_load' signal is '0', the access is internal, where the FIFO is both a source for the Datapath, and a destination for the Datapath (dest
0	F0_DYN	When this bit is set, the associated FIFO configuration may be dynamically controlled. Default Value: 0 **0x0: STATIC:** Default. FIFO direction is static and controlled by the associated Fx_INSEL bits (CFG15). **0x1: DYNAMIC:** The associated FIFO direction is dynamically controlled by the associated 'dx_load' Datapath input signal. When the 'dx_load' signal is '0', the access is internal, where the FIFO is both a source for the Datapath, and a destination for the Datapath (dest

36.1.219 UDB_P1_U1_CFG18

Control Register Mode 0 (used in conjunction with Control Register Mode 1)

Address: 0x400F32D2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CTL_MD0 [7:0]							

Bits	Name	Description
7 : 0	CTL_MD0	CTL_MD1 and CTL_MD0 are concatenated to form an encoding for the mode of each control bit in the control register. Default Value: 0 **0x0: DIRECT:** The value written to that bit drives directly into the routing. **0x1: SYNC:** The value written is resampled by the selected SC clock. The resampled value is driven into the routing. **0x2: DOUBLE_SYNC:** The value written is doubly synced by the selected SC clock. The synched value is driven into the routing. **0x3: PULSE:** The value written is resampled and a synchronous pulse is generated and driven into the routing based on the selected SC clock. At the end of the generated pulse, the control register bit is automatically reset.

36.1.220 UDB_P1_U1_CFG19

Control Register Mode 1 (used in conjunction with Control Register Mode 0)

Address: 0x400F32D3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CTL_MD1 [7:0]							

Bits	Name	Description
7 : 0	CTL_MD1	CTL_MD1 and CTL_MD0 are concatenated to form an encoding for the mode of each control bit in the control register. Default Value: 0 **0x0: DIRECT:** The value written to that bit drives directly into the routing. **0x1: SYNC:** The value written is resampled by the selected SC clock. The resampled value is driven into the routing. **0x2: DOUBLE_SYNC:** The value written is doubly synced by the selected SC clock. The synched value is driven into the routing. **0x3: PULSE:** The value written is resampled and a synchronous pulse is generated and driven into the routing based on the selected SC clock. At the end of the generated pulse, the control register bit is automatically reset.

36.1.221 UDB_P1_U1_CFG20

Status Register input mode selection

Address: 0x400F32D4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	STAT_MD [7:0]							

Bits	Name	Description
7 : 0	STAT_MD	Mode selection for each bit of the status register. A '0' is transparent mode, where internal routing is read idrectly by CPU firmware. A '1' is sticky-clear-on-read mode, where once the given bit is set, it will stay set until the CPU reads the bit. Default Value: 0

36.1.222 UDB_P1_U1_CFG21

Spare register bits

Address: 0x400F32D5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						NC1	NC0

Bits	Name	Description
1	NC1	Spare register bit Default Value: 0
0	NC0	Spare register bit Default Value: 0

36.1.223 UDB_P1_U1_CFG22

SC block configuration control

Address: 0x400F32D6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW	RW	RW	
HW Access	None			R	R	R	R	
Name	None [7:5]			SC_EXT_RES	SC_SYNC_MD	SC_INT_MD	SC_OUT_CTL [1:0]	

Bits	Name	Description
4	SC_EXT_RES	Control register external reset operation. This bit supports autonomous usage of the control register, where a routed reset should clear the writable input registers. By default this is off because the CPU writable register can be cleared in firmware. Default Value: 0 **0x0: DISABLED:** When a routed reset is applied to the control register, only embedded state (sampling registers) are cleared **0x1: ENABLED:** When a routed reset is applied to the control register, all state is cleared, including the CPU writable control bits.
3	SC_SYNC_MD	SC Sync Mode - controls when the status register operates as a 4-bit double synchronizer module Default Value: 0 **0x0: NORMAL:** Normal Mode - Status register operation **0x1: SYNC_MODE:** Sync Mode - Routing inputs sc_in[3:0] are the 4 sync inputs, and connections sc_io[3:0] operate as the sync outputs
2	SC_INT_MD	SC Interrupt Mode - controls when the UDB driving an interrupt generated from the masked OR reduction of status bits 6 to 0 Default Value: 0 **0x0: NORMAL:** Normal Mode - Routing connection sc_io[3] is a normal input to the status register **0x1: INT_MODE:** Interrupt Mode - Routing connection sc_io[3] operates as the UDB interrupt output
1 : 0	SC_OUT_CTL	Selects the output source for the Status and Control routing connections Default Value: 0 **0x0: CONTROL:** Control out, 8-bits of control are driven to the routing connections **0x1: PARALLEL:** Datapath parallel output, 8-bits of datapath parallel output data are driven to the routing connections

(continued)

0x2: COUNTER:
Counter out, 7-bits of count and 1 bit (MSB) of terminal count are driven to the routing connections

0x3: RESERVED:
Reserved

36.1.224 UDB_P1_U1_CFG23

Counter Control

Address: 0x400F32D7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	RW	RW	RW		RW	
HW Access	None	R	R	R	R		R	
Name	None	ALT_CNT	ROUTE_EN	ROUTE_LD	CNT_EN_SEL [3:2]		CNT_LD_SEL [1:0]	

Bits	Name	Description
6	ALT_CNT	Configure the alternate operating mode of the counter Default Value: 0 **0x0: DEFAULT_MODE:** Default counter operating mode **0x1: ALT_MODE:** Alternate counter operating mode
5	ROUTE_EN	Configure the counter enable signal for routing input Default Value: 0 **0x0: DISABLE:** Routed EN signal is not used. EN signal is only controlled by firmware CNT START (ACTL register) **0x1: ROUTED:** Routed EN signal is used, CNT START must be set
4	ROUTE_LD	Configure the counter load signal for routing input Default Value: 0 **0x0: DISABLE:** Routed LD signal is not used **0x1: ROUTED:** Routed LD signal is used
3 : 2	CNT_EN_SEL	Selects the routing inputs for the counter enable signal Default Value: 0 **0x0: SC_IN4:** sc_io_in[0] **0x1: SC_IN5:** sc_io_in[1] **0x2: SC_IN6:** sc_io_in[2] **0x3: SC_IO:** sc_io_in[3]
1 : 0	CNT_LD_SEL	Selects the routing inputs for the counter load signal Default Value: 0

(continued)

0x0: SC_IN0:
sc_in[0]

0x1: SC_IN1:
sc_in[1]

0x2: SC_IN2:
sc_in[2]

0x3: SC_IN3:
sc_in[3]

36.1.225 UDB_P1_U1_CFG24

PLD0 Clock and Reset control

Address: 0x400F32D8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW		RW	
HW Access	R	R	R	R	R		R	
Name	RC_RES_SEL1	RC_RES_SEL0_OR_FRES	RC_INV	RC_EN_INV	RC_EN_MODE [3:2]		RC_EN_SEL [1:0]	

Bits	Name	Description
7	RC_RES_SEL1	Configures the routed reset for the associated UDB component block. The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES = '0' - This bit is not used. When ALT RES = '1' - The bits {RC_SEL1,RC_SEL0_OR_FRES} select the RC routing for routed reset control according to the following: 00 : rc_in [0] 01 : rc_in [1] 10 : rc_in [2] 11 : rc_in [3] Default Value: 0
6	RC_RES_SEL0_OR_FRES	Configures the routed or firmware reset for the associated UDB component block. The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES = '0' - This bit is a firmware reset. When ALT RES = '1' - The bits {RC_SEL1,RC_SEL0_OR_FRES} select the RC routing for routed reset control according to the following: 00 : rc_in [0] 01 : rc_in [1] 10 : rc_in [2] 11 : rc_in [3] Default Value: 0
5	RC_INV	Optionally inverts the clock selection for the associated UDB component block. Default Value: 0 **0x0: NOINV:** Non-inverted **0x1: INVERT:** Inverted
4	RC_EN_INV	Optionally inverts the clock enable selection for the associated UDB component blocks. Default Value: 0 **0x0: NOINV:** Non-inverted **0x1: INVERT:** Inverted
3 : 2	RC_EN_MODE	Selects the operating mode for the clock to the associated UDB component block. Default Value: 0

(continued)

		0x0: OFF: Always off **0x1: ON:** Always on **0x2: POSEDGE:** Positive edge **0x3: LEVEL:** Level sensitive
1 : 0	RC_EN_SEL	Selects channel route for enable control to the associated UDB component block Default Value: 0 **0x0: RC_IN0:** rc_in[0] **0x1: RC_IN1:** rc_in[1] **0x2: RC_IN2:** rc_in[2] **0x3: RC_IN3:** rc_in[3]

36.1.226 UDB_P1_U1_CFG25

PLD1 Clock and Reset control

Address: 0x400F32D9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW		RW	
HW Access	R	R	R	R	R		R	
Name	RC_RES_SEL1	RC_RES_SEL0_OR_FRES	RC_INV	RC_EN_INV	RC_EN_MODE [3:2]		RC_EN_SEL [1:0]	

Bits	Name	Description
7	RC_RES_SEL1	Configures the routed reset for the associated UDB component block. The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES = '0' - This bit is not used. When ALT RES = '1' - The bits {RC_SEL1,RC_SEL0_OR_FRES} select the RC routing for routed reset control according to the following: 00 : rc_in [0] 01 : rc_in [1] 10 : rc_in [2] 11 : rc_in [3] Default Value: 0
6	RC_RES_SEL0_OR_FRES	Configures the routed or firmware reset for the associated UDB component block. The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES = '0' - This bit is a firmware reset. When ALT RES = '1' - The bits {RC_SEL1,RC_SEL0_OR_FRES} select the RC routing for routed reset control according to the following: 00 : rc_in [0] 01 : rc_in [1] 10 : rc_in [2] 11 : rc_in [3] Default Value: 0
5	RC_INV	Optionally inverts the clock selection for the associated UDB component block. Default Value: 0 **0x0: NOINV:** Non-inverted **0x1: INVERT:** Inverted
4	RC_EN_INV	Optionally inverts the clock enable selection for the associated UDB component blocks. Default Value: 0 **0x0: NOINV:** Non-inverted **0x1: INVERT:** Inverted
3 : 2	RC_EN_MODE	Selects the operating mode for the clock to the associated UDB component block. Default Value: 0

(continued)

		0x0: OFF: Always off **0x1: ON:** Always on **0x2: POSEDGE:** Positive edge **0x3: LEVEL:** Level sensitive
1 : 0	RC_EN_SEL	Selects channel route for enable control to the associated UDB component block Default Value: 0 **0x0: RC_IN0:** rc_in[0] **0x1: RC_IN1:** rc_in[1] **0x2: RC_IN2:** rc_in[2] **0x3: RC_IN3:** rc_in[3]

36.1.227 UDB_P1_U1_CFG26

Datapath Clock and Reset control

Address: 0x400F32DA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW		RW	
HW Access	R	R	R	R	R		R	
Name	RC_RES_SEL1	RC_RES_SEL0_OR_FRES	RC_INV	RC_EN_INV	RC_EN_MODE [3:2]		RC_EN_SEL [1:0]	

Bits	Name	Description
7	RC_RES_SEL1	Configures the routed reset for the associated UDB component block. The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES = '0' - This bit is not used. When ALT RES = '1' - The bits {RC_SEL1,RC_SEL0_OR_FRES} select the RC routing for routed reset control according to the following: 00 : rc_in [0] 01 : rc_in [1] 10 : rc_in [2] 11 : rc_in [3] Default Value: 0
6	RC_RES_SEL0_OR_FRES	Configures the routed or firmware reset for the associated UDB component block. The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES = '0' - This bit is a firmware reset. When ALT RES = '1' - The bits {RC_SEL1,RC_SEL0_OR_FRES} select the RC routing for routed reset control according to the following: 00 : rc_in [0] 01 : rc_in [1] 10 : rc_in [2] 11 : rc_in [3] Default Value: 0
5	RC_INV	Optionally inverts the clock selection for the associated UDB component block. Default Value: 0 **0x0: NOINV:** Non-inverted **0x1: INVERT:** Inverted
4	RC_EN_INV	Optionally inverts the clock enable selection for the associated UDB component blocks. Default Value: 0 **0x0: NOINV:** Non-inverted **0x1: INVERT:** Inverted
3 : 2	RC_EN_MODE	Selects the operating mode for the clock to the associated UDB component block. Default Value: 0

(continued)

		0x0: OFF: Always off **0x1: ON:** Always on **0x2: POSEDGE:** Positive edge **0x3: LEVEL:** Level sensitive
1 : 0	RC_EN_SEL	Selects channel route for enable control to the associated UDB component block Default Value: 0 **0x0: RC_IN0:** rc_in[0] **0x1: RC_IN1:** rc_in[1] **0x2: RC_IN2:** rc_in[2] **0x3: RC_IN3:** rc_in[3]

36.1.228 UDB_P1_U1_CFG27

Status/Control Clock and Reset control

Address: 0x400F32DB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW		RW	
HW Access	R	R	R	R	R		R	
Name	RC_RES_SEL1	RC_RES_SEL0_OR_FRES	RC_INV	RC_EN_INV	RC_EN_MODE [3:2]		RC_EN_SEL [1:0]	

Bits	Name	Description
7	RC_RES_SEL1	Configures the routed reset for the associated UDB component block. The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES = '0' - This bit is not used. When ALT RES = '1' - The bits {RC_SEL1,RC_SEL0_OR_FRES} select the RC routing for routed reset control according to the following: 00 : rc_in [0] 01 : rc_in [1] 10 : rc_in [2] 11 : rc_in [3] Default Value: 0
6	RC_RES_SEL0_OR_FRES	Configures the routed or firmware reset for the associated UDB component block. The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES = '0' - This bit is a firmware reset. When ALT RES = '1' - The bits {RC_SEL1,RC_SEL0_OR_FRES} select the RC routing for routed reset control according to the following: 00 : rc_in [0] 01 : rc_in [1] 10 : rc_in [2] 11 : rc_in [3] Default Value: 0
5	RC_INV	Optionally inverts the clock selection for the associated UDB component block. Default Value: 0 **0x0: NOINV:** Non-inverted **0x1: INVERT:** Inverted
4	RC_EN_INV	Optionally inverts the clock enable selection for the associated UDB component blocks. Default Value: 0 **0x0: NOINV:** Non-inverted **0x1: INVERT:** Inverted
3 : 2	RC_EN_MODE	Selects the operating mode for the clock to the associated UDB component block. Default Value: 0

(continued)

		0x0: OFF: Always off **0x1: ON:** Always on **0x2: POSEDGE:** Positive edge **0x3: LEVEL:** Level sensitive
1 : 0	RC_EN_SEL	Selects channel route for enable control to the associated UDB component block Default Value: 0 **0x0: RC_IN0:** rc_in[0] **0x1: RC_IN1:** rc_in[1] **0x2: RC_IN2:** rc_in[2] **0x3: RC_IN3:** rc_in[3]

36.1.229 UDB_P1_U1_CFG28

Clock Selection for PLD1 and PLD0

Address: 0x400F32DC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	PLD1_CK_SEL [7:4]				PLD0_CK_SEL [3:0]			

Bits	Name	Description
7 : 4	PLD1_CK_SEL	Clock selection registers Default Value: 0 **0x0: GCLK0:** gclk[0] **0x1: GCLK1:** gclk[1] **0x2: GCLK2:** gclk[2] **0x3: GCLK3:** gclk[3] **0x4: GCLK4:** gclk[4] **0x5: GCLK5:** gclk[5] **0x6: GCLK6:** gclk[6] **0x7: GCLK7:** gclk[7] **0x8: EXT_CLK:** ext_clk **0x9: SYSCLK:** sysclk
3 : 0	PLD0_CK_SEL	Clock selection registers Default Value: 0 **0x0: GCLK0:** gclk[0] **0x1: GCLK1:** gclk[1] **0x2: GCLK2:** gclk[2] **0x3: GCLK3:** gclk[3]

(continued)

0x4: GCLK4:
gclk[4]

0x5: GCLK5:
gclk[5]

0x6: GCLK6:
gclk[6]

0x7: GCLK7:
gclk[7]

0x8: EXT_CLK:
ext_clk

0x9: SYSCLK:
sysclk

36.1.230 UDB_P1_U1_CFG29

Clock Selection for Datapath, Status and Control

Address: 0x400F32DD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	SC_CK_SEL [7:4]				DP_CK_SEL [3:0]			

Bits	Name	Description
7 : 4	SC_CK_SEL	Clock selection registers Default Value: 0 **0x0: GCLK0:** gclk[0] **0x1: GCLK1:** gclk[1] **0x2: GCLK2:** gclk[2] **0x3: GCLK3:** gclk[3] **0x4: GCLK4:** gclk[4] **0x5: GCLK5:** gclk[5] **0x6: GCLK6:** gclk[6] **0x7: GCLK7:** gclk[7] **0x8: EXT_CLK:** ext_clk **0x9: SYSCLK:** sysclk
3 : 0	DP_CK_SEL	Clock selection registers Default Value: 0 **0x0: GCLK0:** gclk[0] **0x1: GCLK1:** gclk[1] **0x2: GCLK2:** gclk[2] **0x3: GCLK3:** gclk[3]

(continued)

0x4: GCLK4:
gclk[4]

0x5: GCLK5:
gclk[5]

0x6: GCLK6:
gclk[6]

0x7: GCLK7:
gclk[7]

0x8: EXT_CLK:
ext_clk

0x9: SYSCLK:
sysclk

36.1.231 UDB_P1_U1_CFG30

Reset control

Address: 0x400F32DE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	None	RW	RW	RW	RW	
HW Access	R	R	None	R	R	R	R	
Name	SC_RES_POL	DP_RES_POL	None	GUDB_WR	EN_RES_CNTCTL	RES_POL	RES_SEL [1:0]	

Bits	Name	Description
7	SC_RES_POL	Only valid when ALT RES (CFG31) is '1'. This bit controls the polarity of the selected SC routed reset. Default Value: 0 **0x0: NOINV:** Routed reset to the Status and Control block is true polarity. **0x1: INVERT:** Routed reset to the Status and Control block is inverted polarity.
6	DP_RES_POL	Only valid when ALT RES (CFG31) is '1'. This bit controls the polarity of the selected Datapath routed reset. Default Value: 0 **0x0: NOINV:** Routed reset to the Datapath block is true polarity. **0x1: INVERT:** Routed reset to the Datapath block is inverted polarity.
4	GUDB_WR	Enable global write operation for the configuration and working registers in this UDB. When this bit is set, the UDB ID select decoding is bypassed. Default Value: 0 **0x0: DISABLE:** Global UDB configuration/working register write is disabled **0x1: ENABLE:** Global UDB configuration/working register write is enabled
3	EN_RES_CNTCTL	This bit gates the routed reset to the counter/control register. By default, the operation is compatible, i.e., it only applies to the counter. However, if the updated control regisiter modes are used (sync mode, pulse mode, or the ext res bit) then the routed reset applies to the control register also. Default Value: 0 **0x0: DISABLE:** Routed reset is not applied to counter/control register **0x1: ENABLE:** Routed reset is applied to the counter/control register

(continued)

2	RES_POL	The meaning of this bit depends on the value of the ALT RES bit in CFG31. When ALT RES is '0' (compatible mode), this bit sets the polarity of the routed reset. When ALT RES is '1', this bit is unused. Default Value: 0 **0x0: NEGATED:** Polarity of the routed reset is true. **0x1: ASSERTED:** Polarity of the routed reset is inverted.
1 : 0	RES_SEL	The meaning of this bit depends on the value of ALT RES (CFG31). When ALT RES is '0' (compatible mode), this 2 bit field selects the RC routing input for the compatible reset scheme. When the ALT RES bit is '1', these bits are not used. Default Value: 0 **0x0: RC_IN0:** rc_in[0] **0x1: RC_IN1:** rc_in[1] **0x2: RC_IN2:** rc_in[2] **0x3: RC_IN3:** rc_in[3]

36.1.232 UDB_P1_U1_CFG31

Reset control

Address: 0x400F32DF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW		RW	RW	RW	RW
HW Access	R	R	R		R	R	R	R
Name	PLD1_RES_POL	PLD0_RES_POL	EXT_CK_SEL [5:4]		EN_RES_DP	EN_RES_STAT	EXT_SYNC	ALT_RES

Bits	Name	Description
7	PLD1_RES_POL	Not connected. NOTE: There is only one routed reset available to both PLDs in the UDB. When ALT RES is '1', PLD0 RES SEL controls the polarity of the routed reset for both PLDs. Default Value: 0 **0x0: NOINV:** Not Used **0x1: INVERT:** Not Used
6	PLD0_RES_POL	The meaning of this bit depends on the value of ALT RES. When ALT RES (CFG31) is '1', this bit controls the polarity of the selected PLD0 routed reset. NOTE: There is only one routed reset available to both PLDs in the UDB. When ALT RES is '1', PLD0 RES SEL controls the polarity of the routed reset for both PLDs. Default Value: 0 **0x0: NOINV:** Routed reset to the PLD0/PLD1 block is true polarity. **0x1: INVERT:** Routed reset to the PLD0/PLD1 block is inverted polarity.
5 : 4	EXT_CK_SEL	External clock selection Default Value: 0 **0x0: RC_IN0:** rc_in[0] **0x1: RC_IN1:** rc_in[1] **0x2: RC_IN2:** rc_in[2] **0x3: RC_IN3:** rc_in[3]
3	EN_RES_DP	Only valid when ALT RES (CFG31) is '1'. This bit gates the routed reset to the Datapath block. Default Value: 0 **0x0: DISABLE:** Routed reset to the Datapath block is gated off. **0x1: ENABLE:** Routed reset to the Datapath block is on. ALT RES must be '1' and routed reset must be selected in CFG26

(continued)

2	EN_RES_STAT	Only valid when ALT RES (CFG31) is '1'. This bit gates the routed reset to the status register. Default Value: 0 **0x0: NEGATED:** Status register routed reset is gated off **0x1: ASSERTED:** Status register routed reset is on
1	EXT_SYNC	Enable synchronization of selected external clock Default Value: 0 **0x0: DISABLE:** Selected external clock input is not synchronized **0x1: ENABLE:** Selected external clock input is synchronized
0	ALT_RES	This bit toggles between two reset configurations. When this bit is '0', one routed reset is shared by all components in this UDB (compatible mode). When this bit is a 1, each block can select a unique routed reset from the available RC inputs. Default Value: 0 **0x0: COMPATIBLE:** All UDB blocks share a common routed reset. **0x1: ALTERNATE:** Each UDB component block can select and control its individual routed reset.

36.1.233 UDB_P1_U1_DCFG0

Dynamic Configuration RAM

Address: 0x400F32E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW	RW	RW	RW
HW Access	R		R		R	R	R	R
Name	A0_WR_SRC [7:6]		A1_WR_SRC [5:4]		CFB_EN	CI_SEL	SI_SEL	CMP_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW	RW		RW	
HW Access	R			R	R		R	
Name	FUNC [15:13]			SRC_A	SRC_B [11:10]		SHIFT [9:8]	

Bits	Name	Description
15 : 13	FUNC	Dynamic ALU function selection Default Value: X **0x0: PASS:** Pass **0x1: INC_A:** Increment source A **0x2: DEC_A:** Decrement source A **0x3: ADD:** Add **0x4: SUB:** Subtract **0x5: XOR:** Bitwise XOR **0x6: AND:** Bitwise AND **0x7: OR:** Bitwise OR
12	SRC_A	Dynamic ALU source A selection Default Value: X **0x0: A0:** Configuration A **0x1: A1:** Configuration B
11 : 10	SRC_B	Dynamic ALU source B selection Default Value: X

(continued)

		0x0: D0: ALU source B is D0 **0x1: D1:** ALU source B is D1 **0x2: A0:** ALU source B is A0 **0x3: A1:** ALU source B is A1
9 : 8	SHIFT	Dynamic shift selection Default Value: X **0x0: NOSHIFT:** No shift **0x1: LEFT:** Left Shift **0x2: RIGHT:** Right Shift **0x3: SWAP:** Nibble swap
7 : 6	A0_WR_SRC	Dynamic A0 write source selection Default Value: X **0x0: NOWRITE:** no value written to A0 **0x1: ALU:** ALU output written to A0 **0x2: D0:** D1 value written to A0 **0x3: F0:** F1 value written to A0
5 : 4	A1_WR_SRC	Dynamic A1 write source selection Default Value: X **0x0: NOWRITE:** no value written to A1 **0x1: ALU:** ALU output written to A1 **0x2: D1:** D1 value written to A1 **0x3: F1:** F1 value written to A1
3	CFB_EN	Dynamic CRC feedback selection Default Value: X **0x0: DISABLE:** CRC feedback disabled **0x1: ENABLE:** CRC feedback enabled

(continued)

2	CI_SEL	Dynamic carry in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
1	SI_SEL	Dynamic shift in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
0	CMP_SEL	Dynamic compare selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B

36.1.234 UDB_P1_U1_DCFG1

Dynamic Configuration RAM

Address: 0x400F32E2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW	RW	RW	RW
HW Access	R		R		R	R	R	R
Name	A0_WR_SRC [7:6]		A1_WR_SRC [5:4]		CFB_EN	CI_SEL	SI_SEL	CMP_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW	RW		RW	
HW Access	R			R	R		R	
Name	FUNC [15:13]			SRC_A	SRC_B [11:10]		SHIFT [9:8]	

Bits	Name	Description
15 : 13	FUNC	Dynamic ALU function selection Default Value: X **0x0: PASS:** Pass **0x1: INC_A:** Increment source A **0x2: DEC_A:** Decrement source A **0x3: ADD:** Add **0x4: SUB:** Subtract **0x5: XOR:** Bitwise XOR **0x6: AND:** Bitwise AND **0x7: OR:** Bitwise OR
12	SRC_A	Dynamic ALU source A selection Default Value: X **0x0: A0:** Configuration A **0x1: A1:** Configuration B
11 : 10	SRC_B	Dynamic ALU source B selection Default Value: X

(continued)

		0x0: D0: ALU source B is D0 **0x1: D1:** ALU source B is D1 **0x2: A0:** ALU source B is A0 **0x3: A1:** ALU source B is A1
9 : 8	SHIFT	Dynamic shift selection Default Value: X **0x0: NOSHIFT:** No shift **0x1: LEFT:** Left Shift **0x2: RIGHT:** Right Shift **0x3: SWAP:** Nibble swap
7 : 6	A0_WR_SRC	Dynamic A0 write source selection Default Value: X **0x0: NOWRITE:** no value written to A0 **0x1: ALU:** ALU output written to A0 **0x2: D0:** D1 value written to A0 **0x3: F0:** F1 value written to A0
5 : 4	A1_WR_SRC	Dynamic A1 write source selection Default Value: X **0x0: NOWRITE:** no value written to A1 **0x1: ALU:** ALU output written to A1 **0x2: D1:** D1 value written to A1 **0x3: F1:** F1 value written to A1
3	CFB_EN	Dynamic CRC feedback selection Default Value: X **0x0: DISABLE:** CRC feedback disabled **0x1: ENABLE:** CRC feedback enabled

(continued)

2	CI_SEL	Dynamic carry in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
1	SI_SEL	Dynamic shift in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
0	CMP_SEL	Dynamic compare selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B

36.1.235 UDB_P1_U1_DCFG2

Dynamic Configuration RAM

Address: 0x400F32E4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW	RW	RW	RW
HW Access	R		R		R	R	R	R
Name	A0_WR_SRC [7:6]		A1_WR_SRC [5:4]		CFB_EN	CI_SEL	SI_SEL	CMP_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW	RW		RW	
HW Access	R			R	R		R	
Name	FUNC [15:13]			SRC_A	SRC_B [11:10]		SHIFT [9:8]	

Bits	Name	Description
15 : 13	FUNC	Dynamic ALU function selection Default Value: X **0x0: PASS:** Pass **0x1: INC_A:** Increment source A **0x2: DEC_A:** Decrement source A **0x3: ADD:** Add **0x4: SUB:** Subtract **0x5: XOR:** Bitwise XOR **0x6: AND:** Bitwise AND **0x7: OR:** Bitwise OR
12	SRC_A	Dynamic ALU source A selection Default Value: X **0x0: A0:** Configuration A **0x1: A1:** Configuration B
11 : 10	SRC_B	Dynamic ALU source B selection Default Value: X

(continued)

		0x0: D0: ALU source B is D0 **0x1: D1:** ALU source B is D1 **0x2: A0:** ALU source B is A0 **0x3: A1:** ALU source B is A1
9 : 8	SHIFT	Dynamic shift selection Default Value: X **0x0: NOSHIFT:** No shift **0x1: LEFT:** Left Shift **0x2: RIGHT:** Right Shift **0x3: SWAP:** Nibble swap
7 : 6	A0_WR_SRC	Dynamic A0 write source selection Default Value: X **0x0: NOWRITE:** no value written to A0 **0x1: ALU:** ALU output written to A0 **0x2: D0:** D1 value written to A0 **0x3: F0:** F1 value written to A0
5 : 4	A1_WR_SRC	Dynamic A1 write source selection Default Value: X **0x0: NOWRITE:** no value written to A1 **0x1: ALU:** ALU output written to A1 **0x2: D1:** D1 value written to A1 **0x3: F1:** F1 value written to A1
3	CFB_EN	Dynamic CRC feedback selection Default Value: X **0x0: DISABLE:** CRC feedback disabled **0x1: ENABLE:** CRC feedback enabled

(continued)

2	CI_SEL	Dynamic carry in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
1	SI_SEL	Dynamic shift in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
0	CMP_SEL	Dynamic compare selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B

36.1.236 UDB_P1_U1_DCFG3

Dynamic Configuration RAM

Address: 0x400F32E6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW	RW	RW	RW
HW Access	R		R		R	R	R	R
Name	A0_WR_SRC [7:6]		A1_WR_SRC [5:4]		CFB_EN	CI_SEL	SI_SEL	CMP_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW	RW		RW	
HW Access	R			R	R		R	
Name	FUNC [15:13]			SRC_A	SRC_B [11:10]		SHIFT [9:8]	

Bits	Name	Description
15 : 13	FUNC	Dynamic ALU function selection Default Value: X **0x0: PASS:** Pass **0x1: INC_A:** Increment source A **0x2: DEC_A:** Decrement source A **0x3: ADD:** Add **0x4: SUB:** Subtract **0x5: XOR:** Bitwise XOR **0x6: AND:** Bitwise AND **0x7: OR:** Bitwise OR
12	SRC_A	Dynamic ALU source A selection Default Value: X **0x0: A0:** Configuration A **0x1: A1:** Configuration B
11 : 10	SRC_B	Dynamic ALU source B selection Default Value: X

(continued)

		0x0: D0: ALU source B is D0 **0x1: D1:** ALU source B is D1 **0x2: A0:** ALU source B is A0 **0x3: A1:** ALU source B is A1
9 : 8	SHIFT	Dynamic shift selection Default Value: X **0x0: NOSHIFT:** No shift **0x1: LEFT:** Left Shift **0x2: RIGHT:** Right Shift **0x3: SWAP:** Nibble swap
7 : 6	A0_WR_SRC	Dynamic A0 write source selection Default Value: X **0x0: NOWRITE:** no value written to A0 **0x1: ALU:** ALU output written to A0 **0x2: D0:** D1 value written to A0 **0x3: F0:** F1 value written to A0
5 : 4	A1_WR_SRC	Dynamic A1 write source selection Default Value: X **0x0: NOWRITE:** no value written to A1 **0x1: ALU:** ALU output written to A1 **0x2: D1:** D1 value written to A1 **0x3: F1:** F1 value written to A1
3	CFB_EN	Dynamic CRC feedback selection Default Value: X **0x0: DISABLE:** CRC feedback disabled **0x1: ENABLE:** CRC feedback enabled

(continued)

2	CI_SEL	Dynamic carry in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
1	SI_SEL	Dynamic shift in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
0	CMP_SEL	Dynamic compare selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B

36.1.237 UDB_P1_U1_DCFG4

Dynamic Configuration RAM

Address: 0x400F32E8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW	RW	RW	RW
HW Access	R		R		R	R	R	R
Name	A0_WR_SRC [7:6]		A1_WR_SRC [5:4]		CFB_EN	CI_SEL	SI_SEL	CMP_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW	RW		RW	
HW Access	R			R	R		R	
Name	FUNC [15:13]			SRC_A	SRC_B [11:10]		SHIFT [9:8]	

Bits	Name	Description
15 : 13	FUNC	Dynamic ALU function selection Default Value: X **0x0: PASS:** Pass **0x1: INC_A:** Increment source A **0x2: DEC_A:** Decrement source A **0x3: ADD:** Add **0x4: SUB:** Subtract **0x5: XOR:** Bitwise XOR **0x6: AND:** Bitwise AND **0x7: OR:** Bitwise OR
12	SRC_A	Dynamic ALU source A selection Default Value: X **0x0: A0:** Configuration A **0x1: A1:** Configuration B
11 : 10	SRC_B	Dynamic ALU source B selection Default Value: X

(continued)

		0x0: D0: ALU source B is D0 **0x1: D1:** ALU source B is D1 **0x2: A0:** ALU source B is A0 **0x3: A1:** ALU source B is A1
9 : 8	SHIFT	Dynamic shift selection Default Value: X **0x0: NOSHIFT:** No shift **0x1: LEFT:** Left Shift **0x2: RIGHT:** Right Shift **0x3: SWAP:** Nibble swap
7 : 6	A0_WR_SRC	Dynamic A0 write source selection Default Value: X **0x0: NOWRITE:** no value written to A0 **0x1: ALU:** ALU output written to A0 **0x2: D0:** D1 value written to A0 **0x3: F0:** F1 value written to A0
5 : 4	A1_WR_SRC	Dynamic A1 write source selection Default Value: X **0x0: NOWRITE:** no value written to A1 **0x1: ALU:** ALU output written to A1 **0x2: D1:** D1 value written to A1 **0x3: F1:** F1 value written to A1
3	CFB_EN	Dynamic CRC feedback selection Default Value: X **0x0: DISABLE:** CRC feedback disabled **0x1: ENABLE:** CRC feedback enabled

(continued)

2	CI_SEL	Dynamic carry in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
1	SI_SEL	Dynamic shift in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
0	CMP_SEL	Dynamic compare selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B

36.1.238 UDB_P1_U1_DCFG5

Dynamic Configuration RAM

Address: 0x400F32EA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW	RW	RW	RW
HW Access	R		R		R	R	R	R
Name	A0_WR_SRC [7:6]		A1_WR_SRC [5:4]		CFB_EN	CI_SEL	SI_SEL	CMP_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW	RW		RW	
HW Access	R			R	R		R	
Name	FUNC [15:13]			SRC_A	SRC_B [11:10]		SHIFT [9:8]	

Bits	Name	Description
15 : 13	FUNC	Dynamic ALU function selection Default Value: X **0x0: PASS:** Pass **0x1: INC_A:** Increment source A **0x2: DEC_A:** Decrement source A **0x3: ADD:** Add **0x4: SUB:** Subtract **0x5: XOR:** Bitwise XOR **0x6: AND:** Bitwise AND **0x7: OR:** Bitwise OR
12	SRC_A	Dynamic ALU source A selection Default Value: X **0x0: A0:** Configuration A **0x1: A1:** Configuration B
11 : 10	SRC_B	Dynamic ALU source B selection Default Value: X

(continued)

		0x0: D0: ALU source B is D0 **0x1: D1:** ALU source B is D1 **0x2: A0:** ALU source B is A0 **0x3: A1:** ALU source B is A1
9 : 8	SHIFT	Dynamic shift selection Default Value: X **0x0: NOSHIFT:** No shift **0x1: LEFT:** Left Shift **0x2: RIGHT:** Right Shift **0x3: SWAP:** Nibble swap
7 : 6	A0_WR_SRC	Dynamic A0 write source selection Default Value: X **0x0: NOWRITE:** no value written to A0 **0x1: ALU:** ALU output written to A0 **0x2: D0:** D1 value written to A0 **0x3: F0:** F1 value written to A0
5 : 4	A1_WR_SRC	Dynamic A1 write source selection Default Value: X **0x0: NOWRITE:** no value written to A1 **0x1: ALU:** ALU output written to A1 **0x2: D1:** D1 value written to A1 **0x3: F1:** F1 value written to A1
3	CFB_EN	Dynamic CRC feedback selection Default Value: X **0x0: DISABLE:** CRC feedback disabled **0x1: ENABLE:** CRC feedback enabled

(continued)

2	CI_SEL	Dynamic carry in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
1	SI_SEL	Dynamic shift in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
0	CMP_SEL	Dynamic compare selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B

36.1.239 UDB_P1_U1_DCFG6

Dynamic Configuration RAM

Address: 0x400F32EC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW	RW	RW	RW
HW Access	R		R		R	R	R	R
Name	A0_WR_SRC [7:6]		A1_WR_SRC [5:4]		CFB_EN	CI_SEL	SI_SEL	CMP_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW	RW		RW	
HW Access	R			R	R		R	
Name	FUNC [15:13]			SRC_A	SRC_B [11:10]		SHIFT [9:8]	

Bits	Name	Description
15 : 13	FUNC	Dynamic ALU function selection Default Value: X **0x0: PASS:** Pass **0x1: INC_A:** Increment source A **0x2: DEC_A:** Decrement source A **0x3: ADD:** Add **0x4: SUB:** Subtract **0x5: XOR:** Bitwise XOR **0x6: AND:** Bitwise AND **0x7: OR:** Bitwise OR
12	SRC_A	Dynamic ALU source A selection Default Value: X **0x0: A0:** Configuration A **0x1: A1:** Configuration B
11 : 10	SRC_B	Dynamic ALU source B selection Default Value: X

(continued)

		0x0: D0: ALU source B is D0 **0x1: D1:** ALU source B is D1 **0x2: A0:** ALU source B is A0 **0x3: A1:** ALU source B is A1
9 : 8	SHIFT	Dynamic shift selection Default Value: X **0x0: NOSHIFT:** No shift **0x1: LEFT:** Left Shift **0x2: RIGHT:** Right Shift **0x3: SWAP:** Nibble swap
7 : 6	A0_WR_SRC	Dynamic A0 write source selection Default Value: X **0x0: NOWRITE:** no value written to A0 **0x1: ALU:** ALU output written to A0 **0x2: D0:** D1 value written to A0 **0x3: F0:** F1 value written to A0
5 : 4	A1_WR_SRC	Dynamic A1 write source selection Default Value: X **0x0: NOWRITE:** no value written to A1 **0x1: ALU:** ALU output written to A1 **0x2: D1:** D1 value written to A1 **0x3: F1:** F1 value written to A1
3	CFB_EN	Dynamic CRC feedback selection Default Value: X **0x0: DISABLE:** CRC feedback disabled **0x1: ENABLE:** CRC feedback enabled

(continued)

2	CI_SEL	Dynamic carry in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
1	SI_SEL	Dynamic shift in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
0	CMP_SEL	Dynamic compare selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B

36.1.240 UDB_P1_U1_DCFG7

Dynamic Configuration RAM

Address: 0x400F32EE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW	RW	RW	RW
HW Access	R		R		R	R	R	R
Name	A0_WR_SRC [7:6]		A1_WR_SRC [5:4]		CFB_EN	CI_SEL	SI_SEL	CMP_SEL

Bits	15	14	13	12	11	10	9	8
SW Access	RW			RW	RW		RW	
HW Access	R			R	R		R	
Name	FUNC [15:13]			SRC_A	SRC_B [11:10]		SHIFT [9:8]	

Bits	Name	Description
15 : 13	FUNC	Dynamic ALU function selection Default Value: X **0x0: PASS:** Pass **0x1: INC_A:** Increment source A **0x2: DEC_A:** Decrement source A **0x3: ADD:** Add **0x4: SUB:** Subtract **0x5: XOR:** Bitwise XOR **0x6: AND:** Bitwise AND **0x7: OR:** Bitwise OR
12	SRC_A	Dynamic ALU source A selection Default Value: X **0x0: A0:** Configuration A **0x1: A1:** Configuration B
11 : 10	SRC_B	Dynamic ALU source B selection Default Value: X

(continued)

		0x0: D0: ALU source B is D0 **0x1: D1:** ALU source B is D1 **0x2: A0:** ALU source B is A0 **0x3: A1:** ALU source B is A1
9 : 8	SHIFT	Dynamic shift selection Default Value: X **0x0: NOSHIFT:** No shift **0x1: LEFT:** Left Shift **0x2: RIGHT:** Right Shift **0x3: SWAP:** Nibble swap
7 : 6	A0_WR_SRC	Dynamic A0 write source selection Default Value: X **0x0: NOWRITE:** no value written to A0 **0x1: ALU:** ALU output written to A0 **0x2: D0:** D1 value written to A0 **0x3: F0:** F1 value written to A0
5 : 4	A1_WR_SRC	Dynamic A1 write source selection Default Value: X **0x0: NOWRITE:** no value written to A1 **0x1: ALU:** ALU output written to A1 **0x2: D1:** D1 value written to A1 **0x3: F1:** F1 value written to A1
3	CFB_EN	Dynamic CRC feedback selection Default Value: X **0x0: DISABLE:** CRC feedback disabled **0x1: ENABLE:** CRC feedback enabled

(continued)

2	CI_SEL	Dynamic carry in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
1	SI_SEL	Dynamic shift in selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B
0	CMP_SEL	Dynamic compare selection Default Value: X **0x0: CFG_A:** Configuration A **0x1: CFG_B:** Configuration B

37 UDB 8-Bit Working (WRK8) Registers

This section discusses the WRK8 registers. It lists all the registers in mapping tables, in address order.

37.1 Register Details

Register Name	Address
UDB_W8_A00	0x400F0000
UDB_W8_A01	0x400F0001
UDB_W8_A02	0x400F0002
UDB_W8_A03	0x400F0003
UDB_W8_A10	0x400F0010
UDB_W8_A11	0x400F0011
UDB_W8_A12	0x400F0012
UDB_W8_A13	0x400F0013
UDB_W8_D00	0x400F0020
UDB_W8_D01	0x400F0021
UDB_W8_D02	0x400F0022
UDB_W8_D03	0x400F0023
UDB_W8_D10	0x400F0030
UDB_W8_D11	0x400F0031
UDB_W8_D12	0x400F0032
UDB_W8_D13	0x400F0033
UDB_W8_F00	0x400F0040
UDB_W8_F01	0x400F0041
UDB_W8_F02	0x400F0042
UDB_W8_F03	0x400F0043
UDB_W8_F10	0x400F0050
UDB_W8_F11	0x400F0051
UDB_W8_F12	0x400F0052
UDB_W8_F13	0x400F0053
UDB_W8_ST0	0x400F0060
UDB_W8_ST1	0x400F0061

Register Name	Address
UDB_W8_ST2	0x400F0062
UDB_W8_ST3	0x400F0063
UDB_W8_CTL0	0x400F0070
UDB_W8_CTL1	0x400F0071
UDB_W8_CTL2	0x400F0072
UDB_W8_CTL3	0x400F0073
UDB_W8_MSK0	0x400F0080
UDB_W8_MSK1	0x400F0081
UDB_W8_MSK2	0x400F0082
UDB_W8_MSK3	0x400F0083
UDB_W8_ACTL0	0x400F0090
UDB_W8_ACTL1	0x400F0091
UDB_W8_ACTL2	0x400F0092
UDB_W8_ACTL3	0x400F0093
UDB_W8_MC0	0x400F00A0
UDB_W8_MC1	0x400F00A1
UDB_W8_MC2	0x400F00A2
UDB_W8_MC3	0x400F00A3

37.1.1 UDB_W8_A00

Accumulator 0

Address: 0x400F0000

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	A0 [7:0]							

Bits	Name	Description
7 : 0	A0	Accumulator 0 Default Value: 0

37.1.2 UDB_W8_A01

Accumulator 0

Address: 0x400F0001

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	A0 [7:0]							

Bits	Name	Description
7 : 0	A0	Accumulator 0 Default Value: 0

37.1.3 UDB_W8_A02

Accumulator 0

Address: 0x400F0002

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	A0 [7:0]							

Bits	Name	Description
7 : 0	A0	Accumulator 0 Default Value: 0

37.1.4 UDB_W8_A03

Accumulator 0

Address: 0x400F0003

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	A0 [7:0]							

Bits	Name	Description
7 : 0	A0	Accumulator 0 Default Value: 0

37.1.5 UDB_W8_A10

Accumulator 1

Address: 0x400F0010

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	A1 [7:0]							

Bits	Name	Description
7 : 0	A1	Accumulator 1 Default Value: 0

37.1.6 UDB_W8_A11

Accumulator 1

Address: 0x400F0011

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	A1 [7:0]							

Bits	Name	Description
7 : 0	A1	Accumulator 1 Default Value: 0

37.1.7 UDB_W8_A12

Accumulator 1

Address: 0x400F0012

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	A1 [7:0]							

Bits	Name	Description
7 : 0	A1	Accumulator 1 Default Value: 0

37.1.8 UDB_W8_A13

Accumulator 1

Address: 0x400F0013

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	A1 [7:0]							

Bits	Name	Description
7 : 0	A1	Accumulator 1 Default Value: 0

37.1.9 UDB_W8_D00

Data 0

Address: 0x400F0020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	D0 [7:0]							

Bits	Name	Description
7 : 0	D0	Data 0 Default Value: 0

37.1.10 UDB_W8_D01

Data 0

Address: 0x400F0021

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	D0 [7:0]							

Bits	Name	Description
7 : 0	D0	Data 0 Default Value: 0

37.1.11 UDB_W8_D02

Data 0

Address: 0x400F0022

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	D0 [7:0]							

Bits	Name	Description
7 : 0	D0	Data 0 Default Value: 0

37.1.12 UDB_W8_D03

Data 0

Address: 0x400F0023

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	D0 [7:0]							

Bits	Name	Description
7 : 0	D0	Data 0 Default Value: 0

37.1.13 UDB_W8_D10

Data 1

Address: 0x400F0030

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	D1 [7:0]							

Bits	Name	Description
7 : 0	D1	Data 1 Default Value: 0

37.1.14 UDB_W8_D11

Data 1

Address: 0x400F0031

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	D1 [7:0]							

Bits	Name	Description
7 : 0	D1	Data 1 Default Value: 0

37.1.15 UDB_W8_D12

Data 1

Address: 0x400F0032

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	D1 [7:0]							

Bits	Name	Description
7 : 0	D1	Data 1 Default Value: 0

37.1.16 UDB_W8_D13

Data 1

Address: 0x400F0033

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	D1 [7:0]							

Bits	Name	Description
7 : 0	D1	Data 1 Default Value: 0

37.1.17 UDB_W8_F00

FIFO 0

Address: 0x400F0040

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	F0 [7:0]							

Bits	Name	Description
7 : 0	F0	Fifo 0 Default Value: X

37.1.18 UDB_W8_F01

FIFO 0

Address: 0x400F0041

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	F0 [7:0]							

Bits	Name	Description
7 : 0	F0	Fifo 0 Default Value: X

37.1.19 UDB_W8_F02

FIFO 0

Address: 0x400F0042

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	F0 [7:0]							

Bits	Name	Description
7 : 0	F0	Fifo 0 Default Value: X

37.1.20 UDB_W8_F03

FIFO 0

Address: 0x400F0043

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	F0 [7:0]							

Bits	Name	Description
7 : 0	F0	Fifo 0 Default Value: X

37.1.21 UDB_W8_F10

FIFO 1

Address: 0x400F0050

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	F1 [7:0]							

Bits	Name	Description
7 : 0	F1	Fifo 1 Default Value: X

37.1.22 UDB_W8_F11

FIFO 1

Address: 0x400F0051

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	F1 [7:0]							

Bits	Name	Description
7 : 0	F1	Fifo 1 Default Value: X

37.1.23 UDB_W8_F12

FIFO 1

Address: 0x400F0052

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	F1 [7:0]							

Bits	Name	Description
7 : 0	F1	Fifo 1 Default Value: X

37.1.24 UDB_W8_F13

FIFO 1

Address: 0x400F0053

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	F1 [7:0]							

Bits	Name	Description
7 : 0	F1	Fifo 1 Default Value: X

37.1.25 UDB_W8_ST0

Status Register

Address: 0x400F0060

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	ST [7:0]							

Bits	Name	Description
7 : 0	ST	Status register Default Value: 0

37.1.26 UDB_W8_ST1

Status Register

Address: 0x400F0061

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	ST [7:0]							

Bits	Name	Description
7 : 0	ST	Status register Default Value: 0

37.1.27 UDB_W8_ST2

Status Register

Address: 0x400F0062

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	ST [7:0]							

Bits	Name	Description
7 : 0	ST	Status register Default Value: 0

37.1.28 UDB_W8_ST3

Status Register

Address: 0x400F0063

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	ST [7:0]							

Bits	Name	Description
7 : 0	ST	Status register Default Value: 0

37.1.29 UDB_W8_CTL0

Control Register

Address: 0x400F0070

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CTL [7:0]							

Bits	Name	Description
7 : 0	CTL	Control register Default Value: 0

37.1.30 UDB_W8_CTL1

Control Register

Address: 0x400F0071

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CTL [7:0]							

Bits	Name	Description
7 : 0	CTL	Control register Default Value: 0

37.1.31 UDB_W8_CTL2

Control Register

Address: 0x400F0072

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CTL [7:0]							

Bits	Name	Description
7 : 0	CTL	Control register Default Value: 0

37.1.32 UDB_W8_CTL3

Control Register

Address: 0x400F0073

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CTL [7:0]							

Bits	Name	Description
7 : 0	CTL	Control register Default Value: 0

37.1.33 UDB_W8_MSK0

Interrupt Mask

Address: 0x400F0080

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW						
HW Access	None	R						
Name	None	MSK [6:0]						

Bits	Name	Description
6 : 0	MSK	Interrupt Mask Register Default Value: 0

37.1.34 UDB_W8_MSK1

Interrupt Mask

Address: 0x400F0081

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW						
HW Access	None	R						
Name	None	MSK [6:0]						

Bits	Name	Description
6 : 0	MSK	Interrupt Mask Register Default Value: 0

37.1.35 UDB_W8_MSK2

Interrupt Mask

Address: 0x400F0082

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW						
HW Access	None	R						
Name	None	MSK [6:0]						

Bits	Name	Description
6 : 0	MSK	Interrupt Mask Register Default Value: 0

37.1.36 UDB_W8_MSK3

Interrupt Mask

Address: 0x400F0083

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW						
HW Access	None	R						
Name	None	MSK [6:0]						

Bits	Name	Description
6 : 0	MSK	Interrupt Mask Register Default Value: 0

37.1.37 UDB_W8_ACTL0

Auxiliary Control

Address: 0x400F0090

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		RW	RW	RW	RW	RW	RW
Name	None [7:6]		CNT_START	INT_EN	FIFO1_LVL	FIFO0_LVL	FIFO1_CLR	FIFO0_CLR

Bits	Name	Description
5	CNT_START	Control Register Counter Enable Default Value: 0 **0x0: DISABLE:** Counter disabled **0x1: ENABLE:** Counter enabled
4	INT_EN	enable interrupt Default Value: 0 **0x0: DISABLE:** Interrupt disabled **0x1: ENABLE:** Interrupt enabled
3	FIFO1_LVL	FIFO fill status level control Default Value: 0 **0x0: NORMAL:** input mode: FIFO not full; output mode: FIFO not empty **0x1: MID:** input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full
2	FIFO0_LVL	FIFO fill status level control Default Value: 0 **0x0: NORMAL:** input mode: FIFO not full; output mode: FIFO not empty **0x1: MID:** input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full
1	FIFO1_CLR	FIFO clear Default Value: 0 **0x0: NORMAL:** Normal FIFO operation **0x1: CLEAR:** Clear FIFO state

(continued)

0	FIFO0_CLR	FIFO clear Default Value: 0 **0x0: NORMAL:** Normal FIFO operation **0x1: CLEAR:** Clear FIFO state

37.1.38 UDB_W8_ACTL1

Auxiliary Control

Address: 0x400F0091

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		RW	RW	RW	RW	RW	RW
Name	None [7:6]		CNT_START	INT_EN	FIFO1_LVL	FIFO0_LVL	FIFO1_CLR	FIFO0_CLR

Bits	Name	Description
5	CNT_START	Control Register Counter Enable Default Value: 0 **0x0: DISABLE:** Counter disabled **0x1: ENABLE:** Counter enabled
4	INT_EN	enable interrupt Default Value: 0 **0x0: DISABLE:** Interrupt disabled **0x1: ENABLE:** Interrupt enabled
3	FIFO1_LVL	FIFO fill status level control Default Value: 0 **0x0: NORMAL:** input mode: FIFO not full; output mode: FIFO not empty **0x1: MID:** input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full
2	FIFO0_LVL	FIFO fill status level control Default Value: 0 **0x0: NORMAL:** input mode: FIFO not full; output mode: FIFO not empty **0x1: MID:** input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full
1	FIFO1_CLR	FIFO clear Default Value: 0 **0x0: NORMAL:** Normal FIFO operation **0x1: CLEAR:** Clear FIFO state

(continued)

0	FIFO0_CLR	FIFO clear Default Value: 0 **0x0: NORMAL:** Normal FIFO operation **0x1: CLEAR:** Clear FIFO state

37.1.39 UDB_W8_ACTL2

Auxiliary Control

Address: 0x400F0092

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		RW	RW	RW	RW	RW	RW
Name	None [7:6]		CNT_START	INT_EN	FIFO1_LVL	FIFO0_LVL	FIFO1_CLR	FIFO0_CLR

Bits	Name	Description
5	CNT_START	Control Register Counter Enable Default Value: 0 **0x0: DISABLE:** Counter disabled **0x1: ENABLE:** Counter enabled
4	INT_EN	enable interrupt Default Value: 0 **0x0: DISABLE:** Interrupt disabled **0x1: ENABLE:** Interrupt enabled
3	FIFO1_LVL	FIFO fill status level control Default Value: 0 **0x0: NORMAL:** input mode: FIFO not full; output mode: FIFO not empty **0x1: MID:** input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full
2	FIFO0_LVL	FIFO fill status level control Default Value: 0 **0x0: NORMAL:** input mode: FIFO not full; output mode: FIFO not empty **0x1: MID:** input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full
1	FIFO1_CLR	FIFO clear Default Value: 0 **0x0: NORMAL:** Normal FIFO operation **0x1: CLEAR:** Clear FIFO state

(continued)

0	FIFO0_CLR	FIFO clear Default Value: 0 **0x0: NORMAL:** Normal FIFO operation **0x1: CLEAR:** Clear FIFO state

37.1.40 UDB_W8_ACTL3

Auxiliary Control

Address: 0x400F0093

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		RW	RW	RW	RW	RW	RW
Name	None [7:6]		CNT_START	INT_EN	FIFO1_LVL	FIFO0_LVL	FIFO1_CLR	FIFO0_CLR

Bits	Name	Description
5	CNT_START	Control Register Counter Enable Default Value: 0 **0x0: DISABLE:** Counter disabled **0x1: ENABLE:** Counter enabled
4	INT_EN	enable interrupt Default Value: 0 **0x0: DISABLE:** Interrupt disabled **0x1: ENABLE:** Interrupt enabled
3	FIFO1_LVL	FIFO fill status level control Default Value: 0 **0x0: NORMAL:** input mode: FIFO not full; output mode: FIFO not empty **0x1: MID:** input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full
2	FIFO0_LVL	FIFO fill status level control Default Value: 0 **0x0: NORMAL:** input mode: FIFO not full; output mode: FIFO not empty **0x1: MID:** input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full
1	FIFO1_CLR	FIFO clear Default Value: 0 **0x0: NORMAL:** Normal FIFO operation **0x1: CLEAR:** Clear FIFO state

(continued)

0	FIFO0_CLR	FIFO clear Default Value: 0 **0x0: NORMAL:** Normal FIFO operation **0x1: CLEAR:** Clear FIFO state

37.1.41 UDB_W8_MC0

PLD Macrocell reading

Address: 0x400F00A0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	RW				RW			
Name	PLD1_MC [7:4]				PLD0_MC [3:0]			

Bits	Name	Description
7 : 4	PLD1_MC	Read Macrocell 1 Default Value: 0
3 : 0	PLD0_MC	Read Macrocell 0 Default Value: 0

37.1.42 UDB_W8_MC1

PLD Macrocell reading

Address: 0x400F00A1

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	RW				RW			
Name	PLD1_MC [7:4]				PLD0_MC [3:0]			

Bits	Name	Description
7 : 4	PLD1_MC	Read Macrocell 1 Default Value: 0
3 : 0	PLD0_MC	Read Macrocell 0 Default Value: 0

37.1.43 UDB_W8_MC2

PLD Macrocell reading

Address: 0x400F00A2

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	RW				RW			
Name	PLD1_MC [7:4]				PLD0_MC [3:0]			

Bits	Name	Description
7 : 4	PLD1_MC	Read Macrocell 1 Default Value: 0
3 : 0	PLD0_MC	Read Macrocell 0 Default Value: 0

37.1.44 UDB_W8_MC3

PLD Macrocell reading

Address: 0x400F00A3

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	RW				RW			
Name	PLD1_MC [7:4]				PLD0_MC [3:0]			

Bits	Name	Description
7 : 4	PLD1_MC	Read Macrocell 1 Default Value: 0
3 : 0	PLD0_MC	Read Macrocell 0 Default Value: 0

38 WRK16CAT Registers

This section discusses the UDB 16-bit Concatenated Working (WRK16CAT) registers. It lists all the registers in mapping tables, in address order.

38.1 Register Details

Register Name	Address
UDB_CAT16_A0	0x400F1000
UDB_CAT16_A1	0x400F1002
UDB_CAT16_A2	0x400F1004
UDB_CAT16_A3	0x400F1006
UDB_CAT16_D0	0x400F1040
UDB_CAT16_D1	0x400F1042
UDB_CAT16_D2	0x400F1044
UDB_CAT16_D3	0x400F1046
UDB_CAT16_F0	0x400F1080
UDB_CAT16_F1	0x400F1082
UDB_CAT16_F2	0x400F1084
UDB_CAT16_F3	0x400F1086
UDB_CAT16_CTL_ST0	0x400F10C0
UDB_CAT16_CTL_ST1	0x400F10C2
UDB_CAT16_CTL_ST2	0x400F10C4
UDB_CAT16_CTL_ST3	0x400F10C6
UDB_CAT16_ACTL_MSK0	0x400F1100
UDB_CAT16_ACTL_MSK1	0x400F1102
UDB_CAT16_ACTL_MSK2	0x400F1104
UDB_CAT16_ACTL_MSK3	0x400F1106
UDB_CAT16_MC0	0x400F1140
UDB_CAT16_MC1	0x400F1142
UDB_CAT16_MC2	0x400F1144
UDB_CAT16_MC3	0x400F1146

38.1.1 UDB_CAT16_A0

Accumulator Registers {A1,A0}

Address: 0x400F1000

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	A0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	A1 [15:8]							

Bits	Name	Description
15 : 8	A1	Accumulator 1 Register Default Value: 0
7 : 0	A0	Accumulator 0 Register Default Value: 0

38.1.2 UDB_CAT16_A1

Accumulator Registers {A1,A0}

Address: 0x400F1002

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	A0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	A1 [15:8]							

Bits	Name	Description
15 : 8	A1	Accumulator 1 Register Default Value: 0
7 : 0	A0	Accumulator 0 Register Default Value: 0

38.1.3 UDB_CAT16_A2

Accumulator Registers {A1,A0}

Address: 0x400F1004

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	A0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	A1 [15:8]							

Bits	Name	Description
15 : 8	A1	Accumulator 1 Register Default Value: 0
7 : 0	A0	Accumulator 0 Register Default Value: 0

38.1.4 UDB_CAT16_A3

Accumulator Registers {A1,A0}

Address: 0x400F1006

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	A0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	A1 [15:8]							

Bits	Name	Description
15 : 8	A1	Accumulator 1 Register Default Value: 0
7 : 0	A0	Accumulator 0 Register Default Value: 0

38.1.5 UDB_CAT16_D0

Data Registers {D1,D0}

Address: 0x400F1040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	D0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	D1 [15:8]							

Bits	Name	Description
15 : 8	D1	Data 1 Register Default Value: 0
7 : 0	D0	Data 0 Register Default Value: 0

38.1.6 UDB_CAT16_D1

Data Registers {D1,D0}

Address: 0x400F1042

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	D0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	D1 [15:8]							

Bits	Name	Description
15 : 8	D1	Data 1 Register Default Value: 0
7 : 0	D0	Data 0 Register Default Value: 0

38.1.7 UDB_CAT16_D2

Data Registers {D1,D0}

Address: 0x400F1044

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	D0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	D1 [15:8]							

Bits	Name	Description
15 : 8	D1	Data 1 Register Default Value: 0
7 : 0	D0	Data 0 Register Default Value: 0

38.1.8 UDB_CAT16_D3

Data Registers {D1,D0}

Address: 0x400F1046

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	D0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	D1 [15:8]							

Bits	Name	Description
15 : 8	D1	Data 1 Register Default Value: 0
7 : 0	D0	Data 0 Register Default Value: 0

38.1.9 UDB_CAT16_F0

FIFOs {F1,F0}

Address: 0x400F1080

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	F0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	F1 [15:8]							

Bits	Name	Description
15 : 8	F1	FIFO 1 Default Value: X
7 : 0	F0	FIFO 0 Default Value: X

38.1.10 UDB_CAT16_F1

FIFOs {F1,F0}

Address: 0x400F1082

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	F0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	F1 [15:8]							

Bits	Name	Description
15 : 8	F1	FIFO 1 Default Value: X
7 : 0	F0	FIFO 0 Default Value: X

38.1.11 UDB_CAT16_F2

FIFOs {F1,F0}

Address: 0x400F1084

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	F0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	F1 [15:8]							

Bits	Name	Description
15 : 8	F1	FIFO 1 Default Value: X
7 : 0	F0	FIFO 0 Default Value: X

38.1.12 UDB_CAT16_F3

FIFOs {F1,F0}

Address: 0x400F1086

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	F0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	F1 [15:8]							

Bits	Name	Description
15 : 8	F1	FIFO 1 Default Value: X
7 : 0	F0	FIFO 0 Default Value: X

38.1.13 UDB_CAT16_CTL_ST0

Status and Control Registers {CTL,ST}

Address: 0x400F10C0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	ST [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CTL [15:8]							

Bits	Name	Description
15 : 8	CTL	Control Register Default Value: 0
7 : 0	ST	Status Register Default Value: 0

38.1.14 UDB_CAT16_CTL_ST1

Status and Control Registers {CTL,ST}

Address: 0x400F10C2

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	ST [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CTL [15:8]							

Bits	Name	Description
15 : 8	CTL	Control Register Default Value: 0
7 : 0	ST	Status Register Default Value: 0

38.1.15 UDB_CAT16_CTL_ST2

Status and Control Registers {CTL,ST}

Address: 0x400F10C4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	ST [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CTL [15:8]							

Bits	Name	Description
15 : 8	CTL	Control Register Default Value: 0
7 : 0	ST	Status Register Default Value: 0

38.1.16 UDB_CAT16_CTL_ST3

Status and Control Registers {CTL,ST}

Address: 0x400F10C6

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	ST [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CTL [15:8]							

Bits	Name	Description
15 : 8	CTL	Control Register Default Value: 0
7 : 0	ST	Status Register Default Value: 0

38.1.17 UDB_CAT16_ACTL_MSK0

Mask and Auxiliary Control Registers {ACTL,MSK}

Address: 0x400F1100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	MSK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		RW	RW	RW	RW	RW	RW
Name	None [15:14]		CNT_START	INT_EN	FIFO1_LVL	FIFO0_LVL	FIFO1_CLR	FIFO0_CLR

Bits	Name	Description
13	CNT_START	Control Register Counter Enable Default Value: 0 **0x0: DISABLE:** Counter disabled **0x1: ENABLE:** Counter enabled
12	INT_EN	enable interrupt Default Value: 0 **0x0: DISABLE:** Interrupt disabled **0x1: ENABLE:** Interrupt enabled
11	FIFO1_LVL	FIFO fill status level control Default Value: 0 **0x0: NORMAL:** input mode: FIFO not full; output mode: FIFO not empty **0x1: MID:** input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full
10	FIFO0_LVL	FIFO fill status level control Default Value: 0 **0x0: NORMAL:** input mode: FIFO not full; output mode: FIFO not empty **0x1: MID:** input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full
9	FIFO1_CLR	FIFO clear Default Value: 0

(continued)

		0x0: NORMAL: Normal FIFO operation **0x1: CLEAR:** Clear FIFO state
8	FIFO0_CLR	FIFO clear Default Value: 0 **0x0: NORMAL:** Normal FIFO operation **0x1: CLEAR:** Clear FIFO state
7 : 0	MSK	Interrupt Mask Register Default Value: 0

38.1.18 UDB_CAT16_ACTL_MSK1

Mask and Auxiliary Control Registers {ACTL,MSK}

Address: 0x400F1102

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	MSK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		RW	RW	RW	RW	RW	RW
Name	None [15:14]		CNT_START	INT_EN	FIFO1_LVL	FIFO0_LVL	FIFO1_CLR	FIFO0_CLR

Bits	Name	Description
13	CNT_START	Control Register Counter Enable Default Value: 0 **0x0: DISABLE:** Counter disabled **0x1: ENABLE:** Counter enabled
12	INT_EN	enable interrupt Default Value: 0 **0x0: DISABLE:** Interrupt disabled **0x1: ENABLE:** Interrupt enabled
11	FIFO1_LVL	FIFO fill status level control Default Value: 0 **0x0: NORMAL:** input mode: FIFO not full; output mode: FIFO not empty **0x1: MID:** input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full
10	FIFO0_LVL	FIFO fill status level control Default Value: 0 **0x0: NORMAL:** input mode: FIFO not full; output mode: FIFO not empty **0x1: MID:** input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full
9	FIFO1_CLR	FIFO clear Default Value: 0

(continued)

		0x0: NORMAL: Normal FIFO operation **0x1: CLEAR:** Clear FIFO state
8	FIFO0_CLR	FIFO clear Default Value: 0 **0x0: NORMAL:** Normal FIFO operation **0x1: CLEAR:** Clear FIFO state
7 : 0	MSK	Interrupt Mask Register Default Value: 0

38.1.19 UDB_CAT16_ACTL_MSK2

Mask and Auxiliary Control Registers {ACTL,MSK}

Address: 0x400F1104

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	MSK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		RW	RW	RW	RW	RW	RW
Name	None [15:14]		CNT_START	INT_EN	FIFO1_LVL	FIFO0_LVL	FIFO1_CLR	FIFO0_CLR

Bits	Name	Description
13	CNT_START	Control Register Counter Enable Default Value: 0 **0x0: DISABLE:** Counter disabled **0x1: ENABLE:** Counter enabled
12	INT_EN	enable interrupt Default Value: 0 **0x0: DISABLE:** Interrupt disabled **0x1: ENABLE:** Interrupt enabled
11	FIFO1_LVL	FIFO fill status level control Default Value: 0 **0x0: NORMAL:** input mode: FIFO not full; output mode: FIFO not empty **0x1: MID:** input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full
10	FIFO0_LVL	FIFO fill status level control Default Value: 0 **0x0: NORMAL:** input mode: FIFO not full; output mode: FIFO not empty **0x1: MID:** input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full
9	FIFO1_CLR	FIFO clear Default Value: 0

(continued)

		0x0: NORMAL: Normal FIFO operation **0x1: CLEAR:** Clear FIFO state
8	FIFO0_CLR	FIFO clear Default Value: 0 **0x0: NORMAL:** Normal FIFO operation **0x1: CLEAR:** Clear FIFO state
7 : 0	MSK	Interrupt Mask Register Default Value: 0

38.1.20 UDB_CAT16_ACTL_MSK3

Mask and Auxiliary Control Registers {ACTL,MSK}

Address: 0x400F1106

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	MSK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		RW	RW	RW	RW	RW	RW
Name	None [15:14]		CNT_START	INT_EN	FIFO1_LVL	FIFO0_LVL	FIFO1_CLR	FIFO0_CLR

Bits	Name	Description
13	CNT_START	Control Register Counter Enable Default Value: 0 **0x0: DISABLE:** Counter disabled **0x1: ENABLE:** Counter enabled
12	INT_EN	enable interrupt Default Value: 0 **0x0: DISABLE:** Interrupt disabled **0x1: ENABLE:** Interrupt enabled
11	FIFO1_LVL	FIFO fill status level control Default Value: 0 **0x0: NORMAL:** input mode: FIFO not full; output mode: FIFO not empty **0x1: MID:** input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full
10	FIFO0_LVL	FIFO fill status level control Default Value: 0 **0x0: NORMAL:** input mode: FIFO not full; output mode: FIFO not empty **0x1: MID:** input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full
9	FIFO1_CLR	FIFO clear Default Value: 0

(continued)

		0x0: NORMAL: Normal FIFO operation **0x1: CLEAR:** Clear FIFO state
8	FIFO0_CLR	FIFO clear Default Value: 0 **0x0: NORMAL:** Normal FIFO operation **0x1: CLEAR:** Clear FIFO state
7 : 0	MSK	Interrupt Mask Register Default Value: 0

38.1.21 UDB_CAT16_MC0

PLD Macrocell Read Registers {00,MC}

Address: 0x400F1140

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	W				W			
Name	PLD1_MC [7:4]				PLD0_MC [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PLD1_MC	PLD1 Macrocell Read Register Default Value: 0
3 : 0	PLD0_MC	PLD0 Macrocell Read Register Default Value: 0

38.1.22 UDB_CAT16_MC1

PLD Macrocell Read Registers {00,MC}

Address: 0x400F1142

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	W				W			
Name	PLD1_MC [7:4]				PLD0_MC [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PLD1_MC	PLD1 Macrocell Read Register Default Value: 0
3 : 0	PLD0_MC	PLD0 Macrocell Read Register Default Value: 0

38.1.23 UDB_CAT16_MC2

PLD Macrocell Read Registers {00,MC}

Address: 0x400F1144

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	W				W			
Name	PLD1_MC [7:4]				PLD0_MC [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PLD1_MC	PLD1 Macrocell Read Register Default Value: 0
3 : 0	PLD0_MC	PLD0 Macrocell Read Register Default Value: 0

38.1.24 UDB_CAT16_MC3

PLD Macrocell Read Registers {00,MC}

Address: 0x400F1146

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	W				W			
Name	PLD1_MC [7:4]				PLD0_MC [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	Name	Description
7 : 4	PLD1_MC	PLD1 Macrocell Read Register Default Value: 0
3 : 0	PLD0_MC	PLD0 Macrocell Read Register Default Value: 0

39 UDB 16-Bit Working (WRK16DEF) Registers

This section discusses the WRK16DEF registers. It lists all the registers in mapping tables, in address order.

39.1 Register Details

Register Name	Address
UDB_W16_A00	0x400F1000
UDB_W16_A01	0x400F1002
UDB_W16_A02	0x400F1004
UDB_W16_A10	0x400F1020
UDB_W16_A11	0x400F1022
UDB_W16_A12	0x400F1024
UDB_W16_D00	0x400F1040
UDB_W16_D01	0x400F1042
UDB_W16_D02	0x400F1044
UDB_W16_D10	0x400F1060
UDB_W16_D11	0x400F1062
UDB_W16_D12	0x400F1064
UDB_W16_F00	0x400F1080
UDB_W16_F01	0x400F1082
UDB_W16_F02	0x400F1084
UDB_W16_F10	0x400F10A0
UDB_W16_F11	0x400F10A2
UDB_W16_F12	0x400F10A4
UDB_W16_ST0	0x400F10C0
UDB_W16_ST1	0x400F10C2
UDB_W16_ST2	0x400F10C4
UDB_W16_CTL0	0x400F10E0
UDB_W16_CTL1	0x400F10E2
UDB_W16_CTL2	0x400F10E4
UDB_W16_MSK0	0x400F1100
UDB_W16_MSK1	0x400F1102

Register Name	Address
UDB_W16_MSK2	0x400F1104
UDB_W16_ACTL0	0x400F1120
UDB_W16_ACTL1	0x400F1122
UDB_W16_ACTL2	0x400F1124
UDB_W16_MC0	0x400F1140
UDB_W16_MC1	0x400F1142
UDB_W16_MC2	0x400F1144

39.1.1 UDB_W16_A00

Accumulator 0

Address: 0x400F1000

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	A0_LS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	A0_MS [15:8]							

Bits	Name	Description
15 : 8	A0_MS	Accumulator 0 for UDB[n+1] Default Value: 0
7 : 0	A0_LS	Accumulator 0 for UDB[n] Default Value: 0

39.1.2 UDB_W16_A01

Accumulator 0

Address: 0x400F1002

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	A0_LS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	A0_MS [15:8]							

Bits	Name	Description
15 : 8	A0_MS	Accumulator 0 for UDB[n+1] Default Value: 0
7 : 0	A0_LS	Accumulator 0 for UDB[n] Default Value: 0

39.1.3 UDB_W16_A02

Accumulator 0

Address: 0x400F1004

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	A0_LS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	A0_MS [15:8]							

Bits	Name	Description
15 : 8	A0_MS	Accumulator 0 for UDB[n+1] Default Value: 0
7 : 0	A0_LS	Accumulator 0 for UDB[n] Default Value: 0

39.1.4 UDB_W16_A10

Accumulator 1

Address: 0x400F1020

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	A1_LS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	A1_MS [15:8]							

Bits	Name	Description
15 : 8	A1_MS	Accumulator 1 for UDB[n+1] Default Value: 0
7 : 0	A1_LS	Accumulator 1 for UDB[n] Default Value: 0

39.1.5 UDB_W16_A11

Accumulator 1

Address: 0x400F1022

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	A1_LS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	A1_MS [15:8]							

Bits	Name	Description
15 : 8	A1_MS	Accumulator 1 for UDB[n+1] Default Value: 0
7 : 0	A1_LS	Accumulator 1 for UDB[n] Default Value: 0

39.1.6 UDB_W16_A12

Accumulator 1

Address: 0x400F1024

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	A1_LS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	A1_MS [15:8]							

Bits	Name	Description
15 : 8	A1_MS	Accumulator 1 for UDB[n+1] Default Value: 0
7 : 0	A1_LS	Accumulator 1 for UDB[n] Default Value: 0

39.1.7 UDB_W16_D00

Data 0

Address: 0x400F1040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	D0_LS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	D0_MS [15:8]							

Bits	Name	Description
15 : 8	D0_MS	Data 0 for UDB[n+1] Default Value: 0
7 : 0	D0_LS	Data 0 for UDB[n] Default Value: 0

39.1.8 UDB_W16_D01

Data 0

Address: 0x400F1042

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	D0_LS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	D0_MS [15:8]							

Bits	Name	Description
15 : 8	D0_MS	Data 0 for UDB[n+1] Default Value: 0
7 : 0	D0_LS	Data 0 for UDB[n] Default Value: 0

39.1.9 UDB_W16_D02

Data 0

Address: 0x400F1044

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	D0_LS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	D0_MS [15:8]							

Bits	Name	Description
15 : 8	D0_MS	Data 0 for UDB[n+1] Default Value: 0
7 : 0	D0_LS	Data 0 for UDB[n] Default Value: 0

39.1.10 UDB_W16_D10

Data 1

Address: 0x400F1060

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	D1_LS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	D1_MS [15:8]							

Bits	Name	Description
15 : 8	D1_MS	Data 1 for UDB[n+1] Default Value: 0
7 : 0	D1_LS	Data 1 for UDB[n] Default Value: 0

39.1.11 UDB_W16_D11

Data 1

Address: 0x400F1062

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	D1_LS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	D1_MS [15:8]							

Bits	Name	Description
15 : 8	D1_MS	Data 1 for UDB[n+1] Default Value: 0
7 : 0	D1_LS	Data 1 for UDB[n] Default Value: 0

39.1.12 UDB_W16_D12

Data 1

Address: 0x400F1064

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	D1_LS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	D1_MS [15:8]							

Bits	Name	Description
15 : 8	D1_MS	Data 1 for UDB[n+1] Default Value: 0
7 : 0	D1_LS	Data 1 for UDB[n] Default Value: 0

39.1.13 UDB_W16_F00

FIFO 0

Address: 0x400F1080

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	F0_LS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	F0_MS [15:8]							

Bits	Name	Description
15 : 8	F0_MS	Fifo 0 for UDB[n+1] Default Value: X
7 : 0	F0_LS	Fifo 0 for UDB[n] Default Value: X

39.1.14 UDB_W16_F01

FIFO 0

Address: 0x400F1082

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	F0_LS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	F0_MS [15:8]							

Bits	Name	Description
15 : 8	F0_MS	Fifo 0 for UDB[n+1] Default Value: X
7 : 0	F0_LS	Fifo 0 for UDB[n] Default Value: X

39.1.15 UDB_W16_F02

FIFO 0

Address: 0x400F1084

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	F0_LS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	F0_MS [15:8]							

Bits	Name	Description
15 : 8	F0_MS	Fifo 0 for UDB[n+1] Default Value: X
7 : 0	F0_LS	Fifo 0 for UDB[n] Default Value: X

39.1.16 UDB_W16_F10

FIFO 1

Address: 0x400F10A0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	F1_LS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	F1_MS [15:8]							

Bits	Name	Description
15 : 8	F1_MS	Fifo 1 for UDB[n+1] Default Value: X
7 : 0	F1_LS	Fifo 1 for UDB[n] Default Value: X

39.1.17 UDB_W16_F11

FIFO 1

Address: 0x400F10A2

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	F1_LS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	F1_MS [15:8]							

Bits	Name	Description
15 : 8	F1_MS	Fifo 1 for UDB[n+1] Default Value: X
7 : 0	F1_LS	Fifo 1 for UDB[n] Default Value: X

39.1.18 UDB_W16_F12

FIFO 1

Address: 0x400F10A4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	F1_LS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	F1_MS [15:8]							

Bits	Name	Description
15 : 8	F1_MS	Fifo 1 for UDB[n+1] Default Value: X
7 : 0	F1_LS	Fifo 1 for UDB[n] Default Value: X

39.1.19 UDB_W16_ST0

Status Register

Address: 0x400F10C0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	ST_LS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	ST_MS [15:8]							

Bits	Name	Description
15 : 8	ST_MS	Status register for UDB[n+1] Default Value: 0
7 : 0	ST_LS	Status register for UDB[n] Default Value: 0

39.1.20 UDB_W16_ST1

Status Register

Address: 0x400F10C2

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	ST_LS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	ST_MS [15:8]							

Bits	Name	Description
15 : 8	ST_MS	Status register for UDB[n+1] Default Value: 0
7 : 0	ST_LS	Status register for UDB[n] Default Value: 0

39.1.21 UDB_W16_ST2

Status Register

Address: 0x400F10C4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	ST_LS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	ST_MS [15:8]							

Bits	Name	Description
15 : 8	ST_MS	Status register for UDB[n+1] Default Value: 0
7 : 0	ST_LS	Status register for UDB[n] Default Value: 0

39.1.22 UDB_W16_CTL0

Control Register

Address: 0x400F10E0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CTL_LS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CTL_MS [15:8]							

Bits	Name	Description
15 : 8	CTL_MS	Control register for UDB[n+1] Default Value: 0
7 : 0	CTL_LS	Control register for UDB[n] Default Value: 0

39.1.23 UDB_W16_CTL1

Control Register

Address: 0x400F10E2

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CTL_LS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CTL_MS [15:8]							

Bits	Name	Description
15 : 8	CTL_MS	Control register for UDB[n+1] Default Value: 0
7 : 0	CTL_LS	Control register for UDB[n] Default Value: 0

39.1.24 UDB_W16_CTL2

Control Register

Address: 0x400F10E4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CTL_LS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CTL_MS [15:8]							

Bits	Name	Description
15 : 8	CTL_MS	Control register for UDB[n+1] Default Value: 0
7 : 0	CTL_LS	Control register for UDB[n] Default Value: 0

39.1.25 UDB_W16_MSK0

Interrupt Mask

Address: 0x400F1100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW						
HW Access	None	R						
Name	None	MSK_LS [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW						
HW Access	None	R						
Name	None	MSK_MS [14:8]						

Bits	Name	Description
14 : 8	MSK_MS	Interrupt Mask Register Default Value: 0
6 : 0	MSK_LS	Interrupt Mask Register Default Value: 0

39.1.26 UDB_W16_MSK1

Interrupt Mask

Address: 0x400F1102

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW						
HW Access	None	R						
Name	None	MSK_LS [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW						
HW Access	None	R						
Name	None	MSK_MS [14:8]						

Bits	Name	Description
14 : 8	MSK_MS	Interrupt Mask Register Default Value: 0
6 : 0	MSK_LS	Interrupt Mask Register Default Value: 0

39.1.27 UDB_W16_MSK2

Interrupt Mask

Address: 0x400F1104

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW						
HW Access	None	R						
Name	None	MSK_LS [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW						
HW Access	None	R						
Name	None	MSK_MS [14:8]						

Bits	Name	Description
14 : 8	MSK_MS	Interrupt Mask Register Default Value: 0
6 : 0	MSK_LS	Interrupt Mask Register Default Value: 0

39.1.28 UDB_W16_ACTL0

Auxiliary Control

Address: 0x400F1120

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		RW	RW	RW	RW	RW	RW
Name	None [7:6]		CNT_START_LS	INT_EN_LS	FIFO1_LVL_LS	FIFO0_LVL_LS	FIFO1_CLR_LS	FIFO0_CLR_LS

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		RW	RW	RW	RW	RW	RW
Name	None [15:14]		CNT_START_MS	INT_EN_MS	FIFO1_LVL_MS	FIFO0_LVL_MS	FIFO1_CLR_MS	FIFO0_CLR_MS

Bits	Name	Description
13	CNT_START_MS	Control Register Counter Enable Default Value: 0 **0x0: DISABLE:** Counter disabled **0x1: ENABLE:** Counter enabled
12	INT_EN_MS	enable interrupt Default Value: 0 **0x0: DISABLE:** Interrupt disabled **0x1: ENABLE:** Interrupt enabled
11	FIFO1_LVL_MS	FIFO fill status level control Default Value: 0 **0x0: NORMAL:** input mode: FIFO not full; output mode: FIFO not empty **0x1: MID:** input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full
10	FIFO0_LVL_MS	FIFO fill status level control Default Value: 0 **0x0: NORMAL:** input mode: FIFO not full; output mode: FIFO not empty **0x1: MID:** input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

(continued)

9	FIFO1_CLR_MS	FIFO clear Default Value: 0 **0x0: NORMAL:** Normal FIFO operation **0x1: CLEAR:** Clear FIFO state
8	FIFO0_CLR_MS	FIFO clear Default Value: 0 **0x0: NORMAL:** Normal FIFO operation **0x1: CLEAR:** Clear FIFO state
5	CNT_START_LS	Control Register Counter Enable Default Value: 0 **0x0: DISABLE:** Counter disabled **0x1: ENABLE:** Counter enabled
4	INT_EN_LS	enable interrupt Default Value: 0 **0x0: DISABLE:** Interrupt disabled **0x1: ENABLE:** Interrupt enabled
3	FIFO1_LVL_LS	FIFO fill status level control Default Value: 0 **0x0: NORMAL:** input mode: FIFO not full; output mode: FIFO not empty **0x1: MID:** input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full
2	FIFO0_LVL_LS	FIFO fill status level control Default Value: 0 **0x0: NORMAL:** input mode: FIFO not full; output mode: FIFO not empty **0x1: MID:** input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full
1	FIFO1_CLR_LS	FIFO clear Default Value: 0 **0x0: NORMAL:** Normal FIFO operation **0x1: CLEAR:** Clear FIFO state
0	FIFO0_CLR_LS	FIFO clear Default Value: 0

(continued)

0x0: NORMAL:
Normal FIFO operation

0x1: CLEAR:
Clear FIFO state

39.1.29 UDB_W16_ACTL1

Auxiliary Control

Address: 0x400F1122

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		RW	RW	RW	RW	RW	RW
Name	None [7:6]		CNT_START_LS	INT_EN_LS	FIFO1_LVL_LS	FIFO0_LVL_LS	FIFO1_CLR_LS	FIFO0_CLR_LS

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		RW	RW	RW	RW	RW	RW
Name	None [15:14]		CNT_START_MS	INT_EN_MS	FIFO1_LVL_MS	FIFO0_LVL_MS	FIFO1_CLR_MS	FIFO0_CLR_MS

Bits	Name	Description
13	CNT_START_MS	Control Register Counter Enable Default Value: 0 **0x0: DISABLE:** Counter disabled **0x1: ENABLE:** Counter enabled
12	INT_EN_MS	enable interrupt Default Value: 0 **0x0: DISABLE:** Interrupt disabled **0x1: ENABLE:** Interrupt enabled
11	FIFO1_LVL_MS	FIFO fill status level control Default Value: 0 **0x0: NORMAL:** input mode: FIFO not full; output mode: FIFO not empty **0x1: MID:** input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full
10	FIFO0_LVL_MS	FIFO fill status level control Default Value: 0 **0x0: NORMAL:** input mode: FIFO not full; output mode: FIFO not empty **0x1: MID:** input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

(continued)

9	FIFO1_CLR_MS	FIFO clear Default Value: 0 **0x0: NORMAL:** Normal FIFO operation **0x1: CLEAR:** Clear FIFO state
8	FIFO0_CLR_MS	FIFO clear Default Value: 0 **0x0: NORMAL:** Normal FIFO operation **0x1: CLEAR:** Clear FIFO state
5	CNT_START_LS	Control Register Counter Enable Default Value: 0 **0x0: DISABLE:** Counter disabled **0x1: ENABLE:** Counter enabled
4	INT_EN_LS	enable interrupt Default Value: 0 **0x0: DISABLE:** Interrupt disabled **0x1: ENABLE:** Interrupt enabled
3	FIFO1_LVL_LS	FIFO fill status level control Default Value: 0 **0x0: NORMAL:** input mode: FIFO not full; output mode: FIFO not empty **0x1: MID:** input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full
2	FIFO0_LVL_LS	FIFO fill status level control Default Value: 0 **0x0: NORMAL:** input mode: FIFO not full; output mode: FIFO not empty **0x1: MID:** input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full
1	FIFO1_CLR_LS	FIFO clear Default Value: 0 **0x0: NORMAL:** Normal FIFO operation **0x1: CLEAR:** Clear FIFO state
0	FIFO0_CLR_LS	FIFO clear Default Value: 0

(continued)

0x0: NORMAL:
Normal FIFO operation

0x1: CLEAR:
Clear FIFO state

39.1.30 UDB_W16_ACTL2

Auxiliary Control

Address: 0x400F1124

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		RW	RW	RW	RW	RW	RW
Name	None [7:6]		CNT_START_LS	INT_EN_LS	FIFO1_LVL_LS	FIFO0_LVL_LS	FIFO1_CLR_LS	FIFO0_CLR_LS

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		RW	RW	RW	RW	RW	RW
Name	None [15:14]		CNT_START_MS	INT_EN_MS	FIFO1_LVL_MS	FIFO0_LVL_MS	FIFO1_CLR_MS	FIFO0_CLR_MS

Bits	Name	Description
13	CNT_START_MS	Control Register Counter Enable Default Value: 0 **0x0: DISABLE:** Counter disabled **0x1: ENABLE:** Counter enabled
12	INT_EN_MS	enable interrupt Default Value: 0 **0x0: DISABLE:** Interrupt disabled **0x1: ENABLE:** Interrupt enabled
11	FIFO1_LVL_MS	FIFO fill status level control Default Value: 0 **0x0: NORMAL:** input mode: FIFO not full; output mode: FIFO not empty **0x1: MID:** input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full
10	FIFO0_LVL_MS	FIFO fill status level control Default Value: 0 **0x0: NORMAL:** input mode: FIFO not full; output mode: FIFO not empty **0x1: MID:** input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full

(continued)

9	FIFO1_CLR_MS	FIFO clear Default Value: 0 **0x0: NORMAL:** Normal FIFO operation **0x1: CLEAR:** Clear FIFO state
8	FIFO0_CLR_MS	FIFO clear Default Value: 0 **0x0: NORMAL:** Normal FIFO operation **0x1: CLEAR:** Clear FIFO state
5	CNT_START_LS	Control Register Counter Enable Default Value: 0 **0x0: DISABLE:** Counter disabled **0x1: ENABLE:** Counter enabled
4	INT_EN_LS	enable interrupt Default Value: 0 **0x0: DISABLE:** Interrupt disabled **0x1: ENABLE:** Interrupt enabled
3	FIFO1_LVL_LS	FIFO fill status level control Default Value: 0 **0x0: NORMAL:** input mode: FIFO not full; output mode: FIFO not empty **0x1: MID:** input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full
2	FIFO0_LVL_LS	FIFO fill status level control Default Value: 0 **0x0: NORMAL:** input mode: FIFO not full; output mode: FIFO not empty **0x1: MID:** input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full
1	FIFO1_CLR_LS	FIFO clear Default Value: 0 **0x0: NORMAL:** Normal FIFO operation **0x1: CLEAR:** Clear FIFO state
0	FIFO0_CLR_LS	FIFO clear Default Value: 0

(continued)

0x0: NORMAL:
Normal FIFO operation

0x1: CLEAR:
Clear FIFO state

39.1.31 UDB_W16_MC0

PLD Macrocell reading

Address: 0x400F1140

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	RW				RW			
Name	PLD1_MC_LS [7:4]				PLD0_MC_LS [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	R				R			
HW Access	RW				RW			
Name	PLD1_MC_MS [15:12]				PLD0_MC_MS [11:8]			

Bits	Name	Description
15 : 12	PLD1_MC_MS	Read Macrocell 1 for UDB[n+1] Default Value: 0
11 : 8	PLD0_MC_MS	Read Macrocell 0 for UDB[n+1] Default Value: 0
7 : 4	PLD1_MC_LS	Read Macrocell 1 for UDB[n] Default Value: 0
3 : 0	PLD0_MC_LS	Read Macrocell 0 for UDB[n] Default Value: 0

39.1.32 UDB_W16_MC1

PLD Macrocell reading

Address: 0x400F1142

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	RW				RW			
Name	PLD1_MC_LS [7:4]				PLD0_MC_LS [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	R				R			
HW Access	RW				RW			
Name	PLD1_MC_MS [15:12]				PLD0_MC_MS [11:8]			

Bits	Name	Description
15 : 12	PLD1_MC_MS	Read Macrocell 1 for UDB[n+1] Default Value: 0
11 : 8	PLD0_MC_MS	Read Macrocell 0 for UDB[n+1] Default Value: 0
7 : 4	PLD1_MC_LS	Read Macrocell 1 for UDB[n] Default Value: 0
3 : 0	PLD0_MC_LS	Read Macrocell 0 for UDB[n] Default Value: 0

39.1.33 UDB_W16_MC2

PLD Macrocell reading

Address: 0x400F1144

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	RW				RW			
Name	PLD1_MC_LS [7:4]				PLD0_MC_LS [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	R				R			
HW Access	RW				RW			
Name	PLD1_MC_MS [15:12]				PLD0_MC_MS [11:8]			

Bits	Name	Description
15 : 12	PLD1_MC_MS	Read Macrocell 1 for UDB[n+1] Default Value: 0
11 : 8	PLD0_MC_MS	Read Macrocell 0 for UDB[n+1] Default Value: 0
7 : 4	PLD1_MC_LS	Read Macrocell 1 for UDB[n] Default Value: 0
3 : 0	PLD0_MC_LS	Read Macrocell 0 for UDB[n] Default Value: 0

40 UDB 32-Bit Working (WRK32) Registers

This section discusses the WRK32 registers. It lists all the registers in mapping tables, in address order.

40.1 Register Details

Register Name	Address
UDB_W32_A0	0x400F2000
UDB_W32_A1	0x400F2040
UDB_W32_D0	0x400F2080
UDB_W32_D1	0x400F20C0
UDB_W32_F0	0x400F2100
UDB_W32_F1	0x400F2140
UDB_W32_ST	0x400F2180
UDB_W32_CTL	0x400F21C0
UDB_W32_MSK	0x400F2200
UDB_W32_ACTL	0x400F2240
UDB_W32_MC	0x400F2280

40.1.1 UDB_W32_A0

Accumulator 0

Address: 0x400F2000

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	A0_0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	A0_1 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	A0_2 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	A0_3 [31:24]							

Bits	Name	Description
31 : 24	A0_3	Accumulator 0 for UDB[n+3] Default Value: 0
23 : 16	A0_2	Accumulator 0 for UDB[n+2] Default Value: 0
15 : 8	A0_1	Accumulator 0 for UDB[n+1] Default Value: 0
7 : 0	A0_0	Accumulator 0 for UDB[n] Default Value: 0

40.1.2 UDB_W32_A1

Accumulator 1

Address: 0x400F2040

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	A1_0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	A1_1 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	A1_2 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	A1_3 [31:24]							

Bits	Name	Description
31 : 24	A1_3	Accumulator 1 for UDB[n+3] Default Value: 0
23 : 16	A1_2	Accumulator 1 for UDB[n+2] Default Value: 0
15 : 8	A1_1	Accumulator 1 for UDB[n+1] Default Value: 0
7 : 0	A1_0	Accumulator 1 for UDB[n] Default Value: 0

40.1.3 UDB_W32_D0

Data 0

Address: 0x400F2080

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	D0_0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	D0_1 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	D0_2 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	D0_3 [31:24]							

Bits	Name	Description
31 : 24	D0_3	Data 0 for UDB[n+3] Default Value: 0
23 : 16	D0_2	Data 0 for UDB[n+2] Default Value: 0
15 : 8	D0_1	Data 0 for UDB[n+1] Default Value: 0
7 : 0	D0_0	Data 0 for UDB[n] Default Value: 0

40.1.4 UDB_W32_D1

Data 1

Address: 0x400F20C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	D1_0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	D1_1 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	D1_2 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	D1_3 [31:24]							

Bits	Name	Description
31 : 24	D1_3	Data 1 for UDB[n+3] Default Value: 0
23 : 16	D1_2	Data 1 for UDB[n+2] Default Value: 0
15 : 8	D1_1	Data 1 for UDB[n+1] Default Value: 0
7 : 0	D1_0	Data 1 for UDB[n] Default Value: 0

40.1.5 UDB_W32_F0

FIFO 0

Address: 0x400F2100

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	F0_0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	F0_1 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	F0_2 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	F0_3 [31:24]							

Bits	Name	Description
31 : 24	F0_3	Fifo 0 for UDB[n+3] Default Value: X
23 : 16	F0_2	Fifo 0 for UDB[n+2] Default Value: X
15 : 8	F0_1	Fifo 0 for UDB[n+1] Default Value: X
7 : 0	F0_0	Fifo 0 for UDB[n] Default Value: X

40.1.6 UDB_W32_F1

FIFO 1

Address: 0x400F2140

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	F1_0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	F1_1 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	F1_2 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	F1_3 [31:24]							

Bits	Name	Description
31 : 24	F1_3	Fifo 1 for UDB[n+3] Default Value: X
23 : 16	F1_2	Fifo 1 for UDB[n+2] Default Value: X
15 : 8	F1_1	Fifo 1 for UDB[n+1] Default Value: X
7 : 0	F1_0	Fifo 1 for UDB[n] Default Value: X

40.1.7 UDB_W32_ST

Status Register

Address: 0x400F2180

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	ST_0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	ST_1 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	ST_2 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	ST_3 [31:24]							

Bits	Name	Description
31 : 24	ST_3	Status register for UDB[n+3] Default Value: 0
23 : 16	ST_2	Status register for UDB[n+2] Default Value: 0
15 : 8	ST_1	Status register for UDB[n+1] Default Value: 0
7 : 0	ST_0	Status register for UDB[n] Default Value: 0

40.1.8 UDB_W32_CTL

Control Register

Address: 0x400F21C0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CTL_0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CTL_1 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	CTL_2 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	CTL_3 [31:24]							

Bits	Name	Description
31 : 24	CTL_3	Control register for UDB[n+3] Default Value: 0
23 : 16	CTL_2	Control register for UDB[n+2] Default Value: 0
15 : 8	CTL_1	Control register for UDB[n+1] Default Value: 0
7 : 0	CTL_0	Control register for UDB[n] Default Value: 0

40.1.9 UDB_W32_MSK

Interrupt Mask

Address: 0x400F2200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW						
HW Access	None	R						
Name	None	MSK_0 [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW						
HW Access	None	R						
Name	None	MSK_1 [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	None	RW						
HW Access	None	R						
Name	None	MSK_2 [22:16]						

Bits	31	30	29	28	27	26	25	24
SW Access	None	RW						
HW Access	None	R						
Name	None	MSK_3 [30:24]						

Bits	Name	Description
30 : 24	MSK_3	Interrupt Mask Register Default Value: 0
22 : 16	MSK_2	Interrupt Mask Register Default Value: 0
14 : 8	MSK_1	Interrupt Mask Register Default Value: 0
6 : 0	MSK_0	Interrupt Mask Register Default Value: 0

40.1.10 UDB_W32_ACTL

Auxiliary Control

Address: 0x400F2240

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		RW	RW	RW	RW	RW	RW
Name	None [7:6]		CNT_START_0	INT_EN_0	FIFO1_LVL_0	FIFO0_LVL_0	FIFO1_CLR_0	FIFO0_CLR_0

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		RW	RW	RW	RW	RW	RW
Name	None [15:14]		CNT_START_1	INT_EN_1	FIFO1_LVL_1	FIFO0_LVL_1	FIFO1_CLR_1	FIFO0_CLR_1

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		RW	RW	RW	RW	RW	RW
Name	None [23:22]		CNT_START_2	INT_EN_2	FIFO1_LVL_2	FIFO0_LVL_2	FIFO1_CLR_2	FIFO0_CLR_2

Bits	31	30	29	28	27	26	25	24
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		RW	RW	RW	RW	RW	RW
Name	None [31:30]		CNT_START_3	INT_EN_3	FIFO1_LVL_3	FIFO0_LVL_3	FIFO1_CLR_3	FIFO0_CLR_3

Bits	Name	Description
29	CNT_START_3	Control Register Counter Enable Default Value: 0 **0x0: DISABLE:** Counter disabled **0x1: ENABLE:** Counter enabled
28	INT_EN_3	enable interrupt Default Value: 0 **0x0: DISABLE:** Interrupt disabled **0x1: ENABLE:** Interrupt enabled

(continued)

27	FIFO1_LVL_3	FIFO fill status level control Default Value: 0 **0x0: NORMAL:** input mode: FIFO not full; output mode: FIFO not empty **0x1: MID:** input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full
26	FIFO0_LVL_3	FIFO fill status level control Default Value: 0 **0x0: NORMAL:** input mode: FIFO not full; output mode: FIFO not empty **0x1: MID:** input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full
25	FIFO1_CLR_3	FIFO clear Default Value: 0 **0x0: NORMAL:** Normal FIFO operation **0x1: CLEAR:** Clear FIFO state
24	FIFO0_CLR_3	FIFO clear Default Value: 0 **0x0: NORMAL:** Normal FIFO operation **0x1: CLEAR:** Clear FIFO state
21	CNT_START_2	Control Register Counter Enable Default Value: 0 **0x0: DISABLE:** Counter disabled **0x1: ENABLE:** Counter enabled
20	INT_EN_2	enable interrupt Default Value: 0 **0x0: DISABLE:** Interrupt disabled **0x1: ENABLE:** Interrupt enabled
19	FIFO1_LVL_2	FIFO fill status level control Default Value: 0 **0x0: NORMAL:** input mode: FIFO not full; output mode: FIFO not empty **0x1: MID:** input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full
18	FIFO0_LVL_2	FIFO fill status level control Default Value: 0

(continued)

		0x0: NORMAL: input mode: FIFO not full; output mode: FIFO not empty **0x1: MID:** input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full
17	FIFO1_CLR_2	FIFO clear Default Value: 0 **0x0: NORMAL:** Normal FIFO operation **0x1: CLEAR:** Clear FIFO state
16	FIFO0_CLR_2	FIFO clear Default Value: 0 **0x0: NORMAL:** Normal FIFO operation **0x1: CLEAR:** Clear FIFO state
13	CNT_START_1	Control Register Counter Enable Default Value: 0 **0x0: DISABLE:** Counter disabled **0x1: ENABLE:** Counter enabled
12	INT_EN_1	enable interrupt Default Value: 0 **0x0: DISABLE:** Interrupt disabled **0x1: ENABLE:** Interrupt enabled
11	FIFO1_LVL_1	FIFO fill status level control Default Value: 0 **0x0: NORMAL:** input mode: FIFO not full; output mode: FIFO not empty **0x1: MID:** input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full
10	FIFO0_LVL_1	FIFO fill status level control Default Value: 0 **0x0: NORMAL:** input mode: FIFO not full; output mode: FIFO not empty **0x1: MID:** input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full
9	FIFO1_CLR_1	FIFO clear Default Value: 0 **0x0: NORMAL:** Normal FIFO operation

(continued)

		0x1: CLEAR: Clear FIFO state
8	FIFO0_CLR_1	FIFO clear Default Value: 0 **0x0: NORMAL:** Normal FIFO operation **0x1: CLEAR:** Clear FIFO state
5	CNT_START_0	Control Register Counter Enable Default Value: 0 **0x0: DISABLE:** Counter disabled **0x1: ENABLE:** Counter enabled
4	INT_EN_0	enable interrupt Default Value: 0 **0x0: DISABLE:** Interrupt disabled **0x1: ENABLE:** Interrupt enabled
3	FIFO1_LVL_0	FIFO fill status level control Default Value: 0 **0x0: NORMAL:** input mode: FIFO not full; output mode: FIFO not empty **0x1: MID:** input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full
2	FIFO0_LVL_0	FIFO fill status level control Default Value: 0 **0x0: NORMAL:** input mode: FIFO not full; output mode: FIFO not empty **0x1: MID:** input mode: FIFO at least 1/2 empty; output mode: FIFO at least 1/2 full
1	FIFO1_CLR_0	FIFO clear Default Value: 0 **0x0: NORMAL:** Normal FIFO operation **0x1: CLEAR:** Clear FIFO state
0	FIFO0_CLR_0	FIFO clear Default Value: 0 **0x0: NORMAL:** Normal FIFO operation **0x1: CLEAR:** Clear FIFO state

40.1.11 UDB_W32_MC

PLD Macrocell reading

Address: 0x400F2280

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	RW				RW			
Name	PLD1_MC_0 [7:4]				PLD0_MC_0 [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	R				R			
HW Access	RW				RW			
Name	PLD1_MC_1 [15:12]				PLD0_MC_1 [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	R				R			
HW Access	RW				RW			
Name	PLD1_MC_2 [23:20]				PLD0_MC_2 [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	R				R			
HW Access	RW				RW			
Name	PLD1_MC_3 [31:28]				PLD0_MC_3 [27:24]			

Bits	Name	Description
31 : 28	PLD1_MC_3	Read Macrocell 1 for UDB[n+3] Default Value: 0
27 : 24	PLD0_MC_3	Read Macrocell 0 for UDB[n+3] Default Value: 0
23 : 20	PLD1_MC_2	Read Macrocell 1 for UDB[n+2] Default Value: 0
19 : 16	PLD0_MC_2	Read Macrocell 0 for UDB[n+2] Default Value: 0
15 : 12	PLD1_MC_1	Read Macrocell 1 for UDB[n+1] Default Value: 0
11 : 8	PLD0_MC_1	Read Macrocell 0 for UDB[n+1] Default Value: 0
7 : 4	PLD1_MC_0	Read Macrocell 1 for UDB[n] Default Value: 0
3 : 0	PLD0_MC_0	Read Macrocell 0 for UDB[n] Default Value: 0

Revision History

Revision History

Document Title: PSoC 4100-BL/4200-BL Family PSoC(R) 4 BLE Registers Technical Reference Manual (TRM) Document Number: 001-92739				
Revision	**ECN#**	**Issue Date**	**Origin of Change**	**Description of Change**
**	4396118	06/19/2014	KRIS	Specification for new silicon.
*A	4604737	12/22/2014	KRIS	Updated register description as per production silicon.
*B	4683570	06/08/2015	UDYG	Updated UDB Array Bank Control (BCTL) Registers Updated System Resource Sub System Registers Updated SCB Registers Updated Supervisory Flash (128 KB) Registers Added Supervisory Flash (256 KB) Registers Updated Single UDB (UDBSNG) Registers
*C	5144090	02/19/2016	UDYG	Added BLE Sub System Version 2 Registers Added DMA Controller Registers Added DMA Descriptor Registers
*D	5760861	06/02/2017	SHEA	Updated logo and copyright information.
*E	5867894	08/30/2017	KRIS	Sunset review; no content updates