Automotive PSoC® 4: PSoC 4200M Family Datasheet

Programmable System-on-Chip (PSoC®)

General Description

PSoC® 4 is a scalable and reconfigurable platform architecture for a family of programmable embedded system controllers with an Arm® Cortex™-M0 CPU, while being AEC-Q100 compliant. It combines programmable and reconfigurable analog and digital blocks with flexible automatic routing. The PSoC 4200M product family, based on this platform architecture, is a combination of a microcontroller with digital programmable logic, programmable analog, programmable interconnect, high-performance analog-to-digital conversion, opamps with comparator mode, and standard communication and timing peripherals. The PSoC 4200M products will be fully compatible with members of the PSoC 4 platform for new applications and design needs. The programmable analog and digital subsystems allow flexibility and in-field tuning of the design.

Features

32-bit MCU Subsystem

- Automotive Electronics Council (AEC) AEC-Q100 qualified
- 48 MHz Arm Cortex-M0 CPU with single-cycle multiply
- Up to 128 kB of flash with Read Accelerator
- Up to 16 kB of SRAM
- DMA engine

Programmable Analog

- Four opamps that operate in Deep Sleep mode at very low current levels
- All opamps have reconfigurable high current pin-drive, high-bandwidth internal drive, ADC input buffering, and Comparator modes with flexible connectivity allowing input connections to any pin
- Four current DACs (IDACs) for general-purpose or capacitive sensing applications on any pin
- Two low-power comparators that operate in Deep Sleep mode
- 12-bit SAR ADC with 1-Msps conversion rate

Programmable Digital

- Four programmable logic blocks, each with 8 Macrocells and an 8-bit data path (called universal digital blocks or UDBs)
- Cypress-provided peripheral component library, user-defined state machines, and Verilog input

Low Power 1.71 to 5.5 V Operation

- 20-nA Stop Mode with GPIO pin wakeup
- Hibernate and Deep Sleep modes allow wakeup-time versus power trade-offs

Capacitive Sensing

- Cypress Capacitive Sigma-Delta (CSD) technique provides best-in-class SNR (>5:1) and water tolerance
- Cypress-supplied software component makes capacitive sensing design easy
- Automatic hardware tuning (SmartSense™)

Segment LCD Drive

- LCD drive supported on all pins (common or segment)
- Operates in Deep Sleep mode with 4 bits per pin memory

Serial Communication

- Four independent run-time reconfigurable serial communication blocks (SCBs) with reconfigurable I^2C, SPI, UART, or LIN Slave functionality
- Two independent CAN blocks for automotive networking

Timing and Pulse-Width Modulation

- Eight 16-bit timer/counter pulse-width modulator (TCPWM) blocks
- Center-aligned, Edge, and Pseudo-random modes
- Comparator-based triggering of Kill signals for motor drive and other high-reliability digital logic applications

Package Options

- 48-pin, 64-pin TQFP, and 56-QFN packages
- Up to 51 programmable GPIOs
- GPIO pins can be CapSense, LCD, analog, or digital
- Drive modes, strengths, and slew rates are programmable

Temperature Range

- Grade-A: –40 °C to +85 °C
- Grade-S: –40 °C to +105 °C

PSoC Creator Design Environment

- Integrated Development Environment (IDE) provides schematic design entry and build (with analog and digital automatic routing)
- Applications Programming Interface (API component) for all fixed-function and programmable peripherals

Industry-Standard Tool Compatibility

- After schematic entry, development can be done with ARM-based industry-standard development tools

More Information

Cypress provides a wealth of data at www.cypress.com to help you to select the right PSoC device for your design, and to help you to quickly and effectively integrate the device into your design. For a comprehensive list of resources, see the knowledge base article KBA86521, How to Design with PSoC 3, PSoC 4, and PSoC 5LP. Following is an abbreviated list for PSoC 4:

- Overview: PSoC Portfolio, PSoC Roadmap
- Product Selectors: PSoC 1, PSoC 3, PSoC 4, PSoC 5LP
  In addition, PSoC Creator includes a device selection tool.
- Application notes: Cypress offers a large number of PSoC application notes covering a broad range of topics, from basic to advanced level. Recommended application notes for getting started with PSoC 4 are:
  - AN79953: Getting Started With PSoC 4
  - AN88619: PSoC 4 Hardware Design Considerations
  - AN86439: Using PSoC 4 GPIO Pins
  - AN57821: Mixed Signal Circuit Board Layout
  - AN81623: Digital Design Best Practices
  - AN73854: Introduction To Bootloaders
  - AN89610: ARM Cortex Code Optimization
- Technical Reference Manual (TRM) is in two documents:
  - Architecture TRM details each PSoC 4 functional block.
  - Registers TRM describes each of the PSoC 4 registers.
- Development Kits:
  - CY8CKIT-042, PSoC 4 Pioneer Kit, is an easy-to-use and inexpensive development platform. This kit includes connectors for Arduino™ compatible shields and Digilent® Pmod™ daughter cards.
  - CY8CKIT-049 is a very low-cost prototyping platform. It is a low-cost alternative to sampling PSoC 4 devices.
  - CY8CKIT-001 is a common development platform for any one of the PSoC 1, PSoC 3, PSoC 4, or PSoC 5LP families of devices.

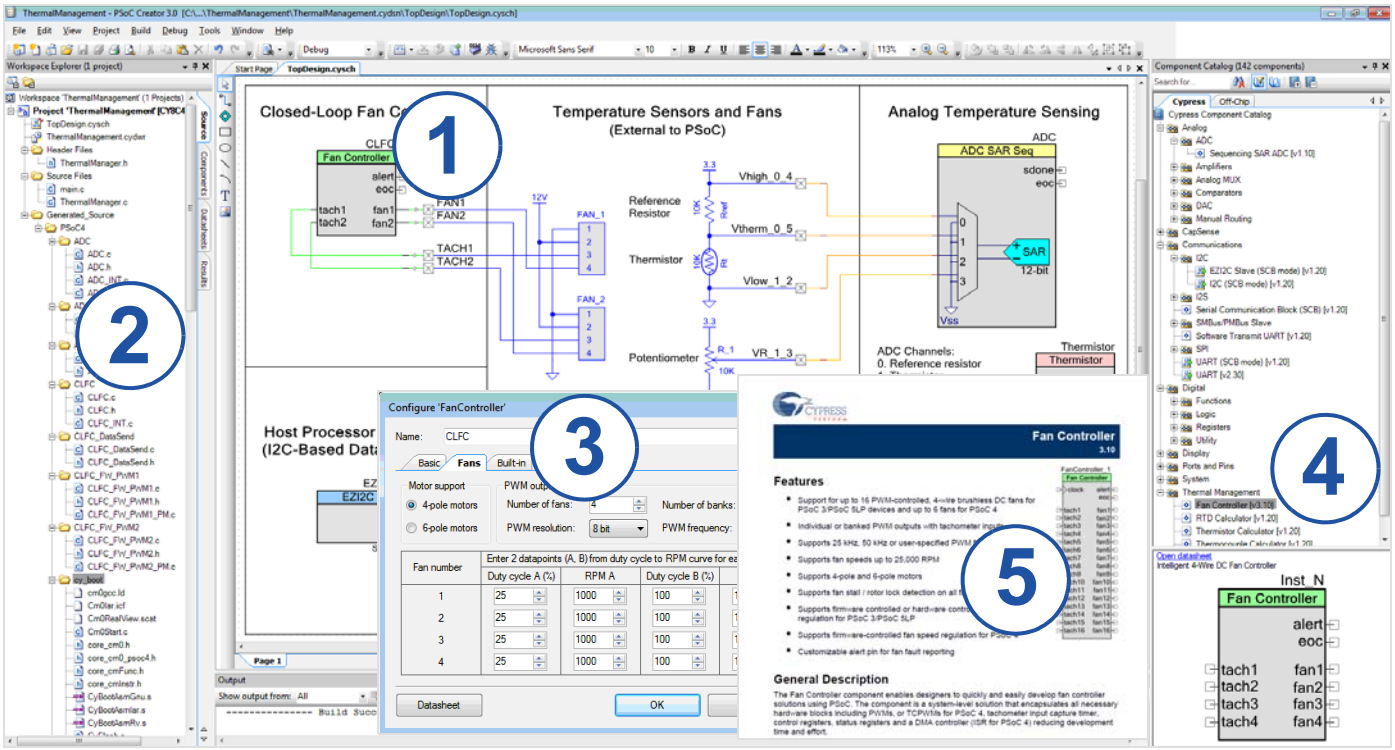
The MiniProg3 device provides an interface for flash programming and debug.

PSoC Creator

PSoC Creator is a free Windows-based Integrated Design Environment (IDE). It enables concurrent hardware and firmware design of PSoC 3, PSoC 4, and PSoC 5LP based systems. Create designs using classic, familiar schematic capture supported by over 100 pre-verified, production-ready PSoC Components; see the list of component datasheets. With PSoC Creator, you can:

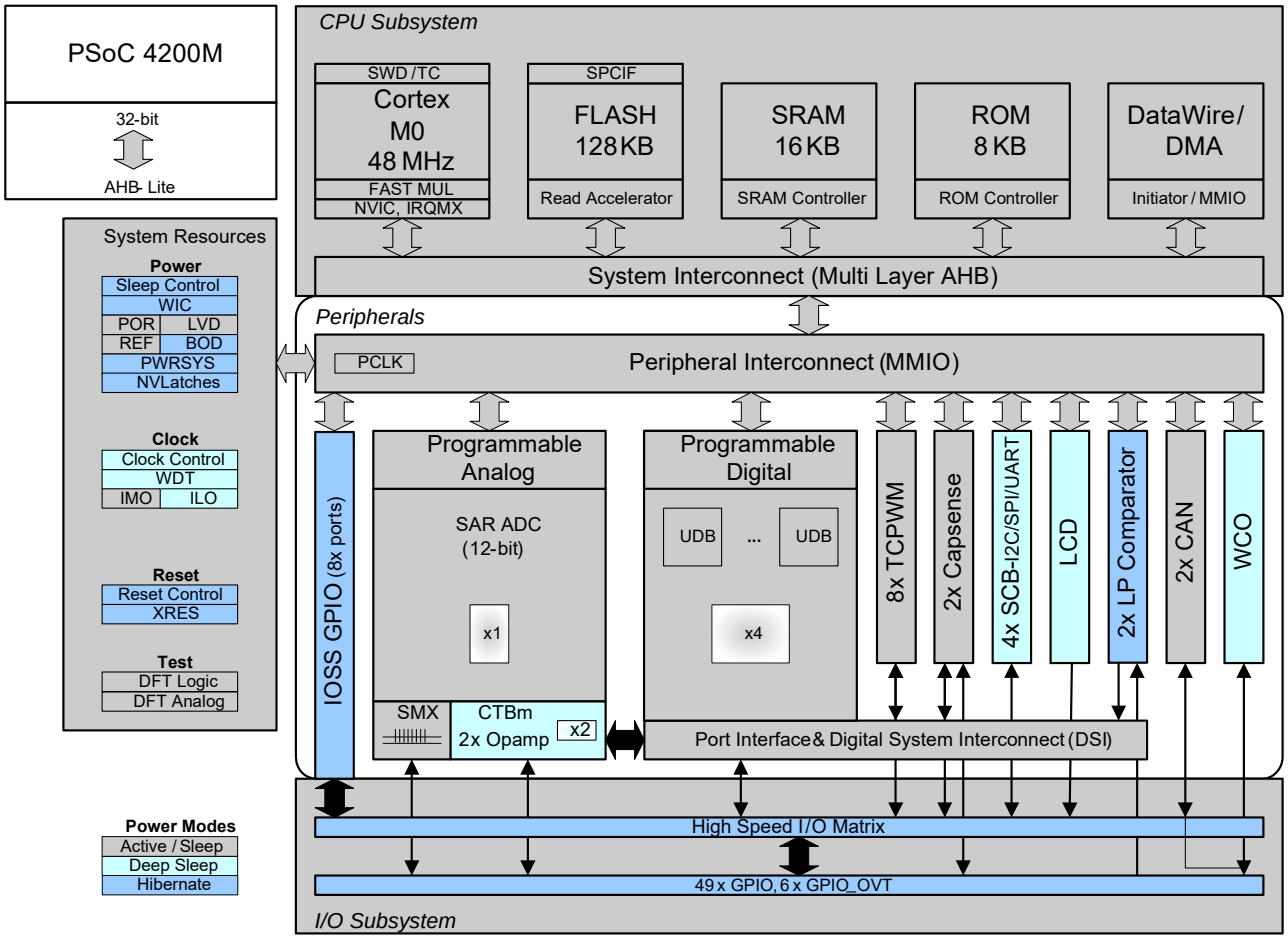
1. Drag and drop component icons to build your hardware system design in the main design workspace
2. Codesign your application firmware with the PSoC hardware, using the PSoC Creator IDE C compiler
3. Configure components using the configuration tools
4. Explore the library of 100+ components
5. Review component datasheets

Figure 1. Multiple-Sensor Example Project in PSoC Creator Contents



Contents

PSoC 4200M Block Diagram



The PSoC 4200-M devices include extensive support for programming, testing, debugging, and tracing both hardware and firmware.

The ARM Serial_Wire Debug (SWD) interface supports all programming and debug features of the device.

Complete debug-on-chip functionality enables full-device debugging in the final system using the standard production device. It does not require special interfaces, debugging pods, simulators, or emulators. Only the standard programming connections are required to fully support debug.

The PSoC Creator Integrated Development Environment (IDE) provides fully integrated programming and debug support for PSoC 4200-M devices. The SWD interface is fully compatible with industry-standard third-party tools. The PSoC 4200-M family provides a level of security not possible with multi-chip application solutions or with microcontrollers. This is due to its ability to disable debug features, robust flash protection, and because it allows customer-proprietary functionality to be implemented in on-chip programmable blocks.

The debug circuits are enabled by default and can only be disabled in firmware. If not enabled, the only way to re-enable them is to erase the entire device, clear flash protection, and reprogram the device with new firmware that enables debugging.

Additionally, all device interfaces can be permanently disabled (device security) for applications concerned about phishing attacks due to a maliciously reprogrammed device or attempts to defeat security by starting and interrupting flash programming sequences. Because all programming, debug, and test interfaces are disabled when maximum device security is enabled, PSoC 4200-M with device security enabled may not be returned for failure analysis. This is a trade-off the PSoC 4200-M allows the customer to make.

Functional Definition

CPU and Memory Subsystem

CPU

The Cortex-M0 CPU in the PSoC 4200-M is part of the 32-bit MCU subsystem, which is optimized for low-power operation with extensive clock gating. Most instructions are 16 bits in length and execute a subset of the Thumb-2 instruction set. The Cypress implementation includes a hardware multiplier that provides a 32-bit result in one cycle. It includes a nested vectored interrupt controller (NVIC) block with 32 interrupt inputs and also includes a Wakeup Interrupt Controller (WIC), which can wake the processor up from the Deep Sleep mode allowing power to be switched off to the main processor when the chip is in the Deep Sleep mode. The Cortex-M0 CPU provides a Non-Maskable Interrupt (NMI) input, which is made available to the user when it is not in use for system functions requested by the user.

The CPU also includes a debug interface, the serial wire debug (SWD) interface, which is a 2-wire form of JTAG; the debug configuration used for PSoC 4200-M has four break-point (address) comparators and two watchpoint (data) comparators.

Flash

The PSoC 4200-M has a flash module with a flash accelerator, tightly coupled to the CPU to improve average access times from the flash block. The flash accelerator delivers 85% of single-cycle SRAM access performance on average. Part of the flash module can be used to emulate EEPROM operation if required.

SRAM

SRAM memory is retained during Hibernate.

SROM

A supervisory ROM that contains boot and configuration routines is provided.

DMA

A DMA engine, with eight channels, is provided that can do 32-bit transfers and has chainable ping-pong descriptors.

System Resources

Power System

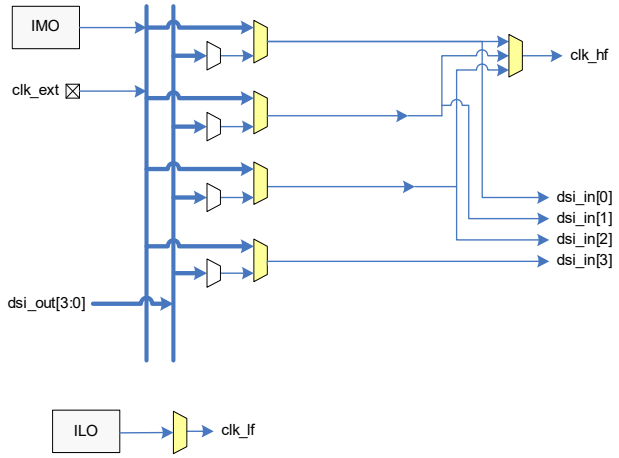
The power system is described in detail in the section Power on page 14. It provides assurance that voltage levels are as required for each respective mode and either delay mode entry (on power-on reset (POR), for example) until voltage levels are as required for proper function or generate resets (brown-out detect (BOD)) or interrupts (low voltage detect (LVD)). The PSoC 4200M operates with a single external supply over the range of 1.71 to 5.5 V and has five different power modes, transitions between which are managed by the power system. The PSoC 4200M provides Sleep, Deep Sleep, Hibernate, and Stop low-power modes.

Clock System

The PSoC 4200-M clock system is responsible for providing clocks to all subsystems that require clocks and for switching between different clock sources without glitching. In addition, the clock system ensures that no meta-stable conditions occur.

The clock system for the PSoC 4200-M consists of a Watch Crystal Oscillator (WCO) running at 32 kHz, the IMO (3 to 48 MHz) and the ILO (32-kHz nominal) internal oscillators, and provision for an external clock.

Figure 2. PSoC 4200M MCU Clocking Architecture



The clk_hf signal can be divided down to generate synchronous clocks for the UDBs, and the analog and digital peripherals. There are a total of 16 clock dividers for the PSoC 4200-M, each with 16-bit divide capability; this allows 12 to be used for the fixed-function blocks and four for the UDBs. The analog clock leads the digital clocks to allow analog events to occur before digital clock-related noise is generated. The 16-bit capability allows a lot of flexibility in generating fine-grained frequency values and is fully supported in PSoC Creator.

IMO Clock Source

The IMO is the primary source of internal clocking in the PSoC 4200M. It is trimmed during testing to achieve the specified accuracy. Trim values are stored in nonvolatile memory. Trimming can also be done on the fly to allow in-field calibration. The IMO default frequency is 24 MHz and it can be adjusted between 3 to 48 MHz in steps of 1 MHz. IMO tolerance with Cypress-provided calibration settings is ±2%.

ILO Clock Source

The ILO is a very low power oscillator, nominally 32 kHz, which is primarily used to generate clocks for peripheral operation in Deep Sleep mode. ILO-driven counters can be calibrated to the IMO to improve accuracy. Cypress provides a software component, which does the calibration.

Crystal Oscillator

The PSoC 4200M clock subsystem also includes a low-frequency crystal oscillator (32-kHz WCO) that is available during the Deep Sleep mode and can be used for Real-Time Clock (RTC) and Watchdog Timer applications.

Watchdog Timer

A watchdog timer is implemented in the clock block running from the low-frequency clock; this allows watchdog operation during Deep Sleep and generates a watchdog reset or an interrupt if not serviced before the timeout occurs. The watchdog reset is recorded in the Reset Cause register.

Reset

The PSoC 4200M can be reset from a variety of sources including a software reset. Reset events are asynchronous and guarantee reversion to a known state. The reset cause is recorded in a register, which is sticky through reset and allows software to determine the cause of the reset. An XRES pin is reserved for external reset to avoid complications with configuration and multiple pin functions during power-on or reconfiguration.

Voltage Reference

The PSoC 4200M reference system generates all internally required references. A 1% voltage reference spec is provided for the 12-bit ADC. To allow better signal-to-noise ratios (SNR) and better absolute accuracy, it is possible to add an external bypass capacitor to the internal reference using a GPIO pin or to use an external reference for the SAR.

Analog Blocks

12-bit SAR ADC

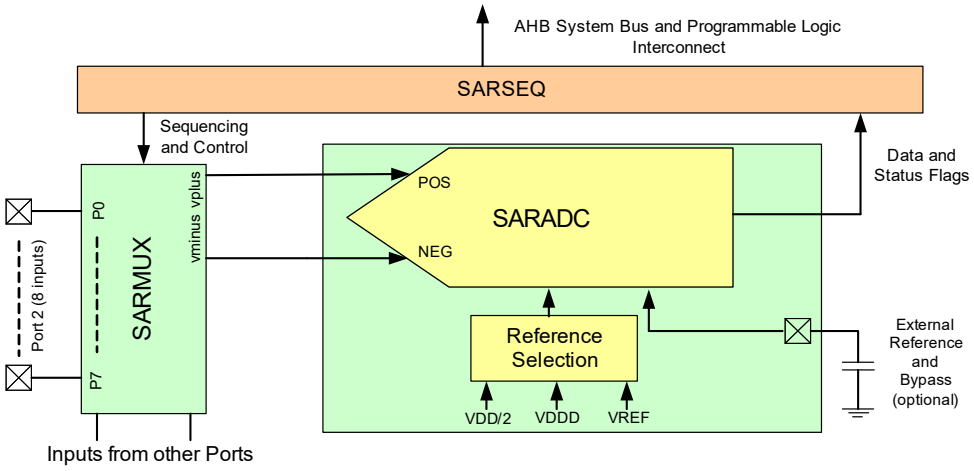
The 12-bit 1 MSample/second SAR ADC can operate at a maximum clock rate of 18 MHz and requires a minimum of 18 clocks at that frequency to do a 12-bit conversion.

The block functionality is augmented for the user by adding a reference buffer to it (trimmable to ±1%) and by providing the choice of three internal voltage references: V_{DD}, $V_{DD}/2$, and V_{REF} (nominally 1.024 V) as well as an external reference through a GPIO pin. The Sample-and-Hold (S/H) aperture is programmable allowing the gain bandwidth requirements of the amplifier driving the SAR inputs, which determine its settling time, to be relaxed if required. The system performance will be 65 dB for true 12-bit precision if appropriate references are used and system noise levels permit. To improve performance in noisy conditions, it is possible to provide an external bypass (through a fixed pin location) for the internal reference amplifier.

The SAR is connected to a fixed set of pins through an 8-input sequencer (expandable to 16 inputs). The sequencer cycles through selected channels autonomously (sequencer scan) and does so with zero switching overhead (that is, the aggregate sampling bandwidth is equal to 1 Msps, whether it is for a single channel or distributed over several channels). The sequencer switching is effected through a state machine or through firmware-driven switching. A feature provided by the sequencer is buffering of each channel to reduce CPU interrupt service requirements. To accommodate signals with varying source impedance and frequency, it is possible to have different sample times programmable for each channel. In addition, the signal range specification through a pair of range registers (low and high range values) is implemented with a corresponding out-of-range interrupt if the digitized value exceeds the programmed range; this allows fast detection of out-of-range values without the necessity of having to wait for a sequencer scan to be completed and the CPU to read the values and check for out-of-range values in software.

The SAR is able to digitize the output of the on-board temperature sensor for calibration and other temperature-dependent functions. The SAR is not available in Deep Sleep and Hibernate modes as it requires a high-speed clock (up to 18 MHz). The SAR operating range is 1.71 to 5.5 V.

Figure 3. SAR ADC System Diagram



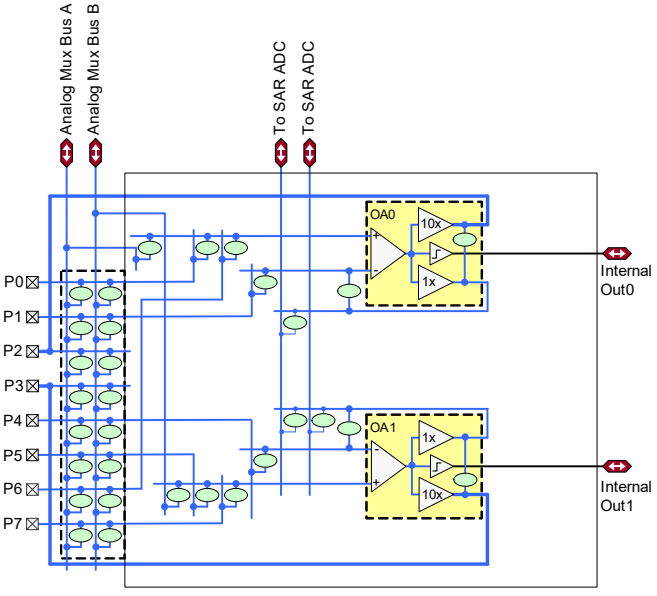
Analog Multiplex Bus

The PSoC 4200M has two concentric analog buses (Analog Mux Bus A and Analog Mux Bus B) that circumnavigate the periphery of the chip. These buses can transport analog signals from any pin to various analog blocks (including the opamps) and to the CapSense blocks allowing, for instance, the ADC to monitor any pin on the chip. These buses are independent and can also be split into three independent sections. This allows one section to be used for CapSense purposes, one for general analog signal processing, and the third for general-purpose digital peripherals and GPIO.

Four Opamps

The PSoC 4200M has four opamps with comparator modes, which allow most common analog functions to be performed on-chip eliminating external components; PGAs, voltage buffers, filters, trans-impedance amplifiers, and other functions can be realized with external passives saving power, cost, and space. The on-chip opamps are designed with enough bandwidth to drive the Sample-and-Hold circuit of the ADC without requiring external buffering. The opamps can operate in the Deep Sleep mode at very low power levels. The following diagram shows one of two identical opamp pairs of the opamp subsystem.

Figure 4. Identical Opamp Pairs in Opamp Subsystem



The ovals in Figure 4 represent analog switches, which may be controlled via user firmware, the SAR sequencer, or user-defined programmable logic. The opamps (OA0 and OA1) are configurable via these switches to perform all standard opamp functions with appropriate feedback components.

The opamps (OA0 and OA1) are programmable and reconfigurable to provide standard opamp functionality via switchable feedback components, unity gain functionality for driving pins directly, or for internal use (such as buffering SAR ADC inputs as indicated in the diagram), or as true comparators.

The opamp inputs provide highly flexible connectivity and can connect directly to dedicated pins or, via the analog mux buses, to any pin on the chip. Analog switch connectivity is controllable by user firmware as well as user-defined programmable digital state machines (implemented via UDBs).

The opamps operate in Deep Sleep mode at very low currents allowing analog circuits to remain operational during Deep Sleep.

Temperature Sensor

The PSoC 4200M has one on-chip temperature sensor. This consists of a diode, which is biased by a current source that can be disabled to save power. The temperature sensor is connected to the ADC, which digitizes the reading and produces a temperature value using Cypress-supplied software that includes calibration and linearization.

Low-power Comparators

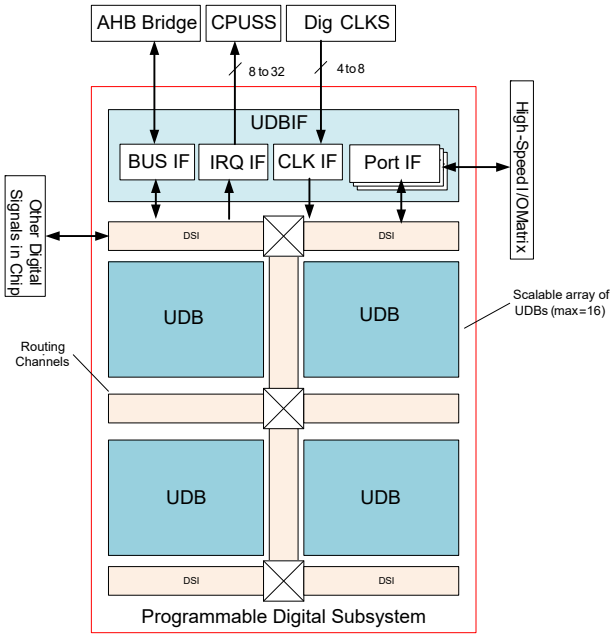
The PSoC 4200M has a pair of low-power comparators, which can also operate in the Deep Sleep and Hibernate modes. This allows the analog system blocks to be disabled while retaining the ability to monitor external voltage levels during low-power modes. The comparator outputs are normally synchronized to avoid meta-stability unless operating in an asynchronous power mode (Hibernate) where the system wake-up circuit is activated by a comparator switch event.

Programmable Digital

Universal Digital Blocks (UDBs) and Port Interfaces

The PSoC 4200M has four UDBs; the UDB array also provides a switched Digital System Interconnect (DSI) fabric that allows signals from peripherals and ports to be routed to and through the UDBs for communication and control. The UDB array is shown in the following figure.

Figure 5. UDB Array

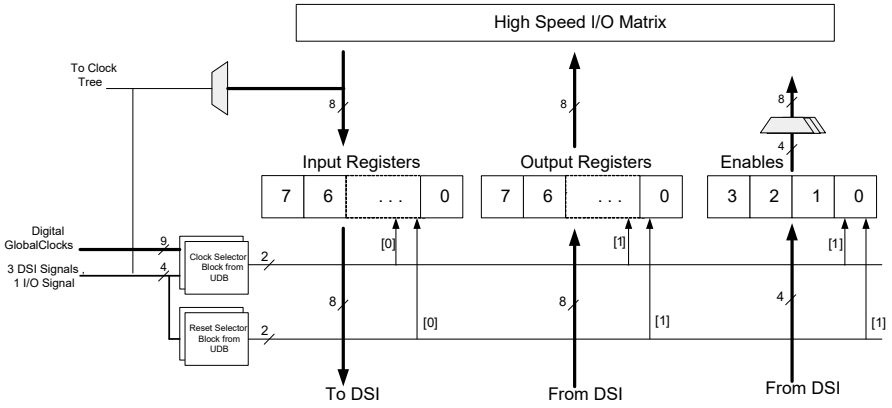


UDBs can be clocked from a clock divider block, from a port interface (required for peripherals such as SPI), and from the DSI network directly or after synchronization.

A port interface is defined, which acts as a register that can be clocked with the same source as the PLDs inside the UDB array. This allows faster operation because the inputs and outputs can be registered at the port interface close to the I/O pins and at the edge of the array. The port interface registers can be clocked by one of the I/Os from the same port. This allows interfaces such as SPI to operate at higher clock speeds by eliminating the delay for the port input to be routed over DSI and used to register other inputs. The port interface is shown in Figure 6.

The UDBs can generate interrupts (one UDB at a time) to the interrupt controller. The UDBs can connect to any pin on Ports 0, 1, 2, and 3 (each port interconnect requires one UDB) through the DSI.

Figure 6. Port Interface



Fixed Function Digital

Timer/Counter/PWM (TCPWM) Block

The TCPWM block uses a16-bit counter with user-programmable period length. There is a Capture register to record the count value at the time of an event (which may be an I/O event), a period register which is used to either stop or auto-reload the counter when its count is equal to the period register, and compare registers to generate compare value signals, which are used as PWM duty cycle outputs. The block also provides true and complementary outputs with programmable offset between them to allow use as deadband programmable complementary PWM outputs. It also has a Kill input to force outputs to a predetermined state; for example, this is used in motor drive systems when an overcurrent state is indicated and the PWMs driving the FETs need to be shut off immediately with no time for software intervention. The PSoC 4200M has eight TCPWM blocks.

Serial Communication Blocks (SCB)

The PSoC 4200M has four SCBs, which can each implement an I^2C, UART, or SPI interface.

I^2C Mode: The hardware I^2C block implements a full multi-master and slave interface (it is capable of multimaster arbitration). This block is capable of operating at speeds of up to 1 Mbps (Fast Mode Plus) and has flexible buffering options to reduce interrupt overhead and latency for the CPU. It also supports EzI^2C that creates a mailbox address range in the memory of the PSoC 4200M and effectively reduces I^2C communication to reading from and writing to an array in memory. In addition, the block supports an 8-deep FIFO for receive and transmit which, by increasing the time given for the CPU to read data, greatly reduces the need for clock stretching caused by the CPU not having read data on time. The FIFO mode is available in all channels and is very useful in the absence of DMA.

The I^2C peripheral is compatible with the I^2C Standard-mode, Fast-mode, and Fast-mode Plus devices as defined in the NXP I^2C-bus specification and user manual (UM10204). The I^2C bus I/O is implemented with GPIO in open-drain modes.

UART Mode: This is a full-feature UART operating at up to 1 Mbps. It supports automotive single-wire interface (LIN), infrared interface (IrDA), and SmartCard (ISO7816) protocols, all of which are minor variants of the basic UART protocol. In addition, it supports the 9-bit multiprocessor mode that allows addressing of peripherals connected over common RX and TX lines. Common UART functions such as parity error, break detect, and frame error are supported. An 8-deep FIFO allows much greater CPU service latencies to be tolerated.

SPI Mode: The SPI mode supports full Motorola SPI, TI SSP (essentially adds a start pulse used to synchronize SPI Codecs), and National Microwire (half-duplex form of SPI). The SPI block can use the FIFO and also supports an EzSPI mode in which data interchange is reduced to reading and writing an array in memory.

LIN Slave Mode: The LIN Slave mode uses the SCB hardware block and implements a full LIN slave interface. This LIN slave is compliant with LIN v1.3 and LIN v2.1/2.2 specification standards. It is certified by C&S GmbH based on the standard protocol and data link layer conformance tests. LIN slave can be operated at baud rates of up to ~20 Kbps with a maximum of 40-meter cable length. PSoC Creator software supports up to two LIN slave interfaces in the PSoC 4 device, providing built-in application programming interfaces (APIs) based on the LIN specification standard.

CAN Blocks

There are two independent CAN blocks which implement CAN 2.0B as defined in the Bosch specifications and conform to ISO-11898-1 standard.

GPIO

The PSoC 4200M has 51 GPIOs in the 64-pin TQFP (0.5-mm pitch) package. The GPIO block implements the following:

- Eight drive strength modes including strong push-pull, resistive pull-up and pull-down, weak (resistive) pull-up and pull-down, open drain and open source, input only, and disabled
- Input threshold select (CMOS or LVTTL)
- Individual control of input and output disables
- Hold mode for latching previous state (used for retaining I/O state in Deep Sleep mode and Hibernate modes)
- Selectable slew rates for dV/dt related noise control to improve EMI

The pins are organized in logical entities called ports, which are 8-bit in width. During power-on and reset, the blocks are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix is used to multiplex between various signals that may connect to an I/O pin. Pin locations for fixed-function peripherals are also fixed to reduce internal multiplexing complexity (these signals do not go through the DSI network). DSI signals are not affected by this and any pin on Ports 0, 1, 2, and 3 may be routed to any UDB through the DSI network. Only pins on Ports 0, 1, 2, and 3 may be routed through DSI signals.

Data output and pin state registers store, respectively, the values to be driven on the pins and the states of the pins themselves.

Every I/O pin can generate an interrupt if so enabled and each I/O port has an interrupt request (IRQ) and interrupt service routine (ISR) vector associated with it (8 for PSoC 4200M).

The Pins of Port 6 (up to 6 depending on the package) are overvoltage tolerant (V_{IN} can exceed V_{DD}). The overvoltage cells will not sink more than 10 µA when their inputs exceed V_{DDIO} in compliance with I^2C specifications.

Special Function Peripherals

LCD Segment Drive

The PSoC 4200M has an LCD controller, which can drive up to four commons and up to 47 segments. Any pin can be either a common or a segment pin. It uses full digital methods to drive the LCD segments requiring no generation of internal LCD voltages.

The two methods used are referred to as digital correlation and PWM.

Digital correlation pertains to modulating the frequency and levels of the common and segment signals to generate the highest RMS voltage across a segment to light it up or to keep the RMS signal zero. This method is good for STN displays but may result in reduced contrast with TN (cheaper) displays.

PWM pertains to driving the panel with PWM signals to effectively use the capacitance of the panel to provide the integration of the modulated pulse-width to generate the desired LCD voltage. This method results in higher power consumption but can result in better results when driving TN displays. LCD operation is supported during Deep Sleep refreshing a small display buffer (4 bits; 1 32-bit register per port).

CapSense

CapSense is supported on all pins in the PSoC 4200M through a CapSense Sigma-Delta (CSD) block that can be connected to any pin through an analog mux bus that any GPIO pin can be connected to via an Analog switch. CapSense functionality can thus be provided on any pin or group of pins in a system under software control. A component is provided for the CapSense block, which provides automatic hardware tuning (Cypress SmartSense™), to make it easy for the user.

Shield voltage can be driven on another Mux Bus to provide water tolerance capability. Water tolerance is provided by driving the shield electrode in phase with the sense electrode to keep the shield capacitance from attenuating the sensed input.

Each CSD block has two IDACs which can be used for general purposes if CapSense is not being used.(both IDACs are available in that case) or if CapSense is used without water tolerance (one IDAC is available). The PSoC 4200M has two CSD blocks which can be used independently; one for CapSense and one providing two IDACs.

The two CapSense blocks are referred to as CSD0 and CSD1. Capacitance sensing inputs on Ports 0, 1, 2, 3, 4, 6, and 7 are sensed by CSD0. Capacitance sensing inputs on Port 5 are sensed by CSD1.

Pinouts

Table 1 provides the pin list for the PSoC 4200M. This table provides the power supply and port pins (for example, P0.0 is Pin 0 of Port 0).

Table 1. Pinouts for Different Packages

64-TQFP		48-TQFP		56-QFN	
Pin	**Name**	**Pin**	**Name**	**Pin**	**Name**
39	P0.0	28	P0.0	31	P0.0
40	P0.1	29	P0.1	32	P0.1
41	P0.2	30	P0.2	33	P0.2
42	P0.3	31	P0.3	34	P0.3
43	P0.4	32	P0.4	35	P0.4
44	P0.5	33	P0.5	36	P0.5
45	P0.6	34	P0.6	37	P0.6
46	P0.7	35	P0.7	38	P0.7
47	XRES	36	XRES	39	XRES
48	VCCD	37	VCCD	40	VCCD
49	VSSD	38	VSSD	41	VSSD
50	VDDD	39	VDDD	42	VDDD
51	P5.0	–	–	43	P5.0
52	P5.1	–	–	44	P5.1
53	P5.2	–	–	45	P5.2
54	P5.3	–	–	46	P5.3
				47	P5.4
55	P5.5	–	–	48	P5.5
56	VDDA	40	VDDA	49	VDDA
57	VSSA	41	VSSA	50	VSSA
58	P1.0	42	P1.0	–	–
59	P1.1	43	P1.1	51	P1.1
60	P1.2	44	P1.2	52	P1.2
61	P1.3	45	P1.3	53	P1.3
62	P1.4	46	P1.4	54	P1.4
63	P1.5	47	P1.5	55	P1.5
64	P1.6	48	P1.6	56	P1.6
1	P1.7/VREF	1	P1.7/VREF	1	P1.7/VREF
2	P2.0	2	P2.0	2	P2.0
3	P2.1	3	P2.1	3	P2.1
4	P2.2	4	P2.2	4	P2.2
5	P2.3	5	P2.3	5	P2.3
6	P2.4	6	P2.4	6	P2.4
7	P2.5	7	P2.5	7	P2.5
8	P2.6	8	P2.6	8	P2.6
9	P2.7	9	P2.7	9	P2.7
10	VSSA	10	VSSIO	10	VSSA
11	VDDA	–	–	11	VDDA

Table 1. Pinouts for Different Packages *(continued)*

64-TQFP		48-TQFP		56-QFN	
Pin	**Name**	**Pin**	**Name**	**Pin**	**Name**
12	P6.0	–	–	–	–
13	P6.1			12	P6.1
14	P6.2	–	–	13	P6.2
15	P6.4	–	–	–	–
16	P6.5	–	–	–	–
17	VSSIO	–	–	14	VSSIO
18	P3.0	12	P3.0	15	P3.0
19	P3.1	13	P3.1	16	P3.1
20	P3.2	14	P3.2	17	P3.2
21	P3.3	16	P3.3	18	P3.3
22	P3.4	17	P3.4	19	P3.4
23	P3.5	18	P3.5	20	P3.5
24	P3.6	19	P3.6	21	P3.6
25	P3.7	20	P3.7	–	–
26	VDDIO	21	VDDIO	22	VDDIO
27	P4.0	22	P4.0	23	P4.0
28	P4.1	23	P4.1	24	P4.1
29	P4.2	24	P4.2	25	P4.2
30	P4.3	25	P4.3	26	P4.3
31	P4.4	–	–	–	–
32	P4.5	–	–	27	P4.5
33	P4.6	–	–	–	–
–	–	–	–	28	P4.7
37	P7.0	26	P7.0	29	P7.0
38	P7.1	27	P7.1	–	–
–	–	–	–	30	P7.2

The pins of Port 6 are overvoltage-tolerant. Pins 34, 35, and 36 are No-Connects on the 64-pin TQFP. Pins 11 and 15 are No-connects in the 48-pin TQFP. All VSS pins must be tied together.

The output drivers of I/O Ports P0 and P7 are connected to VDDD. Output drivers of I/O Ports 1, 2, and 5 are connected to VDDA. Output drivers of I/O Ports 3, 4, and 6 are connected to VDDIO.

Each of the pins shown in Table 1 can have multiple programmable functions as shown in Table 2. Column headings refer to Analog and Alternate pin functions.

Table 2. Alternate Functions Supported by Each Pin

Port/Pin	Analog	Alt. Function 1	Alt. Function 2	Alt. Function 3	Alt. Function 4	Alt. Function 5
P0.0	lpcomp.in_p[0]	–	–	can[1].can_rx:0	–	scb[0].spi_select1:0
P0.1	lpcomp.in_n[0]	–	–	can[1].can_tx:0	–	scb[0].spi_select2:0
P0.2	lpcomp.in_p[1]	–	–	–	–	scb[0].spi_select3:0
P0.3	lpcomp.in_n[1]	–	–	–	–	–
P0.4	wco_in	–	scb[1].uart_rx:0	–	scb[1].i2c_scl:0	scb[1].spi_mosi:1
P0.5	wco_out	–	scb[1].uart_tx:0	–	scb[1].i2c_sda:0	scb[1].spi_miso:1
P0.6	–	ext_clk:0	scb[1].uart_cts:0	–	–	scb[1].spi_clk:1
P0.7	–	–	scb[1].uart_rts:0	can[1].can_tx_enb_n:0	wakeup	scb[1].spi_select0:1
P5.0	ctb1.oa0.inp	tcpwm.line[4]:2	scb[2].uart_rx:0	–	scb[2].i2c_scl:0	scb[2].spi_mosi:0
P5.1	ctb1.oa0.inm	tcpwm.line_compl[4]:2	scb[2].uart_tx:0	–	scb[2].i2c_sda:0	scb[2].spi_miso:0
P5.2	ctb1.oa0.out	tcpwm.line[5]:2	scb[2].uart_cts:0	–	lpcomp.comp[0]:1	scb[2].spi_clk:0
P5.3	ctb1.oa1.out	tcpwm.line_compl[5]:2	scb[2].uart_rts:0	–	lpcomp.comp[1]:1	scb[2].spi_select0:0
P5.4	ctb1.oa1.inm	tcpwm.line[6]:2	–	–	–	scb[2].spi_select1:0
P5.5	ctb1.oa1.inp	tcpwm.line_compl[6]:2	–	–	–	scb[2].spi_select2:0
P5.6	ctb1.oa0.inp_alt	tcpwm.line[7]:0	–	–	–	scb[2].spi_select3:0
P5.7	ctb1.oa1.inp_alt	tcpwm.line_compl[7]:0	–	–	–	–
P1.0	ctb0.oa0.inp	tcpwm.line[2]:1	scb[0].uart_rx:1	–	scb[0].i2c_scl:0	scb[0].spi_mosi:1
P1.1	ctb0.oa0.inm	tcpwm.line_compl[2]:1	scb[0].uart_tx:1	–	scb[0].i2c_sda:0	scb[0].spi_miso:1
P1.2	ctb0.oa0.out	tcpwm.line[3]:1	scb[0].uart_cts:1	–	–	scb[0].spi_clk:1
P1.3	ctb0.oa1.out	tcpwm.line_compl[3]:1	scb[0].uart_rts:1	–	–	scb[0].spi_select0:1
P1.4	ctb0.oa1.inm	tcpwm.line[6]:1	–	–	–	scb[0].spi_select1:1
P1.5	ctb0.oa1.inp	tcpwm.line_compl[6]:1	–	–	–	scb[0].spi_select2:1
P1.6	ctb0.oa0.inp_alt	tcpwm.line[7]:1	–	–	–	scb[0].spi_select3:1
P1.7	ctb0.oa1.inp_alt	tcpwm.line_compl[7]:1	–	–	–	
P2.0	sarmux.0	tcpwm.line[4]:1	–	–	scb[1].i2c_scl:1	scb[1].spi_mosi:2
P2.1	sarmux.1	tcpwm.line_compl[4]:1	–	–	scb[1].i2c_sda:1	scb[1].spi_miso:2
P2.2	sarmux.2	tcpwm.line[5]:1	–	–	–	scb[1].spi_clk:2
P2.3	sarmux.3	tcpwm.line_compl[5]:1	–	–	–	scb[1].spi_select0:2
P2.4	sarmux.4	tcpwm.line[0]:1	–	–	–	scb[1].spi_select1:1
P2.5	sarmux.5	tcpwm.line_compl[0]:1	–	–	–	scb[1].spi_select2:1
P2.6	sarmux.6	tcpwm.line[1]:1	–	–	–	scb[1].spi_select3:1
P2.7	sarmux.7	tcpwm.line_compl[1]:1	–	–	–	scb[3].spi_select0:1

Table 2. Alternate Functions Supported by Each Pin *(continued)*

Port/Pin	Analog	Alt. Function 1	Alt. Function 2	Alt. Function 3	Alt. Function 4	Alt. Function 5
P6.0	—	tcpwm.line[4]:0	scb[3].uart_rx:0	can[0].can_tx_enb_n:0	scb[3].i2c_scl:0	scb[3].spi_mosi:0
P6.1	—	tcpwm.line_compl[4]:0	scb[3].uart_tx:0	can[0].can_rx:0	scb[3].i2c_sda:0	scb[3].spi_miso:0
P6.2	—	tcpwm.line[5]:0	scb[3].uart_cts:0	can[0].can_tx:0	—	scb[3].spi_clk:0
P6.3	—	tcpwm.line_compl[5]:0	scb[3].uart_rts:0	—	—	scb[3].spi_select0:0
P6.4	—	tcpwm.line[6]:0	—	—	—	scb[3].spi_select1:0
P6.5	—	tcpwm.line_compl[6]:0	—	—	—	scb[3].spi_select2:0
P3.0	—	tcpwm.line[0]:0	scb[1].uart_rx:1	—	scb[1].i2c_scl:2	scb[1].spi_mosi:0
P3.1	—	tcpwm.line_compl[0]:0	scb[1].uart_tx:1	—	scb[1].i2c_sda:2	scb[1].spi_miso:0
P3.2	—	tcpwm.line[1]:0	scb[1].uart_cts:1	—	swd_data	scb[1].spi_clk:0
P3.3	—	tcpwm.line_compl[1]:0	scb[1].uart_rts:1	—	swd_clk	scb[1].spi_select0:0
P3.4	—	tcpwm.line[2]:0	—	—	—	scb[1].spi_select1:0
P3.5	—	tcpwm.line_compl[2]:0	—	—	—	scb[1].spi_select2:0
P3.6	—	tcpwm.line[3]:0	—	—	—	scb[1].spi_select3:0
P3.7	—	tcpwm.line_compl[3]:0	—	—	—	
P4.0	—	—	scb[0].uart_rx:0	can[0].can_rx:1	scb[0].i2c_scl:1	scb[0].spi_mosi:0
P4.1	—	—	scb[0].uart_tx:0	can[0].can_tx:1	scb[0].i2c_sda:1	scb[0].spi_miso:0
P4.2	csd[0].c_mod	—	scb[0].uart_cts:0	can[0].can_tx_enb_n:1	lpcomp.comp[0]:0	scb[0].spi_clk:0
P4.3	csd[0].c_sh_tank	—	scb[0].uart_rts:0	—	lpcomp.comp[1]:0	scb[0].spi_select0:0
P4.4	—	—	—	can[1].can_tx_enb_n:1	—	scb[0].spi_select1:2
P4.5	—	—	—	can[1].can_rx:1	—	scb[0].spi_select2:2
P4.6	—	—	—	can[1].can_tx:1	—	scb[0].spi_select3:2
P4.7	—	—	—	—	—	
P7.0	—	tcpwm.line[0]:2	scb[3].uart_rx:1	—	scb[3].i2c_scl:1	scb[3].spi_mosi:1
P7.1	—	tcpwm.line_compl[0]:2	scb[3].uart_tx:1	—	scb[3].i2c_sda:1	scb[3].spi_miso:1
P7.2	—	tcpwm.line[1]:2	scb[3].uart_cts:1	—		scb[3].spi_clk:1

Descriptions of the power pin functions are as follows:

VDDD: Power supply for both analog and digital sections (where there is no V_{DDA} pin).

VDDA: Analog V_{DD} pin where package pins allow; shorted to V_{DDD} otherwise.

VDDIO: I/O pin power domain.

VSSA: Analog ground pin where package pins allow; shorted to VSS otherwise

VSS: Ground pin.

VCCD: Regulated Digital supply (1.8 V ±5%).

Port Pins can all be used as LCD Commons, LCD Segment drivers, or CSD sense and shield pins can be connected to AMUXBUS A or B or can all be used as GPIO pins that can be driven by firmware or DSI signals.

Power

The supply voltage range is 1.71 to 5.5 V with all functions and circuits operating over that range.

The PSoC 4200M family allows two distinct modes of power supply operation: Unregulated External Supply and Regulated External Supply modes.

Unregulated External Supply

In this mode, the PSoC 4200M is powered by an External Power Supply that can be anywhere in the range of 1.8 to 5.5 V. This range is also designed for battery-powered operation, for instance, the chip can be powered from a battery system that starts at 3.5V and works down to 1.8 V. In this mode, the internal regulator of the PSoC 4200M supplies the internal logic and the VCCD output of the PSoC 4200M must be bypassed to ground via an external Capacitor (in the range of 1 to 1.6 µF; X5R ceramic or better).

The grounds, VSSA and VSS, must be shorted together. Bypass capacitors must be used from VDDD and VDDA to ground, typical practice for systems in this frequency range is to use a capacitor in the 1 µF range in parallel with a smaller capacitor (0.1 µF, for example). Note that these are simply rules of thumb and that, for critical applications, the PCB layout, lead inductance, and the Bypass capacitor parasitic should be simulated to design and obtain optimal bypassing.

Table 3. Recommended Bypass Capacitors for Different Power Supply Pins

Power Supply	Bypass Capacitors
VDDD–VSS and VDDIO-VSS	0.1 µF ceramic at each pin plus bulk capacitor 1 to 10 µF.
VDDA–VSSA	0.1 µF ceramic at pin. Additional 1 µF to 10 µF bulk capacitor.
VCCD–VSS	1 µF ceramic capacitor at the VCCD pin.
VREF–VSSA (optional)	The internal bandgap may be bypassed with a 1 µF to 10 µF capacitor for better ADC performance.

Regulated External Supply

In this mode, the PSoC 4200M is powered by an external power supply that must be within the range of 1.71 to 1.89 V (1.8 ±5%); note that this range needs to include power supply ripple. VCCD and VDDD pins are shorted together and bypassed. The internal regulator is disabled in firmware.

Development Support

The PSoC 4200M family has a rich set of documentation, development tools, and online resources to assist you during your development process. Visit www.cypress.com/psoc4 for more information.

Documentation

A suite of documentation supports the PSoC 4200M family to ensure that you can find answers to your questions quickly. This section contains a list of some of the key documents.

Software User Guide: A step-by-step guide for using PSoC Creator. The software user guide shows you how the PSoC Creator build process works in detail, how to use source control with PSoC Creator, and much more.

Component Datasheets: The flexibility of PSoC allows the creation of new peripherals (components) long after the device has gone into production. Component data sheets provide all of the information needed to select and use a particular component, including a functional description, API documentation, example code, and AC/DC specifications.

Application Notes: PSoC application notes discuss a particular application of PSoC in depth; examples include brushless DC motor control and on-chip filtering. Application notes often include example projects in addition to the application note document.

Technical Reference Manual: The Technical Reference Manual (TRM) contains all the technical detail you need to use a PSoC device, including a complete description of all PSoC registers.

Online

In addition to print documentation, the Cypress PSoC forums connect you with fellow PSoC users and experts in PSoC from around the world, 24 hours a day, 7 days a week.

Tools

With industry standard cores, programming, and debugging interfaces, the PSoC 4200M family is part of a development tool ecosystem. Visit us at www.cypress.com/psoccreator for the latest information on the revolutionary, easy to use PSoC Creator IDE, supported third party compilers, programmers, debuggers, and development kits.

Electrical Specifications

Absolute Maximum Ratings

Table 4. Absolute Maximum Ratings[1]

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID1	V_{DD_ABS}	Analog or digital supply relative to V_{SS} ($V_{SSD} = V_{SSA}$)	–0.5	–	6	V	Absolute maximum
SID2	V_{CCD_ABS}	Direct digital core voltage input relative to V_{SSD}	–0.5	–	1.95	V	Absolute maximum
SID3	V_{GPIO_ABS}	GPIO voltage; V_{DDD} or V_{DDA}	–0.5	–	V_{DD}+0.5	V	Absolute maximum
SID4	I_{GPIO_ABS}	Current per GPIO	–25	–	25	mA	Absolute maximum
SID5	$I_{G\text{-}PIO\_injection}$	GPIO injection current per pin	–0.5	–	0.5	mA	Absolute maximum
BID44	ESD_HBM	Electrostatic discharge human body model	2200	–	–	V	–
BID45	ESD_CDM	Electrostatic discharge charged device model	500	–	–	V	–
BID46	LU	Pin current for latch-up	–140	–	140	mA	–

Device Level Specifications

All specifications are valid for –40 °C ≤ T_A ≤ 85 °C for Grade-A devices and –40 °C ≤ T_A ≤ 105 °C for Grade-S devices. Specifications are valid for 1.71 V to 5.5 V, except where noted.

Table 5. DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID53	V_{DDD}	Power supply input voltage ($V_{DDA} = V_{DDD} = V_{DD}$)	1.8	–	5.5	V	With regulator enabled
SID255	V_{DDD}	Power supply input voltage unregulated	1.71	1.8	1.89	V	Internally unregulated Supply
SID54	V_{CCD}	Output voltage (for core logic)	–	1.8	–	V	–
SID55	C_{EFC}	External regulator voltage bypass	1	1.3	1.6	µF	X5R ceramic or better
SID56	C_{EXC}	Power supply decoupling capacitor	–	1	–	µF	X5R ceramic or better
Active Mode, –40 °C to 105 °C							
SID6	I_{DD1}	Execute from flash; CPU at 6 MHz	–	2.2	2.8	mA	–
SID7	I_{DD2}	Execute from flash; CPU at 12 MHz	–	3.7	4.2	mA	–
SID8	I_{DD3}	Execute from flash; CPU at 24 MHz	–	6.7	7.2	mA	–
SID9	I_{DD4}	Execute from flash; CPU at 48 MHz	–	13	13.8	mA	–
Sleep Mode, –40 °C to +105 °C							
SID21	I_{DD16}	I^2C wakeup, WDT, and comparators on. Regulator off.	–	1.75	2.1	mA	V_{DD} = 1.71 to 1.89, 6 MHz
SID22	I_{DD17}	I^2C wakeup, WDT, and comparators on.	–	1.7	2.1	mA	V_{DD} = 1.8 to 5.5, 6 MHz
SID23	I_{DD18}	I^2C wakeup, WDT, and comparators on. Regulator off.	–	2.35	2.8	mA	V_{DD} = 1.71 to 1.89, 12 MHz

Note
1. Usage above the absolute maximum conditions listed in Table 4 may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods of time may affect device reliability. The maximum storage temperature is 150 °C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When used below absolute maximum conditions but above normal operating conditions, the device may not operate to specification.

Table 5. DC Specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID24	I_{DD19}	I^2C wakeup, WDT, and comparators on.	–	2.25	2.8	mA	V_{DD} = 1.8 to 5.5, 12 MHz
Deep Sleep Mode, –40 °C to + 60 °C							
SID30	I_{DD25}	I^2C wakeup and WDT on. Regulator off.	–	1.55	20	µA	V_{DD} = 1.71 to 1.89
SID31	I_{DD26}	I^2C wakeup and WDT on.	–	1.35	15	µA	V_{DD} = 1.8 to 3.6
SID32	I_{DD27}	I^2C wakeup and WDT on.	–	1.5	15	µA	V_{DD} = 3.6 to 5.5
Deep Sleep Mode, +85 °C							
SID33	I_{DD28}	I^2C wakeup and WDT on. Regulator off.	–	–	60	µA	V_{DD} = 1.71 to 1.89
SID34	I_{DD29}	I^2C wakeup and WDT on.	–	–	45	µA	V_{DD} = 1.8 to 3.6
SID35	I_{DD30}	I^2C wakeup and WDT on.	–	–	30	µA	V_{DD} = 3.6 to 5.5
Deep Sleep Mode, +105 °C							
SID33S	I_{DD28S}	I^2C wakeup and WDT on. Regulator Off.	–	–	135	µA	V_{DD} = 1.71 to 1.89
SID34S	I_{DD29S}	I^2C wakeup and WDT on.	–	–	180	µA	V_{DD} = 1.8 to 3.6
SID35S	I_{DD30S}	I^2C wakeup and WDT on.	–	–	140	µA	V_{DD} = 3.6 to 5.5
Hibernate Mode, –40 °C to + 60 °C							
SID39	I_{DD34}	Regulator off	–	150	3000	nA	V_{DD} = 1.71 to 1.89
SID40	I_{DD35}	–	–	150	1000	nA	V_{DD} = 1.8 to 3.6
SID41	I_{DD36}	–	–	150	1100	nA	V_{DD} = 3.6 to 5.5
Hibernate Mode, +85 °C							
SID42	I_{DD37}	Regulator off	–	–	4500	nA	V_{DD} = 1.71 to 1.89
SID43	I_{DD38}	–	–	–	3500	nA	V_{DD} = 1.8 to 3.6
SID44	I_{DD39}	–	–	–	3500	nA	V_{DD} = 3.6 to 5.5
Hibernate Mode, +105 °C							
SID42S	I_{DD37S}	Regulator Off.	–	–	25	µA	V_{DD} = 1.71 to 1.89
SID43S	I_{DD38S}		–	–	25	µA	V_{DD} = 1.8 to 3.6
SID44S	I_{DD39S}		–	–	25	µA	V_{DD} = 3.6 to 5.5
Stop Mode							
SID304	I_{DD43A}	Stop Mode current; V_{DD} = 3.6 V	–	35	85	nA	T = –40 °C to +60 °C
			–	–	1450	nA	T = +85 °C
SID304A	I_{DD43B}	Stop Mode current; V_{DD} = 3.6 V	–	–	5645	nA	T = +85 °C to +105 °C
SID304B	I_{DD43C}	Stop Mode current; V_{DD} = 5.0 V	–	–	5645	nA	T = +85 °C to +105 °C
XRES Current							
SID307	I_{DD_XR}	Supply current while XRES (Active Low) asserted	–	2	5	mA	–

Table 6. AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID48	F_{CPU}	CPU frequency	DC	–	48	MHz	$1.71 \le V_{DD} \le 5.5$
SID49	T_{SLEEP}	Wakeup from sleep mode	–	0	–	µs	Guaranteed by characterization
SID50	$T_{DEEPSLEEP}$	Wakeup from Deep Sleep mode	–	–	25	µs	24 MHz IMO. Guaranteed by characterization.
SID51	$T_{HIBERNATE}$	Wakeup from Hibernate mode	–	–	0.7	ms	Guaranteed by characterization
SID51A	T_{STOP}	Wakeup from Stop mode	–	–	2	ms	Guaranteed by characterization
SID52	$T_{RESETWIDTH}$	External reset pulse width	1	–	–	µs	Guaranteed by characterization

GPIO

Table 7. GPIO DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID57	V_{IH}[2]	Input voltage high threshold	$0.7 \times V_{DDD}$	–	–	V	CMOS Input
SID57A	IIHS	Input current when Pad > V_{DDIO} for OVT inputs	–	–	10	µA	Per I^2C Spec
SID58	V_{IL}	Input voltage low threshold	–	–	$0.3 \times V_{DDD}$	V	CMOS Input
SID241	V_{IH}[2]	LVTTL input, V_{DDD} < 2.7 V	$0.7 \times V_{DDD}$	–	–	V	–
SID242	V_{IL}	LVTTL input, V_{DDD} < 2.7 V	–	–	$0.3 \times V_{DDD}$	V	–
SID243	V_{IH}[2]	LVTTL input, $V_{DDD} \ge 2.7$ V	2.0	–	–	V	–
SID244	V_{IL}	LVTTL input, $V_{DDD} \ge 2.7$ V	–	–	0.8	V	–
SID59	V_{OH}	Output voltage high level	$V_{DDD} - 0.6$	–	–	V	I_{OH} = 4 mA at 3 V V_{DDD}
SID60	V_{OH}	Output voltage high level	$V_{DDD} - 0.5$	–	–	V	I_{OH} = 1 mA at 1.8 V $_{DDD}$
SID61	V_{OL}	Output voltage low level	–	–	0.6	V	I_{OL} = 4 mA at 1.8 V V_{DDD}
SID62	V_{OL}	Output voltage low level	–	–	0.6	V	I_{OL} = 8 mA at 3 V V_{DDD}
SID62A	V_{OL}	Output voltage low level	–	–	0.4	V	I_{OL} = 3 mA at 3 V V_{DDD}
SID63	R_{PULLUP}	Pull-up resistor	3.5	5.6	8.5	kΩ	–
SID64	$R_{PULLDOWN}$	Pull-down resistor	3.5	5.6	8.5	kΩ	–
SID65	I_{IL}	Input leakage current (absolute value)	–	–	2	nA	25 °C, V_{DDD} = 3.0 V. Guaranteed by Characterization.
SID65A	I_{IL_CTBM}	Input leakage current (absolute value) for CTBM pins	–	–	4	nA	Guaranteed by Characterization
SID66	C_{IN}	Input capacitance	–	–	7	pF	–
SID67	V_{HYSTTL}	Input hysteresis LVTTL	25	40	–	mV	$V_{DDD} \ge 2.7$ V
SID68	$V_{HYSCMOS}$	Input hysteresis CMOS	$0.05 \times V_{DDD}$	–	–	mV	–
SID69	I_{DIODE}	Current through protection diode to V_{DD}/Vss	–	–	100	µA	Guaranteed by characterization
SID69A	I_{TOT_GPIO}	Maximum Total Source or Sink Chip Current	–	–	200	mA	Guaranteed by characterization

Note
2. V_{IH} must not exceed V_{DDD} + 0.2 V.

Table 8. GPIO AC Specifications

(Guaranteed by Characterization)[3]

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID70	T_{RISEF}	Rise time in fast strong mode	2	–	12	ns	3.3 V V_{DDD}, Cload = 25 pF
SID71	T_{FALLF}	Fall time in fast strong mode	2	–	12	ns	3.3 V V_{DDD}, Cload = 25 pF
SID72	T_{RISES}	Rise time in slow strong mode	10	–	60	ns	3.3 V V_{DDD}, Cload = 25 pF
SID73	T_{FALLS}	Fall time in slow strong mode	10	–	60	ns	3.3 V V_{DDD}, Cload = 25 pF
SID74	$F_{GPIOUT1}$	GPIO Fout; 3.3 V ≤ V_{DDD} ≤ 5.5 V. Fast strong mode.	–	–	33	MHz	90/10%, 25 pF load, 60/40 duty cycle
SID75	$F_{GPIOUT2}$	GPIO Fout; 1.7 V ≤ V_{DDD} ≤ 3.3 V. Fast strong mode.	–	–	16.7	MHz	90/10%, 25 pF load, 60/40 duty cycle
SID76	$F_{GPIOUT3}$	GPIO Fout; 3.3 V ≤ V_{DDD} ≤ 5.5 V. Slow strong mode.	–	–	7	MHz	90/10%, 25 pF load, 60/40 duty cycle
SID245	$F_{GPIOUT4}$	GPIO Fout; 1.7 V ≤ V_{DDD} ≤ 3.3 V. Slow strong mode.	–	–	3.5	MHz	90/10%, 25 pF load, 60/40 duty cycle
SID246	F_{GPIOIN}	GPIO input operating frequency; 1.71 V ≤ V_{DDD} ≤ 5.5 V	–	–	48	MHz	90/10% V_{IO}

XRES

Table 9. XRES DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ Conditions
SID77	V_{IH}	Input voltage high threshold	0.7 × V_{DDD}	–	–	V	CMOS Input
SID78	V_{IL}	Input voltage low threshold	–	–	0.3 × V_{DDD}	V	CMOS Input
SID79	R_{PULLUP}	Pull-up resistor	3.5	5.6	8.5	kΩ	–
SID80	C_{IN}	Input capacitance	–	3	–	pF	–
SID81	$V_{HYSXRES}$	Input voltage hysteresis	–	100	–	mV	Guaranteed by characterization
SID82	I_{DIODE}	Current through protection diode to V_{DDD}/V_{SS}	–	–	100	µA	Guaranteed by characterization

Table 10. XRES AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID83	$T_{RESEWIDTH}$	Reset pulse width	1	–	–	µs	Guaranteed by characterization

Note

3. Simultaneous switching transitions on many fully-loaded GPIO pins may cause ground perturbations depending on several factors including PCB and decoupling capacitor design. For applications that are very sensitive to ground perturbations, the slower GPIO slew rate setting may be used.

Analog Peripherals

Opamp

Table 11. Opamp Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID269	I_{DD_HI}	Power = high	–	1100	1850	µA	Opamp block current, no load.
SID270	I_{DD_MED}	Power = medium	–	550	950	µA	
SID271	I_{DD_LOW}	Power = low	–	150	350	µA	
SID272	GBW_HI	Power = high	6	–	–	MHz	Load = 20 pF, 0.1 mA. V_{DDA} = 2.7 V
SID273	GBW_MED	Power = medium	4	–	–	MHz	
SID274	GBW_LO	Power = low	–	1	–	MHz	
SID275	$I_{OUT\_MAX\_HI}$	Power = high	10	–	–	mA	$V_{DDA} \geq 2.7$ V, 500 mV from rail
SID276	$I_{OUT\_MAX\_MID}$	Power = medium	10	–	–	mA	
SID277	$I_{OUT\_MAX\_LO}$	Power = low	–	5	–	mA	
SID278	$I_{OUT\_MAX\_HI}$	Power = high	4	–	–	mA	V_{DDA} = 1.71 V, 500 mV from rail
SID279	$I_{OUT\_MAX\_MID}$	Power = medium	4	–	–	mA	
SID280	$I_{OUT\_MAX\_LO}$	Power = low	–	2	–	mA	
SID281	V_{IN}	Input voltage range	–0.05	–	VDDA – 0.2	V	Charge-pump on, $V_{DDA} \geq 2.7$ V
SID282	V_{CM}	Input common mode voltage	–0.05	–	VDDA – 0.2	V	Charge-pump on, $V_{DDA} \geq 2.7$ V
SID283	V_{OUT_1}	Power = high, Iload=10 mA	0.5	–	VDDA – 0.5	V	$V_{DDA} \geq 2.7$ V
SID284	V_{OUT_2}	Power = high, Iload=1 mA	0.2	–	VDDA – 0.2	V	
SID285	V_{OUT_3}	Power = medium, Iload=1 mA	0.2	–	VDDA – 0.2	V	
SID286	V_{OUT_4}	Power = low, Iload=0.1mA	0.2	–	VDDA – 0.2	V	
SID288	V_{OS_TR}	Offset voltage, trimmed	1	±0.5	1	mV	High mode
SID288A	V_{OS_TR}	Offset voltage, trimmed	–	±1	–	mV	Medium mode
SID288B	V_{OS_TR}	Offset voltage, trimmed	–	±2	–	mV	Low mode
SID290	$V_{OS\_DR\_TR}$	Offset voltage drift, trimmed	–10	±3	10	µV/C	High mode
SID290A	$V_{OS\_DR\_TR}$	Offset voltage drift, trimmed	–	±10	–	µV/C	Medium mode
SID290B	$V_{OS\_DR\_TR}$	Offset voltage drift, trimmed	–	±10	–	µV/C	Low mode
SID291	CMRR	DC Common mode rejection ratio. High-power mode. Common Model voltage range from 0.5 V to VDDA - 0.5 V.	60	70	–	dB	V_{DDD} = 3.6 V
SID292	PSRR	At 1 kHz, 100 mV ripple	70	85	–	dB	V_{DDD} = 3.6 V
SID293	V_{N1}	Input referred noise, 1 Hz - 1GHz, power = high	–	94	–	µVrms	–
SID294	V_{N2}	Input referred noise, 1 kHz, power = high	–	72	–	nV/rtHz	–
SID295	V_{N3}	Input referred noise, 10 kHz, power = high	–	28	–	nV/rtHz	–
SID296	V_{N4}	Input referred noise, 100 kHz, power = high	–	15	–	nV/rtHz	–
SID297	Cload	Stable up to maximum load. Performance specs at 50 pF.	–	–	125	pF	–

Table 11. Opamp Specifications *(continued)*

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID298	Slew_rate	Cload = 50 pF, Power = High, $V_{DDA} \geq 2.7$ V	6	–	–	V/µsec	–
SID299	T_op_wake	From disable to enable, no external RC dominating	–	25	–	µsec	–
SID300	T_{PD1}	Response time; power = high	–	150	–	nsec	Comparator mode; 50 mV drive, Trise = Tfall (approx.)
SID301	T_{PD2}	Response time; power = medium	–	400	–	nsec	
SID302	T_{PD3}	Response time; power = low	–	2000	–	nsec	
SID303	Vhyst_op	Hysteresis	–	10	–	mV	
Deep Sleep Mode: Mode 2 is lowest current range. Mode 1 has higher GBW. Deep Sleep mode. $V_{DDA} \geq 2.7$ V.							
SID_DS_1	IDD_HI_M1	Mode 1, High current	–	1400	–	µA	25 °C
SID_DS_2	IDD_MED_M1	Mode 1, Medium current	–	700	–	µA	25 °C
SID_DS_3	IDD_LOW_M1	Mode 1, Low current	–	200	–	µA	25 °C
SID_DS_4	IDD_HI_M2	Mode 2, High current	–	120	–	µA	25 °C
SID_DS_5	IDD_MED_M2	Mode 2, Medium current	–	60	–	µA	25 °C
SID_DS_6	IDD_LOW_M2	Mode 2, Low current	–	15	–	µA	25 °C
SID_DS_7	GBW_HI_M1	Mode 1, High current	–	4	–	MHz	25 °C
SID_DS_8	GBW_MED_M1	Mode 1, Medium current	–	2	–	MHz	25 °C
SID_DS_9	GBW_LOW_M1	Mode 1, Low current	–	0.5	–	MHz	25 °C
SID_DS_10	GBW_HI_M2	Mode 2, High current	–	0.5	–	MHz	20-pF load, no DC load 0.2 V to V_{DDA}-1.5 V
SID_DS_11	GBW_MED_M2	Mode 2, Medium current	–	0.2	–	MHz	20-pF load, no DC load 0.2 V to V_{DDA}-1.5 V
SID_DS_12	GBW_LOW_M2	Mode 2, Low current	–	0.1	–	MHz	20-pF load, no DC load 0.2 V to V_{DDA}-1.5 V
SID_DS_13	VOS_HI_M1	Mode 1, High current	–	5	–	mV	With trim 25 °C, 0.2 V to V_{DDA}-1.5 V
SID_DS_14	VOS_MED_M1	Mode 1, Medium current	–	5	–	mV	With trim 25 °C, 0.2 V to V_{DDA}-1.5 V
SID_DS_15	VOS_LOW_M1	Mode 1, Low current	–	5	–	mV	With trim 25 °C, 0.2 V to V_{DDA}-1.5 V
SID_DS_16	VOS_HI_M2	Mode 2, High current	–	5	–	mV	With trim 25 °C, 0.2 V to V_{DDA}-1.5 V
SID_DS_17	VOS_MED_M2	Mode 2, Medium current	–	5	–	mV	With trim 25 °C, 0.2 V to V_{DDA}-1.5 V
SID_DS_18	VOS_LOW_M2	Mode 2, Low current	–	5	–	mV	With trim 25 °C, 0.2 V to V_{DDA}-1.5 V
SID_DS_19	IOUT_HI_M1	Mode 1, High current	–	10	–	mA	Output is 0.5 V to V_{DDA}-0.5 V
SID_DS_20	IOUT_MED_M1	Mode 1, Medium current	–	10	–	mA	Output is 0.5 V to V_{DDA}-0.5 V
SID_DS_21	IOUT_LOW_M1	Mode 1, Low current	–	4	–	mA	Output is 0.5 V to V_{DDA}-0.5 V
SID_DS_22	IOUT_HI_M2	Mode 2, High current	–	1	–	mA	Output is 0.5 V to V_{DDA}-0.5 V

Table 11. Opamp Specifications *(continued)*

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID_DS_23	IOUT_MED_M2	Mode 2, Medium current	–	1	–	mA	Output is 0.5 V to V_{DDA}-0.5 V
SID_DS_24	IOUT_LOW_M2	Mode 2, Low current	–	0.5	–	mA	Output is 0.5 V to V_{DDA}-0.5 V

Comparator

Table 12. Comparator DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID85	$V_{OFFSET2}$	Input offset voltage, Common Mode voltage range from 0 to V_{DD}-1	–	–	±4	mV	–
SID85A	$V_{OFFSET3}$	Input offset voltage. Ultra low-power mode (V_{DDD} ≥ 2.2 V for Temp < 0 °C, V_{DDD} ≥ 1.8 V for Temp > 0 °C)	–	±12	–	mV	–
SID86	V_{HYST}	Hysteresis when enabled, Common Mode voltage range from 0 to V_{DD} -1.	–	10	35	mV	Guaranteed by characterization
SID87	V_{ICM1}	Input common mode voltage in normal mode	0	–	V_{DDD} – 0.1	V	Modes 1 and 2.
SID247	V_{ICM2}	Input common mode voltage in low power mode (V_{DDD} ≥ 2.2 V for Temp < 0 °C, V_{DDD} ≥ 1.8 V for Temp > 0 °C)	0	–	V_{DDD}	V	–
SID247A	V_{ICM3}	Input common mode voltage in ultra low power mode	0	–	V_{DDD} – 1.15	V	–
SID88	CMRR	Common mode rejection ratio	50	–	–	dB	V_{DDD} ≥ 2.7 V. Guaranteed by characterization
SID88A	CMRR	Common mode rejection ratio	42	–	–	dB	V_{DDD} < 2.7 V. Guaranteed by characterization
SID89	I_{CMP1}	Block current, normal mode	–	–	400	µA	Guaranteed by characterization
SID248	I_{CMP2}	Block current, low power mode	–	–	100	µA	Guaranteed by characterization
SID259	I_{CMP3}	Block current, ultra low power mode (V_{DDD} ≥ 2.2 V for Temp < 0 °C, V_{DDD} ≥ 1.8 V for Temp > 0 °C)	–	6	28	µA	Guaranteed by characterization
SID90	Z_{CMP}	DC input impedance of comparator	35	–	–	MΩ	Guaranteed by characterization

Table 13. Comparator AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID91	T_{RESP1}	Response time, normal mode	–	–	110	ns	50-mV overdrive
SID258	T_{RESP2}	Response time, low power mode	–	–	200	ns	50-mV overdrive
SID92	T_{RESP3}	Response time, ultra low power mode ($V_{DDD} \geq 2.2$ V for Temp < 0 °C, $V_{DDD} \geq 1.8$ V for Temp > 0 °C)	–	–	15	µs	200-mV overdrive

Temperature Sensor

Table 14. Temperature Sensor Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID93	$T_{SENSACC}$	Temperature sensor accuracy	–5	±1	+5	°C	–40 to +105 °C

SAR ADC

Table 15. SAR ADC DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID94	A_RES	Resolution	–	–	12	bits	–
SID95	A_CHNIS_S	Number of channels - single ended	–	–	16	–	8 full speed
SID96	A-CHNKS_D	Number of channels - differential	–	–	8	–	Diff inputs use neighboring I/O
SID97	A-MONO	Monotonicity	–	–	–	–	Yes. Based on characterization.
SID98	A_GAINERR	Gain error	–	–	±0.1	%	With external reference
SID99	A_OFFSET	Input offset voltage	–	–	2	mV	Measured with 1-V V_{REF}.
SID100	A_ISAR	Current consumption	–	–	1	mA	–
SID101	A_VINS	Input voltage range - single ended	V_{SS}	–	V_{DDA}	V	Based on device characterization
SID102	A_VIND	Input voltage range - differential	V_{SS}	–	V_{DDA}	V	Based on device characterization
SID103	A_INRES	Input resistance	–	–	2.2	KΩ	Based on device characterization
SID104	A_INCAP	Input capacitance	–	–	10	pF	Based on device characterization

Table 16. SAR ADC AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID106	A_PSRR	Power supply rejection ratio	70	–	–	dB	–
SID107	A_CMRR	Common mode rejection ratio	66	–	–	dB	Measured at 1 V
SID108	A_SAMP_1	Sample rate with external reference bypass cap	–	–	1	Msps	–
SID108A	A_SAMP_2	Sample rate with no bypass cap. Reference = V_{DD}	–	–	1	Msps	–
SID108B	A_SAMP_3	Sample rate with no bypass cap. Internal reference	–	–	100	Ksps	–
SID109	A_SNDR	Signal-to-noise and distortion ratio (SINAD)	66	–	–	dB	F_{IN} = 10 kHz
SID111	A_INL[4]	Integral non linearity	–1.4	–	+1.4	LSB	V_{DD} = 1.71 to 5.5, 1 Msps, Vref = 1 to 5.5
SID111A	A_INL	Integral non linearity	–1.4	–	+1.4	LSB	V_{DDD} = 1.71 to 3.6, 1 Msps, Vref = 1.71 to V_{DDD}
SID111B	A_INL	Integral non linearity	–1.4	–	+1.4	LSB	V_{DDD} = 1.71 to 5.5, 500 Ksps, Vref = 1 to 5.5
SID112	A_DNL[4]	Differential non linearity	–0.9	–	+1.35	LSB	V_{DDD} = 1.71 to 5.5, 1 Msps, Vref = 1 to 5.5
SID112A	A_DNL	Differential non linearity	–0.9	–	+1.35	LSB	V_{DDD} = 1.71 to 3.6, 1 Msps, Vref = 1.71 to V_{DDD}
SID112B	A_DNL	Differential non linearity	–0.9	–	+1.35	LSB	V_{DDD} = 1.71 to 5.5, 500 Ksps, Vref = 1 to 5.5
SID113	A_THD	Total harmonic distortion	–	–	–65	dB	F_{IN} = 10 kHz

CSD

Table 17. CSD Block Specification

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
CSD Specification							
SID308	VCSD	Voltage range of operation	1.71	–	5.5	V	–
SID309	IDAC1	DNL for 8-bit resolution	–1	–	1	LSB	–
SID310	IDAC1	INL for 8-bit resolution	–3	–	3	LSB	–
SID311	IDAC2	DNL for 7-bit resolution	–1	–	1	LSB	–
SID312	IDAC2	INL for 7-bit resolution	–3	–	3	LSB	–
SID313	SNR	Ratio of counts of finger to noise. Guaranteed by characterization.	5	–	–	Ratio	Capacitance range of 9 to 35 pF, 0.1 pF sensitivity
SID314	IDAC1_CRT1	Output current of Idac1 (8-bits) in High range	–	612	–	µA	–
SID314A	IDAC1_CRT2	Output current of Idac1(8-bits) in Low range	–	306	–	µA	–
SID315	IDAC2_CRT1	Output current of Idac2 (7-bits) in High range	–	304.8	–	µA	–
SID315A	IDAC2_CRT2	Output current of Idac2 (7-bits) in Low range	–	152.4	–	µA	–

Note
4. Refer to http://www.cypress.com/knowledge-base-article/definitions-inl-and-dnl-adc for INL and DNL explanation.

Digital Peripherals

The following specifications apply to the Timer/Counter/PWM peripheral in timer mode.

Timer/Counter/PWM

Table 18. TCPWM Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID.TCPWM.1	ITCPWM1	Block current consumption at 3 MHz	–	–	45	µA	All modes (Timer/Counter/PWM)
SID.TCPWM.2	ITCPWM2	Block current consumption at 12 MHz	–	–	155	µA	All modes (Timer/Counter/PWM)
SID.TCPWM.2A	ITCPWM3	Block current consumption at 48 MHz	–	–	650	µA	All modes (Timer/Counter/PWM)
SID.TCPWM.3	TCPWMFREQ	Operating frequency	–	–	Fc	MHz	Fc max = Fcpu. Maximum = 24 MHz
SID.TCPWM.4	TPWMENEXT	Input Trigger Pulse Width for all Trigger Events	2/Fc	–	–	ns	Trigger Events can be Stop, Start, Reload, Count, Capture, or Kill depending on which mode of operation is selected.
SID.TCPWM.5	TPWMEXT	Output Trigger Pulse widths	2/Fc	–	–	ns	Minimum possible width of Overflow, Underflow, and CC (Counter equals Compare value) trigger outputs
SID.TCPWM.5A	TCRES	Resolution of Counter	1/Fc	–	–	ns	Minimum time between successive counts
SID.TCPWM.5B	PWMRES	PWM Resolution	1/Fc	–	–	ns	Minimum pulse width of PWM Output
SID.TCPWM.5C	QRES	Quadrature inputs resolution	1/Fc	–	–	ns	Minimum pulse width between Quadrature phase inputs.

I^2C

Table 19. Fixed I^2C DC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID149	I_{I2C1}	Block current consumption at 100 kHz	–	–	50	µA	–
SID150	I_{I2C2}	Block current consumption at 400 kHz	–	–	135	µA	–
SID151	I_{I2C3}	Block current consumption at 1 Mbps	–	–	310	µA	–
SID152	I_{I2C4}	I^2C enabled in Deep Sleep mode	–	–	1.4	µA	–

Table 20. Fixed I^2C AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID153	F_{I2C1}	Bit rate	–	–	1	Mbps	–

LCD Direct Drive

Table 21. LCD Direct Drive DC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID154	I_{LCDLOW}	Operating current in low power mode	–	5	–	µA	16 × 4 small segment disp. at 50 Hz
SID155	C_{LCDCAP}	LCD capacitance per segment/common driver	–	500	5000	pF	Guaranteed by Design
SID156	LCD_{OFFSET}	Long-term segment offset	–	20	–	mV	–
SID157	I_{LCDOP1}	PWM Mode current. 5-V bias. 24-MHz IMO	–	0.6	–	mA	32 × 4 segments. 50 Hz, 25 °C
SID158	I_{LCDOP2}	PWM Mode current. 3.3-V bias. 24-MHz IMO.	–	0.5	–	mA	32 × 4 segments. 50 Hz, 25 °C

Table 22. LCD Direct Drive AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID159	F_{LCD}	LCD frame rate	10	50	150	Hz	–

Table 23. Fixed UART DC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID160	I_{UART1}	Block current consumption at 100 Kbits/sec	–	–	55	µA	–
SID161	I_{UART2}	Block current consumption at 1000 Kbits/sec	–	–	312	µA	–

Table 24. Fixed UART AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID162	F_{UART}	Bit rate	–	–	1	Mbps	–

SPI Specifications

Table 25. Fixed SPI DC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID163	I_{SPI1}	Block current consumption at 1 Mbits/sec	–	–	360	µA	–
SID164	I_{SPI2}	Block current consumption at 4 Mbits/sec	–	–	560	µA	–
SID165	I_{SPI3}	Block current consumption at 8 Mbits/sec	–	–	600	µA	–

Table 26. Fixed SPI AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID166	F_{SPI}	SPI operating frequency (master; 6X oversampling)	–	–	8	MHz	–

Table 27. Fixed SPI Master mode AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Unit
SID167	T_{DMO}	MOSI valid after Sclock driving edge	–	–	15	ns
SID168	T_{DSI}	MISO valid before Sclock capturing edge. Full clock, late MISO Sampling used	20	–	–	ns
SID169	T_{HMO}	Previous MOSI data hold time with respect to capturing edge at Slave	0	–	–	ns

Table 28. Fixed SPI Slave mode AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Unit
SID170	T_{DMI}	MOSI valid before Sclock capturing edge	40	–	–	ns
SID171	T_{DSO}	MISO valid after Sclock driving edge	–	–	42 + 3 × (1/FCPU)	ns
SID171A	T_{DSO_ext}	MISO valid after Sclock driving edge in Ext. Clock mode	–	–	48	ns
SID172	T_{HSO}	Previous MISO data hold time	0	–	–	ns
SID172A	$T_{SSELSCK}$	SSEL Valid to first SCK Valid edge	100	–	–	ns

Memory

Table 29. Flash DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID173	V_{PE}	Erase and program voltage	1.71	–	5.5	V	–

Table 30. Flash AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID174	$T_{ROWWRITE}$	Row (block) write time (erase and program)	–	–	20	ms	Row (block) = 128 bytes
SID175	$T_{ROWERASE}$	Row erase time	–	–	13	ms	–
SID176	$T_{ROWPROGRAM}$	Row program time after erase	–	–	7	ms	–
SID178	$T_{BULKERASE}$	Bulk erase time (128 KB)	–	–	35	ms	–
SID179	$T_{SECTORERASE}$	Sector erase time (8 KB)	–	–	15	ms	–
SID180	$T_{DEVPROG}$	Total device program time	–	–	15	seconds	Guaranteed by characterization
SID181	F_{END}	Flash endurance	100 K	–	–	cycles	Guaranteed by characterization
SID182	F_{RET}	Flash retention. $T_A \le 55$ °C, 100 K P/E cycles.	20	–	–	years	Guaranteed by characterization
SID182A	F_{RET}[5]	Flash retention. $T_A \le 85$ °C, 10 K P/E cycles.	10	–	–	years	Guaranteed by characterization
SID182B	F_{RET}[5]	Flash retention. $T_A \le 105$ °C, 10 K P/E cycles, ≤ three years at $T_A \ge 85$ °C	10	20	–	years	Guaranteed by characterization

Note

5. Cypress provides a retention calculator to calculate the retention lifetime based on customers' individual temperature profiles for operation over the –40 °C to +105 °C ambient temperature range. Contact the regional FAEs for assistance.

System Resources

Power-on-Reset (POR) with Brown Out

Table 31. Imprecise Power On Reset (PRES)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID185	$V_{RISEIPOR}$	Rising trip voltage	0.80	–	1.45	V	Guaranteed by characterization
SID186	$V_{FALLIPOR}$	Falling trip voltage	0.75	–	1.4	V	Guaranteed by characterization
SID187	$V_{IPORHYST}$	Hysteresis	15	–	200	mV	Guaranteed by characterization

Table 32. Precise Power On Reset (POR)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID190	$V_{FALLPPOR}$	BOD trip voltage in active and sleep modes	1.64	–	–	V	Guaranteed by characterization
SID192	$V_{FALLDPSLP}$	BOD trip voltage in Deep Sleep	1.4	–	–	V	Guaranteed by characterization

Voltage Monitors

Table 33. Voltage Monitors DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID195	V_{LVI1}	LVI_A/D_SEL[3:0] = 0000b	1.71	1.75	1.79	V	–
SID196	V_{LVI2}	LVI_A/D_SEL[3:0] = 0001b	1.76	1.80	1.85	V	–
SID197	V_{LVI3}	LVI_A/D_SEL[3:0] = 0010b	1.85	1.90	1.95	V	–
SID198	V_{LVI4}	LVI_A/D_SEL[3:0] = 0011b	1.95	2.00	2.05	V	–
SID199	V_{LVI5}	LVI_A/D_SEL[3:0] = 0100b	2.05	2.10	2.15	V	–
SID200	V_{LVI6}	LVI_A/D_SEL[3:0] = 0101b	2.15	2.20	2.26	V	–
SID201	V_{LVI7}	LVI_A/D_SEL[3:0] = 0110b	2.24	2.30	2.36	V	–
SID202	V_{LVI8}	LVI_A/D_SEL[3:0] = 0111b	2.34	2.40	2.46	V	–
SID203	V_{LVI9}	LVI_A/D_SEL[3:0] = 1000b	2.44	2.50	2.56	V	–
SID204	V_{LVI10}	LVI_A/D_SEL[3:0] = 1001b	2.54	2.60	2.67	V	–
SID205	V_{LVI11}	LVI_A/D_SEL[3:0] = 1010b	2.63	2.70	2.77	V	–
SID206	V_{LVI12}	LVI_A/D_SEL[3:0] = 1011b	2.73	2.80	2.87	V	–
SID207	V_{LVI13}	LVI_A/D_SEL[3:0] = 1100b	2.83	2.90	2.97	V	–
SID208	V_{LVI14}	LVI_A/D_SEL[3:0] = 1101b	2.93	3.00	3.08	V	–
SID209	V_{LVI15}	LVI_A/D_SEL[3:0] = 1110b	3.12	3.20	3.28	V	–
SID210	V_{LVI16}	LVI_A/D_SEL[3:0] = 1111b	4.39	4.50	4.61	V	–
SID211	LVI_IDD	Block current	–	–	100	µA	Guaranteed by characterization

Table 34. Voltage Monitors AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID212	$T_{MONTRIP}$	Voltage monitor trip time	–	–	1	µs	Guaranteed by characterization

SWD Interface

Table 35. SWD Interface Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID213	F_SWDCLK1	3.3 V ≤ V_{DD} ≤ 5.5 V	–	–	14	MHz	SWDCLK ≤ 1/3 CPU clock frequency
SID214	F_SWDCLK2	1.71 V ≤ V_{DD} ≤ 3.3 V	–	–	7	MHz	SWDCLK ≤ 1/3 CPU clock frequency
SID215	T_SWDI_SETUP	T = 1/f SWDCLK	0.25 * T	–	–	ns	Guaranteed by characterization
SID216	T_SWDI_HOLD	T = 1/f SWDCLK	0.25 * T	–	–	ns	Guaranteed by characterization
SID217	T_SWDO_VALID	T = 1/f SWDCLK	–	–	0.5 * T	ns	Guaranteed by characterization
SID217A	T_SWDO_HOLD	T = 1/f SWDCLK	1	–	–	ns	Guaranteed by characterization

Internal Main Oscillator

Table 36. IMO DC Specifications

(Guaranteed by Design)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID218	I_{IMO1}	IMO operating current at 48 MHz	–	–	1000	µA	–
SID219	I_{IMO2}	IMO operating current at 24 MHz	–	–	325	µA	–
SID220	I_{IMO3}	IMO operating current at 12 MHz	–	–	225	µA	–
SID221	I_{IMO4}	IMO operating current at 6 MHz	–	–	180	µA	–
SID222	I_{IMO5}	IMO operating current at 3 MHz	–	–	150	µA	–

Table 37. IMO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID223	$F_{IMOTOL1}$	Frequency variation from 3 to 48 MHz	–	–	±2	%	±3% if T_A > 85 °C and IMO frequency < 24 MHz
SID226	$T_{STARTIMO}$	IMO startup time	–	–	12	µs	–
SID227	$T_{JITRMSIMO1}$	RMS Jitter at 3 MHz	–	156	–	ps	–
SID228	$T_{JITRMSIMO2}$	RMS Jitter at 24 MHz	–	145	–	ps	–
SID229	$T_{JITRMSIMO3}$	RMS Jitter at 48 MHz	–	139	–	ps	–

Internal Low-Speed Oscillator

Table 38. ILO DC Specifications

(Guaranteed by Design)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID231	I_{ILO1}	ILO operating current at 32 kHz	–	0.3	1.05	µA	Guaranteed by Characterization
SID233	$I_{ILOLEAK}$	ILO leakage current	–	2	15	nA	Guaranteed by Design

Table 39. ILO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID234	$T_{STARTILO1}$	ILO startup time	–	–	2	ms	Guaranteed by characterization
SID236	$T_{ILODUTY}$	ILO duty cycle	40	50	60	%	Guaranteed by characterization
SID237	$F_{ILOTRIM1}$	32-kHz trimmed frequency	15	32	50	kHz	Max ILO frequency is 70 kHz if T_A > 85 °C

Table 40. External Clock Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID305	ExtClkFreq	External Clock input Frequency	0	–	48	MHz	Guaranteed by characterization
SID306	ExtClkDuty	Duty cycle; Measured at $V_{DD/2}$	45	–	55	%	Guaranteed by characterization

Table 41. Watch Crystal Oscillator (WCO) Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
IMO WCO-PLL Calibrated Mode							
SID330	IMO_{WCO1}	Frequency variation with IMO set to 3 MHz	–0.6	–	0.6	%	Does not include WCO tolerance
SID331	IMO_{WCO2}	Frequency variation with IMO set to 5 MHz	–0.4	–	0.4	%	Does not include WCO tolerance
SID332	IMO_{WCO3}	Frequency variation with IMO set to 7 MHz or 9 MHz	–0.3	–	0.3	%	Does not include WCO tolerance
SID333	IMO_{WCO4}	All other IMO frequency settings	–0.2	–	0.2	%	Does not include WCO tolerance
WCO Specifications							
SID398	F_{WCO}	Crystal frequency	–	32.768		kHz	–
SID399	F_{TOL}	Frequency tolerance	–	50	250	ppm	With 20-ppm crystal.
SID400	ESR	Equivalent series resistance	–	50	–	kΩ	–
SID401	PD	Drive level	–	–	1	µW	–
SID402	T_{START}	Startup time	–	–	500	ms	–
SID403	C_L	Crystal load capacitance	6	–	12.5	pF	–
SID404	C_0	Crystal shunt capacitance	–	1.35	–	pF	–
SID405	I_{WCO1}	Operating current (high power mode)	–	–	8	µA	–

Table 42. UDB AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
Datapath Performance							
SID249	$F_{MAX-TIMER}$	Max frequency of 16-bit timer in a UDB pair	–	–	48	MHz	–
SID250	$F_{MAX-ADDER}$	Max frequency of 16-bit adder in a UDB pair	–	–	48	MHz	–
SID251	F_{MAX_CRC}	Max frequency of 16-bit CRC/PRS in a UDB pair	–	–	48	MHz	–
PLD Performance in UDB							
SID252	F_{MAX_PLD}	Max frequency of 2-pass PLD function in a UDB pair	–	–	48	MHz	–
Clock to Output Performance							
SID253	$T_{CLK\_OUT\_UDB1}$	Prop. delay for clock in to data out at 25 °C, Typ.	–	15	–	ns	–
SID254	$T_{CLK\_OUT\_UDB2}$	Prop. delay for clock in to data out, Worst case.	–	25	–	ns	–

Table 43. Block Specs

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID256[6]	T_{WS48}	Number of wait states at 48 MHz	2	–	–		CPU execution from Flash
SID257[6]	T_{WS24}	Number of wait states at 24 MHz	1	–	–		CPU execution from Flash
SID260	V_{REFSAR}	Trimmed internal reference to SAR	–1	–	+1	%	Percentage of Vbg (1.024 V). Guaranteed by characterization.
SID261	$F_{SARINTREF}$	SAR operating speed without external reference bypass	–	–	100	ksps	12-bit resolution. Guaranteed by characterization.
SID262	$T_{CLKSWITCH}$	Clock switching from clk1 to clk2 in clk1 periods	3	–	4	Periods	Guaranteed by design

Table 44. UDB Port Adaptor Specifications

(Based on LPC Component Specs, Guaranteed by Characterization -10-pF load, 3-V V_{DDIO} and V_{DDD})

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID263	T_{LCLKDO}	LCLK to output delay	–	–	18	ns	–
SID264	$T_{DINLCLK}$	Input setup time to LCLCK rising edge	–	–	7	ns	–
SID265	$T_{DINLCLKHLD}$	Input hold time from LCLK rising edge	0	–	–	ns	–
SID266	$T_{LCLKHIZ}$	LCLK to output tristated	–	–	28	ns	–
SID267	T_{FLCLK}	LCLK frequency	–	–	33	MHz	–
SID268	$T_{LCLKDUTY}$	LCLK duty cycle (percentage high)	40	–	60	%	–

Note
6. Tws48 and Tws24 are guaranteed by Design.

Table 45. CAN Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID420	IDD_CAN	Block current consumption	–	–	200	µA	–
SID421	CAN_bits	CAN Bit rate (Min. 8 MHZ clock)	–	–	1	Mbit/s	–

Ordering Information

Table 46 lists the PSoC 4200M family part numbers and features.

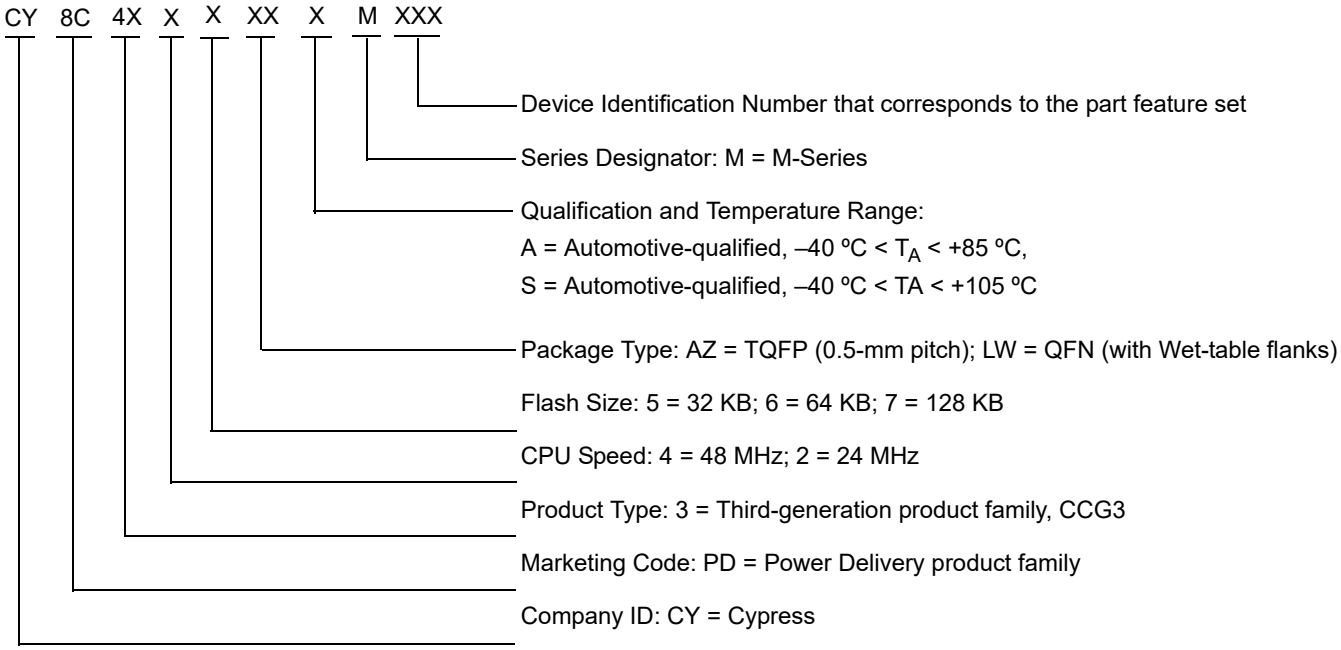
Table 46. Ordering Information

Category	MPN	Features													Package			Temperature Range	
		Max CPU Speed (MHz)	Flash (KB)	SRAM (KB)	UDB	Opamp (CTBm)	CapSense	Direct LCD Drive	12-bit SAR ADC	LP Comparators	TCPWM Blocks	SCB Blocks	CAN	GPIO	48-TQFP	64-TQFP (0.5mm pitch)	56-QFN (W/F)	–40 to +85 °C	–40 to +105 °C
4245	CY8C4245AZA-M443	48	32	4	4	2	✔	✔	1000 ksps	2	8	4	–	38	✔	–	–	✔	–
	CY8C4245AZA-M445	48	32	4	4	2	✔	✔	1000 ksps	2	8	4	–	51	–	✔	–	✔	–
4246	CY8C4246AZA-M443	48	64	8	4	2	✔	✔	1000 ksps	2	8	4	–	38	✔	–	–	✔	–
	CY8C4246AZA-M445	48	64	8	4	2	✔	✔	1000 ksps	2	8	4	–	51	–	✔	–	✔	–
4247	CY8C4247LWA-M464	48	128	16	4	4	✔	✔	1000 ksps	2	8	4	–	46	–	–	✔	✔	–
	CY8C4247AZA-M475	48	128	16	4	4	–	✔	1000 ksps	2	8	4	–	51	–	✔	–	✔	–
	CY8C4247AZA-M483	48	128	16	4	4	✔	✔	1000 ksps	2	8	4	2	38	✔	–	–	✔	–
	CY8C4247AZA-M485	48	128	16	4	4	✔	✔	1000 ksps	2	8	4	2	51	–	✔	–	✔	–
	CY8C4247LWA-M484	48	128	16	4	4	✔	✔	1000 ksps	2	8	4	2	46	–	–	✔	✔	–
4245	CY8C4245AZS-M443	48	32	4	4	2	✔	✔	1000 ksps	2	8	4	–	38	✔	–	–	–	✔
	CY8C4245AZS-M445	48	32	4	4	2	✔	✔	1000 ksps	2	8	4	–	51	–	✔	–	–	✔
4246	CY8C4246AZS-M443	48	64	8	4	2	✔	✔	1000 ksps	2	8	4	–	38	✔	–	–	–	✔
	CY8C4246AZS-M445	48	64	8	4	2	✔	✔	1000 ksps	2	8	4	–	51	–	✔	–	–	✔
4247	CY8C4247LWS-M464	48	128	16	4	4	✔	✔	1000 ksps	2	8	4	–	46	–	–	✔	–	✔
	CY8C4247AZS-M475	48	128	16	4	4	–	✔	1000 ksps	2	8	4	–	51	–	✔	–	–	✔
	CY8C4247AZS-M483	48	128	16	4	4	✔	✔	1000 ksps	2	8	4	2	38	✔	–	–	–	✔
	CY8C4247AZS-M485	48	128	16	4	4	✔	✔	1000 ksps	2	8	4	2	51	–	✔	–	–	✔
	CY8C4247LWS-M484	48	128	16	4	4	✔	✔	1000 ksps	2	8	4	2	46	–	–	✔	–	✔

The nomenclature used in Table 46 is based on the following part numbering convention:

Field	Description	Values	Meaning
CY8C	Cypress Prefix		
4	Architecture	4	PSoC 4
A	Family	2	4200 Family
B	CPU Speed	4	48 MHz
C	Flash Capacity	5	32 KB
		6	64 KB
		7	128 KB
DE	Package Code	AZ	TQFP
		LW	QFN
F	Temperature Range	A	AEC-Q100: –40 °C to +85 °C
		S	AEC-Q100: –40 °C to +105 °C
S	Silicon Family	N/A	PSoC 4 Base Series
		M	PSoC 4 M-Series
XYZ	Attributes Code	000-999	Code of feature set in the specific family

Ordering Code Definitions



Packaging

Table 47 provides the description of the PSoC4200M package dimensions.

Table 47. PSoC4200M Package Dimensions

Spec ID	Package	Description	Package Number
PKG_2	64-pin TQFP	64 TQFP, 10 mm × 10 mm × 1.4 mm height with 0.5 mm pitch	51-85051
PKG_5	48-pin TQFP	48 TQFP, 7 mm × 7 mm × 1.4 mm height with 0.5 mm pitch	51-85135
PKG_6	56-pin QFN	56 QFN, 8 mm × 8 mm × 1.0 mm height with 0.5 mm pitch	001-76517

Table 48. Package Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
T_A	Operating ambient temperature	For Grade-A devices	–40	25	85	°C
		For Grade-S devices	–40	25	105	°C
TJ	Operating junction temperature	For Grade-A devices	–40	–	100	°C
		For Grade-S devices	–40	–	130	°C
TJA	Package θ_{JA} (64-pin TQFP, 0.5-mm pitch)	–	–	56	–	°C/Watt
TJC	Package θ_{JC} (64-pin TQFP, 0.5-mm pitch)	–	–	19.5	–	°C/Watt
TJA	Package θ_{JA} (48-pin TQFP, 0.5-mm pitch)	–	–	67.3	–	°C/Watt
TJC	Package θ_{JC} (48-pin TQFP, 0.5-mm pitch)	–	–	30.4	–	°C/Watt
TJA	Package θ_{JA} (56-pin QFN, 0.5-mm pitch)	–	–	39.4	–	°C/Watt
TJC	Package θ_{JC} (56-pin QFN, 0.5-mm pitch)	–	–	3.58	–	°C/Watt

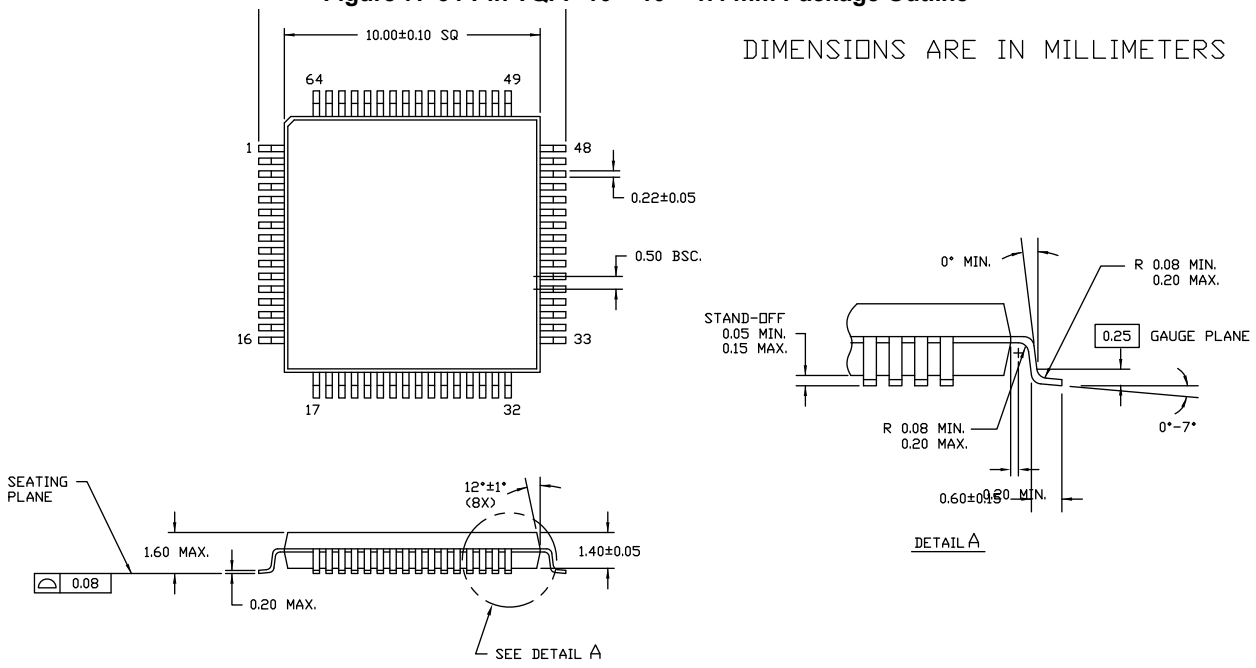
Table 49. Solder Reflow Peak Temperature

Package	Maximum Peak Temperature	Maximum Time at Peak Temperature
All packages	260 °C	30 seconds

Table 50. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2

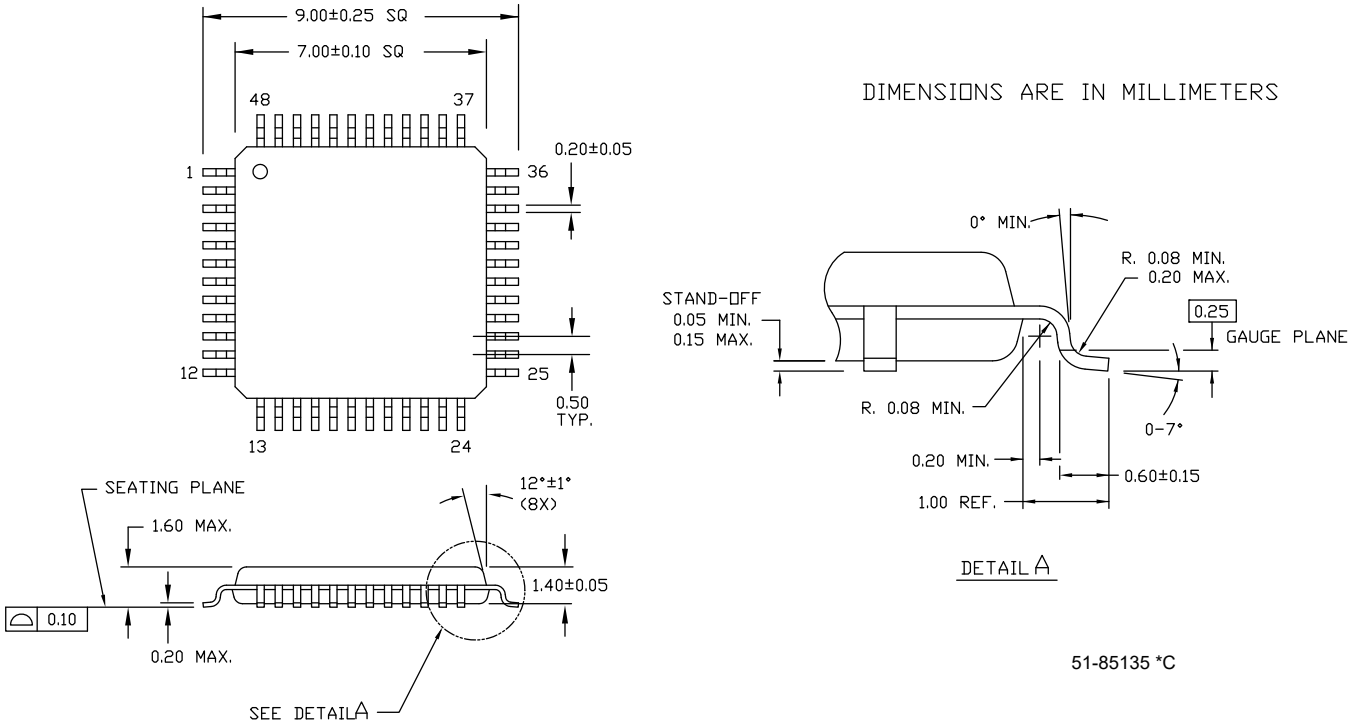
Package	MSL
All packages	MSL 3

Figure 7. 64-Pin TQFP 10 × 10 × 1.4 mm Package Outline



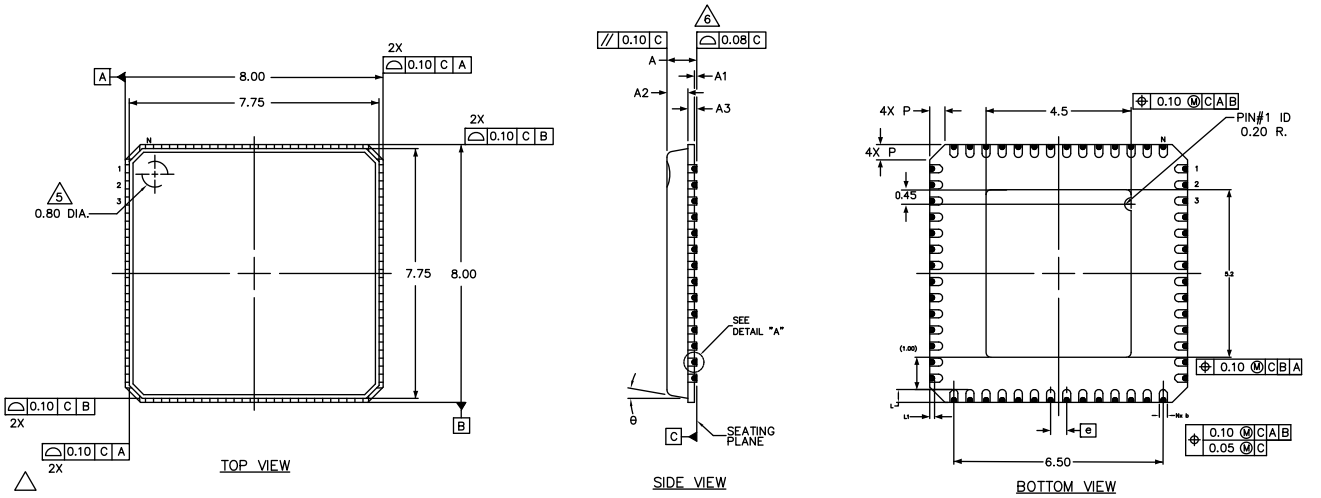
51-85051 *D

Figure 8. 48-Pin 7 × 7 × 1.4 mm TQFP Package Outline



51-85135 *C

Figure 9. 56L QFN 8 × 8 × 1.0 mm LW56 4.5 × 5.2 EPAD (Subcon Punch QFN, Wettable Flanks Package) Package Outline



SYMBOL	COMMON DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A	0.80	0.85	0.90	
A1	0.00	0.01	0.05	6
A2	0.60	0.65	0.70	
A3		0.20 REF		
θ	0	–	12°	
P	0.24	0.42	0.60	
e		0.50 BSC		
N		56		3
L	0.30	0.40	0.50	
L1	0.05	0.15	0.25	
L2	0.05	0.10	0.15	
b	0.20	0.25	0.30	
b1	0.10	0.15	0.20	

NOTES:
1. DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM (0.012 INCHES MAXIMUM)
2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. –1994.
3. N IS THE NUMBER OF TERMINALS
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST BE EXISTED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
6. UNILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS

001-76517 *A

Acronyms

Table 51. Acronyms Used in this Document

Acronym	Description
abus	analog local bus
ADC	analog-to-digital converter
AG	analog global
AHB	AMBA (advanced microcontroller bus architecture) high-performance bus, an ARM data transfer bus
ALU	arithmetic logic unit
AMUXBUS	analog multiplexer bus
API	application programming interface
APSR	application program status register
ARM®	advanced RISC machine, a CPU architecture
ATM	automatic thump mode
BW	bandwidth
CAN	Controller Area Network, a communications protocol
CMRR	common-mode rejection ratio
CPU	central processing unit
CRC	cyclic redundancy check, an error-checking protocol
DAC	digital-to-analog converter, see also IDAC, VDAC
DFB	digital filter block
DIO	digital input/output, GPIO with only digital capabilities, no analog. See GPIO.
DMIPS	Dhrystone million instructions per second
DMA	direct memory access, see also TD
DNL	differential nonlinearity, see also INL
DNU	do not use
DR	port write data registers
DSI	digital system interconnect
DWT	data watchpoint and trace
ECC	error correcting code
ECO	external crystal oscillator
EEPROM	electrically erasable programmable read-only memory
EMI	electromagnetic interference
EMIF	external memory interface
EOC	end of conversion
EOF	end of frame
EPSR	execution program status register
ESD	electrostatic discharge

Table 51. Acronyms Used in this Document *(continued)*

Acronym	Description
ETM	embedded trace macrocell
FIR	finite impulse response, see also IIR
FPB	flash patch and breakpoint
FS	full-speed
GPIO	general-purpose input/output, applies to a PSoC pin
HVI	high-voltage interrupt, see also LVI, LVD
IC	integrated circuit
IDAC	current DAC, see also DAC, VDAC
IDE	integrated development environment
I^2C, or IIC	Inter-Integrated Circuit, a communications protocol
IIR	infinite impulse response, see also FIR
ILO	internal low-speed oscillator, see also IMO
IMO	internal main oscillator, see also ILO
INL	integral nonlinearity, see also DNL
I/O	input/output, see also GPIO, DIO, SIO, USBIO
IPOR	initial power-on reset
IPSR	interrupt program status register
IRQ	interrupt request
ITM	instrumentation trace macrocell
LCD	liquid crystal display
LIN	Local Interconnect Network, a communications protocol.
LR	link register
LUT	lookup table
LVD	low-voltage detect, see also LVI
LVI	low-voltage interrupt, see also HVI
LVTTL	low-voltage transistor-transistor logic
MAC	multiply-accumulate
MCU	microcontroller unit
MISO	master-in slave-out
NC	no connect
NMI	nonmaskable interrupt
NRZ	non-return-to-zero
NVIC	nested vectored interrupt controller
NVL	nonvolatile latch, see also WOL
opamp	operational amplifier
PAL	programmable array logic, see also PLD
PC	program counter
PCB	printed circuit board

Table 51. Acronyms Used in this Document *(continued)*

Acronym	Description
PGA	programmable gain amplifier
PHUB	peripheral hub
PHY	physical layer
PICU	port interrupt control unit
PLA	programmable logic array
PLD	programmable logic device, see also PAL
PLL	phase-locked loop
PMDD	package material declaration data sheet
POR	power-on reset
PRES	precise power-on reset
PRS	pseudo random sequence
PS	port read data register
PSoC®	Programmable System-on-Chip™
PSRR	power supply rejection ratio
PWM	pulse-width modulator
RAM	random-access memory
RISC	reduced-instruction-set computing
RMS	root-mean-square
RTC	real-time clock
RTL	register transfer language
RTR	remote transmission request
RX	receive
SAR	successive approximation register
SC/CT	switched capacitor/continuous time
SCL	I^2C serial clock
SDA	I^2C serial data
S/H	sample and hold
SINAD	signal to noise and distortion ratio
SIO	special input/output, GPIO with advanced features. See GPIO.
SOC	start of conversion
SOF	start of frame
SPI	Serial Peripheral Interface, a communications protocol
SR	slew rate
SRAM	static random access memory
SRES	software reset
SWD	serial wire debug, a test protocol
SWV	single-wire viewer
TD	transaction descriptor, see also DMA

Table 51. Acronyms Used in this Document *(continued)*

Acronym	Description
THD	total harmonic distortion
TIA	transimpedance amplifier
TRM	technical reference manual
TTL	transistor-transistor logic
TX	transmit
UART	Universal Asynchronous Transmitter Receiver, a communications protocol
UDB	universal digital block
USB	Universal Serial Bus
USBIO	USB input/output, PSoC pins used to connect to a USB port
VDAC	voltage DAC, see also DAC, IDAC
WDT	watchdog timer
WOL	write once latch, see also NVL
WRES	watchdog timer reset
XRES	external reset I/O pin
XTAL	crystal

Document Conventions

Units of Measure

Table 52. Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
dB	decibel
fF	femto farad
Hz	hertz
KB	1024 bytes
kbps	kilobits per second
Khr	kilohour
kHz	kilohertz
kΩ	kilo ohm
ksps	kilosamples per second
LSB	least significant bit
Mbps	megabits per second
MHz	megahertz
MΩ	mega-ohm
Msps	megasamples per second
µA	microampere
µF	microfarad
µH	microhenry
µs	microsecond
µV	microvolt
µW	microwatt
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
nV	nanovolt
Ω	ohm
pF	picofarad
ppm	parts per million
ps	picosecond
s	second
sps	samples per second
sqrtHz	square root of hertz
V	volt

Revision History

Description Title: Automotive PSoC® 4: PSoC 4200M Family Datasheet, Programmable System-on-Chip (PSoC®) Document Number: 002-09829				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	5020952	SNPR	11/19/2015	New datasheet
*A	5142819	SNPR	02/18/2016	Updated Features, Pinouts, Device Level Specifications, and Ordering Information. Updated Table 15, Table 30, and Table 48. Added Figure 9 (spec 001-76517 *A) in Ordering Information. Updated Sales, Solutions, and Legal Information with new disclaimer and links.
*B	5508775	SNPR	11/03/2016	Updated Copyright and Disclaimer. Updated Package Options in Features. Updated More Information, Ordering Information, More Information. Updated Table 5, Table 11, Table 14, Table 15, Table 16, Table 30, Table 47, and Table 48. Added Notes 4 and 5. Updated Copyright and Disclaimer.
*C	5631190	SNPR	02/14/2017	DC Specifications: Added temperature range for Sleep Mode. Added specs for +105 °C for Deep Sleep and Hibernate modes. Added SID182B. Added conditions for SID223 and SID237.
*D	5978198	SNPR	11/28/2017	Updated the Cypress logo. Added the PSoC 6 link under PSoC® Solutions.
*E	6560860	SNPR	04/29/2019	Removed Preliminary status. Removed Grade-E temperature range.

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