PSoC™ 4 MCU: PSoC™ 4000T datasheet

Based on Arm® Cortex®-M0+ CPU

General description

PSoC™ 4 is a family of scalable MCUs with an Arm® Cortex®-M0+ CPU. It combines a high-performance capacitive sensing subsystem, programmable and reconfigurable analog and digital blocks. The new PSoC™ 4000T series provides an upgrade path for PSoC™ 4000 and PSoC™ 4000S based designs to fifth-generation HMI technology with software and package compatibility.

PSoC™ 4000T is a member of the PSoC™ 4 MCU family with fifth-generation CAPSENSE™ and multi-sense technology offering ultra-low power touch HMI solution based on an integrated “Always-On” sensing technology, improved performance to enable modern sleek user interface solutions with superior liquid tolerance and provides robust and reliable touch HMI solution for harsh environments.

PSoC™ 4000T is a microcontroller with standard communication, timing peripherals and Infineon’s fifth-generation CAPSENSE™ and multi-sense HMI technology purpose built for varieties of low power applications including wearable, hearable and smart connected IoT products that needs low power operation and improved performance to enable next generation of user experience.

Features

- 32-bit MCU subsystem
  - 48-MHz Arm® Cortex®-M0+ CPU with single-cycle multiply
  - Up to 64 KB of flash with read accelerator
  - Up to 8 KB of SRAM
- Low-power 1.71 V to 5.5 V operation
  - Deep sleep mode with 6 µA always-on touch sensing
  - Active touch detection and tracking with 200 µA (average)
- Fifth-generation CAPSENSE™ sensing
  - All-new ratio-metric sensing architecture in Multi-Sense Converter Low Power (MSCLP) provides best-in-class signal-to-noise ratio (SNR) (>5:1) and liquid tolerance for capacitive sensing.
  - “Always-On” sensing in Deep Sleep mode with hardware-based wake on touch detection for ultra-low power operation in standby mode.
  - Autonomous channel scanning without assistance from the MCU core for low power optimization with active touch detection and tracking
  - Advanced proximity sensing with directivity with machine learning based algorithms
  - Infineon-supplied software middleware makes capacitive sensing design easy
  - Automatic hardware tuning (SmartSense)
- Serial communication
  - Two independent runtime reconfigurable serial communication blocks (SCBs) with re-configurable I^2C, SPI, or UART functionality in one block with master/slave I^2C functionality in the other.
- Timing and pulse-width modulation
  - Two 16-bit timer/counter/pulse-width modulator (TCPWM) blocks
  - Center-aligned, edge, and pseudo-random modes
  - Comparator-based triggering of kill signals
  - Quadrature decoder
- Clock sources
  - ±2% Internal main oscillator (IMO)
  - 40 kHz Internal low-power oscillator (ILO)

Features

- Up to 21 programmable GPIO pins
  - 25-pin WLCSP (0.35 mm pitch), 24-pin QFN (0.5 mm pitch), and a 16-pin QFN package (0.5 mm pitch).
  - GPIO pins can have sensing or digital functionality
- ModusToolbox™ software
  - Comprehensive collection of multi-platform tools and software libraries
  - Includes board support packages (BSPs), peripheral driver library (PDL), and middleware such as CAPSENSE™
- Industry-standard tool compatibility
  - After configuration, development can be done with Arm®-based industry-standard development tools

Development ecosystem

PSoC™ 4 MCU resources

Infineon® provides a wealth of data at **www.infineon.com** to help you select the right PSoC™ MCU device and quickly and effectively integrate it into your design. The following is an abbreviated, hyperlinked list of resources for PSoC™ 4 MCU:

- **Overview: PSoC™ portfolio**
- **Product selectors: PSoC™ 4 MCU**
- **Application notes** cover a broad range of topics, from basic to advanced level; please refer to the following when using this device:
  - **AN79953**: Getting started with PSoC™ 4
  - **AN88619**: PSoC™ 4 MCU hardware design considerations
  - **AN85951**: - PSoC™ 4 and PSoC™ 6 MCU CAPSENSE™ design guide
  - **AN234231**: Achieving lowest power capacitive and inductive sensing with PSoC™ 4000T
  - **AN86233**: PSoC™ 4 MCU power reduction techniques
- **Code examples** demonstrate product features and usage, and are also available on **GitHub repositories**.
- **Technical reference manuals (TRMs)** provide detailed descriptions of PSoC™ 4 MCU architecture and registers.
- **PSoC™ 4 MCU programming specification** provides the information necessary to program PSoC™ 4 MCU nonvolatile memory.
- **Development tools**
  - **ModusToolbox™ software** enables cross platform code development with a robust suite of tools and software libraries.
  - Evaluation, system solution, and development kits will be available for the PSoC™ 4000T at product release.
  - The CY8CKIT-040T PSoC™ 4000T CAPSENSE™ evaluation kit enables you to evaluate and develop with Infineon's fifth-generation, low-power CAPSENSE™ solution using the PSoC™ 4000T device.
  - **MiniProg4** and **MiniProg3** all-in-one development programmers and debuggers.
  - **PSoC™ 4 MCU CAD libraries** provide footprint and schematic support for common tools. **IBIS models** are also available.
- **Training videos** are available on a wide range of topics including the **PSoC™ 101 series**.
- **Infineon developer community** enables connection with fellow PSoC™ developers around the world, 24 hours a day, 7 days a week, and hosts a dedicated **PSoC™ 4 MCU community**.
- WLCSP bootloader package
  The WLCSP bootloader package is supplied with an I2C bootloader installed in flash. The bootloader is compatible with the ModusToolbox™ DFU middleware and has the following default configurations:
  - I2C SCL and SDA connected to port pins P2.2 and P2.3 respectively (external pull-up resistors required)
  - I2C Slave mode, address 0x0C, data rate = 400 Kbps
  - Occupies the bottom 12.5 KB of flash, 0x00000000 to 0x00003200
  - Supports single application, starting from 0x00003200 to max flash size of the variant minus 256 bytes (this 256 bytes is bootloader metadata)
  - Bootloader mode timeout is 2 seconds
  - Features a device-specific Product ID to verify flashing of the application image on the intended target. The Product ID is a four-byte value pre-programmed in the bootloader, where the first 2 bytes (MSB first) are the Silicon ID, and the next two bytes are the bootloader version (0x0002).
  - Other bootloader options are set by the ModusToolbox™ DFU middleware default option

  For more information on this bootloader, see the following application note:
  - **AN236282** - Device Firmware Update (DFU) middleware (MW) for ModusToolbox™

Note that a ModusToolbox™ bootloadable project must be associated with *.hex*, *.cyacd2,* and *.elf* files for the bootloader project that is configured for the target device. The factory-installed bootloader can be overwritten using JTAG or SWD programming.

ModusToolbox™ software

ModusToolbox™ software is comprehensive collection of multi-platform tools and software libraries that enable an immersive development experience for creating converged MCU and wireless systems. It is:

- Comprehensive - it has the resources you need
- Flexible - you can use the resources in your own workflow
- Atomic - you can get just the resources you want

Infineon provides a large collection of code **repositories on GitHub**, including:

- Board support packages (BSPs) aligned with Infineon kits
- Low-level resources, including a peripheral driver library (PDL)
- Middleware enabling industry-leading features such as CAPSENSE™
- An extensive set of thoroughly tested **code example applications**

ModusToolbox™ software is IDE-neutral and easily adaptable to your workflow and preferred development environment. It includes a project creator, peripheral and library configurators, a library manager, as well as the optional Eclipse IDE for ModusToolbox™ software, as **Figure 1** shows. For information on using Infineon tools, refer to the documentation delivered with ModusToolbox™ software, and **AN79953: Getting started with PSoC™ 4**.

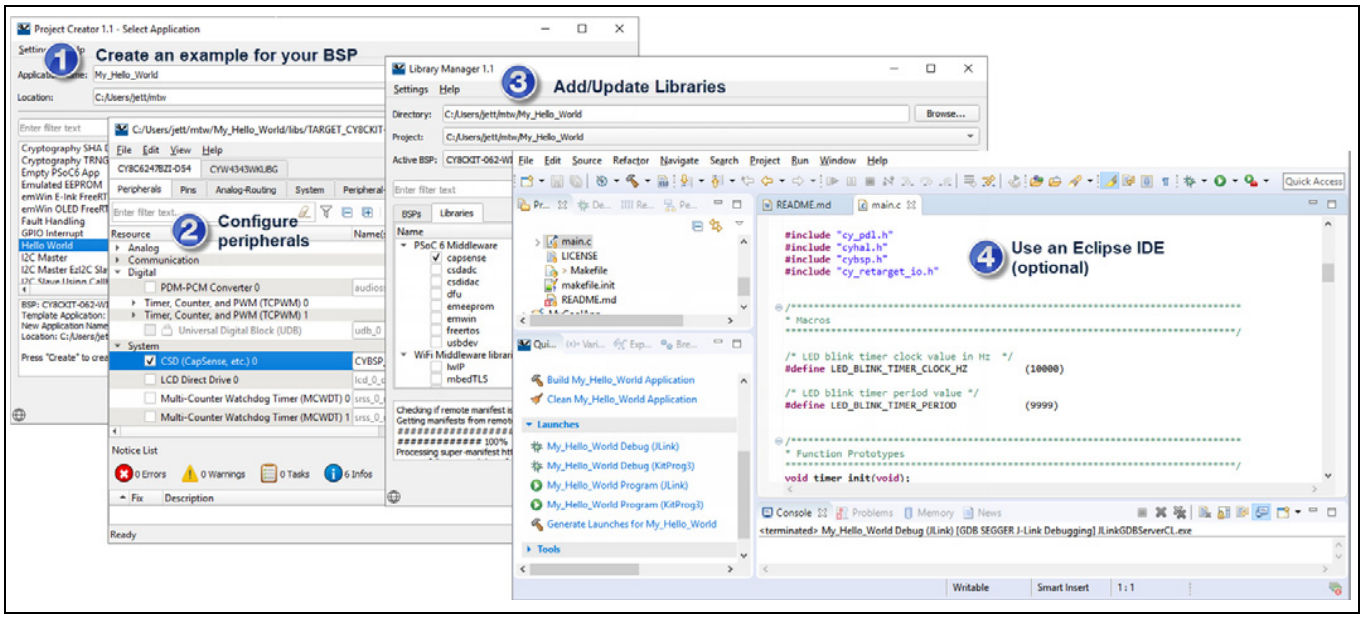

Figure 1 ModusToolbox™ software tools

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Block diagram

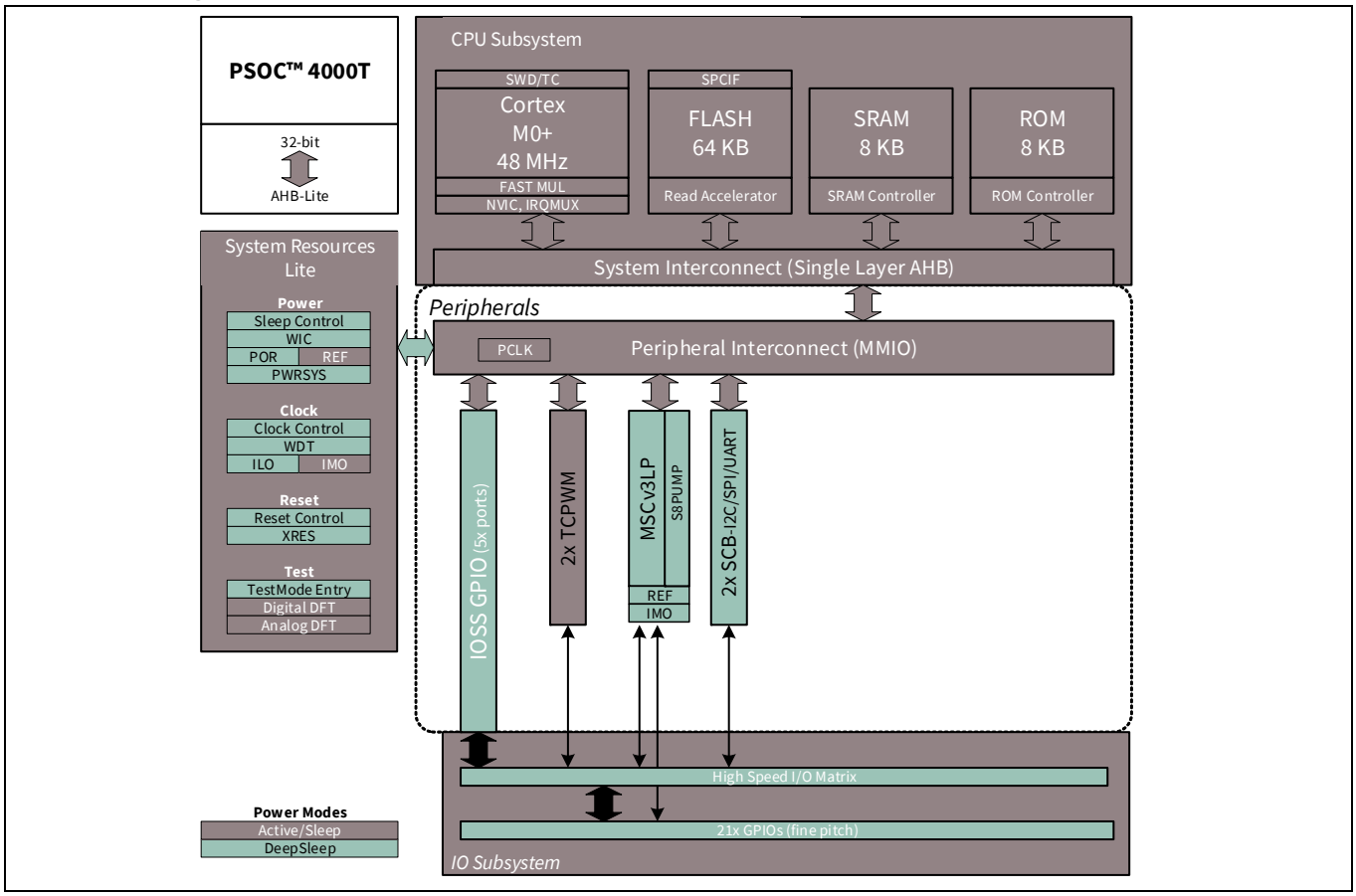


Figure 2 Block diagram

This device includes extensive support for programming, testing, debugging, and tracing both hardware and firmware.

The Arm® serial-wire debug (SWD) interface supports all programming and debug features of the device.

Complete debug-on-chip functionality enables full-device debugging in the final system using the standard production device. It does not require special interfaces, debugging pods, simulators, or emulators. Only the standard programming connections are required to fully support debug.

The ModusToolbox™ IDE provides fully integrated programming and debug support for this device. The SWD interface is fully compatible with industry-standard third-party tools. It has the following advantages:

- Allows disabling of debug features
- Robust flash protection
- Allows customer-proprietary functionality to be implemented in on-chip programmable blocks

The debug circuits are enabled by default and can be disabled in firmware. If they are not enabled, the only way to re-enable them is to erase the entire device if not erase protected, clear flash protection, and reprogram the device with new firmware that enables debugging. Thus firmware control of debugging cannot be over-ridden without erasing the firmware thus providing security.

Additionally, all device interfaces can be permanently disabled (device security) for applications concerned about phishing attacks due to a maliciously reprogrammed device or attempts to defeat security by starting and interrupting flash programming sequences. All programming, debug, and test interfaces are disabled when maximum device security is enabled. Therefore, this device, with device security enabled, may not be returned for failure analysis. This is a trade-off it allows the customer to make.

1 Functional definition

1.1 CPU and memory subsystem

1.1.1 CPU

The Cortex®-M0+ CPU in PSoC™ 4000T is part of the 32-bit MCU subsystem, which is optimized for low-power operation with extensive clock gating. Most instructions are 16 bits in length and the CPU executes a subset of the thumb-2 instruction set. It includes a nested vectored interrupt controller (NVIC) block with eight interrupt inputs and also includes a wakeup interrupt controller (WIC). The WIC can wake the processor from deep sleep mode, allowing power to be switched off to the main processor when the chip is in deep sleep mode.

The CPU subsystem includes the serial wire debug (SWD) interface, which is a two-wire form of JTAG. The debug configuration used for PSoC™ 4000T has four breakpoint (address) comparators and two watchpoint (data) comparators.

1.1.2 Flash

The PSoC™ 4000T device has a 64 KB flash module with a flash accelerator, tightly coupled to the CPU to improve average access times from the flash block. The low-power flash block is designed to deliver two wait-state (WS) access time at 48 MHz. The flash accelerator delivers 85% of single-cycle SRAM access performance on average.

1.1.3 SRAM

8KB of SRAM are provided with zero wait-state access at 48 MHz.

1.1.4 SROM

An 8 KB supervisory ROM that contains boot and configuration routines is provided.

1.2 System resources

1.2.1 Power system

The power system is described in detail in the section **Power**. It provides assurance that voltage levels are as required for each respective mode and either delays mode entry (for example, on power-on reset (POR)) until voltage levels are as required for proper functionality, or generates resets (for example, on brown-out detection). It operates with a single external supply over the range of either 1.8 V ±5% (externally regulated) or 1.8 to 5.5 V (internally regulated) and has three different power modes, transitions between which are managed by the power system. PSoC™ 4000T provides active, sleep, and deep sleep low-power modes.

All subsystems are operational in active mode. The CPU subsystem (CPU, flash, and SRAM) is clock-gated off in sleep mode, while all peripherals and interrupts are active with instantaneous wake-up on a wake-up event. In deep sleep mode, the high-speed clock and associated circuitry is switched off; wake-up from this mode takes 35 µs. The touch sensing system can remain operational in Deep Sleep mode and provide an interrupt in wake-on-touch or proximity modes.

1.2.2 Clock system

The PSoC™ 4000T clock system is responsible for providing clocks to all subsystems that require clocks and for switching between different clock sources without glitching. In addition, the clock system ensures that there are no metastable conditions.

The clock system for the PSoC™ 4000T consists of the IMO, ILO, and provision for an external clock.

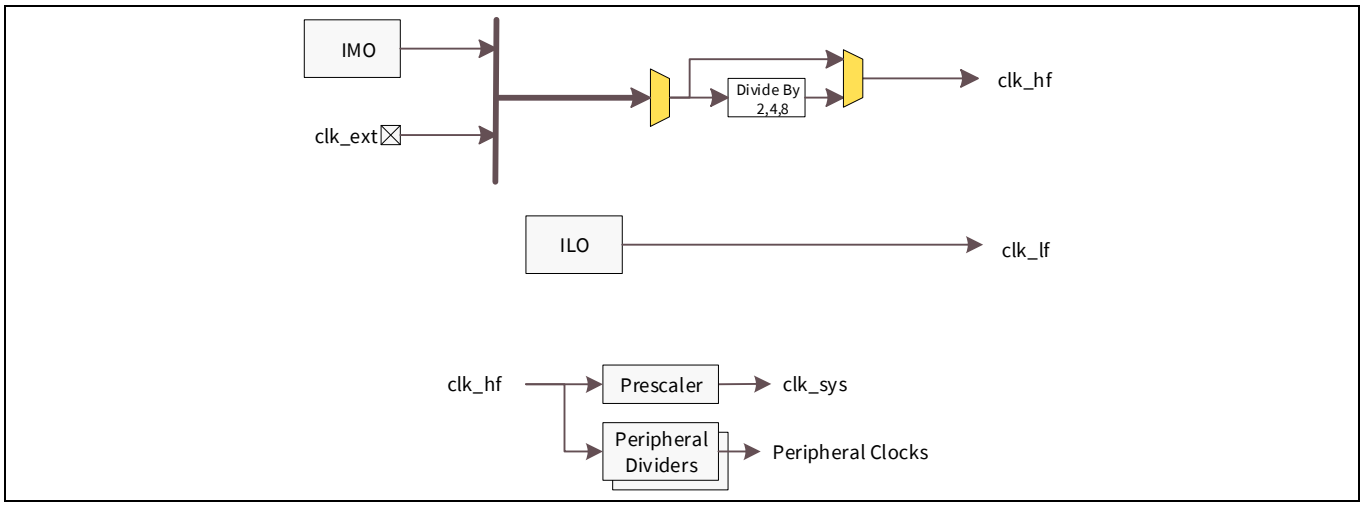


Figure 3 MCU clocking architecture

The HFCLK signal can be divided down as shown to generate synchronous clocks for the peripherals. There are four clock dividers for the PSoC™ 4000T. There are two 16-bit integer dividers allowing a lot of flexibility in generating fine-grained frequency values. And there is one 16.5-bit fractional dividers and one 24.5-bit fractional divider.

1.2.3 IMO clock source

The IMO is the primary source of internal clocking in the PSoC™ 4000T. It is trimmed during testing to achieve the specified accuracy.The IMO default frequency is 24 MHz and it can be adjusted from 24 to 48 MHz in steps of 4 MHz. The IMO tolerance is ±2% over the entire voltage and temperature range.

1.2.4 ILO clock source

The ILO is a very low power, nominally 40 kHz oscillator, which is primarily used to generate clocks for the watchdog timer (WDT) and peripheral operation in deep sleep mode. ILO-driven counters can be calibrated to the IMO to improve accuracy.

1.2.5 Watchdog timer and counters

A watchdog timer is implemented in the clock block running from the ILO; this allows watchdog operation during deep sleep and generates a watchdog reset if not serviced before the set timeout occurs. The watchdog reset is recorded in a reset cause register, which is firmware readable.

1.2.6 Reset

PSoC™ 4000T can be reset from a variety of sources including a software reset. Reset events are asynchronous and guarantee reversion to a known state. The reset cause is recorded in a register, which is sticky through reset and allows software to determine the cause of the reset. An XRES pin is reserved for external reset by asserting it active low. The XRES pin has an internal pull-up resistor that is always enabled.

1.3 Fixed function digital blocks

1.3.1 TCPWM block

The TCPWM block consists of a 16-bit counter with user-programmable period length. There is a capture register to record the count value at the time of an event (which may be an I/O event), a period register that is used to either stop or auto-reload the counter when its count is equal to the period register, and compare registers to generate compare value signals that are used as PWM duty cycle outputs. The block also provides true and complementary outputs with programmable offset between them to allow use as dead-band programmable complementary PWM outputs. It also has a kill input to force outputs to a predetermined state. Each block also incorporates a quadrature decoder. There are two TCPWM blocks in PSoC™ 4000T.

1.3.2 Serial communication block (SCB)

PSoC™ 4000T has two serial communication blocks, which can be programmed to have SPI, I^2C, or UART functionality. One block can operate in any mode, the other block is an I^2C master/slave block primarily intended to be the interface to a host.

1.3.2.1 I^2C mode

The hardware I^2C block implements a full multi-master and slave interface (it is capable of multi-master arbitration). This block is capable of operating at speeds of up to 1000 kbps (fast mode plus) and has flexible buffering options to reduce interrupt overhead and latency for the CPU. It also supports EZI2C that creates a mailbox address range in the memory of PSoC™ 4000T and effectively reduces I^2C communication to reading from and writing to an array in memory. In addition, the block supports an 8-deep FIFO for receive and transmit which, by increasing the time given for the CPU to read data, greatly reduces the need for clock stretching caused by the CPU not having read data on time.

The I^2C peripheral is compatible with the I^2C Standard-mode and Fast-mode devices as defined in the NXP I^2C-bus specification and user manual (UM10204). The I^2C bus I/O is implemented with GPIO in open-drain modes.

PSoC™ 4000T is not completely compliant with the I^2C spec in the following respect:

- GPIO cells are not overvoltage tolerant and, therefore, cannot be hot-swapped or powered up independently of the rest of the I^2C system.

1.3.2.2 UART mode

This is a full-feature UART operating at up to 1-Mbps. In addition, it supports the 9-bit multiprocessor mode that allows addressing of peripherals connected over common Rx and Tx lines. Common UART functions such as parity error, break detect, and frame error are supported. An 8-deep FIFO allows much greater CPU service latencies to be tolerated.

1.3.2.3 SPI mode

The SPI mode supports full Motorola SPI, TI SSP (adds a start pulse used to synchronize SPI Codecs), and National Microwire (half-duplex form of SPI). The SPI block can use the FIFO.

1.4 GPIO

PSoC™ 4000T has up to 21 GPIOs. The GPIO block implements the following:

- Eight drive modes:
  - Analog input mode (input and output buffers disabled)
  - Input only
  - Weak pull-up with strong pull-down
  - Strong pull-up with weak pull-down
  - Open drain with strong pull-down
  - Open drain with strong pull-up
  - Strong pull-up with strong pull-down
  - Weak pull-up with weak pull-down
- Input threshold select (CMOS or LVTTL).
- Individual control of input and output buffer enabling/disabling in addition to the drive strength modes
- Selectable slew rates for dV/dt related noise control to improve EMI

The pins are organized in logical entities called ports, which are 8-bit in width (less for ports 5 and 6). During power-on and reset, the blocks are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix is used to multiplex between various signals that may connect to an I/O pin.

Data output and pin state registers store, respectively, the values to be driven on the pins and the states of the pins themselves. Every I/O pin can generate an interrupt if so enabled and each I/O port has an interrupt request (IRQ) and interrupt service routine (ISR) vector associated with it.

1.5 Special function peripherals

1.5.1 CAPSENSE™ sensing

CAPSENSE™ is supported in PSoC™ 4000T via the MSCLP CAPSENSE™ block. There is one MSCLP block in the PSoC™ 4000T which can be used to scan sense inputs autonomously (without CPU sequencing and intervention) in deep sleep and active modes. CAPSENSE™ function can thus be provided on a pin or group of pins in a system via autonomous scanning or via firmware control.

The PSoC™ 4000T MSCLP block provides the following improvements over previous generation capacitive sensing blocks:

- Improved SNR based on the all new ratio-metric analog architecture and advanced hardware filtering to enable modern sleek user interface solutions with superior liquid tolerance and provides robust and reliable touch HMI solution for harsh environments.
- Higher sensitivity to support smaller sensors, higher proximity detection range, and a much wider range of overlay thicknesses and materials.
- Ultra-low power operation through “Always-On” sensing which provides hardware-based sensor-data-processing for automatic touch detection in device Deep Sleep mode, to allow wake-on-touch operation.
- Autonomous, i.e. CPU independent, channel sequencing and scanning, for low power optimization.
- Improved shield drive method and support for wider range of shield electrode capacitances for superior liquid tolerance.
- Higher sensor capacitance range to support easier layout and wider variety of sensors.
- Improved EMI performance
- A driver is provided for the CAPSENSE™ block for easy usability.
- The CAPSENSE™ block provides multiple sensing methods such as mutual capacitance sensing, self-capacitance sensing, and inductive sensing.
- The MSCLP has two very low power scanning modes: Wake-on-Touch (WoT) and Active Low Refresh (ALR). WoT is an autonomous scanning mode.

2 Pinouts

Table 1 provides the pin list for PSoC™ 4000T for the 16-pin QFN, 24-pin QFN, and 25-pin WLCSP packages.

Table 1 PSoC™ 4000T pin list

16-QFN		24-QFN		25-CSP	
Pin	**Name**	**Pin**	**Name**	**Pin**	**Name**
9	P0.0	13	P0.0	D1	P0.0
10	P0.1	14	P0.1	C3	P0.1
		15	P0.2	C2	P0.2
		16	P0.3	C1	P0.3
11	P0.4	17	P0.4	B1	P0.4
				B2	P0.5
12	XRES	18	XRES	B3	XRES
13	VCCD	19	VCCD	A1	VCCD
14	VSSD	20	VSSD	A2	VSSD
15	VDDD	21	VDDD	A3	VDDD
16	VSSA	22	VSSA	A2	VSSD
		23	P1.0	A4	P1.0
		24	P2.0	B4	P2.0
		1	P2.1	A5	P2.1
1	P2.2	2	P2.2	B5	P2.2
2	P2.3	3	P2.3	C5	P2.3
3	P2.4	4	P2.4	C4	P2.4
4	P2.5	5	P2.5	D5	P2.5
		6	P3.0	E5	P3.0
				D4	P3.1
5	P3.2	7	P3.2	E4	P3.2
6	P3.3	8	P3.3	D3	P3.3
		9	P4.0	E3	P4.0
		10	P4.1	D2	P4.1
7	P4.2	11	P4.2	E2	P4.2
8	P4.3	12	P4.3	E1	P4.3

Descriptions of the power pins are as follows:

VDDD: Power supply for the digital section.

VSSD, VSSA: Ground pins for the digital and CAPSENSE™ sections respectively.

VCCD: Regulated digital supply (1.8 V ±5%)

GPIOs by package:

Number	25-WLCSP	24-QFN	16-QFN
GPIO	21	19	11

2.1 Alternate pin functions

Each port pin has multiple alternate functions. These are defined in **Table 2**. The columns ACT #x and DS #y denote active and deep sleep mode signals respectively.

The notation for a signal is of the form “IPName[x].signal_name[u]:y”, where:

IPName = Name of the block (such as tcpwm)

x = Unique instance of the IP.

Signal_name = Name of the signal.

u = Signal number where there is more than one signal for a particular signal name.

y = Designates copies of the signal name.

For example, the name “tcpwm[0].line_compl[3]:4” indicates that this is instance 0 of a TCPWM block, the signal is “line_compl # 3 (complement of the line output)”, and this is the fourth occurrence (copy) of the signal.

Signal copies are provided to allow flexibility in routing and to maximize use of on-chip resources.

Table 2 Pin alternate function table for PSoC™ 4000T

Name	MSCLP/IOSS	ACT #0	ACT #1	ACT #3	DS #0	DS #1	DS #2	DS #3
P0.0	csd.msc_gpio_ctrl_sns[0]			tcpwm.tr_in[0]	csd.msc_ddrv[0]	csd.ext_sync:0		scb[0].spi_select1:0
P0.1	csd.msc_gpio_ctrl_sns[1]			tcpwm.tr_in[1]	csd.msc_ddrv[1]	csd.ext_sync_clk:0		scb[0].spi_select2:0
P0.2	csd.msc_gpio_ctrl_sns[2]		scb[0].uart_rx:2		csd.msc_ddrv[2]	cpuss.swd_clk:1	scb[0].i2c_scl:2	scb[0].spi_mosi:0
P0.3	csd.msc_gpio_ctrl_sns[3]		scb[0].uart_tx:2		csd.msc_ddrv[3]	cpuss.swd_data:1	scb[0].i2c_sda:2	scb[0].spi_miso:0
P0.4	csd.msc_gpio_ctrl_sns[4]	srss.ext_clk	scb[0].uart_cts:2		csd.msc_ddrv[4]	csd.ext_frm_start:0		scb[0].spi_clk:0
P0.5	csd.msc_gpio_ctrl_sns[5]		scb[0].uart_rts:2		csd.msc_ddrv[5]			scb[0].spi_select0:0
P1.0	csd.msc_gpio_ctrl_sns[6]	tcpwm.line[1]:2		tcpwm.tr_in[2]	csd.msc_ddrv[6]			scb[0].spi_select3:0
P2.0	csd.msc_gpio_ctrl_sns[7]	tcpwm.line_-compl[1]:2		tcpwm.tr_in[3]	csd.msc_ddrv[7]	csd.obs_data[3]		
P2.1	csd.msc_gpio_ctrl_sns[8]				csd.msc_ddrv[8]	csd.obs_data[2]		
P2.2	csd.msc_gpio_ctrl_sns[9]	tcpwm.line[0]:1	scb[0].uart_rx:3	tcpwm.tr_in[4]	csd.msc_ddrv[9]	csd.obs_data[1]	scb[1].i2c_scl:1	scb[0].spi_mosi:3
P2.3	csd.msc_gpio_ctrl_sns[10]	tcpwm.line_-compl[0]:1	scb[0].uart_tx:3	tcpwm.tr_in[5]	csd.msc_ddrv[10]	csd.obs_data[0]	scb[1].i2c_sda:1	scb[0].spi_miso:3
P2.4	csd.msc_gpio_ctrl_sns[11]	tcpwm.line[1]:1	scb[0].uart_cts:3		csd.msc_ddrv[11]	csd.ext_sync:1		scb[0].spi_clk:3
P2.5	csd.msc_gpio_ctrl_sns[12]	tcpwm.line_-compl[1]:1	scb[0].uart_rts:3		csd.msc_ddrv[12]	csd.ext_sync_clk:1		scb[0].spi_select0:3
P3.0	csd.msc_gpio_ctrl_sns[13]	tcpwm.line[0]:0	scb[0].uart_rx:1		csd.msc_ddrv[13]	csd.ext_frm_start:1	scb[0].i2c_scl:1	scb[0].spi_mosi:1
P3.1	csd.msc_gpio_ctrl_sns[14]	tcpwm.line_-compl[0]:0	scb[0].uart_tx:1		csd.msc_ddrv[14]		scb[0].i2c_sda:1	scb[0].spi_miso:1
P3.2	csd.msc_gpio_ctrl_sns[15]	tcpwm.line[1]:0	scb[0].uart_cts:1		csd.msc_ddrv[15]	cpuss.swd_data:0	scb[1].i2c_sda:0	scb[0].spi_clk:1

Table 2 Pin alternate function table for PSoC™ 4000T *(continued)*

Name	MSCLP/IOSS	ACT #0	ACT #1	ACT #3	DS #0	DS #1	DS #2	DS #3
P3.3	csd.msc_gpio_ctrl_sns[16]	tcpwm.line_-compl[1]:0	scb[0].uart_rts:1		csd.msc_ddrv[16]	cpuss.swd_clk:0	scb[1].i2c_scl:0	scb[0].spi_select0:1
P4.0	csd.msc_gpio_ctrl_sns[17]		scb[0].uart_rx:0	tcpwm.tr_in[6]	csd.msc_ddrv[17]		scb[0].i2c_scl:0	scb[0].spi_mosi:2
P4.1	csd.msc_gpio_ctrl_sns[18]		scb[0].uart_tx:0		csd.msc_ddrv[18]		scb[0].i2c_sda:0	scb[0].spi_miso:2
P4.2	csd.msc_gpio_ctrl_cmod1		scb[0].uart_cts:0		csd.msc_c-mod1_ddrv			scb[0].spi_clk:2
P4.3	csd.msc_gpio_ctrl_cmod2		scb[0].uart_rts:0		csd.msc_c-mod2_ddrv			scb[0].spi_select0:2

3 Power

There are two distinct modes of operation. In mode 1, the supply voltage range is 2.0 V to 5.5 V (unregulated externally; internal regulator operational). In mode 2, the supply range is 1.8 V ±5% (externally regulated; 1.71 to 1.89, internal regulator enabled).

3.1 Mode 1: 2.0 V to 5.5 V external supply

In this mode, PSoC™ 4000T is powered by an external power supply that can be anywhere in the range of 2.0 to 5.5 V. This range is also designed for battery-powered operation. For example, the chip can be powered from a battery system that starts at 3.5 V and works down to 2.0 V. In this mode, the internal regulator of PSoC™ 4000T supplies the internal logic and its output is connected to the V_{CCD} pin. The V_{CCD} pin must be bypassed to ground via an external capacitor (2.2 µF; X5R ceramic or better) and must not be connected to anything else.

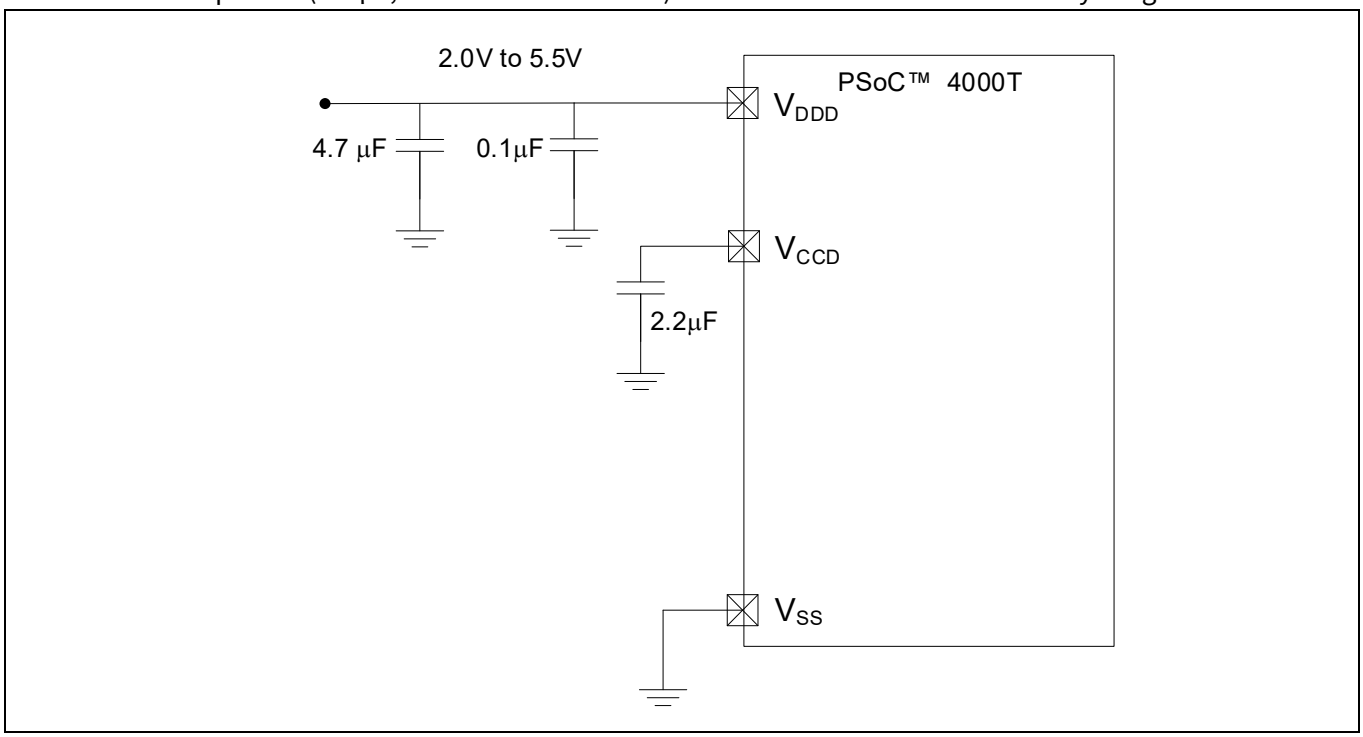


Figure 4 External supply range from 2.0 V to 5.5 V with internal regulator active

3.2 Mode 2: 1.8 V ±5% external supply

In this mode, PSoC™ 4000T is powered by an external power supply that must be within the range of 1.71 to 1.89 V; note that this range needs to include the power supply ripple too. In this mode, the V_{DDD} and V_{CCD} pins are shorted together and bypassed. The internal regulator must be kept enabled.

Bypass capacitors must be used from V_{DDD} to ground. The typical practice for systems in this frequency range is to use a capacitor as shown in **Figure 5**, in parallel with a smaller capacitor (0.1 µF, for example). Note that these are simply rules of thumb and that, for critical applications, the PCB layout, lead inductance, and the bypass capacitor parasitic should be simulated to design and obtain optimal bypassing.

Figure 5 shows an example of a bypass scheme.

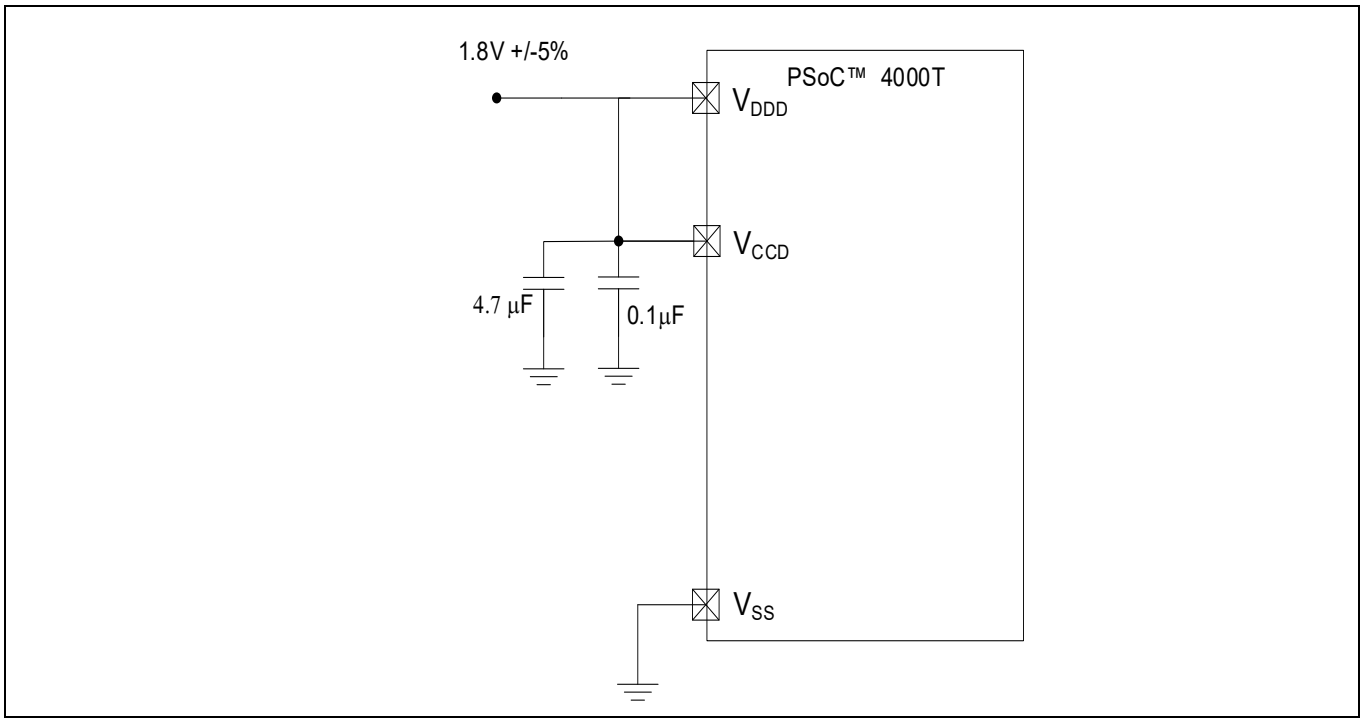


Figure 5 External supply range - 1.8V ±5%

4 Electrical specifications

4.1 Absolute maximum ratings

Table 3 Absolute maximum ratings

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID1	V_{DD_ABS}	Analog or digital supply relative to V_{SS} ($V_{SSD} = V_{SSA}$)	-0.5	-	6.0	V	Absolute maximum
SID2	V_{CCD_ABS}	Direct digital core voltage input relative to Vssd	-0.5	-	1.95	V	Absolute maximum
SID3	V_{GPIO_ABS}	GPIO voltage; V_{DDD} or V_{DDA}	-0.5	-	V_{DDD}+ 0.5	V	Absolute maximum
SID4	I_{GPIO_ABS}	Current per GPIO	-25	-	25	mA	Absolute maximum
SID5	$I_{GPIO\_injection}$	GPIO injection current per pin	-0.5	-	0.5	mA	Absolute maximum
BID44	ESD_HBM	Electrostatic discharge voltage	2200			V	Human Body Model ESD
BID45	ESD_CDM	Electrostatic discharge voltage	500			V	Charged Device Model ESD
BID46	I_LU	Latch-up current limits	-100		100	mA	Max/min current into any input or output, pin-to-pin, pin-to-supply at 125° C ambient

4.2 Device-level specifications

Table 4 DC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID53	V_{DDD}	Power supply Input Voltage	2.0		5.5	V	With internal regulator enabled
SID255	V_{DDD}	Power supply Input Voltage	1.71	1.8	1.89	V	Internal regulator enabled; VCCD connected to VDDD
SID54	V_{CCD}	Output voltage (for core logic)	–	1.8	–	V	With internal regulator enabled
SID55	C_{EFC}	External regulator voltage bypass	–	2.2	–	µF	X5R ceramic or better
SID56	C_{EXC}	Power supply decoupling capacitor (+/-30% max)	–	4.7	–	µF	X5R ceramic or better
Active mode, V_{DDD} = 1.71V to 5.5 V							
SID10	I_{DD5}	Execute from flash; CPU at 6 MHz	–	1.8	2.7	mA	Typ = 25°C @ V_{DDD} = 3.3 V. Max = 85°C @ 5.5 V.
SID16	I_{DD11}	Execute from flash; CPU at 24 MHz	–	3	4.8	mA	Typ = 25°C @ V_{DDD}= 3.3 V. Max = 85°C @ 5.5 V.
SID19	I_{DD14}	Execute from flash; CPU at 48 MHz	–	5.4	6.9	mA	Typ = 25°C @ V_{DDD}= 3.3V. Max = 85°C @ 5.5 V.
Sleep mode, V_{DDD} = 2.0 to 5.5 V (Regulator on)							
SID22	I_{DD17}	I^2C wakeup, WDT, and comparators on. 6 MHz.	–	1.7	2.2	mA	Typ = 25°C @ V_{DDD} = 3.3 V. Max = 85°C @ 5.5 V.
SID25	I_{DD20}	I^2C wakeup, WDT, and comparators on. 12 MHz.	–	2.2	2.5	mA	Typ = 25°C @ V_{DDD} = 3.3 V. Max = 85°C @ 5.5 V.

Table 4 DC specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
Sleep mode, V_{DDD} = 1.71 to 1.89 V							
SID28	I_{DD23}	I^2C wakeup, WDT, and comparators on. 6 MHz.	–	1.7	2.2	mA	Typ = 25°C @ V_{DDD} = 1.8 V. Max = 85°C @ 1.89 V.
SID28A	I_{DD23A}	I^2C wakeup, WDT, and comparators on. 12 MHz.	–	2.2	2.5	mA	Typ = 25°C @ V_{DDD} = 1.8 V. Max = 85°C @ 1.89 V.
Deep sleep mode, V_{DDD} = 2.0 to 3.6 V							
SID31	I_{DD26}	I^2C wakeup and WDT on.	–	2.5	60	µA	Typ = 25°C @ V_{DDD} = 3.3 V. Max = 85°C @ 3.6 V.
SID31A	I_{DD26A}	I^2C wakeup and WDT on.	–	2.5	18	µA	Typ = 25°C @ V_{DDD} = 3.3 V. Max = 55°C @ 3.6 V
Deep sleep mode, V_{DDD} = 3.6 to 5.5 V							
SID34	I_{DD29}	I^2C wakeup and WDT on.	–	2.5	60	µA	Typ = 25°C @ V_{DDD}= 3.3 V. Max = 85°C @ 5.5 V.
SID34A	I_{DD29A}	I^2C wakeup and WDT on.	–	2.5	19	µA	Typ = 25°C @ V_{DDD}= 3.3 V. Max = 55°C @ V_{DDD} = 5.5 V.
Deep sleep mode, V_{DDD} = 1.71 to 1.89 V							
SID37	I_{DD32}	I^2C wakeup and WDT on.	–	2.5	65	µA	Typ = 25°C @ VDDD = 1.8V. Max = 85°C @ 1.89 V
SID37A	I_{DD32A}	I^2C wakeup and WDT on.	–	2.5	16	µA	Typ = 25°C @ VDDD = 1.8V. Max = 55°C @ 1.89 V.
XRES current							
SID307	I_{DD_XR}	Supply current while XRES asserted	–	2.0	5	mA	–

Table 5 AC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID48	F_{CPU}	CPU frequency	DC	–	48	MHz	$1.71 \le V_{DDD} \le 5.5$
SID49	T_{SLEEP}	Wakeup from sleep mode	–	0	–	µs	–
SID50	$T_{DEEPSLEEP}$	Wakeup from deep sleep mode	–	TBD	–	µs	–

4.2.1 GPIO

Table 6 GPIO DC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID57	V_{IH}	Input voltage high threshold	0.7 × V_{DDD}	–	–	V	CMOS input
SID58	V_{IL}	Input voltage low threshold	–	–	0.3 × V_{DDD}	V	CMOS input
SID241	V_{IH}	LVTTL input, V_{DDD} < 2.7V	0.7 × V_{DDD}	–	–	V	–
SID242	V_{IL}	LVTTL input, V_{DDD} < 2.7V	–	–	0.3 × V_{DDD}	V	–
SID243	V_{IH}	LVTTL input, $V_{DDD} \geq$ 2.7V	2.0	–	–	V	–
SID244	V_{IL}	LVTTL input, $V_{DDD} \geq$ 2.7V	–	–	0.8	V	–
SID59	V_{OH}	Output voltage high level	V_{DDD} –0.6	–	–	V	I_{OH} = 4 mA at 3 V V_{DDD}
SID60	V_{OH}	Output voltage high level	V_{DDD} –0.5	–	–	V	I_{OH} = 1 mA at 1.8 V V_{DDD}
SID61	V_{OL}	Output voltage low level	–	–	0.6	V	I_{OL} = 4 mA at 1.8 V V_{DDD}
SID62	V_{OL}	Output voltage low level	–	–	0.6	V	I_{OL} = 10 mA at 3 V V_{DDD}
SID62A	V_{OL}	Output voltage low level	–	–	0.4	V	I_{OL} = 3 mA at 3 V V_{DDD}
SID63	R_{PULLUP}	Pull-up resistor	3.5	5.6	8.5	kΩ	–
SID64	$R_{PULLDOWN}$	Pull-down resistor	3.5	5.6	8.5	kΩ	–
SID65	I_{IL}	Input leakage current (absolute value)	–	–	2	nA	25°C, V_{DDD} = 3.0 V
SID65A	I_{IL_CTBM}	Input leakage on CTBm input pins	–	–	4	nA	–
SID66	C_{IN}	Input capacitance	–	–	7	pF	–
SID67	V_{HYSTTL}	Input hysteresis LVTTL $V_{DDD} \geq$ 2.7V	25	40	–	mV	–
SID68	$V_{HYSCMOS}$	Input hysteresis CMOS	0.05× V_{DDD}	–	–	mV	–
SID69	I_{DIODE}	Current through protection diode to V_{DDD}/V_{SS}	–	–	100	µA	–
SID69A	I_{TOT_GPIO}	Maximum total source or sink chip current	–	–	200	mA	–

Table 7 GPIO AC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID70	T_{RISEF}	Rise time in fast strong mode	2	–	12	ns	3.3 V V_{DDD}, Cload = 25 pF
SID71	T_{FALLF}	Fall time in fast strong mode	2	–	12	ns	3.3 V V_{DDD}, Cload = 25 pF
SID72	T_{RISES}	Rise time in slow strong mode	10	–	60	ns	3.3 V V_{DDD}, Cload = 25 pF
SID73	T_{FALLS}	Fall time in slow strong mode	10	–	60	ns	3.3 V V_{DDD}, Cload = 25 pF
SID74	$F_{GPIOUT1}$	GPIO F_{OUT}; 3.3 V ≤ V_{DDD} ≤ 5.5 V Fast strong mode	–	–	33	MHz	90/10%, 25-pF load, 60/40 duty cycle
SID75	$F_{GPIOUT2}$	GPIO F_{OUT}; 1.71 V ≤ V_{DDD} ≤ 3.3 V Fast strong mode	–	–	16.7	MHz	90/10%, 25-pF load, 60/40 duty cycle
SID76	$F_{GPIOUT3}$	GPIO F_{OUT}; 3.3 V ≤ V_{DDD} ≤ 5.5 V Slow strong mode	–	–	7	MHz	90/10%, 25-pF load, 60/40 duty cycle
SID245	$F_{GPIOUT4}$	GPIO F_{OUT}; 1.71 V ≤ V_{DDD} ≤ 3.3 V Slow strong mode.	–	–	3.5	MHz	90/10%, 25-pF load, 60/40 duty cycle
SID246	F_{GPIOIN}	GPIO input operating frequency; 1.71 V ≤ V_{DDD} ≤ 5.5 V	–	–	48	MHz	90/10% V_{IO}

4.2.2 XRES

Table 8 XRES DC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID77	V_{IH}	Input voltage high threshold	0.7 × V_{DDD}	–	–	V	CMOS input
SID78	V_{IL}	Input voltage low threshold	–	–	0.3 × V_{DDD}	V	CMOS input
SID79	R_{PULLUP}	Pull-up resistor	–	60	–	kΩ	–
SID80	C_{IN}	Input capacitance	–	–	7	pF	–
SID81	$V_{HYSXRES}$	Input voltage hysteresis	–	100	–	mV	–
SID82	I_{DIODE}	Current through protection diode to V_{DDD}/V_{SS}	–	–	100	µA	–

Table 9 XRES AC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID83	$T_{RESETWIDTH}$	Reset pulse width	1	–	–	µs	–
BID194	$T_{RESETWAKE}$	Wake-up time from reset release	–	–	2.7	ms	–

4.2.3 CAPSENSE™ block

Table 10 MSCLP CAPSENSE™ specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SIDMSC_2	$V_{DD\_RIPPLE\_1.8}$	Max allowed ripple on power supply, 1kHz to 10MHz	–	–	±25	mV	V_{DDD} ≥ 1.75 V (with ripple), 25 °C TA, Sensitivity ≥ 50 counts/0.1 pF, 2 pF < Cs < 50 pF
SIDMSC_2B	F_{MOD}	Modulator frequency	–	–	46	MHz	All V_{DDD}
SIDMSC_2C	$F_{MSCLP\_IMO\_TOL}$	MSCLP clock frequency variation at 25, 38, and 46 MHz	–2	–	+2.5	%	All V_{DDD}
SIDMSC_5	V_{MSC_LP}	Voltage range of operation	1.71	–	5.5	V	1.8 V ±5% Externally regulated, 2V to 5.5 V Externally unregulated
SIDMSC_6	SNR	Ratio of counts of finger to noise. Guaranteed by characterization	5	–	–	Ratio	Capacitance range of 5 to 50 pF, Sensitivity ≥ 50 counts/0.1 pF. VDDA ≥ 2 V.
SIDMSC_7	CMOD	External modulator capacitor.	–	2.2	–	nF	5-V rating, X7R or NP0 cap.
SIDMSC_x8	$F_{CAPSENSE}$	Capacitive sense freq. range	45		6000	kHz	
SIDMSC_9	Noise Floor (CNS)	System Noise Floor	–	0.1	–	fF-rms	With 8 pF input capacitance
SIDMSC_10	CIN_Self	Input capacitance Range for Self Capacitance	2	–	200	pF	
SIDMSC_10A	CIN_Mutual	Input capacitance Range for Mutual Capacitance	0.5	–	30	pF	
SIDMSC_11	MSC_WOT	Average current. Wake On Touch mode. 16 Hz refresh rate		6		µA	52-pF sensor value, 0.2 pF sensitivity, 1.8 V.
SIDMSC_12	MSC_ALR	Average current. Active Low Refresh mode. 32 Hz refresh rate.		50		µA	13 sensors, 4 pF each, 0.1pf sensitivity, 1.8 V.
SIDMSC_13	MSC_ACT	Average current. CAPSENSE™ active scan mode. 128 Hz refresh rate.		200		µA	13 sensors, 4 pF each, 0.1pf sensitivity, 1.8 V.
SIDMSC_12A	MSC_ALR4	Average current. Active Low Refresh mode. 32 Hz refresh rate.		30		µA	4 sensors, 4 pF each, 0.1 pF sensitivity, 1.8 V.
SIDMSC_13A	MSC_ACT4	Average current. CAPSENSE™ active scan mode. 128 Hz refresh rate.		110		µA	4 sensors, 4 pF each, 0.1 pF sensitivity, 1.8 V.
SIDMSC_14	$I_{DD\_MSC\_SCAN\_46}$	Sub-system current in CAPSENSE™ active scan mode at 46 MHz		2.5		mA	V_{DDD} = 1.8 V
SIDMSC_15	$I_{DD\_MSC\_SCAN\_38}$	Subsystem current in CAPSENSE™ active scan mode at 38 MHz		2		mA	V_{DDD} = 1.8 V

Table 10 MSCLP CAPSENSE™ specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SIDMSC_16	$I_{DD\_MSC\_SCAN\_25}$	Subsystem current in CAPSENSE™ active scan mode at 25 MHz		1.5		mA	V_{DDD} = 1.8 V
SIDMSC_18	$I_{DD\_MSC\_SBY\_46}$	Subsystem current in Standby mode at 46 MHz (CAPSENSE™ block enabled and ready to begin frame)	–	1.5	–	mA	V_{DDD} = 1.8 V
SIDMSC_19	$I_{DD\_MSC\_SBY\_38}$	Subsystem current in Standby mode at 38 MHz (CAPSENSE™ block enabled and ready to begin frame)	–	1.25	–	mA	V_{DDD} = 1.8 V
SIDMSC_20	$I_{DD\_MSC\_SBY\_25}$	Subsystem current in Standby mode at 25 MHz (CAPSENSE™ block enabled and ready to begin frame)	–	1	–	mA	V_{DDD} = 1.8 V

4.3 Digital peripherals

4.3.1 Timer counter pulse-width modulator (TCPWM)

Table 11 TCPWM specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.TCPWM.1	ITCPWM1	Block current consumption at 3 MHz	–	–	45	µA	All modes (Timer/counter/PWM)
SID.TCPWM.2	ITCPWM2	Block current consumption at 12 MHz	–	–	155	µA	All modes (Timer/counter/PWM)
SID.TCPWM.2A	ITCPWM3	Block current consumption at 48 MHz	–	–	650	µA	All modes (Timer/counter/PWM)
SID.TCPWM.3	$TCPWM_{FREQ}$	Operating frequency	–	–	Fc	MHz	Fc max = Fcpu. Maximum = 48 MHz
SID.TCPWM.4	$TPWM_{ENEXT}$	Input trigger pulse width	2/Fc	–	–	ns	For all trigger events
SID.TCPWM.5	$TPWM_{EXT}$	Output trigger pulse widths	2/Fc	–	–	ns	Minimum possible width of overflow, underflow, and CC (counter equals compare value) trigger outputs
SID.TCPWM.5A	TC_{RES}	Resolution of counter	1/Fc	–	–	ns	Minimum time between successive counts
SID.TCPWM.5B	PWM_{RES}	PWM resolution	1/Fc	–	–	ns	Minimum pulse width of PWM output
SID.TCPWM.5C	Q_{RES}	Quadrature inputs resolution	1/Fc	–	–	ns	Minimum pulse width between quadrature phase inputs

4.3.2 I²C

Table 12 I²C DC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID149	I_{I2C1}	Block current consumption at 100 kHz	–	–	50	µA	–
SID150	I_{I2C2}	Block current consumption at 400 kHz	–	–	135	µA	–
SID151	I_{I2C3}	Block current consumption at 1-Mbps	–	–	310	µA	–
SID152	I_{I2C4}	Block current in deep sleep mode	–	1	–	µA	–

Table 13 I²C AC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID153	F_{I2C1}	Bit rate	–	–	1	Mbps	HS I²C slave mode

4.3.3 UART

Table 14 UART DC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID160	I_{UART1}	Block current consumption at 100 Kbps	–	–	55	µA	–
SID161	I_{UART2}	Block current consumption at 1000 Kbps	–	–	312	µA	–

Table 15 UART AC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID162	F_{UART}	Bit rate	–	–	1	Mbps	–

4.3.4 SPI

Table 16 SPI DC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID163	ISPI1	Block current consumption at 1-Mbps	–	–	360	µA	–
SID164	ISPI2	Block current consumption at 4-Mbps	–	–	560	µA	–
SID165	ISPI3	Block current consumption at 8-Mbps	–	–	600	µA	–

Table 17 SPI AC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID166	FSPI	SPI operating frequency (Master; 6x oversampling)	–	–	8	MHz	–
SPI master mode AC specifications							

Table 17 SPI AC specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID167	TDMO	MOSI valid after sclock driving edge	–	–	15	ns	–
SID168	TDSI	MISO Valid before sclock capturing edge	20	–	–	ns	Full clock, late MISO sampling
SID169	THMO	Previous MOSI data hold time	0	–	–	ns	Referred to Slave capturing edge
SPI slave mode AC specifications							
SID170	TDMI	MOSI valid before sclock capturing edge	40	–	–	ns	–
SID171	TDSO	MISO valid after sclock driving edge	–	–	42 + 3*Tcpu	ns	$T_{CPU} = 1/F_{CPU}$
SID171A	TDSO_EXT	MISO valid after sclock driving edge in Ext. Clk mode	–	–	48	ns	–
SID172	THSO	Previous MISO data hold time	0	–	–	ns	–
SID172A	TSSELSSCK	SSEL valid to first SCK valid edge	100	–	–	ns	–

4.4 Memory

Table 18 Flash DC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID173	V_{PE}	Erase and program voltage	1.71	–	5.5	V	–
SID173A	I_{PW}	Page write current at 16 MHz	–	–	3.5	mA	5.5 V V_{DDD}

Table 19 Flash AC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID174	$T_{ROWWRITE}$	Row (block) write time (erase and program)	–	–	20	ms	Row (block) = 256 bytes
SID175	$T_{ROWERASE}$	Row erase time	–	–	16	ms	–
SID176	$T_{ROWPROGRAM}$	Row program time after erase	–	–	4	ms	–
SID178	$T_{BULKERASE}$	Bulk erase time (32 KB)	–	–	35	ms	–
SID180	$T_{DEVPROG}$	Total device program time	–	–	7	Seconds	–
SID181	F_{END}	Flash endurance	100K	–	–	Cycles	–
SID182	F_{RET}	Flash retention. $T_A \leq 55$ °C, 100 K P/E cycles	20	–	–	Years	–
SID182A	–	Flash retention. $T_A \leq 85$ °C, 10K P/E cycles	10	–	–	Years	–
SID256	TWS48	Number of wait states at 48 MHz	2	–	–		CPU execution from Flash
SID257	TWS24	Number of wait states at 24 MHz	1	–	–		CPU execution from Flash

4.5 System resources

4.5.1 Power-on reset (POR)

Table 20 Power-on reset (PRES)

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.CLK#6	SR_POW-ER_UP	Power supply slew rate	1	–	67	V/ms	At power-up
SID185	$V_{RISEIPOR}$	Rising trip voltage	0.80	–	1.45	V	–
SID186	$V_{FALLIPOR}$	Falling trip voltage	0.70	–	1.4	V	–

Table 21 Brown-out detect (BOD) for V_{CCD}

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID190	$V_{FALLPPOR}$	BOD trip voltage in active and sleep modes	1.48	–	1.62	V	–
SID192	$V_{FALLDPSLP}$	BOD trip voltage in deep sleep	1.11	–	1.5	V	–

4.5.2 SWD interface

Table 22 SWD interface specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID213	F_SWDCLK1	3.3 V ≤ V_{DDD} ≤ 5.5 V	–	–	14	MHz	SWDCLK ≤ 1/3 FCPU
SID214	F_SWDCLK2	1.71 V ≤ V_{DDD} ≤ 3.3 V	–	–	7	MHz	SWDCLK ≤ 1/3 FCPU
SID215	T_SWDI_-SETUP	T = 1/f SWDCLK	0.25*T	–	–	ns	–
SID216	T_SWDI_HOLD	T = 1/f SWDCLK	0.25*T	–	–	ns	–
SID217	T_SWDO_VALID	T = 1/f SWDCLK	–	–	0.5*T	ns	–
SID217A	T_SWDO_HOLD	T = 1/f SWDCLK	1	–	–	ns	–

4.5.3 Internal main oscillator

Table 23 IMO DC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID218	I_{IMO1}	IMO operating current at 48 MHz	–	–	250	µA	–
SID219	I_{IMO2}	IMO operating current at 24 MHz	–	–	180	µA	–

Table 24 IMO AC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID223	$F_{IMOTOL1}$	Frequency variation at 24, 32, and 48 MHz (trimmed)	–	–	±2	%	–
SID226	$T_{STARTIMO}$	IMO startup time	–	–	7	µs	–
SID228	$T_{JITRMSIMO2}$	RMS jitter at 24 MHz	–	145	–	ps	–

4.5.4 Internal low-speed oscillator

Table 25 ILO DC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID231	I_{ILO2}	ILO operating current at 32 KHz	–	0.3	1.05	µA	–

Table 26 ILO AC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID234	$T_{STARTILO1}$	ILO startup time	–	–	2	ms	–
SID236	$T_{ILODUTY}$	ILO duty cycle	40	50	60	%	–
SID237	$F_{ILOTRIM1}$	ILO frequency range	20	40	80	kHz	–

5 Ordering information

The marketing part numbers for the PSoC™ 4000T devices are listed in the following table.

Table 27 PSoC™ 4000T ordering information

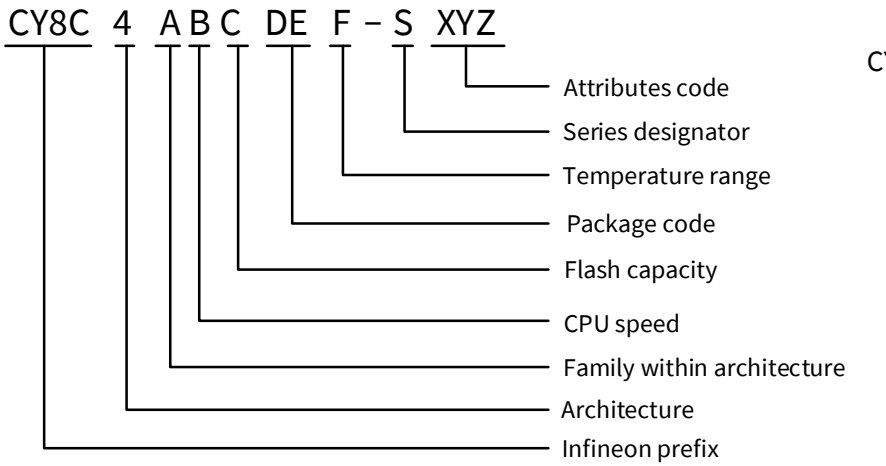
Category	Product	Features								Packages			Temp range (°C)
		Max CPU Speed (MHz)	Flash (KB)	SRAM (KB)	CAPSENSE™	Inductive	TCPWM blocks	SCB blocks	GPIO	24-QFN	16-QFN	25-WLCSP	
40x5	CY8C4025LQI-T412	24	32	4	1		2	2	19	X			-40 to 85
	CY8C4025LQI-T411	24	32	4	1		2	2	11		X		-40 to 85
	CY8C4025FNI-T412T	24	32	4	1		2	2	21			X	-40 to 85
	CY8C4045LQI-T412	48	32	4	1		2	2	19	X			-40 to 85
	CY8C4045LQI-T411	48	32	4	1		2	2	11		X		-40 to 85
	CY8C4045FNI-T412T	48	32	4	1		2	2	21			X	-40 to 85
40x6	CY8C4026LQI-T412	24	64	8	1		2	2	19	X			-40 to 85
	CY8C4026LQI-T411	24	64	8	1		2	2	11		X		-40 to 85
	CY8C4026FNI-T412T	24	64	8	1		2	2	21			X	-40 to 85
	CY8C4046LQI-T412	48	64	8	1		2	2	19	X			-40 to 85
	CY8C4046LQI-T411	48	64	8	1		2	2	11		X		-40 to 85
	CY8C4046FNI-T412T	48	64	8	1		2	2	21			X	-40 to 85
	CY8C4046LQI-T452	48	64	8	1	1	2	2	19	X			-40 to 85
	CY8C4046LQI-T451	48	64	8	1	1	2	2	11		X		-40 to 85
	CY8C4046FNI-T452T	48	64	8	1	1	2	2	21			X	-40 to 85

Ordering information

The nomenclature used in the preceding table is based on the following part numbering convention:

Field	Description	Values	Meaning
CY8C	Infineon prefix	-	-
4	Architecture	4	PSoC™ 4
A	Family	0	PSoC™ 4000 family
		1	PSoC™ 4100 family
		2	PSoC™ 4200 family
B	CPU speed	2	24 MHz
		4	48 MHz
C	Flash capacity	4	16 KB
		5	32 KB
		6	64 KB
		7	128 KB
		8	256 KB
		9	384 KB
DE	Package code	AX	TQFP (0.8-mm pitch)
		AZ	TQFP (0.5-mm pitch)
		LQ	QFN
		PV	SSOP
		FN	CSP
F	Temperature range	I	Industrial
		Q	Extended industrial
S	Series designator	S	PSoC™ 4 S-series
		M	PSoC™ 4 M-series
		L	PSoC™ 4 L-series
		BL	PSoC™ 4 Bluetooth® LE-series
		T	PSoC™ 4 T series
XYZ	Attributes code	000-999	Code of feature set in the specific family

The following is an example of a part number:



Example:
CY8C4025LQI-T412

CY8C: Infineon prefix
4: PSoC™ 4 MCU
0: 4000 family
2: 24 MHz
5: 32 KB
LQ: QFN
I: Industrial
T: 4000T series
412: Feature set

6 Packaging

The PSoC™ 4000T is offered in 25-WLCSP, 24-QFN, and 16-QFN packages.

Table 28 provides the package dimensions and Infineon drawing numbers.

Table 28 Package list

Spec ID#	Package	Description	Package diagram
BID20	25-pin WLCSP	0.35mm pitch	002-34703
BID27	24-pin QFN	4 × 4 × 0.6 mm height with 0.5-mm pitch	002-16934
BID34A	16-pin QFN	3 X 3 X 0.6 mm height with 0.5-mm pitch	001-09116

Table 29 Package thermal characteristics

Parameter	Description	Package	Min	Typ	Max	Unit
T_A	Operating ambient temperature	–	–40	25	85	°C
T_J	Operating junction temperature	–	–40	25	105	°C
T_{JA}	Package θ_{JA}	WLCSP 25 (0.35mm pitch)	–	TBD	–	°C/Watt
T_{JC}	Package θ_{JC}	WLCSP 25 (0.35mm pitch)	–	TBD	–	°C/Watt
T_{JA}	Package θ_{JA}	QFN 24 (0.5mm pitch)	–	TBD	–	°C/Watt
T_{JC}	Package θ_{JC}	QFN 24 (0.5mm pitch)	–	TBD	–	°C/Watt
T_{JA}	Package θ_{JA}	QFN 16	–	TBD	–	°C/Watt
T_{JC}	Package θ_{JC}	QFN 16	–	TBD	–	°C/Watt

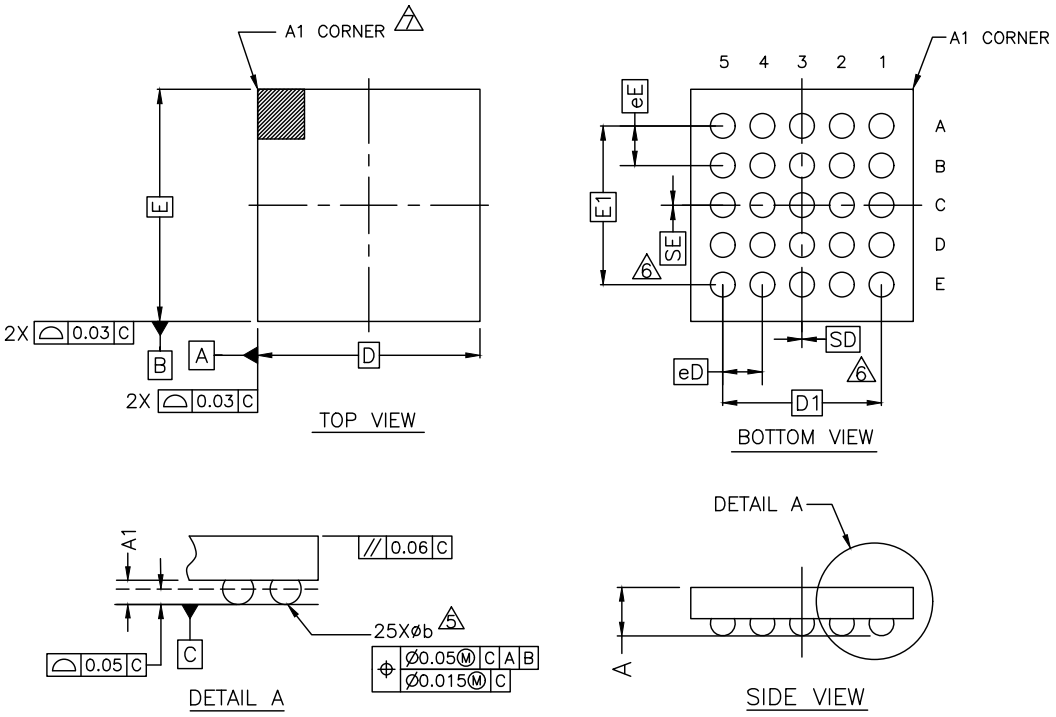
Table 30 Solder reflow peak temperature

Package	Maximum peak temperature	Maximum time at peak temperature
All	260°C	30 seconds

Table 31 Package moisture sensitivity level (MSL), IPC/JEDEC J-STD-020

Package	MSL
All	MSL 3

6.1 Package diagrams



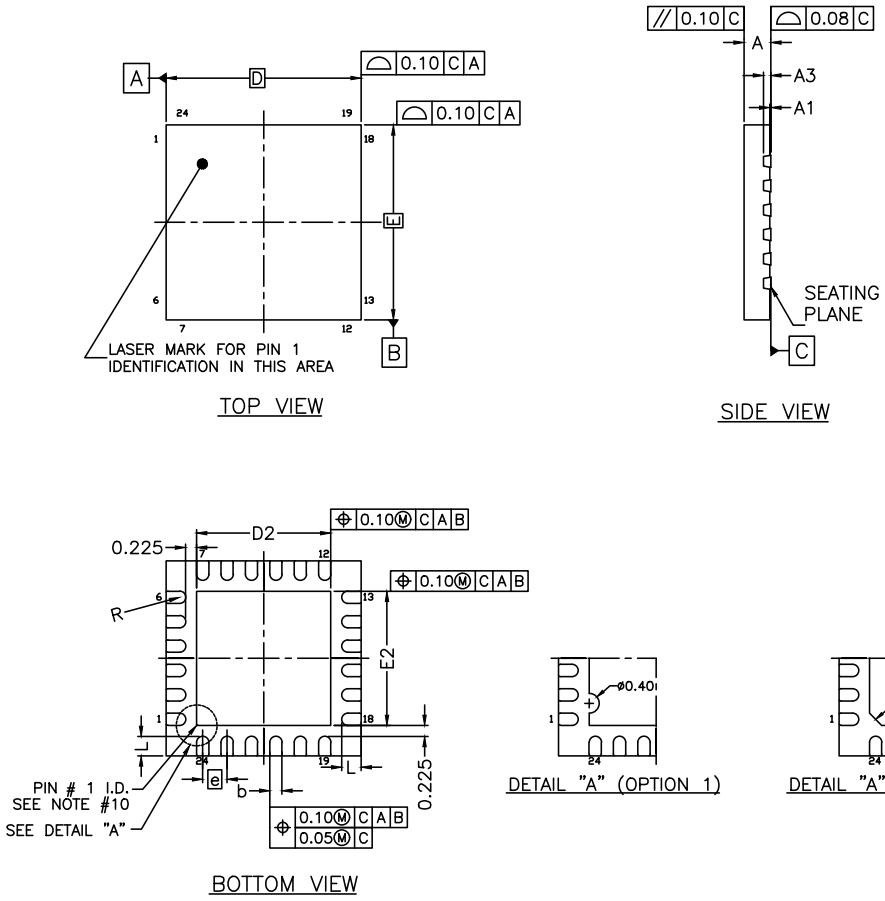
SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	0.467
A1	0.122	-	-
D	1.961 BSC		
E	2.046 BSC		
D1	1.40 BSC		
E1	1.40 BSC		
MD	5		
ME	5		
N	25		
Øb	0.188	0.218	0.248
eD	0.35 BSC		
eE	0.35 BSC		
SD/SE	0.00 BSC		

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. SOLDER BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
3. "e" REPRESENTS THE SOLDER BALL GRID PITCH.
4. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
5. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
6. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
7. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALIZED MARK, INDENTATION OR OTHER MEANS.
8. JEDEC SPECIFICATION NO. REF. : N/A.

002-34703 **

Figure 6 25-ball WLCSP (1.961 × 2.046 × 0.467mm)



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	0.60
A1	0.00	—	0.05
A3 (Option 1)	0.152 REF		
A3 (Option 2)	0.127 REF		
b	0.18	0.25	0.30
D	4.00 BSC		
D2	2.65	2.75	2.85
E	4.00 BSC		
E2	2.65	2.75	2.85
L	0.30	0.40	0.50
e	0.50 BSC		
R	0.09	—	—

NOTES
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIE THICKNESS ALLOWABLE IS 0.305 mm MAXIMUM(.012 INCHES MAXIMUM)
3. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. -1994.
4. THE PIN #1 IDENTIFIER MUST BE PLACED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
5. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
6. PACKAGE WARPAGE MAX 0.08 mm.
7. APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
8. APPLIED ONLY TO TERMINALS.
9. JEDEC SPECIFICATION NO. REF: N.A.
10. INDEX FEATURE CAN EITHER BE AN OPTION 1 : "MOUSE BITE" OR OPTION 2 : CHAMFER.

002-16934 *E

Figure 7 24-pin QFN ((4 × 4 × 0.60mm) 2.75 × 2.75 E-pad (sawn)) package outline, PG-VQFN-24

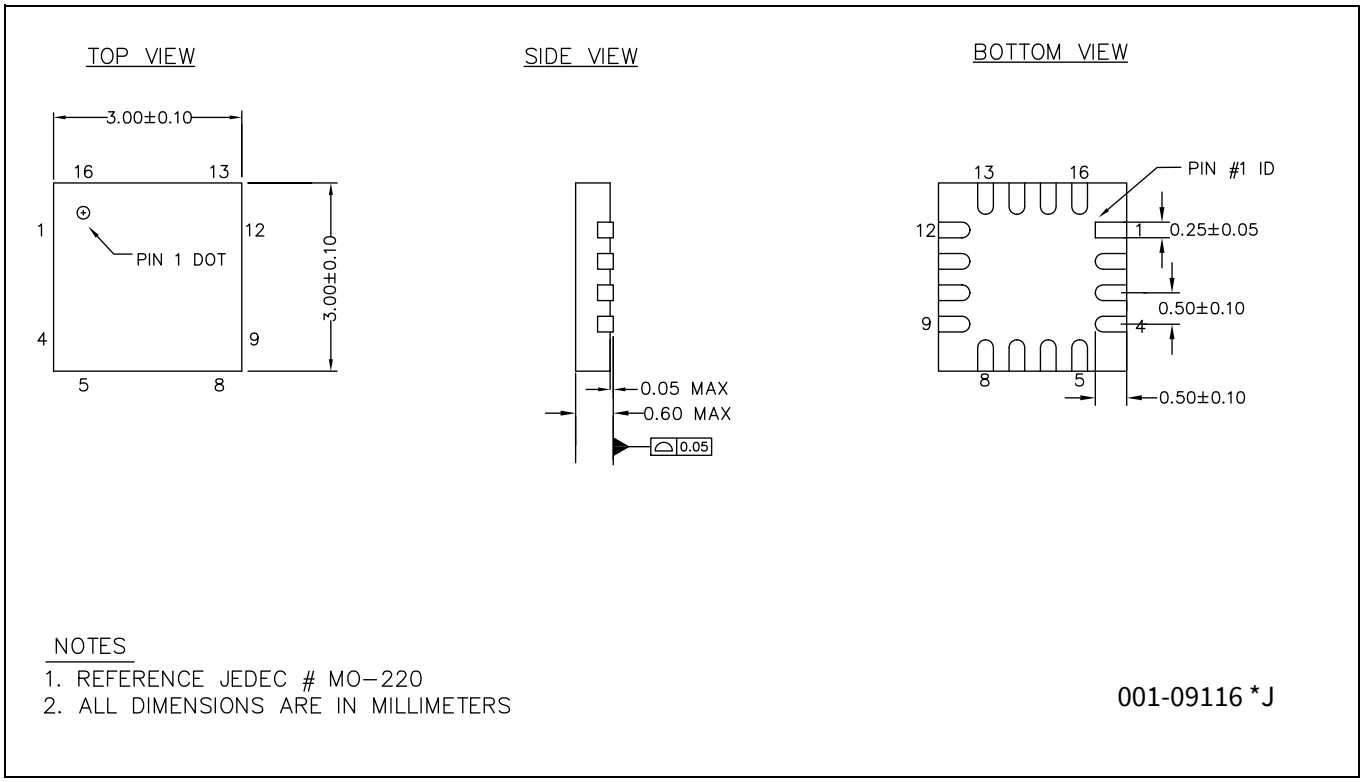
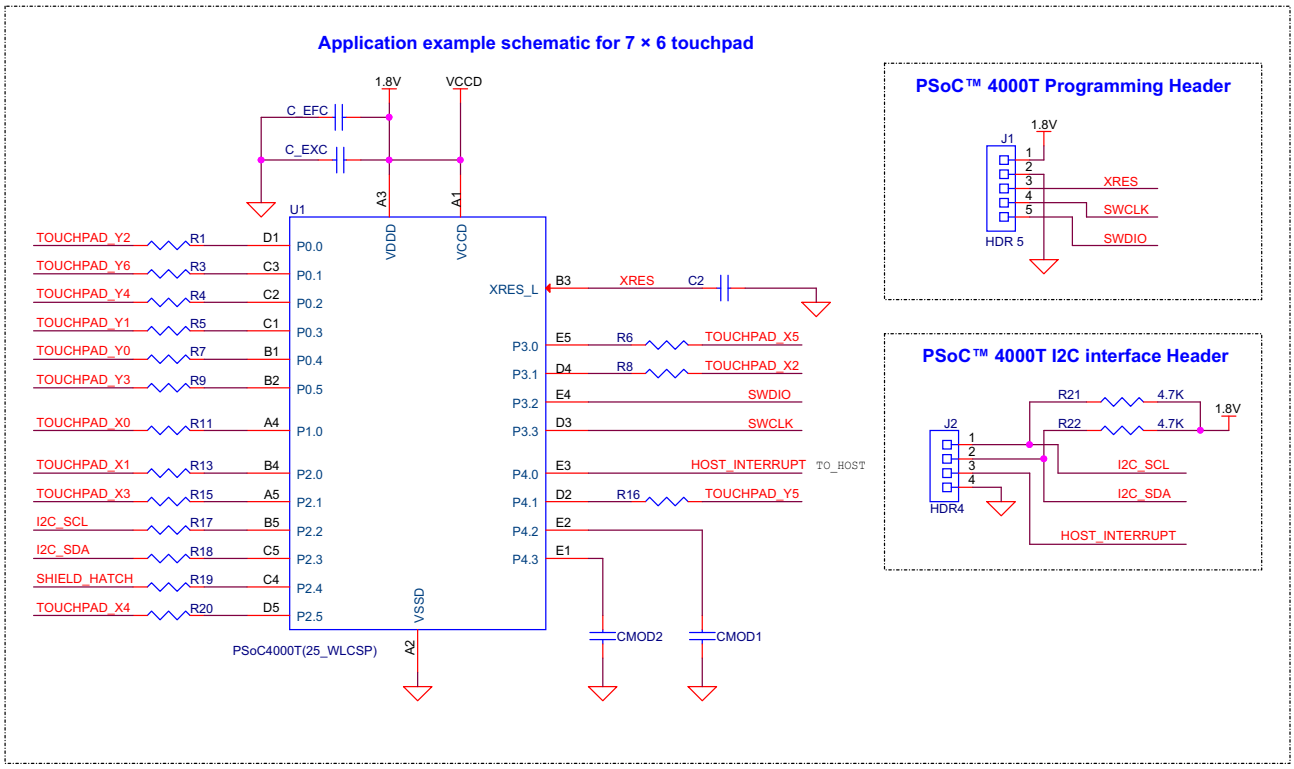


Figure 8 16-pin QFN (3 × 3 × 0.6 mm, sawn), PG-USON-16

7 Application example schematic for 7 × 6 touchpad



This is a reference schematic, which you can modify based on your application needs and must conform to this datasheet, application note **AN88619** (PSoC™ 4 MCU hardware design considerations), and the "sensor pin selection" and other schematic guidelines provided in **AN85951** (PSoC™ 4 and PSoC™ 6 CAPSENSE™ Design Guide).

Series resistors on sensor and shield lines are recommended to be 560 ohm but can be altered. Refer to **AN85951** for more details on "Series resistors on CAPSENSE™ pins".

For CMOD1 and CMOD2, use the value indicated in the electrical specifications for CMOD in this datasheet.

8 Acronyms

Table 32 Acronyms used in this document

Acronym	Description
abus	analog local bus
ADC	analog-to-digital converter
AG	analog global
AHB	AMBA (advanced microcontroller bus architecture) high-performance bus, an Arm® data transfer bus
ALU	arithmetic logic unit
AMUXBUS	analog multiplexer bus
API	application programming interface
APSR	application program status register
Arm®	advanced RISC machine, a CPU architecture
ATM	automatic thump mode
BW	bandwidth
CAN	controller area network, a communications protocol
CMRR	common-mode rejection ratio
CPU	central processing unit
CRC	cyclic redundancy check, an error-checking protocol
DAC	digital-to-analog converter, see also IDAC, VDAC
DFB	digital filter block
DIO	digital input/output, GPIO with only digital capabilities, no analog. See GPIO.
DMIPS	Dhrystone million instructions per second
DMA	direct memory access, see also TD
DNL	differential nonlinearity, see also INL
DNU	do not use
DR	port write data registers
DSI	digital system interconnect
DWT	data watchpoint and trace
ECC	error correcting code
ECO	external crystal oscillator
EEPROM	electrically erasable programmable read-only memory
EMI	electromagnetic interference
EMIF	external memory interface
EOC	end of conversion
EOF	end of frame
EPSR	execution program status register
ESD	electrostatic discharge
ETM	embedded trace macrocell
FIR	finite impulse response, see also IIR
FPB	flash patch and breakpoint

Table 32 Acronyms used in this document *(continued)*

Acronym	Description
FS	full-speed
GPIO	general-purpose input/output, applies to a PSoC™ pin
HVI	high-voltage interrupt, see also LVI, LVD
IC	integrated circuit
IDAC	current DAC, see also DAC, VDAC
IDE	integrated development environment
I^2C, or IIC	Inter-Integrated Circuit, a communications protocol
IIR	infinite impulse response, see also FIR
ILO	internal low-speed oscillator, see also IMO
IMO	internal main oscillator, see also ILO
INL	integral nonlinearity, see also DNL
I/O	input/output, see also GPIO, DIO, SIO, USBIO
IPOR	initial power-on reset
IPSR	interrupt program status register
IRQ	interrupt request
ITM	instrumentation trace macrocell
LCD	liquid crystal display
LIN	local interconnect network, a communications protocol.
LR	link register
LUT	lookup table
LVD	low-voltage detect, see also LVI
LVI	low-voltage interrupt, see also HVI
LVTTL	low-voltage transistor-transistor logic
MAC	multiply-accumulate
MCU	microcontroller unit
MISO	master-in slave-out
NC	no connect
NMI	nonmaskable interrupt
NRZ	non-return-to-zero
NVIC	nested vectored interrupt controller
NVL	nonvolatile latch, see also WOL
opamp	operational amplifier
PAL	programmable array logic, see also PLD
PC	program counter
PCB	printed circuit board
PGA	programmable gain amplifier
PHUB	peripheral hub
PHY	physical layer
PICU	port interrupt control unit
PLA	programmable logic array

Table 32 Acronyms used in this document *(continued)*

Acronym	Description
PLD	programmable logic device, see also PAL
PLL	phase-locked loop
PMDD	package material declaration data sheet
POR	power-on reset
PRES	precise power-on reset
PRS	pseudo random sequence
PS	port read data register
PSRR	power supply rejection ratio
PWM	pulse-width modulator
RAM	random-access memory
RISC	reduced-instruction-set computing
RMS	root-mean-square
RTC	real-time clock
RTL	register transfer language
RTR	remote transmission request
RX	receive
SAR	successive approximation register
SC/CT	switched capacitor/continuous time
SCL	I^2C serial clock
SDA	I^2C serial data
S/H	sample and hold
SINAD	signal to noise and distortion ratio
SIO	special input/output, GPIO with advanced features. See GPIO.
SOC	start of conversion
SOF	start of frame
SPI	Serial Peripheral Interface, a communications protocol
SR	slew rate
SRAM	static random access memory
SRES	software reset
SWD	serial wire debug, a test protocol
SWV	single-wire viewer
TD	transaction descriptor, see also DMA
THD	total harmonic distortion
TIA	transimpedance amplifier
TRM	technical reference manual
TTL	transistor-transistor logic
TX	transmit
UART	Universal Asynchronous Transmitter Receiver, a communications protocol
UDB	universal digital block
USB	Universal Serial Bus

Table 32 Acronyms used in this document *(continued)*

Acronym	Description
USBIO	USB input/output, PSoC™ pins used to connect to a USB port
VDAC	voltage DAC, see also DAC, IDAC
WDT	watchdog timer
WOL	write once latch, see also NVL
WRES	watchdog timer reset
XRES	external reset I/O pin
XTAL	crystal

9 Document conventions

9.1 Units of measure

Table 33 Units of measure

Symbol	Unit of measure
°C	degrees celsius
dB	decibel
fF	femto farad
Hz	hertz
KB	1024 bytes
kbps	kilobits per second
Khr	kilohour
kHz	kilohertz
kΩ	kilo ohm
ksps	kilosamples per second
LSB	least significant bit
Mbps	megabits per second
MHz	megahertz
MΩ	mega-ohm
Msps	megasamples per second
µA	microampere
µF	microfarad
µH	microhenry
µs	microsecond
µV	microvolt
µW	microwatt
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
nV	nanovolt
Ω	ohm
pF	picofarad
ppm	parts per million
ps	picosecond
s	second
sps	samples per second
sqrtHz	square root of hertz
V	volt

Revision history

Document revision	Date	Description of changes
**	2021-10-13	Initial release
*A	2022-01-20	Updated min value of SID53. Added specs SIDMSC_14 through SIDMSC_21. Removed SID151H.
*B	2022-06-17	Replaced Multi-sense Converter with Multi-Sense Converter Low Power. Updated document links in **Development ecosystem**. Updated **CAPSENSE™ sensing**. Updated **Pinouts**. Updated power diagrams. Added **Application example schematic for 7 × 6 touchpad**. Added **Ordering information** and updated **Packaging**. Added **Revision history**.
*C	2023-03-01	Updated **Power**. Updated **DC specifications**. Updated **MSCLP CAPSENSE™ specifications**. Updated **Application example schematic for 7 × 6 touchpad**. Removed Errata.
*D	2023-03-07	Changed VDD references to VDDD. Updated description for SID53 and SID255.
*E	2023-08-04	Updated the WLCSP bootloader section in **Development ecosystem**. Updated **CAPSENSE™ sensing**. Updated **DC specifications**. Updated **MSCLP CAPSENSE™ specifications**. Updated **Ordering information**.
*F	2023-08-11	Updated conditions for specs SID28, SID28A, SID31A, SID37, and SID37A.
*G	2023-08-29	Updated device name in **Block diagram**. Updated **MSCLP CAPSENSE™ specifications**. Changed datasheet status to Final.
*H	2023-12-12	Updated the web page links. Updated the part number nomenclature table and diagram.

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