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PSoC 4100S Max

PSoC 4 Registers Technical Reference Manual (TRM)

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Register Mapping

The Register Mapping section discusses the PSoC® 4100S Max PSoC 4 registers and lists all the registers in mapping tables, in address order. The PSoC 4 device requires peripheral register accesses to match the hardware register size. Otherwise, the peripheral might ignore the transfer and Hard Fault exception will be generated. It is recommended to use the APIs provided by the core library for accessing the registers.

For Architecture details, refer to PSoC 4100S Max PSoC 4 Architecture Technical Reference Manual (TRM).

Register General Conventions

The register conventions specific to this section and the Register Reference chapter are listed in this table.

Convention	Example	Description
'x' in a register name	ACBxxCR1	Multiple instances/address ranges of the same register
R	R : 00	Read register or bit(s)
W	W : 00	Write register or bit(s)
WOC	WOC:0	Write one to clear
WZC	WZC:0	Write zero to clear
RC	RC:0	Read to clear
WC	WC:0	Write to clear
NA	NA:000	Reserved
U	R:U	Undefined
00	RW : 00	Reset value is 0x00
XX	RW : XX	Register is not reset

Acronyms

This table lists the acronyms used in this document.

Symbol	Unit of Measure
ABUS	analog output bus
AC	alternating current
ADC	analog-to-digital converter
AHB	AMBA (advanced microcontroller bus architecture) high-performance bus, an ARM data transfer bus
API	application programming interface
APOR	analog power-on reset
BC	broadcast clock
BOM	bill of materials
BR	bit rate
BRA	bus request acknowledge
BRQ	bus request
CAN	controller area network
CI	carry in

Symbol	Unit of Measure
CMP	compare
CO	carry out
CPU	central processing unit
CRC	cyclic redundancy check
CSD	CapSense sigma delta
CT	continuous time
DAC	digital-to-analog converter
DC	direct current
DI	digital or data input
DMA	direct memory access
DNL	differential nonlinearity
DO	digital or data output
DSI	digital signal interface
DSM	deep-sleep mode
ECO	external crystal oscillator
EEPROM	electrically erasable programmable read only memory
EMIF	external memory interface
FB	feedback
FIFO	first in first out
FSR	full scale range
GPIO	general purpose I/O
HCI	host-controller interface
HFCLK	high-frequency clock
I^2C	inter-integrated circuit
IDE	integrated development environment
ILO	internal low-speed oscillator
IMO	internal main oscillator
INL	integral nonlinearity
I/O	input/output
IOR	I/O read
IOW	I/O write
IRES	initial power on reset
IRA	interrupt request acknowledge
IRQ	interrupt request
ISR	interrupt service routine
IVR	interrupt vector read
L2CAP	logical link control and adaptation protocol
LRb	last received bit
LRB	last received byte
LSb	least significant bit
LSB	least significant byte
LUT	lookup table
MISO	master-in-slave-out
MMIO	memory mapped input/output
MOSI	master-out-slave-in
MSb	most significant bit
MSB	most significant byte
PC	program counter
PCH	program counter high

Symbol	Unit of Measure
PCL	program counter low
PD	power down
PGA	programmable gain amplifier
PM	power management
PMA	PSoC memory arbiter
POR	power-on reset
PPOR	precision power-on reset
PRS	pseudo random sequence
PSoC®	Programmable System-on-Chip
PSRR	power supply rejection ratio
PSSDC	power system sleep duty cycle
PWM	pulse width modulator
RAM	random-access memory
RETI	return from interrupt
RF	radio frequency
ROM	read only memory
RW	read/write
SAR	successive approximation register
SC	switched capacitor
SCB	serial communication block
SIE	serial interface engine
SIO	special I/O
SE0	single-ended zero
SNR	signal-to-noise ratio
SOF	start of frame
SOI	start of instruction
SP	stack pointer
SPD	sequential phase detector
SPI	serial peripheral interconnect
SPIM	serial peripheral interconnect master
SPIS	serial peripheral interconnect slave
SRAM	static random-access memory
SROM	supervisory read only memory
SSADC	single slope ADC
SSC	supervisory system call
SYSCLK	system clock
SWD	single wire debug
TC	terminal count
TD	transaction descriptors
UART	universal asynchronous receiver/transmitter
UDB	universal digital block
USB	universal serial bus
USBIO	USB I/O
WCO	watch crystal oscillator
WDT	watchdog timer
WDR	watchdog reset
XRES	external reset
XRES_N	external reset, active low

1 Supervisory Flash Registers

This section discusses the Supervisory Flash (SFLASH) registers. It lists all the registers in mapping tables, in address order.

1.1 Register Details

Register	Address	Description
SFLASH_SILICON_ID	0x0FFFE244	Silicon ID
SFLASH_HIB_KEY_DELAY	0x0FFFE250	Hibernate wakeup value for PWR_KEY_DELAY
SFLASH_DPSLP_KEY_DELAY	0x0FFFE252	DeepSleep wakeup value for PWR_KEY_DELAY
SFLASH_SWD_CONFIG	0x0FFFE254	SWD pinout selector (not present in TSG4/TSG5-M)
SFLASH_INITIAL_SPCIF_TRIM_M2_DAC0	0x0FFFE256	FLASH IDAC trim used during boot
SFLASH_SWD_LISTEN	0x0FFFE258	Listen Window Length
SFLASH_FLASH_START	0x0FFFE25C	Flash Image Start Address
SFLASH_SAR_TEMP_MULTIPLIER	0x0FFFE264	SAR Temperature Sensor Multiplication Factor
SFLASH_SAR_TEMP_OFFSET	0x0FFFE266	SAR Temperature Sensor Offset
SFLASH_IMO_TRIM_USBMODE_24	0x0FFFE33E	USB IMO TRIM 24MHz
SFLASH_IMO_TRIM_USBMODE_48	0x0FFFE33F	USB IMO TRIM 48MHz
SFLASH_IMO_TCTRIM_LT0	0x0FFFE34C	IMO TempCo Trim Register (SRSS-Lite)
SFLASH_IMO_TCTRIM_LT1	0x0FFFE34D	IMO TempCo Trim Register (SRSS-Lite). See SFLASH_IMO_TCTRIM_LT0 for the details of bit fields.
SFLASH_IMO_TCTRIM_LT2	0x0FFFE34E	IMO TempCo Trim Register (SRSS-Lite). See SFLASH_IMO_TCTRIM_LT0 for the details of bit fields.
SFLASH_IMO_TCTRIM_LT3	0x0FFFE34F	IMO TempCo Trim Register (SRSS-Lite). See SFLASH_IMO_TCTRIM_LT0 for the details of bit fields.
SFLASH_IMO_TCTRIM_LT4	0x0FFFE350	IMO TempCo Trim Register (SRSS-Lite). See SFLASH_IMO_TCTRIM_LT0 for the details of bit fields.
SFLASH_IMO_TCTRIM_LT5	0x0FFFE351	IMO TempCo Trim Register (SRSS-Lite). See SFLASH_IMO_TCTRIM_LT0 for the details of bit fields.
SFLASH_IMO_TCTRIM_LT6	0x0FFFE352	IMO TempCo Trim Register (SRSS-Lite). See SFLASH_IMO_TCTRIM_LT0 for the details of bit fields.
SFLASH_IMO_TCTRIM_LT7	0x0FFFE353	IMO TempCo Trim Register (SRSS-Lite). See SFLASH_IMO_TCTRIM_LT0 for the details of bit fields.
SFLASH_IMO_TCTRIM_LT8	0x0FFFE354	IMO TempCo Trim Register (SRSS-Lite). See SFLASH_IMO_TCTRIM_LT0 for the details of bit fields.
SFLASH_IMO_TCTRIM_LT9	0x0FFFE355	IMO TempCo Trim Register (SRSS-Lite). See SFLASH_IMO_TCTRIM_LT0 for the details of bit fields.
SFLASH_IMO_TCTRIM_LT10	0x0FFFE356	IMO TempCo Trim Register (SRSS-Lite). See SFLASH_IMO_TCTRIM_LT0 for the details of bit fields.
SFLASH_IMO_TCTRIM_LT11	0x0FFFE357	IMO TempCo Trim Register (SRSS-Lite). See SFLASH_IMO_TCTRIM_LT0 for the details of bit fields.
SFLASH_IMO_TCTRIM_LT12	0x0FFFE358	IMO TempCo Trim Register (SRSS-Lite). See SFLASH_IMO_TCTRIM_LT0 for the details of bit fields.

Register	Address	Description
SFLASH_IMO_TCTRIM_LT13	0x0FFFE359	IMO TempCo Trim Register (SRSS-Lite). See SFLASH_IMO_TCTRIM_LT0 for the details of bit fields.
SFLASH_IMO_TCTRIM_LT14	0x0FFFE35A	IMO TempCo Trim Register (SRSS-Lite). See SFLASH_IMO_TCTRIM_LT0 for the details of bit fields.
SFLASH_IMO_TCTRIM_LT15	0x0FFFE35B	IMO TempCo Trim Register (SRSS-Lite). See SFLASH_IMO_TCTRIM_LT0 for the details of bit fields.
SFLASH_IMO_TCTRIM_LT16	0x0FFFE35C	IMO TempCo Trim Register (SRSS-Lite). See SFLASH_IMO_TCTRIM_LT0 for the details of bit fields.
SFLASH_IMO_TCTRIM_LT17	0x0FFFE35D	IMO TempCo Trim Register (SRSS-Lite). See SFLASH_IMO_TCTRIM_LT0 for the details of bit fields.
SFLASH_IMO_TCTRIM_LT18	0x0FFFE35E	IMO TempCo Trim Register (SRSS-Lite). See SFLASH_IMO_TCTRIM_LT0 for the details of bit fields.
SFLASH_IMO_TCTRIM_LT19	0x0FFFE35F	IMO TempCo Trim Register (SRSS-Lite). See SFLASH_IMO_TCTRIM_LT0 for the details of bit fields.
SFLASH_IMO_TCTRIM_LT20	0x0FFFE360	IMO TempCo Trim Register (SRSS-Lite). See SFLASH_IMO_TCTRIM_LT0 for the details of bit fields.
SFLASH_IMO_TCTRIM_LT21	0x0FFFE361	IMO TempCo Trim Register (SRSS-Lite). See SFLASH_IMO_TCTRIM_LT0 for the details of bit fields.
SFLASH_IMO_TCTRIM_LT22	0x0FFFE362	IMO TempCo Trim Register (SRSS-Lite). See SFLASH_IMO_TCTRIM_LT0 for the details of bit fields.
SFLASH_IMO_TCTRIM_LT23	0x0FFFE363	IMO TempCo Trim Register (SRSS-Lite). See SFLASH_IMO_TCTRIM_LT0 for the details of bit fields.
SFLASH_IMO_TCTRIM_LT24	0x0FFFE364	IMO TempCo Trim Register (SRSS-Lite). See SFLASH_IMO_TCTRIM_LT0 for the details of bit fields.
SFLASH_IMO_TRIM_LT0	0x0FFFE365	IMO Frequency Trim Register (SRSS-Lite)
SFLASH_IMO_TRIM_LT1	0x0FFFE366	IMO Frequency Trim Register (SRSS-Lite). See SFLASH_IMO_TRIM_LT0 for the details of bit fields.
SFLASH_IMO_TRIM_LT2	0x0FFFE367	IMO Frequency Trim Register (SRSS-Lite). See SFLASH_IMO_TRIM_LT0 for the details of bit fields.
SFLASH_IMO_TRIM_LT3	0x0FFFE368	IMO Frequency Trim Register (SRSS-Lite). See SFLASH_IMO_TRIM_LT0 for the details of bit fields.
SFLASH_IMO_TRIM_LT4	0x0FFFE369	IMO Frequency Trim Register (SRSS-Lite). See SFLASH_IMO_TRIM_LT0 for the details of bit fields.
SFLASH_IMO_TRIM_LT5	0x0FFFE36A	IMO Frequency Trim Register (SRSS-Lite). See SFLASH_IMO_TRIM_LT0 for the details of bit fields.
SFLASH_IMO_TRIM_LT6	0x0FFFE36B	IMO Frequency Trim Register (SRSS-Lite). See SFLASH_IMO_TRIM_LT0 for the details of bit fields.
SFLASH_IMO_TRIM_LT7	0x0FFFE36C	IMO Frequency Trim Register (SRSS-Lite). See SFLASH_IMO_TRIM_LT0 for the details of bit fields.
SFLASH_IMO_TRIM_LT8	0x0FFFE36D	IMO Frequency Trim Register (SRSS-Lite). See SFLASH_IMO_TRIM_LT0 for the details of bit fields.
SFLASH_IMO_TRIM_LT9	0x0FFFE36E	IMO Frequency Trim Register (SRSS-Lite). See SFLASH_IMO_TRIM_LT0 for the details of bit fields.
SFLASH_IMO_TRIM_LT10	0x0FFFE36F	IMO Frequency Trim Register (SRSS-Lite). See SFLASH_IMO_TRIM_LT0 for the details of bit fields.
SFLASH_IMO_TRIM_LT11	0x0FFFE370	IMO Frequency Trim Register (SRSS-Lite). See SFLASH_IMO_TRIM_LT0 for the details of bit fields.
SFLASH_IMO_TRIM_LT12	0x0FFFE371	IMO Frequency Trim Register (SRSS-Lite). See SFLASH_IMO_TRIM_LT0 for the details of bit fields.
SFLASH_IMO_TRIM_LT13	0x0FFFE372	IMO Frequency Trim Register (SRSS-Lite). See SFLASH_IMO_TRIM_LT0 for the details of bit fields.
SFLASH_IMO_TRIM_LT14	0x0FFFE373	IMO Frequency Trim Register (SRSS-Lite). See SFLASH_IMO_TRIM_LT0 for the details of bit fields.
SFLASH_IMO_TRIM_LT15	0x0FFFE374	IMO Frequency Trim Register (SRSS-Lite). See SFLASH_IMO_TRIM_LT0 for the details of bit fields.
SFLASH_IMO_TRIM_LT16	0x0FFFE375	IMO Frequency Trim Register (SRSS-Lite). See SFLASH_IMO_TRIM_LT0 for the details of bit fields.
SFLASH_IMO_TRIM_LT17	0x0FFFE376	IMO Frequency Trim Register (SRSS-Lite). See SFLASH_IMO_TRIM_LT0 for the details of bit fields.
SFLASH_IMO_TRIM_LT18	0x0FFFE377	IMO Frequency Trim Register (SRSS-Lite). See SFLASH_IMO_TRIM_LT0 for the details of bit fields.
SFLASH_IMO_TRIM_LT19	0x0FFFE378	IMO Frequency Trim Register (SRSS-Lite). See SFLASH_IMO_TRIM_LT0 for the details of bit fields.
SFLASH_IMO_TRIM_LT20	0x0FFFE379	IMO Frequency Trim Register (SRSS-Lite). See SFLASH_IMO_TRIM_LT0 for the details of bit fields.

Register	Address	Description
SFLASH_IMO_TRIM_LT21	0x0FFFE37A	IMO Frequency Trim Register (SRSS-Lite). See SFLASH_IMO_TRIM_LT0 for the details of bit fields.
SFLASH_IMO_TRIM_LT22	0x0FFFE37B	IMO Frequency Trim Register (SRSS-Lite). See SFLASH_IMO_TRIM_LT0 for the details of bit fields.
SFLASH_IMO_TRIM_LT23	0x0FFFE37C	IMO Frequency Trim Register (SRSS-Lite). See SFLASH_IMO_TRIM_LT0 for the details of bit fields.
SFLASH_IMO_TRIM_LT24	0x0FFFE37D	IMO Frequency Trim Register (SRSS-Lite). See SFLASH_IMO_TRIM_LT0 for the details of bit fields.

1.1.1 SFLASH_SILICON_ID

Silicon ID

Address: 0x0FFFE244

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	ID [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	ID	Silicon ID Default Value: X

1.1.2 SFLASH_HIB_KEY_DELAY

Hibernate wakeup value for PWR_KEY_DELAY

Address: 0x0FFFE250

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	WAKEUP_HOLDOFF [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						WAKEUP_HOLDOFF [9:8]	

Bits	Name	Description
9 : 0	WAKEUP_HOLDOFF	Delay (in 12MHz IMO clock cycles) to wait for references to settle on wakeup from hibernate/ deepsleep. PBOD is ignored and system does not resume until this delay expires. Note that the same delay on POR is hard-coded. Default Value: X

1.1.3 SFLASH_DPSLP_KEY_DELAY

DeepSleep wakeup value for PWR_KEY_DELAY

Address: 0x0FFFE252

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	WAKEUP_HOLDOFF [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						WAKEUP_HOLDOFF [9:8]	

Bits	Name	Description
9 : 0	WAKEUP_HOLDOFF	Delay (in 12MHz IMO clock cycles) to wait for references to settle on wakeup from hibernate/ deepsleep. PBOD is ignored and system does not resume until this delay expires. Note that the same delay on POR is hard-coded. Default Value: X

1.1.4 SFLASH_SWD_CONFIG

SWD pinout selector (not present in TSG4/TSG5-M)

Address: 0x0FFFE254

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							
Name	None [7:1]							SWD_SE-LECT

Bits	Name	Description
0	SWD_SELECT	0: Use Primary SWD location 1: Use Alternate SWD location Default Value: X

1.1.5 SFLASH_INITIAL_SPCIF_TRIM_M2_DAC0

FLASH IDAC trim used during boot

Address: 0x0FFFE256

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW			RW				
HW Access	R			R				
Name	SLOPE [7:5]			IDAC [4:0]				

Bits	Name	Description
7 : 5	SLOPE	See SPCIF_TRIM1 Default Value: 0
4 : 0	IDAC	See SPCIF_TRIM1 Default Value: 0

1.1.6 SFLASH_SWD_LISTEN

Listen Window Length

Address: 0x0FFFE258

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	CYCLES [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	CYCLES [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	CYCLES [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	CYCLES [31:24]							

Bits	Name	Description
31 : 0	CYCLES	Number of clock cycles Default Value: X

1.1.7 SFLASH_FLASH_START

Flash Image Start Address

Address: 0x0FFFE25C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	ADDRESS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	ADDRESS [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	ADDRESS [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	ADDRESS [31:24]							

Bits	Name	Description
31 : 0	ADDRESS	Start Address Default Value: X

1.1.8 SFLASH_SAR_TEMP_MULTIPLIER

SAR Temperature Sensor Multiplication Factor

Address: 0x0FFFE264

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	TEMP_MULTIPLIER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	TEMP_MULTIPLIER [15:8]							

Bits	Name	Description
15 : 0	TEMP_MULTIPLIER	Multiplier value for SAR temperature sensor in fixed point 0.16 format. Note: this field exists in products that contain SAR (m0s8sar) only. Default Value: X

1.1.9 SFLASH_SAR_TEMP_OFFSET

SAR Temperature Sensor Offset

Address: 0x0FFFE266

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	TEMP_OFFSET [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	TEMP_OFFSET [15:8]							

Bits	Name	Description
15 : 0	TEMP_OFFSET	Offset value for SAR temperature sensor in fixed point 10.6 format. Note: this field exists in products that contain SAR (m0s8sar) only. Default Value: X

1.1.10 SFLASH_IMO_TRIM_USBMODE_24

USB IMO TRIM 24MHz

Address: 0x0FFFE33E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	TRIM_24 [7:0]							

Bits	Name	Description
7 : 0	TRIM_24	TRIM value for IMO with USB at 24MHz Default Value: X

1.1.11 SFLASH_IMO_TRIM_USBMODE_48

USB IMO TRIM 48MHz

Address: 0x0FFFE33F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	TRIM_24 [7:0]							

Bits	Name	Description
7 : 0	TRIM_24	TRIM value for IMO with USB at 24MHz Default Value: X

1.1.12 SFLASH_IMO_TCTRIM_LT0

IMO TempCo Trim Register (SRSS-Lite)

Address: 0x0FFFE34C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW		RW				
HW Access	None	R		R				
Name	None	TCTRIM [6:5]		STEPSIZE [4:0]				

Bits	Name	Description
6 : 5	TCTRIM	IMO temperature compesation trim. These bits are determined at manufacturing time to adjust for temperature dependence. This bits are dependent on frequency and need to be changed using the Cypress provided frequency change algorithm. Default Value: 2
4 : 0	STEPSIZE	IMO trim stepsize bits. These bits are determined at manufacturing time to adjust for process variation. They are used to tune the stepsize of the FSOFFSET and OFFSET trims. Default Value: 16

1.1.13 SFLASH_IMO_TRIM_LT0

IMO Frequency Trim Register (SRSS-Lite)

Address: 0x0FFFE365

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	OFFSET [7:0]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default Value: X

2 Peripheral Registers

This section discusses the Peripheral registers. It lists all the registers in mapping tables, in address order.

2.1 Register Details

Register	Address	Description
PERI_DIV_CMD	0x40010000	Divider command register
PERI_PCLK_CTL0	0x40010100	Programmable clock control register
PERI_PCLK_CTL1	0x40010104	Programmable clock control register. See PERI_PCLK_CTL0 for the details of bit fields.
PERI_PCLK_CTL2	0x40010108	Programmable clock control register. See PERI_PCLK_CTL0 for the details of bit fields.
PERI_PCLK_CTL3	0x4001010C	Programmable clock control register. See PERI_PCLK_CTL0 for the details of bit fields.
PERI_PCLK_CTL4	0x40010110	Programmable clock control register. See PERI_PCLK_CTL0 for the details of bit fields.
PERI_PCLK_CTL5	0x40010114	Programmable clock control register. See PERI_PCLK_CTL0 for the details of bit fields.
PERI_PCLK_CTL6	0x40010118	Programmable clock control register. See PERI_PCLK_CTL0 for the details of bit fields.
PERI_PCLK_CTL7	0x4001011C	Programmable clock control register. See PERI_PCLK_CTL0 for the details of bit fields.
PERI_PCLK_CTL8	0x40010120	Programmable clock control register. See PERI_PCLK_CTL0 for the details of bit fields.
PERI_PCLK_CTL9	0x40010124	Programmable clock control register. See PERI_PCLK_CTL0 for the details of bit fields.
PERI_PCLK_CTL10	0x40010128	Programmable clock control register. See PERI_PCLK_CTL0 for the details of bit fields.
PERI_PCLK_CTL11	0x4001012C	Programmable clock control register. See PERI_PCLK_CTL0 for the details of bit fields.
PERI_PCLK_CTL12	0x40010130	Programmable clock control register. See PERI_PCLK_CTL0 for the details of bit fields.
PERI_PCLK_CTL13	0x40010134	Programmable clock control register. See PERI_PCLK_CTL0 for the details of bit fields.
PERI_PCLK_CTL14	0x40010138	Programmable clock control register. See PERI_PCLK_CTL0 for the details of bit fields.
PERI_PCLK_CTL15	0x4001013C	Programmable clock control register. See PERI_PCLK_CTL0 for the details of bit fields.
PERI_PCLK_CTL16	0x40010140	Programmable clock control register. See PERI_PCLK_CTL0 for the details of bit fields.
PERI_PCLK_CTL17	0x40010144	Programmable clock control register. See PERI_PCLK_CTL0 for the details of bit fields.
PERI_PCLK_CTL18	0x40010148	Programmable clock control register. See PERI_PCLK_CTL0 for the details of bit fields.
PERI_PCLK_CTL19	0x4001014C	Programmable clock control register. See PERI_PCLK_CTL0 for the details of bit fields.
PERI_PCLK_CTL20	0x40010150	Programmable clock control register. See PERI_PCLK_CTL0 for the details of bit fields.
PERI_PCLK_CTL21	0x40010154	Programmable clock control register. See PERI_PCLK_CTL0 for the details of bit fields.
PERI_PCLK_CTL22	0x40010158	Programmable clock control register. See PERI_PCLK_CTL0 for the details of bit fields.
PERI_PCLK_CTL23	0x4001015C	Programmable clock control register. See PERI_PCLK_CTL0 for the details of bit fields.
PERI_DIV_16_CTL0	0x40010300	Divider control register (for 16.0 divider)
PERI_DIV_16_CTL1	0x40010304	Divider control register (for 16.0 divider). See PERI_DIV_16_CTL0 for the details of bit fields.

Register	Address	Description
PERI_DIV_16_CTL2	0x40010308	Divider control register (for 16.0 divider). See PERI_DIV_16_CTL0 for the details of bit fields.
PERI_DIV_16_CTL3	0x4001030C	Divider control register (for 16.0 divider). See PERI_DIV_16_CTL0 for the details of bit fields.
PERI_DIV_16_CTL4	0x40010310	Divider control register (for 16.0 divider). See PERI_DIV_16_CTL0 for the details of bit fields.
PERI_DIV_16_CTL5	0x40010314	Divider control register (for 16.0 divider). See PERI_DIV_16_CTL0 for the details of bit fields.
PERI_DIV_16_CTL6	0x40010318	Divider control register (for 16.0 divider). See PERI_DIV_16_CTL0 for the details of bit fields.
PERI_DIV_16_CTL7	0x4001031C	Divider control register (for 16.0 divider). See PERI_DIV_16_CTL0 for the details of bit fields.
PERI_DIV_16_CTL8	0x40010320	Divider control register (for 16.0 divider). See PERI_DIV_16_CTL0 for the details of bit fields.
PERI_DIV_16_CTL9	0x40010324	Divider control register (for 16.0 divider). See PERI_DIV_16_CTL0 for the details of bit fields.
PERI_DIV_16_CTL10	0x40010328	Divider control register (for 16.0 divider). See PERI_DIV_16_CTL0 for the details of bit fields.
PERI_DIV_16_CTL11	0x4001032C	Divider control register (for 16.0 divider). See PERI_DIV_16_CTL0 for the details of bit fields.
PERI_DIV_16_CTL12	0x40010330	Divider control register (for 16.0 divider). See PERI_DIV_16_CTL0 for the details of bit fields.
PERI_DIV_16_CTL13	0x40010334	Divider control register (for 16.0 divider). See PERI_DIV_16_CTL0 for the details of bit fields.
PERI_DIV_16_CTL14	0x40010338	Divider control register (for 16.0 divider). See PERI_DIV_16_CTL0 for the details of bit fields.
PERI_DIV_16_5_CTL0	0x40010400	Divider control register (for 16.5 divider)
PERI_DIV_16_5_CTL1	0x40010404	Divider control register (for 16.5 divider). See PERI_DIV_16_5_CTL0 for the details of bit fields.
PERI_DIV_16_5_CTL2	0x40010408	Divider control register (for 16.5 divider). See PERI_DIV_16_5_CTL0 for the details of bit fields.
PERI_DIV_16_5_CTL3	0x4001040C	Divider control register (for 16.5 divider). See PERI_DIV_16_5_CTL0 for the details of bit fields.
PERI_DIV_16_5_CTL4	0x40010410	Divider control register (for 16.5 divider). See PERI_DIV_16_5_CTL0 for the details of bit fields.
PERI_DIV_24_5_CTL	0x40010500	Divider control register (for 24.5 divider)
PERI_TR_CTL	0x40010600	Trigger control register
PERI_TR_GROUP0_TR_OUT_CTL0	0x40012000	Trigger control register
PERI_TR_GROUP0_TR_OUT_CTL1	0x40012004	Trigger control register. See PERI_TR_GROUP0_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GROUP0_TR_OUT_CTL2	0x40012008	Trigger control register. See PERI_TR_GROUP0_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GROUP0_TR_OUT_CTL3	0x4001200C	Trigger control register. See PERI_TR_GROUP0_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GROUP0_TR_OUT_CTL4	0x40012010	Trigger control register. See PERI_TR_GROUP0_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GROUP0_TR_OUT_CTL5	0x40012014	Trigger control register. See PERI_TR_GROUP0_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GROUP0_TR_OUT_CTL6	0x40012018	Trigger control register. See PERI_TR_GROUP0_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GROUP0_TR_OUT_CTL7	0x4001201C	Trigger control register. See PERI_TR_GROUP0_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GROUP0_TR_OUT_CTL8	0x40012020	Trigger control register. See PERI_TR_GROUP0_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GROUP0_TR_OUT_CTL9	0x40012024	Trigger control register. See PERI_TR_GROUP0_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GROUP0_TR_OUT_CTL10	0x40012028	Trigger control register. See PERI_TR_GROUP0_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GROUP0_TR_OUT_CTL11	0x4001202C	Trigger control register. See PERI_TR_GROUP0_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GROUP0_TR_OUT_CTL12	0x40012030	Trigger control register. See PERI_TR_GROUP0_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GROUP0_TR_OUT_CTL13	0x40012034	Trigger control register. See PERI_TR_GROUP0_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GROUP0_TR_OUT_CTL14	0x40012038	Trigger control register. See PERI_TR_GROUP0_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GROUP0_TR_OUT_CTL15	0x4001203C	Trigger control register. See PERI_TR_GROUP0_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GROUP0_TR_OUT_CTL16	0x40012040	Trigger control register. See PERI_TR_GROUP0_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GROUP0_TR_OUT_CTL17	0x40012044	Trigger control register. See PERI_TR_GROUP0_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GROUP1_TR_OUT_CTL0	0x40012200	Trigger control register
PERI_TR_GROUP1_TR_OUT_CTL1	0x40012204	Trigger control register. See PERI_TR_GROUP1_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GROUP1_TR_OUT_CTL2	0x40012208	Trigger control register. See PERI_TR_GROUP1_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GROUP1_TR_OUT_CTL3	0x4001220C	Trigger control register. See PERI_TR_GROUP1_TR_OUT_CTL0 for the details of bit fields.

Register	Address	Description
PERI_TR_GROUP1_TR_OUT_CTL4	0x40012210	Trigger control register. See PERI_TR_GROUP1_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GROUP1_TR_OUT_CTL5	0x40012214	Trigger control register. See PERI_TR_GROUP1_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GROUP1_TR_OUT_CTL6	0x40012218	Trigger control register. See PERI_TR_GROUP1_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GROUP2_TR_OUT_CTL	0x40012400	Trigger control register
PERI_TR_GROUP3_TR_OUT_CTL0	0x40012600	Trigger control register
PERI_TR_GROUP3_TR_OUT_CTL1	0x40012604	Trigger control register. See PERI_TR_GROUP3_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GROUP3_TR_OUT_CTL2	0x40012608	Trigger control register. See PERI_TR_GROUP3_TR_OUT_CTL0 for the details of bit fields.
PERI_TR_GROUP3_TR_OUT_CTL3	0x4001260C	Trigger control register. See PERI_TR_GROUP3_TR_OUT_CTL0 for the details of bit fields.

2.1.1 PERI_DIV_CMD

Divider command register

Address: 0x40010000

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW					
HW Access	R		R					
Name	SEL_TYPE [7:6]		SEL_DIV [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW					
HW Access	R		R					
Name	PA_SEL_TYPE [15:14]		PA_SEL_DIV [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None					
HW Access	RW1C	RW1C	None					
Name	ENABLE	DISABLE	None [29:24]					

Bits	Name	Description
31	ENABLE	Clock divider enable command (mutually exclusive with DISABLE). Typically, SW sets this field to '1' to enable a divider and HW sets this field to '0' to indicate that divider enabling has completed. When a divider is enabled, its integer and fractional (if present) counters are initialized to "0". If a divider is to be re-enabled using different integer and fractional divider values, the SW should follow these steps: 0: Disable the divider using the DIV_CMD.DISABLE field. 1: Configure the divider's DIV_XXX_CTL register. 2: Enable the divider using the DIV_CMD_ENABLE field. The SEL_DIV and SEL_TYPE fields specify which divider is to be enabled. The enabled divider may be phase aligned to either "clk_hf" (typical usage) or to ANY enabled divider. The PA_SEL_DIV and P_SEL_TYPE fields specify the reference divider. The HW sets the ENABLE field to '0' when the enabling is performed and the HW set the DIV_XXX_CTL.EN field of the divider to '1' when the enabling is performed. Note that enabling with phase alignment to a low frequency divider takes time. E.g. To align to a divider that generates a clock of "clk_hf"/n (with n being the integer divider value INT_DIV+1), up to n cycles may be required to perform alignment. Phase alignment to "clk_hf" takes affect immediately. SW can set this field to '0' during phase alignment to abort the enabling process. Default Value: 0

2.1.1 PERI_DIV_CMD (continued)

30	DISABLE	Clock divider disable command (mutually exlusive with ENABLE). SW sets this field to '1' and HW sets this field to '0'. The SEL_DIV and SEL_TYPE fields specify which divider is to be disabled. The HW sets the DISABLE field to '0' immediately and the HW sets the DIV_XXX_CTL.EN field of the divider to '0' immediately. Default Value: 0
15 : 14	PA_SEL_TYPE	Specifies the divider type of the divider to which phase alignment is performed for the clock enable command: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
13 : 8	PA_SEL_DIV	(PA_SEL_TYPE, PA_SEL_DIV) pecifies the divider to which phase alignment is performed for the clock enable command. Any enabled divider can be used as reference. This allows all dividers to be aligned with each other, even when they are enabled at different times. If PA_SEL_DIV is "63" and "PA_SEL_TYPE" is "3", "clk_hf" is used as reference. Default Value: 63
7 : 6	SEL_TYPE	Specifies the divider type of the divider on which the command is performed: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
5 : 0	SEL_DIV	(SEL_TYPE, SEL_DIV) specifies the divider on which the command (DISABLE/ENABLE) is performed. If SEL_DIV is "63" and "SEL_TYPE" is "3" (default/reset value), no divider is specified and no clock signal(s) are generated. Default Value: 63

2.1.2 PERI_PCLK_CTL0

Programmable clock control register

Address: 0x40010100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None		RW			
HW Access	R		None		R			
Name	SEL_TYPE [7:6]		None [5:4]		SEL_DIV [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	SEL_TYPE	Specifies divider type: 0: 8.0 (integer) clock dividers. 1: 16.0 (integer) clock dividers. 2: 16.5 (fractional) clock dividers. 3: 24.5 (fractional) clock dividers. Default Value: 3
3 : 0	SEL_DIV	Specifies one of the dividers of the divider type specified by SEL_TYPE. If SEL_DIV is "63" and "SEL_TYPE" is "3" (default/reset value), no divider is specified and no clock control signal(s) are generated. When transitioning a clock between two out of phase dividers, spurious clock control signals may be generated for one "clk_hf" cycle during this transition. These clock control signals may cause a single clock period that is smaller than any of the two divider periods. To prevent these spurious clock signals, the clock multiplexer can be disconnected (SEL_DIV is "63" and "SEL_TYPE" is "3") for a transition time that is larger than the smaller of the two divider periods. Default Value: 15

2.1.3 PERI_DIV_16_CTL0

Divider control register (for 16.0 divider)

Address: 0x40010300

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INT16_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INT16_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 8	INT16_DIV	Integer division by (1+INT16_DIV). Allows for integer divisions in the range [1, 65,536]. Note: this type of divider does NOT allow for a fractional division. For the generation of a divided clock, the integer division range is restricted to [2, 65,536]. For the generation of a 50/50% duty cycle digital divided clock, the integer division range is restricted to even numbers in the range [2, 65,536]. The generation of a 50/50 % duty cycle analog divided clock has no restrictions. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0
0	EN	Divider enabled. HW sets this field to '1' as a result of an ENABLE command. HW sets this field to '0' as a result on a DISABLE command. Note that this field is retained. As a result, the divider does NOT have to be re-enabled after transitioning from DeepSleep to Active power mode. Default Value: 0

2.1.4 PERI_DIV_16_5_CTL0

Divider control register (for 16.5 divider)

Address: 0x40010400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		R
HW Access	R					None		RW
Name	FRAC5_DIV [7:3]					None [2:1]		EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INT16_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INT16_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 8	INT16_DIV	Integer division by (1+INT16_DIV). Allows for integer divisions in the range [1, 65,536]. Note: combined with fractional division, this divider type allows for a division in the range [1, 65,536 31/32] in 1/32 increments. For the generation of a divided clock, the division range is restricted to [2, 65,536 31/32]. For the generation of a 50/50% duty cycle divided clock, the division range is restricted to [2, 65,536]. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0
7 : 3	FRAC5_DIV	Fractional division by (FRAC5_DIV/32). Allows for fractional divisions in the range [0, 31/32]. Note that fractional division results in clock jitter as some clock periods may be 1 "clk_hf" cycle longer than other clock periods. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0

2.1.4 PERI_DIV_16_5_CTL0 (continued)

0	EN	Divider enabled. HW sets this field to '1' as a result of an ENABLE command. HW sets this field to '0' as a result on a DISABLE command. Note that this field is retained. As a result, the divider does NOT have to be re-enabled after transitioning from DeepSleep to Active power mode. Default Value: 0

2.1.5 PERI_DIV_24_5_CTL

Divider control register (for 24.5 divider)

Address: 0x40010500

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW					None		R
HW Access	R					None		RW
Name	FRAC5_DIV [7:3]					None [2:1]		EN

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	INT24_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INT24_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	INT24_DIV [31:24]							

Bits	Name	Description
31 : 8	INT24_DIV	Integer division by (1+INT24_DIV). Allows for integer divisions in the range [1, 16,777,216]. Note: combined with fractional division, this divider type allows for a division in the range [1, 16,777,216 31/32] in 1/32 increments. For the generation of a divided clock, the integer division range is restricted to [2, 16,777,216 31/32]. For the generation of a 50/50% duty cycle divided clock, the division range is restricted to [2, 16,777,216]. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0
7 : 3	FRAC5_DIV	Fractional division by (FRAC5_DIV/32). Allows for fractional divisions in the range [0, 31/32]. Note that fractional division results in clock jitter as some clock periods may be 1 "clk_hf" cycle longer than other clock periods. Note that this field is retained. However, the counter that is used to implement the division is not and will be initialized by HW to "0" when transitioning from DeepSleep to Active power mode. Default Value: 0

2.1.5 PERI_DIV_24_5_CTL (continued)

0	EN	Divider enabled. HW sets this field to '1' as a result of an ENABLE command. HW sets this field to '0' as a result on a DISABLE command. Note that this field is retained. As a result, the divider does NOT have to be re-enabled after transitioning from DeepSleep to Active power mode. Default Value: 0

2.1.6 PERI_TR_CTL

Trigger control register

Address: 0x40010600

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW						
HW Access	None	R						
Name	None	TR_SEL [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				TR_GROUP [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	TR_COUNT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None					
HW Access	RW1C	R	None					
Name	TR_ACT	TR_OUT	None [29:24]					

Bits	Name	Description
31	TR_ACT	SW sets this field to '1' by to activate (set to '1') a trigger as identified by TR_SEL and TR_OUT for TR_COUNT cycles. HW sets this field to '0' when the cycle counter is decremented to "0". Note: a TR_COUNT value of 255 is a special case and trigger activation is under direct control of the TR_ACT field (the counter is not decremented). Default Value: 0
30	TR_OUT	Specifies whether trigger activation is for a specific input or ouput trigger of the trigger multiplexer. Activation of a specific input trigger, will result in activation of all output triggers that have the specific input trigger selected through their TR_OUT_CTL.SEL field. Activation of a specific output trigger, will result in activation of the specified TR_SEL output trigger only. '0': TR_SEL selection and trigger activation is for an input trigger to the trigger multiplexer. '1': TR_SEL selection and trigger activation is for an output trigger from the trigger multiplexer. Default Value: 0
23 : 16	TR_COUNT	Amount of cycles a specific trigger is activated. During activation (TR_ACT is '1'), HW decrements this field to "0" using a cycle counter. During activation, SW should not modify this register field. A value of 255 is a special case: HW does NOT decrement this field to "0" and trigger activation is under direct control of TR_ACT: when TR_ACT is '1' the trigger is activated and when TR_ACT is '0' the trigger is deactivated. Default Value: 0

2.1.6 PERI_TR_CTL (continued)

11 : 8	TR_GROUP	Specifies the trigger group. Default Value: 0
6 : 0	TR_SEL	Specifies the activated trigger when TR_ACT is '1'. TR_OUT specifies whether the activated trigger is an input trigger or output trigger to the trigger multiplexer. During activation (TR_ACT is '1'), SW should not modify this register field. If the specified trigger is not present, the trigger activation has no effect. Default Value: 0

2.1.7 PERI_TR_GROUP0_TR_OUT_CTL0

Trigger control register

Address: 0x40012000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW						
HW Access	None	R						
Name	None	SEL [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
6 : 0	SEL	Specifies input trigger. This field is typically set during the setup of a chip use case scenario. Changing this field while activated triggers are present on the input triggers may result in unpredictable behavior. Note that input trigger 0 (default value) is typically connected to a constant signal level of '0', and as a result will not cause HW activation of the output trigger. Default Value: 0

2.1.8 PERI_TR_GROUP1_TR_OUT_CTL0

Trigger control register

Address: 0x40012200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		SEL [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	SEL	Specifies input trigger. This field is typically set during the setup of a chip use case scenario. Changing this field while activated triggers are present on the input triggers may result in unpredictable behavior. Note that input trigger 0 (default value) is typically connected to a constant signal level of '0', and as a result will not cause HW activation of the output trigger. Default Value: 0

2.1.9 PERI_TR_GROUP2_TR_OUT_CTL

Trigger control register

Address: 0x40012400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		SEL [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	SEL	Specifies input trigger. This field is typically set during the setup of a chip use case scenario. Changing this field while activated triggers are present on the input triggers may result in unpredictable behavior. Note that input trigger 0 (default value) is typically connected to a constant signal level of '0', and as a result will not cause HW activation of the output trigger. Default Value: 0

2.1.10 PERI_TR_GROUP3_TR_OUT_CTL0

Trigger control register

Address: 0x40012600

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			R				
Name	None [7:5]			SEL [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4 : 0	SEL	Specifies input trigger. This field is typically set during the setup of a chip use case scenario. Changing this field while activated triggers are present on the input triggers may result in unpredictable behavior. Note that input trigger 0 (default value) is typically connected to a constant signal level of '0', and as a result will not cause HW activation of the output trigger. Default Value: 0

3 High Speed IO Matrix (HSIOM) Registers

This section discusses the HSIOM registers. It lists all the registers in mapping tables, in address order.

3.1 Register Details

Register	Address	Description
HSIOM_PORT_SEL0	0x40020000	Port selection register
HSIOM_PORT_SEL1	0x40020100	Port selection register. See HSIOM_PORT_SEL0 for the details of bit fields.
HSIOM_PORT_SEL2	0x40020200	Port selection register. See HSIOM_PORT_SEL0 for the details of bit fields.
HSIOM_PORT_SEL3	0x40020300	Port selection register. See HSIOM_PORT_SEL0 for the details of bit fields.
HSIOM_PORT_SEL4	0x40020400	Port selection register. See HSIOM_PORT_SEL0 for the details of bit fields.
HSIOM_PORT_SEL5	0x40020500	Port selection register. See HSIOM_PORT_SEL0 for the details of bit fields.
HSIOM_PORT_SEL6	0x40020600	Port selection register
HSIOM_PORT_SEL7	0x40020700	Port selection register. See HSIOM_PORT_SEL0 for the details of bit fields.
HSIOM_PORT_SEL8	0x40020800	Port selection register
HSIOM_PORT_SEL9	0x40020900	Port selection register. See HSIOM_PORT_SEL8 for the details of bit fields.
HSIOM_PORT_SEL10	0x40020A00	Port selection register. See HSIOM_PORT_SEL6 for the details of bit fields.
HSIOM_PORT_SEL11	0x40020B00	Port selection register. See HSIOM_PORT_SEL6 for the details of bit fields.
HSIOM_PORT_SEL12	0x40020C00	Port selection register
HSIOM_PUMP_CTL	0x40022000	Pump control
HSIOM_AMUX_SPLIT_CTL0	0x40022100	AMUX splitter cell control
HSIOM_AMUX_SPLIT_CTL1	0x40022104	AMUX splitter cell control. See HSIOM_AMUX_SPLIT_CTL0 for the details of bit fields.
HSIOM_AMUX_SPLIT_CTL2	0x40022108	AMUX splitter cell control. See HSIOM_AMUX_SPLIT_CTL0 for the details of bit fields.

3.1.1 HSIOM_PORT_SEL0

Port selection register

Address: 0x40020000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO1_SEL [7:4]				IO0_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO3_SEL [15:12]				IO2_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO5_SEL [23:20]				IO4_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO7_SEL [31:28]				IO6_SEL [27:24]			

Bits	Name	Description
31 : 28	IO7_SEL	Selects connection for IO pad 7 route. Default Value: 0
27 : 24	IO6_SEL	Selects connection for IO pad 6 route. Default Value: 0
23 : 20	IO5_SEL	Selects connection for IO pad 5 route. Default Value: 0
19 : 16	IO4_SEL	Selects connection for IO pad 4 route. Default Value: 0
15 : 12	IO3_SEL	Selects connection for IO pad 3 route. Default Value: 0
11 : 8	IO2_SEL	Selects connection for IO pad 2 route. Default Value: 0
7 : 4	IO1_SEL	Selects connection for IO pad 1 route. Default Value: 0
3 : 0	IO0_SEL	Selects connection for IO pad 0 route. Default Value: 0

3.1.1 HSIOM_PORT_SEL0 (continued)

0x0: GPIO :

SW controlled GPIO.

0x1: GPIO_DSI :

SW controlled "out", DSI controlled "oe_n".

0x2: DSI_DSI :

DSI controlled "out" and "oe_n".

0x3: DSI_GPIO :

DSI controlled "out", SW controlled "oe_n".

0x4: CSD_SENSE :

CapSense sense connection (analog mode)

0x5: CSD_SHIELD :

CapSense shield connection (analog mode)

0x6: AMUXA :

AMUXBUS A connection.

0x7: AMUXB :

AMUXBUS B connection.

0x8: ACT_0 :

Chip specific Active source 0 connection.

0x9: ACT_1 :

Chip specific Active source 1 connection.

0xa: ACT_2 :

Chip specific Active source 2 connection.

0xb: ACT_3 :

Chip specific Active source 3 connection.

3.1.1 HSIOM_PORT_SEL0 (continued)

0xc: LCD_COM :

LCD common connection. This mode provides DeepSleep functionality (provided that the LCD block is enabled and properly configured).

0xd: LCD_SEG :

LCD segment connection. This mode provides DeepSleep functionality (provided that the LCD block is enabled and properly configured).

0xc: DS_0 :

Chip specific DeepSleep source 0 connection.

0xd: DS_1 :

Chip specific DeepSleep source 1 connection.

0xe: DS_2 :

Chip specific DeepSleep source 2 connection.

0xf: DS_3 :

Chip specific DeepSleep source 3 connection.

3.1.2 HSIOM_PORT_SEL6

Port selection register

Address: 0x40020600

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO1_SEL [7:4]				IO0_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO3_SEL [15:12]				IO2_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO5_SEL [23:20]				IO4_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 20	IO5_SEL	Selects connection for IO pad 5 route. Default Value: 0
19 : 16	IO4_SEL	Selects connection for IO pad 4 route. Default Value: 0
15 : 12	IO3_SEL	Selects connection for IO pad 3 route. Default Value: 0
11 : 8	IO2_SEL	Selects connection for IO pad 2 route. Default Value: 0
7 : 4	IO1_SEL	Selects connection for IO pad 1 route. Default Value: 0
3 : 0	IO0_SEL	Selects connection for IO pad 0 route. Default Value: 0 **0x0: GPIO :** SW controlled GPIO.

3.1.2 HSIOM_PORT_SEL6 (continued)

0x1: GPIO_DSI :

SW controlled "out", DSI controlled "oe_n".

0x2: DSI_DSI :

DSI controlled "out" and "oe_n".

0x3: DSI_GPIO :

DSI controlled "out", SW controlled "oe_n".

0x4: CSD_SENSE :

CapSense sense connection (analog mode)

0x5: CSD_SHIELD :

CapSense shield connection (analog mode)

0x6: AMUXA :

AMUXBUS A connection.

0x7: AMUXB :

AMUXBUS B connection.

0x8: ACT_0 :

Chip specific Active source 0 connection.

0x9: ACT_1 :

Chip specific Active source 1 connection.

0xa: ACT_2 :

Chip specific Active source 2 connection.

0xb: ACT_3 :

Chip specific Active source 3 connection.

0xc: LCD_COM :

LCD common connection. This mode provides DeepSleep functionality (provided that the LCD block is enabled and properly configured).

3.1.2 HSIOM_PORT_SEL6 (continued)

0xd: LCD_SEG :

LCD segment connection. This mode provides DeepSleep functionality (provided that the LCD block is enabled and properly configured).

0xc: DS_0 :

Chip specific DeepSleep source 0 connection.

0xd: DS_1 :

Chip specific DeepSleep source 1 connection.

0xe: DS_2 :

Chip specific DeepSleep source 2 connection.

0xf: DS_3 :

Chip specific DeepSleep source 3 connection.

3.1.3 HSIOM_PORT_SEL8

Port selection register

Address: 0x40020800

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO1_SEL [7:4]				IO0_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO3_SEL [15:12]				IO2_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 12	IO3_SEL	Selects connection for IO pad 3 route. Default Value: 0
11 : 8	IO2_SEL	Selects connection for IO pad 2 route. Default Value: 0
7 : 4	IO1_SEL	Selects connection for IO pad 1 route. Default Value: 0
3 : 0	IO0_SEL	Selects connection for IO pad 0 route. Default Value: 0 **0x0: GPIO :** SW controlled GPIO. **0x1: GPIO_DSI :** SW controlled "out", DSI controlled "oe_n".

3.1.3 HSIOM_PORT_SEL8 (continued)

0x2: DSI_DSI :

DSI controlled "out" and "oe_n".

0x3: DSI_GPIO :

DSI controlled "out", SW controlled "oe_n".

0x4: CSD_SENSE :

CapSense sense connection (analog mode)

0x5: CSD_SHIELD :

CapSense shield connection (analog mode)

0x6: AMUXA :

AMUXBUS A connection.

0x7: AMUXB :

AMUXBUS B connection.

0x8: ACT_0 :

Chip specific Active source 0 connection.

0x9: ACT_1 :

Chip specific Active source 1 connection.

0xa: ACT_2 :

Chip specific Active source 2 connection.

0xb: ACT_3 :

Chip specific Active source 3 connection.

0xc: LCD_COM :

LCD common connection. This mode provides DeepSleep functionality (provided that the LCD block is enabled and properly configured).

0xd: LCD_SEG :

LCD segment connection. This mode provides DeepSleep functionality (provided that the LCD block is enabled and properly configured).

3.1.3 HSIOM_PORT_SEL8 (continued)

0xc: DS_0 :

Chip specific DeepSleep source 0 connection.

0xd: DS_1 :

Chip specific DeepSleep source 1 connection.

0xe: DS_2 :

Chip specific DeepSleep source 2 connection.

0xf: DS_3 :

Chip specific DeepSleep source 3 connection.

3.1.4 HSIOM_PORT_SEL12

Port selection register

Address: 0x40020C00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	RW				RW			
Name	IO1_SEL [7:4]				IO0_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	IO1_SEL	Selects connection for IO pad 1 route. Default Value: 0
3 : 0	IO0_SEL	Selects connection for IO pad 0 route. Default Value: 0 **0x0: GPIO :** SW controlled GPIO. **0x1: GPIO_DSI :** SW controlled "out", DSI controlled "oe_n". **0x2: DSI_DSI :** DSI controlled "out" and "oe_n".

3.1.4 HSIOM_PORT_SEL12 (continued)

0x3: DSI_GPIO :

DSI controlled "out", SW controlled "oe_n".

0x4: CSD_SENSE :

CapSense sense connection (analog mode)

0x5: CSD_SHIELD :

CapSense shield connection (analog mode)

0x6: AMUXA :

AMUXBUS A connection.

0x7: AMUXB :

AMUXBUS B connection.

0x8: ACT_0 :

Chip specific Active source 0 connection.

0x9: ACT_1 :

Chip specific Active source 1 connection.

0xa: ACT_2 :

Chip specific Active source 2 connection.

0xb: ACT_3 :

Chip specific Active source 3 connection.

0xc: LCD_COM :

LCD common connection. This mode provides DeepSleep functionality (provided that the LCD block is enabled and properly configured).

0xd: LCD_SEG :

LCD segment connection. This mode provides DeepSleep functionality (provided that the LCD block is enabled and properly configured).

0xc: DS_0 :

Chip specific DeepSleep source 0 connection.

3.1.4 HSIOM_PORT_SEL12 (continued)

0xd: DS_1 :

Chip specific DeepSleep source 1 connection.

0xe: DS_2 :

Chip specific DeepSleep source 2 connection.

0xf: DS_3 :

Chip specific DeepSleep source 3 connection.

3.1.5 HSIOM_PUMP_CTL

Pump control

Address: 0x40022000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							CLOCK_-SEL

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	ENABLED	None [30:24]						

Bits	Name	Description
31	ENABLED	Pump enabled: '0': Disabled. '1': Enabled. Default Value: 0
0	CLOCK_SEL	Clock select: '0': External clock. '1': Internal clock (deprecated). Default Value: 0

3.1.6 HSIOM_AMUX_SPLIT_CTL0

AMUX splitter cell control

Address: 0x40022100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	RW	RW	None	RW	RW	RW
HW Access	None	R	R	R	None	R	R	R
Name	None	SWITCH_B-B_S0	SWITCH_B-B_SR	SWITCH_B-B_SL	None	SWITCH_AA_S0	SWITCH_AA_SR	SWITCH_AA_SL

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
6	SWITCH_BB_S0	T-switch control for AMUXBUSB vssa/ground switch. Default Value: 0
5	SWITCH_BB_SR	T-switch control for Right AMUXBUSB switch. Default Value: 0
4	SWITCH_BB_SL	T-switch control for Left AMUXBUSB switch. Default Value: 0
2	SWITCH_AA_S0	T-switch control for AMUXBUSA vssa/ground switch: '0': switch open. '1': switch closed. Default Value: 0
1	SWITCH_AA_SR	T-switch control for Right AMUXBUSA switch: '0': switch open. '1': switch closed. Default Value: 0

3.1.6 HSIOM_AMUX_SPLIT_CTL0 (continued)

0	SWITCH_AA_SL	T-switch control for Left AMUXBUSA switch: '0': switch open. '1': switch closed. Default Value: 0

4 System Resources Subsystem (SRSS) Registers

This section discusses the SRSS registers. It lists all the registers in mapping tables, in address order.

4.1 Register Details

Register	Address	Description
PWR_CONTROL	0x40030000	Power Mode Control
PWR_KEY_DELAY	0x40030004	Power System Key&Delay Register
PWR_DDFT_SELECT	0x4003000C	Power DDFT Mode Selection Register
TST_MODE	0x40030014	Test Mode Control Register
CLK_SELECT	0x40030028	Clock Select Register
CLK_ILO_CONFIG	0x4003002C	ILO Configuration
CLK_IMO_CONFIG	0x40030030	IMO Configuration
CLK_DFT_SELECT	0x40030034	Clock DFT Mode Selection Register
WDT_DISABLE_KEY	0x40030038	Watchdog Disable Key Register
WDT_COUNTER	0x4003003C	Watchdog Counter Register
WDT_MATCH	0x40030040	Watchdog Match Register
SRSS_INTR	0x40030044	SRSS Interrupt Register
SRSS_INTR_SET	0x40030048	SRSS Interrupt Set Register
SRSS_INTR_MASK	0x4003004C	SRSS Interrupt Mask Register
RES_CAUSE	0x40030054	Reset Cause Observation Register
PWR_BG_TRIM1	0x40030F00	Bandgap Trim Register
PWR_BG_TRIM2	0x40030F04	Bandgap Trim Register
CLK_IMO_SELECT	0x40030F08	IMO Frequency Select Register
CLK_IMO_TRIM1	0x40030F0C	IMO Trim Register
CLK_IMO_TRIM2	0x40030F10	IMO Trim Register
PWR_PWRSYS_TRIM1	0x40030F14	Power System Trim Register
CLK_IMO_TRIM3	0x40030F18	IMO Trim Register

4.1.1 PWR_CONTROL

Power Mode Control

Address: 0x40030000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R	R	R			
HW Access	None		RW	RW	RW			
Name	None [7:6]		LP-M_READY	DEBUG_-SESSION	POWER_MODE [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	None			R		RW	RW
HW Access	A	None			RW		R	R
Name	EXT_VCCD	None [22:20]			SPARE [19:18]		OVER_-TEMP_-THRESH	OVER_-TEMP_EN

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23	EXT_VCCD	Always write 0 except as noted below. For PSoC 4000 CapSense products, set this bit if Vccd is provided externally (on Vccd pin). Setting this bit turns off the active regulator and will lead to system reset (BOD) unless both Vddd and Vccd pins are supplied externally. This register bit only resets for XRES, POR, or a detected BOD. Default Value: 0
19 : 18	SPARE	Spare AHB readback bits that are hooked to PWR_PWRSYS_TRIM1.SPARE_TRIM[1:0] through spare logic equivalent to bitwise inversion. Engineering only. Default Value: 0
17	OVER_TEMP_THRESH	Over-temperature threshold. 0: TEMP_HIGH condition occurs between 120C and 125C. 1: TEMP_HIGH condition occurs between 60C and 75C (used for testing). Default Value: 0

4.1.1 PWR_CONTROL (continued)

16	OVER_TEMP_EN	Enable the die over temperature sensor. Must be enabled when using the TEMP_HIGH interrupt. 0: Disable 1: Enable Default Value: 0
5	LPM_READY	Indicates whether the low power mode regulator is ready to enter DEEPSLEEP mode. 0: If DEEPSLEEP mode is requested, device will enter SLEEP mode. When low power regulators are ready, device will automatically enter the originally requested mode. 1: Normal operation. DEEPSLEEP works as described. Default Value: 0
4	DEBUG_SESSION	Indicates whether a debug session is active 0: Inactive 1: Active Default Value: 0 **0x0: NO_SESSION :** No debug session active **0x1: SESSION_ACTIVE :** Debug session is active
3 : 0	POWER_MODE	Current power mode of the device. Note that this field cannot be read in all power modes on actual silicon. Default Value: 0 **0x0: RESET :** RESET state **0x1: ACTIVE :** ACTIVE state **0x2: SLEEP :** SLEEP state **0x3: DEEP_SLEEP :** DEEP_SLEEP state

4.1.2 PWR_KEY_DELAY

Power System Key Register

Address: 0x40030004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	WAKEUP_HOLDOFF [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						WAKEUP_HOLDOFF [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 0	WAKEUP_HOLDOFF	Delay to wait for references to settle on wakeup from deepsleep. BOD is ignored and system does not resume until this delay expires. Note that the same delay on POR is hard-coded. The default assumes the output of the predivider is 48MHz + 3%. Firmware may scale this setting according to the fastest actual clock frequency that can occur when waking from DEEPSLEEP. Default Value: 248

4.1.3 PWR_DDFT_SELECT

Power DDFT Mode Selection Register

Address: 0x4003000C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	DDFT1_SEL [7:4]				DDFT0_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	DDFT1_SEL	Select signal for power DDFT output #1 Default Value: 0 **0x0: WAKEUP :** wakeup **0x1: AWAKE :** awake **0x2: ACT_POWER_EN :** act_power_en **0x3: ACT_POWER_UP :** act_power_up

4.1.3 PWR_DDFT_SELECT (continued)

0x4: ACT_POWER_GOOD :

act_power_good

0x5: ACT_REF_VALID :

act_ref_valid

0x6: ACT_REG_VALID :

act_reg_valid

0x7: ACT_COMP_OUT :

act_comp_out

0x8: ACT_TEMP_HIGH :

act_temp_high

0x9: DPSLP_COMP_OUT :

dpslp_comp_out

0xa: DPSLP_POWER_UP :

dpslp_power_up

0xb: AWAKE_DELAYED :

awake_delayed

0xc: LPM_READY :

lpm_ready

0xd: SLEEPHOLDACK_N :

sleepholdack_n

0xe: GND :

1'b0

0xf: PWR :

1'b1

3 : 0	DDFT0_SEL	Select signal for power DDFT output #0 Default Value: 0

4.1.3 PWR_DDFT_SELECT (continued)

0x0: WAKEUP :

wakeup

0x1: AWAKE :

awake

0x2: ACT_POWER_EN :

act_power_en

0x3: ACT_POWER_UP :

act_power_up

0x4: ACT_POWER_GOOD :

act_power_good

0x5: ACT_REF_EN :

srss_adft_control_act_ref_en

0x6: ACT_COMP_EN :

srss_adft_control_act_comp_en

0x7: DPSLP_REF_EN :

srss_adft_control_dpslp_ref_en

0x8: DPSLP_REG_EN :

srss_adft_control_dpslp_reg_en

0x9: DPSLP_COMP_EN :

srss_adft_control_dpslp_comp_en

0xa: OVER_TEMP_EN :

pwr_control_over_temp_en

0xb: SLEEPHOLDREQ_N :

sleepholdreq_n

4.1.3 PWR_DDFT_SELECT (continued)

0xc: ADFT_BUF_EN :

adft_buf_en

0xd: ATPG_OBSERVE :

ATPG observe point (no functional purpose)

0xe: GND :

1'b0

0xf: PWR :

1'b1

4.1.4 TST_MODE

Test Mode Control Register

Address: 0x40030014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					R	None	
HW Access	None					RW	None	
Name	None [7:3]					SWD_CON-NECTED	None	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	R	None	RW	None			
HW Access	R	RW	None	A	None			
Name	TEST_-MODE	TEST_KEY_DFT_EN	None	BLOCK_ALT_XRES	None [27:24]			

Bits	Name	Description
31	TEST_MODE	Setting this bit will prevent BootROM from yielding execution to Flash image. 0: Normal operation mode 1: Test mode (any test mode) Default Value: 0
30	TEST_KEY_DFT_EN	This bit is set when a XRES test mode key is shifted in. It is the value of the test_key_dft_en signal. When this bit is set, the BootROM will not yield execution to the FLASH image (same function as setting TEST_MODE bit below). Default Value: 0
28	BLOCK_ALT_XRES	Relevant only for parts that have the alternate XRES mechanism of overloading a GPIO pin temporarily as alternate XRES during test. When set, this bit blocks the alternate XRES function, such that the pin can be used for normal I/O or for ddft/adft observation. See SAS Part-V and Part-IX for details. This register bit only resets for XRES, POR, or a detected BOD. Default Value: 0
2	SWD_CONNECTED	Indicates SWD Connection status 0: SWD not active 1: SWD activated (Line Reset & Connect sequence passed) Default Value: 0

4.1.5 CLK_SELECT

Clock Select Register

Address: 0x40030028

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	SYSCLK_DIV [7:6]		PUMP_SEL [5:4]		HFCLK_DIV [3:2]		HFCLK_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 6	SYSCLK_DIV	Select clk_sys prescaler value. Default Value: 0 **0x0: NO_DIV :** clk_sys= clk_hf/1 **0x1: DIV_BY_2 :** clk_sys= clk_hf/2 **0x2: DIV_BY_4 :** clk_sys= clk_hf/4 **0x3: DIV_BY_8 :** clk_sys= clk_hf/8

4.1.5 CLK_SELECT (continued)

5 : 4	PUMP_SEL	Selects clock source for charge pump clock. This clock is not guaranteed to be glitch free when changing any of its sources or settings. Default Value: 0 **0x0: GND :** No clock, connect to gnd **0x1: IMO :** Use main IMO output **0x2: HFCLK :** Use clk_hf (using selected source after predivider but before prescaler)
3 : 2	HFCLK_DIV	Selects clk_hf predivider value. Default Value: 2 **0x0: NO_DIV :** Transparent mode, feed through selected clock source w/o dividing. **0x1: DIV_BY_2 :** Divide selected clock source by 2 **0x2: DIV_BY_4 :** Divide selected clock source by 4 **0x3: DIV_BY_8 :** Divide selected clock source by 8
1 : 0	HFCLK_SEL	Selects a source for clk_hf and dsi_in[0]. Note that not all products support all clock sources. Selecting a clock source that is not supported will result in undefined behavior. Default Value: 0 **0x0: IMO :** IMO - Internal R/C Oscillator **0x1: EXTCLK :** EXTCLK - External Clock Pin **0x2: ECO :** ECO - External-Crystal Oscillator or PLL subsystem output

4.1.6 CLK_ILO_CONFIG

ILO Configuration

Address: 0x4003002C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	RW	None						
Name	ENABLE	None						

Bits	Name	Description
31	ENABLE	Master enable for ILO oscillator. This bit is hardware set whenever the WDT_DISABLE_KEY is not set to the magic value. Default Value: 1

4.1.7 CLK_IMO_CONFIG

IMO Configuration

Address: 0x40030030

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	ENABLE	None						

Bits	Name	Description
31	ENABLE	Master enable for IMO oscillator. Clearing this bit will disable the IMO. Don't do this if the system is running off it. Default Value: 1

4.1.8 CLK_DFT_SELECT

Clock DFT Mode Selection Register

Address: 0x40030034

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	RW		RW			
HW Access	None	R	R		R			
Name	None	DFT_EDGE0	DFT_DIV0 [5:4]		DFT_SEL0 [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW	RW		RW			
HW Access	None	R	R		R			
Name	None	DFT_EDGE1	DFT_DIV1 [13:12]		DFT_SEL1 [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
14	DFT_EDGE1	Edge sensitivity for in-line divider on output #1 (only relevant when DIV1>0). Default Value: 0 **0x0: POSEDGE :** Use posedge for divider **0x1: NEGEDGE :** Use negedge for divider
13 : 12	DFT_DIV1	DFT Output Divide Down. Default Value: 0 **0x0: NO_DIV :** Direct Output

4.1.8 CLK_DFT_SELECT (continued)

		0x1: DIV_BY_2 : Divide by 2 **0x2: DIV_BY_4 :** Divide by 4 **0x3: DIV_BY_8 :** Divide by 8
11 : 8	DFT_SEL1	Select signal for DFT output #1 Default Value: 0 **0x0: NC :** Disabled - output is 0 **0x1: ILO :** clk_ilo: ILO output **0x2: IMO :** clk_imo: IMO primary output **0x3: ECO :** clk_eco: ECO output **0x4: EXTCLK :** clk_ext: external clock input **0x5: HFCLK :** clk_hf: root of the high-speed clock tree **0x6: LFCLK :** clk_lf: root of the low-speed clock tree **0x7: SYSCLK :** clk_sys: root of the CPU/AHB clock tree (gated version of clk_hf) **0x8: PUMPCLK :** clk_pump: clock provided to charge pumps in FLASH and PA

4.1.8 CLK_DFT_SELECT (continued)

		0x9: SLPCTRLCLK : clk_slpctrl: clock provided to SleepController
6	DFT_EDGE0	Edge sensitivity for in-line divider on output #0 (only relevant when DIV0>0). Default Value: 0 **0x0: POSEDGE :** Use posedge for divider **0x1: NEGEDGE :** Use negedge for divider
5 : 4	DFT_DIV0	DFT Output Divide Down. Default Value: 0 **0x0: NO_DIV :** Direct Output **0x1: DIV_BY_2 :** Divide by 2 **0x2: DIV_BY_4 :** Divide by 4 **0x3: DIV_BY_8 :** Divide by 8
3 : 0	DFT_SEL0	Select signal for DFT output #0 Default Value: 0 **0x0: NC :** Disabled - output is 0 **0x1: ILO :** clk_ilo: ILO output **0x2: IMO :** clk_imo: IMO primary output **0x3: ECO :** clk_eco: ECO output

4.1.8 CLK_DFT_SELECT (continued)

0x4: EXTCLK :

clk_ext: external clock input

0x5: HFCLK :

clk_hf: root of the high-speed clock tree

0x6: LFCLK :

clk_lf: root of the low-speed clock tree

0x7: SYSCLK :

clk_sys: root of the CPU/AHB clock tree (gated version of clk_hf)

0x8: PUMPCLK :

clk_pump: clock provided to charge pumps in FLASH and PA

0x9: SLPCTRLCLK :

clk_slpctrl: clock provided to SleepController

4.1.9 WDT_DISABLE_KEY

Watchdog Disable Key Register

Address: 0x40030038

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	KEY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	KEY [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	KEY [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	KEY [31:24]							

Bits	Name	Description
31 : 0	KEY	Disables WDT reset when equal to 0xACED8865. The WDT reset functions normally for any other setting. Default Value: 0

4.1.10 WDT_COUNTER

Watchdog Counter Register

Address: 0x4003003C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	COUNTER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	COUNTER [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	COUNTER	Current value of WDT Counter Default Value: 0

4.1.11 WDT_MATCH

Watchdog Match Register

Address: 0x40030040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	MATCH [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	MATCH [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				IGNORE_BITS [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	IGNORE_BITS	The number of MSB bits of the watchdog timer that are NOT checked against MATCH. This value provides control over the time-to-reset of the watchdog (which happens after 3 successive matches). Note that certain products may enforce a minimum value for this register through design time configuration. Default Value: 0
15 : 0	MATCH	Match value for Watchdog counter. Every time WDT_COUNTER reaches MATCH an interrupt is generated. Two unserviced interrupts will lead to a system reset (i.e. at the third match). Default Value: 4096

4.1.12 SRSS_INTR

SRSS Interrupt Register

Address: 0x40030044

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1C	RW1C
HW Access	None						A	A
Name	None [7:2]						TEMP_HIGH	WDT_-MATCH

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	TEMP_HIGH	Regulator over-temp interrupt. This interrupt can occur when a short circuit exists on the vccd pin or when extreme loads are applied on IO-cells causing the die to overheat. Firmware is encourage to shutdown all IO cells and then go to DeepSleep mode when this interrupt occurs if protection against such conditions is desired. Default Value: 0
0	WDT_MATCH	WDT Interrupt Request. This bit is set each time WDT_COUNTR==WDT_MATCH. Clearing this bit also feeds the watch dog. Missing 2 interrupts in a row will generate brown-out reset. Due to internal synchronization, it takes 2 SYSCLK cycles to update after a W1C. Default Value: 0

4.1.13 SRSS_INTR_SET

SRSS Interrupt Set Register

Address: 0x40030048

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1S	None
HW Access	None						A	None
Name	None [7:2]						TEMP_HIGH	None

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	TEMP_HIGH	Writing 1 to this bit internally sets the overtemp interrupt. This can be observed by reading SRSS_INTR.TEMP_HIGH. This bit always reads back as zero. Default Value: 0

4.1.14 SRSS_INTR_MASK

SRSS Interrupt Mask Register

Address: 0x4003004C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						TEMP_HIGH	WDT_-MATCH

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	TEMP_HIGH	Masks REG_OVERTEMP interrupt Default Value: 0
0	WDT_MATCH	Clearing this bit will not forward the interrupt to the CPU. It will not, however, disable the WDT reset generation on 2 missed interrupts. Default Value: 0

4.1.15 RES_CAUSE

Reset Cause Observation Register

Address: 0x40030054

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW1C	RW1C	None		RW1C
HW Access	None			A	A	None		A
Name	None [7:5]			RESET_SOFT	RESET_PROT_FAULT	None [2:1]		RESET_WDT

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4	RESET_SOFT	Cortex-M0 requested a system reset through it's SYSRESETREQ. This can be done via a debugger probe or in firmware. Default Value: 0
3	RESET_PROT_FAULT	A protection violation occurred that requires a RESET. This includes, but is not limited to, hitting a debug breakpoint while in Privileged Mode. Default Value: 0
0	RESET_WDT	A WatchDog Timer reset has occurred since last power cycle. Default Value: 0

4.1.16 PWR_BG_TRIM1

Bandgap Trim Register

Address: 0x40030F00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		REF_VTRIM [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	REF_VTRIM	Trims the bandgap reference voltage output. Used to trim the VBG to the voltage where its temperature curvature is minimal. Bit [5] is unused within the bandgap block. Default Value: 16

4.1.17 PWR_BG_TRIM2

Bandgap Trim Register

Address: 0x40030F04

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		REF_ITRIM [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	REF_ITRIM	Trims the bandgap reference current output. Used to trim the IBG to the voltage where its temperature curvature is minimal. Default Value: 28

4.1.18 CLK_IMO_SELECT

IMO Frequency Select Register

Address: 0x40030F08

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW		
HW Access	None					R		
Name	None [7:3]					FREQ [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2 : 0	FREQ	Select operating frequency Default Value: 0 **0x0: 24_MHZ :** IMO runs at 24 MHz **0x1: 28_MHZ :** IMO runs at 28 MHz **0x2: 32_MHZ :** IMO runs at 32 MHz **0x3: 36_MHZ :** IMO runs at 36 MHz

4.1.18 CLK_IMO_SELECT (continued)

0x4: 40_MHZ :

IMO runs at 40 MHz

0x5: 44_MHZ :

IMO runs at 44 MHz

0x6: 48_MHZ :

IMO runs at 48 MHz

4.1.19 CLK_IMO_TRIM1

IMO Trim Register

Address: 0x40030F0C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	OFFSET [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. This field is hardware updated during USB osclock mode. This field is mapped to the most significant bits of the IMO trim imo_clk_trim[10:3]. The step size of 1 LSB on this field is approximately 120 kHz. Default Value: 128

4.1.20 CLK_IMO_TRIM2

IMO Trim Register

Address: 0x40030F10

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW		
HW Access	None					RW		
Name	None [7:3]					FSOFFSET [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2 : 0	FSOFFSET	Frequency trim bits. These bits are not trimmed during manufacturing and kept at 0 under normal operation. This field is hardware updated during USB osclock mode. This field is mapped to the least significant bits of the IMO trim imo_clk_trim[2:0]. The step size of 1 LSB on this field is approximately 15 kHz. Default Value: 0

4.1.21 PWR_PWRSYS_TRIM1

Power System Trim Register

Address: 0x40030F14

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	SPARE_TRIM [7:4]				DPSLP_REF_TRIM [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	SPARE_TRIM	Active-Reference temperature compensation trim (repurposed from spare bits). Bits [7:6] - trim the Active-Reference IREF temperature coefficient (TC). 00: TC = 0 (unchanged) 01: TC = +80ppm/C 10: TC = -80ppm/C 11: TC = -150ppm/C Bits [5:4] - trim the Active-Reference VREF temperature coefficient (TC). 00: TC = 0 (unchanged) 01: TC = -50ppm/C 10: TC = -80ppm/C 11: TC = +150ppm/C Default Value: 0
3 : 0	DPSLP_REF_TRIM	Trims the DeepSleep reference that is used by the DeepSleep regulator and DeepSleep power comparator. Default Value: 0

4.1.22 CLK_IMO_TRIM3

IMO Trim Register

Address: 0x40030F18

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW		RW				
HW Access	None	R		R				
Name	None	TCTRIM [6:5]		STEPSIZE [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
6 : 5	TCTRIM	IMO temperature compesation trim. These bits are determined at manufacturing time to adjust for temperature dependence. This bits are dependent on frequency and need to be changed using the Cypress provided frequency change algorithm. Default Value: 2
4 : 0	STEPSIZE	IMO trim stepsize bits. These bits are determined at manufacturing time to adjust for process variation. They are used to tune the stepsize of the FSOFFSET and OFFSET trims. Default Value: 16

5 General Purpose IO (GPIO) Registers

This section discusses the GPIO registers. It lists all the registers in mapping tables, in address order.

5.1 Register Details

Register	Address	Description
GPIO_PRT0_DR	0x40040000	Port output data register
GPIO_PRT0_PS	0x40040004	Port IO pad state register
GPIO_PRT0_PC	0x40040008	Port configuration register
GPIO_PRT0_INTR_CFG	0x4004000C	Port interrupt configuration register
GPIO_PRT0_INTR	0x40040010	Port interrupt status register
GPIO_PRT0_PC2	0x40040018	Port configuration register 2
GPIO_PRT0_DR_SET	0x40040040	Port output data set register
GPIO_PRT0_DR_CLR	0x40040044	Port output data clear register
GPIO_PRT0_DR_INV	0x40040048	Port output data invert register
GPIO_PRT1_DR	0x40040100	Port output data register. See GPIO_PRT0_DR for the details of bit fields.
GPIO_PRT1_PS	0x40040104	Port IO pad state register. See GPIO_PRT0_PS for the details of bit fields.
GPIO_PRT1_PC	0x40040108	Port configuration register. See GPIO_PRT0_PC for the details of bit fields.
GPIO_PRT1_INTR_CFG	0x4004010C	Port interrupt configuration register. See GPIO_PRT0_INTR_CFG for the details of bit fields.
GPIO_PRT1_INTR	0x40040110	Port interrupt status register. See GPIO_PRT0_INTR for the details of bit fields.
GPIO_PRT1_PC2	0x40040118	Port configuration register 2. See GPIO_PRT0_PC2 for the details of bit fields.
GPIO_PRT1_DR_SET	0x40040140	Port output data set register. See GPIO_PRT0_DR_SET for the details of bit fields.
GPIO_PRT1_DR_CLR	0x40040144	Port output data clear register. See GPIO_PRT0_DR_CLR for the details of bit fields.
GPIO_PRT1_DR_INV	0x40040148	Port output data invert register. See GPIO_PRT0_DR_INV for the details of bit fields.
GPIO_PRT2_DR	0x40040200	Port output data register. See GPIO_PRT0_DR for the details of bit fields.
GPIO_PRT2_PS	0x40040204	Port IO pad state register. See GPIO_PRT0_PS for the details of bit fields.
GPIO_PRT2_PC	0x40040208	Port configuration register. See GPIO_PRT0_PC for the details of bit fields.
GPIO_PRT2_INTR_CFG	0x4004020C	Port interrupt configuration register. See GPIO_PRT0_INTR_CFG for the details of bit fields.
GPIO_PRT2_INTR	0x40040210	Port interrupt status register. See GPIO_PRT0_INTR for the details of bit fields.
GPIO_PRT2_PC2	0x40040218	Port configuration register 2. See GPIO_PRT0_PC2 for the details of bit fields.
GPIO_PRT2_DR_SET	0x40040240	Port output data set register. See GPIO_PRT0_DR_SET for the details of bit fields.
GPIO_PRT2_DR_CLR	0x40040244	Port output data clear register. See GPIO_PRT0_DR_CLR for the details of bit fields.
GPIO_PRT2_DR_INV	0x40040248	Port output data invert register. See GPIO_PRT0_DR_INV for the details of bit fields.

Register	Address	Description
GPIO_PRT3_DR	0x40040300	Port output data register. See GPIO_PRT0_DR for the details of bit fields.
GPIO_PRT3_PS	0x40040304	Port IO pad state register. See GPIO_PRT0_PS for the details of bit fields.
GPIO_PRT3_PC	0x40040308	Port configuration register. See GPIO_PRT0_PC for the details of bit fields.
GPIO_PRT3_INTR_CFG	0x4004030C	Port interrupt configuration register. See GPIO_PRT0_INTR_CFG for the details of bit fields.
GPIO_PRT3_INTR	0x40040310	Port interrupt status register. See GPIO_PRT0_INTR for the details of bit fields.
GPIO_PRT3_PC2	0x40040318	Port configuration register 2. See GPIO_PRT0_PC2 for the details of bit fields.
GPIO_PRT3_DR_SET	0x40040340	Port output data set register. See GPIO_PRT0_DR_SET for the details of bit fields.
GPIO_PRT3_DR_CLR	0x40040344	Port output data clear register. See GPIO_PRT0_DR_CLR for the details of bit fields.
GPIO_PRT3_DR_INV	0x40040348	Port output data invert register. See GPIO_PRT0_DR_INV for the details of bit fields.
GPIO_PRT4_DR	0x40040400	Port output data register. See GPIO_PRT0_DR for the details of bit fields.
GPIO_PRT4_PS	0x40040404	Port IO pad state register. See GPIO_PRT0_PS for the details of bit fields.
GPIO_PRT4_PC	0x40040408	Port configuration register. See GPIO_PRT0_PC for the details of bit fields.
GPIO_PRT4_INTR_CFG	0x4004040C	Port interrupt configuration register. See GPIO_PRT0_INTR_CFG for the details of bit fields.
GPIO_PRT4_INTR	0x40040410	Port interrupt status register. See GPIO_PRT0_INTR for the details of bit fields.
GPIO_PRT4_PC2	0x40040418	Port configuration register 2. See GPIO_PRT0_PC2 for the details of bit fields.
GPIO_PRT4_DR_SET	0x40040440	Port output data set register. See GPIO_PRT0_DR_SET for the details of bit fields.
GPIO_PRT4_DR_CLR	0x40040444	Port output data clear register. See GPIO_PRT0_DR_CLR for the details of bit fields.
GPIO_PRT4_DR_INV	0x40040448	Port output data invert register. See GPIO_PRT0_DR_INV for the details of bit fields.
GPIO_PRT5_DR	0x40040500	Port output data register. See GPIO_PRT0_DR for the details of bit fields.
GPIO_PRT5_PS	0x40040504	Port IO pad state register. See GPIO_PRT0_PS for the details of bit fields.
GPIO_PRT5_PC	0x40040508	Port configuration register. See GPIO_PRT0_PC for the details of bit fields.
GPIO_PRT5_INTR_CFG	0x4004050C	Port interrupt configuration register. See GPIO_PRT0_INTR_CFG for the details of bit fields.
GPIO_PRT5_INTR	0x40040510	Port interrupt status register. See GPIO_PRT0_INTR for the details of bit fields.
GPIO_PRT5_PC2	0x40040518	Port configuration register 2. See GPIO_PRT0_PC2 for the details of bit fields.
GPIO_PRT5_DR_SET	0x40040540	Port output data set register. See GPIO_PRT0_DR_SET for the details of bit fields.
GPIO_PRT5_DR_CLR	0x40040544	Port output data clear register. See GPIO_PRT0_DR_CLR for the details of bit fields.
GPIO_PRT5_DR_INV	0x40040548	Port output data invert register. See GPIO_PRT0_DR_INV for the details of bit fields.
GPIO_PRT6_DR	0x40040600	Port output data register
GPIO_PRT6_PS	0x40040604	Port IO pad state register
GPIO_PRT6_PC	0x40040608	Port configuration register
GPIO_PRT6_INTR_CFG	0x4004060C	Port interrupt configuration register
GPIO_PRT6_INTR	0x40040610	Port interrupt status register
GPIO_PRT6_PC2	0x40040618	Port configuration register 2
GPIO_PRT6_DR_SET	0x40040640	Port output data set register. See GPIO_PRT0_DR_SET for the details of bit fields.
GPIO_PRT6_DR_CLR	0x40040644	Port output data clear register. See GPIO_PRT0_DR_CLR for the details of bit fields.
GPIO_PRT6_DR_INV	0x40040648	Port output data invert register. See GPIO_PRT0_DR_INV for the details of bit fields.
GPIO_PRT7_DR	0x40040700	Port output data register. See GPIO_PRT0_DR for the details of bit fields.
GPIO_PRT7_PS	0x40040704	Port IO pad state register. See GPIO_PRT0_PS for the details of bit fields.
GPIO_PRT7_PC	0x40040708	Port configuration register. See GPIO_PRT0_PC for the details of bit fields.
GPIO_PRT7_INTR_CFG	0x4004070C	Port interrupt configuration register. See GPIO_PRT0_INTR_CFG for the details of bit fields.
GPIO_PRT7_INTR	0x40040710	Port interrupt status register. See GPIO_PRT0_INTR for the details of bit fields.
GPIO_PRT7_PC2	0x40040718	Port configuration register 2. See GPIO_PRT0_PC2 for the details of bit fields.

Register	Address	Description
GPIO_PRT7_DR_SET	0x40040740	Port output data set register. See GPIO_PRT0_DR_SET for the details of bit fields.
GPIO_PRT7_DR_CLR	0x40040744	Port output data clear register. See GPIO_PRT0_DR_CLR for the details of bit fields.
GPIO_PRT7_DR_INV	0x40040748	Port output data invert register. See GPIO_PRT0_DR_INV for the details of bit fields.
GPIO_PRT8_DR	0x40040800	Port output data register
GPIO_PRT8_PS	0x40040804	Port IO pad state register
GPIO_PRT8_PC	0x40040808	Port configuration register
GPIO_PRT8_INTR_CFG	0x4004080C	Port interrupt configuration register
GPIO_PRT8_INTR	0x40040810	Port interrupt status register
GPIO_PRT8_PC2	0x40040818	Port configuration register 2
GPIO_PRT8_DR_SET	0x40040840	Port output data set register. See GPIO_PRT0_DR_SET for the details of bit fields.
GPIO_PRT8_DR_CLR	0x40040844	Port output data clear register. See GPIO_PRT0_DR_CLR for the details of bit fields.
GPIO_PRT8_DR_INV	0x40040848	Port output data invert register. See GPIO_PRT0_DR_INV for the details of bit fields.
GPIO_PRT9_DR	0x40040900	Port output data register. See GPIO_PRT8_DR for the details of bit fields.
GPIO_PRT9_PS	0x40040904	Port IO pad state register. See GPIO_PRT8_PS for the details of bit fields.
GPIO_PRT9_PC	0x40040908	Port configuration register. See GPIO_PRT8_PC for the details of bit fields.
GPIO_PRT9_INTR_CFG	0x4004090C	Port interrupt configuration register. See GPIO_PRT8_INTR_CFG for the details of bit fields.
GPIO_PRT9_INTR	0x40040910	Port interrupt status register. See GPIO_PRT8_INTR for the details of bit fields.
GPIO_PRT9_PC2	0x40040918	Port configuration register 2. See GPIO_PRT8_PC2 for the details of bit fields.
GPIO_PRT9_DR_SET	0x40040940	Port output data set register. See GPIO_PRT0_DR_SET for the details of bit fields.
GPIO_PRT9_DR_CLR	0x40040944	Port output data clear register. See GPIO_PRT0_DR_CLR for the details of bit fields.
GPIO_PRT9_DR_INV	0x40040948	Port output data invert register. See GPIO_PRT0_DR_INV for the details of bit fields.
GPIO_PRT10_DR	0x40040A00	Port output data register. See GPIO_PRT6_DR for the details of bit fields.
GPIO_PRT10_PS	0x40040A04	Port IO pad state register. See GPIO_PRT6_PS for the details of bit fields.
GPIO_PRT10_PC	0x40040A08	Port configuration register. See GPIO_PRT6_PC for the details of bit fields.
GPIO_PRT10_INTR_CFG	0x40040A0C	Port interrupt configuration register. See GPIO_PRT6_INTR_CFG for the details of bit fields.
GPIO_PRT10_INTR	0x40040A10	Port interrupt status register. See GPIO_PRT6_INTR for the details of bit fields.
GPIO_PRT10_PC2	0x40040A18	Port configuration register 2. See GPIO_PRT6_PC2 for the details of bit fields.
GPIO_PRT10_DR_SET	0x40040A40	Port output data set register. See GPIO_PRT0_DR_SET for the details of bit fields.
GPIO_PRT10_DR_CLR	0x40040A44	Port output data clear register. See GPIO_PRT0_DR_CLR for the details of bit fields.
GPIO_PRT10_DR_INV	0x40040A48	Port output data invert register. See GPIO_PRT0_DR_INV for the details of bit fields.
GPIO_PRT11_DR	0x40040B00	Port output data register. See GPIO_PRT6_DR for the details of bit fields.
GPIO_PRT11_PS	0x40040B04	Port IO pad state register. See GPIO_PRT6_PS for the details of bit fields.
GPIO_PRT11_PC	0x40040B08	Port configuration register. See GPIO_PRT6_PC for the details of bit fields.
GPIO_PRT11_INTR_CFG	0x40040B0C	Port interrupt configuration register. See GPIO_PRT6_INTR_CFG for the details of bit fields.
GPIO_PRT11_INTR	0x40040B10	Port interrupt status register. See GPIO_PRT6_INTR for the details of bit fields.
GPIO_PRT11_PC2	0x40040B18	Port configuration register 2. See GPIO_PRT6_PC2 for the details of bit fields.
GPIO_PRT11_DR_SET	0x40040B40	Port output data set register. See GPIO_PRT0_DR_SET for the details of bit fields.
GPIO_PRT11_DR_CLR	0x40040B44	Port output data clear register. See GPIO_PRT0_DR_CLR for the details of bit fields.
GPIO_PRT11_DR_INV	0x40040B48	Port output data invert register. See GPIO_PRT0_DR_INV for the details of bit fields.
GPIO_PRT12_DR	0x40040C00	Port output data register
GPIO_PRT12_PS	0x40040C04	Port IO pad state register
GPIO_PRT12_PC	0x40040C08	Port configuration register

Register	Address	Description
GPIO_PRT12_INTR_CFG	0x40040C0C	Port interrupt configuration register
GPIO_PRT12_INTR	0x40040C10	Port interrupt status register
GPIO_PRT12_PC2	0x40040C18	Port configuration register 2
GPIO_PRT12_DR_SET	0x40040C40	Port output data set register. See GPIO_PRT0_DR_SET for the details of bit fields.
GPIO_PRT12_DR_CLR	0x40040C44	Port output data clear register. See GPIO_PRT0_DR_CLR for the details of bit fields.
GPIO_PRT12_DR_INV	0x40040C48	Port output data invert register. See GPIO_PRT0_DR_INV for the details of bit fields.
GPIO_INTR_CAUSE	0x40041000	Interrupt port cause register

5.1.1 GPIO_PRT0_DR

Port output data register

Address: 0x40040000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	DATA7	IO pad 7 output data. Default Value: 0
6	DATA6	IO pad 6 output data. Default Value: 0
5	DATA5	IO pad 5 output data. Default Value: 0
4	DATA4	IO pad 4 output data. Default Value: 0
3	DATA3	IO pad 3 output data. Default Value: 0
2	DATA2	IO pad 2 output data. Default Value: 0
1	DATA1	IO pad 1 output data. Default Value: 0
0	DATA0	IO pad 0 output data. Default Value: 0

5.1.2 GPIO_PRT0_PS

Port IO pad state register

Address: 0x40040004

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							FLT_DATA

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_DATA	Reads of this register return the logical state of the filtered pin. Default Value: 0
7	DATA7	IO pad 7 state. Default Value: 0
6	DATA6	IO pad 6 state. Default Value: 0
5	DATA5	IO pad 5 state. Default Value: 0
4	DATA4	IO pad 4 state. Default Value: 0
3	DATA3	IO pad 3 state. Default Value: 0
2	DATA2	IO pad 2 state. Default Value: 0
1	DATA1	IO pad 1 state. Default Value: 0

5.1.2 GPIO_PRT0_PS (continued)

0	DATA0	IO pad 0 state: 1: Logic high, if the pin voltage is above the input buffer threshold, logic high. 0: Logic low, if the pin voltage is below that threshold, logic low. If the drive mode for the pin is set to high Z Analog, the pin state will read 0 independent of the voltage on the pin. Default Value: 0

5.1.3 GPIO_PRT0_PC

Port configuration register

Address: 0x40040008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW			RW		
HW Access	R		R			R		
Name	DM2 [7:6]		DM1 [5:3]			DM0 [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW			RW			RW
HW Access	R	R			R			R
Name	DM5	DM4 [14:12]			DM3 [11:9]			DM2

Bits	23	22	21	20	19	18	17	16
SW Access	RW			RW			RW	
HW Access	R			R			R	
Name	DM7 [23:21]			DM6 [20:18]			DM5 [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None				RW	RW
HW Access	R		None				R	R
Name	PORT_IB_MODE_SEL [31:30]		None [29:26]				PORT_SLOW	PORT_VTRIP_SEL

Bits	Name	Description
31 : 30	PORT_IB_MODE_SEL	This field selects the input buffer reference. The size (1 or 2 bits) and functionality is dependent on the IO cell. For GPIOv2 IO cells, bit PORT_IB_MODE_SEL[1] is not used (GPIOv2 IO cell replaces GPIO IO cell): "0"/"2": CMOS input buffer (PORT_VTRIP_SEL is '0'), LVTTL input buffer (PORT_VTRIP_SEL is '1') "1"/"3": vcchib. For GPIO_OVTv2 and SIOv2 IO cells: "0": CMOS input buffer (PORT_VTRIP_SEL is '0'), LVTTL input buffer (PORT_VTRIP_SEL is '1') "1": vcchib. "2": OVT. "3": Reference (possibly from reference generator cell). For SIO IO cell, this field is present but not used as the SIO IO cell does not provide input buffer mode select functionality (SIOv2 IO cell will replace SIO IO cell, as soon as it is available). For GPIOV1P2 and GPIOV1P2_I2C cells, PC.PORT_IB_MODE_SEL unused. Refer to DS register. Default Value: 0

5.1.3 GPIO_PRT0_PC (continued)

25	PORT_SLOW	This field controls the output edge rate of all pins on the port: '0': fast. '1': slow. Default Value: 0
24	PORT_VTRIP_SEL	The GPIO cells include a VTRIP_SEL signal to alter the input buffer voltage. Note: this bit is ignored for SIO ports, the VTRIP_SEL settings in the SIO register are used instead (a separate VTRIP_SEL is provided for each pin pair). 0: input buffer functions as a CMOS input buffer. 1: input buffer functions as a LVTTL input buffer. For GPIOV1P2 and GPIOV1P_I2C cells, PC.PORT_VTRIP_SEL is unused. Refer to DS register Default Value: 0
23 : 21	DM7	The GPIO drive mode for IO pad 7. Default Value: 0
20 : 18	DM6	The GPIO drive mode for IO pad 6. Default Value: 0
17 : 15	DM5	The GPIO drive mode for IO pad 5. Default Value: 0
14 : 12	DM4	The GPIO drive mode for IO pad 4. Default Value: 0
11 : 9	DM3	The GPIO drive mode for IO pad 3. Default Value: 0
8 : 6	DM2	The GPIO drive mode for IO pad 2. Default Value: 0
5 : 3	DM1	The GPIO drive mode for IO pad 1. Default Value: 0
2 : 0	DM0	The GPIO drive mode for IO pad 0. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the HSIOM is properly configured (HSIOM_PRT_SELx) before turning the IO on here to avoid producing glitches on the bus. Default Value: 0 **0x0: OFF :** Mode 0 (analog mode): Output buffer off (high Z). Input buffer off. **0x1: INPUT :** Mode 1: Output buffer off (high Z). Input buffer on. **0x2: 0_PU :** Mode 2: Strong pull down ('0'), weak/resistive pull up (PU). Input buffer on. For GPIOV1P2_I2C, Strong pull down only. **0x3: PD_1 :** Mode 3: Weak/resistive pull down (PD), strong pull up ('1'). Input buffer on. For GPIOV1P2_I2C: Weak pull down only.

5.1.3 GPIO_PRT0_PC (continued)

0x4: 0_Z :

Mode 4: Strong pull down ('0'), open drain (pull up off). Input buffer on.
For GPIOV1P2_I2C, Strong pull down only.

0x5: Z_1 :

Mode 5: Open drain (pull down off), strong pull up ('1'). Input buffer on.
Illegal for GPIOV1P2_I2C

0x6: 0_1 :

Mode 6: Strong pull down ('0'), strong pull up ('1'). Input buffer on.
For GPIOV1P2_I2C, Strong pull down only.

0x7: PD_PU :

Mode 7: Weak/resistive pull down (PD), weak/resistive pull up (PU). Input buffer on.
For GPIOV1P2_I2C: Weak pull down only.

5.1.4 GPIO_PRT0_INTR_CFG

Port interrupt configuration register

Address: 0x4004000C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	EDGE3_SEL [7:6]		EDGE2_SEL [5:4]		EDGE1_SEL [3:2]		EDGE0_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	EDGE7_SEL [15:14]		EDGE6_SEL [13:12]		EDGE5_SEL [11:10]		EDGE4_SEL [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW			RW	
HW Access	None			R			R	
Name	None [23:21]			FLT_SEL [20:18]			FLT_EDGE_SEL [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
20 : 18	FLT_SEL	Selects which pin is routed through the 50ns glitch filter to provide a glitch-safe interrupt. Default Value: 0
17 : 16	FLT_EDGE_SEL	Same for the glitch filtered pin (selected by FLT_SELECT). Default Value: 0 **0x0: DISABLE :** Disabled **0x1: RISING :** Rising edge **0x2: FALLING :** Falling edge

5.1.4 GPIO_PRT0_INTR_CFG (continued)

		0x3: BOTH : Both rising and falling edges
15 : 14	EDGE7_SEL	Sets which edge will trigger an IRQ for IO pad 7. Default Value: 0
13 : 12	EDGE6_SEL	Sets which edge will trigger an IRQ for IO pad 6. Default Value: 0
11 : 10	EDGE5_SEL	Sets which edge will trigger an IRQ for IO pad 5. Default Value: 0
9 : 8	EDGE4_SEL	Sets which edge will trigger an IRQ for IO pad 4. Default Value: 0
7 : 6	EDGE3_SEL	Sets which edge will trigger an IRQ for IO pad 3. Default Value: 0
5 : 4	EDGE2_SEL	Sets which edge will trigger an IRQ for IO pad 2. Default Value: 0
3 : 2	EDGE1_SEL	Sets which edge will trigger an IRQ for IO pad 1. Default Value: 0
1 : 0	EDGE0_SEL	Sets which edge will trigger an IRQ for IO pad 0. Default Value: 0
		0x0: DISABLE : Disabled **0x1: RISING :** Rising edge **0x2: FALLING :** Falling edge **0x3: BOTH :** Both rising and falling edges

5.1.5 GPIO_PRT0_INTR

Port interrupt status register

Address: 0x40040010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	A	A	A	A	A	A	A	A
Name	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1C
HW Access	None							A
Name	None [15:9]							FLT_DATA

Bits	23	22	21	20	19	18	17	16
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	PS_DATA7	PS_DATA6	PS_DATA5	PS_DATA4	PS_DATA3	PS_DATA2	PS_DATA1	PS_DATA0

Bits	31	30	29	28	27	26	25	24
SW Access	None							R
HW Access	None							W
Name	None [31:25]							PS_FLT_-DATA

Bits	Name	Description
24	PS_FLT_DATA	This is a duplicate of the contents of the PS register, provided here to allow reading of both pin state and interrupt state of the port in a single read operation. Default Value: 0
23	PS_DATA7	Default Value: 0
22	PS_DATA6	Default Value: 0
21	PS_DATA5	Default Value: 0
20	PS_DATA4	Default Value: 0
19	PS_DATA3	Default Value: 0
18	PS_DATA2	Default Value: 0
17	PS_DATA1	Default Value: 0
16	PS_DATA0	` Default Value: 0
8	FLT_DATA	Deglitched interrupt pending (selected by FLT_SELECT). Default Value: 0

5.1.5 GPIO_PRT0_INTR (continued)

7	DATA7	Interrupt pending on IO pad 7. Firmware writes 1 to clear the interrupt. Default Value: 0
6	DATA6	Interrupt pending on IO pad 6. Firmware writes 1 to clear the interrupt. Default Value: 0
5	DATA5	Interrupt pending on IO pad 5. Firmware writes 1 to clear the interrupt. Default Value: 0
4	DATA4	Interrupt pending on IO pad 4. Firmware writes 1 to clear the interrupt. Default Value: 0
3	DATA3	Interrupt pending on IO pad 3. Firmware writes 1 to clear the interrupt. Default Value: 0
2	DATA2	Interrupt pending on IO pad 2. Firmware writes 1 to clear the interrupt. Default Value: 0
1	DATA1	Interrupt pending on IO pad 1. Firmware writes 1 to clear the interrupt. Default Value: 0
0	DATA0	Interrupt pending on IO pad 0. Firmware writes 1 to clear the interrupt. Default Value: 0

5.1.6 GPIO_PRT0_PC2

Port configuration register 2

Address: 0x40040018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	INP_DIS7	INP_DIS6	INP_DIS5	INP_DIS4	INP_DIS3	INP_DIS2	INP_DIS1	INP_DIS0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	INP_DIS7	Disables the input buffer for IO pad 7. Default Value: 0
6	INP_DIS6	Disables the input buffer for IO pad 6. Default Value: 0
5	INP_DIS5	Disables the input buffer for IO pad 5. Default Value: 0
4	INP_DIS4	Disables the input buffer for IO pad 4. Default Value: 0
3	INP_DIS3	Disables the input buffer for IO pad 3. Default Value: 0
2	INP_DIS2	Disables the input buffer for IO pad 2. Default Value: 0
1	INP_DIS1	Disables the input buffer for IO pad 1. Default Value: 0

5.1.6 GPIO_PRT0_PC2 (continued)

0	INP_DIS0	Disables the input buffer for IO pad 0 independent of the port control drive mode (PC.DM). This bit should be set when analog signals are present on the pin and PC.DM != 0 is required to use the output driver. Default Value: 0

5.1.7 GPIO_PRT0_DR_SET

Port output data set register

Address: 0x40040040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	IO pad i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] set to '1'. Default Value: 0

5.1.8 GPIO_PRT0_DR_CLR

Port output data clear register

Address: 0x40040044

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	IO pad i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] set to '0'. Default Value: 0

5.1.9 GPIO_PRT0_DR_INV

Port output data invert register

Address: 0x40040048

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	IO pad i: '0': Output state DR.DATA[i] not affected. '1': Output state DR.DATA[i] inverted ('0' => '1', '1' => '0'). Default Value: 0

5.1.10 GPIO_PRT6_DR

Port output data register

Address: 0x40040600

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		RW	RW	RW	RW	RW	RW
Name	None [7:6]		DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	DATA5	IO pad 5 output data. Default Value: 0
4	DATA4	IO pad 4 output data. Default Value: 0
3	DATA3	IO pad 3 output data. Default Value: 0
2	DATA2	IO pad 2 output data. Default Value: 0
1	DATA1	IO pad 1 output data. Default Value: 0
0	DATA0	IO pad 0 output data. Default Value: 0

5.1.11 GPIO_PRT6_PS

Port IO pad state register

Address: 0x40040604

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R	R	R	R	R	R
HW Access	None		W	W	W	W	W	W
Name	None [7:6]		DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							FLT_DATA

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_DATA	Reads of this register return the logical state of the filtered pin. Default Value: 0
5	DATA5	IO pad 5 state. Default Value: 0
4	DATA4	IO pad 4 state. Default Value: 0
3	DATA3	IO pad 3 state. Default Value: 0
2	DATA2	IO pad 2 state. Default Value: 0
1	DATA1	IO pad 1 state. Default Value: 0

5.1.11 GPIO_PRT6_PS (continued)

0	DATA0	IO pad 0 state: 1: Logic high, if the pin voltage is above the input buffer threshold, logic high. 0: Logic low, if the pin voltage is below that threshold, logic low. If the drive mode for the pin is set to high Z Analog, the pin state will read 0 independent of the voltage on the pin. Default Value: 0

5.1.12 GPIO_PRT6_PC

Port configuration register

Address: 0x40040608

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW			RW		
HW Access	R		R			R		
Name	DM2 [7:6]		DM1 [5:3]			DM0 [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW			RW			RW
HW Access	R	R			R			R
Name	DM5	DM4 [14:12]			DM3 [11:9]			DM2

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	
HW Access	None						R	
Name	None [23:18]						DM5 [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None				RW	RW
HW Access	R		None				R	R
Name	PORT_IB_MODE_SEL [31:30]		None [29:26]				PORT_SLOW	PORT_VTRIP_SEL

Bits	Name	Description
31 : 30	PORT_IB_MODE_SEL	This field selects the input buffer reference. The size (1 or 2 bits) and functionality is dependent on the IO cell. For GPIOv2 IO cells, bit PORT_IB_MODE_SEL[1] is not used (GPIOv2 IO cell replaces GPIO IO cell): "0"/"2": CMOS input buffer (PORT_VTRIP_SEL is '0'), LVTTL input buffer (PORT_VTRIP_SEL is '1') "1"/"3": vcchib. For GPIO_OVTv2 and SIOv2 IO cells: "0": CMOS input buffer (PORT_VTRIP_SEL is '0'), LVTTL input buffer (PORT_VTRIP_SEL is '1') "1": vcchib. "2": OVT. "3": Reference (possibly from reference generator cell). For SIO IO cell, this field is present but not used as the SIO IO cell does not provide input buffer mode select functionality (SIOv2 IO cell will replace SIO IO cell, as soon as it is available). For GPIOV1P2 and GPIOV1P2_I2C cells, PC.PORT_IB_MODE_SEL unused. Refer to DS register. Default Value: 0

5.1.12 GPIO_PRT6_PC (continued)

25	PORT_SLOW	This field controls the output edge rate of all pins on the port: '0': fast. '1': slow. Default Value: 0
24	PORT_VTRIP_SEL	The GPIO cells include a VTRIP_SEL signal to alter the input buffer voltage. Note: this bit is ignored for SIO ports, the VTRIP_SEL settings in the SIO register are used instead (a separate VTRIP_SEL is provided for each pin pair). 0: input buffer functions as a CMOS input buffer. 1: input buffer functions as a LVTTL input buffer. For GPIOV1P2 and GPIOV1P_I2C cells, PC.PORT_VTRIP_SEL is unused. Refer to DS register Default Value: 0
17 : 15	DM5	The GPIO drive mode for IO pad 5. Default Value: 0
14 : 12	DM4	The GPIO drive mode for IO pad 4. Default Value: 0
11 : 9	DM3	The GPIO drive mode for IO pad 3. Default Value: 0
8 : 6	DM2	The GPIO drive mode for IO pad 2. Default Value: 0
5 : 3	DM1	The GPIO drive mode for IO pad 1. Default Value: 0
2 : 0	DM0	The GPIO drive mode for IO pad 0. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the HSIOM is properly configured (HSIOM_PRT_SELx) before turning the IO on here to avoid producing glitches on the bus. Default Value: 0 **0x0: OFF :** Mode 0 (analog mode): Output buffer off (high Z). Input buffer off. **0x1: INPUT :** Mode 1: Output buffer off (high Z). Input buffer on. **0x2: 0_PU :** Mode 2: Strong pull down ('0'), weak/resistive pull up (PU). Input buffer on. For GPIOV1P2_I2C, Strong pull down only. **0x3: PD_1 :** Mode 3: Weak/resistive pull down (PD), strong pull up ('1'). Input buffer on. For GPIOV1P2_I2C: Weak pull down only. **0x4: 0_Z :** Mode 4: Strong pull down ('0'), open drain (pull up off). Input buffer on. For GPIOV1P2_I2C, Strong pull down only.

5.1.12 GPIO_PRT6_PC (continued)

0x5: Z_1 :

Mode 5: Open drain (pull down off), strong pull up ('1'). Input buffer on.
Illegal for GPIOV1P2_I2C

0x6: 0_1 :

Mode 6: Strong pull down ('0'), strong pull up ('1'). Input buffer on.
For GPIOV1P2_I2C, Strong pull down only.

0x7: PD_PU :

Mode 7: Weak/resistive pull down (PD), weak/resistive pull up (PU). Input buffer on.
For GPIOV1P2_I2C: Weak pull down only.

5.1.13 GPIO_PRT6_INTR_CFG

Port interrupt configuration register

Address: 0x4004060C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	EDGE3_SEL [7:6]		EDGE2_SEL [5:4]		EDGE1_SEL [3:2]		EDGE0_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW		RW	
HW Access	None				R		R	
Name	None [15:12]				EDGE5_SEL [11:10]		EDGE4_SEL [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW			RW	
HW Access	None			R			R	
Name	None [23:21]			FLT_SEL [20:18]			FLT_EDGE_SEL [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
20 : 18	FLT_SEL	Selects which pin is routed through the 50ns glitch filter to provide a glitch-safe interrupt. Default Value: 0
17 : 16	FLT_EDGE_SEL	Same for the glitch filtered pin (selected by FLT_SELECT). Default Value: 0 **0x0: DISABLE :** Disabled **0x1: RISING :** Rising edge **0x2: FALLING :** Falling edge

5.1.13 GPIO_PRT6_INTR_CFG (continued)

		0x3: BOTH : Both rising and falling edges
11 : 10	EDGE5_SEL	Sets which edge will trigger an IRQ for IO pad 5. Default Value: 0
9 : 8	EDGE4_SEL	Sets which edge will trigger an IRQ for IO pad 4. Default Value: 0
7 : 6	EDGE3_SEL	Sets which edge will trigger an IRQ for IO pad 3. Default Value: 0
5 : 4	EDGE2_SEL	Sets which edge will trigger an IRQ for IO pad 2. Default Value: 0
3 : 2	EDGE1_SEL	Sets which edge will trigger an IRQ for IO pad 1. Default Value: 0
1 : 0	EDGE0_SEL	Sets which edge will trigger an IRQ for IO pad 0. Default Value: 0
		0x0: DISABLE : Disabled **0x1: RISING :** Rising edge **0x2: FALLING :** Falling edge **0x3: BOTH :** Both rising and falling edges

5.1.14 GPIO_PRT6_INTR

Port interrupt status register

Address: 0x40040610

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	None		A	A	A	A	A	A
Name	None [7:6]		DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1C
HW Access	None							A
Name	None [15:9]							FLT_DATA

Bits	23	22	21	20	19	18	17	16
SW Access	None		R	R	R	R	R	R
HW Access	None		W	W	W	W	W	W
Name	None [23:22]		PS_DATA5	PS_DATA4	PS_DATA3	PS_DATA2	PS_DATA1	PS_DATA0

Bits	31	30	29	28	27	26	25	24
SW Access	None							R
HW Access	None							W
Name	None [31:25]							PS_FLT_-DATA

Bits	Name	Description
24	PS_FLT_DATA	This is a duplicate of the contents of the PS register, provided here to allow reading of both pin state and interrupt state of the port in a single read operation. Default Value: 0
21	PS_DATA5	Default Value: 0
20	PS_DATA4	Default Value: 0
19	PS_DATA3	Default Value: 0
18	PS_DATA2	Default Value: 0
17	PS_DATA1	Default Value: 0
16	PS_DATA0	` Default Value: 0
8	FLT_DATA	Deglitched interrupt pending (selected by FLT_SELECT). Default Value: 0
5	DATA5	Interrupt pending on IO pad 5. Firmware writes 1 to clear the interrupt. Default Value: 0

5.1.14 GPIO_PRT6_INTR (continued)

4	DATA4	Interrupt pending on IO pad 4. Firmware writes 1 to clear the interrupt. Default Value: 0
3	DATA3	Interrupt pending on IO pad 3. Firmware writes 1 to clear the interrupt. Default Value: 0
2	DATA2	Interrupt pending on IO pad 2. Firmware writes 1 to clear the interrupt. Default Value: 0
1	DATA1	Interrupt pending on IO pad 1. Firmware writes 1 to clear the interrupt. Default Value: 0
0	DATA0	Interrupt pending on IO pad 0. Firmware writes 1 to clear the interrupt. Default Value: 0

5.1.15 GPIO_PRT6_PC2

Port configuration register 2

Address: 0x40040618

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		R	R	R	R	R	R
Name	None [7:6]		INP_DIS5	INP_DIS4	INP_DIS3	INP_DIS2	INP_DIS1	INP_DIS0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	INP_DIS5	Disables the input buffer for IO pad 5. Default Value: 0
4	INP_DIS4	Disables the input buffer for IO pad 4. Default Value: 0
3	INP_DIS3	Disables the input buffer for IO pad 3. Default Value: 0
2	INP_DIS2	Disables the input buffer for IO pad 2. Default Value: 0
1	INP_DIS1	Disables the input buffer for IO pad 1. Default Value: 0
0	INP_DIS0	Disables the input buffer for IO pad 0 independent of the port control drive mode (PC.DM). This bit should be set when analog signals are present on the pin and PC.DM != 0 is required to use the output driver. Default Value: 0

5.1.16 GPIO_PRT8_DR

Port output data register

Address: 0x40040800

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				RW	RW	RW	RW
Name	None [7:4]				DATA3	DATA2	DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	DATA3	IO pad 3 output data. Default Value: 0
2	DATA2	IO pad 2 output data. Default Value: 0
1	DATA1	IO pad 1 output data. Default Value: 0
0	DATA0	IO pad 0 output data. Default Value: 0

5.1.17 GPIO_PRT8_PS

Port IO pad state register

Address: 0x40040804

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R	R	R	R
HW Access	None				W	W	W	W
Name	None [7:4]				DATA3	DATA2	DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							FLT_DATA

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_DATA	Reads of this register return the logical state of the filtered pin. Default Value: 0
3	DATA3	IO pad 3 state. Default Value: 0
2	DATA2	IO pad 2 state. Default Value: 0
1	DATA1	IO pad 1 state. Default Value: 0
0	DATA0	IO pad 0 state: 1: Logic high, if the pin voltage is above the input buffer threshold, logic high. 0: Logic low, if the pin voltage is below that threshold, logic low. If the drive mode for the pin is set to high Z Analog, the pin state will read 0 independent of the voltage on the pin. Default Value: 0

5.1.18 GPIO_PRT8_PC

Port configuration register

Address: 0x40040808

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW			RW		
HW Access	R		R			R		
Name	DM2 [7:6]		DM1 [5:3]			DM0 [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			RW
HW Access	None				R			R
Name	None [15:12]				DM3 [11:9]			DM2

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None				RW	RW
HW Access	R		None				R	R
Name	PORT_IB_MODE_SEL [31:30]		None [29:26]				PORT_SLOW	PORT_VTRIP_SEL

Bits	Name	Description
31 : 30	PORT_IB_MODE_SEL	This field selects the input buffer reference. The size (1 or 2 bits) and functionality is dependent on the IO cell. For GPIOv2 IO cells, bit PORT_IB_MODE_SEL[1] is not used (GPIOv2 IO cell replaces GPIO IO cell): "0"/"2": CMOS input buffer (PORT_VTRIP_SEL is '0'), LVTTL input buffer (PORT_VTRIP_SEL is '1') "1"/"3": vcchib. For GPIO_OVTv2 and SIOv2 IO cells: "0": CMOS input buffer (PORT_VTRIP_SEL is '0'), LVTTL input buffer (PORT_VTRIP_SEL is '1') "1": vcchib. "2": OVT. "3": Reference (possibly from reference generator cell). For SIO IO cell, this field is present but not used as the SIO IO cell does not provide input buffer mode select functionality (SIOv2 IO cell will replace SIO IO cell, as soon as it is available). For GPIOV1P2 and GPIOV1P2_I2C cells, PC.PORT_IB_MODE_SEL unused. Refer to DS register. Default Value: 0

5.1.18 GPIO_PRT8_PC (continued)

25	PORT_SLOW	This field controls the output edge rate of all pins on the port: '0': fast. '1': slow. Default Value: 0
24	PORT_VTRIP_SEL	The GPIO cells include a VTRIP_SEL signal to alter the input buffer voltage. Note: this bit is ignored for SIO ports, the VTRIP_SEL settings in the SIO register are used instead (a separate VTRIP_SEL is provided for each pin pair). 0: input buffer functions as a CMOS input buffer. 1: input buffer functions as a LVTTL input buffer. For GPIOV1P2 and GPIOV1P_I2C cells, PC.PORT_VTRIP_SEL is unused. Refer to DS register Default Value: 0
11 : 9	DM3	The GPIO drive mode for IO pad 3. Default Value: 0
8 : 6	DM2	The GPIO drive mode for IO pad 2. Default Value: 0
5 : 3	DM1	The GPIO drive mode for IO pad 1. Default Value: 0
2 : 0	DM0	The GPIO drive mode for IO pad 0. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the HSIOM is properly configured (HSIOM_PRT_SELx) before turning the IO on here to avoid producing glitches on the bus. Default Value: 0 **0x0: OFF :** Mode 0 (analog mode): Output buffer off (high Z). Input buffer off. **0x1: INPUT :** Mode 1: Output buffer off (high Z). Input buffer on. **0x2: 0_PU :** Mode 2: Strong pull down ('0'), weak/resistive pull up (PU). Input buffer on. For GPIOV1P2_I2C, Strong pull down only. **0x3: PD_1 :** Mode 3: Weak/resistive pull down (PD), strong pull up ('1'). Input buffer on. For GPIOV1P2_I2C: Weak pull down only. **0x4: 0_Z :** Mode 4: Strong pull down ('0'), open drain (pull up off). Input buffer on. For GPIOV1P2_I2C, Strong pull down only. **0x5: Z_1 :** Mode 5: Open drain (pull down off), strong pull up ('1'). Input buffer on. Illegal for GPIOV1P2_I2C

5.1.18 GPIO_PRT8_PC (continued)

0x6: 0_1 :

Mode 6: Strong pull down ('0'), strong pull up ('1'). Input buffer on.
For GPIOV1P2_I2C, Strong pull down only.

0x7: PD_PU :

Mode 7: Weak/resistive pull down (PD), weak/resistive pull up (PU). Input buffer on.
For GPIOV1P2_I2C: Weak pull down only.

5.1.19 GPIO_PRT8_INTR_CFG

Port interrupt configuration register

Address: 0x4004080C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	EDGE3_SEL [7:6]		EDGE2_SEL [5:4]		EDGE1_SEL [3:2]		EDGE0_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW			RW	
HW Access	None			R			R	
Name	None [23:21]			FLT_SEL [20:18]			FLT_EDGE_SEL [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
20 : 18	FLT_SEL	Selects which pin is routed through the 50ns glitch filter to provide a glitch-safe interrupt. Default Value: 0
17 : 16	FLT_EDGE_SEL	Same for the glitch filtered pin (selected by FLT_SELECT). Default Value: 0 **0x0: DISABLE :** Disabled **0x1: RISING :** Rising edge **0x2: FALLING :** Falling edge

5.1.19 GPIO_PRT8_INTR_CFG (continued)

		0x3: BOTH : Both rising and falling edges
7 : 6	EDGE3_SEL	Sets which edge will trigger an IRQ for IO pad 3. Default Value: 0
5 : 4	EDGE2_SEL	Sets which edge will trigger an IRQ for IO pad 2. Default Value: 0
3 : 2	EDGE1_SEL	Sets which edge will trigger an IRQ for IO pad 1. Default Value: 0
1 : 0	EDGE0_SEL	Sets which edge will trigger an IRQ for IO pad 0. Default Value: 0
		0x0: DISABLE : Disabled **0x1: RISING :** Rising edge **0x2: FALLING :** Falling edge **0x3: BOTH :** Both rising and falling edges

5.1.20 GPIO_PRT8_INTR

Port interrupt status register

Address: 0x40040810

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1C	RW1C	RW1C	RW1C
HW Access	None				A	A	A	A
Name	None [7:4]				DATA3	DATA2	DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1C
HW Access	None							A
Name	None [15:9]							FLT_DATA

Bits	23	22	21	20	19	18	17	16
SW Access	None				R	R	R	R
HW Access	None				W	W	W	W
Name	None [23:20]				PS_DATA3	PS_DATA2	PS_DATA1	PS_DATA0

Bits	31	30	29	28	27	26	25	24
SW Access	None							R
HW Access	None							W
Name	None [31:25]							PS_FLT_-DATA

Bits	Name	Description
24	PS_FLT_DATA	This is a duplicate of the contents of the PS register, provided here to allow reading of both pin state and interrupt state of the port in a single read operation. Default Value: 0
19	PS_DATA3	Default Value: 0
18	PS_DATA2	Default Value: 0
17	PS_DATA1	Default Value: 0
16	PS_DATA0	` Default Value: 0
8	FLT_DATA	Deglitched interrupt pending (selected by FLT_SELECT). Default Value: 0
3	DATA3	Interrupt pending on IO pad 3. Firmware writes 1 to clear the interrupt. Default Value: 0
2	DATA2	Interrupt pending on IO pad 2. Firmware writes 1 to clear the interrupt. Default Value: 0

5.1.20 GPIO_PRT8_INTR (continued)

1	DATA1	Interrupt pending on IO pad 1. Firmware writes 1 to clear the interrupt. Default Value: 0
0	DATA0	Interrupt pending on IO pad 0. Firmware writes 1 to clear the interrupt. Default Value: 0

5.1.21 GPIO_PRT8_PC2

Port configuration register 2

Address: 0x40040818

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [7:4]				INP_DIS3	INP_DIS2	INP_DIS1	INP_DIS0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	INP_DIS3	Disables the input buffer for IO pad 3. Default Value: 0
2	INP_DIS2	Disables the input buffer for IO pad 2. Default Value: 0
1	INP_DIS1	Disables the input buffer for IO pad 1. Default Value: 0
0	INP_DIS0	Disables the input buffer for IO pad 0 independent of the port control drive mode (PC.DM). This bit should be set when analog signals are present on the pin and PC.DM != 0 is required to use the output driver. Default Value: 0

5.1.22 GPIO_PRT12_DR

Port output data register

Address: 0x40040C00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						RW	RW
Name	None [7:2]						DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	DATA1	IO pad 1 output data. Default Value: 0
0	DATA0	IO pad 0 output data. Default Value: 0

5.1.23 GPIO_PRT12_PS

Port IO pad state register

Address: 0x40040C04

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						W	W
Name	None [7:2]						DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							FLT_DATA

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	FLT_DATA	Reads of this register return the logical state of the filtered pin. Default Value: 0
1	DATA1	IO pad 1 state. Default Value: 0
0	DATA0	IO pad 0 state: 1: Logic high, if the pin voltage is above the input buffer threshold, logic high. 0: Logic low, if the pin voltage is below that threshold, logic low. If the drive mode for the pin is set to high Z Analog, the pin state will read 0 independent of the voltage on the pin. Default Value: 0

5.1.24 GPIO_PRT12_PC

Port configuration register

Address: 0x40040C08

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW			RW		
HW Access	None		R			R		
Name	None [7:6]		DM1 [5:3]			DM0 [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None				RW	RW
HW Access	R		None				R	R
Name	PORT_IB_MODE_SEL [31:30]		None [29:26]				PORT_SLOW	PORT_VTRIP_SEL

Bits	Name	Description
31 : 30	PORT_IB_MODE_SEL	This field selects the input buffer reference. The size (1 or 2 bits) and functionality is dependent on the IO cell. For GPIOv2 IO cells, bit PORT_IB_MODE_SEL[1] is not used (GPIOv2 IO cell replaces GPIO IO cell): "0"/"2": CMOS input buffer (PORT_VTRIP_SEL is '0'), LVTTL input buffer (PORT_VTRIP_SEL is '1') "1"/"3": vcchib. For GPIO_OVTv2 and SIOv2 IO cells: "0": CMOS input buffer (PORT_VTRIP_SEL is '0'), LVTTL input buffer (PORT_VTRIP_SEL is '1') "1": vcchib. "2": OVT. "3": Reference (possibly from reference generator cell). For SIO IO cell, this field is present but not used as the SIO IO cell does not provide input buffer mode select functionality (SIOv2 IO cell will replace SIO IO cell, as soon as it is available). For GPIOV1P2 and GPIOV1P2_I2C cells, PC.PORT_IB_MODE_SEL unused. Refer to DS register. Default Value: 0

5.1.24 GPIO_PRT12_PC (continued)

25	PORT_SLOW	This field controls the output edge rate of all pins on the port: '0': fast. '1': slow. Default Value: 0
24	PORT_VTRIP_SEL	The GPIO cells include a VTRIP_SEL signal to alter the input buffer voltage. Note: this bit is ignored for SIO ports, the VTRIP_SEL settings in the SIO register are used instead (a separate VTRIP_SEL is provided for each pin pair). 0: input buffer functions as a CMOS input buffer. 1: input buffer functions as a LVTTL input buffer. For GPIOV1P2 and GPIOV1P_I2C cells, PC.PORT_VTRIP_SEL is unused. Refer to DS register Default Value: 0
5 : 3	DM1	The GPIO drive mode for IO pad 1. Default Value: 0
2 : 0	DM0	The GPIO drive mode for IO pad 0. Note: when initializing IO's that are connected to a live bus (such as I2C), make sure the HSIOM is properly configured (HSIOM_PRT_SELx) before turning the IO on here to avoid producing glitches on the bus. Default Value: 0 **0x0: OFF :** Mode 0 (analog mode): Output buffer off (high Z). Input buffer off. **0x1: INPUT :** Mode 1: Output buffer off (high Z). Input buffer on. **0x2: 0_PU :** Mode 2: Strong pull down ('0'), weak/resistive pull up (PU). Input buffer on. For GPIOV1P2_I2C, Strong pull down only. **0x3: PD_1 :** Mode 3: Weak/resistive pull down (PD), strong pull up ('1'). Input buffer on. For GPIOV1P2_I2C: Weak pull down only. **0x4: 0_Z :** Mode 4: Strong pull down ('0'), open drain (pull up off). Input buffer on. For GPIOV1P2_I2C, Strong pull down only. **0x5: Z_1 :** Mode 5: Open drain (pull down off), strong pull up ('1'). Input buffer on. Illegal for GPIOV1P2_I2C **0x6: 0_1 :** Mode 6: Strong pull down ('0'), strong pull up ('1'). Input buffer on. For GPIOV1P2_I2C, Strong pull down only.

5.1.24 GPIO_PRT12_PC (continued)

0x7: PD_PU :

Mode 7: Weak/resistive pull down (PD), weak/resistive pull up (PU). Input buffer on.
For GPIOV1P2_I2C: Weak pull down only.

5.1.25 GPIO_PRT12_INTR_CFG

Port interrupt configuration register

Address: 0x40040C0C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW		RW	
HW Access	None				R		R	
Name	None [7:4]				EDGE1_SEL [3:2]		EDGE0_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW			RW	
HW Access	None			R			R	
Name	None [23:21]			FLT_SEL [20:18]			FLT_EDGE_SEL [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
20 : 18	FLT_SEL	Selects which pin is routed through the 50ns glitch filter to provide a glitch-safe interrupt. Default Value: 0
17 : 16	FLT_EDGE_SEL	Same for the glitch filtered pin (selected by FLT_SELECT). Default Value: 0 **0x0: DISABLE :** Disabled **0x1: RISING :** Rising edge **0x2: FALLING :** Falling edge

5.1.25 GPIO_PRT12_INTR_CFG (continued)

		0x3: BOTH : Both rising and falling edges
3 : 2	EDGE1_SEL	Sets which edge will trigger an IRQ for IO pad 1. Default Value: 0
1 : 0	EDGE0_SEL	Sets which edge will trigger an IRQ for IO pad 0. Default Value: 0
		0x0: DISABLE : Disabled
		0x1: RISING : Rising edge
		0x2: FALLING : Falling edge
		0x3: BOTH : Both rising and falling edges

5.1.26 GPIO_PRT12_INTR

Port interrupt status register

Address: 0x40040C10

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1C	RW1C
HW Access	None						A	A
Name	None [7:2]						DATA1	DATA0

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1C
HW Access	None							A
Name	None [15:9]							FLT_DATA

Bits	23	22	21	20	19	18	17	16
SW Access	None						R	R
HW Access	None						W	W
Name	None [23:18]						PS_DATA1	PS_DATA0

Bits	31	30	29	28	27	26	25	24
SW Access	None							R
HW Access	None							W
Name	None [31:25]							PS_FLT_-DATA

Bits	Name	Description
24	PS_FLT_DATA	This is a duplicate of the contents of the PS register, provided here to allow reading of both pin state and interrupt state of the port in a single read operation. Default Value: 0
17	PS_DATA1	Default Value: 0
16	PS_DATA0	` Default Value: 0
8	FLT_DATA	Deglitched interrupt pending (selected by FLT_SELECT). Default Value: 0
1	DATA1	Interrupt pending on IO pad 1. Firmware writes 1 to clear the interrupt. Default Value: 0
0	DATA0	Interrupt pending on IO pad 0. Firmware writes 1 to clear the interrupt. Default Value: 0

5.1.27 GPIO_PRT12_PC2

Port configuration register 2

Address: 0x40040C18

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						INP_DIS1	INP_DIS0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	INP_DIS1	Disables the input buffer for IO pad 1. Default Value: 0
0	INP_DIS0	Disables the input buffer for IO pad 0 independent of the port control drive mode (PC.DM). This bit should be set when analog signals are present on the pin and PC.DM != 0 is required to use the output driver. Default Value: 0

5.1.28 GPIO_INTR_CAUSE

Interrupt port cause register

Address: 0x40041000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	PORT_INT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None			R				
HW Access	None			W				
Name	None [15:13]			PORT_INT [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
12 : 0	PORT_INT	Each IO port has an associated bit field in this register. The bit field reflects the IO port's interrupt line (bit field i reflects "gpio_interrupts[i]" for IO port i). The register is used when the system uses a shared/combined interrupt line "gpio_interrupt". The SW ISR reads the register to determine which IO port(s) is responsible for the shared/combined interrupt line "gpio_interrupt". Once, the IO port(s) is determined, the IO port's INTR register is read to determine the IO pad(s) in the IO port that caused the interrupt. Default Value: 0

6 Programmable IO (PRGIO) Registers

This section discusses the PRGIO registers. It lists all the registers in mapping tables, in address order.

6.1 Register Details

Register	Address	Description
PRGIO_PRT0_CTL	0x40050000	Control register
PRGIO_PRT0_SYNC_CTL	0x40050010	Synchronization control register
PRGIO_PRT0_LUT_SEL0	0x40050020	LUT component input selection
PRGIO_PRT0_LUT_SEL1	0x40050024	LUT component input selection. See PRGIO_PRT0_LUT_SEL0 for the details of bit fields.
PRGIO_PRT0_LUT_SEL2	0x40050028	LUT component input selection. See PRGIO_PRT0_LUT_SEL0 for the details of bit fields.
PRGIO_PRT0_LUT_SEL3	0x4005002C	LUT component input selection. See PRGIO_PRT0_LUT_SEL0 for the details of bit fields.
PRGIO_PRT0_LUT_SEL4	0x40050030	LUT component input selection. See PRGIO_PRT0_LUT_SEL0 for the details of bit fields.
PRGIO_PRT0_LUT_SEL5	0x40050034	LUT component input selection. See PRGIO_PRT0_LUT_SEL0 for the details of bit fields.
PRGIO_PRT0_LUT_SEL6	0x40050038	LUT component input selection. See PRGIO_PRT0_LUT_SEL0 for the details of bit fields.
PRGIO_PRT0_LUT_SEL7	0x4005003C	LUT component input selection. See PRGIO_PRT0_LUT_SEL0 for the details of bit fields.
PRGIO_PRT0_LUT_CTL0	0x40050040	LUT component control register
PRGIO_PRT0_LUT_CTL1	0x40050044	LUT component control register. See PRGIO_PRT0_LUT_CTL0 for the details of bit fields.
PRGIO_PRT0_LUT_CTL2	0x40050048	LUT component control register. See PRGIO_PRT0_LUT_CTL0 for the details of bit fields.
PRGIO_PRT0_LUT_CTL3	0x4005004C	LUT component control register. See PRGIO_PRT0_LUT_CTL0 for the details of bit fields.
PRGIO_PRT0_LUT_CTL4	0x40050050	LUT component control register. See PRGIO_PRT0_LUT_CTL0 for the details of bit fields.
PRGIO_PRT0_LUT_CTL5	0x40050054	LUT component control register. See PRGIO_PRT0_LUT_CTL0 for the details of bit fields.
PRGIO_PRT0_LUT_CTL6	0x40050058	LUT component control register. See PRGIO_PRT0_LUT_CTL0 for the details of bit fields.
PRGIO_PRT0_LUT_CTL7	0x4005005C	LUT component control register. See PRGIO_PRT0_LUT_CTL0 for the details of bit fields.
PRGIO_PRT0_DU_SEL	0x400500C0	Data unit component input selection
PRGIO_PRT0_DU_CTL	0x400500C4	Data unit component control register
PRGIO_PRT0_DATA	0x400500F0	Data register
PRGIO_PRT1_CTL	0x40050100	Control register. See PRGIO_PRT0_CTL for the details of bit fields.
PRGIO_PRT1_SYNC_CTL	0x40050110	Synchronization control register. See PRGIO_PRT0_SYNC_CTL for the details of bit fields.
PRGIO_PRT1_LUT_SEL0	0x40050120	LUT component input selection. See PRGIO_PRT0_LUT_SEL0 for the details of bit fields.
PRGIO_PRT1_LUT_SEL1	0x40050124	LUT component input selection. See PRGIO_PRT0_LUT_SEL0 for the details of bit fields.
PRGIO_PRT1_LUT_SEL2	0x40050128	LUT component input selection. See PRGIO_PRT0_LUT_SEL0 for the details of bit fields.
PRGIO_PRT1_LUT_SEL3	0x4005012C	LUT component input selection. See PRGIO_PRT0_LUT_SEL0 for the details of bit fields.

Register	Address	Description
PRGIO_PRT1_LUT_SEL4	0x40050130	LUT component input selection. See PRGIO_PRT0_LUT_SEL0 for the details of bit fields.
PRGIO_PRT1_LUT_SEL5	0x40050134	LUT component input selection. See PRGIO_PRT0_LUT_SEL0 for the details of bit fields.
PRGIO_PRT1_LUT_SEL6	0x40050138	LUT component input selection. See PRGIO_PRT0_LUT_SEL0 for the details of bit fields.
PRGIO_PRT1_LUT_SEL7	0x4005013C	LUT component input selection. See PRGIO_PRT0_LUT_SEL0 for the details of bit fields.
PRGIO_PRT1_LUT_CTL0	0x40050140	LUT component control register. See PRGIO_PRT0_LUT_CTL0 for the details of bit fields.
PRGIO_PRT1_LUT_CTL1	0x40050144	LUT component control register. See PRGIO_PRT0_LUT_CTL0 for the details of bit fields.
PRGIO_PRT1_LUT_CTL2	0x40050148	LUT component control register. See PRGIO_PRT0_LUT_CTL0 for the details of bit fields.
PRGIO_PRT1_LUT_CTL3	0x4005014C	LUT component control register. See PRGIO_PRT0_LUT_CTL0 for the details of bit fields.
PRGIO_PRT1_LUT_CTL4	0x40050150	LUT component control register. See PRGIO_PRT0_LUT_CTL0 for the details of bit fields.
PRGIO_PRT1_LUT_CTL5	0x40050154	LUT component control register. See PRGIO_PRT0_LUT_CTL0 for the details of bit fields.
PRGIO_PRT1_LUT_CTL6	0x40050158	LUT component control register. See PRGIO_PRT0_LUT_CTL0 for the details of bit fields.
PRGIO_PRT1_LUT_CTL7	0x4005015C	LUT component control register. See PRGIO_PRT0_LUT_CTL0 for the details of bit fields.
PRGIO_PRT1_DU_SEL	0x400501C0	Data unit component input selection. See PRGIO_PRT0_DU_SEL for the details of bit fields.
PRGIO_PRT1_DU_CTL	0x400501C4	Data unit component control register. See PRGIO_PRT0_DU_CTL for the details of bit fields.
PRGIO_PRT1_DATA	0x400501F0	Data register. See PRGIO_PRT0_DATA for the details of bit fields.
PRGIO_PRT2_CTL	0x40050200	Control register. See PRGIO_PRT0_CTL for the details of bit fields.
PRGIO_PRT2_SYNC_CTL	0x40050210	Synchronization control register. See PRGIO_PRT0_SYNC_CTL for the details of bit fields.
PRGIO_PRT2_LUT_SEL0	0x40050220	LUT component input selection. See PRGIO_PRT0_LUT_SEL0 for the details of bit fields.
PRGIO_PRT2_LUT_SEL1	0x40050224	LUT component input selection. See PRGIO_PRT0_LUT_SEL0 for the details of bit fields.
PRGIO_PRT2_LUT_SEL2	0x40050228	LUT component input selection. See PRGIO_PRT0_LUT_SEL0 for the details of bit fields.
PRGIO_PRT2_LUT_SEL3	0x4005022C	LUT component input selection. See PRGIO_PRT0_LUT_SEL0 for the details of bit fields.
PRGIO_PRT2_LUT_SEL4	0x40050230	LUT component input selection. See PRGIO_PRT0_LUT_SEL0 for the details of bit fields.
PRGIO_PRT2_LUT_SEL5	0x40050234	LUT component input selection. See PRGIO_PRT0_LUT_SEL0 for the details of bit fields.
PRGIO_PRT2_LUT_SEL6	0x40050238	LUT component input selection. See PRGIO_PRT0_LUT_SEL0 for the details of bit fields.
PRGIO_PRT2_LUT_SEL7	0x4005023C	LUT component input selection. See PRGIO_PRT0_LUT_SEL0 for the details of bit fields.
PRGIO_PRT2_LUT_CTL0	0x40050240	LUT component control register. See PRGIO_PRT0_LUT_CTL0 for the details of bit fields.
PRGIO_PRT2_LUT_CTL1	0x40050244	LUT component control register. See PRGIO_PRT0_LUT_CTL0 for the details of bit fields.
PRGIO_PRT2_LUT_CTL2	0x40050248	LUT component control register. See PRGIO_PRT0_LUT_CTL0 for the details of bit fields.
PRGIO_PRT2_LUT_CTL3	0x4005024C	LUT component control register. See PRGIO_PRT0_LUT_CTL0 for the details of bit fields.
PRGIO_PRT2_LUT_CTL4	0x40050250	LUT component control register. See PRGIO_PRT0_LUT_CTL0 for the details of bit fields.
PRGIO_PRT2_LUT_CTL5	0x40050254	LUT component control register. See PRGIO_PRT0_LUT_CTL0 for the details of bit fields.
PRGIO_PRT2_LUT_CTL6	0x40050258	LUT component control register. See PRGIO_PRT0_LUT_CTL0 for the details of bit fields.
PRGIO_PRT2_LUT_CTL7	0x4005025C	LUT component control register. See PRGIO_PRT0_LUT_CTL0 for the details of bit fields.
PRGIO_PRT2_DU_SEL	0x400502C0	Data unit component input selection. See PRGIO_PRT0_DU_SEL for the details of bit fields.
PRGIO_PRT2_DU_CTL	0x400502C4	Data unit component control register. See PRGIO_PRT0_DU_CTL for the details of bit fields.
PRGIO_PRT2_DATA	0x400502F0	Data register. See PRGIO_PRT0_DATA for the details of bit fields.

6.1.1 PRGIO_PRT0_CTL

Control register

Address: 0x40050000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	BYPASS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW				
HW Access	None			R				
Name	None [15:13]			CLOCK_SRC [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None					RW	RW
HW Access	R	None					R	R
Name	ENABLED	None [30:26]					PIPE-LINE_EN	HLD_OVR

Bits	Name	Description
31	ENABLED	Enable for programmable IO. Should only be set to '1' when the programmable IO is completely configured: '0': Disabled (signals are bypassed; behavior as if BYPASS is 0xFF). When disabled, the fabric (data unit and LUTs) reset is activated. If the IP is disabled: - The PIPELINE_EN register field should be set to '1', to ensure low power consumption by preventing combinatorial loops. - The CLOCK_SRC register field should be set to "20"-"30" (clock is constant '0'), to ensure low power consumption. '1': Enabled. Once enabled, it takes 3 "clk_fabric" clock cycles till the fabric reset is de-activated and the fabric becomes fully functional. This ensures that the IO pins' input synchronizer states are flushed when the fabric is fully functional. Default Value: 0
25	PIPELINE_EN	Enable for pipeline register: '0': Disabled (register is bypassed). '1': Enabled. Default Value: 1

6.1.1 PRGIO_PRT0_CTL (continued)

24	HLD_OVR	IO cell hold override functionality. In DeepSleep and Hibernate power modes, the HSIOM holds the IO cell output and output enable signals if Active functionality is connected to the IO pads. This is undesirable if the PRGIO is supposed to deliver DeepSleep or Hibernate output functionality on these IO pads. This field is used to control the hold override functionality from the PRGIO: '0': The HSIOM controls the IO cell hold override functionality ("hsiom_hld_ovr"). '1': The PRGIO controls the IO cel hold override functionality: - In bypass mode (ENABLED is '0' or BYPASS[i] is '1'), the HSIOM control is used. - In NON bypass mode (ENABLED is '1' and BYPASS[i] is '0'), the PRGIO sets hold override to "pwr_hld_ovr_hib" to enable PRGIO functionality in DeepSleep and Hibernate power modes (but disables it in Stop power mode). Note that in Hibernate power mode, the PRGIO should not rely on the state of Active or DeepSleep functionality signals from the HSIOM: these signals are clamped to '0' in Hibernate" Default Value: Undefined
12 : 8	CLOCK_SRC	Clock ("clk_fabric") and reset ("rst_fabric_n") source selection: "0": io_data_in[0]/'1'. ... "7": io_data_in[7]/'1'. "8": chip_data[0]/'1'. ... "15": chip_data[7]/'1'. "16": clk_prgio/rst_sys_act_n. Used for both Active functionality synchronous logic on "clk_prgio". This selection is intended for synchronous operation on a PCLK specified clock frequency ("clock_prgio_en"). Note that the fabric's clocked elements are frequency aligned, but NOT phase aligned to "clk_sys". "17": clk_prgio/rst_sys_dpslp_n. Used for both DeepSleep functionality synchronous logic on "clk_prgio" (note that "clk_prgio" is NOT available in DeepSleep and Hibernate power modes). This selection is intended for synchronous operation on a PCLK specified clock frequency ("clock_prgio_en"). Note that the fabric's clocked elements are frequency aligned, but NOT phase aligned to "clk_sys". "18": clk_prgio/rst_sys_hib_n. Used for both Hibernate functionality synchronous logic on "clk_prgio" (note that "clk_prgio" is NOT available in DeepSleep and Hibernate power modes). This selection is intended for synchronous operation on a PCLK specified clock frequency ("clock_prgio_en"). Note that the fabric's clocked elements are frequency aligned, but NOT phase aligned to "clk_sys". "19": clk_lf/rst_lf_dpslp_n (note that "clk_lf" is only available in DeepSleep power mode). This selection is intended for synchronous operation on"clk_lf". Note that the fabric's clocked elements are frequency aligned, but NOT phase aligned to other "clk_lf" clocked elements. "20"-"30": Clock source is constant '0'. Any of these clock sources should be selected when the IP is disabled to ensure low power consumption. "31": clk_sys/'1'. This selection is NOT intended for "clk_sys" operation, but for asynchronous operation: three "clk_sys" cycles after enabling the IP, the IP is fully functional (reset is de-activated). To be used for asynchronous (clockless) fabric functionality. Default Value: 20
7 : 0	BYPASS	Bypass of the programmable IO, one bit for each IO pin: BYPASS[i] is for IO pin i. When ENABLED is '1', this field is used. When ENABLED is '0', this field is NOT used and PRGIO is always bypassed. '0': No bypass (programmable IO fabric is exposed). '1': Bypass (programmable IO fabric is hidden). Default Value: Undefined

6.1.2 PRGIO_PRT0_SYNC_CTL

Synchronization control register

Address: 0x40050010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	IO_SYNC_EN [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CHIP_SYNC_EN [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 8	CHIP_SYNC_EN	Synchronization of the chip input signals to "clk_fabric", one bit for each input: CHIP_SYNC_EN[i] is for input i. '0': No synchronization. '1': Synchronization. Default Value: Undefined
7 : 0	IO_SYNC_EN	Synchronization of the IO pin input signals to "clk_fabric", one bit for each IO pin: IO_SYNC_EN[i] is for IO pin i. '0': No synchronization. '1': Synchronization. Default Value: Undefined

6.1.3 PRGIO_PRT0_LUT_SEL0

LUT component input selection

Address: 0x40050020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				LUT_TR0_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				LUT_TR1_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				LUT_TR2_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	LUT_TR2_SEL	LUT input signal "tr2_in" source selection. Encoding is the same as for LUT_TR1_SEL. Default Value: Undefined
11 : 8	LUT_TR1_SEL	LUT input signal "tr1_in" source selection: "0": LUT 0 output. "1": LUT 1 output. "2": LUT 2 output. "3": LUT 3 output. "4": LUT 4 output. "5": LUT 5 output. "6": LUT 6 output. "7": LUT 7 output. "8": chip_data[0] (for LUTs 0, 1, 2, 3); chip_data[4] (for LUTs 4, 5, 6, 7). "9": chip_data[1] (for LUTs 0, 1, 2, 3); chip_data[5] (for LUTs 4, 5, 6, 7). "10": chip_data[2] (for LUTs 0, 1, 2, 3); chip_data[6] (for LUTs 4, 5, 6, 7). "11": chip_data[3] (for LUTs 0, 1, 2, 3); chip_data[7] (for LUTs 4, 5, 6, 7). "12": io_data_in[0] (for LUTs 0, 1, 2, 3); io_data_in[4] (for LUTs 4, 5, 6, 7). "13": io_data_in[1] (for LUTs 0, 1, 2, 3); io_data_in[5] (for LUTs 4, 5, 6, 7). "14": io_data_in[2] (for LUTs 0, 1, 2, 3); io_data_in[6] (for LUTs 4, 5, 6, 7). "15": io_data_in[3] (for LUTs 0, 1, 2, 3); io_data_in[7] (for LUTs 4, 5, 6, 7). Default Value: Undefined

6.1.3 PRGIO_PRT0_LUT_SEL0 (continued)

3 : 0	LUT_TR0_SEL	LUT input signal "tr0_in" source selection: "0": Data unit output. "1": LUT 1 output. "2": LUT 2 output. "3": LUT 3 output. "4": LUT 4 output. "5": LUT 5 output. "6": LUT 6 output. "7": LUT 7 output. "8": chip_data[0] (for LUTs 0, 1, 2, 3); chip_data[4] (for LUTs 4, 5, 6, 7). "9": chip_data[1] (for LUTs 0, 1, 2, 3); chip_data[5] (for LUTs 4, 5, 6, 7). "10": chip_data[2] (for LUTs 0, 1, 2, 3); chip_data[6] (for LUTs 4, 5, 6, 7). "11": chip_data[3] (for LUTs 0, 1, 2, 3); chip_data[7] (for LUTs 4, 5, 6, 7). "12": io_data_in[0] (for LUTs 0, 1, 2, 3); io_data_in[4] (for LUTs 4, 5, 6, 7). "13": io_data_in[1] (for LUTs 0, 1, 2, 3); io_data_in[5] (for LUTs 4, 5, 6, 7). "14": io_data_in[2] (for LUTs 0, 1, 2, 3); io_data_in[6] (for LUTs 4, 5, 6, 7). "15": io_data_in[3] (for LUTs 0, 1, 2, 3); io_data_in[7] (for LUTs 4, 5, 6, 7). Default Value: Undefined

6.1.4 PRGIO_PRT0_LUT_CTL0

LUT component control register

Address: 0x40050040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	LUT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						LUT_OPC [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 8	LUT_OPC	LUT opcode specifies the LUT operation: "0": Combinatoral output, no feedback. tr_out = LUT[{tr2_in, tr1_in, tr0_in}]. "1": Combinatorial output, feedback. tr_out = LUT[{lut_reg, tr1_in, tr0_in}]. On clock: lut_reg <= tr_in2. "2": Sequential output, no feedback. temp = LUT[{tr2_in, tr1_in, tr0_in}]. tr_out = lut_reg. On clock: lut_reg <= temp. "3": Register with asynchronous set and reset. tr_out = lut_reg. enable = (tr2_in ^ LUT[4]) | LUT[5]. set = enable & (tr1_in ^ LUT[2]) & LUT[3]. clr = enable & (tr0_in ^ LUT[0]) & LUT[1]. Asynchronously (no clock required): lut_reg <= if (clr) '0' else if (set) '1' Default Value: Undefined

6.1.4 PRGIO_PRT0_LUT_CTL0 (continued)

7 : 0	LUT	LUT configuration. Depending on the LUT opcode LUT_OPC, the internal state lut_reg (captured in a flip-flop) and the LUT input signals tr0_in, tr1_in, tr2_in, the LUT configuration is used to determine the LUT output signal and the next sequential state (lut_reg). Default Value: Undefined

6.1.5 PRGIO_PRT0_DU_SEL

Data unit component input selection

Address: 0x400500C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				DU_TR0_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				DU_TR1_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				DU_TR2_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None		RW		None		RW	
HW Access	None		R		None		R	
Name	None [31:30]		DU_DATA1_SEL [29:28]		None [27:26]		DU_DATA0_SEL [25:24]	

Bits	Name	Description
29 : 28	DU_DATA1_SEL	Data unit input data "data1_in" source selection. Encoding is the same as for DU_DATA0_SEL. Default Value: Undefined
25 : 24	DU_DATA0_SEL	Data unit input data "data0_in" source selection: "0": Constant "0". "1": chip_data[7:0]. "2": io_data_in[7:0]. "3": DATA.DATA MMIO register field. Default Value: Undefined
19 : 16	DU_TR2_SEL	Data unit input signal "tr2_in" source selection. Encoding is the same as for DU_TR0_SEL. Default Value: Undefined
11 : 8	DU_TR1_SEL	Data unit input signal "tr1_in" source selection. Encoding is the same as for DU_TR0_SEL. Default Value: Undefined

6.1.5 PRGIO_PRT0_DU_SEL (continued)

3 : 0	DU_TR0_SEL	Data unit input signal "tr0_in" source selection: "0": Constant '0'. "1": Constant '1'. "2": Data unit output. "10-3": LUT 7 - 0 outputs. Otherwise: Undefined. Default Value: Undefined

6.1.6 PRGIO_PRT0_DU_CTL

Data unit component control register

Address: 0x400500C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW		
HW Access	None					R		
Name	None [7:3]					DU_SIZE [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				DU_OPC [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11 : 8	DU_OPC	Data unit opcode specifies the data unit operation: "1": INCR "2": DECR "3": INCR_WRAP "4": DECR_WRAP "5": INCR_DECR "6": INCR_DECR_WRAP "7": ROR "8": SHR "9": AND_OR "10": SHR_MAJ3 "11": SHR_EQL. Otherwise: Undefined. Default Value: Undefined
2 : 0	DU_SIZE	Size/width of the data unit data operands (in bits) is DU_SIZE+1. E.g., if DU_SIZE is 7, the width is 8 bits. Default Value: Undefined

6.1.7 PRGIO_PRT0_DATA

Data register

Address: 0x400500F0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA	Data unit input data source. Default Value: Undefined

7 CPU Sub System (CPUSS) Registers

This section discusses the CPUSS registers. It lists all the registers in mapping tables, in address order.

7.1 Register Details

Register	Address	Description
CPUSS_SYSREQ	0x40100004	SYSCALL control register
CPUSS_SYSARG	0x40100008	SYSARG control register
CPUSS_PROTECTION	0x4010000C	Protection control register
CPUSS_PRIV_ROM	0x40100010	ROM privilege register
CPUSS_PRIV_RAM	0x40100014	RAM privilege register
CPUSS_PRIV_FLASH	0x40100018	Flash privilege register
CPUSS_WOUNDING	0x4010001C	Wounding register
CPUSS_FLASH_CTL	0x40100030	FLASH control register
CPUSS_ROM_CTL	0x40100034	ROM control register
CPUSS_RAM_CTL	0x40100038	RAM control register
CPUSS_DMAC_CTL	0x4010003C	DMA controller register
CPUSS_SL_CTL0	0x40100100	Slave control register
CPUSS_SL_CTL1	0x40100104	Slave control register. See CPUSS_SL_CTL0 for the details of bit fields.
CPUSS_SL_CTL2	0x40100108	Slave control register. See CPUSS_SL_CTL0 for the details of bit fields.
CPUSS_SL_CTL3	0x4010010C	Slave control register. See CPUSS_SL_CTL0 for the details of bit fields.

7.1.1 CPUSS_SYSREQ

SYSCALL control register

Address: 0x40100004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	SYSCALL_COMMAND [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	SYSCALL_COMMAND [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	R	R	RW	RW	None		
HW Access	R	A	RW	A	R	None		
Name	SY-SCALL_REQ	HMAS-TER_0	ROM_AC-CESS_EN	PRIVI-LEGED	DIS_RE-SET_VECT_REL	None [26:24]		

Bits	Name	Description
31	SYSCALL_REQ	CPU/DAP writes a '1' to this field to request a SystemCall. The HMASTER_0 field indicates the source of the write access. Setting this field to '1' immediate results in a NMI. The SystemCall NMI interrupt handler sets this field to '0' after servicing the request. Default Value: 0
30	HMASTER_0	Indicates the source of the write access to the SYSREQ register. '0': CPU write access. '1': DAP write access. HW sets this field when the SYSREQ register is written to and SYSCALL_REQ is '0' (the last time it is set is when SW sets SYSCALL_REQ from '0' to '1'). Default Value: 0
29	ROM_ACCESS_EN	Indicates that executing from Boot ROM is enabled. HW sets this field to '1', on reset or when the SystemCall NMI vector is fetched from Boot ROM. HW sets this field to '0', when the CPU is NOT executing from either Boot or System ROM. This bit is used for debug purposes only. Default Value: 1

7.1.1 CPUSS_SYSREQ (continued)

28	PRIVILEGED	Indicates whether the system is in privileged ('1') or user mode ('0'). Only CPU SW executing from ROM can set this field to '1' when ROM_ACCESS_EN is '1' (the CPU is executing a SystemCall NMI interrupt handler). Any other write to this field sets is to '0'. This field is used as the AHB-Lite hprot[1] signal to implement Cypress proprietary user/privileged modes. These modes are used to enable/disable access to specific MMIO registers and memory regions. Default Value: 1
27	DIS_RESET_VECT_REL	Disable Reset Vector fetch relocation: '0': CPU accesses to locations 0x0000:0000 - 0x0000:0007 are redirected to ROM. '1': CPU accesses to locations 0x0000:0000 - 0x0000:0007 are made to flash. Note that this field defaults to '0' on reset, ensuring actual reset vector fetches are always made to ROM. Note that this field does not affect DAP accesses. Flash DfT routines may set this bit to '1' to enable uninhibited read-back of programmed data in the first flash page. Default Value: 0
15 : 0	SYSCALL_COMMAND	Opcode of the system call being requested. Default Value: 0

7.1.2 CPUSS_SYSARG

SYSARG control register

Address: 0x40100008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access								
Name	SYSCALL_ARG [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access								
Name	SYSCALL_ARG [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access								
Name	SYSCALL_ARG [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access								
Name	SYSCALL_ARG [31:24]							

Bits	Name	Description
31 : 0	SYSCALL_ARG	Argument to System Call specified in SYSREQ. Semantics of argument depends on system call made. Typically a pointer to a parameter block. Default Value: 0

7.1.3 CPUSS_PROTECTION

Protection control register

Address: 0x4010000C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				A			
Name	None [7:4]				PROTECTION_MODE [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1S	RW	None					
HW Access	R	A	None					
Name	PROTEC-TION_LOCK	FLASH_LOCK	None [29:24]					

Bits	Name	Description
31	PROTECTION_LOCK	Setting this field will block (ignore) any further writes to the PROTECTION_MODE field in this register. Once '1', this field cannot be cleared. Default Value: 0
30	FLASH_LOCK	Setting this bit will force SPCIF.ADDRESS.AXA to be ignored, which prevents SM Flash from being erased or overwritten. It is used to indicate the DEAD protection mode. Writes to this field are ignored when PROTECTION_LOCK is '1' Default Value: 0
3 : 0	PROTECTION_MODE	Current protection mode; this field is available as a global signal everywhere in the system. Writes to this field are ignored when PROTECTION_LOCK is '1': 0b1xxx: BOOT 0b01xx: KILL 0b001x: PROTECTED 0b0001: OPEN 0b0000: VIRGIN (also used for DEAD mode, but then FLASH_LOCK is also set) Default Value: 15

7.1.4 CPUSS_PRIV_ROM

ROM privilege register

Address: 0x40100010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	BROM_PROT_LIMIT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	BROM_PROT_LIMIT	Indicates the limit where the privileged area of the Boot ROM partition starts in increments of 256 Bytes. "0": Entire Boot ROM is Privileged. "1": First 256 Bytes are User accessible. ... BROM_PROT_LIMIT >= "Boot ROM partition capacity": Entire Boot ROM partition is user mode accessible. Default Value: 0

7.1.5 CPUSS_PRIV_RAM

RAM privilege register

Address: 0x40100014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	RAM_PROT_LIMIT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							RAM_PROT_LIMIT

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8 : 0	RAM_PROT_LIMIT	Indicates the limit where the privileged area of SRAM starts in increments of 256 Bytes. "0": Entire SRAM is Privileged. "1": First 256 Bytes are User accessible. Any number larger than the size of the SRAM indicates that the entire SRAM is user mode accessible. Default Value: 0

7.1.6 CPUSS_PRIV_FLASH

Flash privilege register

Address: 0x40100018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	FLASH_PROT_LIMIT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				FLASH_PROT_LIMIT [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11 : 0	FLASH_PROT_LIMIT	Indicates the limit where the privileged area of flash starts in increments of 256 Bytes. "0": Entire flash is Privileged. "1": First 256 Bytes are User accessible. Any number larger than the size of the flash indicates that the entire flash is user mode accessible. Note that SuperVisory rows are always User accessible. If FLASH_PROT_LIMIT defines a non-empty privileged area, the boot ROM will assume that a system call table exists at the beginning of the Flash privileged area and use it for all SystemCalls made using SYSREQ. Default Value: 0

7.1.7 CPUSS_WOUNDING

Wounding register

Address: 0x4010001C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None	RW1S			None	RW1S		
HW Access	None	R			None	R		
Name	None	FLASH_WOUND [22:20]			None	RAM_WOUND [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
22 : 20	FLASH_WOUND	Indicates the amount of accessible flash in this part. The value in this field is effectively write-once (it is only possible to set bits, not clear them). The remainder portion of flash is not accessible and will return an AHB-Lite bus error. "0": entire memory accessible "1": first 1/2 of the memory accessible "2": first 1/4 of the memory accessible "3": first 1/8 of the memory accessible "4": first 1/16 of the memory accessible "5": first 1/32 of the memory accessible "6": first 1/64 of the memory accessible "7": first 1/128 of the memory accessible (used for the DEAD protection mode) Default Value: 0

7.1.7 CPUSS_WOUNDING (continued)

18 : 16	RAM_WOUND	Indicates the amount of accessible RAM 0 memory capacitty in this part. The value in this field is effectively write-once (it is only possible to set bits, not clear them). The remainder portion of SRAM is not accessible and will return an AHB-Lite bus error. "0": entire memory accessible "1": first 1/2 of the memory accessible "2": first 1/4 of the memory accessible "3": first 1/8 of the memory accessible "4": first 1/16 of the memory accessible "5": first 1/32 of the memory accessible "6": first 1/64 of the memory accessible "7": first 1/128 of the memory accessible Default Value: 0

7.1.8 CPUSS_FLASH_CTL

FLASH control register

Address: 0x40100030

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	None		RW	
HW Access	None			R	None		R	
Name	None [7:5]			PREF_EN	None [3:2]		FLASH_WS [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							RW1C
Name	None [15:9]							FLASH_IN-VALIDATE

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	
HW Access	None						R	
Name	None [23:18]						ARB [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
17 : 16	ARB	Arbitration policy: "0": CPU has priority "1": DW/DMA has priority "2": Roundrobin "3": Roundrobin - sticky Default Value: 0
8	FLASH_INVALIDATE	1': Invalidates the content of the flash controller's buffers. Default Value: 0
4	PREF_EN	Prefetch enable: '0': disabled. This is a desirable seeting when FLASH_WS is "0" or when predictable execution behavior is required. '1': enabled. Default Value: 0

7.1.8 CPUSS_FLASH_CTL (continued)

1 : 0	FLASH_WS	Amount of ROM wait states: "0": 0 wait states (fast flash: [0, 24] MHz system frequency, slow flash: [0, 16] MHz system frequency) "1": 1 wait state (fast flash: [24, 48] MHz system frequency, slow flash: [16, 32] MHz system frequency) "2": 2 wait states (slow flash: [32, 48] MHz system frequency) "3": 3 wait states (can be used to give more time for flash access if 2 wait states are not sufficient) Default Value: 0

7.1.9 CPUSS_ROM_CTL

ROM control register

Address: 0x40100034

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							ROM_WS

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	ROM_WS	Amount of ROM wait states: '0': 0 wait states. Use this setting for newer, faster ROM design. Use this setting for older, slower ROM design and frequencies in the range [0, 24] MHz. '1': 1 wait state. Use this setting for older, slower ROM design and frequencies in the range <24, 48] MHz. Should always be set to 0. Default Value: 0

7.1.10 CPUSS_RAM_CTL

RAM control register

Address: 0x40100038

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	
HW Access	None						R	
Name	None [23:18]						ARB [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
17 : 16	ARB	Arbitration policy: "0": CPU has priority "1": DW/DMA has priority "2": Roundrobin "3": Roundrobin - sticky Default Value: 0

7.1.11 CPUSS_DMAC_CTL

DMA controller register

Address: 0x4010003C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	
HW Access	None						R	
Name	None [23:18]						ARB [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
17 : 16	ARB	Arbitration policy: "0": CPU has priority "1": DW/DMA has priority "2": Roundrobin "3": Roundrobin - sticky Default Value: 0

7.1.12 CPUSS_SL_CTL0

Slave control register

Address: 0x40100100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	
HW Access	None						R	
Name	None [23:18]						ARB [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
17 : 16	ARB	Arbitration policy: "0": CPU priority "1": DMA priority "2": Roundrobin "3": Roundrobin - sticky Default Value: 0

8 Direct Memory Access (DMA) Registers

This section discusses the DMA registers. It lists all the registers in mapping tables, in address order.

8.1 Register Details

Register	Address	Description
DMAC_CTL	0x40101000	Control register
DMAC_STATUS	0x40101010	Status register
DMAC_STATUS_SRC_ADDR	0x40101014	Source address status register
DMAC_STATUS_DST_ADDR	0x40101018	Destination address register
DMAC_STATUS_CH_ACT	0x4010101C	Channel activation status register
DMAC_CH_CTL0	0x40101080	Channel control register
DMAC_CH_CTL1	0x40101084	Channel control register. See DMAC_CH_CTL0 for the details of bit fields.
DMAC_CH_CTL2	0x40101088	Channel control register. See DMAC_CH_CTL0 for the details of bit fields.
DMAC_CH_CTL3	0x4010108C	Channel control register. See DMAC_CH_CTL0 for the details of bit fields.
DMAC_CH_CTL4	0x40101090	Channel control register. See DMAC_CH_CTL0 for the details of bit fields.
DMAC_CH_CTL5	0x40101094	Channel control register. See DMAC_CH_CTL0 for the details of bit fields.
DMAC_CH_CTL6	0x40101098	Channel control register. See DMAC_CH_CTL0 for the details of bit fields.
DMAC_CH_CTL7	0x4010109C	Channel control register. See DMAC_CH_CTL0 for the details of bit fields.
DMAC_CH_CTL8	0x401010A0	Channel control register. See DMAC_CH_CTL0 for the details of bit fields.
DMAC_CH_CTL9	0x401010A4	Channel control register. See DMAC_CH_CTL0 for the details of bit fields.
DMAC_CH_CTL10	0x401010A8	Channel control register. See DMAC_CH_CTL0 for the details of bit fields.
DMAC_CH_CTL11	0x401010AC	Channel control register. See DMAC_CH_CTL0 for the details of bit fields.
DMAC_CH_CTL12	0x401010B0	Channel control register. See DMAC_CH_CTL0 for the details of bit fields.
DMAC_CH_CTL13	0x401010B4	Channel control register. See DMAC_CH_CTL0 for the details of bit fields.
DMAC_CH_CTL14	0x401010B8	Channel control register. See DMAC_CH_CTL0 for the details of bit fields.
DMAC_CH_CTL15	0x401010BC	Channel control register. See DMAC_CH_CTL0 for the details of bit fields.
DMAC_INTR	0x401017F0	Interrupt register
DMAC_INTR_SET	0x401017F4	Interrupt set register
DMAC_INTR_MASK	0x401017F8	Interrupt mask register
DMAC_INTR_MASKED	0x401017FC	Interrupt masked register
DMAC_DESCR0_PING_SRC	0x40101800	Ping source address
DMAC_DESCR0_PING_DST	0x40101804	Ping destination address

Register	Address	Description
DMAC_DESCR0_PING_CTL	0x40101808	Ping control word
DMAC_DESCR0_PING_STATUS	0x4010180C	Ping status word
DMAC_DESCR0_PONG_SRC	0x40101810	Pong source address
DMAC_DESCR0_PONG_DST	0x40101814	Pong destination address
DMAC_DESCR0_PONG_CTL	0x40101818	Pong control word
DMAC_DESCR0_PONG_STATUS	0x4010181C	Pong status word
DMAC_DESCR1_PING_SRC	0x40101820	Ping source address. See DMAC_DESCR0_PING_SRC for the details of bit fields.
DMAC_DESCR1_PING_DST	0x40101824	Ping destination address. See DMAC_DESCR0_PING_DST for the details of bit fields.
DMAC_DESCR1_PING_CTL	0x40101828	Ping control word. See DMAC_DESCR0_PING_CTL for the details of bit fields.
DMAC_DESCR1_PING_STATUS	0x4010182C	Ping status word. See DMAC_DESCR0_PING_STATUS for the details of bit fields.
DMAC_DESCR1_PONG_SRC	0x40101830	Pong source address. See DMAC_DESCR0_PONG_SRC for the details of bit fields.
DMAC_DESCR1_PONG_DST	0x40101834	Pong destination address. See DMAC_DESCR0_PONG_DST for the details of bit fields.
DMAC_DESCR1_PONG_CTL	0x40101838	Pong control word. See DMAC_DESCR0_PONG_CTL for the details of bit fields.
DMAC_DESCR1_PONG_STATUS	0x4010183C	Pong status word. See DMAC_DESCR0_PONG_STATUS for the details of bit fields.
DMAC_DESCR2_PING_SRC	0x40101840	Ping source address. See DMAC_DESCR0_PING_SRC for the details of bit fields.
DMAC_DESCR2_PING_DST	0x40101844	Ping destination address. See DMAC_DESCR0_PING_DST for the details of bit fields.
DMAC_DESCR2_PING_CTL	0x40101848	Ping control word. See DMAC_DESCR0_PING_CTL for the details of bit fields.
DMAC_DESCR2_PING_STATUS	0x4010184C	Ping status word. See DMAC_DESCR0_PING_STATUS for the details of bit fields.
DMAC_DESCR2_PONG_SRC	0x40101850	Pong source address. See DMAC_DESCR0_PONG_SRC for the details of bit fields.
DMAC_DESCR2_PONG_DST	0x40101854	Pong destination address. See DMAC_DESCR0_PONG_DST for the details of bit fields.
DMAC_DESCR2_PONG_CTL	0x40101858	Pong control word. See DMAC_DESCR0_PONG_CTL for the details of bit fields.
DMAC_DESCR2_PONG_STATUS	0x4010185C	Pong status word. See DMAC_DESCR0_PONG_STATUS for the details of bit fields.
DMAC_DESCR3_PING_SRC	0x40101860	Ping source address. See DMAC_DESCR0_PING_SRC for the details of bit fields.
DMAC_DESCR3_PING_DST	0x40101864	Ping destination address. See DMAC_DESCR0_PING_DST for the details of bit fields.
DMAC_DESCR3_PING_CTL	0x40101868	Ping control word. See DMAC_DESCR0_PING_CTL for the details of bit fields.
DMAC_DESCR3_PING_STATUS	0x4010186C	Ping status word. See DMAC_DESCR0_PING_STATUS for the details of bit fields.
DMAC_DESCR3_PONG_SRC	0x40101870	Pong source address. See DMAC_DESCR0_PONG_SRC for the details of bit fields.
DMAC_DESCR3_PONG_DST	0x40101874	Pong destination address. See DMAC_DESCR0_PONG_DST for the details of bit fields.
DMAC_DESCR3_PONG_CTL	0x40101878	Pong control word. See DMAC_DESCR0_PONG_CTL for the details of bit fields.
DMAC_DESCR3_PONG_STATUS	0x4010187C	Pong status word. See DMAC_DESCR0_PONG_STATUS for the details of bit fields.
DMAC_DESCR4_PING_SRC	0x40101880	Ping source address. See DMAC_DESCR0_PING_SRC for the details of bit fields.
DMAC_DESCR4_PING_DST	0x40101884	Ping destination address. See DMAC_DESCR0_PING_DST for the details of bit fields.
DMAC_DESCR4_PING_CTL	0x40101888	Ping control word. See DMAC_DESCR0_PING_CTL for the details of bit fields.
DMAC_DESCR4_PING_STATUS	0x4010188C	Ping status word. See DMAC_DESCR0_PING_STATUS for the details of bit fields.
DMAC_DESCR4_PONG_SRC	0x40101890	Pong source address. See DMAC_DESCR0_PONG_SRC for the details of bit fields.
DMAC_DESCR4_PONG_DST	0x40101894	Pong destination address. See DMAC_DESCR0_PONG_DST for the details of bit fields.
DMAC_DESCR4_PONG_CTL	0x40101898	Pong control word. See DMAC_DESCR0_PONG_CTL for the details of bit fields.
DMAC_DESCR4_PONG_STATUS	0x4010189C	Pong status word. See DMAC_DESCR0_PONG_STATUS for the details of bit fields.
DMAC_DESCR5_PING_SRC	0x401018A0	Ping source address. See DMAC_DESCR0_PING_SRC for the details of bit fields.
DMAC_DESCR5_PING_DST	0x401018A4	Ping destination address. See DMAC_DESCR0_PING_DST for the details of bit fields.
DMAC_DESCR5_PING_CTL	0x401018A8	Ping control word. See DMAC_DESCR0_PING_CTL for the details of bit fields.
DMAC_DESCR5_PING_STATUS	0x401018AC	Ping status word. See DMAC_DESCR0_PING_STATUS for the details of bit fields.

Register	Address	Description
DMAC_DESCR5_PONG_SRC	0x401018B0	Pong source address. See DMAC_DESCR0_PONG_SRC for the details of bit fields.
DMAC_DESCR5_PONG_DST	0x401018B4	Pong destination address. See DMAC_DESCR0_PONG_DST for the details of bit fields.
DMAC_DESCR5_PONG_CTL	0x401018B8	Pong control word. See DMAC_DESCR0_PONG_CTL for the details of bit fields.
DMAC_DESCR5_PONG_STATUS	0x401018BC	Pong status word. See DMAC_DESCR0_PONG_STATUS for the details of bit fields.
DMAC_DESCR6_PING_SRC	0x401018C0	Ping source address. See DMAC_DESCR0_PING_SRC for the details of bit fields.
DMAC_DESCR6_PING_DST	0x401018C4	Ping destination address. See DMAC_DESCR0_PING_DST for the details of bit fields.
DMAC_DESCR6_PING_CTL	0x401018C8	Ping control word. See DMAC_DESCR0_PING_CTL for the details of bit fields.
DMAC_DESCR6_PING_STATUS	0x401018CC	Ping status word. See DMAC_DESCR0_PING_STATUS for the details of bit fields.
DMAC_DESCR6_PONG_SRC	0x401018D0	Pong source address. See DMAC_DESCR0_PONG_SRC for the details of bit fields.
DMAC_DESCR6_PONG_DST	0x401018D4	Pong destination address. See DMAC_DESCR0_PONG_DST for the details of bit fields.
DMAC_DESCR6_PONG_CTL	0x401018D8	Pong control word. See DMAC_DESCR0_PONG_CTL for the details of bit fields.
DMAC_DESCR6_PONG_STATUS	0x401018DC	Pong status word. See DMAC_DESCR0_PONG_STATUS for the details of bit fields.
DMAC_DESCR7_PING_SRC	0x401018E0	Ping source address. See DMAC_DESCR0_PING_SRC for the details of bit fields.
DMAC_DESCR7_PING_DST	0x401018E4	Ping destination address. See DMAC_DESCR0_PING_DST for the details of bit fields.
DMAC_DESCR7_PING_CTL	0x401018E8	Ping control word. See DMAC_DESCR0_PING_CTL for the details of bit fields.
DMAC_DESCR7_PING_STATUS	0x401018EC	Ping status word. See DMAC_DESCR0_PING_STATUS for the details of bit fields.
DMAC_DESCR7_PONG_SRC	0x401018F0	Pong source address. See DMAC_DESCR0_PONG_SRC for the details of bit fields.
DMAC_DESCR7_PONG_DST	0x401018F4	Pong destination address. See DMAC_DESCR0_PONG_DST for the details of bit fields.
DMAC_DESCR7_PONG_CTL	0x401018F8	Pong control word. See DMAC_DESCR0_PONG_CTL for the details of bit fields.
DMAC_DESCR7_PONG_STATUS	0x401018FC	Pong status word. See DMAC_DESCR0_PONG_STATUS for the details of bit fields.
DMAC_DESCR8_PING_SRC	0x40101900	Ping source address. See DMAC_DESCR0_PING_SRC for the details of bit fields.
DMAC_DESCR8_PING_DST	0x40101904	Ping destination address. See DMAC_DESCR0_PING_DST for the details of bit fields.
DMAC_DESCR8_PING_CTL	0x40101908	Ping control word. See DMAC_DESCR0_PING_CTL for the details of bit fields.
DMAC_DESCR8_PING_STATUS	0x4010190C	Ping status word. See DMAC_DESCR0_PING_STATUS for the details of bit fields.
DMAC_DESCR8_PONG_SRC	0x40101910	Pong source address. See DMAC_DESCR0_PONG_SRC for the details of bit fields.
DMAC_DESCR8_PONG_DST	0x40101914	Pong destination address. See DMAC_DESCR0_PONG_DST for the details of bit fields.
DMAC_DESCR8_PONG_CTL	0x40101918	Pong control word. See DMAC_DESCR0_PONG_CTL for the details of bit fields.
DMAC_DESCR8_PONG_STATUS	0x4010191C	Pong status word. See DMAC_DESCR0_PONG_STATUS for the details of bit fields.
DMAC_DESCR9_PING_SRC	0x40101920	Ping source address. See DMAC_DESCR0_PING_SRC for the details of bit fields.
DMAC_DESCR9_PING_DST	0x40101924	Ping destination address. See DMAC_DESCR0_PING_DST for the details of bit fields.
DMAC_DESCR9_PING_CTL	0x40101928	Ping control word. See DMAC_DESCR0_PING_CTL for the details of bit fields.
DMAC_DESCR9_PING_STATUS	0x4010192C	Ping status word. See DMAC_DESCR0_PING_STATUS for the details of bit fields.
DMAC_DESCR9_PONG_SRC	0x40101930	Pong source address. See DMAC_DESCR0_PONG_SRC for the details of bit fields.
DMAC_DESCR9_PONG_DST	0x40101934	Pong destination address. See DMAC_DESCR0_PONG_DST for the details of bit fields.
DMAC_DESCR9_PONG_CTL	0x40101938	Pong control word. See DMAC_DESCR0_PONG_CTL for the details of bit fields.
DMAC_DESCR9_PONG_STATUS	0x4010193C	Pong status word. See DMAC_DESCR0_PONG_STATUS for the details of bit fields.
DMAC_DESCR10_PING_SRC	0x40101940	Ping source address. See DMAC_DESCR0_PING_SRC for the details of bit fields.
DMAC_DESCR10_PING_DST	0x40101944	Ping destination address. See DMAC_DESCR0_PING_DST for the details of bit fields.
DMAC_DESCR10_PING_CTL	0x40101948	Ping control word. See DMAC_DESCR0_PING_CTL for the details of bit fields.
DMAC_DESCR10_PING_STATUS	0x4010194C	Ping status word. See DMAC_DESCR0_PING_STATUS for the details of bit fields.
DMAC_DESCR10_PONG_SRC	0x40101950	Pong source address. See DMAC_DESCR0_PONG_SRC for the details of bit fields.
DMAC_DESCR10_PONG_DST	0x40101954	Pong destination address. See DMAC_DESCR0_PONG_DST for the details of bit fields.

Register	Address	Description
DMAC_DESCR10_PONG_CTL	0x40101958	Pong control word. See DMAC_DESCR0_PONG_CTL for the details of bit fields.
DMAC_DESCR10_PONG_STATUS	0x4010195C	Pong status word. See DMAC_DESCR0_PONG_STATUS for the details of bit fields.
DMAC_DESCR11_PING_SRC	0x40101960	Ping source address. See DMAC_DESCR0_PING_SRC for the details of bit fields.
DMAC_DESCR11_PING_DST	0x40101964	Ping destination address. See DMAC_DESCR0_PING_DST for the details of bit fields.
DMAC_DESCR11_PING_CTL	0x40101968	Ping control word. See DMAC_DESCR0_PING_CTL for the details of bit fields.
DMAC_DESCR11_PING_STATUS	0x4010196C	Ping status word. See DMAC_DESCR0_PING_STATUS for the details of bit fields.
DMAC_DESCR11_PONG_SRC	0x40101970	Pong source address. See DMAC_DESCR0_PONG_SRC for the details of bit fields.
DMAC_DESCR11_PONG_DST	0x40101974	Pong destination address. See DMAC_DESCR0_PONG_DST for the details of bit fields.
DMAC_DESCR11_PONG_CTL	0x40101978	Pong control word. See DMAC_DESCR0_PONG_CTL for the details of bit fields.
DMAC_DESCR11_PONG_STATUS	0x4010197C	Pong status word. See DMAC_DESCR0_PONG_STATUS for the details of bit fields.
DMAC_DESCR12_PING_SRC	0x40101980	Ping source address. See DMAC_DESCR0_PING_SRC for the details of bit fields.
DMAC_DESCR12_PING_DST	0x40101984	Ping destination address. See DMAC_DESCR0_PING_DST for the details of bit fields.
DMAC_DESCR12_PING_CTL	0x40101988	Ping control word. See DMAC_DESCR0_PING_CTL for the details of bit fields.
DMAC_DESCR12_PING_STATUS	0x4010198C	Ping status word. See DMAC_DESCR0_PING_STATUS for the details of bit fields.
DMAC_DESCR12_PONG_SRC	0x40101990	Pong source address. See DMAC_DESCR0_PONG_SRC for the details of bit fields.
DMAC_DESCR12_PONG_DST	0x40101994	Pong destination address. See DMAC_DESCR0_PONG_DST for the details of bit fields.
DMAC_DESCR12_PONG_CTL	0x40101998	Pong control word. See DMAC_DESCR0_PONG_CTL for the details of bit fields.
DMAC_DESCR12_PONG_STATUS	0x4010199C	Pong status word. See DMAC_DESCR0_PONG_STATUS for the details of bit fields.
DMAC_DESCR13_PING_SRC	0x401019A0	Ping source address. See DMAC_DESCR0_PING_SRC for the details of bit fields.
DMAC_DESCR13_PING_DST	0x401019A4	Ping destination address. See DMAC_DESCR0_PING_DST for the details of bit fields.
DMAC_DESCR13_PING_CTL	0x401019A8	Ping control word. See DMAC_DESCR0_PING_CTL for the details of bit fields.
DMAC_DESCR13_PING_STATUS	0x401019AC	Ping status word. See DMAC_DESCR0_PING_STATUS for the details of bit fields.
DMAC_DESCR13_PONG_SRC	0x401019B0	Pong source address. See DMAC_DESCR0_PONG_SRC for the details of bit fields.
DMAC_DESCR13_PONG_DST	0x401019B4	Pong destination address. See DMAC_DESCR0_PONG_DST for the details of bit fields.
DMAC_DESCR13_PONG_CTL	0x401019B8	Pong control word. See DMAC_DESCR0_PONG_CTL for the details of bit fields.
DMAC_DESCR13_PONG_STATUS	0x401019BC	Pong status word. See DMAC_DESCR0_PONG_STATUS for the details of bit fields.
DMAC_DESCR14_PING_SRC	0x401019C0	Ping source address. See DMAC_DESCR0_PING_SRC for the details of bit fields.
DMAC_DESCR14_PING_DST	0x401019C4	Ping destination address. See DMAC_DESCR0_PING_DST for the details of bit fields.
DMAC_DESCR14_PING_CTL	0x401019C8	Ping control word. See DMAC_DESCR0_PING_CTL for the details of bit fields.
DMAC_DESCR14_PING_STATUS	0x401019CC	Ping status word. See DMAC_DESCR0_PING_STATUS for the details of bit fields.
DMAC_DESCR14_PONG_SRC	0x401019D0	Pong source address. See DMAC_DESCR0_PONG_SRC for the details of bit fields.
DMAC_DESCR14_PONG_DST	0x401019D4	Pong destination address. See DMAC_DESCR0_PONG_DST for the details of bit fields.
DMAC_DESCR14_PONG_CTL	0x401019D8	Pong control word. See DMAC_DESCR0_PONG_CTL for the details of bit fields.
DMAC_DESCR14_PONG_STATUS	0x401019DC	Pong status word. See DMAC_DESCR0_PONG_STATUS for the details of bit fields.
DMAC_DESCR15_PING_SRC	0x401019E0	Ping source address. See DMAC_DESCR0_PING_SRC for the details of bit fields.
DMAC_DESCR15_PING_DST	0x401019E4	Ping destination address. See DMAC_DESCR0_PING_DST for the details of bit fields.
DMAC_DESCR15_PING_CTL	0x401019E8	Ping control word. See DMAC_DESCR0_PING_CTL for the details of bit fields.
DMAC_DESCR15_PING_STATUS	0x401019EC	Ping status word. See DMAC_DESCR0_PING_STATUS for the details of bit fields.
DMAC_DESCR15_PONG_SRC	0x401019F0	Pong source address. See DMAC_DESCR0_PONG_SRC for the details of bit fields.
DMAC_DESCR15_PONG_DST	0x401019F4	Pong destination address. See DMAC_DESCR0_PONG_DST for the details of bit fields.
DMAC_DESCR15_PONG_CTL	0x401019F8	Pong control word. See DMAC_DESCR0_PONG_CTL for the details of bit fields.
DMAC_DESCR15_PONG_STATUS	0x401019FC	Pong status word. See DMAC_DESCR0_PONG_STATUS for the details of bit fields.

8.1.1 DMAC_CTL

Control register

Address: 0x40101000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	ENABLED	None						

Bits	Name	Description
31	ENABLED	0': IP is disabled. Non-retainable MMIO registers and logic functionality are reset (retainable MMIO registers are NOT reset): - INTR register is set to "0". - DW/DMA functionality is aborted. - DW/DMA controller input/pending triggers are de-activated. - DW/DMA controller output triggers are de-activated. Disabling the IP has the same effect as an active "rst_sys_act_n" reset in DeepSleep power mode. To prevent a loss of active (pending) DW/DMA triggers when disabling the IP or when transitioning from Active to DeepSleep power mode, the STATUS.ACTIVE and STATUS_CH_ACT.CH fields can be used. Note that most MMIO registers are retainable, and a transition from DeepSleep to Active/Sleep power modes makes the DW/DMA controller operational, and ready to react to DW/DMA input triggers that are activated after the transition. Triggers are Active/Sleep functionality. '1': IP is enabled. Default Value: 0

8.1.2 DMAC_STATUS

Status register

Address: 0x40101010

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None				R			
HW Access	None				W			
Name	None [23:20]				CH_ADDR [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	R		None	R		
HW Access	W	W	W		None	W		
Name	ACTIVE	PING_PONG	PRIO [29:28]		None	STATE [26:24]		

Bits	Name	Description
31	ACTIVE	Specifies if there is a currently active (pending) channel in the data transfer engine: '0': no currently active channel. '1': currently active channel. Default Value: 0
30	PING_PONG	Specifies the descriptor of the channel is currently in use. "0" - PING descriptor "1" - PONG descriptor Default Value: Undefined
29 : 28	PRIO	Specifies the priority of the currently active channel. Default Value: Undefined

8.1.2 DMAC_STATUS (continued)

26 : 24	STATE	State of the data transfer engine. "0": DEFAULT state. "1": Loading descriptor (SRC, DST, CONTROL and STATUS words). "2": Loading data element from source location. "3": Storing data element to destination location. "4": Storing descriptor (STATUS word). "5": Wait for trigger de-activation. "6": Storing descriptor with error response (STATUS word). Default Value: 0
19 : 16	CH_ADDR	Specifies the channel number of the currently active channel. E.g. if we have 32 channels, the channel number address with CH_ADDR_WIDTH is LOG2 (32) = 5, and this field is a 5-bit field. If channel 7 is active, STATUS.ACTIVE is '1' and STATUS.CH_ADDR is "7". Default Value: Undefined
15 : 0	DATA_NR	Specifies the index of the currently active data transfer. This value increases from "0" to CONTROL.DATA_NR. Default Value: Undefined

8.1.3 DMAC_STATUS_SRC_ADDR

Source address status register

Address: 0x40101014

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Base address or current address of source location of currently active channel. The specific address information is cycle dependent. This field is provided for debug purposes. Functionally, no assumption should be made on whether the base or current address is provided. The specifics of the currently active channel are available through STATUS. Note while reading the STATUS, STATUS_SRC_ADDR and STATUS_DST_ADDR registers, the transfer engine may have moved from one active channel to another. Default Value: Undefined

8.1.4 DMAC_STATUS_DST_ADDR

Destination address register

Address: 0x40101018

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Base address or current address of destination location of currently active channel. The specific address information is cycle dependent. This field is provided for debug purposes. Functionally, no assumption should be made on whether the base or current address is provided. The specifics of the currently active channel are available through STATUS. Note while reading the STATUS, STATUS_SRC_ADDR and STATUS_DST_ADDR registers, the transfer engine may have moved from one active channel to another. Default Value: Undefined

8.1.5 DMAC_STATUS_CH_ACT

Channel activation status register

Address: 0x4010101C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	CH [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	CH [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CH	Channel activation status. Bit i is associated to channel i, with i = 0, ..., CH_NR-1. Software reads this field to get information on all actively pending channels (either in pending or in the data transfer engine). Default Value: 0

8.1.6 DMAC_CH_CTL0

Channel control register

Address: 0x40101080

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW		None			
HW Access	RW1C	RW	R		None			
Name	ENABLED	PING_PONG	PRIO [29:28]		None [27:24]			

Bits	Name	Description
31	ENABLED	'0': channel disabled. The channel's trigger is ignored and the channel cannot be activated. If the activated channel is disabled, the data transfer(s) are aborted. '1': channel enabled. Software sets this field to '1' to enable a specific channel. Hardware sets this field to '0' on erroneous channel behavior (the specific error is specified by STATUS.RESP in the channel's descriptor structure). Default Value: 0
30	PING_PONG	Each channel has two descriptor structures for double buffering purposes. As the controller operates on one structure, the main CPU can operate on the other structure. The descriptor structures are identified as PING ('0') and PONG ('1'). This field identifies the descriptor structure that is currently in use by the controller. Software sets this field to the desired descriptor structure. Hardware inverts the field value on the completion of a descriptor structure when CONTROL.FLIPPING of the current descriptor structure is set to '1'. Default Value: 0

8.1.6 DMAC_CH_CTL0 (continued)

29 : 28	PRIO	Channel priority, with "0" representing the highest priority and "3" representing the lowest priority. Priority decoding uses the channel priority to determine the highest priority activated channel. If multiple activated channels have the same highest priority, the channel with the lowest index i, is considered the highest priority activated channel. Default Value: 0

8.1.7 DMAC_INTR

Interrupt register

Address: 0x401017F0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C							
HW Access	RW1S							
Name	CH [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1C							
HW Access	RW1S							
Name	CH [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CH	Set to '1', when event is detected. Write INTR field with '1', to clear bit. Write INTR_SET field with '1', to set bit. Default Value: 0

8.1.8 DMAC_INTR_SET

Interrupt set register

Address: 0x401017F4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S							
HW Access	A							
Name	CH [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1S							
HW Access	A							
Name	CH [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CH	Write INTR_SET field with '1' to set corresponding INTR field (a write of '0' has no effect). Default Value: 0

8.1.9 DMAC_INTR_MASK

Interrupt mask register

Address: 0x401017F8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CH [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CH [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CH	Mask for corresponding field in INTR register. Default Value: 0

8.1.10 DMAC_INTR_MASKED

Interrupt masked register

Address: 0x401017FC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	CH [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	CH [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CH	Logical BITWISE AND of corresponding request and mask fields. Default Value: 0

8.1.11 DMAC_DESCR0_PING_SRC

Ping source address

Address: 0x40101800

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Base address of source location. The effective source location is calculated by adding on offset (derived from PING.STATUS.CURR_DATA_NR) to this base address. Default Value: Undefined

8.1.12 DMAC_DESCR0_PING_DST

Ping destination address

Address: 0x40101804

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	Base address of destination location. The effective destination location is calculated by adding on offset (derived from PING.STATUS.CURR_DATA_NR) to this base address. Default Value: Undefined

8.1.13 DMAC_DESCR0_PING_CTL

Ping control word

Address: 0x40101808

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	None		RW	
HW Access	RW	RW	RW	RW	None		RW	
Name	SRC_AD-DR_INCR	SRC_TRAN SFER_SIZE	DST_AD-DR_INCR	DST_TRAN SFER_SIZE	None [19:18]		DATA_SIZE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW		RW	RW	RW	RW	RW	
HW Access	RW		RW	RW	RW	RW	RW	
Name	OPCODE [31:30]		FLIPPING	PREEMPT-ABLE	SET_-CAUSE	INV_DE-SCR	WAIT_FOR_DEACT [25:24]	

Bits	Name	Description

8.1.13 DMAC_DESCR0_PING_CTL (continued)

31 : 30	OPCODE	Specifies the specific data transfer (only when the VALID bit of the descriptor's STATUS word is '1'): "0": A single trigger initiates a single data element transfer (DW mode). This opcode specifies a transfer of a single data element. The current descriptor is completed when the amount of transferred single data elements equals the programmed buffer size (DATA_NR+1). "1": A single trigger initiates a single descriptor transfer (DMA mode). This opcode specifies a transfer of DATA_NR+1 data elements as specified by the current descriptor structure. The current descriptor is completed when its data transfer is completed. "2": A single trigger initiates a descriptor list transfer (DMA mode). This opcode specifies a transfer of DATA_NR+1 data elements as specified by the current descriptor structure and by successive valid descriptors. The current descriptor is completed when its data transfer is completed. This OPCODE relies on FLIPPING to be set to '1', such that the CH_CTLi.PING_PONG field is flipped/inverted and the successive descriptor is used. This continues for as long as the successive descriptor is valid. Note that as the HW is using the PING/PONG descriptor, the SW can prepare the alternate PONG/PING descriptor. The interrupt mechanism is used by HW to convey to the SW that the current descriptor is completed (and can be prepared for a successive transfer). After completerion of the opcode (and waiting for de-activation, the channel's output trigger is activated). Default Value: Undefined
29	FLIPPING	'1': On completion of the current descriptor structure, the current descriptor identifier CH_CTLi.PING_PONG is flipped/inverted. In DMA mode, descriptor list transfer, flipping of the current descriptor identifier can be used to construct a linked list of descriptor structures. Default Value: Undefined
28	PREEMPTABLE	'1': Transfer is preemptable. In DMA mode (OPCODE is "1" or "2"), multi data element transfers are constructed out of multiple single data element load (from the source location) and store (to the destination location) sequences. This field allows higher priority activated channels to preempt the current transfer in between these atomic (load, store) sequences. Preemption will NOT deactivate the current channel. As a result, after completion of a higher priority activated channel, the current channel is rescheduled. Default Value: Undefined
27	SET_CAUSE	'1': On completion of the current descriptor structure, the interrupt cause field of the channel is set to '1' (INTR.CH[i]). Default Value: Undefined
26	INV_DESCR	'1': On completion of the current descriptor structure, the VALID bit of the descriptor's STATUS word is set to '0'. Default Value: Undefined

8.1.13 DMAC_DESCR0_PING_CTL (continued)

25 : 24	WAIT_FOR_DEACT	Specifies whether the data transfer engine should wait for the channel to be deactivated; i.e. the selected system trigger is not active. This field is used to synchronize the controller's data transfer(s) with the agent that generated the trigger. This field is ONLY used at the completion of an opcode. E.g., a FIFO indicates that it is empty and it needs a new data sample. The agent removes the trigger ONLY when the data sample has been written by the transfer engine AND received by the agent. Furthermore, the agent's trigger may be delayed by a few cycles before it reaches the DW/DMA controller. This field is used for level sensitive trigger, which reflect state (pulse sensitive triggers should have this field set to "0"). The wait cycles incurred by this field reduce DW/DMA controller performance. "0": Do not wait for de-activation (for pulse sensitive triggers). "1": Wait for up to 4 cycles. "2": Wait for up to 8 cycles. "3": Wait indefinitely. This option may result in DW/DMA controller lockup if the system trigger is not de-activated by the source agent. Default Value: Undefined
23	SRC_ADDR_INCR	Specifies whether the source location address is incremented by the SRC_TRANSFER_SIZE after each single data element transfer or not. '0': No increment, typically used for receive (RX) FIFO structures. '1': Increment, typically used for memory structures. Default Value: Undefined
22	SRC_TRANSFER_SIZE	Specifies the bus transfer size to the source location: '0': As specified by DATA_SIZE. '1': Word (32 bits). Distinguishing bus transfer size from data element size allows for source components with data elements that are smaller than their 32-bit bus interface width. E.g., an ADC source has a 32-bit bus transfer size, but only provides a 16-bit data element. Default Value: Undefined
21	DST_ADDR_INCR	Specifies whether the destination location address is incremented by the DST_TRANSFER_SIZE after each single data element transfer or not. '0' : No increment, typically used for transmit (TX) FIFO structures. '1': Increment, typically used for memory structures. Default Value: Undefined
20	DST_TRANSFER_SIZE	Specifies the bus transfer size to the destination location: '0': As specified by DATA_SIZE. '1': Word (32 bits). Distinguishing bus transfer size from data element size allows for destination components with data elements that are smaller than their 32-bit bus interface width. E.g., a DAC destination has a 32-bit bus transfer size, but only requires a 16-bit data element. Default Value: Undefined

8.1.13 DMAC_DESCR0_PING_CTL (continued)

17 : 16	DATA_SIZE	Specifies the data element size: "0": Byte (8 bits). "1": Halfword (16 bits). "2": Word (32 bits). DATA_SIZE, SRC_TRANSFER_SIZE and DST_TRANSFER_SIZE together determine how data elements are transferred. The following are the 9 legal settings: - DATA is 8 bit, SRC is 8 bit, DST is 8 bit - DATA is 8 bit, SRC is 32 bit (higher 24 bits are dropped), DST is 8 bit - DATA is 8 bit, SRC is 8 bit, DST is 32 bit (higher 24 bits are made "0") - DATA is 8 bit, SRC is 32 bit (higher 24 bits are dropped), DST is 32 bit (higher 24 bits are made "0") - DATA is 16 bit, SRC is 16 bit, DST is 16 bit - DATA is 16 bit, SRC is 32 bit (higher 16 bits are dropped), DST is 16 bit - DATA is 16 bit, SRC is 16 bit, DST is 32 bit (higher 16 bits are made "0") - DATA is 16 bit, SRC is 32 bit (higher 16 bits are dropped), DST is 32 bit (higher 16 bits are made "0") - DATA is 32 bit, SRC is 32 bit, DST is 32 bit Default Value: Undefined
15 : 0	DATA_NR	Number of data elements that are transferred by a single descriptor. In DW mode (OPCODE is "0") each trigger initiates the transfer of a single data element. This field specifies the source and/or destination buffer size in data elements: buffer size = DATA_NR+1. The buffer is typically associated to a memory structure. In DMA mode (OPCODE is "1" or "2") each trigger initiates the transfer of DATA_NR+1 data elements. Default Value: Undefined

8.1.14 DMAC_DESCR0_PING_STATUS

Ping status word

Address: 0x4010180C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None					RW		
HW Access	None					RW		
Name	None [23:19]					RESPONSE [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	RW	None						
Name	VALID	None [30:24]						

Bits	Name	Description
31	VALID	'0': Invalid, cannot be used for a data transfer. An attempt to use this descriptor for a data transfer will result in an INVALID_DESCR response code (and the interrupt cause bit is set to '1'). '1': Valid. Hardware set this field to '0' when a descriptor is done, but only if CONTROL.INV_DESCR is '1'. Software sets this field to '1' when a descriptor is initialized. Default Value: Undefined

8.1.14 DMAC_DESCR0_PING_STATUS (continued)

18 : 16	RESPONSE	Response code (the first two codes NO_ERROR and DONE are the result of normal behavior, the other codes are the result of erroneous behavior). "0"/NO_ERROR: No error. Setting this response does NOT set the interrupt cause bit to '1'. STATUS.VALID is NOT affected. CH_CTLi.ENABLED is NOT affected. CH_CTLi.PING_PONG is not updated. This response is used for an unused or not completed descriptor. Software should set the RESPONSE field to "0"/NO_ERROR during descriptor initialization. "1"/DONE: Descriptor is done (without errors). Setting this response sets the interrupt cause bit to '1' if CONTROL.SET_CAUSE is '1'. STATUS.VALID is set to '0' if CONTROL.INV_DESCR is '1'. CH_CTLi.ENABLED is NOT affected. CH_CTLi.PING_PONG is updated if CONTROL.FLIPPING is '1'. "2"/SRC_BUS_ERROR: Bus error while loading data from the source location. Setting this response sets the interrupt cause bit to '1'. STATUS.VALID is set '0'. CH_CTLi.ENABLED is set to '0'. CH_CTLi.PING_PONG is not updated (it identifies the descriptor that caused the error). "3"/DST_BUS_ERROR: Bus error while storing data to the destination location. Setting this response sets the interrupt cause bit to '1'. STATUS.VALID is set '0'. CH_CTLi.ENABLED is set to '0'. CH_CTLi.PING_PONG is not updated (it identifies the descriptor that caused the error). "4"/SRC_MISAL: Misalignment of source address. This occurs on a 16-bit bus transfer that is not 2-byte aligned or on a 32-bit bus transfer that is not 4-byte aligned. Setting this response sets the interrupt cause bit to '1'. STATUS.VALID is set '0'. CH_CTLi.ENABLED is set to '0'. CH_CTLi.PING_PONG is not updated (it identifies the descriptor that caused the error). "5"/DST_MISAL: Misalignment of destination address. This occurs on a 16-bit bus transfer that is not 2-byte aligned or on a 32-bit bus transfer that is not 4-byte aligned. Setting this response sets the interrupt cause bit to '1'. STATUS.VALID is set '0'. CH_CTLi.ENABLED is set to '0'. CH_CTLi.PING_PONG is not updated (it identifies the descriptor that caused the error). "6"/INVALID_DESCR: Invalid descriptor (STATUS.VALID is '0'). This occurs when an activated channel has an invalid descriptor. CH_CTLi.ENABLED is set to '0'. CH_CTLi.PING_PONG is not updated (it identifies the descriptor that caused the error). Default Value: Undefined
15 : 0	CURR_DATA_NR	Specifies the index of the current data transfer. This value increases from 0 to CONTROL.DATA_NR. HW sets this field: - When a descriptor is done (RESPONSE is DONE), the field is set to "0" when PING_CTL.INV_DESCR is '0' and the field is set to PING_CTL.DATA_NR when PING_CTL.INV_DESCR is '1'. - When a descriptor is not done (RESPONSE is NO_ERROR), the field reflects the progress of a data transfer. - In case of erroneous behavior (RESPONSE is neither DONE or NO_ERROR), the field is not updated, but keeps its value to ease debugging. HW only modifies this field for an active descriptor (STATUS.VALID to be '1'). At descriptor initialization, SW should set this field to "0". This field allows software to read the progress of the data transfer. Note that SRC.ADDR and DST.ADDR represent base addresses and are not modified during data transfer. However, STATUS.CURR_DATA_NR is modified during data transfer and provides an offset wrt. the base addresses. Default Value: Undefined

8.1.15 DMAC_DESCR0_PONG_SRC

Pong source address

Address: 0x40101810

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	See description of PING_SRC. Default Value: Undefined

8.1.16 DMAC_DESCR0_PONG_DST

Pong destination address

Address: 0x40101814

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	ADDR [31:24]							

Bits	Name	Description
31 : 0	ADDR	See description of PING_DST. Default Value: Undefined

8.1.17 DMAC_DESCR0_PONG_CTL

Pong control word

Address: 0x40101818

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	None		RW	
HW Access	RW	RW	RW	RW	None		RW	
Name	SRC_AD-DR_INCR	SRC_TRAN SFER_SIZE	DST_AD-DR_INCR	DST_TRAN SFER_SIZE	None [19:18]		DATA_SIZE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	RW		RW	RW	RW	RW	RW	
HW Access	RW		RW	RW	RW	RW	RW	
Name	OPCODE [31:30]		FLIPPING	PREEMPT-ABLE	SET_-CAUSE	INV_DE-SCR	WAIT_FOR_DEACT [25:24]	

Bits	Name	Description
31 : 30	OPCODE	See description of PING_CTL. Default Value: Undefined
29	FLIPPING	See description of PING_CTL. Default Value: Undefined
28	PREEMPTABLE	See description of PING_CTL. Default Value: Undefined
27	SET_CAUSE	See description of PING_CTL. Default Value: Undefined
26	INV_DESCR	See description of PING_CTL. Default Value: Undefined
25 : 24	WAIT_FOR_DEACT	See description of PING_CTL. Default Value: Undefined
23	SRC_ADDR_INCR	See description of PING_CTL. Default Value: Undefined

8.1.17 DMAC_DESCR0_PONG_CTL (continued)

22	SRC_TRANSFER_SIZE	See description of PING_CTL. Default Value: Undefined
21	DST_ADDR_INCR	See description of PING_CTL. Default Value: Undefined
20	DST_TRANSFER_SIZE	See description of PING_CTL. Default Value: Undefined
17 : 16	DATA_SIZE	See description of PING_CTL. Default Value: Undefined
15 : 0	DATA_NR	See description of PING_CTL. Default Value: Undefined

8.1.18 DMAC_DESCR0_PONG_STATUS

Pong status word

Address: 0x4010181C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CURR_DATA_NR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None					RW		
HW Access	None					RW		
Name	None [23:19]					RESPONSE [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	RW	None						
Name	VALID	None [30:24]						

Bits	Name	Description
31	VALID	See description of PING_STATUS. Default Value: Undefined
18 : 16	RESPONSE	See description of PING_STATUS. Default Value: Undefined
15 : 0	CURR_DATA_NR	See description of PING_STATUS. Default Value: Undefined

9 SPC Interface (SPCIF) Registers

This section discusses the System Performance Controller Interface (SPCIF) registers. It lists all the registers in mapping tables, in address order.

9.1 Register Details

Register	Address	Description
SPCIF_GEOMETRY	0x40110000	Flash/NVL geometry information
SPCIF_INTR	0x401107F0	SPCIF interrupt request register
SPCIF_INTR_SET	0x401107F4	SPCIF interrupt set request register
SPCIF_INTR_MASK	0x401107F8	SPCIF interrupt mask register
SPCIF_INTR_MASKED	0x401107FC	SPCIF interrupt masked request register

9.1.1 SPCIF_GEOMETRY

Flash/NVL geometry information

Address: 0x40110000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	FLASH [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R		R					
HW Access	W		W					
Name	SFLASH [15:14]		FLASH [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	R		R		R			
HW Access	W		W		W			
Name	FLASH_ROW [23:22]		NUM_FLASH [21:20]		SFLASH [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access		None						
Name	DE_CP-D_LP	None [30:24]						

Bits	Name	Description
31	DE_CPD_LP	0': SRAM busy wait loop has not been copied. '1': Busy wait loop has been written into SRAM. Default Value: 0
23 : 22	FLASH_ROW	Page size in 64 Byte multiples (chip dependent): "0": 64 byte "1": 128 byte "2": 192 byte "3": 256 byte The page size is used to detemine the number of Bytes in a page for Flash page based operations (e.g. PGM_PAGE). Note: the field name FLASH_ROW is misleading, as this field specifies the number of Bytes in a page, rather than the number of Bytes in a row. In a single plane flash macro architecture, a page consists of a single row. However, in a multi plane flash macro architecture, a page consists of multiple rows from different planes. Default Value: Undefined

9.1.1 SPCIF_GEOMETRY (continued)

21 : 20	NUM_FLASH	Number of flash macros (chip dependent): "0": 1 flash macro "1": 2 flash macros "2": 3 flash macros "3": 4 flash macros Default Value: Undefined
19 : 14	SFLASH	Supervisory flash capacity in 256 Byte multiples (chip dependent). If multiple flash macros are present, this field provides the supervisory flash capacity of all flash macros together: "0": 256 Bytes. "1": 2*256 Bytes. ... "63": 64*256 Bytes. Default Value: Undefined
13 : 0	FLASH	Regular flash capacity in 256 Byte multiples (chip dependent). If multiple flash macros are present, this field provides the flash capacity of all flash macros together: "0": 256 Bytes. "1": 2*256 Bytes. ... "16383": 16384*256 Bytes. Default Value: Undefined

9.1.2 SPCIF_INTR

SPCIF interrupt request register

Address: 0x401107F0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1C
HW Access	None							RW1S
Name	None [7:1]							TIMER

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	TIMER	Timer counter value reaches "0". Set to '1', when event is detected. Write INTR field with '1', to clear bit. Write INTR_SET field with '1', to set bit. Default Value: 0

9.1.3 SPCIF_INTR_SET

SPCIF interrupt set request register

Address: 0x401107F4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1S
HW Access	None							A
Name	None [7:1]							TIMER

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	TIMER	Write INTR_SET field with '1' to set corresponding INTR field. Default Value: 0

9.1.4 SPCIF_INTR_MASK

SPCIF interrupt mask register

Address: 0x401107F8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							TIMER

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	TIMER	Mask for corresponding field in INTR register. Default Value: 0

9.1.5 SPCIF_INTR_MASKED

SPCIF interrupt masked request register

Address: 0x401107FC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							W
Name	None [7:1]							TIMER

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	TIMER	Logical and of corresponding request and mask fields. Default Value: 0

10 Control Area Network (TTCANFD) Registers

This section discusses the Control Area Network (TTCANFD/M_TTCAN) registers. It lists all the registers in mapping tables, in address order.

10.1 Register Details

Register	Address	Description
CANFD0_CH0_CREL	0x40400000	Core Release Register
CANFD0_CH0_ENDN	0x40400004	Endian Register
CANFD0_CH0_DBTP	0x4040000C	Data Bit Timing & Prescaler Register
CANFD0_CH0_TEST	0x40400010	Test Register
CANFD0_CH0_RWD	0x40400014	RAM Watchdog
CANFD0_CH0_CCCR	0x40400018	CC Control Register
CANFD0_CH0_NBTP	0x4040001C	Nominal Bit Timing & Prescaler Register
CANFD0_CH0_TSCC	0x40400020	Timestamp Counter Configuration
CANFD0_CH0_TSCV	0x40400024	Timestamp Counter Value
CANFD0_CH0_TOCC	0x40400028	Timeout Counter Configuration
CANFD0_CH0_TOCV	0x4040002C	Timeout Counter Value
CANFD0_CH0_ECR	0x40400040	Error Counter Register
CANFD0_CH0_PSR	0x40400044	Protocol Status Register
CANFD0_CH0_TDCR	0x40400048	Transmitter Delay Compensation Register
CANFD0_CH0_IR	0x40400050	Interrupt Register
CANFD0_CH0_IE	0x40400054	Interrupt Enable
CANFD0_CH0_ILS	0x40400058	Interrupt Line Select
CANFD0_CH0_ILE	0x4040005C	Interrupt Line Enable
CANFD0_CH0_GFC	0x40400080	Global Filter Configuration
CANFD0_CH0_SIDFC	0x40400084	Standard ID Filter Configuration
CANFD0_CH0_XIDFC	0x40400088	Extended ID Filter Configuration
CANFD0_CH0_XIDAM	0x40400090	Extended ID AND Mask
CANFD0_CH0_HPMS	0x40400094	High Priority Message Status
CANFD0_CH0_NDAT1	0x40400098	New Data 1
CANFD0_CH0_NDAT2	0x4040009C	New Data 2
CANFD0_CH0_RXF0C	0x404000A0	Rx FIFO 0 Configuration

Register	Address	Description
CANFD0_CH0_RXF0S	0x404000A4	Rx FIFO 0 Status
CANFD0_CH0_RXF0A	0x404000A8	Rx FIFO 0 Acknowledge
CANFD0_CH0_RXBC	0x404000AC	Rx Buffer Configuration
CANFD0_CH0_RXF1C	0x404000B0	Rx FIFO 1 Configuration
CANFD0_CH0_RXF1S	0x404000B4	Rx FIFO 1 Status
CANFD0_CH0_RXF1A	0x404000B8	Rx FIFO 1 Acknowledge
CANFD0_CH0_RXESC	0x404000BC	Rx Buffer / FIFO Element Size Configuration
CANFD0_CH0_TXBC	0x404000C0	Tx Buffer Configuration
CANFD0_CH0_TXFQS	0x404000C4	Tx FIFO/Queue Status
CANFD0_CH0_TXESC	0x404000C8	Tx Buffer Element Size Configuration
CANFD0_CH0_TXBRP	0x404000CC	Tx Buffer Request Pending
CANFD0_CH0_TXBAR	0x404000D0	Tx Buffer Add Request
CANFD0_CH0_TXBCR	0x404000D4	Tx Buffer Cancellation Request
CANFD0_CH0_TXBTO	0x404000D8	Tx Buffer Transmission Occurred
CANFD0_CH0_TXBCF	0x404000DC	Tx Buffer Cancellation Finished
CANFD0_CH0_TXBTIE	0x404000E0	Tx Buffer Transmission Interrupt Enable
CANFD0_CH0_TXBCIE	0x404000E4	Tx Buffer Cancellation Finished Interrupt Enable
CANFD0_CH0_TXEFC	0x404000F0	Tx Event FIFO Configuration
CANFD0_CH0_TXEFS	0x404000F4	Tx Event FIFO Status
CANFD0_CH0_TXEFA	0x404000F8	Tx Event FIFO Acknowledge
CANFD0_CH0_TTTMC	0x40400100	TT Trigger Memory Configuration
CANFD0_CH0_TTRMC	0x40400104	TT Reference Message Configuration
CANFD0_CH0_TTOCF	0x40400108	TT Operation Configuration
CANFD0_CH0_TTMLM	0x4040010C	TT Matrix Limits
CANFD0_CH0_TURCF	0x40400110	TUR Configuration
CANFD0_CH0_TTOCN	0x40400114	TT Operation Control
CANFD0_CH0_TTGTP	0x40400118	TT Global Time Preset
CANFD0_CH0_TTTMK	0x4040011C	TT Time Mark
CANFD0_CH0_TTIR	0x40400120	TT Interrupt Register
CANFD0_CH0_TTIE	0x40400124	TT Interrupt Enable
CANFD0_CH0_TTILS	0x40400128	TT Interrupt Line Select
CANFD0_CH0_TTOST	0x4040012C	TT Operation Status
CANFD0_CH0_TURNA	0x40400130	TUR Numerator Actual
CANFD0_CH0_TTLGT	0x40400134	TT Local & Global Time
CANFD0_CH0_TTCTC	0x40400138	TT Cycle Time & Count
CANFD0_CH0_TTCPT	0x4040013C	TT Capture Time
CANFD0_CH0_TTCSM	0x40400140	TT Cycle Sync Mark
CANFD0_CH0_RXFTOP_CTL	0x40400180	Receive FIFO Top control
CANFD0_CH0_RXFTOP0_STAT	0x404001A0	Receive FIFO 0 Top Status
CANFD0_CH0_RXFTOP0_DATA	0x404001A8	Receive FIFO 0 Top Data
CANFD0_CH0_RXFTOP1_STAT	0x404001B0	Receive FIFO 1 Top Status
CANFD0_CH0_RXFTOP1_DATA	0x404001B8	Receive FIFO 1 Top Data

Register	Address	Description
CANFD0_CTL	0x40401000	Global CAN control register
CANFD0_STATUS	0x40401004	Global CAN status register
CANFD0_INTR0_CAUSE	0x40401010	Consolidated interrupt0 cause register
CANFD0_INTR1_CAUSE	0x40401014	Consolidated interrupt1 cause register
CANFD0_TS_CTL	0x40401020	Time Stamp control register
CANFD0_TS_CNT	0x40401024	Time Stamp counter value

10.1.1 CANFD0_CH0_CREL

Core Release Register

Address: 0x40400000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	DAY [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	MON [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R				R			
HW Access	R				R			
Name	SUBSTEP [23:20]				YEAR [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	R				R			
HW Access	R				R			
Name	REL [31:28]				STEP [27:24]			

Bits	Name	Description
31 : 28	REL	Core Release One digit, BCD-coded. Default Value: 0
27 : 24	STEP	Step of Core Release One digit, BCD-coded. Default Value: 0
23 : 20	SUBSTEP	Sub-step of Core Release One digit, BCD-coded. Default Value: 0
19 : 16	YEAR	Time Stamp Year One digit, BCD-coded. This field is set by generic parameter on M_TTCAN synthesis. Default Value: 0
15 : 8	MON	Time Stamp Month Two digits, BCD-coded. This field is set by generic parameter on M_TTCAN synthesis. Default Value: 0
7 : 0	DAY	Time Stamp Day Two digits, BCD-coded. This field is set by generic parameter on M_TTCAN synthesis. Default Value: 0

10.1.2 CANFD0_CH0_ENDN

Endian Register

Address: 0x40400004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	ETV [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	ETV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ETV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ETV [31:24]							

Bits	Name	Description
31 : 0	ETV	Endianness Test Value The endianness test value is 0x87654321. Default Value: 2271560481

10.1.3 CANFD0_CH0_DBTP

Data Bit Timing & Prescaler Register

Address: 0x4040000C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	DTSEG2 [7:4]				DSJW [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW				
HW Access	None			R				
Name	None [15:13]			DTSEG1 [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	RW	None		RW				
HW Access	R	None		R				
Name	TDC	None [22:21]		DBRP [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23	TDC	Transmitter Delay Compensation 0= Transmitter Delay Compensation disabled 1= Transmitter Delay Compensation enabled Default Value: 0
20 : 16	DBRP	Data Bit Rate Prescaler 0x00-0x1F The value by which the oscillator frequency is divided for generating the bit time quanta. The bit time is built up from a multiple of this quanta. Valid values for the Bit Rate Prescaler are 0 to 31. The actual interpretation by the hardware of this value is such that one more than the value programmed here is used. Default Value: 0
12 : 8	DTSEG1	Data time segment before sample point 0x00-0x1F Valid values are 0 to 31. The actual interpretation by the hardware of this value is such that one more than the programmed value is used. Default Value: 10
7 : 4	DTSEG2	Data time segment after sample point 0x0-0xF Valid values are 0 to 15. The actual interpretation by the hardware of this value is such that one more than the programmed value is used. Default Value: 3

10.1.3 CANFD0_CH0_DBTP (continued)

3 : 0	DSJW	Data (Re)Synchronization Jump Width 0x0-0xF Valid values are 0 to 15. The actual interpretation by the hardware of this value is such that one more than the value programmed here is used. Default Value: 3

10.1.4 CANFD0_CH0_TEST

Test Register

Address: 0x40400010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	RW		RW	RW	RW	RW	RW
HW Access	R	R		R	R	R	R	R
Name	RX	TX [6:5]		LBCK	CAT	CAM	TAT	TAM

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	RX	Receive Pin Monitors the actual value of pin m_ttcan_rx 0= The CAN bus is dominant (m_ttcan_rx = '0') 1= The CAN bus is recessive (m_ttcan_rx = '1') Default Value: Undefined
6 : 5	TX	Control of Transmit Pin 00 Reset value, m_ttcan_tx controlled by the CAN Core, updated at the end of the CAN bit time 01 Sample Point can be monitored at pin m_ttcan_tx 10 Dominant ('0') level at pin m_ttcan_tx 11 Recessive ('1') at pin m_ttcan_tx Default Value: 0
4	LBCK	Loop Back Mode 0= Reset value, Loop Back Mode is disabled 1= Loop Back Mode is enabled (see Section 3.1.9, Test Modes) Default Value: 0

10.1.4 CANFD0_CH0_TEST (continued)

3	CAT	ASC is not supported by M_TTCAN Check ASC Transmit Control Monitors level at output pin m_ttcan_asct. 0= Output pin m_ttcan_asct = '0' Default Value: 0
2	CAM	ASC is not supported by M_TTCAN Check ASC Multiplexer Control Monitors level at output pin m_ttcan_ascm. 0= Output pin m_ttcan_ascm = '0' 1= Output pin m_ttcan_ascm = '1' Default Value: 0
1	TAT	ASC is not supported by M_TTCAN Test ASC Transmit Control Controls output pin m_ttcan_asct in test mode, ORed with the signal from the FSE 0= Level at pin m_ttcan_asct controlled by FSE 1= Level at pin m_ttcan_asct = '1' Default Value: 0
0	TAM	ASC is not supported by M_TTCAN Test ASC Multiplexer Control Controls output pin m_ttcan_ascm in test mode, ORed with the signal from the FSE 0= Level at pin m_ttcan_ascm controlled by FSE 1= Level at pin m_ttcan_ascm = '1' Default Value: 0

10.1.5 CANFD0_CH0_RWD

RAM Watchdog

Address: 0x40400014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	WDC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	WDV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 8	WDV	Watchdog Value Actual Message RAM Watchdog Counter Value. Default Value: 0
7 : 0	WDC	Watchdog Configuration Start value of the Message RAM Watchdog Counter. With the reset value of '00' the counter is disabled. Default Value: 0

10.1.6 CANFD0_CH0_CCCR

CC Control Register

Address: 0x40400018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	TEST	DAR	MON_	CSR	CSA	ASM	CCE	INIT

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	None		RW	RW
HW Access	R	R	R	R	None		R	R
Name	NISO	TXP	EFBI	PXHD	None [11:10]		BRSE	FDOE

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15	NISO	Non ISO Operation If this bit is set, the M_TTCAN uses the CAN FD frame format as specified by the Bosch CAN FD Specification V1.0. 0= CAN FD frame format according to ISO 11898-1:2015 1= CAN FD frame format according to Bosch CAN FD Specification V1.0 addressing the non-ISO CAN FD Default Value: 0
14	TXP	Transmit Pause If this bit is set, the M_TTCAN pauses for two CAN bit times before starting the next transmission after itself has successfully transmitted a frame (see Section 3.5). 0= Transmit pause disabled 1= Transmit pause enabled Default Value: 0
13	EFBI	Edge Filtering during Bus Integration 0= Edge filtering disabled 1= Two consecutive dominant tq required to detect an edge for hard synchronization Default Value: 0

10.1.6 CANFD0_CH0_CCCR (continued)

12	PXHD	Protocol Exception Handling Disable 0= Protocol exception handling enabled 1= Protocol exception handling disabled Default Value: 0
9	BRSE	Bit Rate Switch Enable 0= Bit rate switching for transmissions disabled 1= Bit rate switching for transmissions enabled Default Value: 0
8	FDOE	FD Operation Enable 0= FD operation disabled 1= FD operation enabled Default Value: 0
7	TEST	Test Mode Enable 0= Normal operation, register TEST holds reset values 1= Test Mode, write access to register TEST enabled Default Value: 0
6	DAR	Disable Automatic Retransmission 0= Automatic retransmission of messages not transmitted successfully enabled 1= Automatic retransmission disabled Default Value: 0
5	MON_	Bus Monitoring Mode Bit MON can only be set by the Host when both CCE and INIT are set to '1'. The bit can be reset by the Host at any time. 0= Bus Monitoring Mode is disabled 1= Bus Monitoring Mode is enabled Default Value: 0
4	CSR	Clock Stop Request, not supported by M_TTCAN use CTL.STOP_REQ at the group level instead. 0= No clock stop is requested 1= Clock stop requested. When clock stop is requested, first INIT and then CSA will be set after all pending transfer requests have been completed and the CAN bus reached idle. Default Value: 0
3	CSA	Clock Stop Acknowledge 0= No clock stop acknowledged 1= M_TTCAN may be set in power down by stopping m_ttcan_hclk and m_ttcan_cclk Default Value: 0
2	ASM	Restricted Operation Mode Bit ASM can only be set by the Host when both CCE and INIT are set to '1'. The bit can be reset by the Host at any time. For a description of the Restricted Operation Mode see Section 3.1.5. 0= Normal CAN operation 1= Restricted Operation Mode active Default Value: 0
1	CCE	Configuration Change Enable 0= The CPU has no write access to the protected configuration registers 1= The CPU has write access to the protected configuration registers (while CCCR.INIT = '1') Default Value: 0
0	INIT	Initialization 0= Normal Operation 1= Initialization is started Default Value: 1

10.1.7 CANFD0_CH0_NBTP

Nominal Bit Timing & Prescaler Register

Address: 0x4040001C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW						
HW Access	None	R						
Name	None	NTSEG2 [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	NTSEG1 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	NBRP [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							RW
HW Access	R							R
Name	NSJW [31:25]							NBRP

Bits	Name	Description
31 : 25	NSJW	Nominal (Re)Synchronization Jump Width 0x00-0x7F Valid values are 0 to 127. The actual interpretation by the hardware of this value is such that one more than the value programmed here is used. Default Value: 3
24 : 16	NBRP	Nominal Bit Rate Prescaler 0x000-0x1FFThe value by which the oscillator frequency is divided for generating the bit time quanta. The bit time is built up from a multiple of this quanta. Valid values for the Bit Rate Prescaler are 0 to 511. The actual interpretation by the hardware of this value is such that one more than the value programmed here is used. Default Value: 0
15 : 8	NTSEG1	Nominal Time segment before sample point 0x01-0xFF Valid values are 1 to 255. The actual interpretation by the hardware of this value is such that one more than the programmed value is used. Default Value: 10
6 : 0	NTSEG2	Nominal Time segment after sample point 0x01-0x7F Valid values are 1 to 127. The actual interpretation by the hardware of this value is such that one more than the programmed value is used. Default Value: 3

10.1.8 CANFD0_CH0_TSCC

Timestamp Counter Configuration

Address: 0x40400020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	
HW Access	None						R	
Name	None [7:2]						TSS [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				TCP [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	TCP	Timestamp Counter Prescaler (still used for TOCC) 0x0-0xF Configures the timestamp and timeout counters time unit in multiples of CAN bit times [1...16]. The actual interpretation by the hardware of this value is such that one more than the value programmed here is used. Default Value: 0
1 : 0	TSS	Timestamp Select, should always be set to external timestamp counter 00= Timestamp counter value always 0x0000 01= Timestamp counter value incremented according to TCP 10= External timestamp counter value used 11= Same as '00' Default Value: 0

10.1.9 CANFD0_CH0_TSCV

Timestamp Counter Value

Address: 0x40400024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	TSC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	TSC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	TSC	Timestamp Counter, not used for M_TTCAN The internal/external Timestamp Counter value is captured on start of frame (both Rx and Tx). When TSCC.TSS = '01', the Timestamp Counter is incremented in multiples of CAN bit times [1...16] depending on the configuration of TSCC.TCP. A wrap around sets interrupt flag IR.TSW. Write access resets the counter to zero. When TSCC.TSS = '10', TSC reflects the external Timestamp Counter value. A write access has no impact. Default Value: 0

10.1.10 CANFD0_CH0_TOCC

Timeout Counter Configuration

Address: 0x40400028

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW		RW
HW Access	None					R		R
Name	None [7:3]					TOS [2:1]		ETOC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	TOP [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	TOP [31:24]							

Bits	Name	Description
31 : 16	TOP	Timeout Period Start value of the Timeout Counter (down-counter). Configures the Timeout Period. Default Value: 65535
2 : 1	TOS	Timeout Select When operating in Continuous mode, a write to TOCV presets the counter to the value configured by TOCC.TOP and continues down-counting. When the Timeout Counter is controlled by one of the FIFOs, an empty FIFO presets the counter to the value configured by TOCC.TOP. Down-counting is started when the first FIFO element is stored. 00= Continuous operation 01= Timeout controlled by Tx Event FIFO 10= Timeout controlled by Rx FIFO 0 11= Timeout controlled by Rx FIFO 1 Default Value: 0

10.1.10 CANFD0_CH0_TOCC (continued)

0	ETOC	Enable Timeout Counter 0= Timeout Counter disabled 1= Timeout Counter enabled Default Value: 0

10.1.11 CANFD0_CH0_TOCV

Timeout Counter Value

Address: 0x4040002C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	TOC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	TOC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	TOC	Timeout Counter The Timeout Counter is decremented in multiples of CAN bit times [1...16] depending on the configuration of TSCC.TCP. When decremented to zero, interrupt flag IR.TOO is set and the Timeout Counter is stopped. Start and reset/restart conditions are configured via TOCC.TOS. Default Value: 65535

10.1.12 CANFD0_CH0_ECR

Error Counter Register

Address: 0x40400040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	TEC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R	R						
HW Access	RW	RW						
Name	RP	REC [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW1C							
Name	CEL [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	CEL	CAN Error Logging The counter is incremented each time when a CAN protocol error causes the Transmit Error Counter or the Receive Error Counter to be incremented. It is reset by read access to CEL. The counter stops at 0xFF; the next increment of TEC or REC sets interrupt flag IR.ELO. Default Value: 0
15	RP	Receive Error Passive 0= The Receive Error Counter is below the error passive level of 128 1= The Receive Error Counter has reached the error passive level of 128 Default Value: 0
14 : 8	REC	Receive Error Counter Actual state of the Receive Error Counter, values between 0 and 127 Default Value: 0
7 : 0	TEC	Transmit Error Counter Actual state of the Transmit Error Counter, values between 0 and 255 Default Value: 0

10.1.13 CANFD0_CH0_PSR

Protocol Status Register

Address: 0x40400044

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R		R		
HW Access	RW	RW	RW	RW		RW1S		
Name	BO	EW	EP	ACT [4:3]		LEC [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None	R	R	R	R	R		
HW Access	None	RW1C	RW1C	RW1C	RW1C	RW1S		
Name	None	PXE	RFDF	RBRS	RESI	DLEC [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	None	R						
HW Access	None	RW						
Name	None	TDCV [22:16]						

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
22 : 16	TDCV	Transmitter Delay Compensation Value 0x00-0x7F Position of the secondary sample point, defined by the sum of the measured delay from m_can_tx to m_can_rx and TDCR.TDCO. The SSP position is, in the data phase, the number of mtq between the start of the transmitted bit and the secondary sample point. Valid values are 0 to 127 mtq. Default Value: 0
14	PXE	Protocol Exception Event , Reset on Read 0= No protocol exception event occurred since last read access 1= Protocol exception event occurred Default Value: 0
13	RFDF	Received a CAN FD Message , Reset on Read This bit is set independent of acceptance filtering. 0= Since this bit was reset by the CPU, no CAN FD message has been received 1= Message in CAN FD format with FDF flag set has been received Default Value: 0

10.1.13 CANFD0_CH0_PSR (continued)

12	RBRS	BRS flag of last received CAN FD Message , Reset on Read This bit is set together with RFDF, independent of acceptance filtering. 0= Last received CAN FD message did not have its BRS flag set 1= Last received CAN FD message had its BRS flag set Default Value: 0
11	RESI	ESI flag of last received CAN FD Message , Reset on Read This bit is set together with RFDF, independent of acceptance filtering. 0= Last received CAN FD message did not have its ESI flag set 1= Last received CAN FD message had its ESI flag set Default Value: 0
10 : 8	DLEC	Data Phase Last Error Code , Set on Read Type of last error that occurred in the data phase of a CAN FD format frame with its BRS flag set. Coding is the same as for LEC. This field will be cleared to zero when a CAN FD format frame with its BRS flag set has been transferred (reception or transmission) without error. Default Value: 7
7	BO	Bus_Off Status 0= The M_CAN is not Bus_Off 1= The M_CAN is in Bus_Off state Default Value: 0
6	EW	Warning Status 0= Both error counters are below the Error_Warning limit of 96 1= At least one of error counter has reached the Error_Warning limit of 96 Default Value: 0
5	EP	Error Passive 0= The M_CAN is in the Error_Active state. It normally takes part in bus communication and sends an active error flag when an error has been detected 1= The M_CAN is in the Error_Passive state Default Value: 0
4 : 3	ACT	Activity Monitors the module's CAN communication state. 00= Synchronizing - node is synchronizing on CAN communication 01= Idle - node is neither receiver nor transmitter 10= Receiver - node is operating as receiver 11= Transmitter - node is operating as transmitter Default Value: 0

10.1.13 CANFD0_CH0_PSR (continued)

2 : 0	LEC	Last Error Code, Set on Read0 The LEC indicates the type of the last error to occur on the CAN bus. This field will be cleared to '0' when a message has been transferred (reception or transmission) without error. 0= No Error: No error occurred since LEC has been reset by successful reception or transmission. 1= Stuff Error: More than 5 equal bits in a sequence have occurred in a part of a received message where this is not allowed. 2= Form Error: A fixed format part of a received frame has the wrong format. 3= AckError: The message transmitted by the M_TTCAN was not acknowledged by another node. 4= Bit1Error: During the transmission of a message (with the exception of the arbitration field), the device wanted to send a recessive level (bit of logical value '1'), but the monitored bus value was dominant. 5= Bit0Error: During the transmission of a message (or acknowledge bit, or active error flag, or overload flag), the device wanted to send a dominant level (data or identifier bit logical value 0'), but the monitored bus value was recessive. During Bus_Off recovery this status is set each time a sequence of 11 recessive bits has been monitored. This enables the CPU to monitor the proceeding of the Bus_Off recovery sequence (indicating the bus is not stuck at dominant or continuously disturbed). 6= CRCError: The CRC check sum of a received message was incorrect. The CRC of an incoming message does not match with the CRC calculated from the received data. 7= NoChange: Any read access to the Protocol Status Register re-initializes the LEC to '7'. When the LEC shows the value '7', no CAN bus event was detected since the last CPU read access to the Protocol Status Register. Default Value: 7

10.1.14 CANFD0_CH0_TDCR

Transmitter Delay Compensation Register

Address: 0x40400048

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW						
HW Access	None	R						
Name	None	TDCF [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW						
HW Access	None	R						
Name	None	TDCO [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
14 : 8	TDCO	Transmitter Delay Compensation Offset 0x00-0x7F Offset value defining the distance between the measured delay from m_ttcan_tx to m_ttcan_rx and the secondary sample point. Valid values are 0 to 127 mtq. Default Value: 0
6 : 0	TDCF	Transmitter Delay Compensation Filter Window Length 0x00-0x7F Defines the minimum value for the SSP position, dominant edges on m_ttcan_rx that would result in an earlier SSP position are ignored for transmitter delay measurement. The feature is enabled when TDCF is configured to a value greater than TDCO. Valid values are 0 to 127 mtq Default Value: 0

10.1.15 CANFD0_CH0_IR

Interrupt Register

Address: 0x40400050

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	RF1L_	RF1F	RF1W	RF1N	RF0L_	RF0F	RF0W	RF0N

Bits	15	14	13	12	11	10	9	8
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	TEFL_	TEFF	TEFW	TEFN	TFE	TCF	TC	HPM

Bits	23	22	21	20	19	18	17	16
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	EP_	ELO	BEU	BEC	DRX	TOO	MRAF	TSW

Bits	31	30	29	28	27	26	25	24
SW Access	None		RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	None		RW	RW	RW	RW	RW	RW
Name	None [31:30]		ARA	PED	PEA	WDI	BO_	EW_

Bits	Name	Description
29	ARA	Access to Reserved Address 0= No access to reserved address occurred 1= Access to reserved address occurred Default Value: 0
28	PED	Protocol Error in Data Phase (Data Bit Time is used) 0= No protocol error in data phase 1= Protocol error in data phase detected (PSR.DLEC != 0,7) Default Value: 0
27	PEA	Protocol Error in Arbitration Phase (Nominal Bit Time is used) 0= No protocol error in arbitration phase 1= Protocol error in arbitration phase detected (PSR.LEC != 0,7) Default Value: 0
26	WDI	Watchdog Interrupt 0= No Message RAM Watchdog event occurred 1= Message RAM Watchdog event due to missing READY Default Value: 0

10.1.15 CANFD0_CH0_IR (continued)

25	BO_	Bus_Off Status 0= Bus_Off status unchanged 1= Bus_Off status changed Default Value: 0
24	EW_	Warning Status 0= Error_Warning status unchanged 1= Error_Warning status changed Default Value: 0
23	EP_	Error Passive 0= Error_Passive status unchanged 1= Error_Passive status changed Default Value: 0
22	ELO	Error Logging Overflow 0= CAN Error Logging Counter did not overflow 1= Overflow of CAN Error Logging Counter occurred Default Value: 0
21	BEU	Bit Error Uncorrected. Message RAM bit error detected, uncorrected. The flag is set in the following case. - M_TTCAN reads from an out of range Message RAM address. Message RAM bit error sets CCCR.INIT to '1'. This is done to avoid transmission of corrupted data. 0= No bit error detected when reading from Message RAM 1= Bit error detected, uncorrected Default Value: 0
20	BEC	Reserved. This bit always reads as 0. Default Value: 0
19	DRX	Message stored to Dedicated Rx Buffer The flag is set whenever a received message has been stored into a dedicated Rx Buffer. 0= No Rx Buffer updated 1= At least one received message stored into a Rx Buffer Default Value: 0
18	TOO	Timeout Occurred 0= No timeout 1= Timeout reached Default Value: 0
17	MRAF	Message RAM Access Failure The flag is set, when the Rx Handler - has not completed acceptance filtering or storage of an accepted message until the arbitration field of the following message has been received. In this case acceptance filtering or message storage is aborted and the Rx Handler starts processing of the following message. - was not able to write a message to the Message RAM. In this case message storage is aborted. In both cases the FIFO put index is not updated resp. the New Data flag for a dedicated Rx Buffer is not set, a partly stored message is overwritten when the next message is stored to this location. The flag is also set when the Tx Handler was not able to read a message from the Message RAM in time. In this case message transmission is aborted. In case of a Tx Handler access failure the M_TTCAN is switched into Restricted Operation Mode (see Section 3.1.5). To leave Restricted Operation Mode, the Host CPU has to reset CCCR.ASM. 0= No Message RAM access failure occurred 1= Message RAM access failure occurred Default Value: 0

10.1.15 CANFD0_CH0_IR (continued)

16	TSW	Timestamp Wraparound 0= No timestamp counter wrap-around 1= Timestamp counter wrapped around Default Value: 0
15	TEFL_	Tx Event FIFO Element Lost 0= No Tx Event FIFO element lost 1= Tx Event FIFO element lost, also set after write attempt to Tx Event FIFO of size zero Default Value: 0
14	TEFF	Tx Event FIFO Full 0= Tx Event FIFO not full 1= Tx Event FIFO full Default Value: 0
13	TEFW	Tx Event FIFO Watermark Reached 0= Tx Event FIFO fill level below watermark 1= Tx Event FIFO fill level reached watermark Default Value: 0
12	TEFN	Tx Event FIFO New Entry 0= Tx Event FIFO unchanged 1= Tx Handler wrote Tx Event FIFO element Default Value: 0
11	TFE	Tx FIFO Empty 0= Tx FIFO non-empty 1= Tx FIFO empty Default Value: 0
10	TCF	Transmission Cancellation Finished 0= No transmission cancellation finished 1= Transmission cancellation finished Default Value: 0
9	TC	Transmission Completed 0= No transmission completed 1= Transmission completed Default Value: 0
8	HPM	High Priority Message 0= No high priority message received 1= High priority message received Default Value: 0
7	RF1L_	Rx FIFO 1 Message Lost 0= No Rx FIFO 1 message lost 1= Rx FIFO 1 message lost, also set after write attempt to Rx FIFO 1 of size zero Default Value: 0
6	RF1F	Rx FIFO 1 Full 0= Rx FIFO 1 not full 1= Rx FIFO 1 full Default Value: 0
5	RF1W	Rx FIFO 1 Watermark Reached 0= Rx FIFO 1 fill level below watermark 1= Rx FIFO 1 fill level reached watermark Default Value: 0

10.1.15 CANFD0_CH0_IR (continued)

4	RF1N	Rx FIFO 1 New Message 0= No new message written to Rx FIFO 1 1= New message written to Rx FIFO 1 Default Value: 0
3	RF0L_	Rx FIFO 0 Message Lost 0= No Rx FIFO 0 message lost 1= Rx FIFO 0 message lost, also set after write attempt to Rx FIFO 0 of size zero Default Value: 0
2	RF0F	Rx FIFO 0 Full 0= Rx FIFO 0 not full 1= Rx FIFO 0 full Default Value: 0
1	RF0W	Rx FIFO 0 Watermark Reached 0= Rx FIFO 0 fill level below watermark 1= Rx FIFO 0 fill level reached watermark Default Value: 0
0	RF0N	Rx FIFO 0 New Message 0= No new message written to Rx FIFO 0 1= New message written to Rx FIFO 0 Default Value: 0

10.1.16 CANFD0_CH0_IE

Interrupt Enable

Address: 0x40400054

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	RF1LE	RF1FE	RF1WE	RF1NE	RF0LE	RF0FE	RF0WE	RF0NE

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	TEFLE	TEFFE	TEFWE	TEFNE	TFEE	TCFE	TCE	HPME

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	EPE	ELOE	BEUE	BECE	DRXE	TOOE	MRAFE	TSWE

Bits	31	30	29	28	27	26	25	24
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		R	R	R	R	R	R
Name	None [31:30]		ARAE	PEDE	PEAE	WDIE	BOE	EWE

Bits	Name	Description
29	ARAE	Access to Reserved Address Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
28	PEDE	Protocol Error in Data Phase Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
27	PEAE	Protocol Error in Arbitration Phase Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
26	WDIE	Watchdog Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0

10.1.16 CANFD0_CH0_IE (continued)

25	BOE	Bus_Off Status Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
24	EWE	Warning Status Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
23	EPE	Error Passive Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
22	ELOE	Error Logging Overflow Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
21	BEUE	Bit Error Uncorrected Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
20	BECE	Bit Error Corrected Interrupt Enable (not used in M_TTCAN) 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
19	DRXE	Message stored to Dedicated Rx Buffer Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
18	TOOE	Timeout Occurred Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
17	MRAFE	Message RAM Access Failure Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
16	TSWE	Timestamp Wraparound Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
15	TEFLE	Tx Event FIFO Event Lost Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
14	TEFFE	Tx Event FIFO Full Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0

10.1.16 CANFD0_CH0_IE (continued)

13	TEFWE	Tx Event FIFO Watermark Reached Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
12	TEFNE	Tx Event FIDO New Entry Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
11	TFEE	Tx FIFO Empty Interrupt Enable 0= Interrupt Disabled 1= Interrupt EnabledTx FIFO Empty Interrupt Enable Default Value: 0
10	TCFE	Transmission Cancellation Finished Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
9	TCE	Transmission Completed Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
8	HPME	High Priority Message Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
7	RF1LE	Rx FIFO 1 Message Lost Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
6	RF1FE	Rx FIFO 1 Full Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
5	RF1WE	Rx FIFO 1 Watermark Reached Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
4	RF1NE	Rx FIFO 1 New Message Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
3	RF0LE	Rx FIFO 0 Message Lost Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
2	RF0FE	Rx FIFO 0 Full Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0

10.1.16 CANFD0_CH0_IE (continued)

1	RF0WE	Rx FIFO 0 Watermark Reached Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
0	RF0NE	Rx FIFO 0 New Message Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0

10.1.17 CANFD0_CH0_ILS

Interrupt Line Select

Address: 0x40400058

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	RF1LL	RF1FL	RF1WL	RF1NL	RF0LL	RF0FL	RF0WL	RF0NL

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	TEFLL	TEFFL	TEFWL	TEFNL	TFEL	TCFL	TCL	HPML

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	EPL	ELOL	BEUL	BECL	DRXL	TOOL	MRAFL	TSWL

Bits	31	30	29	28	27	26	25	24
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		R	R	R	R	R	R
Name	None [31:30]		ARAL	PEDL	PEAL	WDIL	BOL	EWL

Bits	Name	Description
29	ARAL	Access to Reserved Address Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
28	PEDL	Protocol Error in Data Phase Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
27	PEAL	Protocol Error in Arbitration Phase Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
26	WDIL	Watchdog Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0

10.1.17 CANFD0_CH0_ILS (continued)

25	BOL	Bus_Off Status Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
24	EWL	Warning Status Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
23	EPL	Error Passive Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
22	ELOL	Error Logging Overflow Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
21	BEUL	Bit Error Uncorrected Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
20	BECL	Bit Error Corrected Interrupt Select (not used in M_TTCAN) 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
19	DRXL	Message stored to Dedicated Rx Buffer Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
18	TOOL	Timeout Occurred Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
17	MRAFL	Message RAM Access Failure Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
16	TSWL	Timestamp Wraparound Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
15	TEFLL	Tx Event FIFO Event Lost Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
14	TEFFL	Tx Event FIFO Full Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0

10.1.17 CANFD0_CH0_ILS (continued)

13	TEFWL	Tx Event FIFO Watermark Reached Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
12	TEFNL	Tx Event FIFO New Entry Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
11	TFEL	Tx FIFO Empty Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
10	TCFL	Transmission Cancellation Finished Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
9	TCL	Transmission Completed Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
8	HPML	High Priority Message Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
7	RF1LL	Rx FIFO 1 Message Lost Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
6	RF1FL	Rx FIFO 1 Full Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
5	RF1WL	Rx FIFO 1 Watermark Reached Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
4	RF1NL	Rx FIFO 1 New Message Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
3	RF0LL	Rx FIFO 0 Message Lost Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
2	RF0FL	Rx FIFO 0 Full Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0

10.1.17 CANFD0_CH0_ILS (continued)

1	RF0WL	Rx FIFO 0 Watermark Reached Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
0	RF0NL	Rx FIFO 0 New Message Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0

10.1.18 CANFD0_CH0_ILE

Interrupt Line Enable

Address: 0x4040005C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						EINT1	EINT0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	EINT1	Enable Interrupt Line 1 0= Interrupt line m_ttcan_int1 disabled 1= Interrupt line m_ttcan_int1 enabled Default Value: 0
0	EINT0	Enable Interrupt Line 0 0= Interrupt line m_ttcan_int0 disabled 1= Interrupt line m_ttcan_int0 enabled Default Value: 0

10.1.19 CANFD0_CH0_GFC

Global Filter Configuration

Address: 0x40400080

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW		RW		RW	RW
HW Access	None		R		R		R	R
Name	None [7:6]		ANFS [5:4]		ANFE [3:2]		RRFS	RRFE

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 4	ANFS	Accept Non-matching Frames Standard Defines how received messages with 11-bit IDs that do not match any element of the filter list are treated. 00= Accept in Rx FIFO 0 01= Accept in Rx FIFO 1 10= Reject 11= Reject Default Value: 0
3 : 2	ANFE	Accept Non-matching Frames Extended Defines how received messages with 29-bit IDs that do not match any element of the filter list are treated. 00= Accept in Rx FIFO 0 01= Accept in Rx FIFO 1 10= Reject 11= Reject Default Value: 0

10.1.19 CANFD0_CH0_GFC (continued)

1	RRFS	Reject Remote Frames Standard 0= Filter remote frames with 11-bit standard IDs 1= Reject all remote frames with 11-bit standard IDs Default Value: 0
0	RRFE	Reject Remote Frames Extended 0= Filter remote frames with 29-bit extended IDs 1= Reject all remote frames with 29-bit extended IDs Default Value: 0

10.1.20 CANFD0_CH0_SIDFC

Standard ID Filter Configuration

Address: 0x40400084

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW						None	
HW Access	R						None	
Name	FLSSA [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	FLSSA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	LSS [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	LSS	List Size Standard 0= No standard Message ID filter 1-128= Number of standard Message ID filter elements 128= Values greater than 128 are interpreted as 128 Default Value: 0
15 : 2	FLSSA	Filter List Standard Start Address Start address of standard Message ID filter list (32-bit word address, see Figure 2). Default Value: 0

10.1.21 CANFD0_CH0_XIDFC

Extended ID Filter Configuration

Address: 0x40400088

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW						None	
HW Access	R						None	
Name	FLESA [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	FLESA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None	RW						
HW Access	None	R						
Name	None	LSE [22:16]						

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
22 : 16	LSE	List Size Extended 0= No extended Message ID filter 1-64= Number of extended Message ID filter elements 64= Values greater than 64 are interpreted as 64 Default Value: 0
15 : 2	FLESA	Filter List Extended Start Address Start address of extended Message ID filter list (32-bit word address, see Figure 2). Default Value: 0

10.1.22 CANFD0_CH0_XIDAM

Extended ID AND Mask

Address: 0x40400090

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	EIDM [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	EIDM [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	EIDM [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None			RW				
HW Access	None			R				
Name	None [31:29]			EIDM [28:24]				

Bits	Name	Description
28 : 0	EIDM	Extended ID Mask For acceptance filtering of extended frames the Extended ID AND Mask is ANDed with the Message ID of a received frame. Intended for masking of 29-bit IDs in SAE J1939. With the reset value of all bits set to one the mask is not active. Default Value: 536870911

10.1.23 CANFD0_CH0_HPMS

High Priority Message Status

Address: 0x40400094

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R		R					
HW Access	RW		RW					
Name	MSI [7:6]		BIDX [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	R	R						
HW Access	RW	RW						
Name	FLST	FIDX [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15	FLST	Filter List Indicates the filter list of the matching filter element. 0= Standard Filter List 1= Extended Filter List Default Value: 0
14 : 8	FIDX	Filter Index Index of matching filter element. Range is 0 to SIDFC.LSS - 1 resp. XIDFC.LSE - 1. Default Value: 0
7 : 6	MSI	Message Storage Indicator 00= No FIFO selected 01= FIFO message lost 10= Message stored in FIFO 0 11= Message stored in FIFO 1 Default Value: 0
5 : 0	BIDX	Buffer Index Index of Rx FIFO element to which the message was stored. Only valid when MSI[1] = '1'. Default Value: 0

10.1.24 CANFD0_CH0_NDAT1

New Data 1

Address: 0x40400098

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C							
HW Access	RW							
Name	ND [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1C							
HW Access	RW							
Name	ND [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW1C							
HW Access	RW							
Name	ND [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1C							
HW Access	RW							
Name	ND [31:24]							

Bits	Name	Description
31 : 0	ND	New Data The register holds the New Data flags of Rx Buffers 0 to 31. The flags are set when the respective Rx Buffer has been updated from a received frame. The flags remain set until the Host clears them. A flag is cleared by writing a '1' to the corresponding bit position. Writing a '0' has no effect. A hard reset will clear the register. 0= Rx Buffer not updated 1= Rx Buffer updated from new message Default Value: 0

10.1.25 CANFD0_CH0_NDAT2

New Data 2

Address: 0x4040009C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C							
HW Access	RW							
Name	ND [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1C							
HW Access	RW							
Name	ND [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW1C							
HW Access	RW							
Name	ND [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1C							
HW Access	RW							
Name	ND [31:24]							

Bits	Name	Description
31 : 0	ND	New Data The register holds the New Data flags of Rx Buffers 32 to 63. The flags are set when the respective Rx Buffer has been updated from a received frame. The flags remain set until the Host clears them. A flag is cleared by writing a '1' to the corresponding bit position. Writing a '0' has no effect. A hard reset will clear the register. 0= Rx Buffer not updated 1= Rx Buffer updated from new message Default Value: 0

10.1.26 CANFD0_CH0_RXF0C

Rx FIFO 0 Configuration

Address: 0x404000A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW						None	
HW Access	R						None	
Name	F0SA [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	F0SA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None	RW						
HW Access	None	R						
Name	None	F0S [22:16]						

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW						
HW Access	R	R						
Name	F0OM	F0WM [30:24]						

Bits	Name	Description
31	F0OM	FIFO 0 Operation Mode FIFO 0 can be operated in blocking or in overwrite mode (see Section 3.4.2). 0= FIFO 0 blocking mode 1= FIFO 0 overwrite mode Default Value: 0
30 : 24	F0WM	Rx FIFO 0 Watermark 0= Watermark interrupt disabled 1-64= Level for Rx FIFO 0 watermark interrupt (IR.RF0W) 64= Watermark interrupt disabled Default Value: 0
22 : 16	F0S	Rx FIFO 0 Size 0= No Rx FIFO 0 1-64= Number of Rx FIFO 0 elements 64= Values greater than 64 are interpreted as 64 The Rx FIFO 0 elements are indexed from 0 to F0S-1 Default Value: 0
15 : 2	F0SA	Rx FIFO 0 Start Address Start address of Rx FIFO 0 in Message RAM (32-bit word address, see Figure 2). Default Value: 0

10.1.27 CANFD0_CH0_RXF0S

Rx FIFO 0 Status

Address: 0x404000A4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	R						
HW Access	None	RW						
Name	None	F0FL [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None		R					
HW Access	None		RW					
Name	None [15:14]		F0GI [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	None		R					
HW Access	None		RW					
Name	None [23:22]		F0PI [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	None						R	R
HW Access	None						RW	RW
Name	None [31:26]						RF0L	F0F

Bits	Name	Description
25	RF0L	Rx FIFO 0 Message Lost This bit is a copy of interrupt flag IR.RF0L. When IR.RF0L is reset, this bit is also reset. 0= No Rx FIFO 0 message lost 1= Rx FIFO 0 message lost, also set after write attempt to Rx FIFO 0 of size zero Default Value: 0
24	F0F	Rx FIFO 0 Full 0= Rx FIFO 0 not full 1= Rx FIFO 0 full Default Value: 0
21 : 16	F0PI	Rx FIFO 0 Put Index Rx FIFO 0 write index pointer, range 0 to 63. Default Value: 0
13 : 8	F0GI	Rx FIFO 0 Get Index Rx FIFO 0 read index pointer, range 0 to 63. This field is updated by the software writing to RxF0A.F0AI Default Value: 0

10.1.27 CANFD0_CH0_RXF0S (continued)

6 : 0	F0FL	Rx FIFO 0 Fill Level Number of elements stored in Rx FIFO 0, range 0 to 64. Default Value: 0

10.1.28 CANFD0_CH0_RXF0A

Rx FIFO 0 Acknowledge

Address: 0x404000A8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		A					
Name	None [7:6]		F0AI [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	F0AI	Rx FIFO 0 Acknowledge Index After the Host has read a message or a sequence of messages from Rx FIFO 0 it has to write the buffer index of the last element read from Rx FIFO 0 to F0AI. This will set the Rx FIFO 0 Get Index RXF0S.F0GI to F0AI + 1 and update the FIFO 0 Fill Level RXF0S.F0FL. Default Value: 0

10.1.29 CANFD0_CH0_RXBC

Rx Buffer Configuration

Address: 0x404000AC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW						None	
HW Access	R						None	
Name	RBSA [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	RBSA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 2	RBSA	Rx Buffer Start Address Configures the start address of the Rx Buffers section in the Message RAM (32-bit word address). Also used to reference debug messages A,B,C. Default Value: 0

10.1.30 CANFD0_CH0_RXF1C

Rx FIFO 1 Configuration

Address: 0x404000B0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW						None	
HW Access	R						None	
Name	F1SA [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	F1SA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None	RW						
HW Access	None	R						
Name	None	F1S [22:16]						

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW						
HW Access	R	R						
Name	F1OM	F1WM [30:24]						

Bits	Name	Description
31	F1OM	FIFO 1 Operation Mode FIFO 1 can be operated in blocking or in overwrite mode (see Section 3.4.2). 0= FIFO 1 blocking mode 1= FIFO 1 overwrite mode Default Value: 0
30 : 24	F1WM	Rx FIFO 1 Watermark 0= Watermark interrupt disabled 1-64= Level for Rx FIFO 1 watermark interrupt (IR.RF1W) 64= Watermark interrupt disabled Default Value: 0
22 : 16	F1S	Rx FIFO 1 Size 0= No Rx FIFO 1 1-64= Number of Rx FIFO 1 elements 64= Values greater than 64 are interpreted as 64 The Rx FIFO 1 elements are indexed from 0 to F1S - 1 Default Value: 0
15 : 2	F1SA	Rx FIFO 1 Start Address Start address of Rx FIFO 1 in Message RAM (32-bit word address, see Figure 2). Default Value: 0

10.1.31 CANFD0_CH0_RXF1S

Rx FIFO 1 Status

Address: 0x404000B4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	R						
HW Access	None	RW						
Name	None	F1FL [6:0]						

Bits	15	14	13	12	11	10	9	8
SW Access	None		R					
HW Access	None		RW					
Name	None [15:14]		F1GI [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	None		R					
HW Access	None		RW					
Name	None [23:22]		F1PI [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	R		None				R	R
HW Access	RW		None				RW	RW
Name	DMS [31:30]		None [29:26]				RF1L	F1F

Bits	Name	Description
31 : 30	DMS	Debug Message Status 00= Idle state, wait for reception of debug messages, DMA request is cleared 01= Debug message A received 10= Debug messages A, B received 11= Debug messages A, B, C received, DMA request is set Default Value: 0
25	RF1L	Rx FIFO 1 Message Lost This bit is a copy of interrupt flag IR.RF1L. When IR.RF1L is reset, this bit is also reset. 0= No Rx FIFO 1 message lost 1= Rx FIFO 1 message lost, also set after write attempt to Rx FIFO 1 of size zero Default Value: 0
24	F1F	Rx FIFO 1 Full 0= Rx FIFO 1 not full 1= Rx FIFO 1 full Default Value: 0
21 : 16	F1PI	Rx FIFO 1 Put Index Rx FIFO 1 write index pointer, range 0 to 63. Default Value: 0

10.1.31 CANFD0_CH0_RXF1S (continued)

13 : 8	F1GI	Rx FIFO 1 Get Index Rx FIFO 1 read index pointer, range 0 to 63. This field is updated by the software writing to RxF1A.FAI Default Value: 0
6 : 0	F1FL	Rx FIFO 1 Fill Level Number of elements stored in Rx FIFO 1, range 0 to 64. Default Value: 0

10.1.32 CANFD0_CH0_RXF1A

Rx FIFO 1 Acknowledge

Address: 0x404000B8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		A					
Name	None [7:6]		F1AI [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	F1AI	Rx FIFO 1 Acknowledge Index After the Host has read a message or a sequence of messages from Rx FIFO 1 it has to write the buffer index of the last element read from Rx FIFO 1 to F1AI. This will set the Rx FIFO 1 Get Index RXF1S.F1GI to F1AI + 1 and update the FIFO 1 Fill Level RXF1S.F1FL. Default Value: 0

10.1.33 CANFD0_CH0_RXESC

Rx Buffer / FIFO Element Size Configuration

Address: 0x404000BC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	F1DS [6:4]			None	F0DS [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW		
HW Access	None					R		
Name	None [15:11]					RBDS [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10 : 8	RBDS	Rx Buffer Data Field Size 000= 8 byte data field 001= 12 byte data field 010= 16 byte data field 011= 20 byte data field 100= 24 byte data field 101= 32 byte data field 110= 48 byte data field 111= 64 byte data field Default Value: 0
6 : 4	F1DS	Rx FIFO 1 Data Field Size 000= 8 byte data field 001= 12 byte data field 010= 16 byte data field 011= 20 byte data field 100= 24 byte data field 101= 32 byte data field 110= 48 byte data field 111= 64 byte data field Default Value: 0

10.1.33 CANFD0_CH0_RXESC (continued)

2 : 0	F0DS	Rx FIFO 0 Data Field Size 000= 8 byte data field 001= 12 byte data field 010= 16 byte data field 011= 20 byte data field 100= 24 byte data field 101= 32 byte data field 110= 48 byte data field 111= 64 byte data field Default Value: 0

10.1.34 CANFD0_CH0_TXBC

Tx Buffer Configuration

Address: 0x404000C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW						None	
HW Access	R						None	
Name	TBSA [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	TBSA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW					
HW Access	None		R					
Name	None [23:22]		NDTB [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	None	RW	RW					
HW Access	None	R	R					
Name	None	TFQM	TFQS [29:24]					

Bits	Name	Description
30	TFQM	Tx FIFO/Queue Mode 0= Tx FIFO operation 1= Tx Queue operation Default Value: 0
29 : 24	TFQS	Transmit FIFO/Queue Size 0= No Tx FIFO/Queue 1-32= Number of Tx Buffers used for Tx FIFO/Queue 32= Values greater than 32 are interpreted as 32 Default Value: 0
21 : 16	NDTB	Number of Dedicated Transmit Buffers 0= No Dedicated Tx Buffers 1-32= Number of Dedicated Tx Buffers 32= Values greater than 32 are interpreted as 32 Default Value: 0
15 : 2	TBSA	Tx Buffers Start Address Start address of Tx Buffers section in Message RAM (32-bit word address, see Figure 2). Default Value: 0

10.1.35 CANFD0_CH0_TXFQS

Tx FIFO/Queue Status

Address: 0x404000C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R					
HW Access	None		RW					
Name	None [7:6]		TFFL [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None			R				
HW Access	None			RW				
Name	None [15:13]			TFGI [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	None		R	R				
HW Access	None		RW	RW				
Name	None [23:22]		TFQF	TFQPI [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
21	TFQF	Tx FIFO/Queue Full 0= Tx FIFO/Queue not full 1= Tx FIFO/Queue full Default Value: 0
20 : 16	TFQPI	Tx FIFO/Queue Put Index Tx FIFO/Queue write index pointer, range 0 to 31. Default Value: 0
12 : 8	TFGI	Tx FIFO Get Index Tx FIFO read index pointer, range 0 to 31. Read as zero when Tx Queue operation is configured TXBC.TFQM = '1'). Default Value: 0
5 : 0	TFFL	Tx FIFO Free Level Number of consecutive free Tx FIFO elements starting from TFGI, range 0 to 32. Read as zero when Tx Queue operation is configured (TXBC.TFQM = '1') Default Value: 0

10.1.36 CANFD0_CH0_TXESC

Tx Buffer Element Size Configuration

Address: 0x404000C8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW		
HW Access	None					R		
Name	None [7:3]					TBDS [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2 : 0	TBDS	Tx Buffer Data Field Size 000= 8 byte data field 001= 12 byte data field 010= 16 byte data field 011= 20 byte data field 100= 24 byte data field 101= 32 byte data field 110= 48 byte data field 111= 64 byte data field Default Value: 0

10.1.37 CANFD0_CH0_TXBRP

Tx Buffer Request Pending

Address: 0x404000CC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	TRP [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	TRP [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	TRP [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	TRP [31:24]							

Bits	Name	Description

10.1.37 CANFD0_CH0_TXBRP (continued)

31 : 0	TRP	Transmission Request Pending Each Tx Buffer has its own Transmission Request Pending bit. The bits are set via register TX-BAR. The bits are reset after a requested transmission has completed or has been cancelled via register TXBCR. TXBRP bits are set only for those Tx Buffers configured via TXBC. After a TXBRP bit has been set, a Tx scan (see Section 3.5, Tx Handling) is started to check for the pending Tx request with the highest priority (Tx Buffer with lowest Message ID). A cancellation request resets the corresponding transmission request pending bit of register TXBRP. In case a transmission has already been started when a cancellation is requested, this is done at the end of the transmission, regardless whether the transmission was successful or not. The cancellation request bits are reset directly after the corresponding TXBRP bit has been reset. After a cancellation has been requested, a finished cancellation is signaled via TXBCF after successful transmission together with the corresponding TXBTO bit when the transmission has not yet been started at the point of cancellation when the transmission has been aborted due to lost arbitration when an error occurred during frame transmission In DAR mode all transmissions are automatically cancelled if they are not successful. The corresponding TXBCF bit is set for all unsuccessful transmissions. 0= No transmission request pending 1= Transmission request pending Default Value: 0

10.1.38 CANFD0_CH0_TXBAR

Tx Buffer Add Request

Address: 0x404000D0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	AR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	AR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	AR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	AR [31:24]							

Bits	Name	Description
31 : 0	AR	Add Request Each Tx Buffer has its own Add Request bit. Writing a '1' will set the corresponding Add Request bit; writing a '0' has no impact. This enables the Host to set transmission requests for multiple Tx Buffers with one write to TXBAR. TXBAR bits are set only for those Tx Buffers configured via TXBC. When no Tx scan is running, the bits are reset immediately, else the bits remain set until the Tx scan process has completed. 0= No transmission request added 1= Transmission requested added Default Value: 0

10.1.39 CANFD0_CH0_TXBCR

Tx Buffer Cancellation Request

Address: 0x404000D4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	CR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	CR [31:24]							

Bits	Name	Description
31 : 0	CR	Cancellation Request Each Tx Buffer has its own Cancellation Request bit. Writing a '1' will set the corresponding Cancellation Request bit; writing a '0' has no impact. This enables the Host to set cancellation requests for multiple Tx Buffers with one write to TXBCR. TXBCR bits are set only for those Tx Buffers configured via TXBC. The bits remain set until the corresponding bit of TXBRP is reset. 0= No cancellation pending 1= Cancellation pending Default Value: 0

10.1.40 CANFD0_CH0_TXBTO

Tx Buffer Transmission Occurred

Address: 0x404000D8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	TO [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	TO [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	TO [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	TO [31:24]							

Bits	Name	Description
31 : 0	TO	Transmission Occurred Each Tx Buffer has its own Transmission Occurred bit. The bits are set when the corresponding TXBRP bit is cleared after a successful transmission. The bits are reset when a new transmission is requested by writing a '1' to the corresponding bit of register TXBAR. 0= No transmission occurred 1= Transmission occurred Default Value: 0

10.1.41 CANFD0_CH0_TXBCF

Tx Buffer Cancellation Finished

Address: 0x404000DC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	CF [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	CF [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	CF [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	CF [31:24]							

Bits	Name	Description
31 : 0	CF	Cancellation Finished Each Tx Buffer has its own Cancellation Finished bit. The bits are set when the corresponding TXBRP bit is cleared after a cancellation was requested via TXBCR. In case the corresponding TXBRP bit was not set at the point of cancellation, CF is set immediately. The bits are reset when a new transmission is requested by writing a '1' to the corresponding bit of register TXBAR. 0= No transmit buffer cancellation 1= Transmit buffer cancellation finished Default Value: 0

10.1.42 CANFD0_CH0_TXBTIE

Tx Buffer Transmission Interrupt Enable

Address: 0x404000E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	TIE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	TIE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	TIE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	TIE [31:24]							

Bits	Name	Description
31 : 0	TIE	Transmission Interrupt Enable Each Tx Buffer has its own Transmission Interrupt Enable bit. 0= Transmission interrupt disabled 1= Transmission interrupt enable Default Value: 0

10.1.43 CANFD0_CH0_TXBCIE

Tx Buffer Cancellation Finished Interrupt Enable

Address: 0x404000E4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CFIE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CFIE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	CFIE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	CFIE [31:24]							

Bits	Name	Description
31 : 0	CFIE	Cancellation Finished Interrupt Enable Each Tx Buffer has its own Cancellation Finished Interrupt Enable bit. 0= Cancellation finished interrupt disabled 1= Cancellation finished interrupt enabled Default Value: 0

10.1.44 CANFD0_CH0_TXEFC

Tx Event FIFO Configuration

Address: 0x404000F0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW						None	
HW Access	R						None	
Name	EFSA [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	EFSA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW					
HW Access	None		R					
Name	None [23:22]		EFS [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	None		RW					
HW Access	None		R					
Name	None [31:30]		EFWM [29:24]					

Bits	Name	Description
29 : 24	EFWM	Event FIFO Watermark 0= Watermark interrupt disabled 1-32= Level for Tx Event FIFO watermark interrupt (IR.TEFW) 32= Watermark interrupt disabled Default Value: 0
21 : 16	EFS	Event FIFO Size 0= Tx Event FIFO disabled 1-32= Number of Tx Event FIFO elements 32= Values greater than 32 are interpreted as 32 The Tx Event FIFO elements are indexed from 0 to EFS-1 Default Value: 0
15 : 2	EFSA	Event FIFO Start Address Start address of Tx Event FIFO in Message RAM (32-bit word address, see Figure 2). Default Value: 0

10.1.45 CANFD0_CH0_TXEFS

Tx Event FIFO Status

Address: 0x404000F4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R					
HW Access	None		RW					
Name	None [7:6]		EFFL [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None			R				
HW Access	None			RW				
Name	None [15:13]			EFGI [12:8]				

Bits	23	22	21	20	19	18	17	16
SW Access	None			R				
HW Access	None			RW				
Name	None [23:21]			EFPI [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	None						R	R
HW Access	None						RW	RW
Name	None [31:26]						TEFL	EFF

Bits	Name	Description
25	TEFL	Tx Event FIFO Element Lost This bit is a copy of interrupt flag IR.TEFL. When IR.TEFL is reset, this bit is also reset. 0= No Tx Event FIFO element lost 1= Tx Event FIFO element lost, also set after write attempt to Tx Event FIFO of size zero. Default Value: 0
24	EFF	Event FIFO Full 0= Tx Event FIFO not full 1= Tx Event FIFO full Default Value: 0
20 : 16	EFPI	Event FIFO Put Index Tx Event FIFO write index pointer, range 0 to 31. Default Value: 0
12 : 8	EFGI	Event FIFO Get Index Tx Event FIFO read index pointer, range 0 to 31. Default Value: 0
5 : 0	EFFL	Event FIFO Fill Level Number of elements stored in Tx Event FIFO, range 0 to 32. Default Value: 0

10.1.46 CANFD0_CH0_TXEFA

Tx Event FIFO Acknowledge

Address: 0x404000F8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			R				
Name	None [7:5]			EFAI [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4 : 0	EFAI	Event FIFO Acknowledge Index After the Host has read an element or a sequence of elements from the Tx Event FIFO it has to write the index of the last element read from Tx Event FIFO to EFAI. This will set the Tx Event FIFO Get Index TXEFS.EFGI to EFAI + 1 and update the Event FIFO Fill Level TXEFS.EFFL. Default Value: 0

10.1.47 CANFD0_CH0_TTTMC

TT Trigger Memory Configuration

Address: 0x40400100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW						None	
HW Access	R						None	
Name	TMSA [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	TMSA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None	RW						
HW Access	None	R						
Name	None	TME [22:16]						

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
22 : 16	TME	Trigger Memory Elements 0= No Trigger Memory 1-64= Number of Trigger Memory elements 64= Values greater than 64 are interpreted as 64 Default Value: 0
15 : 2	TMSA	Trigger Memory Start Address Start address of Trigger Memory in Message RAM (32-bit word address, see Figure 2). Default Value: 0

10.1.48 CANFD0_CH0_TTRMC

TT Reference Message Configuration

Address: 0x40400104

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	RID [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	RID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	RID [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None	RW				
HW Access	R	R	None	R				
Name	RMPS	XTD	None	RID [28:24]				

Bits	Name	Description
31	RMPS	Reference Message Payload Select Ignored in case of time slaves. 0= Reference message has no additional payload 1= The following elements are taken from Tx Buffer 0: Message Marker MM, Event FIFO Control EFC, Data Length Code DLC, Data Bytes DB Level 1: bytes 2-8, Level 0,2: bytes 5-8) Default Value: 0
30	XTD	Extended Identifier 0= 11-bit standard identifier 1= 29-bit extended identifier Default Value: 0
28 : 0	RID	Reference Identifier Identifier transmitted with reference message and used for reference message filtering. Standard or extended reference identifier depending on bit XTD. A standard identifier has to be written to ID[28:18]. Default Value: 0

10.1.49 CANFD0_CH0_TTOCF

TT Operation Configuration

Address: 0x40400108

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW			RW	RW	None	RW	
HW Access	R			R	R	None	R	
Name	LDSDL [7:5]			TM	GEN	None	OM [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW						
HW Access	R	R						
Name	EECS	IRTO [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	AWL [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [31:27]					EVTP	ECC	EGTF

Bits	Name	Description
26	EVTP	Event Trigger Polarity 0= Rising edge trigger 1= Falling edge trigger Default Value: 0
25	ECC	Enable Clock Calibration 0= Automatic clock calibration in TTCAN Level 0,2 is disabled 1= Automatic clock calibration in TTCAN Level 0,2 is enabled Default Value: 0
24	EGTF	Enable Global Time Filtering 0= Global time filtering in TTCAN Level 0,2 is disabled 1= Global time filtering in TTCAN Level 0,2 is enabled Default Value: 0
23 : 16	AWL	Application Watchdog Limit The application watchdog can be disabled by programming AWL to 0x00. 0x00-FF Maximum time after which the application has to serve the application watchdog. The application watchdog is incremented once each 256 NTUs. Default Value: 1

10.1.49 CANFD0_CH0_TTOCF (continued)

15	EECS	Enable External Clock Synchronization If enabled, TUR configuration (TURCF.NCL only) may be updated during TTCAN operation. 0= External clock synchronization in TTCAN Level 0,2 disabled 1= External clock synchronization in TTCAN Level 0,2 enabled Default Value: 0
14 : 8	IRTO	Initial Reference Trigger Offset 0x00-7F Positive offset, range from 0 to 127 Default Value: 0
7 : 5	LDSDL	LD of Synchronization Deviation Limit The Synchronization Deviation Limit SDL is configured by its dual logarithm LDSDL with SDL = 2(LDSDL + 5). It should not exceed the clock tolerance given by the CAN bit timing configuration. 0x0-7 LD of Synchronization Deviation Limit (SDL <= 32...4096) Default Value: 0
4	TM	Time Master 0= Time Master function disabled 1= Potential Time Master Default Value: 0
3	GEN	Gap Enable 0= Strictly time-triggered operation 1= External event-synchronized time-triggered operation Default Value: 0
1 : 0	OM	Operation Mode 00= Event-driven CAN communication, default 01= TTCAN level 1 10= TTCAN level 2 11= TTCAN level 0 Default Value: 0

10.1.50 CANFD0_CH0_TTMLM

TT Matrix Limits

Address: 0x4040010C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW					
HW Access	R		R					
Name	CSS [7:6]		CCM [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				TXEW [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	ENTT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None				RW			
HW Access	None				R			
Name	None [31:28]				ENTT [27:24]			

Bits	Name	Description
27 : 16	ENTT	Expected Number of Tx Triggers 0x000-FFF Expected number of Tx Triggers in one Matrix Cycle Default Value: 0
11 : 8	TXEW	Tx Enable Window 0x0-F Length of Tx enable window, 1-16 NTU cycles Default Value: 0
7 : 6	CSS	Cycle Start Synchronization Enables sync pulse output at pin m_ttcan_soc. 00= No sync pulse 01= Sync pulse at start of basic cycle 10= Sync pulse at start of matrix cycle 11= Reserved Default Value: 0

10.1.50 CANFD0_CH0_TTMLM (continued)

5 : 0	CCM	Cycle Count Max 0x00 1 Basic Cycle per Matrix Cycle 0x01 2 Basic Cycles per Matrix Cycle 0x03 4 Basic Cycles per Matrix Cycle 0x07 8 Basic Cycles per Matrix Cycle 0x0F 16 Basic Cycles per Matrix Cycle 0x1F 32 Basic Cycles per Matrix Cycle 0x3F 64 Basic Cycles per Matrix Cycle others Reserved Default Value: 0

10.1.51 CANFD0_CH0_TURCF

TUR Configuration

Address: 0x40400110

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	NCL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	NCL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DC [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None	RW					
HW Access	R	None	R					
Name	ELT	None	DC [29:24]					

Bits	Name	Description
31	ELT	Enable Local Time 0= Local time is stopped, default 1= Local time is enabled Default Value: 0
29 : 16	DC	Denominator Configuration 0x0000 Illegal value 0x0001-3FFF Denominator Configuration Default Value: 4096
15 : 0	NCL	Numerator Configuration Low Write access to the TUR Numerator Configuration Low is only possible during configuration with TURCF.ELT = '0' or if TTOCF.EECS (external clock synchronization enabled) is set. When a new value for NCL is written outside TT Configuration Mode, the new value takes effect when TTOST.WECS is cleared to '0'. NCL is locked TTOST.WECS is '1'. 0x0000-FFFF Numerator Configuration Low Default Value: 0

10.1.52 CANFD0_CH0_TTOCN

TT Operation Control

Address: 0x40400114

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW	RW		RW	RW	RW
HW Access	R		R	R		R	R	R
Name	TMC [7:6]		RTIE	SWS [4:3]		SWP	ECS	SGT

Bits	15	14	13	12	11	10	9	8
SW Access	R	None	RW	RW	RW	RW	RW	RW
HW Access	RW	None	R	R	R	R	R	R
Name	LCKC	None	ESCN	NIG	TMG	FGP	GCS	TTIE

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15	LCKC	TT Operation Control Register Locked Set by a write access to register TTOCN. Reset when the updated configuration has been synchronized into the CAN clock domain. 0= Write access to TTOCN enabled 1= Write access to TTOCN locked Default Value: 0
13	ESCN	External Synchronization Control If enabled the M_TTCAN synchronizes its cycle time phase to an external event signaled by a rising edge at pin m_ttcan_evt (see Section 4.11). 0= External synchronization disabled 1= External synchronization enabled Default Value: 0

10.1.52 CANFD0_CH0_TTOCN (continued)

12	NIG	Next is Gap This bit can only be set when the M_TTCAN is the actual Time Master and when it is configured for external event-synchronized time-triggered operation (TTOCF.GEN = '1') 0= No action, reset by reception of any reference message 1= Transmit next reference message with Next_is_Gap = '1' Default Value: 0
11	TMG	Time Mark Gap 0= Reset by each reference message 1= Next reference message started when Register Time Mark interrupt TTIR.RTMI is activated Default Value: 0
10	FGP	Finish Gap Set by the CPU, reset by each reference message 0= No reference message requested 1= Application requested start of reference message Default Value: 0
9	GCS	Gap Control Select 0= Gap control independent from m_ttcan_evt 1= Gap control by input pin m_ttcan_evt Default Value: 0
8	TTIE	Trigger Time Mark Interrupt Pulse Enable External time mark events are configured by trigger memory element TMEX (see Section 2.4.7). A trigger time mark interrupt pulse is generated when the trigger memory element becomes active, and the M_TTCAN is in synchronization state In_Schedule or In_Gap. 0= Trigger Time Mark Interrupt output m_ttcan_tmp disabled 1= Trigger Time Mark Interrupt output m_ttcan_tmp enabled Default Value: 0
7 : 6	TMC	Register Time Mark Compare 00= No Register Time Mark Interrupt generated 01= Register Time Mark Interrupt if Time Mark = cycle time 10= Register Time Mark Interrupt if Time Mark = local time 11= Register Time Mark Interrupt if Time Mark = global time Default Value: 0
5	RTIE	Register Time Mark Interrupt Pulse Enable Register time mark interrupts are configured by register TTTMK. A register time mark interrupt pulse with the length of one NTU is generated when the time referenced by TTOCN.TMC (cycle, local, or global) equals TTTMK.TM, independent of the synchronization state. 0= Register Time Mark Interrupt output m_ttcan_rtp disabled 1= Register Time Mark Interrupt output m_ttcan_rtp enabled Default Value: 0
4 : 3	SWS	Stop Watch Source 00= Stop Watch disabled 01= Actual value of cycle time is copied to TTCPT.SWV 10= Actual value of local time is copied to TTCPT.SWV 11= Actual value of global time is copied to TTCPT.SWV Default Value: 0
2	SWP	Stop Watch Polarity 0= Rising edge trigger 1= Falling edge trigger Default Value: 0

10.1.52 CANFD0_CH0_TTOCN (continued)

1	ECS	External Clock Synchronization Writing a '1' to ECS sets TTOST.WECS if the node is the actual Time Master. ECS is reset after one Host clock period. The external clock synchronization takes effect at the start of the next basic cycle. Default Value: 0
0	SGT	Set Global time Writing a '1' to SGT sets TTOST.WGDT if the node is the actual Time Master. SGT is reset after one Host clock period. The global time preset takes effect when the node transmits the next reference message with the Master_Ref_Mark modified by the preset value written to TTGTP. Default Value: 0

10.1.53 CANFD0_CH0_TTGTP

TT Global Time Preset

Address: 0x40400118

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	TP [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	TP [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	CTP [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	CTP [31:24]							

Bits	Name	Description
31 : 16	CTP	Cycle Time Target Phase CTP is write-protected while TTOCN.ESCN or TTOST.SPL are set (see Section 4.11). 0x0000-FFFF Defines target value of cycle time when a rising edge of m_ttcan_evt is expected Default Value: 0
15 : 0	TP	Time Preset TP is write-protected while TTOST.WGTD is set. 0x0000-7FFF Next Master Reference Mark = Master Reference Mark + TP 0x8000 reserved 0x8001-FFFF Next Master Reference Mark = Master Reference Mark - (0x10000 - TP) Default Value: 0

10.1.54 CANFD0_CH0_TTTMK

TT Time Mark

Address: 0x4040011C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	TM_ [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	TM_ [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None	RW						
HW Access	None	R						
Name	None	TICC [22:16]						

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	RW	None						
Name	LCKM	None [30:24]						

Bits	Name	Description
31	LCKM	TT Time Mark Register Locked Always set by a write access to registers TTOCN. Set by write access to register TTTMK when TTOCN.TMC != '00'. Reset when the registers have been synchronized into the CAN clock domain. 0= Write access to TTTMK enabled 1= Write access to TTTMK locked Default Value: 0
22 : 16	TICC	Time Mark Cycle Code Cycle count for which the time mark is valid. 0b000000x valid for all cycles 0b000001c valid every second cycle at cycle count mod2 = c 0b00001cc valid every fourth cycle at cycle count mod4 = cc 0b0001ccc valid every eighth cycle at cycle count mod8 = ccc 0b001cccc valid every sixteenth cycle at cycle count mod16 = cccc 0b01ccccc valid every thirty-second cycle at cycle count mod32 = ccccc 0b1cccccc valid every sixty-fourth cycle at cycle count mod64 = cccccc Default Value: 0

10.1.54 CANFD0_CH0_TTTMK (continued)

15 : 0	TM_	Time Mark 0x0000-FFFF Time Mark Default Value: 0

10.1.55 CANFD0_CH0_TTIR

TT Interrupt Register

Address: 0x40400120

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	GTW	SWE	TTMI	RTMI	SOG	CSM_	SMC	SBC

Bits	15	14	13	12	11	10	9	8
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	RW	RW	RW	RW	RW	RW	RW	RW
Name	IWT	ELC	SE2	SE1	TXO	TXU	GTE	GTD

Bits	23	22	21	20	19	18	17	16
SW Access	None					RW1C	RW1C	RW1C
HW Access	None					RW	RW	RW
Name	None [23:19]					CER	AW	WT

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
18	CER	Configuration Error Trigger out of order. 0= No error found in trigger list 1= Error found in trigger list Default Value: 0
17	AW	Application Watchdog 0= Application watchdog served in time 1= Application watchdog not served in time Default Value: 0
16	WT	Watch Trigger 0= No missing reference message 1= Missing reference message (Level 0: cycle time 0xFF00) Default Value: 0
15	IWT	Initialization Watch Trigger The initialization is restarted by resetting IWT. 0= No missing reference message during system startup 1= No system startup due to missing reference message Default Value: 0

10.1.55 CANFD0_CH0_TTIR (continued)

14	ELC	Error Level Changed Not set when error level changed during initialization. 0= No change in error level 1= Error level changed Default Value: 0
13	SE2	Scheduling Error 2 0= No scheduling error 2 1= Scheduling error 2 occurred Default Value: 0
12	SE1	Scheduling Error 1 0= No scheduling error 1 1= Scheduling error 1 occurred Default Value: 0
11	TXO	Tx Count Overflow 0= Number of Tx Trigger as expected 1= More Tx trigger than expected in one matrix cycle Default Value: 0
10	TXU	Tx Count Underflow 0= Number of Tx Trigger as expected 1= Less Tx trigger than expected in one matrix cycle Default Value: 0
9	GTE	Global Time Error Synchronization deviation SD exceeds limit specified by TTOCF.LDSDL, TTCAN Level 0,2 only. 0= Synchronization deviation within limit 1= Synchronization deviation exceeded limit Default Value: 0
8	GTD	Global Time Discontinuity 0= No discontinuity of global time 1= Discontinuity of global time Default Value: 0
7	GTW	Global Time Wrap 0= No global time wrap occurred 1= Global time wrap from 0xFFFF to 0x0000 occurred Default Value: 0
6	SWE	Stop Watch Event 0= No rising/falling edge at stop watch trigger pin m_ttcan_swt detected 1= Rising/falling edge at stop watch trigger pin m_ttcan_swt detected Default Value: 0
5	TTMI	Trigger Time Mark Event Internal Internal time mark events are configured by trigger memory element TMIN (see Section 2.4.7). Set when the trigger memory element becomes active, and the M_TTCAN is in synchronization state In_Gap or In_Schedule. 0= Time mark not reached 1= Time mark reached (Level 0: cycle time TTOCF.IRTO * 0x200) Default Value: 0

10.1.55 CANFD0_CH0_TTIR (continued)

4	RTMI	Register Time Mark Interrupt Set when time referenced by TTOCN.TMC (cycle, local, or global) equals TTTMK.TM, independent of the synchronization state. 0= Time mark not reached 1= Time mark reached Default Value: 0
3	SOG	Start of Gap 0= No reference message seen with Next_is_Gap bit set 1= Reference message with Next_is_Gap bit set becomes valid Default Value: 0
2	CSM_	Change of Synchronization Mode 0= No change in master to slave relation or schedule synchronization 1= Master to slave relation or schedule synchronization changed, also set when TTOST.SPL is reset Default Value: 0
1	SMC	Start of Matrix Cycle 0= No Matrix Cycle started since bit has been reset 1= Matrix Cycle started Default Value: 0
0	SBC	Start of Basic Cycle 0= No Basic Cycle started since bit has been reset 1= Basic Cycle started Default Value: 0

10.1.56 CANFD0_CH0_TTIE

TT Interrupt Enable

Address: 0x40400124

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	GTWE	SWEE	TTMIE	RTMIE	SOGE	CSME	SMCE	SBCE

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	IWTE	ELCE	SE2E	SE1E	TXOE	TXUE	GTEE	GTDE

Bits	23	22	21	20	19	18	17	16
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [23:19]					CERE	AWE_	WTE

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
18	CERE	Configuration Error Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
17	AWE_	Application Watchdog Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
16	WTE	Watch Trigger Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
15	IWTE	Initialization Watch Trigger Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0

10.1.56 CANFD0_CH0_TTIE (continued)

14	ELCE	Change Error Level Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
13	SE2E	Scheduling Error 2 Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
12	SE1E	Scheduling Error 1 Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
11	TXOE	Tx Count Overflow Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
10	TXUE	Tx Count Underflow Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
9	GTEE	Global Time Error Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
8	GTDE	Global Time Discontinuity Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
7	GTWE	Global Time Wrap Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
6	SWEE	Stop Watch Event Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
5	TTMIE	Trigger Time Mark Event Internal Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
4	RTMIE	Register Time Mark Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
3	SOGE	Start of Gap Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0

10.1.56 CANFD0_CH0_TTIE (continued)

2	CSME	Change of Synchronization Mode Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
1	SMCE	Start of Matrix Cycle Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0
0	SBCE	Start of Basic Cycle Interrupt Enable 0= Interrupt Disabled 1= Interrupt Enabled Default Value: 0

10.1.57 CANFD0_CH0_TTILS

TT Interrupt Line Select

Address: 0x40400128

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	GTWL	SWEL	TTMIL	RTMIL	SOGL	CSML	SMCL	SBCL

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	IWTL	ELCL	SE2L	SE1L	TXOL	TXUL	GTEL	GTDL

Bits	23	22	21	20	19	18	17	16
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [23:19]					CERL	AWL_	WTL

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
18	CERL	Configuration Error Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
17	AWL_	Application Watchdog Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
16	WTL	Watch Trigger Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
15	IWTL	Initialization Watch Trigger Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0

10.1.57 CANFD0_CH0_TTILS (continued)

14	ELCL	Change Error Level Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
13	SE2L	Scheduling Error 2 Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
12	SE1L	Scheduling Error 1 Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
11	TXOL	Tx Count Overflow Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
10	TXUL	Tx Count Underflow Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
9	GTEL	Global Time Error Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
8	GTDL	Global Time Discontinuity Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
7	GTWL	Global Time Wrap Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
6	SWEL	Stop Watch Event Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
5	TTMIL	Trigger Time Mark Event Internal Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
4	RTMIL	Register Time Mark Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
3	SOGL	Start of Gap Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0

10.1.57 CANFD0_CH0_TTILS (continued)

2	CSML	Change of Synchronization Mode Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
1	SMCL	Start of Matrix Cycle Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0
0	SBCL	Start of Basic Cycle Interrupt Select 0= Assign to interrupt enabled by ILE.EINT0 1= Assign to interrupt enabled by ILE.EINT1 Default Value: 0

10.1.58 CANFD0_CH0_TTOST

TT Operation Status

Address: 0x4040012C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R		R		R	
HW Access	RW	RW	RW		RW		RW	
Name	QCS	QGTP	SYS [5:4]		MS [3:2]		EL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	RTO [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R	R	None					
HW Access	RW	RW	None					
Name	GFI	WGTD	None [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	R	R	R	R		
HW Access	RW	RW	RW	RW	RW	RW		
Name	SPL	WECS	AWE	WFE	GSI	TMP [26:24]		

Bits	Name	Description
31	SPL	Schedule Phase Lock The bit is valid only when external synchronization is enabled (TTOCN.ESCN = '1'). In this case it signals that the difference between cycle time configured by TTGTP.CTP and the cycle time at the rising edge at pin m_ttcan_evt is less or equal 9 NTU (see Section 4.11). 0= Phase outside range 1= Phase inside range Default Value: 0
30	WECS	Wait for External Clock Synchronization 0= No external clock synchronization pending 1= Node waits for external clock synchronization to take effect. The bit is reset at the start of the next basic cycle. Default Value: 0

10.1.58 CANFD0_CH0_TTOST (continued)

29	AWE	Application Watchdog Event The application watchdog is served by reading TTOST. When the watchdog is not served in time, bit AWE is set, all TTCAN communication is stopped, and the M_TTCAN is set into Bus Monitoring Mode. 0= Application Watchdog served in time 1= Failed to serve Application Watchdog in time Default Value: 0
28	WFE	Wait for Event 0= No Gap announced, reset by a reference message with Next_is_Gap = '0' 1= Reference message with Next_is_Gap = '1' received Default Value: 0
27	GSI	Gap Started Indicator 0= No Gap in schedule, reset by each reference message and for all time slaves 1= Gap time after Basic Cycle has started Default Value: 0
26 : 24	TMP	Time Master Priority 0x0-7 Priority of actual Time Master Default Value: 0
23	GFI	Gap Finished Indicator Set when the CPU writes TTOCN.FGP, or by a time mark interrupt if TMG = '1', or via input pin m_ttcan_evt if TTOCN.GCS = '1'. Not set by Ref_Trigger_Gap or when Gap is finished by another node sending a reference message. 0= Reset at the end of each reference message 1= Gap finished by M_TTCAN Default Value: 0
22	WGTD	Wait for Global Time Discontinuity 0= No global time preset pending 1= Node waits for the global time preset to take effect. The bit is reset when the node has transmitted a reference message with Disc_Bit = '1' or after it received a reference message. Default Value: 0
15 : 8	RTO	Reference Trigger Offset The Reference Trigger Offset value is a signed integer with a range from -127 (0x81) to 127 (0x7F). There is no notification when the lower limit of -127 is reached. In case the M_TTCAN becomes Time Master (MS[1:0] = '11'), the reset of RTO is delayed due to synchronization between Host and CAN clock domain. For time slaves the value configured by TTOCF.IRTO is read. 0x00-FF Actual Reference Trigger offset value Default Value: 0
7	QCS	Quality of Clock Speed Only relevant in TTCAN Level 0 and Level 2, otherwise fixed to '1'. 0= Local clock speed not synchronized to Time Master clock speed 1= Synchronization Deviation <= SDL Default Value: 0
6	QGTP	Quality of Global Time Phase Only relevant in TTCAN Level 0 and Level 2, otherwise fixed to '0'. 0= Global time not valid 1= Global time in phase with Time Master Default Value: 0

10.1.58 CANFD0_CH0_TTOST (continued)

5 : 4	SYS	Synchronization State 00= Out of Synchronization 01= Synchronizing to TTCAN communication 10= Schedule suspended by Gap (In_Gap) 11= Synchronized to schedule (In_Schedule) Default Value: 0
3 : 2	MS	Master State 00= Master_Off, no master properties relevant 01= Operating as Time Slave 10= Operating as Backup Time Master 11= Operating as current Time Master Default Value: 0
1 : 0	EL	Error Level 00= Severity 0 - No Error 01= Severity 1 - Warning 10= Severity 2 - Error 11= Severity 3 - Severe Error Default Value: 0

10.1.59 CANFD0_CH0_TURNA

TUR Numerator Actual

Address: 0x40400130

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	NAV [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	NAV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						R	
HW Access	None						RW	
Name	None [23:18]						NAV [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
17 : 0	NAV	Numerator Actual Value 0x0EFFF reserved 0x0F000-20FFF Actual numerator value 0x21000 reserved Default Value: 65536

10.1.60 CANFD0_CH0_TTLGT

TT Local & Global Time

Address: 0x40400134

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	LT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	LT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	GT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	GT [31:24]							

Bits	Name	Description
31 : 16	GT	Global Time Non-fractional part of the sum of the node's local time and its local offset (see Section 4.5). 0x0000-FFFF Global time value of TTCAN network Default Value: 0
15 : 0	LT	Local Time Non-fractional part of local time, incremented once each local NTU (see Section 4.5). 0x0000-FFFF Local time value of TTCAN node Default Value: 0

10.1.61 CANFD0_CH0_TTCTC

TT Cycle Time & Count

Address: 0x40400138

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	CT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	CT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None		R					
HW Access	None		RW					
Name	None [23:22]		CC [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
21 : 16	CC	Cycle Count 0x00-3F Number of actual Basic Cycle in the System Matrix Default Value: 63
15 : 0	CT	Cycle Time Non-fractional part of the difference of the node's local time and Ref_Mark (see Section 4.5). 0x0000-FFFF Cycle time value of TTCAN Basic Cycle Default Value: 0

10.1.62 CANFD0_CH0_TTCPT

TT Capture Time

Address: 0x4040013C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R					
HW Access	None		RW					
Name	None [7:6]		CCV [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	SWV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	SWV [31:24]							

Bits	Name	Description
31 : 16	SWV	Stop Watch Value On a rising/falling edge (as configured via TTOCN.SWP) at the Stop Watch Trigger pin m_ttcan_swt, when TTOCN.SWS is != '00' and TTIR.SWE is '0', the actual time value as selected by TTOCN.SWS (cycle, local, global) is copied to SWV and TTIR.SWE will be set to '1'. Capturing of the next stop watch value is enabled by resetting TTIR.SWE. 0x0000-FFFF Captured Stop Watch value Default Value: 0
5 : 0	CCV	Cycle Count Value Cycle count value captured together with SWV. 0x00-3F Captured cycle count value Default Value: 0

10.1.63 CANFD0_CH0_TTCSM

TT Cycle Sync Mark

Address: 0x40400140

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	CSM [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	CSM [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CSM	Cycle Sync Mark The Cycle Sync Mark is measured Default Value: 0

10.1.64 CANFD0_CH0_RXFTOP_CTL

Receive FIFO Top control

Address: 0x40400180

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						F1TPE	F0TPE

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	F1TPE	FIFO 1 Top Pointer Enable. Default Value: 0
0	F0TPE	FIFO 0 Top Pointer Enable. This enables the FIFO top pointer logic to set the FIFO Top Address (FnTA) and message word counter. This logic is also disabled when the IP is being reconfigured (CCCR.CCE=1). When this logic is disabled a Read from RXFTOP0_DATA is undefined. Default Value: 0

10.1.65 CANFD0_CH0_RXFTOP0_STAT

Receive FIFO 0 Top Status

Address: 0x404001A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	F0TA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	F0TA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	F0TA	Current FIFO 0 Top Address. This is a pointer to the next word in the message buffer defined by the FIFO Start Address (FnSA), Get Index (FnGI), the FIFO message size (FnDS) and the message word counter (FnMWC) FnTA = FnSA + FnGI * msg_size[FnDS] + FnMWC Default Value: 0

10.1.66 CANFD0_CH0_RXFTOP0_DATA

Receive FIFO 0 Top Data

Address: 0x404001A8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	F0TD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	F0TD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	F0TD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	F0TD [31:24]							

Bits	Name	Description
31 : 0	F0TD	When enabled (F0TPE=1) read data from MRAM at location FnTA. This register can have a read side effect if the following conditions are met: - M_TTCAN not being reconfigured (CCCR.CCE=0) - FIFO Top Pointer logic is enabled (FnTPE=1) - FIFO is not empty (FnFL!=0) The read side effect is as follows: - if FnMWC pointed to the last word of the message (as indicated by FnDS) then the corresponding message index (FnGI) is automatically acknowledge by a write to FnAI - FnMWC is incremented (or restarted if FnMWC pointed to the last word of the message) - the FIFO top address FnTA is incremented (with FIFO wrap around) When this logic is disabled (F0TPE=0) a Read from this register returns undefined data. Default Value: Undefined

10.1.67 CANFD0_CH0_RXFTOP1_STAT

Receive FIFO 1 Top Status

Address: 0x404001B0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	F1TA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	F1TA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	F1TA	See F0TA description Default Value: 0

10.1.68 CANFD0_CH0_RXFTOP1_DATA

Receive FIFO 1 Top Data

Address: 0x404001B8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	F1TD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	F1TD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	F1TD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	F1TD [31:24]							

Bits	Name	Description
31 : 0	F1TD	See F0TD description Default Value: Undefined

10.1.69 CANFD0_CTL

Global CAN control register

Address: 0x40401000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							STOP_REQ

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	MRAM_OFF	None [30:24]						

Bits	Name	Description
31	MRAM_OFF	MRAM off 0= Default MRAM on (with MRAM retained in DeepSleep). 1= Switch MRAM off (not retained) to save power. Before setting this bit all the CAN channels have to be powered down using the STOP_REQ/ACK bits. When the MRAM is off any access attempt to it is considered an address error (as if MRAM_-SIZE=0). After switching the MRAM on again software needs to allow for a certain power up time before MRAM can be used, i.e. before STOP_REQ can be de-asserted. The power up time is equivalent to the system SRAM power up time specified in the CPUSS.RAM_PWR_DELAY_CTL register. To meet S8 platform requirements, MRAM_OFF should be set to 0 prior to transitioning to Hiber-nate mode. Default Value: 0
0	STOP_REQ	Clock Stop Request for each TTCAN IP . The m_ttcan_clkstop_req of each TTCAN IP is directly driven by these bits. Default Value: 0

10.1.70 CANFD0_STATUS

Global CAN status register

Address: 0x40401004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							STOP_ACK

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	STOP_ACK	Clock Stop Acknowledge for each TTCAN IP. These bits are directly driven by m_ttcan_clkstop_ack of each TTCAN IP. When this bit is set the corresponding TTCAN IP clocks will be gated off, except HCLK will enabled for each AHB write Default Value: 0

10.1.71 CANFD0_INTR0_CAUSE

Consolidated interrupt0 cause register

Address: 0x40401010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							INT0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	INT0	Show pending m_ttcan_int0 of each channel Default Value: 0

10.1.72 CANFD0_INTR1_CAUSE

Consolidated interrupt1 cause register

Address: 0x40401014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							INT1

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	INT1	Show pending m_ttcan_int1 of each channel Default Value: 0

10.1.73 CANFD0_TS_CTL

Time Stamp control register

Address: 0x40401020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	PRESCALE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	PRESCALE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	ENABLED	None [30:24]						

Bits	Name	Description
31	ENABLED	Counter enable bit 0 = Count disabled. Stop counting up and keep the counter value 1 = Count enabled. Start counting up from the current value Default Value: 0
15 : 0	PRESCALE	Time Stamp counter prescale value. When enabled divide the Host clock (HCLK) by PRESCALE+1 to create Time Stamp clock ticks. Default Value: 0

10.1.74 CANFD0_TS_CNT

Time Stamp counter value

Address: 0x40401024

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	VALUE	The counter value of the Time Stamp Counter. When enabled this counter will count Time Stamp clock ticks from the pre-scaler. When written this counter and the pre-scaler will reset to 0 (write data is ignored). Default Value: 0

11 Inter-IC Sound Bus (I2S) Registers

This section discusses the Inter-IC Sound Bus (I2S) registers. It lists all the registers in mapping tables, in address order.

11.1 Register Details

Register	Address	Description
I2S0_CTL	0x404F0000	Control
I2S0_CLOCK_CTL	0x404F0010	Clock control
I2S0_CMD	0x404F0020	Command
I2S0_TR_CTL	0x404F0040	Trigger control
I2S0_TX_CTL	0x404F0080	Transmitter control
I2S0_TX_FIFO_CTL	0x404F0200	TX FIFO control
I2S0_TX_FIFO_STATUS	0x404F0204	TX FIFO status
I2S0_TX_FIFO_WR	0x404F0208	TX FIFO write
I2S0_INTR	0x404F0F00	Interrupt register
I2S0_INTR_SET	0x404F0F04	Interrupt set register
I2S0_INTR_MASK	0x404F0F08	Interrupt mask register
I2S0_INTR_MASKED	0x404F0F0C	Interrupt masked register

11.1.1 I2S0_CTL

Control

Address: 0x404F0000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None	RW	None					
HW Access	None	R	None					
Name	None	TX_EN-ABLED	None					

Bits	Name	Description
30	TX_ENABLED	Enables the I2S TX component: '0': Disabled. '1': Enabled. Default Value: 0

11.1.2 I2S0_CLOCK_CTL

Clock control

Address: 0x404F0010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		CLOCK_DIV [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							CLOCK_-SEL

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	CLOCK_SEL	Selects clock to be used by I2S: '0': Internal clock ("clk_audio_i2s") '1': External clock ("clk_i2s_if") Default Value: 0
5 : 0	CLOCK_DIV	Frequency divisor for generating I2S clock frequency. The selected clock with CLOCK_SEL is divided by this. "0": Bypass "1": 2 x "2": 3 x "3": 4 x ... "62": 63 x "63": 64 x Default Value: 0

11.1.3 I2S0_CMD

Command

Address: 0x404F0020

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							TX_START

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							TX_PAUSE

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	TX_PAUSE	Pause enable: '0': Disabled (TX FIFO data is sent over I2S). '1': Enabled ("0" data is sent over I2S, instead of TX FIFO data). Default Value: 0
0	TX_START	Transmitter enable: '0': Disabled. '1': Enabled. Default Value: 0

11.1.4 I2S0_TR_CTL

Trigger control

Address: 0x404F0040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							TX-_REQ_EN

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	TX_REQ_EN	Trigger output ("tr_i2s_tx_req") enable for requests of DMA transfer in transmission '0': Disabled. '1': Enabled. Default Value: 0

11.1.5 I2S0_TX_CTL

Transmitter control

Address: 0x404F0080

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW			RW	None		
HW Access	R	R			R	None		
Name	MS	CH_NR [6:4]			B_-CLOCK_-INV	None		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW	RW	None	RW	RW	
HW Access	None		R	R	None	R	R	
Name	None [15:14]		WD_EN	OVHDATA	None	WS_PULSE	I2S_MODE [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	WORD_LEN [22:20]			None	CH_LEN [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [31:26]						SCKI_POL	SCKO_POL

Bits	Name	Description
25	SCKI_POL	Reserved, and always 0. Note: Slave mode is not supported by this device. Default Value: 0
24	SCKO_POL	TX master bit clock polarity. When this bit is 1, the outgoing tx_sck signal is inverted after it has been transmitted from the I2S transceiver core. This bit does not affect the internal serial data transmission timing. The word sync (TX_WS) signal is not affected by this bit setting. '0': When transmitter is in master mode, serial data is transmitted from the falling bit clock edge '1': When transmitter is in master mode, serial data is transmitted from the rising bit clock edge Default Value: 0
22 : 20	WORD_LEN	Word length in number of bits: Note: - When this field is configured to "6" or "7", the length is set to 32-bit (same as "5"). - Don't configure this field as beyond Channel length. Default Value: 4

11.1.5 I2S0_TX_CTL (continued)

0x0: BIT_LEN8 :

8-bit

0x1: BIT_LEN16 :

16-bit

0x2: BIT_LEN18 :

18-bit

0x3: BIT_LEN20 :

20-bit

0x4: BIT_LEN24 :

24-bit

0x5: BIT_LEN32 :

32-bit

18 : 16	CH_LEN	Channel length in number of bits: Note: - When this field is configured to "6" or "7", the length is set to 32-bit (same as "5"). - When TDM mode, must be 32-bit length to this field. Default Value: 4

0x0: BIT_LEN8 :

8-bit

0x1: BIT_LEN16 :

16-bit

0x2: BIT_LEN18 :

18-bit

0x3: BIT_LEN20 :

20-bit

0x4: BIT_LEN24 :

24-bit

11.1.5 I2S0_TX_CTL (continued)

		0x5: BIT_LEN32 : 32-bit
13	WD_EN	Reserved, and always 0. Note: Slave mode is not supported by this device. Default Value: 0
12	OVHDATA	Set overhead value: '0': Set to '0' '1': Set to '1' Default Value: 0
10	WS_PULSE	Set WS pulse width in TDM mode: Note: When not TDM mode, must be "1". Default Value: 1 **0x0: SCK_PERIOD :** Pulse width is 1 SCK period **0x1: CH_LENGTH :** Pulse width is 1 channel length
9 : 8	I2S_MODE	Select I2S, left-justified or TDM: Default Value: 1 **0x0: LEFT_JUSTIFIED :** Left Justified **0x1: I2S :** I2S mode **0x2: TDM_A :** TDM mode A, the 1st Channel align to WSO Rising Edge **0x3: TDM_B :** TDM mode B, the 1st Channel align to WSO Rising edge with1 SCK Delay
7	MS	Set interface in master mode (write always 1). Note: Slave mode is not supported by this device. Default Value: 0 **0x0: SLAVE :** Slave

11.1.5 I2S0_TX_CTL (continued)

		0x1: MASTER : Master
6 : 4	CH_NR	Specifies number of channels per frame: Note: only "2channels" is supported during Left Justfied or I2S mode. Hence software must set "1" to this field in the modes. Default Value: 1 **0x0: CH_NUM1 :** 1 channel **0x1: CH_NUM2 :** 2 channels **0x2: CH_NUM3 :** 3 channels **0x3: CH_NUM4 :** 4 channels **0x4: CH_NUM5 :** 5 channels **0x5: CH_NUM6 :** 6 channels **0x6: CH_NUM7 :** 7 channels **0x7: CH_NUM8 :** 8 channels
3	B_CLOCK_INV	Reserved, and always 0. Note: Slave mode is not supported by this device. Default Value: 0 **0x0: FALLING_EDGE_TX :** SDO transmitted at SCK falling edge when TX_CTL.SCKI_POL=0

11.1.5 I2S0_TX_CTL (continued)

0x1: RISING_EDGE_TX :

SDO transmitted at SCK rising edge when TX_CTL.SCKI_POL=0

11.1.6 I2S0_TX_FIFO_CTL

TX FIFO control

Address: 0x404F0200

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	TRIGGER_LEVEL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [23:18]						FREEZE	CLEAR

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
17	FREEZE	When '1', hardware reads from the TX FIFO do not remove FIFO entries. Freeze will not advance the TX FIFO read pointer. This field is used only for debugging purposes. Default Value: 0
16	CLEAR	When '1', the TX FIFO and TX_BUF are cleared/invalidated. Invalidation will last for as long as this field is '1'. If a quick clear/invalidation is required, the field should be set to '1' and be followed by a set to '0'. If a clear/invalidation is required for an extended time period, the field should be set to '1' during the complete time period. Default Value: 0
7 : 0	TRIGGER_LEVEL	Trigger level. When the TX FIFO has less entries than the number of this field, a transmitter trigger event is generated. Default Value: 0

11.1.7 I2S0_TX_FIFO_STATUS

TX FIFO status

Address: 0x404F0204

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	USED [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							USED

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	RD_PTR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	WR_PTR [31:24]							

Bits	Name	Description
31 : 24	WR_PTR	TX FIFO write pointer: FIFO location at which a new data frame is written by the host. This field is used only for debugging purposes. Default Value: 0
23 : 16	RD_PTR	TX FIFO read pointer: FIFO location from which a data frame is read by the hardware.This field is used only for debugging purposes. Default Value: 0
8 : 0	USED	Number of entries in the TX FIFO. The field value is in the range [0, 256]. Default Value: 0

11.1.8 I2S0_TX_FIFO_WR

TX FIFO write

Address: 0x404F0208

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	W							
HW Access	R							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	W							
HW Access	R							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data written into the TX FIFO. Behavior is similar to that of a PUSH operation. Note: Don't access to this register while TX_FIFO_CTL.CLEAR is '1'. Default Value: 0

11.1.9 I2S0_INTR

Interrupt register

Address: 0x404F0F00

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW1C	RW1C	RW1C	None		RW1C	RW1C
HW Access	None	RW1S	RW1S	RW1S	None		RW1S	RW1S
Name	None	TX_UN-DERFLOW	TX_OVER-FLOW	TX_EMPTY	None [3:2]		TX_NOT_-FULL	TX_TRIG-GER

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1C
HW Access	None							RW1S
Name	None [15:9]							TX_WD

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	TX_WD	Reserved, and always 0. Note: Slave mode is not supported by this device. Default Value: 0
6	TX_UNDERFLOW	Attempt to read from an empty TX FIFO. This happens when the IP is ready to transfer data and TX_EMPTY is '1'. Default Value: 0
5	TX_OVERFLOW	Attempt to write to a full TX FIFO. Default Value: 0
4	TX_EMPTY	TX FIFO is empty; i.e. it has 0 entries. Default Value: 0
1	TX_NOT_FULL	TX FIFO is not full. Default Value: 0
0	TX_TRIGGER	Less entries in the TX FIFO than the value specified by TRIGGER_LEVEL in TX_FIFO_CTRL. Default Value: 0

11.1.10 I2S0_INTR_SET

Interrupt set register

Address: 0x404F0F04

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW1S	RW1S	RW1S	None		RW1S	RW1S
HW Access	None	A	A	A	None		A	A
Name	None	TX_UN-DERFLOW	TX_OVER-FLOW	TX_EMPTY	None [3:2]		TX_NOT_-FULL	TX_TRIG-GER

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW1S
HW Access	None							A
Name	None [15:9]							TX_WD

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	TX_WD	Reserved, and always 0. Note: Slave mode is not supported by this device. Default Value: 0
6	TX_UNDERFLOW	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
5	TX_OVERFLOW	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
4	TX_EMPTY	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
1	TX_NOT_FULL	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	TX_TRIGGER	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

11.1.11 I2S0_INTR_MASK

Interrupt mask register

Address: 0x404F0F08

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	RW	RW	None		RW	RW
HW Access	None	R	R	R	None		R	R
Name	None	TX_UN-DERFLOW	TX_OVER-FLOW	TX_EMPTY	None [3:2]		TX_NOT_-FULL	TX_TRIG-GER

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							TX_WD

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	TX_WD	Reserved, and always 0. Note: Slave mode is not supported by this device. Default Value: 0
6	TX_UNDERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
5	TX_OVERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
4	TX_EMPTY	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	TX_NOT_FULL	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	TX_TRIGGER	Mask bit for corresponding bit in interrupt request register. Default Value: 0

11.1.12 I2S0_INTR_MASKED

Interrupt masked register

Address: 0x404F0F0C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	R	R	R	None		R	R
HW Access	None	W	W	W	None		W	W
Name	None	TX_UN-DERFLOW	TX_OVER-FLOW	TX_EMPTY	None [3:2]		TX_NOT_-FULL	TX_TRIG-GER

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							TX_WD

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	TX_WD	Reserved, and always 0. Note: Slave mode is not supported by this device. Default Value: 0
6	TX_UNDERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
5	TX_OVERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
4	TX_EMPTY	Logical and of corresponding request and mask bits. Default Value: 0
1	TX_NOT_FULL	Logical and of corresponding request and mask bits. Default Value: 0
0	TX_TRIGGER	Logical and of corresponding request and mask bits. Default Value: 0

12 Timer, Counter, PWM (TCPWM) Registers

This section discusses the Timer, Counter, PWM (TCPWM) registers. It lists all the registers in mapping tables, in address order.

12.1 Register Details

Register	Address	Description
TCPWM_CTRL	0x40200000	TCPWM control register 0.
TCPWM_CMD	0x40200008	TCPWM command register.
TCPWM_INTR_CAUSE	0x4020000C	TCPWM Counter interrupt cause register.
TCPWM_CNT0_CTRL	0x40200100	Counter control register
TCPWM_CNT0_STATUS	0x40200104	Counter status register
TCPWM_CNT0_COUNTER	0x40200108	Counter count register
TCPWM_CNT0_CC	0x4020010C	Counter compare/capture register
TCPWM_CNT0_CC_BUFF	0x40200110	Counter buffered compare/capture register
TCPWM_CNT0_PERIOD	0x40200114	Counter period register
TCPWM_CNT0_PERIOD_BUFF	0x40200118	Counter buffered period register
TCPWM_CNT0_TR_CTRL0	0x40200120	Counter trigger control register 0
TCPWM_CNT0_TR_CTRL1	0x40200124	Counter trigger control register 1
TCPWM_CNT0_TR_CTRL2	0x40200128	Counter trigger control register 2
TCPWM_CNT0_INTR	0x40200130	Interrupt request register.
TCPWM_CNT0_INTR_SET	0x40200134	Interrupt set request register.
TCPWM_CNT0_INTR_MASK	0x40200138	Interrupt mask register.
TCPWM_CNT0_INTR_MASKED	0x4020013C	Interrupt masked request register
TCPWM_CNT1_CTRL	0x40200140	Counter control register. See TCPWM_CNT0_CTRL for the details of bit fields.
TCPWM_CNT1_STATUS	0x40200144	Counter status register. See TCPWM_CNT0_STATUS for the details of bit fields.
TCPWM_CNT1_COUNTER	0x40200148	Counter count register. See TCPWM_CNT0_COUNTER for the details of bit fields.
TCPWM_CNT1_CC	0x4020014C	Counter compare/capture register. See TCPWM_CNT0_CC for the details of bit fields.
TCPWM_CNT1_CC_BUFF	0x40200150	Counter buffered compare/capture register. See TCPWM_CNT0_CC_BUFF for the details of bit fields.
TCPWM_CNT1_PERIOD	0x40200154	Counter period register. See TCPWM_CNT0_PERIOD for the details of bit fields.
TCPWM_CNT1_PERIOD_BUFF	0x40200158	Counter buffered period register. See TCPWM_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM_CNT1_TR_CTRL0	0x40200160	Counter trigger control register 0. See TCPWM_CNT0_TR_CTRL0 for the details of bit fields.
TCPWM_CNT1_TR_CTRL1	0x40200164	Counter trigger control register 1. See TCPWM_CNT0_TR_CTRL1 for the details of bit fields.

Register	Address	Description
TCPWM_CNT1_TR_CTRL2	0x40200168	Counter trigger control register 2. See TCPWM_CNT0_TR_CTRL2 for the details of bit fields.
TCPWM_CNT1_INTR	0x40200170	Interrupt request register.. See TCPWM_CNT0_INTR for the details of bit fields.
TCPWM_CNT1_INTR_SET	0x40200174	Interrupt set request register.. See TCPWM_CNT0_INTR_SET for the details of bit fields.
TCPWM_CNT1_INTR_MASK	0x40200178	Interrupt mask register.. See TCPWM_CNT0_INTR_MASK for the details of bit fields.
TCPWM_CNT1_INTR_MASKED	0x4020017C	Interrupt masked request register. See TCPWM_CNT0_INTR_MASKED for the details of bit fields.
TCPWM_CNT2_CTRL	0x40200180	Counter control register. See TCPWM_CNT0_CTRL for the details of bit fields.
TCPWM_CNT2_STATUS	0x40200184	Counter status register. See TCPWM_CNT0_STATUS for the details of bit fields.
TCPWM_CNT2_COUNTER	0x40200188	Counter count register. See TCPWM_CNT0_COUNTER for the details of bit fields.
TCPWM_CNT2_CC	0x4020018C	Counter compare/capture register. See TCPWM_CNT0_CC for the details of bit fields.
TCPWM_CNT2_CC_BUFF	0x40200190	Counter buffered compare/capture register. See TCPWM_CNT0_CC_BUFF for the details of bit fields.
TCPWM_CNT2_PERIOD	0x40200194	Counter period register. See TCPWM_CNT0_PERIOD for the details of bit fields.
TCPWM_CNT2_PERIOD_BUFF	0x40200198	Counter buffered period register. See TCPWM_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM_CNT2_TR_CTRL0	0x402001A0	Counter trigger control register 0. See TCPWM_CNT0_TR_CTRL0 for the details of bit fields.
TCPWM_CNT2_TR_CTRL1	0x402001A4	Counter trigger control register 1. See TCPWM_CNT0_TR_CTRL1 for the details of bit fields.
TCPWM_CNT2_TR_CTRL2	0x402001A8	Counter trigger control register 2. See TCPWM_CNT0_TR_CTRL2 for the details of bit fields.
TCPWM_CNT2_INTR	0x402001B0	Interrupt request register.. See TCPWM_CNT0_INTR for the details of bit fields.
TCPWM_CNT2_INTR_SET	0x402001B4	Interrupt set request register.. See TCPWM_CNT0_INTR_SET for the details of bit fields.
TCPWM_CNT2_INTR_MASK	0x402001B8	Interrupt mask register.. See TCPWM_CNT0_INTR_MASK for the details of bit fields.
TCPWM_CNT2_INTR_MASKED	0x402001BC	Interrupt masked request register. See TCPWM_CNT0_INTR_MASKED for the details of bit fields.
TCPWM_CNT3_CTRL	0x402001C0	Counter control register. See TCPWM_CNT0_CTRL for the details of bit fields.
TCPWM_CNT3_STATUS	0x402001C4	Counter status register. See TCPWM_CNT0_STATUS for the details of bit fields.
TCPWM_CNT3_COUNTER	0x402001C8	Counter count register. See TCPWM_CNT0_COUNTER for the details of bit fields.
TCPWM_CNT3_CC	0x402001CC	Counter compare/capture register. See TCPWM_CNT0_CC for the details of bit fields.
TCPWM_CNT3_CC_BUFF	0x402001D0	Counter buffered compare/capture register. See TCPWM_CNT0_CC_BUFF for the details of bit fields.
TCPWM_CNT3_PERIOD	0x402001D4	Counter period register. See TCPWM_CNT0_PERIOD for the details of bit fields.
TCPWM_CNT3_PERIOD_BUFF	0x402001D8	Counter buffered period register. See TCPWM_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM_CNT3_TR_CTRL0	0x402001E0	Counter trigger control register 0. See TCPWM_CNT0_TR_CTRL0 for the details of bit fields.
TCPWM_CNT3_TR_CTRL1	0x402001E4	Counter trigger control register 1. See TCPWM_CNT0_TR_CTRL1 for the details of bit fields.
TCPWM_CNT3_TR_CTRL2	0x402001E8	Counter trigger control register 2. See TCPWM_CNT0_TR_CTRL2 for the details of bit fields.
TCPWM_CNT3_INTR	0x402001F0	Interrupt request register.. See TCPWM_CNT0_INTR for the details of bit fields.
TCPWM_CNT3_INTR_SET	0x402001F4	Interrupt set request register.. See TCPWM_CNT0_INTR_SET for the details of bit fields.
TCPWM_CNT3_INTR_MASK	0x402001F8	Interrupt mask register.. See TCPWM_CNT0_INTR_MASK for the details of bit fields.
TCPWM_CNT3_INTR_MASKED	0x402001FC	Interrupt masked request register. See TCPWM_CNT0_INTR_MASKED for the details of bit fields.
TCPWM_CNT4_CTRL	0x40200200	Counter control register. See TCPWM_CNT0_CTRL for the details of bit fields.
TCPWM_CNT4_STATUS	0x40200204	Counter status register. See TCPWM_CNT0_STATUS for the details of bit fields.
TCPWM_CNT4_COUNTER	0x40200208	Counter count register. See TCPWM_CNT0_COUNTER for the details of bit fields.
TCPWM_CNT4_CC	0x4020020C	Counter compare/capture register. See TCPWM_CNT0_CC for the details of bit fields.
TCPWM_CNT4_CC_BUFF	0x40200210	Counter buffered compare/capture register. See TCPWM_CNT0_CC_BUFF for the details of bit fields.
TCPWM_CNT4_PERIOD	0x40200214	Counter period register. See TCPWM_CNT0_PERIOD for the details of bit fields.
TCPWM_CNT4_PERIOD_BUFF	0x40200218	Counter buffered period register. See TCPWM_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM_CNT4_TR_CTRL0	0x40200220	Counter trigger control register 0. See TCPWM_CNT0_TR_CTRL0 for the details of bit fields.
TCPWM_CNT4_TR_CTRL1	0x40200224	Counter trigger control register 1. See TCPWM_CNT0_TR_CTRL1 for the details of bit fields.

Register	Address	Description
TCPWM_CNT4_TR_CTRL2	0x40200228	Counter trigger control register 2. See TCPWM_CNT0_TR_CTRL2 for the details of bit fields.
TCPWM_CNT4_INTR	0x40200230	Interrupt request register.. See TCPWM_CNT0_INTR for the details of bit fields.
TCPWM_CNT4_INTR_SET	0x40200234	Interrupt set request register.. See TCPWM_CNT0_INTR_SET for the details of bit fields.
TCPWM_CNT4_INTR_MASK	0x40200238	Interrupt mask register.. See TCPWM_CNT0_INTR_MASK for the details of bit fields.
TCPWM_CNT4_INTR_MASKED	0x4020023C	Interrupt masked request register. See TCPWM_CNT0_INTR_MASKED for the details of bit fields.
TCPWM_CNT5_CTRL	0x40200240	Counter control register. See TCPWM_CNT0_CTRL for the details of bit fields.
TCPWM_CNT5_STATUS	0x40200244	Counter status register. See TCPWM_CNT0_STATUS for the details of bit fields.
TCPWM_CNT5_COUNTER	0x40200248	Counter count register. See TCPWM_CNT0_COUNTER for the details of bit fields.
TCPWM_CNT5_CC	0x4020024C	Counter compare/capture register. See TCPWM_CNT0_CC for the details of bit fields.
TCPWM_CNT5_CC_BUFF	0x40200250	Counter buffered compare/capture register. See TCPWM_CNT0_CC_BUFF for the details of bit fields.
TCPWM_CNT5_PERIOD	0x40200254	Counter period register. See TCPWM_CNT0_PERIOD for the details of bit fields.
TCPWM_CNT5_PERIOD_BUFF	0x40200258	Counter buffered period register. See TCPWM_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM_CNT5_TR_CTRL0	0x40200260	Counter trigger control register 0. See TCPWM_CNT0_TR_CTRL0 for the details of bit fields.
TCPWM_CNT5_TR_CTRL1	0x40200264	Counter trigger control register 1. See TCPWM_CNT0_TR_CTRL1 for the details of bit fields.
TCPWM_CNT5_TR_CTRL2	0x40200268	Counter trigger control register 2. See TCPWM_CNT0_TR_CTRL2 for the details of bit fields.
TCPWM_CNT5_INTR	0x40200270	Interrupt request register.. See TCPWM_CNT0_INTR for the details of bit fields.
TCPWM_CNT5_INTR_SET	0x40200274	Interrupt set request register.. See TCPWM_CNT0_INTR_SET for the details of bit fields.
TCPWM_CNT5_INTR_MASK	0x40200278	Interrupt mask register.. See TCPWM_CNT0_INTR_MASK for the details of bit fields.
TCPWM_CNT5_INTR_MASKED	0x4020027C	Interrupt masked request register. See TCPWM_CNT0_INTR_MASKED for the details of bit fields.
TCPWM_CNT6_CTRL	0x40200280	Counter control register. See TCPWM_CNT0_CTRL for the details of bit fields.
TCPWM_CNT6_STATUS	0x40200284	Counter status register. See TCPWM_CNT0_STATUS for the details of bit fields.
TCPWM_CNT6_COUNTER	0x40200288	Counter count register. See TCPWM_CNT0_COUNTER for the details of bit fields.
TCPWM_CNT6_CC	0x4020028C	Counter compare/capture register. See TCPWM_CNT0_CC for the details of bit fields.
TCPWM_CNT6_CC_BUFF	0x40200290	Counter buffered compare/capture register. See TCPWM_CNT0_CC_BUFF for the details of bit fields.
TCPWM_CNT6_PERIOD	0x40200294	Counter period register. See TCPWM_CNT0_PERIOD for the details of bit fields.
TCPWM_CNT6_PERIOD_BUFF	0x40200298	Counter buffered period register. See TCPWM_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM_CNT6_TR_CTRL0	0x402002A0	Counter trigger control register 0. See TCPWM_CNT0_TR_CTRL0 for the details of bit fields.
TCPWM_CNT6_TR_CTRL1	0x402002A4	Counter trigger control register 1. See TCPWM_CNT0_TR_CTRL1 for the details of bit fields.
TCPWM_CNT6_TR_CTRL2	0x402002A8	Counter trigger control register 2. See TCPWM_CNT0_TR_CTRL2 for the details of bit fields.
TCPWM_CNT6_INTR	0x402002B0	Interrupt request register.. See TCPWM_CNT0_INTR for the details of bit fields.
TCPWM_CNT6_INTR_SET	0x402002B4	Interrupt set request register.. See TCPWM_CNT0_INTR_SET for the details of bit fields.
TCPWM_CNT6_INTR_MASK	0x402002B8	Interrupt mask register.. See TCPWM_CNT0_INTR_MASK for the details of bit fields.
TCPWM_CNT6_INTR_MASKED	0x402002BC	Interrupt masked request register. See TCPWM_CNT0_INTR_MASKED for the details of bit fields.
TCPWM_CNT7_CTRL	0x402002C0	Counter control register. See TCPWM_CNT0_CTRL for the details of bit fields.
TCPWM_CNT7_STATUS	0x402002C4	Counter status register. See TCPWM_CNT0_STATUS for the details of bit fields.
TCPWM_CNT7_COUNTER	0x402002C8	Counter count register. See TCPWM_CNT0_COUNTER for the details of bit fields.
TCPWM_CNT7_CC	0x402002CC	Counter compare/capture register. See TCPWM_CNT0_CC for the details of bit fields.
TCPWM_CNT7_CC_BUFF	0x402002D0	Counter buffered compare/capture register. See TCPWM_CNT0_CC_BUFF for the details of bit fields.
TCPWM_CNT7_PERIOD	0x402002D4	Counter period register. See TCPWM_CNT0_PERIOD for the details of bit fields.
TCPWM_CNT7_PERIOD_BUFF	0x402002D8	Counter buffered period register. See TCPWM_CNT0_PERIOD_BUFF for the details of bit fields.
TCPWM_CNT7_TR_CTRL0	0x402002E0	Counter trigger control register 0. See TCPWM_CNT0_TR_CTRL0 for the details of bit fields.
TCPWM_CNT7_TR_CTRL1	0x402002E4	Counter trigger control register 1. See TCPWM_CNT0_TR_CTRL1 for the details of bit fields.

Register	Address	Description
TCPWM_CNT7_TR_CTRL2	0x402002E8	Counter trigger control register 2. See TCPWM_CNT0_TR_CTRL2 for the details of bit fields.
TCPWM_CNT7_INTR	0x402002F0	Interrupt request register.. See TCPWM_CNT0_INTR for the details of bit fields.
TCPWM_CNT7_INTR_SET	0x402002F4	Interrupt set request register.. See TCPWM_CNT0_INTR_SET for the details of bit fields.
TCPWM_CNT7_INTR_MASK	0x402002F8	Interrupt mask register.. See TCPWM_CNT0_INTR_MASK for the details of bit fields.
TCPWM_CNT7_INTR_MASKED	0x402002FC	Interrupt masked request register. See TCPWM_CNT0_INTR_MASKED for the details of bit fields.

12.1.1 TCPWM_CTRL

TCPWM control register 0.

Address: 0x40200000

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	COUNTER_ENABLED [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	COUNTER_ENABLED	Counter enables for counters 0 up to CNT_NR-1. '0': counter disabled. '1': counter enabled. Counter static configuration information (e.g. CTRL.MODE, all TR_CTRL0, TR_CTRL1, and TR_CTRL2 register fields) should only be modified when the counter is disabled. When a counter is disabled, command and status information associated to the counter is cleared by HW, this includes: - the associated counter triggers in the CMD register are set to '0'. - the counter's interrupt cause fields in counter's INTR register. - the counter's status fields in counter's STATUS register.. - the counter's trigger outputs ("tr_overflow", "tr_underflow" and "tr_compare_match"). - the counter's line outputs ("line_out" and "line_compl_out"). Default Value: 0

12.1.2 TCPWM_CMD

TCPWM command register.

Address: 0x40200008

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S							
HW Access	RW1C							
Name	COUNTER_CAPTURE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1S							
HW Access	RW1C							
Name	COUNTER_RELOAD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW1S							
HW Access	RW1C							
Name	COUNTER_STOP [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1S							
HW Access	RW1C							
Name	COUNTER_START [31:24]							

Bits	Name	Description
31 : 24	COUNTER_START	Counters SW start trigger. For HW behavior, see COUNTER_CAPTURE field. Default Value: 0
23 : 16	COUNTER_STOP	Counters SW stop trigger. For HW behavior, see COUNTER_CAPTURE field. Default Value: 0
15 : 8	COUNTER_RELOAD	Counters SW reload trigger. For HW behavior, see COUNTER_CAPTURE field. Default Value: 0
7 : 0	COUNTER_CAPTURE	Counters SW capture trigger. When written with '1', a capture trigger is generated and the HW sets the field to '0' when the SW trigger has taken effect. It should be noted that the HW operates on the counter frequency. If the counter is disabled through CTRL.COUNTER_ENABLED, the field is immediately set to '0'. Default Value: 0

12.1.3 TCPWM_INTR_CAUSE

TCPWM Counter interrupt cause register.

Address: 0x4020000C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	COUNTER_INT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	COUNTER_INT	Counters interrupt signal active. If the counter is disabled through CTRL.COUNTER_ENABLED, the associated interrupt field is immediately set to '0'. Default Value: 0

12.1.4 TCPWM_CNT0_CTRL

Counter control register

Address: 0x40200100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [7:4]				PWM_STOP_ON_KILL	PWM_SYNC_KILL	AUTO_RELOAD_PERIOD	AUTO_RELOAD_CC

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	GENERIC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW		None	RW	RW	
HW Access	None		R		None	R	R	
Name	None [23:22]		QUADRATURE_MODE [21:20]		None	ONE_SHOT	UP_DOWN_MODE [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None					RW		
HW Access	None					R		
Name	None [31:27]					MODE [26:24]		

Bits	Name	Description
26 : 24	MODE	Counter mode. Default Value: 0 **0x0: TIMER :** Timer mode **0x2: CAPTURE :** Capture mode **0x3: QUAD :** Quadrature encoding mode

12.1.4 TCPWM_CNT0_CTRL (continued)

		0x4: PWM : Pulse width modulation (PWM) mode **0x5: PWM_DT :** PWM with deadtime insertion mode **0x6: PWM_PR :** Pseudo random pulse width modulation
21 : 20	QUADRATURE_MODE	In QUAD mode selects quadrature encoding mode (X1/X2/X4). In PWM, PWM_DT and PWM_PR modes, these two bits can be used to invert "dt_line_out" and "dt_line_compl_out". Inversion is the last step in generation of "dt_line_out" and "dt_line_compl_out"; i.e. a disabled output line "dt_line_out" has the value QUADRATURE_MODE[0] and a disabled output line "dt_line_compl_out" has the value QUADRATURE_MODE[1]. Default Value: 0 **0x0: X1 :** X1 encoding (QUAD mode) **0x1: X2 :** X2 encoding (QUAD mode) **0x2: X4 :** X4 encoding (QUAD mode) **0x1: INV_OUT :** When bit 0 is '1', QUADRATURE_MODE[0] inverts "dt_line_out" (PWM/PWM_DT modes) **0x2: INV_COMPL_OUT :** When bit 1 is '1', QUADRATURE_MODE[1] inverts "dt_line_compl_out" (PWM/PWM_DT modes)
18	ONE_SHOT	When '0', counter runs continuous. When '1', counter is turned off by hardware when a terminal count event is generated. Default Value: 0
17 : 16	UP_DOWN_MODE	Determines counter direction. Default Value: 0 **0x0: COUNT_UP :** Count up (to PERIOD). An overflow event is generated when the counter reaches PERIOD. A terminal count event is generated when the counter reaches PERIOD.

12.1.4 TCPWM_CNT0_CTRL (continued)

0x1: COUNT_DOWN :

Count down (to "0"). An underflow event is generated when the counter reaches "0". A terminal count event is generated when the counter reaches "0".

0x2: COUNT_UPDN1 :

Count up (to PERIOD), then count down (to "0"). An overflow event is generated when the counter reaches PERIOD. An underflow event is generated when the counter reaches "0". A terminal count event is generated when the counter reaches "0".

0x3: COUNT_UPDN2 :

Count up (to PERIOD), then count down (to "0"). An overflow event is generated when the counter reaches PERIOD. An underflow event is generated when the counter reaches "0". A terminal count event is generated when the counter reaches "0" AND when the counter reaches PERIOD (this counter direction can be used for PWM functionality with asymmetrical updates).

15 : 8	GENERIC	Generic 8-bit control field. In PWM_DT mode, this field is used to determine the dead time: amount of dead time cycles in the counter clock domain. In all other modes, the lower 3 bits of this field determine pre-scaling of the selected counter clock. Default Value: 0

0x0: DIVBY1 :

Divide by 1 (other-than-PWM_DT mode)

0x1: DIVBY2 :

Divide by 2 (other-than-PWM_DT mode)

0x2: DIVBY4 :

Divide by 4 (other-than-PWM_DT mode)

0x3: DIVBY8 :

Divide by 8 (other-than-PWM_DT mode)

0x4: DIVBY16 :

Divide by 16 (other-than-PWM_DT mode)

0x5: DIVBY32 :

Divide by 32 (other-than-PWM_DT mode)

0x6: DIVBY64 :

Divide by 64 (other-than-PWM_DT mode)

12.1.4 TCPWM_CNT0_CTRL (continued)

		0x7: DIVBY128 : Divide by 128 (other-than-PWM_DT mode)
3	PWM_STOP_ON_KILL	Specifies whether the counter stops on a kill events: '0': kill event does NOT stop counter. '1': kill event stops counter. This field has a function in PWM, PWM_DT and PWM_PR modes only. Default Value: 0
2	PWM_SYNC_KILL	Specifies asynchronous/synchronous kill behavior: '1': synchronous kill mode: the kill event disables the "dt_line_out" and "dt_line_compl_out" signals till the next terminal count event (synchronous kill). In synchronous kill mode, STOP_EDGE should be RISING_EDGE. '0': asynchronous kill mode: the kill event only disables the "dt_line_out" and "dt_line_compl_out" signals when present. In asynchronous kill mode, STOP_EDGE should be NO_EDGE_DET. This field has a function in PWM and PWM_DT modes only. This field is only used when PWM_STOP_ON_KILL is '0'. Default Value: 0
1	AUTO_RELOAD_PERIOD	Specifies switching of the PERIOD and buffered PERIOD values. This field has a function in PWM, PWM_DT and PWM_PR modes. '0': never switch. '1': switch on a terminal count event with and actively pending siwtch event. Default Value: 0
0	AUTO_RELOAD_CC	Specifies switching of the CC and buffered CC values. This field has a function in TIMER, PWM, PWM_DT and PWM_PR modes. Timer mode: '0': never switch. '1': switch on a compare match event. PWM, PWM_DT, PWM_PR modes: '0: never switch. '1': switch on a terminal count event with an actively pending switch event. Default Value: 0

12.1.5 TCPWM_CNT0_STATUS

Counter status register

Address: 0x40200104

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							DOWN

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	GENERIC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	RW	None						
Name	RUNNING	None [30:24]						

Bits	Name	Description
31	RUNNING	When '0', the counter is NOT running. When '1', the counter is running. Default Value: 0
15 : 8	GENERIC	Generic 8-bit counter field. In PWM_DT mode, this counter is used for dead time insertion. In all other modes, this counter is used for pre-scaling the selected counter clock. PWM_DT mode can NOT use prescaled clock functionality. Default Value: 0
0	DOWN	When '0', counter is counting up. When '1', counter is counting down. In QUAD mode, this field indicates the direction of the latest counter change: '0' when last incremented and '1' when last decremented. Default Value: 0

12.1.6 TCPWM_CNT0_COUNTER

Counter count register

Address: 0x40200108

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	COUNTER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	COUNTER [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	COUNTER	16-bit counter value. It is advised to not write to this field when the counter is running. Default Value: 0

12.1.7 TCPWM_CNT0_CC

Counter compare/capture register

Address: 0x4020010C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CC	In CAPTURE mode, captures the counter value. In other modes, compared to counter value. Default Value: 65535

12.1.8 TCPWM_CNT0_CC_BUFF

Counter buffered compare/capture register

Address: 0x40200110

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	CC [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	CC [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CC	Additional buffer for counter CC register. Default Value: 65535

12.1.9 TCPWM_CNT0_PERIOD

Counter period register

Address: 0x40200114

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	PERIOD	Period value: upper value of the counter. When the counter should count for n cycles, this field should be set to n-1. Default Value: 65535

12.1.10 TCPWM_CNT0_PERIOD_BUFF

Counter buffered period register

Address: 0x40200118

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	PERIOD	Additional buffer for counter PERIOD register. Default Value: 65535

12.1.11 TCPWM_CNT0_TR_CTRL0

Counter trigger control register 0

Address: 0x40200120

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	COUNT_SEL [7:4]				CAPTURE_SEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW				RW			
HW Access	R				R			
Name	STOP_SEL [15:12]				RELOAD_SEL [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				START_SEL [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19 : 16	START_SEL	Selects one of the 16 input triggers as a start trigger. In QUAD mode, this is the second phase (phi B). Default Value: 0
15 : 12	STOP_SEL	Selects one of the 16 input triggers as a stop trigger. In PWM, PWM_DT and PWM_PR modes, this is the kill trigger. In these modes, the kill trigger is used to either temporarily block the PWM outputs (PWM_STOP_ON_KILL is '0') or stop the functionality (PWM_STOP_ON_KILL is '1'). For the PWM and PWM_DT modes, the blocking of the output signals can be asynchronous (STOP_EDGE should be NO_EDGE_DET) in which case the blocking is as long as the trigger is '1' or synchronous (STOP_EDGE should be RISING_EDGE) in which case it extends till the next terminal count event. Default Value: 0
11 : 8	RELOAD_SEL	Selects one of the 16 input triggers as a reload trigger. In QUAD mode, this is the index or revolution pulse. In this mode, it will update the counter with the value in the TCPWM_CNTn_PERIOD register. Default Value: 0
7 : 4	COUNT_SEL	Selects one of the 16 input triggers as a count trigger. In QUAD mode, this is the first phase (phi A). Default setting selects input trigger 1, which is always '1'. Default Value: 1

12.1.11 TCPWM_CNT0_TR_CTRL0 (continued)

3 : 0	CAPTURE_SEL	Selects one of the 16 input triggers as a capture trigger. Input trigger 0 is always '0' and input trigger 1 is always '1'. Input trigger 2 is the first external trigger line (tcpwm.tr_in[0]). In the PWM, PWM_DT and PWM_PR modes this trigger is used to switch the values if the compare and period registers with their buffer counterparts. Default Value: 0

12.1.12 TCPWM_CNT0_TR_CTRL1

Counter trigger control register 1

Address: 0x40200124

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		RW		RW		RW	
HW Access	R		R		R		R	
Name	STOP_EDGE [7:6]		RELOAD_EDGE [5:4]		COUNT_EDGE [3:2]		CAPTURE_EDGE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						START_EDGE [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9 : 8	START_EDGE	A start event will start the counter; i.e. the counter will become running. Starting does NOT enable the counter. A start event will not initialize the counter whereas the reload event does. Default Value: 3 **0x0: RISING_EDGE :** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE :** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES :** Rising AND falling edge. Any odd amount of edges generates an event.

12.1.12 TCPWM_CNT0_TR_CTRL1 (continued)

		0x3: NO_EDGE_DET : No edge detection, use trigger as is.
7 : 6	STOP_EDGE	A stop event, will stop the counter; i.e. it will no longer be running. Stopping will NOT disable the counter. Default Value: 3 **0x0: RISING_EDGE :** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE :** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES :** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET :** No edge detection, use trigger as is.
5 : 4	RELOAD_EDGE	A reload event will initialize the counter. When counting up, the counter is initialized to "0". When counting down, the counter is initialized with PERIOD. Default Value: 3 **0x0: RISING_EDGE :** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE :** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES :** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET :** No edge detection, use trigger as is.
3 : 2	COUNT_EDGE	A counter event will increase or decrease the counter by '1'. Default Value: 3 **0x0: RISING_EDGE :** Rising edge. Any rising edge generates an event.

12.1.12 TCPWM_CNT0_TR_CTRL1 (continued)

		0x1: FALLING_EDGE : Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES :** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET :** No edge detection, use trigger as is.
1 : 0	CAPTURE_EDGE	A capture event will copy the counter value into the CC register. Default Value: 3 **0x0: RISING_EDGE :** Rising edge. Any rising edge generates an event. **0x1: FALLING_EDGE :** Falling edge. Any falling edge generates an event. **0x2: BOTH_EDGES :** Rising AND falling edge. Any odd amount of edges generates an event. **0x3: NO_EDGE_DET :** No edge detection, use trigger as is.

12.1.13 TCPWM_CNT0_TR_CTRL2

Counter trigger control register 2

Address: 0x40200128

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW		RW		RW	
HW Access	None		R		R		R	
Name	None [7:6]		UNDERFLOW_MODE [5:4]		OVERFLOW_MODE [3:2]		CC_MATCH_MODE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 4	UNDERFLOW_MODE	Determines the effect of a counter underflow event (COUNTER reaches "0") on the "line_out" output signals. Default Value: 3 **0x0: SET :** Set to '1' **0x1: CLEAR :** Set to '0' **0x2: INVERT :** Invert

12.1.13 TCPWM_CNT0_TR_CTRL2 (continued)

		0x3: NO_CHANGE : No Change
3 : 2	OVERFLOW_MODE	Determines the effect of a counter overflow event (COUNTER reaches PERIOD) on the "line_out" output signals. Default Value: 3 **0x0: SET :** Set to '1' **0x1: CLEAR :** Set to '0' **0x2: INVERT :** Invert **0x3: NO_CHANGE :** No Change
1 : 0	CC_MATCH_MODE	Determines the effect of a compare match event (COUNTER equals CC register) on the "line_out" output signals. Note that INVERT is especially useful for center aligned pulse width modulation. To generate a duty cycle of 0%, the counter CC register should be set to "0". For a 100% duty cycle, the counter CC register should be set to larger than the counter PERIOD register. Default Value: 3 **0x0: SET :** Set to '1' **0x1: CLEAR :** Set to '0' **0x2: INVERT :** Invert **0x3: NO_CHANGE :** No Change

12.1.14 TCPWM_CNT0_INTR

Interrupt request register.

Address: 0x40200130

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1C	RW1C
HW Access	None						RW1S	RW1S
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Counter matches CC register event. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
0	TC	Terminal count event. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0

12.1.15 TCPWM_CNT0_INTR_SET

Interrupt set request register.

Address: 0x40200134

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1S	RW1S
HW Access	None						A	A
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	TC	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

12.1.16 TCPWM_CNT0_INTR_MASK

Interrupt mask register.

Address: 0x40200138

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	TC	Mask bit for corresponding bit in interrupt request register. Default Value: 0

12.1.17 TCPWM_CNT0_INTR_MASKED

Interrupt masked request register

Address: 0x4020013C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						W	W
Name	None [7:2]						CC_MATCH	TC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CC_MATCH	Logical and of corresponding request and mask bits. Default Value: 0
0	TC	Logical and of corresponding request and mask bits. Default Value: 0

13 Watch Crystal Oscillator (WCO) Registers

This section discusses the WCO registers. It lists all the registers in mapping tables, in address order.

13.1 Register Details

Register	Address	Description
WCO_CONFIG	0x40220000	WCO Configuration Register
WCO_STATUS	0x40220004	WCO Status Register
WCO_DPLL	0x40220008	WCO DPLL Register
WCO_WDT_CTRLOW	0x40220200	Watchdog Counters 0/1
WCO_WDT_CTRHIGH	0x40220204	Watchdog Counter 2
WCO_WDT_MATCH	0x40220208	Watchdog counter match values
WCO_WDT_CONFIG	0x4022020C	Watchdog Counters Configuration
WCO_WDT_CONTROL	0x40220210	Watchdog Counters Control
WCO_WDT_CLKEN	0x40220214	Watchdog Counters Clock Enable
WCO_TRIM	0x40220F00	WCO Trim Register

13.1.1 WCO_CONFIG

WCO Configuration Register

Address: 0x40220000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [7:3]					EXT_IN-PUT_EN	LPM_AUTO	LPM_EN

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	ENBUS [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None					
HW Access	R	R	None					
Name	IP_ENABLE	DPLL_EN-ABLE	None [29:24]					

Bits	Name	Description
31	IP_ENABLE	Master enable for IP - disables both WCO and DPLL Default Value: 0
30	DPLL_ENABLE	Enable DPLL operation. The Oscillator is specified to be stable after 500 ms thus the DPLL should be asserted no sooner than that after IP_ENABLE is set. Default Value: 0
23 : 16	ENBUS	Test Mode Control bits enbus[7] - N/A enbus[6] - 1=enable both primary Beta Multipliers enbus[5] - N/A enbus[4] - N/A enbus[3] - Load Resistor Control enbus[2] - Load Resistor Control enbus[1] - Load Resistor Control enbus[0] - Load Resistor Control Default Value: 71
2	EXT_INPUT_EN	Disables the load resistor and allows external clock input for XTAL pin Default Value: 0

13.1.1 WCO_CONFIG (continued)

1	LPM_AUTO	Automatically control low power mode (only relevant when LPM_EN=0): 0: Do not enter low power mode (LPM) in DeepSleep 1: Enter low power mode (LPM) in DeepSleep. The logic monitors !act_power_en to determine the device has entered DeepSleep. Default Value: 1
0	LPM_EN	Force block into Low Power Mode: 0: Do not force low power mode (LPM) on 1: Force low power mode (LPM) on Default Value: 0

13.1.2 WCO_STATUS

WCO Status Register

Address: 0x40220004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							OUT_BLNK_A

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	OUT_BLNK_A	Indicates that output has transitioned - This bit is intended for Test Mode Only and is not a reliable indicator. Default Value: 0

13.1.3 WCO_DPLL

WCO DPLL Register

Address: 0x40220008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DPLL_MULT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW		
HW Access	None					R		
Name	None [15:11]					DPLL_MULT [10:8]		

Bits	23	22	21	20	19	18	17	16
SW Access	RW		RW			RW		
HW Access	R		R			R		
Name	DPLL_LF_LIMIT [23:22]		DPLL_LF_PGAIN [21:19]			DPLL_LF_IGAIN [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	None		RW					
HW Access	None		R					
Name	None [31:30]		DPLL_LF_LIMIT [29:24]					

Bits	Name	Description
29 : 22	DPLL_LF_LIMIT	Maximum IMO offset allowed (used to prevent DPLL dynamics from selecting an IMO frequency that the logic cannot support) Default Value: 255
21 : 19	DPLL_LF_PGAIN	DPLL Loop Filter Proportionial Gain Setting 0x0 - 0.0625 0x1 - 0.125 0x2 - 0.25 0x3 - 0.5 0x4 - 1.0 0x5 - 2.0 0x6 - 4.0 0x7 - 8.0 Default Value: 0

13.1.3 WCO_DPLL (continued)

18 : 16	DPLL_LF_IGAIN	DPLL Loop Filter Integral Gain Setting 0x0 - 0.0625 0x1 - 0.125 0x2 - 0.25 0x3 - 0.5 0x4 - 1.0 0x5 - 2.0 0x6 - 4.0 0x7 - 8.0 Default Value: 0
10 : 0	DPLL_MULT	Multiplier to determine IMO frequency in multiples of the WCO frequency Fimo = (DPLL_MULT + 1) * Fwco Default Value: 0

13.1.4 WCO_WDT_CTRLOW

Watchdog Counters 0/1

Address: 0x40220200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	WDT_CTR0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	WDT_CTR0 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	WDT_CTR1 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	WDT_CTR1 [31:24]							

Bits	Name	Description
31 : 16	WDT_CTR1	Current value of WDT Counter 1 Default Value: 0
15 : 0	WDT_CTR0	Current value of WDT Counter 0 Default Value: 0

13.1.5 WCO_WDT_CTRHIGH

Watchdog Counter 2

Address: 0x40220204

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	WDT_CTR2 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	WDT_CTR2 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	WDT_CTR2 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	WDT_CTR2 [31:24]							

Bits	Name	Description
31 : 0	WDT_CTR2	Current value of WDT Counter 2 Default Value: 0

13.1.6 WCO_WDT_MATCH

Watchdog counter match values

Address: 0x40220208

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	WDT_MATCH0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	WDT_MATCH0 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	WDT_MATCH1 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	WDT_MATCH1 [31:24]							

Bits	Name	Description
31 : 16	WDT_MATCH1	Match value for Watchdog Counter 1 Default Value: 0
15 : 0	WDT_MATCH0	Match value for Watchdog Counter 0 Default Value: 0

13.1.7 WCO_WDT_CONFIG

Watchdog Counters Configuration

Address: 0x4022020C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	
HW Access	None				R	R	R	
Name	None [7:4]				WDT_CAS-CADE0_1	WDT_-CLEAR0	WDT_MODE0 [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	RW	RW	
HW Access	None				R	R	R	
Name	None [15:12]				WDT_CAS-CADE1_2	WDT_-CLEAR1	WDT_MODE1 [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							WDT_-MODE2

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None	RW				
HW Access	R		None	R				
Name	LFCLK_SEL [31:30]		None	WDT_BITS2 [28:24]				

Bits	Name	Description
31 : 30	LFCLK_SEL	Select source for LFCLK: 0: ILO - Internal R/C Oscillator 1: WCO - Internal Crystal Oscillator 2-3: Reserved - do not use Note that not all products support all clock sources. Selecting a clock source that is not supported will result in undefined behavior. To safely change LFCLK_SEL wait for WDT_CTRLOW/WDT_CTRHIGH to change then chaneg the setting immediately. Default Value: 0
28 : 24	WDT_BITS2	Bit to observe for WDT_INT2: 0: Assert when bit0 of WDT_CTR2 toggles (one int every tick) .. 31: Assert when bit31 of WDT_CTR2 toggles (one int every 2^31 ticks) Default Value: 0
16	WDT_MODE2	Watchdog Counter 2 Mode. Default Value: 0

13.1.7 WCO_WDT_CONFIG (continued)

		0x0: NOTHING : Free running counter with no interrupt requests **0x1: INT :** Free running counter with interrupt request when a specified bit in CTR2 toggles (see WDT_BITS2)
11	WDT_CASCADE1_2	Cascade Watchdog Counters 1,2. Counter 2 increments the cycle after WDT_CTR1=WDT_-MATCH1. It is allowed to cascade all three WDT counters. 0: Independent counters 1: Cascaded counters. When cascading all three counters, WDT_CLEAR1 must be 1 Default Value: 0
10	WDT_CLEAR1	Clear Watchdog Counter when WDT_CTR1=WDT_MATCH1. In other words WDT_CTR1 divides LFCLK by (WDT_MATCH1+1). 0: Free running counter 1: Clear on match Default Value: 0
9 : 8	WDT_MODE1	Watchdog Counter Action on Match (WDT_CTR1=WDT_MATCH1). Default Value: 0 **0x0: NOTHING :** Do nothing **0x1: INT :** Assert WDT_INTx **0x2: RESET :** Assert WDT Reset - Not Supported - here for backwards compatibility **0x3: INT_THEN_RESET :** Assert WDT_INTx, assert WDT Reset after 3rd unhandled interrupt - Not supported - here for backwards compatibility.
3	WDT_CASCADE0_1	Cascade Watchdog Counters 0,1. Counter 1 increments the cycle after WDT_CTR0=WDT_-MATCH0. 0: Independent counters 1: Cascaded counters Default Value: 0
2	WDT_CLEAR0	Clear Watchdog Counter when WDT_CTR0=WDT_MATCH0. In other words WDT_CTR0 divides LFCLK by (WDT_MATCH0+1). 0: Free running counter 1: Clear on match Default Value: 0
1 : 0	WDT_MODE0	Watchdog Counter Action on Match (WDT_CTR0=WDT_MATCH0). Default Value: 0

13.1.7 WCO_WDT_CONFIG (continued)

0x0: NOTHING :

Do nothing

0x1: INT :

Assert WDT_INTx

0x2: RESET :

Assert WDT Reset - Not Supported - here for backwards compatibility

0x3: INT_THEN_RESET :

Assert WDT_INTx, assert WDT Reset after 3rd unhandled interrupt. Not supported - here for Backwards compatibility.

13.1.8 WCO_WDT_CONTROL

Watchdog Counters Control

Address: 0x40220210

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1S	RW1C	R	RW
HW Access	None				RW0C	A	RW	R
Name	None [7:4]				WDT_RESET0	WDT_INT0	WDT_ENABLED0	WDT_ENABLE0

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW1S	RW1C	R	RW
HW Access	None				RW0C	A	RW	R
Name	None [15:12]				WDT_RESET1	WDT_INT1	WDT_ENABLED1	WDT_ENABLE1

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW1S	RW1C	R	RW
HW Access	None				RW0C	A	RW	R
Name	None [23:20]				WDT_RESET2	WDT_INT2	WDT_ENABLED2	WDT_ENABLE2

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
19	WDT_RESET2	Resets counter 2 back to 0000_0000. Hardware will reset this bit after counter was reset. This will take several LFCLK cycles to take effect. Wait until the reset completes before enabling the WDT. Default Value: 0
18	WDT_INT2	WDT Interrupt Request. This bit is set by hardware as configured by this registers. This bit must be cleared by firmware. After WDT_CTR2, WDT_CONTROL must be read for the hardware to internally remove the clear flag. Failure to do this may result in missing the next interrupt. Default Value: 0
17	WDT_ENABLED2	Indicates actual state of counter. May lag WDT_ENABLE2 by up to 3 LFCLK cycles. After changing WDT_ENABLE2, do not enter DEEPSLEEP mode until this field acknowledges the change. Default Value: 0

13.1.8 WCO_WDT_CONTROL (continued)

16	WDT_ENABLE2	Enable Counter 2 0: Counter is disabled (not clocked) 1: Counter is enabled (counting up) Note: This field takes considerable time (up to 3 LFCLK cycles) to take effect. It must not be changed more than once in that period. Default Value: 0
11	WDT_RESET1	Resets counter 1 back to 0000. Hardware will reset this bit after counter was reset. This will take several LFCLK cycles to take effect. Wait until the reset completes before enabling the WDT. Default Value: 0
10	WDT_INT1	WDT Interrupt Request. This bit is set by hardware as configured by this registers. This bit must be cleared by firmware. After WDT_CTR1, WDT_CONTROL must be read for the hardware to internally remove the clear flag. Failure to do this may result in missing the next interrupt. Default Value: 0
9	WDT_ENABLED1	Indicates actual state of counter. May lag WDT_ENABLE1 by up to 3 LFCLK cycles. After changing WDT_ENABLE1, do not enter DEEPSLEEP mode until this field acknowledges the change. Default Value: 0
8	WDT_ENABLE1	Enable Counter 1 0: Counter is disabled (not clocked) 1: Counter is enabled (counting up) Note: This field takes considerable time (up to 3 LFCLK cycles) to take effect. It must not be changed more than once in that period. Default Value: 0
3	WDT_RESET0	Resets counter 0 back to 0000. Hardware will reset this bit after counter was reset. This will take several LFCLK cycles to take effect. Wait until the reset completes before enabling the WDT. Default Value: 0
2	WDT_INT0	WDT Interrupt Request. This bit is set by hardware as configured by this registers. This bit must be cleared by firmware. Clearing this bit also prevents Reset from happening when WDT_MODEx=3. After W1C, WDT_CONTROL must be read for the hardware to internally remove the clear flag. Failure to do this may result in missing the next interrupt. Default Value: 0
1	WDT_ENABLED0	Indicates actual state of counter. May lag WDT_ENABLE0 by up to 3 LFCLK cycles. After changing WDT_ENABLE0, do not enter DEEPSLEEP mode until this field acknowledges the change. Default Value: 0
0	WDT_ENABLE0	Enable Counter 0 0: Counter is disabled (not clocked) 1: Counter is enabled (counting up) Note: This field takes considerable time (up to 3 LFCLK cycles) to take effect. It must not be changed more than once in that period. Default Value: 0

13.1.9 WCO_WDT_CLKEN

Watchdog Counters Clock Enable

Address: 0x40220214

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						CLK_ILO_EN_-FOR_WDT	CLK_W-CO_EN_-FOR_WDT

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	CLK_ILO_EN_FOR_WDT	Enables the ILO clock for use by the WDT logic. Wait at least 4 ILO clock cycles for a change to take effect. Must be 0 when switching WDT_CONFIG.LFCLK_SEL. Should be 0 if CLK_W-CO_EN_FOR_WDT=1. Default Value: 0
0	CLK_WCO_EN_-FOR_WDT	Enables the WCO clock for use by the WDT logic. Wait at least 4 WCO clock cycles for a change to take effect. Must be 0 when switching WDT_CONFIG.LFCLK_SEL. Should be 0 if CLK_ILO_EN_FOR_WDT=1 Default Value: 0

13.1.10 WCO_TRIM

WCO Trim Register

Address: 0x40220F00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW		None	RW		
HW Access	None		R		None	R		
Name	None [7:6]		LPM_GM [5:4]		None	XGM [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 4	LPM_GM	GM setting for LPM (bandwidth = DC/ms) - Used when WCO.LPM_AUTO=0 or when LPM_AUTO=1 and not in DeepSleep mode. Default Value: 1
2 : 0	XGM	Amplifier GM setting - Used when WCO.LPM_AUTO=0 or when LPM_AUTO=1 and not in DeepSleep mode. 0x0 - 3370 nA 0x1 - 2620 nA 0x2 - 2250 nA 0x3 - 1500 nA 0x4 - 1870 nA 0x5 - 1120 nA 0x6 - 750 nA 0x7 - 0 nA Default Value: 1

14 Serial Communication Block (SCB) Registers

This section discusses the SCB registers. It lists all the registers in mapping tables, in address order.

14.1 Register Details

Register	Address	Description
SCB0_CTRL	0x40240000	Generic control
SCB0_STATUS	0x40240004	Generic status
SCB0_SPI_CTRL	0x40240020	SPI control
SCB0_SPI_STATUS	0x40240024	SPI status
SCB0_SPI_TX_CTRL	0x40240028	SPI transmitter control
SCB0_SPI_RX_CTRL	0x4024002C	SPI receiver control
SCB0_UART_CTRL	0x40240040	UART control
SCB0_UART_TX_CTRL	0x40240044	UART transmitter control
SCB0_UART_RX_CTRL	0x40240048	UART receiver control
SCB0_UART_RX_STATUS	0x4024004C	UART receiver status
SCB0_UART_FLOW_CTRL	0x40240050	UART flow control
SCB0_I2C_CTRL	0x40240060	I2C control
SCB0_I2C_STATUS	0x40240064	I2C status
SCB0_I2C_M_CMD	0x40240068	I2C master command
SCB0_I2C_S_CMD	0x4024006C	I2C slave command
SCB0_I2C_CFG	0x40240070	I2C configuration
SCB0_I2C_STRETCH_CTRL	0x40240074	I2C stretch control
SCB0_I2C_STRETCH_STATUS	0x40240078	I2C stretch status
SCB0_I2C_CTRL_HS	0x40240080	I2C control for High-Speed mode
SCB0_TX_CTRL	0x40240200	Transmitter control
SCB0_TX_FIFO_CTRL	0x40240204	Transmitter FIFO control
SCB0_TX_FIFO_STATUS	0x40240208	Transmitter FIFO status
SCB0_TX_FIFO_WR	0x40240240	Transmitter FIFO write
SCB0_RX_CTRL	0x40240300	Receiver control
SCB0_RX_FIFO_CTRL	0x40240304	Receiver FIFO control
SCB0_RX_FIFO_STATUS	0x40240308	Receiver FIFO status
SCB0_RX_MATCH	0x40240310	Slave address and mask

Register	Address	Description
SCB0_RX_FIFO_RD	0x40240340	Receiver FIFO read
SCB0_RX_FIFO_RD	0x40240344	Receiver FIFO read silent
SCB0_EZ_DATA0	0x40240400	Memory buffer
SCB0_EZ_DATA1	0x40240404	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB0_EZ_DATA2	0x40240408	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB0_EZ_DATA3	0x4024040C	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB0_EZ_DATA4	0x40240410	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB0_EZ_DATA5	0x40240414	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB0_EZ_DATA6	0x40240418	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB0_EZ_DATA7	0x4024041C	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB0_EZ_DATA8	0x40240420	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB0_EZ_DATA9	0x40240424	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB0_EZ_DATA10	0x40240428	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB0_EZ_DATA11	0x4024042C	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB0_EZ_DATA12	0x40240430	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB0_EZ_DATA13	0x40240434	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB0_EZ_DATA14	0x40240438	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB0_EZ_DATA15	0x4024043C	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB0_EZ_DATA16	0x40240440	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB0_EZ_DATA17	0x40240444	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB0_EZ_DATA18	0x40240448	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB0_EZ_DATA19	0x4024044C	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB0_EZ_DATA20	0x40240450	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB0_EZ_DATA21	0x40240454	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB0_EZ_DATA22	0x40240458	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB0_EZ_DATA23	0x4024045C	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB0_EZ_DATA24	0x40240460	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB0_EZ_DATA25	0x40240464	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB0_EZ_DATA26	0x40240468	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB0_EZ_DATA27	0x4024046C	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB0_EZ_DATA28	0x40240470	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB0_EZ_DATA29	0x40240474	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB0_EZ_DATA30	0x40240478	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB0_EZ_DATA31	0x4024047C	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB0_INTR_CAUSE	0x40240E00	Active clocked interrupt signal
SCB0_INTR_I2C_EC	0x40240E80	Externally clocked I2C interrupt request
SCB0_INTR_I2C_EC_MASK	0x40240E88	Externally clocked I2C interrupt mask
SCB0_INTR_I2C_EC_MASKED	0x40240E8C	Externally clocked I2C interrupt masked
SCB0_INTR_SPI_EC	0x40240EC0	Externally clocked SPI interrupt request
SCB0_INTR_SPI_EC_MASK	0x40240EC8	Externally clocked SPI interrupt mask
SCB0_INTR_SPI_EC_MASKED	0x40240ECC	Externally clocked SPI interrupt masked
SCB0_INTR_M	0x40240F00	Master interrupt request

Register	Address	Description
SCB0_INTR_M_SET	0x40240F04	Master interrupt set request
SCB0_INTR_M_MASK	0x40240F08	Master interrupt mask
SCB0_INTR_M_MASKED	0x40240F0C	Master interrupt masked request
SCB0_INTR_S	0x40240F40	Slave interrupt request
SCB0_INTR_S_SET	0x40240F44	Slave interrupt set request
SCB0_INTR_S_MASK	0x40240F48	Slave interrupt mask
SCB0_INTR_S_MASKED	0x40240F4C	Slave interrupt masked request
SCB0_INTR_TX	0x40240F80	Transmitter interrupt request
SCB0_INTR_TX_SET	0x40240F84	Transmitter interrupt set request
SCB0_INTR_TX_MASK	0x40240F88	Transmitter interrupt mask
SCB0_INTR_TX_MASKED	0x40240F8C	Transmitter interrupt masked request
SCB0_INTR_RX	0x40240FC0	Receiver interrupt request
SCB0_INTR_RX_SET	0x40240FC4	Receiver interrupt set request
SCB0_INTR_RX_MASK	0x40240FC8	Receiver interrupt mask
SCB0_INTR_RX_MASKED	0x40240FCC	Receiver interrupt masked request
SCB1_CTRL	0x40250000	Generic control. See SCB0_CTRL for the details of bit fields.
SCB1_STATUS	0x40250004	Generic status. See SCB0_STATUS for the details of bit fields.
SCB1_SPI_CTRL	0x40250020	SPI control. See SCB0_SPI_CTRL for the details of bit fields.
SCB1_SPI_STATUS	0x40250024	SPI status. See SCB0_SPI_STATUS for the details of bit fields.
SCB1_SPI_TX_CTRL	0x40250028	SPI transmitter control. See SCB0_SPI_TX_CTRL for the details of bit fields.
SCB1_SPI_RX_CTRL	0x4025002C	SPI receiver control. See SCB0_SPI_RX_CTRL for the details of bit fields.
SCB1_UART_CTRL	0x40250040	UART control. See SCB0_UART_CTRL for the details of bit fields.
SCB1_UART_TX_CTRL	0x40250044	UART transmitter control. See SCB0_UART_TX_CTRL for the details of bit fields.
SCB1_UART_RX_CTRL	0x40250048	UART receiver control. See SCB0_UART_RX_CTRL for the details of bit fields.
SCB1_UART_RX_STATUS	0x4025004C	UART receiver status. See SCB0_UART_RX_STATUS for the details of bit fields.
SCB1_UART_FLOW_CTRL	0x40250050	UART flow control. See SCB0_UART_FLOW_CTRL for the details of bit fields.
SCB1_I2C_CTRL	0x40250060	I2C control. See SCB0_I2C_CTRL for the details of bit fields.
SCB1_I2C_STATUS	0x40250064	I2C status
SCB1_I2C_M_CMD	0x40250068	I2C master command. See SCB0_I2C_M_CMD for the details of bit fields.
SCB1_I2C_S_CMD	0x4025006C	I2C slave command. See SCB0_I2C_S_CMD for the details of bit fields.
SCB1_I2C_CFG	0x40250070	I2C configuration. See SCB0_I2C_CFG for the details of bit fields.
SCB1_I2C_STRETCH_CTRL	0x40250074	I2C stretch control. See SCB0_I2C_STRETCH_CTRL for the details of bit fields.
SCB1_I2C_STRETCH_STATUS	0x40250078	I2C stretch status. See SCB0_I2C_STRETCH_STATUS for the details of bit fields.
SCB1_TX_CTRL	0x40250200	Transmitter control. See SCB0_TX_CTRL for the details of bit fields.
SCB1_TX_FIFO_CTRL	0x40250204	Transmitter FIFO control. See SCB0_TX_FIFO_CTRL for the details of bit fields.
SCB1_TX_FIFO_STATUS	0x40250208	Transmitter FIFO status. See SCB0_TX_FIFO_STATUS for the details of bit fields.
SCB1_TX_FIFO_WR	0x40250240	Transmitter FIFO write. See SCB0_TX_FIFO_WR for the details of bit fields.
SCB1_RX_CTRL	0x40250300	Receiver control. See SCB0_RX_CTRL for the details of bit fields.
SCB1_RX_FIFO_CTRL	0x40250304	Receiver FIFO control. See SCB0_RX_FIFO_CTRL for the details of bit fields.
SCB1_RX_FIFO_STATUS	0x40250308	Receiver FIFO status. See SCB0_RX_FIFO_STATUS for the details of bit fields.
SCB1_RX_MATCH	0x40250310	Slave address and mask. See SCB0_RX_MATCH for the details of bit fields.
SCB1_RX_FIFO_RD	0x40250340	Receiver FIFO read. See SCB0_RX_FIFO_RD for the details of bit fields.

Register	Address	Description
SCB1_RX_FIFO_RD_SILENT	0x40250344	Receiver FIFO read silent. See SCB0_RX_FIFO_RD_SILENT for the details of bit fields.
SCB1_EZ_DATA0	0x40250400	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB1_EZ_DATA1	0x40250404	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB1_EZ_DATA2	0x40250408	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB1_EZ_DATA3	0x4025040C	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB1_EZ_DATA4	0x40250410	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB1_EZ_DATA5	0x40250414	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB1_EZ_DATA6	0x40250418	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB1_EZ_DATA7	0x4025041C	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB1_EZ_DATA8	0x40250420	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB1_EZ_DATA9	0x40250424	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB1_EZ_DATA10	0x40250428	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB1_EZ_DATA11	0x4025042C	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB1_EZ_DATA12	0x40250430	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB1_EZ_DATA13	0x40250434	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB1_EZ_DATA14	0x40250438	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB1_EZ_DATA15	0x4025043C	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB1_EZ_DATA16	0x40250440	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB1_EZ_DATA17	0x40250444	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB1_EZ_DATA18	0x40250448	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB1_EZ_DATA19	0x4025044C	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB1_EZ_DATA20	0x40250450	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB1_EZ_DATA21	0x40250454	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB1_EZ_DATA22	0x40250458	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB1_EZ_DATA23	0x4025045C	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB1_EZ_DATA24	0x40250460	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB1_EZ_DATA25	0x40250464	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB1_EZ_DATA26	0x40250468	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB1_EZ_DATA27	0x4025046C	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB1_EZ_DATA28	0x40250470	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB1_EZ_DATA29	0x40250474	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB1_EZ_DATA30	0x40250478	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB1_EZ_DATA31	0x4025047C	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB1_INTR_CAUSE	0x40250E00	Active clocked interrupt signal. See SCB0_INTR_CAUSE for the details of bit fields.
SCB1_INTR_I2C_EC	0x40250E80	Externally clocked I2C interrupt request. See SCB0_INTR_I2C_EC for the details of bit fields.
SCB1_INTR_I2C_EC_MASK	0x40250E88	Externally clocked I2C interrupt mask. See SCB0_INTR_I2C_EC_MASK for the details of bit fields.
SCB1_INTR_I2C_EC_MASKED	0x40250E8C	Externally clocked I2C interrupt masked. See SCB0_INTR_I2C_EC_MASKED for the details of bit fields.
SCB1_INTR_SPI_EC	0x40250EC0	Externally clocked SPI interrupt request. See SCB0_INTR_SPI_EC for the details of bit fields.
SCB1_INTR_SPI_EC_MASK	0x40250EC8	Externally clocked SPI interrupt mask. See SCB0_INTR_SPI_EC_MASK for the details of bit fields.
SCB1_INTR_SPI_EC_MASKED	0x40250ECC	Externally clocked SPI interrupt masked. See SCB0_INTR_SPI_EC_MASKED for the details of bit fields.
SCB1_INTR_M	0x40250F00	Master interrupt request. See SCB0_INTR_M for the details of bit fields.

Register	Address	Description
SCB1_INTR_M_SET	0x40250F04	Master interrupt set request. See SCB0_INTR_M_SET for the details of bit fields.
SCB1_INTR_M_MASK	0x40250F08	Master interrupt mask. See SCB0_INTR_M_MASK for the details of bit fields.
SCB1_INTR_M_MASKED	0x40250F0C	Master interrupt masked request. See SCB0_INTR_M_MASKED for the details of bit fields.
SCB1_INTR_S	0x40250F40	Slave interrupt request. See SCB0_INTR_S for the details of bit fields.
SCB1_INTR_S_SET	0x40250F44	Slave interrupt set request. See SCB0_INTR_S_SET for the details of bit fields.
SCB1_INTR_S_MASK	0x40250F48	Slave interrupt mask. See SCB0_INTR_S_MASK for the details of bit fields.
SCB1_INTR_S_MASKED	0x40250F4C	Slave interrupt masked request. See SCB0_INTR_S_MASKED for the details of bit fields.
SCB1_INTR_TX	0x40250F80	Transmitter interrupt request. See SCB0_INTR_TX for the details of bit fields.
SCB1_INTR_TX_SET	0x40250F84	Transmitter interrupt set request. See SCB0_INTR_TX_SET for the details of bit fields.
SCB1_INTR_TX_MASK	0x40250F88	Transmitter interrupt mask. See SCB0_INTR_TX_MASK for the details of bit fields.
SCB1_INTR_TX_MASKED	0x40250F8C	Transmitter interrupt masked request. See SCB0_INTR_TX_MASKED for the details of bit fields.
SCB1_INTR_RX	0x40250FC0	Receiver interrupt request. See SCB0_INTR_RX for the details of bit fields.
SCB1_INTR_RX_SET	0x40250FC4	Receiver interrupt set request. See SCB0_INTR_RX_SET for the details of bit fields.
SCB1_INTR_RX_MASK	0x40250FC8	Receiver interrupt mask. See SCB0_INTR_RX_MASKfor the details of bit fields.
SCB1_INTR_RX_MASKED	0x40250FCC	Receiver interrupt masked request. See SCB0_INTR_RX_MASKED for the details of bit fields.
SCB2_CTRL	0x40260000	Generic control. See SCB0_CTRL for the details of bit fields.
SCB2_STATUS	0x40260004	Generic status. See SCB0_STATUS for the details of bit fields.
SCB2_SPI_CTRL	0x40260020	SPI control. See SCB0_SPI_CTRL for the details of bit fields.
SCB2_SPI_STATUS	0x40260024	SPI status. See SCB0_SPI_STATUS for the details of bit fields.
SCB2_SPI_TX_CTRL	0x40260028	SPI transmitter control. See SCB0_SPI_TX_CTRL for the details of bit fields.
SCB2_SPI_RX_CTRL	0x4026002C	SPI receiver control. See SCB0_SPI_RX_CTRL for the details of bit fields.
SCB2_UART_CTRL	0x40260040	UART control. See SCB0_UART_CTRL for the details of bit fields.
SCB2_UART_TX_CTRL	0x40260044	UART transmitter control. See SCB0_UART_TX_CTRL for the details of bit fields.
SCB2_UART_RX_CTRL	0x40260048	UART receiver control. See SCB0_UART_RX_CTRL for the details of bit fields.
SCB2_UART_RX_STATUS	0x4026004C	UART receiver status. See SCB0_UART_RX_STATUS for the details of bit fields.
SCB2_UART_FLOW_CTRL	0x40260050	UART flow control. See SCB0_UART_FLOW_CTRL for the details of bit fields.
SCB2_I2C_CTRL	0x40260060	I2C control. See SCB0_I2C_CTRL for the details of bit fields.
SCB2_I2C_STATUS	0x40260064	I2C status. See SCB1_I2C_STATUS for the details of bit fields.
SCB2_I2C_M_CMD	0x40260068	I2C master command. See SCB0_I2C_M_CMD for the details of bit fields.
SCB2_I2C_S_CMD	0x4026006C	I2C slave command. See SCB0_I2C_S_CMD for the details of bit fields.
SCB2_I2C_CFG	0x40260070	I2C configuration. See SCB0_I2C_CFG for the details of bit fields.
SCB2_I2C_STRETCH_CTRL	0x40260074	I2C stretch control. See SCB0_I2C_STRETCH_CTRL for the details of bit fields.
SCB2_I2C_STRETCH_STATUS	0x40260078	I2C stretch status. See SCB0_I2C_STRETCH_STATUS for the details of bit fields.
SCB2_TX_CTRL	0x40260200	Transmitter control. See SCB0_TX_CTRL for the details of bit fields.
SCB2_TX_FIFO_CTRL	0x40260204	Transmitter FIFO control. See SCB0_TX_FIFO_CTRL for the details of bit fields.
SCB2_TX_FIFO_STATUS	0x40260208	Transmitter FIFO status. See SCB0_TX_FIFO_STATUS for the details of bit fields.
SCB2_TX_FIFO_WR	0x40260240	Transmitter FIFO write. See SCB0_TX_FIFO_WR for the details of bit fields.
SCB2_RX_CTRL	0x40260300	Receiver control. See SCB0_RX_CTRL for the details of bit fields.
SCB2_RX_FIFO_CTRL	0x40260304	Receiver FIFO control. See SCB0_RX_FIFO_CTRL for the details of bit fields.
SCB2_RX_FIFO_STATUS	0x40260308	Receiver FIFO status. See SCB0_RX_FIFO_STATUS for the details of bit fields.
SCB2_RX_MATCH	0x40260310	Slave address and mask. See SCB0_RX_MATCH for the details of bit fields.
SCB2_RX_FIFO_RD	0x40260340	Receiver FIFO read. See SCB0_RX_FIFO_RD for the details of bit fields.

Register	Address	Description
SCB2_RX_FIFO_RD_SILENT	0x40260344	Receiver FIFO read silent. See SCB0_RX_FIFO_RD_SILENT for the details of bit fields.
SCB2_EZ_DATA0	0x40260400	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB2_EZ_DATA1	0x40260404	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB2_EZ_DATA2	0x40260408	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB2_EZ_DATA3	0x4026040C	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB2_EZ_DATA4	0x40260410	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB2_EZ_DATA5	0x40260414	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB2_EZ_DATA6	0x40260418	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB2_EZ_DATA7	0x4026041C	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB2_EZ_DATA8	0x40260420	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB2_EZ_DATA9	0x40260424	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB2_EZ_DATA10	0x40260428	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB2_EZ_DATA11	0x4026042C	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB2_EZ_DATA12	0x40260430	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB2_EZ_DATA13	0x40260434	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB2_EZ_DATA14	0x40260438	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB2_EZ_DATA15	0x4026043C	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB2_EZ_DATA16	0x40260440	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB2_EZ_DATA17	0x40260444	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB2_EZ_DATA18	0x40260448	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB2_EZ_DATA19	0x4026044C	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB2_EZ_DATA20	0x40260450	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB2_EZ_DATA21	0x40260454	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB2_EZ_DATA22	0x40260458	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB2_EZ_DATA23	0x4026045C	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB2_EZ_DATA24	0x40260460	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB2_EZ_DATA25	0x40260464	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB2_EZ_DATA26	0x40260468	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB2_EZ_DATA27	0x4026046C	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB2_EZ_DATA28	0x40260470	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB2_EZ_DATA29	0x40260474	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB2_EZ_DATA30	0x40260478	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB2_EZ_DATA31	0x4026047C	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB2_INTR_CAUSE	0x40260E00	Active clocked interrupt signal. See SCB0_INTR_CAUSE for the details of bit fields.
SCB2_INTR_I2C_EC	0x40260E80	Externally clocked I2C interrupt request. See SCB0_INTR_I2C_EC for the details of bit fields.
SCB2_INTR_I2C_EC_MASK	0x40260E88	Externally clocked I2C interrupt mask. See SCB0_INTR_I2C_EC_MASK for the details of bit fields.
SCB2_INTR_I2C_EC_MASKED	0x40260E8C	Externally clocked I2C interrupt masked. See SCB0_INTR_I2C_EC_MASKED for the details of bit fields.
SCB2_INTR_SPI_EC	0x40260EC0	Externally clocked SPI interrupt request. See SCB0_INTR_SPI_EC for the details of bit fields.
SCB2_INTR_SPI_EC_MASK	0x40260EC8	Externally clocked SPI interrupt mask. See SCB0_INTR_SPI_EC_MASK for the details of bit fields.
SCB2_INTR_SPI_EC_MASKED	0x40260ECC	Externally clocked SPI interrupt masked. See SCB0_INTR_SPI_EC_MASKED for the details of bit fields.
SCB2_INTR_M	0x40260F00	Master interrupt request. See SCB0_INTR_M for the details of bit fields.

Register	Address	Description
SCB2_INTR_M_SET	0x40260F04	Master interrupt set request. See SCB0_INTR_M_SET for the details of bit fields.
SCB2_INTR_M_MASK	0x40260F08	Master interrupt mask. See SCB0_INTR_M_MASK for the details of bit fields.
SCB2_INTR_M_MASKED	0x40260F0C	Master interrupt masked request. See SCB0_INTR_M_MASKED for the details of bit fields.
SCB2_INTR_S	0x40260F40	Slave interrupt request. See SCB0_INTR_S for the details of bit fields.
SCB2_INTR_S_SET	0x40260F44	Slave interrupt set request. See SCB0_INTR_S_SET for the details of bit fields.
SCB2_INTR_S_MASK	0x40260F48	Slave interrupt mask. See SCB0_INTR_S_MASK for the details of bit fields.
SCB2_INTR_S_MASKED	0x40260F4C	Slave interrupt masked request. See SCB0_INTR_S_MASKED for the details of bit fields.
SCB2_INTR_TX	0x40260F80	Transmitter interrupt request. See SCB0_INTR_TX for the details of bit fields.
SCB2_INTR_TX_SET	0x40260F84	Transmitter interrupt set request. See SCB0_INTR_TX_SET for the details of bit fields.
SCB2_INTR_TX_MASK	0x40260F88	Transmitter interrupt mask. See SCB0_INTR_TX_MASK for the details of bit fields.
SCB2_INTR_TX_MASKED	0x40260F8C	Transmitter interrupt masked request. See SCB0_INTR_TX_MASKED for the details of bit fields.
SCB2_INTR_RX	0x40260FC0	Receiver interrupt request. See SCB0_INTR_RX for the details of bit fields.
SCB2_INTR_RX_SET	0x40260FC4	Receiver interrupt set request. See SCB0_INTR_RX_SET for the details of bit fields.
SCB2_INTR_RX_MASK	0x40260FC8	Receiver interrupt mask. See SCB0_INTR_RX_MASKfor the details of bit fields.
SCB2_INTR_RX_MASKED	0x40260FCC	Receiver interrupt masked request. See SCB0_INTR_RX_MASKED for the details of bit fields.
SCB3_CTRL	0x40270000	Generic control. See SCB0_CTRL for the details of bit fields.
SCB3_STATUS	0x40270004	Generic status. See SCB0_STATUS for the details of bit fields.
SCB3_SPI_CTRL	0x40270020	SPI control. See SCB0_SPI_CTRL for the details of bit fields.
SCB3_SPI_STATUS	0x40270024	SPI status. See SCB0_SPI_STATUS for the details of bit fields.
SCB3_SPI_TX_CTRL	0x40270028	SPI transmitter control. See SCB0_SPI_TX_CTRL for the details of bit fields.
SCB3_SPI_RX_CTRL	0x4027002C	SPI receiver control. See SCB0_SPI_RX_CTRL for the details of bit fields.
SCB3_UART_CTRL	0x40270040	UART control. See SCB0_UART_CTRL for the details of bit fields.
SCB3_UART_TX_CTRL	0x40270044	UART transmitter control. See SCB0_UART_TX_CTRL for the details of bit fields.
SCB3_UART_RX_CTRL	0x40270048	UART receiver control. See SCB0_UART_RX_CTRL for the details of bit fields.
SCB3_UART_RX_STATUS	0x4027004C	UART receiver status. See SCB0_UART_RX_STATUS for the details of bit fields.
SCB3_UART_FLOW_CTRL	0x40270050	UART flow control. See SCB0_UART_FLOW_CTRL for the details of bit fields.
SCB3_I2C_CTRL	0x40270060	I2C control. See SCB0_I2C_CTRL for the details of bit fields.
SCB3_I2C_STATUS	0x40270064	I2C status. See SCB1_I2C_STATUS for the details of bit fields.
SCB3_I2C_M_CMD	0x40270068	I2C master command. See SCB0_I2C_M_CMD for the details of bit fields.
SCB3_I2C_S_CMD	0x4027006C	I2C slave command. See SCB0_I2C_S_CMD for the details of bit fields.
SCB3_I2C_CFG	0x40270070	I2C configuration. See SCB0_I2C_CFG for the details of bit fields.
SCB3_I2C_STRETCH_CTRL	0x40270074	I2C stretch control. See SCB0_I2C_STRETCH_CTRL for the details of bit fields.
SCB3_I2C_STRETCH_STATUS	0x40270078	I2C stretch status. See SCB0_I2C_STRETCH_STATUS for the details of bit fields.
SCB3_TX_CTRL	0x40270200	Transmitter control. See SCB0_TX_CTRL for the details of bit fields.
SCB3_TX_FIFO_CTRL	0x40270204	Transmitter FIFO control. See SCB0_TX_FIFO_CTRL for the details of bit fields.
SCB3_TX_FIFO_STATUS	0x40270208	Transmitter FIFO status. See SCB0_TX_FIFO_STATUS for the details of bit fields.
SCB3_TX_FIFO_WR	0x40270240	Transmitter FIFO write. See SCB0_TX_FIFO_WR for the details of bit fields.
SCB3_RX_CTRL	0x40270300	Receiver control. See SCB0_RX_CTRL for the details of bit fields.
SCB3_RX_FIFO_CTRL	0x40270304	Receiver FIFO control. See SCB0_RX_FIFO_CTRL for the details of bit fields.
SCB3_RX_FIFO_STATUS	0x40270308	Receiver FIFO status. See SCB0_RX_FIFO_STATUS for the details of bit fields.
SCB3_RX_MATCH	0x40270310	Slave address and mask. See SCB0_RX_MATCH for the details of bit fields.
SCB3_RX_FIFO_RD	0x40270340	Receiver FIFO read. See SCB0_RX_FIFO_RD for the details of bit fields.

Register	Address	Description
SCB3_RX_FIFO_RD_SILENT	0x40270344	Receiver FIFO read silent. See SCB0_RX_FIFO_RD_SILENT for the details of bit fields.
SCB3_EZ_DATA0	0x40270400	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB3_EZ_DATA1	0x40270404	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB3_EZ_DATA2	0x40270408	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB3_EZ_DATA3	0x4027040C	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB3_EZ_DATA4	0x40270410	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB3_EZ_DATA5	0x40270414	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB3_EZ_DATA6	0x40270418	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB3_EZ_DATA7	0x4027041C	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB3_EZ_DATA8	0x40270420	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB3_EZ_DATA9	0x40270424	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB3_EZ_DATA10	0x40270428	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB3_EZ_DATA11	0x4027042C	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB3_EZ_DATA12	0x40270430	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB3_EZ_DATA13	0x40270434	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB3_EZ_DATA14	0x40270438	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB3_EZ_DATA15	0x4027043C	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB3_EZ_DATA16	0x40270440	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB3_EZ_DATA17	0x40270444	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB3_EZ_DATA18	0x40270448	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB3_EZ_DATA19	0x4027044C	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB3_EZ_DATA20	0x40270450	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB3_EZ_DATA21	0x40270454	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB3_EZ_DATA22	0x40270458	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB3_EZ_DATA23	0x4027045C	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB3_EZ_DATA24	0x40270460	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB3_EZ_DATA25	0x40270464	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB3_EZ_DATA26	0x40270468	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB3_EZ_DATA27	0x4027046C	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB3_EZ_DATA28	0x40270470	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB3_EZ_DATA29	0x40270474	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB3_EZ_DATA30	0x40270478	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB3_EZ_DATA31	0x4027047C	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB3_INTR_CAUSE	0x40270E00	Active clocked interrupt signal. See SCB0_INTR_CAUSE for the details of bit fields.
SCB3_INTR_I2C_EC	0x40270E80	Externally clocked I2C interrupt request. See SCB0_INTR_I2C_EC for the details of bit fields.
SCB3_INTR_I2C_EC_MASK	0x40270E88	Externally clocked I2C interrupt mask. See SCB0_INTR_I2C_EC_MASK for the details of bit fields.
SCB3_INTR_I2C_EC_MASKED	0x40270E8C	Externally clocked I2C interrupt masked. See SCB0_INTR_I2C_EC_MASKED for the details of bit fields.
SCB3_INTR_SPI_EC	0x40270EC0	Externally clocked SPI interrupt request. See SCB0_INTR_SPI_EC for the details of bit fields.
SCB3_INTR_SPI_EC_MASK	0x40270EC8	Externally clocked SPI interrupt mask. See SCB0_INTR_SPI_EC_MASK for the details of bit fields.
SCB3_INTR_SPI_EC_MASKED	0x40270ECC	Externally clocked SPI interrupt masked. See SCB0_INTR_SPI_EC_MASKED for the details of bit fields.
SCB3_INTR_M	0x40270F00	Master interrupt request. See SCB0_INTR_M for the details of bit fields.

Register	Address	Description
SCB3_INTR_M_SET	0x40270F04	Master interrupt set request. See SCB0_INTR_M_SET for the details of bit fields.
SCB3_INTR_M_MASK	0x40270F08	Master interrupt mask. See SCB0_INTR_M_MASK for the details of bit fields.
SCB3_INTR_M_MASKED	0x40270F0C	Master interrupt masked request. See SCB0_INTR_M_MASKED for the details of bit fields.
SCB3_INTR_S	0x40270F40	Slave interrupt request. See SCB0_INTR_S for the details of bit fields.
SCB3_INTR_S_SET	0x40270F44	Slave interrupt set request. See SCB0_INTR_S_SET for the details of bit fields.
SCB3_INTR_S_MASK	0x40270F48	Slave interrupt mask. See SCB0_INTR_S_MASK for the details of bit fields.
SCB3_INTR_S_MASKED	0x40270F4C	Slave interrupt masked request. See SCB0_INTR_S_MASKED for the details of bit fields.
SCB3_INTR_TX	0x40270F80	Transmitter interrupt request. See SCB0_INTR_TX for the details of bit fields.
SCB3_INTR_TX_SET	0x40270F84	Transmitter interrupt set request. See SCB0_INTR_TX_SET for the details of bit fields.
SCB3_INTR_TX_MASK	0x40270F88	Transmitter interrupt mask. See SCB0_INTR_TX_MASK for the details of bit fields.
SCB3_INTR_TX_MASKED	0x40270F8C	Transmitter interrupt masked request. See SCB0_INTR_TX_MASKED for the details of bit fields.
SCB3_INTR_RX	0x40270FC0	Receiver interrupt request. See SCB0_INTR_RX for the details of bit fields.
SCB3_INTR_RX_SET	0x40270FC4	Receiver interrupt set request. See SCB0_INTR_RX_SET for the details of bit fields.
SCB3_INTR_RX_MASK	0x40270FC8	Receiver interrupt mask. See SCB0_INTR_RX_MASKfor the details of bit fields.
SCB3_INTR_RX_MASKED	0x40270FCC	Receiver interrupt masked request. See SCB0_INTR_RX_MASKED for the details of bit fields.
SCB4_CTRL	0x40280000	Generic control. See SCB0_CTRL for the details of bit fields.
SCB4_STATUS	0x40280004	Generic status. See SCB0_STATUS for the details of bit fields.
SCB4_SPI_CTRL	0x40280020	SPI control. See SCB0_SPI_CTRL for the details of bit fields.
SCB4_SPI_STATUS	0x40280024	SPI status. See SCB0_SPI_STATUS for the details of bit fields.
SCB4_SPI_TX_CTRL	0x40280028	SPI transmitter control. See SCB0_SPI_TX_CTRL for the details of bit fields.
SCB4_SPI_RX_CTRL	0x4028002C	SPI receiver control. See SCB0_SPI_RX_CTRL for the details of bit fields.
SCB4_UART_CTRL	0x40280040	UART control. See SCB0_UART_CTRL for the details of bit fields.
SCB4_UART_TX_CTRL	0x40280044	UART transmitter control. See SCB0_UART_TX_CTRL for the details of bit fields.
SCB4_UART_RX_CTRL	0x40280048	UART receiver control. See SCB0_UART_RX_CTRL for the details of bit fields.
SCB4_UART_RX_STATUS	0x4028004C	UART receiver status. See SCB0_UART_RX_STATUS for the details of bit fields.
SCB4_UART_FLOW_CTRL	0x40280050	UART flow control. See SCB0_UART_FLOW_CTRL for the details of bit fields.
SCB4_I2C_CTRL	0x40280060	I2C control. See SCB0_I2C_CTRL for the details of bit fields.
SCB4_I2C_STATUS	0x40280064	I2C status. See SCB1_I2C_STATUS for the details of bit fields.
SCB4_I2C_M_CMD	0x40280068	I2C master command. See SCB0_I2C_M_CMD for the details of bit fields.
SCB4_I2C_S_CMD	0x4028006C	I2C slave command. See SCB0_I2C_S_CMD for the details of bit fields.
SCB4_I2C_CFG	0x40280070	I2C configuration. See SCB0_I2C_CFG for the details of bit fields.
SCB4_I2C_STRETCH_CTRL	0x40280074	I2C stretch control. See SCB0_I2C_STRETCH_CTRL for the details of bit fields.
SCB4_I2C_STRETCH_STATUS	0x40280078	I2C stretch status. See SCB0_I2C_STRETCH_STATUS for the details of bit fields.
SCB4_TX_CTRL	0x40280200	Transmitter control. See SCB0_TX_CTRL for the details of bit fields.
SCB4_TX_FIFO_CTRL	0x40280204	Transmitter FIFO control. See SCB0_TX_FIFO_CTRL for the details of bit fields.
SCB4_TX_FIFO_STATUS	0x40280208	Transmitter FIFO status. See SCB0_TX_FIFO_STATUS for the details of bit fields.
SCB4_TX_FIFO_WR	0x40280240	Transmitter FIFO write. See SCB0_TX_FIFO_WR for the details of bit fields.
SCB4_RX_CTRL	0x40280300	Receiver control. See SCB0_RX_CTRL for the details of bit fields.
SCB4_RX_FIFO_CTRL	0x40280304	Receiver FIFO control. See SCB0_RX_FIFO_CTRL for the details of bit fields.
SCB4_RX_FIFO_STATUS	0x40280308	Receiver FIFO status. See SCB0_RX_FIFO_STATUS for the details of bit fields.
SCB4_RX_MATCH	0x40280310	Slave address and mask. See SCB0_RX_MATCH for the details of bit fields.
SCB4_RX_FIFO_RD	0x40280340	Receiver FIFO read. See SCB0_RX_FIFO_RD for the details of bit fields.

Register	Address	Description
SCB4_RX_FIFO_RD_SILENT	0x40280344	Receiver FIFO read silent. See SCB0_RX_FIFO_RD_SILENT for the details of bit fields.
SCB4_EZ_DATA0	0x40280400	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB4_EZ_DATA1	0x40280404	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB4_EZ_DATA2	0x40280408	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB4_EZ_DATA3	0x4028040C	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB4_EZ_DATA4	0x40280410	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB4_EZ_DATA5	0x40280414	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB4_EZ_DATA6	0x40280418	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB4_EZ_DATA7	0x4028041C	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB4_EZ_DATA8	0x40280420	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB4_EZ_DATA9	0x40280424	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB4_EZ_DATA10	0x40280428	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB4_EZ_DATA11	0x4028042C	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB4_EZ_DATA12	0x40280430	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB4_EZ_DATA13	0x40280434	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB4_EZ_DATA14	0x40280438	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB4_EZ_DATA15	0x4028043C	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB4_EZ_DATA16	0x40280440	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB4_EZ_DATA17	0x40280444	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB4_EZ_DATA18	0x40280448	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB4_EZ_DATA19	0x4028044C	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB4_EZ_DATA20	0x40280450	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB4_EZ_DATA21	0x40280454	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB4_EZ_DATA22	0x40280458	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB4_EZ_DATA23	0x4028045C	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB4_EZ_DATA24	0x40280460	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB4_EZ_DATA25	0x40280464	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB4_EZ_DATA26	0x40280468	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB4_EZ_DATA27	0x4028046C	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB4_EZ_DATA28	0x40280470	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB4_EZ_DATA29	0x40280474	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB4_EZ_DATA30	0x40280478	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB4_EZ_DATA31	0x4028047C	Memory buffer. See SCB0_EZ_DATA0 for the details of bit fields.
SCB4_INTR_CAUSE	0x40280E00	Active clocked interrupt signal. See SCB0_INTR_CAUSE for the details of bit fields.
SCB4_INTR_I2C_EC	0x40280E80	Externally clocked I2C interrupt request. See SCB0_INTR_I2C_EC for the details of bit fields.
SCB4_INTR_I2C_EC_MASK	0x40280E88	Externally clocked I2C interrupt mask. See SCB0_INTR_I2C_EC_MASK for the details of bit fields.
SCB4_INTR_I2C_EC_MASKED	0x40280E8C	Externally clocked I2C interrupt masked. See SCB0_INTR_I2C_EC_MASKED for the details of bit fields.
SCB4_INTR_SPI_EC	0x40280EC0	Externally clocked SPI interrupt request. See SCB0_INTR_SPI_EC for the details of bit fields.
SCB4_INTR_SPI_EC_MASK	0x40280EC8	Externally clocked SPI interrupt mask. See SCB0_INTR_SPI_EC_MASK for the details of bit fields.
SCB4_INTR_SPI_EC_MASKED	0x40280ECC	Externally clocked SPI interrupt masked. See SCB0_INTR_SPI_EC_MASKED for the details of bit fields.
SCB4_INTR_M	0x40280F00	Master interrupt request. See SCB0_INTR_M for the details of bit fields.

Register	Address	Description
SCB4_INTR_M_SET	0x40280F04	Master interrupt set request. See SCB0_INTR_M_SET for the details of bit fields.
SCB4_INTR_M_MASK	0x40280F08	Master interrupt mask. See SCB0_INTR_M_MASK for the details of bit fields.
SCB4_INTR_M_MASKED	0x40280F0C	Master interrupt masked request. See SCB0_INTR_M_MASKED for the details of bit fields.
SCB4_INTR_S	0x40280F40	Slave interrupt request. See SCB0_INTR_S for the details of bit fields.
SCB4_INTR_S_SET	0x40280F44	Slave interrupt set request. See SCB0_INTR_S_SET for the details of bit fields.
SCB4_INTR_S_MASK	0x40280F48	Slave interrupt mask. See SCB0_INTR_S_MASK for the details of bit fields.
SCB4_INTR_S_MASKED	0x40280F4C	Slave interrupt masked request. See SCB0_INTR_S_MASKED for the details of bit fields.
SCB4_INTR_TX	0x40280F80	Transmitter interrupt request. See SCB0_INTR_TX for the details of bit fields.
SCB4_INTR_TX_SET	0x40280F84	Transmitter interrupt set request. See SCB0_INTR_TX_SET for the details of bit fields.
SCB4_INTR_TX_MASK	0x40280F88	Transmitter interrupt mask. See SCB0_INTR_TX_MASK for the details of bit fields.
SCB4_INTR_TX_MASKED	0x40280F8C	Transmitter interrupt masked request. See SCB0_INTR_TX_MASKED for the details of bit fields.
SCB4_INTR_RX	0x40280FC0	Receiver interrupt request. See SCB0_INTR_RX for the details of bit fields.
SCB4_INTR_RX_SET	0x40280FC4	Receiver interrupt set request. See SCB0_INTR_RX_SET for the details of bit fields.
SCB4_INTR_RX_MASK	0x40280FC8	Receiver interrupt mask. See SCB0_INTR_RX_MASKfor the details of bit fields.
SCB4_INTR_RX_MASKED	0x40280FCC	Receiver interrupt masked request. See SCB0_INTR_RX_MASKED for the details of bit fields.

14.1.1 SCB0_CTRL

Generic control

Address: 0x40240000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				OVS [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW		None			RW	RW	RW
HW Access	R		None			R	R	R
Name	MEM_WIDTH [15:14]		None [13:11]			EZ_MODE	EC_OP_-MODE	EC_AM_-MODE

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [23:18]						BLOCK	ADDR_AC-CEPT

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None		RW	None		RW	
HW Access	R	None		R	None		R	
Name	ENABLED	None [30:29]		EC_AC-CESS	None [27:26]		MODE [25:24]	

Bits	Name	Description

14.1.1 SCB0_CTRL (continued)

31	ENABLED	SCB block is enabled ('1') or not ('0'). The proper order in which to initialize SCB is as follows: - Program protocol specific information using SPI_CTRL, UART_CTRL (and UART_TX_CTRL and UART_RX_CTRL) or I2C_CTRL registers. This includes selection of a submode, master/slave functionality and transmitter/receiver functionality when applicable. - Program generic transmitter (TX_CTRL) and receiver (RX_CTRL) information. This includes enabling of the transmitter and receiver functionality. - Program transmitter FIFO (TX_FIFO_CTRL) and receiver FIFO (RX_FIFO_CTRL) information. - Program CTRL register to enable SCB, select the specific operation mode and oversampling factor. Generally when this block is enabled, no control information should be changed. Changes should be made AFTER disabling this block, e.g. to modify the operation mode (from I2C to SPI) or to go from externally to internally clocked. The change takes effect after the block is re-enabled. Note that disabling the block will cause re-initialization of the design and associated state is lost (e.g. FIFO content). Specific to SPI master case, when SCB is idle, below registers can be changed without disabling SCB block, TX_CTRL TX_FIFO_CTRL RX_CTRL RX_FIFO_CTRL SPI_CTRL.SSEL, Default Value: 0
28	EC_ACCESS	EC_ACCESS is used to enable I2CS_EC or SPIS_EC access to internal EZ memory. 1: enable clk_scb 0: disable clk_scb Before going to deepsleep this field should be set to 1. when waking up from DeepSleep power mode, and PLL is locked (clk_scb is at expected frequency), this filed should be set to 0. Default Value: 0
25 : 24	MODE	Mode of operation (3: Reserved) Default Value: 3 **0x0: I2C :** Inter-Integrated Circuits (I2C) mode. **0x1: SPI :** Serial Peripheral Interface (SPI) mode. **0x2: UART :** Universal Asynchronous Receiver/Transmitter (UART) mode.
17	BLOCK	Only used in externally clocked mode. If the externally clocked logic and the internal CPU accesses to EZ memory coincide/collide, this bit determines whether the CPU access should block and result in bus wait states ('BLOCK is 1') or not (BLOCK is '0'). IF BLOCK is '0' and the accesses collide, CPU read operations return 0xffff:ffff and CPU write operations are ignored. Colliding accesses are registered as interrupt causes: INTR_TX.BLOCKED and INTR_RX.BLOCKED. Default Value: 0

14.1.1 SCB0_CTRL (continued)

16	ADDR_ACCEPT	Determines whether a received matching address is accepted in the RX FIFO ('1') or not ('0'). In I2C mode, this field is used to allow the slave to put the received slave address or general call address in the RX FIFO. Note that a received matching address is put in the RX FIFO when this bit is '1' for both I2C read and write transfers. In multi-processor UART receiver mode, this field is used to allow the receiver to put the received address in the RX FIFO. Note: non-matching addresses are never put in the RX FIFO. Default Value: 0
15 : 14	MEM_WIDTH	Determines the number of bits per FIFO data element, depending on physical SRAM cell data width. On M0S8/MXS40S platform, the SRAM data width is 16 bit, so WORD (2) is not supported. On MXS40E platform, the SRAM data width is 32 bits. Default Value: 1 **0x0: BYTE :** 8-bit FIFO data elements. This mode provides the biggest amount of FIFO entries, but TX_CTRL.DATA_WIDTH and RX_CTRL.DATA_WIDTH are restricted to [0, 7]. **0x1: HALFWORD :** 16-bit FIFO data elements. TX_CTRL.DATA_WIDTH and RX_CTRL.DATA_WIDTH are restricted to [0, 15]. **0x2: WORD :** 32-bit FIFO data elements. This mode provides the smallest amount of FIFO entries, but TX_CTRL.DATA_WIDTH and RX_CTRL.DATA_WIDTH can be in a range of [0, 31]. **0x3: Reserved :** This setting is reserved. Do not use.
10	EZ_MODE	Non EZ mode ('0') or EZ mode ('1'). In EZ mode, a meta protocol is applied to the serial interface protocol. This meta protocol adds meaning to the data frames transferred by the serial interface protocol: a data frame can represent a memory address, a write memory data element or a read memory data element. EZ mode is only used for synchronous serial interface protocols: SPI and I2C. In SPI mode, only Motorola submode (all Motorola modes: 0, 1, 2, 3) is supported and the transmitter should use continuous data frames; i.e. data frames not separated by slave deselection. This mode is only applicable to slave functionality. In EZ mode, the slave can read from and write to an addressable memory structure of 32 bytes. In EZ mode, data frames should 8-bit in size and should be transmitted and received with the Most Significant Bit (MSB) first. In UART mode this field should be '0'. Default Value: 0

14.1.1 SCB0_CTRL (continued)

9	EC_OP_MODE	This field specifies the clocking for the SCB block '0': Internally clocked mode '1': externally clocked mode In internally clocked mode, the serial interface protocols run off the SCB clock. In externally clocked mode, the serial interface protocols run off the clock as provided by the serial interface. Externally clocked operation mode is only used for synchronous serial interface protocols (SPI and I2C) in slave mode AND EZ mode. In SPI mode, only Motorola submode (all Motorola modes: 0, 1, 2, 3) is supported. The maximum SPI slave, EZ mode bitrate is 48 Mbps (transmission and IO delays outside the IP will degrade the effective bitrate). In UART mode this field should be '0'. Default Value: 0
8	EC_AM_MODE	This field specifies the clocking for the address matching (I2C) or slave selection detection logic (SPI) '0': Internally clocked mode '1': Externally clocked mode In internally clocked mode, the serial interface protocols run off the SCB clock. In externally clocked mode, the serial interface protocols run off the clock as provided by the serial interface. The clocking for the rest of the logic is determined by CTRL.EC_OP_MODE. Externally clocked mode is only used for synchronous serial interface protocols (SPI and I2C) in slave mode. In SPI mode, only Motorola submode (all Motorola modes: 0, 1, 2, 3) is supported. In UART mode this field should be '0'. Default Value: 0

14.1.1 SCB0_CTRL (continued)

3 : 0	OVS	Serial interface bit period oversampling factor expressed in SCB clock cycles. Used for SPI and UART functionality. OVS + 1 SCB clock cycles constitute a single serial interface clock/bit cycle. This field is NOT used in externally clocked mode. If OVS is odd, the oversampling factor is even and the low and high phase of the interface clock period are the same. If OVS is even, the oversampling factor is odd and the low and high phase can differ by 1 SCB clock period. In SPI master mode, the valid range is [3, 15]. At an SCB frequency of 48 MHz, the maximum SPI bit rate is 12 Mbps, assuming ideal (0 ns) IO cell and routing (chip and board) delay. The calculated maximum bit rate decreases, when realistic chip and routing delays are taken into account. The effective system bit rate is dependent on the external SPI slave that we communicate with. If the SPI output clock to SPI MISO input round trip delay is significant (multiple SPI output clock cycles), it may be necessary to increase OVS and/or to set SPI_CTRL.LATE_MISO_SAMPLE to '1' to achieve the maximum possible system bit rate. In SPI slave mode, the OVS field is NOT used. However, there is a frequency requirement for the SCB clock wrt. the SPI input clock (IF) on the interface to guarantee functional correct behavior. This requirement is expressed as a ratio: SCB clock/IF clock. The ratio is dependent on the setting of RX_CTRL.MEDIAN and the external SPI master's capability to support "late MISO sample" functionality (similar to our SPI master functionality represented by SPI_CTRL.LATE_MISO_SAMPLE): - MEDIAN is '0' and external SPI master has NO "late MISO sample functionality": SCB clock/IF clock >= 6. At a SCB frequency of 48 MHz, the maximum bit rate is 8 Mbps. - MEDIAN is '0' and external SPI master has "late MISO sample functionality": SCB clock/IF clock >= 3. At a SCB frequency of 48 MHz, the maximum bit rate is 16 Mbps. - MEDIAN is '1' and external SPI master has NO "late MISO sample functionality": SCB clock/IF clock >= 8. At a SCB frequency of 48 MHz, the maximum bit rate is 6 Mbps. - MEDIAN is '1' and external SPI master has "late MISO sample functionality": SCB clock/IF clock >= 4. At a SCB frequency of 48 MHz, the maximum bit rate is 12 Mbps. As discussed earlier, the calculated maximum bit rate decreases, when realistic chip and routing delays are taken into account. In UART standard submode (including LIN), the valid range is [7, 15]. In UART SmartCard submode, the valid range is [7, 15]. In UART TX IrDA submode this field indirectly specifies the oversampling. The oversampling determines the interface clock/bit cycle and the width of the pulse. Only normal transmission mode is supported, the pulse is roughly 3/16 of the bit period (for all bit rates). There is only one valid OVS value: - 0: 16 times oversampling. SCB clock frequency of 16*115.2 KHz for 115.2 Kbps. SCB clock frequency of 16*57.6 KHz for 57.6 Kbps. SCB clock frequency of 16*38.4 KHz for 38.4 Kbps. SCB clock frequency of 16*19.2 KHz for 19.2 Kbps. SCB clock frequency of 16*9.6 KHz for 9.6 Kbps. SCB clock frequency of 16*2.4 KHz for 2.4 Kbps. SCB clock frequency of 16*1.2 KHz for 1.2 Kbps. - all other values are not used in normal mode. In UART RX IrDA submode (1.2, 2.4, 9.6, 19.2, 38.4, 57.6 and 115.2 Kbps) this field indirectly specifies the oversampling. The oversampling determines the interface clock/bit cycle and the width of the pulse. In normal transmission mode, this pulse is roughly 3/16 of the bit period (for all bit rates). In low power transmission mode, this pulse is potentially smaller (down to 1.62 us typical and 1.41 us minimal) than 3/16 of the bit period (for < 115.2 Kbps bitrates). Pulse widths greater or equal than two SCB clock cycles are guaranteed to be detected by the receiver. Pulse widths less than two SCB clock cycles and greater or equal than one SCB clock cycle may be detected by the receiver. Pulse widths less than one SCB clock cycle will not be detected by the receiver. RX_CTRL.MEDIAN should be set to '1' for IrDA receiver functionality. The SCB clock (as provided by the programmable clock block) and the oversampling together determine the IrDA bitrate. Normal mode, OVS field values (with the required SCB clock frequency): - 0: 16 times oversampling. SCB clock frequency of 16*115.2 KHz for 115.2 Kbps. SCB clock frequency of 16*57.6 KHz for 57.6 Kbps. SCB clock frequency of 16*38.4 KHz for 38.4 Kbps. SCB clock frequency of 16*19.2 KHz for 19.2 Kbps. SCB clock frequency of 16*9.6 KHz for 9.6 Kbps. SCB clock frequency of 16*2.4 KHz for 2.4 Kbps. SCB clock frequency of 16*1.2 KHz for 1.2 Kbps. - all other values are not used in normal mode. Low power mode, OVS field values (with the required SCB clock frequency): - 0: 16 times oversampling. SCB clock frequency of 16*115.2 KHz for 115.2 Kbps. - 1: 32 times oversampling. SCB clock frequency of 32*57.6 KHz for 57.6 Kbps. - 2: 48 times oversampling. SCB clock frequency of 48*38.4 KHz for 38.4 Kbps. - 3: 96 times oversampling. SCB clock frequency of 96*19.2 KHz for 19.2 Kbps. - 4: 192 times oversampling. SCB clock frequency of 192*9.6 KHz for 9.6 Kbps. - 5: 768 times oversampling. SCB clock frequency of 768*2.4 KHz for 2.4 Kbps. - 6: 1536 times oversampling. SCB clock frequency of 1536*1.2 KHz for 1.2 Kbps. - all other values are not used in low power mode. Default Value: 15

14.1.2 SCB0_STATUS

Generic status

Address: 0x40240004

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							W
Name	None [7:1]							EC_BUSY

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	EC_BUSY	Indicates whether the externally clocked logic is potentially accessing the EZ memory (this is only possible in EZ mode). This bit can be used by SW to determine whether it is safe to issue a SW access to the EZ memory (without bus wait states (a blocked SW access) or bus errors being generated). Note that the INTR_TX.BLOCKED and INTR_RX.BLOCKED interrupt causes are used to indicate whether a SW access was actually blocked by externally clocked logic. Default Value: Undefined

14.1.3 SCB0_SPI_CTRL

SPI control

Address: 0x40240020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		R	R	R	R	R	R
Name	None [7:6]		SCLK_-CONTINU-OUS	LATE_MISO_SAMPLE	CPOL	CPHA	SE-LECT_PRE-CEDE	SSEL_-CONTINU-OUS

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW	RW	RW	RW	RW	RW	RW
HW Access	None	R	R	R	R	R	R	R
Name	None	SSEL_INTER_-FRAME_DEL	SSEL_HOLD_DEL	SSEL_SET-UP_DEL	SSEL_PO-LARITY3	SSEL_PO-LARITY2	SSEL_PO-LARITY1	SSEL_PO-LARITY0

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							LOOPBACK

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None			RW		RW	
HW Access	R	None			R		R	
Name	MASTER_-MODE	None [30:28]			SSEL [27:26]		MODE [25:24]	

Bits	Name	Description
31	MASTER_MODE	Master ('1') or slave ('0') mode. In master mode, transmission will commence on availability of data frames in the TX FIFO. In slave mode, when selected and there is no data frame in the TX FIFO, the slave will transmit all '1's. In both master and slave modes, received data frames will be lost if the RX FIFO is full. Default Value: 0
27 : 26	SSEL	Selects one of the four incoming/outgoing SPI slave select signals: - 0: Slave 0, SSEL[0]. - 1: Slave 1, SSEL[1]. - 2: Slave 2, SSEL[2]. - 3: Slave 3, SSEL[3]. SCB block should be disabled when changes are made to this field. Default Value: 0

14.1.3 SCB0_SPI_CTRL (continued)

25 : 24	MODE	Submode of SPI operation (3: Reserved). Default Value: 3 **0x0: SPI_MOTOROLA :** SPI Motorola submode. In master mode, when not transmitting data (Slave SELECT is inactive), SCLK is stable at CPOL. In slave mode, when not selected, SCLK is ignored; i.e. it can be either stable or clocking. In master mode, when there is no data to transmit (TX FIFO is empty), Slave SELECT is inactive. **0x1: SPI_TI :** SPI Texas Instruments submode. In master mode, when not transmitting data, SCLK is stable at '0'. In slave mode, when not selected, SCLK is ignored; i.e. it can be either stable or clocking. In master mode, when there is no data to transmit (TX FIFO is empty), Slave SELECT is inactive; i.e. no pulse is generated. **0x2: SPI_NS :** SPI National Semiconductors submode. In master mode, when not transmitting data, SCLK is stable at '0'. In slave mode, when not selected, SCLK is ignored; i.e. it can be either stable or clocking. In master mode, when there is no data to transmit (TX FIFO is empty), Slave SELECT is inactive.
16	LOOPBACK	Local loopback control (does NOT affect the information on the pins). Only used in master mode. Not used in National Semiconductors submode. '0': No local loopback '1': the SPI master MISO line is connected to the SPI master MOSI line. In other words, in loop-back mode the SPI master receives on MISO what it transmits on MOSI. Default Value: 0
14	SSEL_INTER_-FRAME_DEL	Indicates the SPI SELECT inter-dataframe delay (between SELECT deactivation and SELECT activation). '0': 1.5 SPI clock cycles '1': 2.5 SPI clock cycles Only applies in SPI MOTOROLA submode and when SPI_CTRL.SSEL_CONTINUOUS=0, CTRL.OVS>=3. above are ideal case at SCB block level, and there is inaccuracy of one clk_scb cycle. Default Value: 0
13	SSEL_HOLD_DEL	Indicates the SPI SELECT hold delay (between SPI clock edge to sample the last MOSI bit, and SELECT deactivation). '0': 0.75 SPI clock cycles '1': 1.75 SPI clock cycles Only applies in SPI MOTOROLA submode and when SCLK_CONTINUOUS=0, CTRL.OVS>=3. above are ideal case at SCB block level, and there is inaccuracy of one clk_scb cycle. Default Value: 0
12	SSEL_SETUP_DEL	Indicates the SPI SELECT setup delay (between SELECT activation and SCLK clock edge to sample the first MOSI bit). '0': 0.75 SPI clock cycles '1': 1.75 SPI clock cycles Only applies in SPI MOTOROLA submode and when SCLK_CONTINUOUS=0, CTRL.OVS>=3. above are ideal case at SCB block level, and there is inaccuracy of one clk_scb cycle. Default Value: 0

14.1.3 SCB0_SPI_CTRL (continued)

11	SSEL_POLARITY3	Slave select polarity. Default Value: 0
10	SSEL_POLARITY2	Slave select polarity. Default Value: 0
9	SSEL_POLARITY1	Slave select polarity. Default Value: 0
8	SSEL_POLARITY0	Slave select polarity. SSEL_POLARITY0 applies to the outgoing SPI slave select signal 0 (master mode) and to the incoming SPI slave select signal (slave mode). For Motorola and National Semiconductors submodes: '0': slave select is low/'0' active. '1': slave select is high/'1' active. For Texas Instruments submode: '0': high/'1' active precede/coincide pulse. '1': low/'0' active precede/coincide pulse. Default Value: 0
5	SCLK_CONTINUOUS	Only applicable in master mode. '0': SCLK is generated, when the SPI master is enabled and data is transmitted. '1': SCLK is generated, when the SPI master is enabled. This mode is useful for slave devices that use SCLK for functional operation other than just SPI functionality. Default Value: 0
4	LATE_MISO_SAMPLE	Changes the SCLK edge on which MISO is captured. Only used in master mode. When '0', the default applies (for Motorola as determined by CPOL and CPHA, for Texas Instruments on the falling edge of SCLK and for National Semiconductors on the rising edge of SCLK). When '1', the alternate clock edge is used (which comes half a SPI SCLK period later). Late sampling addresses the round trip delay associated with transmitting SCLK from the master to the slave and transmitting MISO from the slave to the master. Default Value: 1
3	CPOL	Indicates the clock polarity. This field, together with the CPHA field, indicates when MOSI data is driven and MISO data is captured: - CPOL is '0': SCLK is '0' when not transmitting data. - CPOL is '1': SCLK is '1' when not transmitting data. Default Value: 0
2	CPHA	Indicates the clock phase. This field, together with the CPOL field, indicates when MOSI data is driven and MISO data is captured: - Motorola mode 0. CPOL is '0', CPHA is '0': MOSI is driven on a falling edge of SCLK. MISO is captured on a rising edge of SCLK. - Motorola mode 1. CPOL is '0', CPHA is '1': MOSI is driven on a rising edge of SCLK. MISO is captured on a falling edge of SCLK. - Motorola mode 2. CPOL is '1', CPHA is '0': MOSI is driven on a rising edge of SCLK. MISO is captured on a falling edge of SCLK. - Motorola mode 3. CPOL is '1', CPHA is '1': MOSI is driven on a falling edge of SCLK. MISO is captured on a rising edge of SCLK. In SPI Motorola submode, all four CPOL/CPHA modes are valid. in SPI NS submode, only CPOL=0 CPHA=0 mode is valid. in SPI TI submode, only CPOL=0 CPHA=1 mode is valid. Default Value: 0

14.1.3 SCB0_SPI_CTRL (continued)

1	SELECT_PRECEDE	Only used in SPI Texas Instruments' submode. When '1', the data frame start indication is a pulse on the Slave SELECT line that precedes the transfer of the first data frame bit. When '0', the data frame start indication is a pulse on the Slave SELECT line that coincides with the transfer of the first data frame bit. Default Value: 0
0	SSEL_CONTINUOUS	Continuous SPI data transfers enabled ('1') or not ('0'). This field is used in master mode. In slave mode, both continuous and non-continuous SPI data transfers are supported independent of this field. When continuous transfers are enabled individual data frame transfers are not necessarily separated by slave deselection (as indicated by the level or pulse on the SELECT line): if the TX FIFO has multiple data frames, data frames are send out without slave deselection. When continuous transfers are not enabled individual data frame transfers are always separated by slave deselection: independent of the availability of TX FIFO data frames, data frames are sent out with slave deselection. Default Value: 0

14.1.4 SCB0_SPI_STATUS

SPI status

Address: 0x40240024

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						W	W
Name	None [7:2]						SPI_EC_BUSY	BUS_BUSY

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	CURR_EZ_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	BASE_EZ_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	BASE_EZ_ADDR	SPI base EZ address. Address as provided by a SPI write transfer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable, as clock domain synchronization is not performed in the design. Default Value: Undefined
15 : 8	CURR_EZ_ADDR	SPI current EZ address. Current address pointer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable (during an ongoing transfer when SPI_EC_BUSY is '1'), as clock domain synchronization is not performed in the design. Default Value: Undefined
1	SPI_EC_BUSY	Indicates whether the externally clocked logic is potentially accessing the EZ memory and/or updating BASE_ADDR or CURR_ADDR (this is only possible in EZ mode). This bit can be used by SW to determine whether BASE_ADDR and CURR_ADDR are reliable. Default Value: Undefined
0	BUS_BUSY	SPI bus is busy. The bus is considered busy ('1') during an ongoing transaction. For Motorola and National submodes, the busy bit is '1', when the slave selection is activated. For TI submode, the busy bit is '1' from the time the preceding/coinciding slave select is activated for the first transmitted data frame, till the last MOSI/MISO bit of the last data frame is transmitted. Default Value: Undefined

14.1.5 SCB0_SPI_TX_CTRL

SPI transmitter control

Address: 0x40240028

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	None			
HW Access	None		R	R	None			
Name	None [7:6]		PARITY_ENABLED	PARITY	None			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							MOSI_IDLE_HIGH

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
16	MOSI_IDLE_HIGH	SPI master MOSI output level when SELECT output inactive, 0: retain the level of last data bit 1: change to high, (MOSI level is high, before the first data bit time, and after data bit time, defined SSEL/SCLK driving edge with CPOL/CPHA) Default Value: 0
5	PARITY_ENABLED	Parity generation enabled ('1') or not ('0'). Default Value: 0
4	PARITY	Parity bit. When '0', the transmitter generates an even parity. When '1', the transmitter generates an odd parity. Default Value: 0

14.1.6 SCB0_SPI_RX_CTRL

SPI receiver control

Address: 0x4024002C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	None			
HW Access	None		R	R	None			
Name	None [7:6]		PARITY_ENABLED	PARITY	None			

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							DROP_ON_PARITY_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	DROP_ON_PARITY_ERROR	Behavior when a parity check fails. When '0', received data is send to the RX FIFO. When '1', received data is dropped and lost. Default Value: 0
5	PARITY_ENABLED	Parity checking enabled ('1') or not ('0'). Default Value: 0
4	PARITY	Parity bit. When '0', the receiver expects an even parity. When '1', the receiver expects an odd parity. Default Value: 0

14.1.7 SCB0_UART_CTRL

UART control

Address: 0x40240040

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							LOOPBACK

Bits	31	30	29	28	27	26	25	24
SW Access	None						RW	
HW Access	None						R	
Name	None [31:26]						MODE [25:24]	

Bits	Name	Description
25 : 24	MODE	Submode of UART operation (3: Reserved) Default Value: 3 **0x0: UART_STD :** Standard UART submode. **0x1: UART_SMARTCARD :** SmartCard (ISO7816) submode. Support for negative acknowledgement (NACK) on the receiver side and retransmission on the transmitter side. **0x2: UART_IRDA :** Infrared Data Association (IrDA) submode. Return to Zero modulation scheme. In this mode, the oversampling factor should be 16, that is OVS should be set to 15.

14.1.7 SCB0_UART_CTRL (continued)

16	LOOPBACK	Local loopback control (does NOT affect the information on the pins). 0: Loopback is not enabled 1: UART_TX is connected to UART_RX. UART_RTS is connected to UART_CTS. This allows a SCB UART transmitter to communicate with its receiver counterpart. Default Value: 0

14.1.8 SCB0_UART_TX_CTRL

UART transmitter control

Address: 0x40240044

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	None	RW		
HW Access	None		R	R	None	R		
Name	None [7:6]		PARITY_ENABLED	PARITY	None	STOP_BITS [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							RETRY_ON_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	RETRY_ON_NACK	When '1', a data frame is retransmitted when a negative acknowledgement is received. Only applicable to the SmartCard submode. Default Value: 0
5	PARITY_ENABLED	Parity generation enabled ('1') or not ('0'). Only applicable in standard UART submodes. In SmartCard submode, parity generation is always enabled through hardware. In IrDA submode, parity generation is always disabled through hardware Default Value: 0
4	PARITY	Parity bit. When '0', the transmitter generates an even parity. When '1', the transmitter generates an odd parity. Only applicable in standard UART and SmartCard submodes. Default Value: 0
2 : 0	STOP_BITS	Stop bits. STOP_BITS + 1 is the duration of the stop period in terms of halve bit periods. Valid range is [1, 7]; i.e. a stop period should last at least one bit period. Default Value: 2

14.1.9 SCB0_UART_RX_CTRL

UART receiver control

Address: 0x40240048

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW	RW	RW	None	RW		
HW Access	None	R	R	R	None	R		
Name	None	POLARITY	PARITY_ENABLED	PARITY	None	STOP_BITS [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW	RW	None	RW	RW	RW
HW Access	None		R	R	None	R	R	R
Name	None [15:14]		SKIP_START	LIN_MODE	None	MP_MODE	DROP_ON_FRAME_ERROR	DROP_ON_PARITY_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				BREAK_WIDTH [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None							RW
HW Access	None							R
Name	None [31:25]							BREAK_LEVEL

Bits	Name	Description
24	BREAK_LEVEL	0: low level pulse detection, like Break field in LIN protocol 1: high level pulse detection, like IFS field in CXPI protocol, or idle line state in UART Default Value: 0

14.1.9 SCB0_UART_RX_CTRL (continued)

19 : 16	BREAK_WIDTH	Break width. BREAK_WIDTH + 1 is the minimum width in bit periods of a break. During a break the transmitted/received line value is '0'. This feature is useful for standard UART submode and LIN submode ("break field" detection). Once, the break is detected, the INTR_RX.BREAK_DETECT bit is set to '1'. Note that break detection precedes baud rate detection, which is used to synchronize/refine the receiver clock to the transmitter clock. As a result, break detection operates with an unsynchronized/unrefined receiver clock. Therefore, the receiver's definition of a bit period is imprecise and the setting of this field should take this imprecision into account. The LIN standard also accounts for this imprecision: a LIN start bit followed by 8 data bits allows for up to 9 consecutive '0' bit periods during regular transmission, whereas the LIN break detection should be at least 13 consecutive '0' bit periods. This provides for a margin of 4 bit periods. Therefore, the default value of this field is set to 10, representing a minimal break field with of 10+1 = 11 bit periods; a value in between the 9 consecutive bit periods of a regular transmission and the 13 consecutive bit periods of a break field. This provides for slight imprecisions of the receiver clock wrt. the transmitter clock. There should not be a need to program this field to any value other than its default value. Default Value: 10
13	SKIP_START	Only applicable in standard UART submode. When '1', the receiver skips start bit detection for the first received data frame. Instead, it synchronizes on the first received data frame bit, which should be a '1'. This functionality is intended for wake up from DeepSleep when receiving a data frame. The transition from idle ('1') to START ('0') on the RX line is used to wake up the CPU. The transition detection (and the associated wake up functionality) is performed by the GPIO2 IP. The woken up CPU will enable the SCB's UART receiver functionality. Once enabled, it is assumed that the START bit is ongoing (the CPU wakeup and SCB enable time should be less than the START bit period). The SCB will synchronize to a '0' to '1' transition, which indicates the first data frame bit is received (first data frame bit should be '1'). After synchronization to the first data frame bit, the SCB will resume normal UART functionality: subsequent data frames will be synchronized on the receipt of a START bit. Default Value: 0
12	LIN_MODE	Only applicable in standard UART submode. When '1', the receiver performs break detection and baud rate detection on the incoming data. First, break detection counts the amount of bit periods that have a line value of '0'. BREAK_WIDTH specifies the minimum required amount of bit periods. Successful break detection sets the INTR_RX.BREAK_DETECT interrupt cause to '1'. Second, baud rate detection counts the amount of peripheral clock periods that are use to receive the synchronization byte (0x55; least significant bit first). The count is available through UART_RX_STATUS.BR_COUNTER. Successful baud rate detection sets the INTR_RX.BAUD_DETECT interrupt cause to '1' (BR_COUNTER is reliable). This functionality is used to synchronize/refine the receiver clock to the transmitter clock. The receiver software can use the BR_COUNTER value to set the right IP clock (from the programmable clock IP) to guarantee successful receipt of the first LIN data frame (Protected Identifier Field) after the synchronization byte. Default Value: 0
10	MP_MODE	Multi-processor mode. When '1', multi-processor mode is enabled. In this mode, RX_CTRL.DATA_WIDTH should indicate a 9-bit data frame. In multi-processor mode, the 9th received bit of a data frame separates addresses (bit is '1') from data (bit is '0'). A received address is matched with RX_MATCH.DATA and RX_MATCH.MASK. In the case of a match, subsequent received data are sent to the RX FIFO. In the case of NO match, subsequent received data are dropped. Default Value: 0
9	DROP_ON_FRAME_ERROR	Behavior when an error is detected in a start or stop period. When '0', received data is sent to the RX FIFO. When '1', received data is dropped and lost. Default Value: 0

14.1.9 SCB0_UART_RX_CTRL (continued)

8	DROP_ON_PARITY_ERROR	Behavior when a parity check fails. When '0', received data is sent to the RX FIFO. When '1', received data is dropped and lost. Only applicable in standard UART and SmartCard submodes (negatively acknowledged SmartCard data frames may be dropped with this field). Default Value: 0
6	POLARITY	Inverts incoming RX line signal. Inversion is after local loopback. This functionality is intended for IrDA receiver functionality. Default Value: 0
5	PARITY_ENABLED	Parity checking enabled ('1') or not ('0'). Only applicable in standard UART submode. In SmartCard submode, parity checking is always enabled through hardware. In IrDA submode, parity checking is always disabled through hardware. Default Value: 0
4	PARITY	Parity bit. When '0', the receiver expects an even parity. When '1', the receiver expects an odd parity. Only applicable in standard UART and SmartCard submodes. Default Value: 0
2 : 0	STOP_BITS	Stop bits. STOP_BITS + 1 is the duration of the stop period in terms of half bit periods. Valid range is [1, 7]; i.e. a stop period should last at least one bit period. Note that in case of a stop bits error, the successive data frames may get lost as the receiver needs to resynchronize its start bit detection. The amount of lost data frames depends on both the amount of stop bits, the idle time between data frames and the data frame value. Default Value: 2

14.1.10 SCB0_UART_RX_STATUS

UART receiver status

Address: 0x4024004C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	BR_COUNTER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None				R			
HW Access	None				W			
Name	None [15:12]				BR_COUNTER [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11 : 0	BR_COUNTER	Amount of SCB clock periods that constitute the transmission of a 0x55 data frame (sent least significant bit first) as determined by the receiver. BR_COUNTER / 8 is the amount of SCB clock periods that constitute a bit period. This field has valid data when INTR_RX.BAUD_DETECT is set to '1'. Default Value: Undefined

14.1.11 SCB0_UART_FLOW_CTRL

UART flow control

Address: 0x40240050

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				TRIGGER_LEVEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							RTS_POLARITY

Bits	31	30	29	28	27	26	25	24
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [31:26]						CTS_ENABLED	CTS_POLARITY

Bits	Name	Description
25	CTS_ENABLED	Enable use of CTS input signal by the UART transmitter: '0': Disabled. The UART transmitter ignores the CTS input signal and transmits when a data frame is available for transmission in the TX FIFO or the TX shift register. '1': Enabled. The UART transmitter uses CTS input signal to qualify the transmission of data. It transmits when CTS input signal is active and a data frame is available for transmission in the TX FIFO or the TX shift register. If UART_CTRL.LOOPBACK is '1', the CTS input signal is driven by the RTS output signal locally in SCB (both signals are subjected to signal polarity changes are indicated by RTS_POLARITY and CTS_POLARITY). Default Value: 0
24	CTS_POLARITY	Polarity of the CTS input signal '0': CTS is active low ; '1': CTS is active high; Default Value: 0

14.1.11 SCB0_UART_FLOW_CTRL (continued)

16	RTS_POLARITY	Polarity of the RTS output signal: '0': RTS is active low; '1': RTS is active high; During SCB reset (Hibernate system power mode), RTS output signal is '1'. This represents an inactive state assuming an active low polarity. Default Value: 0
3 : 0	TRIGGER_LEVEL	Trigger level. When the receiver FIFO has less entries than the amount of this field, a Ready To Send (RTS) output signal is activated. By setting this field to "0", flow control is effectively disabled (may be useful for debug purposes). Default Value: 0

14.1.12 SCB0_I2C_CTRL

I2C control

Address: 0x40240060

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	LOW_PHASE_OVS [7:4]				HIGH_PHASE_OVS [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW	RW	RW	RW	RW	None	RW	RW
HW Access	R	R	R	R	R	None	R	R
Name	S_NOT_READY_-DATA_NACK	S_NOT_READY_AD-DR_NACK	S_READY_DATA_ACK	S_READY_ADDR_ACK	S_GENER-AL_IGNORE	None	M_NOT_READY_-DATA_NACK	M_READY_DATA_ACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							LOOPBACK

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None					
HW Access	R	R	None					
Name	MASTER_-MODE	SLAVE_-MODE	None [29:24]					

Bits	Name	Description
31	MASTER_MODE	Master mode enabled ('1') or not ('0'). Note that both master and slave modes can be enabled at the same time. This allows the IP to address itself. Default Value: 0
30	SLAVE_MODE	Slave mode enabled ('1') or not ('0'). Default Value: 0
16	LOOPBACK	Local loopback control (does NOT affect the information on the pins). Only applicable in master/slave mode. When '0', no loopback When '1', loopback is enabled internally in the peripheral, and as a result unaffected by other I2C devices. This allows a SCB I2C peripheral to address itself. Default Value: 0

14.1.12 SCB0_I2C_CTRL (continued)

15	S_NOT_READY_-DATA_NACK	Only used when: - non EZ mode Functionality is as follows: - 1: a received data element byte the slave is immediately NACK'd when the receiver FIFO is full. - 0: clock stretching is performed (till the receiver FIFO is no longer full). Default Value: 1
14	S_NOT_READY_AD-DR_NACK	This field is used during an address match or general call address in internally clocked mode Only used when: - EC_AM_MODE is '0', EC_OP_MODE is '0', S_GENERAL_IGNORE is '0] and non EZ mode. Functionality is as follows: - 1: a received (matching) slave address is immediately NACK'd when the receiver FIFO is full. - 0: clock stretching is performed (till the receiver FIFO is no longer full). For externally clocked logic (EC_AM is '1') on an address match or general call address (and S_GENERAL_IGNORE is '0'). Only used when (NOT used when EC_AM is '1' and EC_OP is '1' and address match and EZ mode): - EC_AM is '1' and EC_OP is '0'. - EC_AM is '1' and general call address match. - EC_AM is '1' and non EZ mode. Functionality is as follows: - 1: a received (matching or general) slave address is always immediately NACK'd. There are two possibilities: 1). the SCB clock is available (in Active system power mode) and it handles the rest of the current transfer. In this case the I2C master will not observe the NACK. 2).SCB clock is not present (in DeepSleep system power mode). In this case the I2C master will observe the NACK and may retry the transfer in the future (which gives the internally clocked logic the time to wake up from DeepSleep system power mode). - 0: clock stretching is performed (till the SCB clock is available). The logic will handle the ongoing transfer as soon as the clock is enabled. Default Value: 1
13	S_READY_DATA_ACK	When '1', a received data element by the slave is immediately ACK'd when the receiver FIFO is not full. In EZ mode, this field should be set to '1'. Default Value: 1
12	S_READY_ADDR_ACK	When '1', a received (matching) slave address is immediately ACK'd when the receiver FIFO is not full. In EZ mode, this field should be set to '1'. Default Value: 1
11	S_GENERAL_IGNORE	When '1', a received general call slave address is immediately NACK'd (no ACK or clock stretching) and treated as a non matching slave address. This is useful for slaves that do not need any data supplied within the general call structure. Default Value: 1
9	M_NOT_READY_-DATA_NACK	for I2C master, the NACKed byte should be properly received. it write the data byte, before ACK/NACK decision. When '1', if a received data element byte is written, and the receiver FIFO become full, the master send out NACK . if the reciever FIFO is full (the received data byte cannot be written), it stretch SCL(extend SCL low phase) until the receiver FIFO changes to not full, to write the last byte, then send out NACK. When '0', clock stretching is used instead (till the receiver FIFO is no longer full). Default Value: 1
8	M_READY_DATA_ACK	When '1', a received data element by the master is immediately ACK'd when the receiver FIFO is not full. Default Value: 1

14.1.12 SCB0_I2C_CTRL (continued)

7 : 4	LOW_PHASE_OVS	Serial I2C interface low phase oversampling factor. LOW_PHASE_OVS + 1 SCB clock periods constitute the low phase of a bit period. The valid range is [7, 15] with input signal median filtering and [6, 15] without input signal median filtering. The field is only used in master mode. In slave mode, the field is NOT used. However, there is a frequency requirement for the SCB clock wrt. the regular (no stretching) interface (IF) low time to guarantee functionally correct behavior. With input signal median filtering, the IF low time should be >= 8 SCB clock cycles and <= 16 IP clock cycles. Without input signal median filtering, the IF low time should be >= 7 SCB clock cycles and <= 16 SCB clock cycles. in slave mode, this field is used to define number of clk_scb cycles for tSU-DAT timing (from ACK/NACK/data ready, to SCL rising edge (released from I2C slave clock stretching)) Default Value: 8
3 : 0	HIGH_PHASE_OVS	Serial I2C interface high phase oversampling factor. HIGH_PHASE_OVS + 1 SCB clock periods constitute the high phase of a bit period. The valid range is [5, 15] with input signal median filtering and [4, 15] without input signal median filtering. The field is only used in master mode. In slave mode, the field is NOT used. However, there is a frequency requirement for the SCB clock wrt. the regular interface (IF) high time to guarantee functional correct behavior. With input signal median filtering, the IF high time should be >= 6 SCB clock cycles and <= 16 SCB clock cycles. Without input signal median filtering, the IF high time should be >= 5 SCB clock cycles and <= 16 SCB clock cycles. Default Value: 8

14.1.13 SCB0_I2C_STATUS

I2C status

Address: 0x40240064

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R	R	None	R	R	R
HW Access	None		W	W	None	W	W	W
Name	None [7:6]		M_READ	S_READ	None	I2CS_IC_BUSY	I2C_EC_BUSY	BUS_BUSY

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	CURR_EZ_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	BASE_EZ_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							R
HW Access	None							W
Name	None [31:25]							HS_MODE

Bits	Name	Description
24	HS_MODE	this is to indicate I2C Hs-mode transfer, it is set, after "Start, master-code, NACK"" pattern, for I2CM, at SCL falling edge, (INTR_M.I2C_HS_ENTER triggers), for I2CS_IC, at SCL falling edge, (INTR_S.I2C_HS_ENTER triggers), for I2CS_EC, at SCL rising edge, after 2-DFF synchronization delay, when CTRL.EC_AM =1, AND CTRL.EC_ACCESS =0, it is cleared when Stop pattern is detected, for I2CM, INTR_M.I2C_HS_EXIT triggers, for I2CS_IC, INTR_S.I2C_HS_EXIT triggers, for I2CS_EC, there is no respective interrupt. Default Value: 0
23 : 16	BASE_EZ_ADDR	I2C slave base EZ address. Address as provided by an I2C write transfer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable, as clock domain synchronization is not performed in the design. Default Value: Undefined

14.1.13 SCB0_I2C_STATUS (continued)

15 : 8	CURR_EZ_ADDR	I2C slave current EZ address. Current address pointer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable (during an ongoing transfer when I2C_EC_BUSY is '1'), as clock domain synchronization is not performed in the design. Default Value: Undefined
5	M_READ	I2C master read transfer ('1') or I2C master write transfer ('0'). When the I2C master is inactive/idle or transmitting START, REPEATED START, STOP or an address, this field is '0". Default Value: 0
4	S_READ	I2C slave read transfer ('1') or I2C slave write transfer ('0'). When the I2C slave is inactive/idle or receiving START, REPEATED START, STOP or an address, this field is '0". Default Value: 0
2	I2CS_IC_BUSY	Indicates whether the internally clocked slave logic is being accessed by external I2C master. --set at ADDR_MATCH --clear at START/RESET, STOP detection, or BUS_ERROR This bit can be used by SW to determine whether I2CS_IC is busy before entering DeepSleep. Default Value: 0
1	I2C_EC_BUSY	Indicates whether the externally clocked logic is potentially accessing the EZ memory and/or updating BASE_EZ_ADDR or CURR_EZ_ADDR (this is only possible in EZ mode). This bit can be used by SW to determine whether BASE_EZ_ADDR and CURR_EZ_ADDR are reliable. Default Value: Undefined
0	BUS_BUSY	I2C bus is busy. The bus is considered busy ('1'), from the time a START is detected or from the time the SCL line is '0'. The bus is considered idle ('0'), from the time a STOP is detected. If SCB block is disabled, BUS_BUSY is '0'. After enabling the block, it takes time for the BUS_BUSY to detect a busy bus. This time is the maximum high time of the SCL line. For a 100 kHz interface frequency, this maximum high time may last roughly 5 us (half a bit period). For single master systems, BUS_BUSY does not have to be used to detect an idle bus before a master starts a transfer using I2C_M_CMD.M_START (no bus collisions). For multi-master systems, BUS_BUSY can be used to detect an idle bus before a master starts a transfer using I2C_M_CMD.M_START_ON_IDLE (to prevent bus collisions). Default Value: 0

14.1.14 SCB0_I2C_M_CMD

I2C master command

Address: 0x40240068

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW	RW	RW	RW
HW Access	None			RW1C	RW1C	RW1C	RW1C	RW1C
Name	None [7:5]			M_STOP	M_NACK	M_ACK	M_START_ ON_IDLE	M_START

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4	M_STOP	When '1', attempt to transmit a STOP. When this action is performed, the hardware sets this field to '0'. I2C_M_CMD.M_START has a higher priority than this command: in situations where both a STOP and a REPEATED START could be transmitted, M_START takes precedence over M_STOP. Default Value: 0
3	M_NACK	for I2C master, the NACKed byte should be properly received. it write the data byte, before ACK/ NACK decision. When '1', attempt to transmit a negative acknowledgement (NACK). if the reciever FIFO is full (the received data byte cannot be written), it stretch SCL(extend SCL low phase) until the receiver FIFO changes to not full, to write the last byte, then send out NACK. When this action is performed, the hardware sets this field to '0'. Default Value: 0
2	M_ACK	When '1', attempt to transmit an acknowledgement (ACK). When this action is performed, the hardware sets this field to '0'. Default Value: 0

14.1.14 SCB0_I2C_M_CMD (continued)

1	M_START_ON_IDLE	When '1', transmit a START as soon as the bus is idle (I2C_STATUS.BUS_BUSY is '0', note that BUSY has a default value of '0'). For bus idle detection the hardware relies on STOP detection. As a result, bus idle detection is only functional after at least one I2C bus transfer has been detected on the bus (default/reset value of BUSY is '0') . A START is only transmitted when the master state machine is in the default state. When this action is performed, the hardware sets this field to '0'. Default Value: 0
0	M_START	When '1', transmit a START or REPEATED START. Whether a START or REPEATED START is transmitted depends on the state of the master state machine. A START is only transmitted when the master state machine is in the default state. A REPEATED START is transmitted when the master state machine is not in the default state, but is working on an ongoing transaction. The REPEATED START can only be transmitted after a NACK or ACK has been received for a transmitted data element or after a NACK has been transmitted for a received data element. When this action is performed, the hardware sets this field to '0'. Default Value: 0

14.1.15 SCB0_I2C_S_CMD

I2C slave command

Address: 0x4024006C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW	RW	RW
HW Access	None					R	RW1C	RW1C
Name	None [7:3]					S_TX-_ONES_ON_EMPTY	S_NACK	S_ACK

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							S_STRETCH_HS

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	S_STRETCH_HS	When '1', attempt to stretch SCL at time t1, SCL falling edge after "START, Master-code, NACK" pattern is detected. When I2C_CTRL.HS_ENABLED is set, it should be set; after wakeup from DeepSleep power mode, it should also be set. When INTR_S.I2C_HS_ENTER triggers, firmware configure clk_scb to meet I2C Hs-mode timing requirements, then firmware can clear this bit. Default Value: 0
2	S_TX_ONES_ON_EMPTY	When '1', attempt to send ones when TX_FIFO is empty. Once hardware starts to send ones, it will continue send ones until NACK is received, regardless of TX_FIFO status (even if new data is written into TX_FIFO). This bit is used to avoid stretching SCL, which is not expected for some master devices. Default Value: 0

14.1.15 SCB0_I2C_S_CMD (continued)

1	S_NACK	When '1', attempt to transmit a negative acknowledgement (NACK). When this action is performed, the hardware sets this field to '0'. In EZ mode, this field should be set to '0' (it is only to be used in non EZ mode). This command has a higher priority than I2C_S_CMD.S_ACK, I2C_CTRL.S_READY_ADDR_ACK or I2C_CTRL.S_READY_DATA_ACK. Default Value: 0
0	S_ACK	When '1', attempt to transmit an acknowledgement (ACK). When this action is performed, the hardware sets this field to '0'. In EZ mode, this field should be set to '0' (it is only to be used in non EZ mode). Default Value: 0

14.1.16 SCB0_I2C_CFG

I2C configuration

Address: 0x40240070

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	None		RW	
HW Access	None			R	None		R	
Name	None [7:5]			SDA_IN_-FILT_SEL	None [3:2]		SDA_IN_FILT_TRIM [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None			RW	None		RW	
HW Access	None			R	None		R	
Name	None [15:13]			SCL_IN_-FILT_SEL	None [11:10]		SCL_IN_FILT_TRIM [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW		RW		RW	
HW Access	None		R		R		R	
Name	None [23:22]		SDA_OUT_FILT2_TRIM [21:20]		SDA_OUT_FILT1_TRIM [19:18]		SDA_OUT_FILT0_TRIM [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None		RW		None			
HW Access	None		R		None			
Name	None [31:30]		SDA_OUT_FILT_SEL [29:28]		None [27:24]			

Bits	Name	Description
29 : 28	SDA_OUT_FILT_SEL	Selection of cumulative filter delay on SDA output to meet tHD_DAT parameter "0": 0 ns. "1": 50 ns (filter 0 enabled). "2": 100 ns (filters 0 and 1 enabled). "3": 150 ns (filters 0, 1 and 2 enabled). Default Value: 0
21 : 20	SDA_OUT_FILT2_TRIM	Trim settings for the 50ns delay filter on SDA output used to guarantee tHD_DAT I2C parameter. Default setting meets the I2C spec. Programmability available if required Default Value: 2
19 : 18	SDA_OUT_FILT1_TRIM	Trim settings for the 50ns delay filter on SDA output used to guarantee tHD_DAT I2C parameter. Default setting meets the I2C spec. Programmability available if required Default Value: 2
17 : 16	SDA_OUT_FILT0_TRIM	Trim settings for the 50ns delay filter on SDA output used to guarantee tHD_DAT I2C parameter. Default setting meets the I2C spec. Programmability available if required Default Value: 2

14.1.16 SCB0_I2C_CFG (continued)

12	SCL_IN_FILT_SEL	Enable for 50ns glitch filter on SCL input '0': 0 ns. '1: 50 ns (filter enabled). Default Value: 1
9 : 8	SCL_IN_FILT_TRIM	Trim settings for the 50ns glitch filter on the SDA input. Default setting meets the I2C glitch rejections specs. Programmability available if required Default Value: 0
4	SDA_IN_FILT_SEL	Enable for 50ns glitch filter on SDA input '0': 0 ns. '1: 50 ns (filter enabled). Default Value: 1
1 : 0	SDA_IN_FILT_TRIM	Trim settings for the 50ns glitch filter on the SDA input. Default setting meets the I2C glitch rejections specs. Programmability available if required Default Value: 3

14.1.17 SCB0_I2C_STRETCH_CTRL

I2C stretch control

Address: 0x40240074

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				STRETCH_THRESHOLD [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	STRETCH_THRESHOLD	stretch threthold. Typically it is the SCL turaound delay (including IO cell delay, SCL rise time, analog filter delay), in number of clk_scb cycles. When STRETCH_COUNT is higher than this STRETCH_THRESHOLD, STRETCH_DETECTED will be set. STRETCH_DETECTED should be less than "HOVS-2", HOVS means I2C_CTRL.HIGH_PHASE_OVS, or I2C_CTRL_HS.HOVS_HS. Default Value: 0

14.1.18 SCB0_I2C_STRETCH_STATUS

I2C stretch status

Address: 0x40240078

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R	R	R			
HW Access	None		W	W	W			
Name	None [7:6]		SYNC_DE-TECTED	STRETCH_ DETECTED	STRETCH_COUNT [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							R
HW Access	None							W
Name	None [15:9]							STRETCH-ING

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
8	STRETCHING	I2C SCL is stretched by this block (DUT), for I2C master, this can happen when TX FIFO is empty, or RX_FIFO is full, or ACK/NACK is not decided, or RESTART/STOP is not decided. For I2C slave, this can heppend, TX FIFO is empty, or RX_FIFO is full, or ACK/NACK is not decided. Default Value: 0
5	SYNC_DETECTED	synchronization detected. Set when I2C falling edge comes in earler than expected (suppressed by another I2C master during synchronization). Default Value: 0
4	STRETCH_DETECTED	stretch detected. Set when I2C rising edge comes later than expected (suppressed by another master or slave), and STRETCH_COUNT is higher than STRETCH_THRESHOLD. Default Value: 0

14.1.18 SCB0_I2C_STRETCH_STATUS (continued)

3 : 0	STRETCH_COUNT	stretch count. Started when I2C device start to drive high phase on internal SCL output signal, stalled when it detected high level on SCL input signal. Default Value: 0

14.1.19 SCB0_I2C_CTRL_HS

I2C control for High-Speed mode

Address: 0x40240080

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW				RW			
HW Access	R				R			
Name	LOVS_HS [7:4]				HOVS_HS [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	HS_EN-ABLED	None [30:24]						

Bits	Name	Description
31	HS_ENABLED	0': I2C Hs-mode is disabled, '1': I2C Hs-mode is enabled, when I2C Hs-mode is disabled and the IP is in I2C slave mode, hardware response to incoming Hs-mode transfers are undefined. When I2C Hs-mode is disabled and the IP is in I2C master mode, firmware should not generate Hs-mode transfers. Default Value: 0
7 : 4	LOVS_HS	Serial I2C interface low phase oversampling factor for I2C Hs-mode. LOVS_HS + 1 peripheral clock periods constitute the low phase of a bit period. Hardware switch from I2C_CTRL.LOW_PHASE_OVS to this value automacitcally, at time t1; and switch back time tFS (when STOP detected). Firmware configure clk_scb frequency properly between t1 and tH. Default Value: 8

14.1.19 SCB0_I2C_CTRL_HS (continued)

3 : 0	HOVS_HS	Serial I2C interface high phase oversampling factor for I2C Hs-mode. HOVS_HS + 1 peripheral clock periods constitute the high phase of a bit period. Hardware switch from I2C_CTRL.HIGH_PHASE_OVS to this value automacitcally, at time t1; and switch back time tFS (when STOP detected). Firmware configure clk_scb frequency properly between t1 and tH. Default Value: 8

14.1.20 SCB0_TX_CTRL

Transmitter control

Address: 0x40240200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			R				
Name	None [7:5]			DATA_WIDTH [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None							RW
HW Access	None							R
Name	None [15:9]							MSB_-FIRST

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [23:18]						OPEN_DRAIN_SCL	OPEN_DRAIN

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description

14.1.20 SCB0_TX_CTRL (continued)

17	OPEN_DRAIN_SCL	Each IO cell "xxx" has two associated IP output signals "xxx_out_en" and "xxx_out". '0': Normal operation mode. Typically, this operation mode is used for IO cells that are connected to (board) wires/lines that are driven by a single IO cell. In this operation mode, for an IO cell "xxx" that is used as an output, the "xxx_out_en" output enable signal is typically constant '1' the "xxx_out" output is the outputted value. In other words, in normal operation mode, the "xxx_out" output is used to control the IO cell output value: "xxx_out" is '0' to drive an IO cell output value of '0' and "xxx_out" is '1' to drive an IO cell output value of '1'. '1': Open drain operation mode. Typically this operation mode is used for IO cells that are connected to (board) wires/lines that are driven by multiple IO cells (possibly on multiple chips). In this operation mode, for and IO cell "xxx" that is used as an output, the "xxx_out_en" output controls the outputted value. Typically, open drain operation mode drives low/'0' and the "xxx_out" output is constant '1'. In other words, in open drain operation mode, the "xxx_out_en" output is used to control the IO cell output value: in drive low/'0' mode: "xxx_out_en" is '1' (drive enabled) to drive an IO cell output value of '0' and "xxx_out_en" is '1' (drive disabled) to not drive an IO cell output value (another IO cell can drive the wire/line or a pull up results in a wire/line value '1'). this bit is applicable to I2C SCL only. I2C SDA always work in open-drain mode. this is not applicable to M0S8, which does not need special control in SCB for open-drain drive mode. Default Value: 1
16	OPEN_DRAIN	Each IO cell "xxx" has two associated IP output signals "xxx_out_en" and "xxx_out". '0': Normal operation mode. Typically, this operation mode is used for IO cells that are connected to (board) wires/lines that are driven by a single IO cell. In this operation mode, for an IO cell "xxx" that is used as an output, the "xxx_out_en" output enable signal is typically constant '1' the "xxx_out" output is the outputted value. In other words, in normal operation mode, the "xxx_out" output is used to control the IO cell output value: "xxx_out" is '0' to drive an IO cell output value of '0' and "xxx_out" is '1' to drive an IO cell output value of '1'. '1': Open drain operation mode. Typically this operation mode is used for IO cells that are connected to (board) wires/lines that are driven by multiple IO cells (possibly on multiple chips). In this operation mode, for and IO cell "xxx" that is used as an output, the "xxx_out_en" output controls the outputted value. Typically, open drain operation mode drives low/'0' and the "xxx_out" output is constant '1'. In other words, in open drain operation mode, the "xxx_out_en" output is used to control the IO cell output value: in drive low/'0' mode: "xxx_out_en" is '1' (drive enabled) to drive an IO cell output value of '0' and "xxx_out_en" is '1' (drive disabled) to not drive an IO cell output value (another IO cell can drive the wire/line or a pull up results in a wire/line value '1'). The open drain mode is supported for: - UART mode, "uart_tx" IO cell. - SPI mode, "spi_miso" IO cell. this bit is not applicable to I2C mode, "i2c_scl" and "i2c_sda" IO cells. Default Value: 0
8	MSB_FIRST	Least significant bit first ('0') or most significant bit first ('1'). For I2C, this field should be '1'. Default Value: 1
4 : 0	DATA_WIDTH	Dataframe width, depending on CTRL.MEM_WIDTH. DATA_WIDTH + 1 is the amount of bits in a transmitted data frame. This number does not include start, parity and stop bits. For UART mode, the valid range is [3, 8]. For SPI, the valid range is [3, 31]. For I2C the only valid value is 7. In EZ mode (for both SPI and I2C), the only valid value is 7. Default Value: 7

14.1.21 SCB0_TX_FIFO_CTRL

Transmitter FIFO control

Address: 0x40240204

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				TRIGGER_LEVEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [23:18]						FREEZE	CLEAR

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
17	FREEZE	When '1', hardware reads from the transmitter FIFO do not remove FIFO entries. Freeze will not advance the TX FIFO read pointer. Default Value: 0
16	CLEAR	When '1', the transmitter FIFO and transmitter shift register are cleared/invalidated. Invalidation will last for as long as this field is '1'. If a quick clear/invalidation is required, the field should be set to '1' and be followed by a set to '0'. If a clear/invalidation is required for an extended time period, the field should be set to '1' during the complete time period. Default Value: 0
3 : 0	TRIGGER_LEVEL	Trigger level. When the transmitter FIFO has less entries than the number of this field, a transmitter trigger event INTR_TX.TRIGGER is generated. Default Value: 0

14.1.22 SCB0_TX_FIFO_STATUS

Transmitter FIFO status

Address: 0x40240208

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R			
HW Access	None				W			
Name	None [7:5]				USED [4:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	R	None						
HW Access	W	None						
Name	SR_VALID	None [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	None				R			
HW Access	None				W			
Name	None [23:20]				RD_PTR [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None				R			
HW Access	None				W			
Name	None [31:28]				WR_PTR [27:24]			

Bits	Name	Description
27 : 24	WR_PTR	FIFO write pointer: FIFO location at which a new data frame is written. Default Value: 0
19 : 16	RD_PTR	FIFO read pointer: FIFO location from which a data frame is read by the hardware. Default Value: 0
15	SR_VALID	Indicates whether the TX shift registers holds a valid data frame ('1') or not ('0'). The shift register can be considered the top of the TX FIFO (the data frame is not included in the USED field of the TX FIFO). The shift register is a working register and holds the data frame that is currently transmitted (when the protocol state machine is transmitting a data frame) or the data frame that is transmitted next (when the protocol state machine is not transmitting a data frame). Default Value: 0
4 : 0	USED	Amount of entries in the transmitter FIFO. The value of this field ranges from 0 to FF_DATA_NR (EZ_DATA_NR/2). Default Value: 0

14.1.23 SCB0_TX_FIFO_WR

Transmitter FIFO write

Address: 0x40240240

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	W							
HW Access	R							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	W							
HW Access	R							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	W							
HW Access	R							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	W							
HW Access	R							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data frame written into the transmitter FIFO. Behavior is similar to that of a PUSH operation. Note that when CTRL.MEM_WIDTH is "0", only DATA[7:0] are used and when CTRL.MEM_WIDTH is "1", only DATA[15:0] are used. A write to a full TX FIFO sets INTR_TX.OVERFLOW to '1'. Default Value: 0

14.1.24 SCB0_RX_CTRL

Receiver control

Address: 0x40240300

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			R				
Name	None [7:5]			DATA_WIDTH [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [15:10]						MEDIAN	MSB_-FIRST

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	MEDIAN	Median filter. When '1', a digital 3 taps median filter is performed on input interface lines. This filter should reduce the susceptibility to errors. However, its requires higher oversampling values. For UART IrDA submode, this field should always be '1'. Default Value: 0
8	MSB_FIRST	Least significant bit first ('0') or most significant bit first ('1'). For I2C, this field should be '1'. Default Value: 1
4 : 0	DATA_WIDTH	Dataframe width, depending on CTRL.MEM_WIDTH. DATA_WIDTH + 1 is the expected amount of bits in received data frame. This number does not include start, parity and stop bits. For UART mode, the valid range is [3, 8]. For SPI, the valid range is [3, 31]. For I2C the only valid value is 7. In EZ mode (for both SPI and I2C), the only valid value is 7. Default Value: 7

14.1.25 SCB0_RX_FIFO_CTRL

Receiver FIFO control

Address: 0x40240304

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				TRIGGER_LEVEL [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [23:18]						FREEZE	CLEAR

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
17	FREEZE	When '1', hardware writes to the receiver FIFO have no effect. Freeze will not advance the RX FIFO write pointer. Default Value: 0
16	CLEAR	When '1', the receiver FIFO and receiver shift register are cleared/invalidated. Invalidation will last for as long as this field is '1'. If a quick clear/invalidation is required, the field should be set to '1' and be followed by a set to '0'. If a clear/invalidation is required for an extended time period, the field should be set to '1' during the complete time period. Default Value: 0
3 : 0	TRIGGER_LEVEL	Trigger level. When the receiver FIFO has more entries than the number of this field, a receiver trigger event INTR_RX.TRIGGER is generated. Default Value: 0

14.1.26 SCB0_RX_FIFO_STATUS

Receiver FIFO status

Address: 0x40240308

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R			
HW Access	None				W			
Name	None [7:5]				USED [4:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	R	None						
HW Access	W	None						
Name	SR_VALID	None [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	None				R			
HW Access	None				W			
Name	None [23:20]				RD_PTR [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	None				R			
HW Access	None				W			
Name	None [31:28]				WR_PTR [27:24]			

Bits	Name	Description
27 : 24	WR_PTR	FIFO write pointer: FIFO location at which a new data frame is written by the hardware. Default Value: 0
19 : 16	RD_PTR	FIFO read pointer: FIFO location from which a data frame is read. Default Value: 0
15	SR_VALID	Indicates whether the RX shift registers holds a (partial) valid data frame ('1') or not ('0'). The shift register can be considered the bottom of the RX FIFO (the data frame is not included in the USED field of the RX FIFO). The shift register is a working register and holds the data frame that is currently being received (when the protocol state machine is receiving a data frame). Default Value: 0
4 : 0	USED	Amount of entries in the receiver FIFO. The value of this field ranges from 0 to FF_DATA_NR (EZ_DATA_NR/2). Default Value: 0

14.1.27 SCB0_RX_MATCH

Slave address and mask

Address: 0x40240310

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	ADDR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	MASK [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	MASK	Slave device address mask. This field is a mask that specifies which of the slave address bits take part in the matching. MATCH = ((ADDR & MASK) == ("slave address" & MASK)). Default Value: 0
7 : 0	ADDR	Slave device address. In UART multi-processor mode, all 8 bits are used. In I2C slave mode, only bits 7 down to 1 are used. This reflects the organization of the first transmitted byte in a I2C transfer: the first 7 bits represent the address of the addressed slave, and the last 1 bit is a read/write indicator ('0': write, '1': read). Default Value: 0

14.1.28 SCB0_RX_FIFO_RD

Receiver FIFO read

Address: 0x40240340

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data read from the receiver FIFO. Reading a data frame will remove the data frame from the FIFO; i.e. behavior is similar to that of a POP operation. Note that when CTRL.MEM_WIDTH is "0", only DATA[7:0] are used and when CTRL.MEM_WIDTH is "1", only DATA[15:0] are used A read from an empty RX FIFO sets INTR_RX.UNDERFLOW to '1'. When this register is read through the debugger, the data frame will not be removed from the FIFO. Similar in operation to RX_FIFO_RD_SILENT Default Value: Undefined

14.1.29 SCB0_RX_FIFO_RD_SILENT

Receiver FIFO read silent

Address: 0x40240344

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Data read from the receiver FIFO. Reading a data frame will NOT remove the data frame from the FIFO; i.e. behavior is similar to that of a PEEK operation. Note that when CTRL.MEM_WIDTH is "0", only DATA[7:0] are used and when CTRL.MEM_WIDTH is "1", only DATA[15:0] are used A read from an empty RX FIFO sets INTR_RX.UNDERFLOW to '1'. Default Value: Undefined

14.1.30 SCB0_EZ_DATA0

Memory buffer

Address: 0x40240400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	EZ_DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	EZ_DATA	Data in buffer memory location. In case of a blocked discarded access, a read access returns 0xffff:ffff and a write access is dropped. Note that the 0xffff:ffff value is unique (not a legal EZ_-DATA byte value) and can be detected by SW. Note that a discarded write access can be detected by reading back the written value. Default Value: Undefined

14.1.31 SCB0_INTR_CAUSE

Active clocked interrupt signal

Address: 0x40240E00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R	R	R	R	R	R
HW Access	None		W	W	W	W	W	W
Name	None [7:6]		SPI_EC	I2C_EC	RX	TX	S	M

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	SPI_EC	Externally clocked SPI interrupt active ("interrupt_spi_ec"): INTR_SPI_EC_MASKED != 0. Default Value: 0
4	I2C_EC	Externally clock I2C interrupt active ("interrupt_i2c_ec"): INTR_I2C_EC_MASKED != 0. Default Value: 0
3	RX	Receiver interrupt active ("interrupt_rx"): INTR_RX_MASKED != 0. Default Value: 0
2	TX	Transmitter interrupt active ("interrupt_tx"): INTR_TX_MASKED != 0. Default Value: 0
1	S	Slave interrupt active ("interrupt_slave"): INTR_S_MASKED != 0. Default Value: 0
0	M	Master interrupt active ("interrupt_master"): INTR_M_MASKED != 0. Default Value: 0

14.1.32 SCB0_INTR_I2C_EC

Externally clocked I2C interrupt request

Address: 0x40240E80

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1C	RW1C	RW1C	RW1C
HW Access	None				A	A	A	A
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	STOP detection after a read transfer occurred. Activated on the end of a read transfer (I2C STOP). This event is an indication that a buffer memory location has been read from. Only available for a slave request with an address match, in EZ and CMD_RESP modes, when CTRL.EC_OP_MODE is '1'. Default Value: 0
2	EZ_WRITE_STOP	STOP detection after a write transfer occurred. Activated on the end of a write transfer (I2C STOP). This event is an indication that a buffer memory location has been written to. For EZ mode: a transfer that only writes the base address does NOT activate this event. Only available for a slave request with an address match, in EZ and CMD_RESP modes, when CTRL.EC_OP_MODE is '1'. Default Value: 0
1	EZ_STOP	STOP detection. Activated on the end of a every transfer (I2C STOP). Only available for a slave request with an address match, in EZ and CMD_RESP modes, when CTRL.EC_OP_MODE is '1'. Default Value: 0

14.1.32 SCB0_INTR_I2C_EC (continued)

0	WAKE_UP	Wake up request. Active on incoming slave request (with address match). Only used when CTRL.EC_AM_MODE is '1'. Default Value: 0

14.1.33 SCB0_INTR_I2C_EC_MASK

Externally clocked I2C interrupt mask

Address: 0x40240E88

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	EZ_WRITE_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	EZ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	WAKE_UP	Mask bit for corresponding bit in interrupt request register. Default Value: 0

14.1.34 SCB0_INTR_I2C_EC_MASKED

Externally clocked I2C interrupt masked

Address: 0x40240E8C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R	R	R	R
HW Access	None				W	W	W	W
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
2	EZ_WRITE_STOP	Logical and of corresponding request and mask bits. Default Value: 0
1	EZ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
0	WAKE_UP	Logical and of corresponding request and mask bits. Default Value: 0

14.1.35 SCB0_INTR_SPI_EC

Externally clocked SPI interrupt request

Address: 0x40240EC0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1C	RW1C	RW1C	RW1C
HW Access	None				A	A	A	A
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	STOP detection after a read transfer occurred. Activated on the end of a read transfer (SPI de-selection). This event is an indication that a buffer memory location has been read from. Only used in EZ and CMD_RESP modes and when CTRL.EC_OP_MODE is '1'. Default Value: 0
2	EZ_WRITE_STOP	STOP detection after a write transfer occurred. Activated on the end of a write transfer (SPI de-selection). This event is an indication that a buffer memory location has been written to. For EZ mode: a transfer that only writes the base address does NOT activate this event. Only used in EZ and CMD_RESP modes and when CTRL.EC_OP_MODE is '1'. Default Value: 0
1	EZ_STOP	STOP detection. Activated on the end of a every transfer (SPI deselection). Only available in EZ and CMD_RESP mode and when CTRL.EC_OP_MODE is '1'. Default Value: 0

14.1.35 SCB0_INTR_SPI_EC (continued)

0	WAKE_UP	Wake up request. Active on incoming slave request when externally clocked selection is '1'. Only used when CTRL.EC_AM_MODE is '1'. Default Value: 0

14.1.36 SCB0_INTR_SPI_EC_MASK

Externally clocked SPI interrupt mask

Address: 0x40240EC8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	EZ_WRITE_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	EZ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	WAKE_UP	Mask bit for corresponding bit in interrupt request register. Default Value: 0

14.1.37 SCB0_INTR_SPI_EC_MASKED

Externally clocked SPI interrupt masked

Address: 0x40240ECC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R	R	R	R
HW Access	None				W	W	W	W
Name	None [7:4]				EZ_READ_STOP	EZ_WRITE_STOP	EZ_STOP	WAKE_UP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	EZ_READ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
2	EZ_WRITE_STOP	Logical and of corresponding request and mask bits. Default Value: 0
1	EZ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
0	WAKE_UP	Logical and of corresponding request and mask bits. Default Value: 0

14.1.38 SCB0_INTR_M

Master interrupt request

Address: 0x40240F00

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW1C	None	RW1C	RW1C	RW1C
HW Access	None			RW1S	None	RW1S	RW1S	RW1S
Name	None [7:5]			I2C_STOP	None	I2C_ACK	I2C_NACK	I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW1C	RW1C
HW Access	None						RW1S	RW1S
Name	None [15:10]						SPI_DONE	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None						RW1C	RW1C
HW Access	None						RW1S	RW1S
Name	None [31:26]						I2C_HS_EXIT	I2C_HS_ENTER

Bits	Name	Description
25	I2C_HS_EXIT	exited I2C Hs-mode, after STOP detection. Default Value: 0
24	I2C_HS_ENTER	entered I2C Hs-mode, at time t1, SCL falling edge after "START, 8-bit master code (0000_1XXX), NACK" sequence. Default Value: 0
9	SPI_DONE	SPI master transfer done event: all data frames in the transmit FIFO are sent, the transmit FIFO is empty (both TX FIFO and transmit shifter register are empty), and SPI select output pin is de-selected. Default Value: 0
8	I2C_BUS_ERROR	I2C master bus error (unexpected detection of START or STOP condition). Default Value: 0
4	I2C_STOP	I2C master STOP. Set to '1', when the master has transmitted a STOP. Default Value: 0

14.1.38 SCB0_INTR_M (continued)

2	I2C_ACK	I2C master acknowledgement. Set to '1', when the master receives a ACK (typically after the master transmitted the slave address or TX data). Default Value: 0
1	I2C_NACK	I2C master negative acknowledgement. Set to '1', when the master receives a NACK (typically after the master transmitted the slave address or TX data). Default Value: 0
0	I2C_ARB_LOST	I2C master lost arbitration: the value driven by the master on the SDA line is not the same as the value observed on the SDA line. The Firmware should clear the TX FIFO, to re-do this transfer. Default Value: 0

14.1.39 SCB0_INTR_M_SET

Master interrupt set request

Address: 0x40240F04

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW1S	None	RW1S	RW1S	RW1S
HW Access	None			A	None	A	A	A
Name	None [7:5]			I2C_STOP	None	I2C_ACK	I2C_NACK	I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW1S	RW1S
HW Access	None						A	A
Name	None [15:10]						SPI_DONE	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None						RW1S	RW1S
HW Access	None						A	A
Name	None [31:26]						I2C_HS_EXIT	I2C_HS_ENTER

Bits	Name	Description
25	I2C_HS_EXIT	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
24	I2C_HS_ENTER	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
9	SPI_DONE	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
8	I2C_BUS_ERROR	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
4	I2C_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
2	I2C_ACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
1	I2C_NACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

14.1.39 SCB0_INTR_M_SET (continued)

0	I2C_ARB_LOST	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

14.1.40 SCB0_INTR_M_MASK

Master interrupt mask

Address: 0x40240F08

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	None	RW	RW	RW
HW Access	None			R	None	R	R	R
Name	None [7:5]			I2C_STOP	None	I2C_ACK	I2C_NACK	I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [15:10]						SPI_DONE	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [31:26]						I2C_HS_EXIT	I2C_HS_ENTER

Bits	Name	Description
25	I2C_HS_EXIT	Mask bit for corresponding bit in interrupt request register. Default Value: 0
24	I2C_HS_ENTER	Mask bit for corresponding bit in interrupt request register. Default Value: 0
9	SPI_DONE	Mask bit for corresponding bit in interrupt request register. Default Value: 0
8	I2C_BUS_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
4	I2C_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	I2C_ACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	I2C_NACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0

14.1.40 SCB0_INTR_M_MASK (continued)

0	I2C_ARB_LOST	Mask bit for corresponding bit in interrupt request register. Default Value: 0

14.1.41 SCB0_INTR_M_MASKED

Master interrupt masked request

Address: 0x40240F0C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			R	None	R	R	R
HW Access	None			W	None	W	W	W
Name	None [7:5]			I2C_STOP	None	I2C_ACK	I2C_NACK	I2C_ARB_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None						R	R
HW Access	None						W	W
Name	None [15:10]						SPI_DONE	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None						R	R
HW Access	None						W	W
Name	None [31:26]						I2C_HS_EXIT	I2C_HS_ENTER

Bits	Name	Description
25	I2C_HS_EXIT	Logical and of corresponding request and mask bits. Default Value: 0
24	I2C_HS_ENTER	Logical and of corresponding request and mask bits. Default Value: 0
9	SPI_DONE	Logical and of corresponding request and mask bits. Default Value: 0
8	I2C_BUS_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
4	I2C_STOP	Logical and of corresponding request and mask bits. Default Value: 0
2	I2C_ACK	Logical and of corresponding request and mask bits. Default Value: 0
1	I2C_NACK	Logical and of corresponding request and mask bits. Default Value: 0

14.1.41 SCB0_INTR_M_MASKED (continued)

0	I2C_ARB_LOST	Logical and of corresponding request and mask bits. Default Value: 0

14.1.42 SCB0_INTR_S

Slave interrupt request

Address: 0x40240F40

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
Name	I2C_GEN-ERAL	I2C_AD-DR_MATCH	I2C_START	I2C_STOP	I2C_WRITE_STOP	I2C_ACK	I2C_NACK	I2C_AR-B_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW1C	RW1C	RW1C	RW1C
HW Access	None				RW1S	RW1S	RW1S	RW1S
Name	None [15:12]				SPI_BUS_ERROR	SPI_EZ_STOP	SPI_EZ_WRITE_STOP	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW1C
HW Access	None							RW1S
Name	None [23:17]							I2C_RE-START

Bits	31	30	29	28	27	26	25	24
SW Access	None						RW1C	RW1C
HW Access	None						RW1S	RW1S
Name	None [31:26]						I2C_HS_EXIT	I2C_HS_ENTER

Bits	Name	Description
25	I2C_HS_EXIT	exited I2C Hs-mode, after STOP detection. Default Value: 0
24	I2C_HS_ENTER	entered I2C Hs-mode, at time t1, SCL falling edge after "START, 8-bit master code (0000_1XXX), NACK" sequence. Default Value: 0
16	I2C_RESTART	I2C slave RESTART received. Set to '1', when REPEATED START event is detected. In the case of externally clocked address matching (CTRL.EC_AM_MODE is '1') AND clock stretching is performed (I2C_CTRL.S_NOT_READY_ADDR_NACK is '0'), this field is NOT set. this is not applicable when address in previous transfer is master-code. Default Value: 0

14.1.42 SCB0_INTR_S (continued)

11	SPI_BUS_ERROR	SPI slave deselected at an unexpected time in the SPI transfer. The Firmware may decide to clear the TX and RX FIFOs in case of this error. Default Value: 0
10	SPI_EZ_STOP	SPI slave deselected after any EZ SPI transfer occurred. Default Value: 0
9	SPI_EZ_WRITE_STOP	SPI slave deselected after a write EZ SPI transfer occurred. Default Value: 0
8	I2C_BUS_ERROR	I2C slave bus error (unexpected detection of START or STOP condition). This should not occur, it represents erroneous I2C bus behavior. In case of a bus error, the I2C slave state machine abort the ongoing transfer. The Firmware may decide to clear the TX and RX FIFOs in case of this error. Default Value: 0
7	I2C_GENERAL	I2C slave general call address received. If CTRL.ADDR_ACCEPT, the received address 0x00 (including the R/W bit) is available in the RX FIFO. In the case of externally clocked address matching (CTRL.EC_AM_MODE is '1') and internally clocked operation (CTRL.EC_OP_MODE is '0'), this field is set when the event is detected. Default Value: 0
6	I2C_ADDR_MATCH	I2C slave matching address received. If CTRL.ADDR_ACCEPT, the received address (including the R/W bit) is available in the RX FIFO. In the case of externally clocked address matching (CTRL.EC_AM_MODE is '1') and internally clocked operation (CTRL.EC_OP_MODE is '0'), this field is set when the event is detected. Default Value: 0
5	I2C_START	I2C slave START received. Set to '1', when START or REPEATED START event is detected. In the case of externally clocked address matching (CTRL.EC_AM_MODE is '1') AND clock stretching is performed (I2C_CTRL.S_NOT_READY_ADDR_NACK is '0'), this field is NOT set. The Firmware should use INTR_S_EC.WAKE_UP, INTR_S.I2C_ADDR_MATCH and INTR_S.I2C_GENERAL. Default Value: 0
4	I2C_STOP	I2C STOP event for I2C (read or write) transfer intended for this slave (address matching is performed). Set to '1', when STOP or REPEATED START event is detected. The REPEATED START event is included in this interrupt cause such that the I2C transfers separated by a REPEATED START can be distinguished and potentially treated separately by the Firmware. Note that the second I2C transfer (after a REPEATED START) may be to a different slave address. The event is detected on any I2C transfer intended for this slave. Note that a I2C address intended for the slave (address is matching) will result in a I2C_STOP event independent of whether the I2C address is ACK'd or NACK'd. this is not applicable when address in previous transfer is master-code. Default Value: 0

14.1.42 SCB0_INTR_S (continued)

3	I2C_WRITE_STOP	I2C STOP event for I2C write transfer intended for this slave (address matching is performed). Set to '1', when STOP or REPEATED START event is detected. The REPEATED START event is included in this interrupt cause such that the I2C transfers separated by a REPEATED START can be distinguished and potentially treated separately by the Firmware. Note that the second I2C transfer (after a REPEATED START) may be to a different slave address. In non EZ mode, the event is detected on any I2C write transfer intended for this slave. Note that a I2C write address intended for the slave (address is matching and a it is a write transfer) will result in a I2C_WRITE_STOP event independent of whether the I2C address is ACK'd or NACK'd. In EZ mode, the event is detected only on I2C write transfers that have EZ data written to the memory structure (an I2C write transfer that only communicates an I2C address and EZ address, will not result in this event being detected). this is not applicable when address in previous transfer is master-code. Default Value: 0
2	I2C_ACK	I2C slave acknowledgement received. Set to '1', when the slave receives a ACK (typically after the slave transmitted TX data). Default Value: 0
1	I2C_NACK	I2C slave negative acknowledgement received. Set to '1', when the slave receives a NACK (typically after the slave transmitted TX data). Default Value: 0
0	I2C_ARB_LOST	I2C slave lost arbitration: the value driven on the SDA line is not the same as the value observed on the SDA line (while the SCL line is '1'). This should not occur, it represents erroneous I2C bus behavior. In case of lost arbitration, the I2C slave state machine aborts the ongoing transfer. The Firmware may decide to clear the TX and RX FIFOs in case of this error. Default Value: 0

14.1.43 SCB0_INTR_S_SET

Slave interrupt set request

Address: 0x40240F44

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	A	A	A	A	A	A	A	A
Name	I2C_GEN-ERAL	I2C_AD-DR_MATCH	I2C_START	I2C_STOP	I2C_WRITE_STOP	I2C_ACK	I2C_NACK	I2C_AR-B_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW1S	RW1S	RW1S	RW1S
HW Access	None				A	A	A	A
Name	None [15:12]				SPI_BUS_ERROR	SPI_EZ_STOP	SPI_EZ_WRITE_STOP	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW1S
HW Access	None							A
Name	None [23:17]							I2C_RE-START

Bits	31	30	29	28	27	26	25	24
SW Access	None						RW1S	RW1S
HW Access	None						A	A
Name	None [31:26]						I2C_HS_EXIT	I2C_HS_ENTER

Bits	Name	Description
25	I2C_HS_EXIT	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
24	I2C_HS_ENTER	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
16	I2C_RESTART	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
11	SPI_BUS_ERROR	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
10	SPI_EZ_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
9	SPI_EZ_WRITE_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

14.1.43 SCB0_INTR_S_SET (continued)

8	I2C_BUS_ERROR	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
7	I2C_GENERAL	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
6	I2C_ADDR_MATCH	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
5	I2C_START	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
4	I2C_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
3	I2C_WRITE_STOP	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
2	I2C_ACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
1	I2C_NACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	I2C_ARB_LOST	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

14.1.44 SCB0_INTR_S_MASK

Slave interrupt mask

Address: 0x40240F48

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	I2C_GEN-ERAL	I2C_AD-DR_MATCH	I2C_START	I2C_STOP	I2C_WRITE_STOP	I2C_ACK	I2C_NACK	I2C_AR-B_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [15:12]				SPI_BUS_ERROR	SPI_EZ_STOP	SPI_EZ_WRITE_STOP	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							RW
HW Access	None							R
Name	None [23:17]							I2C_RE-START

Bits	31	30	29	28	27	26	25	24
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [31:26]						I2C_HS_EXIT	I2C_HS_ENTER

Bits	Name	Description
25	I2C_HS_EXIT	Mask bit for corresponding bit in interrupt request register. Default Value: 0
24	I2C_HS_ENTER	Mask bit for corresponding bit in interrupt request register. Default Value: 0
16	I2C_RESTART	Mask bit for corresponding bit in interrupt request register. Default Value: 0
11	SPI_BUS_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
10	SPI_EZ_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
9	SPI_EZ_WRITE_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0

14.1.44 SCB0_INTR_S_MASK (continued)

8	I2C_BUS_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
7	I2C_GENERAL	Mask bit for corresponding bit in interrupt request register. Default Value: 0
6	I2C_ADDR_MATCH	Mask bit for corresponding bit in interrupt request register. Default Value: 0
5	I2C_START	Mask bit for corresponding bit in interrupt request register. Default Value: 0
4	I2C_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
3	I2C_WRITE_STOP	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	I2C_ACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	I2C_NACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	I2C_ARB_LOST	Mask bit for corresponding bit in interrupt request register. Default Value: 0

14.1.45 SCB0_INTR_S_MASKED

Slave interrupt masked request

Address: 0x40240F4C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	I2C_GEN-ERAL	I2C_AD-DR_MATCH	I2C_START	I2C_STOP	I2C_WRITE_STOP	I2C_ACK	I2C_NACK	I2C_AR-B_LOST

Bits	15	14	13	12	11	10	9	8
SW Access	None				R	R	R	R
HW Access	None				W	W	W	W
Name	None [15:12]				SPI_BUS_ERROR	SPI_EZ_STOP	SPI_EZ_WRITE_STOP	I2C_BUS_ERROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							R
HW Access	None							W
Name	None [23:17]							I2C_RE-START

Bits	31	30	29	28	27	26	25	24
SW Access	None						R	R
HW Access	None						W	W
Name	None [31:26]						I2C_HS_EXIT	I2C_HS_ENTER

Bits	Name	Description
25	I2C_HS_EXIT	Logical and of corresponding request and mask bits. Default Value: 0
24	I2C_HS_ENTER	Logical and of corresponding request and mask bits. Default Value: 0
16	I2C_RESTART	Logical and of corresponding request and mask bits. Default Value: 0
11	SPI_BUS_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
10	SPI_EZ_STOP	Logical and of corresponding request and mask bits. Default Value: 0
9	SPI_EZ_WRITE_STOP	Logical and of corresponding request and mask bits. Default Value: 0

14.1.45 SCB0_INTR_S_MASKED (continued)

8	I2C_BUS_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
7	I2C_GENERAL	Logical and of corresponding request and mask bits. Default Value: 0
6	I2C_ADDR_MATCH	Logical and of corresponding request and mask bits. Default Value: 0
5	I2C_START	Logical and of corresponding request and mask bits. Default Value: 0
4	I2C_STOP	Logical and of corresponding request and mask bits. Default Value: 0
3	I2C_WRITE_STOP	Logical and of corresponding request and mask bits. Default Value: 0
2	I2C_ACK	Logical and of corresponding request and mask bits. Default Value: 0
1	I2C_NACK	Logical and of corresponding request and mask bits. Default Value: 0
0	I2C_ARB_LOST	Logical and of corresponding request and mask bits. Default Value: 0

14.1.46 SCB0_INTR_TX

Transmitter interrupt request

Address: 0x40240F80

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	None		RW1C	RW1C
HW Access	RW1S	RW1S	RW1S	RW1S	None		RW1S	RW1S
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	EMPTY	None [3:2]		NOT_FULL	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW1C	RW1C	RW1C
HW Access	None					RW1S	RW1S	RW1S
Name	None [15:11]					UART_AR-B_LOST	UART_-DONE	UART_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10	UART_ARB_LOST	UART lost arbitration: the value driven on the TX line is not the same as the value observed on the RX line. This condition event is useful when transmitter and receiver share a TX/RX line. This is the case in LIN or SmartCard modes. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
9	UART_DONE	UART transmitter done event. This happens when the IP is done transferring all data in the TX FIFO, and the last stop field is transmitted (both TX FIFO and transmit shifter register are empty). Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
8	UART_NACK	UART transmitter received a negative acknowledgement in SmartCard mode. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
7	BLOCKED	SW cannot get access to the EZ memory (EZ data access), due to an externally clocked EZ access. This may happen when STATUS.EC_BUSY is '1'. Default Value: 0

14.1.46 SCB0_INTR_TX (continued)

6	UNDERFLOW	Attempt to read from an empty TX FIFO. This happens when SCB is ready to transfer data and EMPTY is '1'. Only used in FIFO mode. Default Value: 0
5	OVERFLOW	Attempt to write to a full TX FIFO. Only used in FIFO mode. Default Value: 0
4	EMPTY	TX FIFO is empty; i.e. it has 0 entries. Only used in FIFO mode. Default Value: 0
1	NOT_FULL	TX FIFO is not full. Dependent on CTRL.MEM_WIDTH: (FF_DATA_NR = EZ_DATA_NR/2) MEM_WIDTH is "0": # entries != FF_DATA_NR. MEM_WIDTH is "1": # entries != FF_DATA_NR/2. MEM_WIDTH is "2": # entries != FF_DATA_NR/4. Only used in FIFO mode. Default Value: 0
0	TRIGGER	Less entries in the TX FIFO than the value specified by TX_FIFO_CTRL.TRIGGER_LEVEL. Only used in FIFO mode. Default Value: 0

14.1.47 SCB0_INTR_TX_SET

Transmitter interrupt set request

Address: 0x40240F84

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	RW1S	None		RW1S	RW1S
HW Access	A	A	A	A	None		A	A
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	EMPTY	None [3:2]		NOT_FULL	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW1S	RW1S	RW1S
HW Access	None					A	A	A
Name	None [15:11]					UART_AR-B_LOST	UART_-DONE	UART_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10	UART_ARB_LOST	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
9	UART_DONE	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
8	UART_NACK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
7	BLOCKED	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
6	UNDERFLOW	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
5	OVERFLOW	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
4	EMPTY	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

14.1.47 SCB0_INTR_TX_SET (continued)

1	NOT_FULL	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	TRIGGER	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

14.1.48 SCB0_INTR_TX_MASK

Transmitter interrupt mask

Address: 0x40240F88

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	None		RW	RW
HW Access	R	R	R	R	None		R	R
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	EMPTY	None [3:2]		NOT_FULL	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [15:11]					UART_AR-B_LOST	UART_-DONE	UART_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10	UART_ARB_LOST	Mask bit for corresponding bit in interrupt request register. Default Value: 0
9	UART_DONE	Mask bit for corresponding bit in interrupt request register. Default Value: 0
8	UART_NACK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
7	BLOCKED	Mask bit for corresponding bit in interrupt request register. Default Value: 0
6	UNDERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
5	OVERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
4	EMPTY	Mask bit for corresponding bit in interrupt request register. Default Value: 0

14.1.48 SCB0_INTR_TX_MASK (continued)

1	NOT_FULL	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	TRIGGER	Mask bit for corresponding bit in interrupt request register. Default Value: 0

14.1.49 SCB0_INTR_TX_MASKED

Transmitter interrupt masked request

Address: 0x40240F8C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	None		R	R
HW Access	W	W	W	W	None		W	W
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	EMPTY	None [3:2]		NOT_FULL	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None					R	R	R
HW Access	None					W	W	W
Name	None [15:11]					UART_AR-B_LOST	UART_-DONE	UART_NACK

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
10	UART_ARB_LOST	Logical and of corresponding request and mask bits. Default Value: 0
9	UART_DONE	Logical and of corresponding request and mask bits. Default Value: 0
8	UART_NACK	Logical and of corresponding request and mask bits. Default Value: 0
7	BLOCKED	Logical and of corresponding request and mask bits. Default Value: 0
6	UNDERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
5	OVERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
4	EMPTY	Logical and of corresponding request and mask bits. Default Value: 0

14.1.49 SCB0_INTR_TX_MASKED (continued)

1	NOT_FULL	Logical and of corresponding request and mask bits. Default Value: 0
0	TRIGGER	Logical and of corresponding request and mask bits. Default Value: 0

14.1.50 SCB0_INTR_RX

Receiver interrupt request

Address: 0x40240FC0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	None	RW1C	RW1C	None	RW1C
HW Access	RW1S	RW1S	RW1S	None	RW1S	RW1S	None	RW1S
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	None	FULL	NOT_EMP-TY	None	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW1C	RW1C	RW1C	RW1C
HW Access	None				RW1S	RW1S	RW1S	RW1S
Name	None [15:12]				BREAK_-DETECT	BAUD_DE-TECT	PARI-TY_ERROR	FRAME_ER ROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	BREAK_DETECT	Break detection is successful: the line is '0' for UART_RX_CTRL.BREAK_WIDTH + 1 bit period. Can occur at any time to address unanticipated break fields; i.e. "break-in-data" is supported. This feature is supported for the UART standard and LIN submodes. For the UART standard submodes, ongoing receipt of data frames is NOT affected; i.e. Firmware is expected to take the proper action. For the LIN submode, possible ongoing receipt of a data frame is stopped and the (partially) received data frame is dropped and baud rate detection is started. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0
10	BAUD_DETECT	LIN baudrate detection is completed. The receiver software uses the UART_RX_STA-TUS.BR_COUNTER value to set the right IP clock (from the programmable clock IP) to guaran-tee successful receipt of the first LIN data frame (Protected Identifier Field) after the synchronization byte. Set to '1', when event is detected. Write with '1' to clear bit. Default Value: 0

14.1.50 SCB0_INTR_RX (continued)

9	PARITY_ERROR	Parity error in received data frame. Set to '1', when event is detected. Write with '1' to clear bit. If UART_RX_CTL.DROP_ON_PARITY_ERROR is '1', the received frame is dropped. If UART_RX_CTL.DROP_ON_PARITY_ERROR is '0', the received frame is send to the RX FIFO. In SmartCard submode, negatively acknowledged data frames generate a parity error. Note that Firmware can only identify the erroneous data frame in the RX FIFO if it is fast enough to read the data frame before the hardware writes a next data frame into the RX FIFO. Default Value: 0
8	FRAME_ERROR	Frame error in received data frame. Set to '1', when event is detected. Write with '1' to clear bit. This can be either a start or stop bit(s) error: Start bit error: after the detection of the beginning of a start bit period (RX line changes from '1' to '0'), the middle of the start bit period is sampled erroneously (RX line is '1'). Note: a start bit error is detected BEFORE a data frame is received. Stop bit error: the RX line is sampled as '0', but a '1' was expected. Note: a stop bit error may result in failure to receive successive data frame(s). Note: a stop bit error is detected AFTER a data frame is received. A stop bit error is detected after a data frame is received, and the UART_RX_CTL.DROP_ON_-FRAME_ERROR field specifies whether the received frame is dropped or send to the RX FIFO. If UART_RX_CTL.DROP_ON_FRAME_ERROR is '1', the received data frame is dropped. If UART_RX_CTL.DROP_ON_FRAME_ERROR is '0', the received data frame is send to the RX FIFO. Note that Firmware can only identify the erroneous data frame in the RX FIFO if it is fast enough to read the data frame before the hardware writes a next data frame into the RX FIFO; i.e. the RX FIFO does not have error flags to tag erroneous data frames. Default Value: 0
7	BLOCKED	SW cannot get access to the EZ memory (EZ_DATA accesses), due to an externally clocked EZ access. This may happen when STATUS.EC_BUSY is '1'. Default Value: 0
6	UNDERFLOW	Attempt to read from an empty RX FIFO. Only used in FIFO mode. Default Value: 0
5	OVERFLOW	Attempt to write to a full RX FIFO. Note: in I2C mode, the OVERFLOW is set when a data frame is received and the RX FIFO is full, independent of whether it is ACK'd or NACK'd. Only used in FIFO mode. Default Value: 0
3	FULL	RX FIFO is full. Note that received data frames are lost when the RX FIFO is full. Dependent on CTRL.MEM_WIDTH: (FF_DATA_NR = EZ_DATA_NR/2) MEM_WIDTH is "0": # entries == FF_DATA_NR. MEM_WIDTH is "1": # entries == FF_DATA_NR/2. MEM_WIDTH is "2": # entries == FF_DATA_NR/4. Only used in FIFO mode. Default Value: 0
2	NOT_EMPTY	RX FIFO is not empty. Only used in FIFO mode. Default Value: 0
0	TRIGGER	More entries in the RX FIFO than the value specified by RX_FIFO_CTRL.TRIGGER_LEVEL. Only used in FIFO mode. Default Value: 0

14.1.51 SCB0_INTR_RX_SET

Receiver interrupt set request

Address: 0x40240FC4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	None	RW1S	RW1S	None	RW1S
HW Access	A	A	A	None	A	A	None	A
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	None	FULL	NOT_EMP-TY	None	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW1S	RW1S	RW1S	RW1S
HW Access	None				A	A	A	A
Name	None [15:12]				BREAK_-DETECT	BAUD_DE-TECT	PARI-TY_ERROR	FRAME_ER ROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	BREAK_DETECT	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
10	BAUD_DETECT	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
9	PARITY_ERROR	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
8	FRAME_ERROR	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
7	BLOCKED	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
6	UNDERFLOW	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
5	OVERFLOW	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0

14.1.51 SCB0_INTR_RX_SET (continued)

3	FULL	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
2	NOT_EMPTY	Write with '1' to set corresponding bit in interrupt status register. Default Value: 0
0	TRIGGER	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

14.1.52 SCB0_INTR_RX_MASK

Receiver interrupt mask

Address: 0x40240FC8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	None	RW	RW	None	RW
HW Access	R	R	R	None	R	R	None	R
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	None	FULL	NOT_EMP-TY	None	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [15:12]				BREAK_-DETECT	BAUD_DE-TECT	PARI-TY_ERROR	FRAME_ER ROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	BREAK_DETECT	Mask bit for corresponding bit in interrupt request register. Default Value: 0
10	BAUD_DETECT	Mask bit for corresponding bit in interrupt request register. Default Value: 0
9	PARITY_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
8	FRAME_ERROR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
7	BLOCKED	Mask bit for corresponding bit in interrupt request register. Default Value: 0
6	UNDERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
5	OVERFLOW	Mask bit for corresponding bit in interrupt request register. Default Value: 0

14.1.52 SCB0_INTR_RX_MASK (continued)

3	FULL	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	NOT_EMPTY	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	TRIGGER	Mask bit for corresponding bit in interrupt request register. Default Value: 0

14.1.53 SCB0_INTR_RX_MASKED

Receiver interrupt masked request

Address: 0x40240FCC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	None	R	R	None	R
HW Access	W	W	W	None	W	W	None	W
Name	BLOCKED	UNDER-FLOW	OVER-FLOW	None	FULL	NOT_EMP-TY	None	TRIGGER

Bits	15	14	13	12	11	10	9	8
SW Access	None				R	R	R	R
HW Access	None				W	W	W	W
Name	None [15:12]				BREAK_-DETECT	BAUD_DE-TECT	PARI-TY_ERROR	FRAME_ER ROR

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	BREAK_DETECT	Logical and of corresponding request and mask bits. Default Value: 0
10	BAUD_DETECT	Logical and of corresponding request and mask bits. Default Value: 0
9	PARITY_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
8	FRAME_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
7	BLOCKED	Logical and of corresponding request and mask bits. Default Value: 0
6	UNDERFLOW	Logical and of corresponding request and mask bits. Default Value: 0
5	OVERFLOW	Logical and of corresponding request and mask bits. Default Value: 0

14.1.53 SCB0_INTR_RX_MASKED (continued)

3	FULL	Logical and of corresponding request and mask bits. Default Value: 0
2	NOT_EMPTY	Logical and of corresponding request and mask bits. Default Value: 0
0	TRIGGER	Logical and of corresponding request and mask bits. Default Value: 0

14.1.54 SCB1_I2C_STATUS

I2C status

Address: 0x40250064

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		R	R	None	R	R	R
HW Access	None		W	W	None	W	W	W
Name	None [7:6]		M_READ	S_READ	None	I2CS_IC_BUSY	I2C_EC_BUSY	BUS_BUSY

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	CURR_EZ_ADDR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	BASE_EZ_ADDR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 16	BASE_EZ_ADDR	I2C slave base EZ address. Address as provided by an I2C write transfer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable, as clock domain synchronization is not performed in the design. Default Value: Undefined
15 : 8	CURR_EZ_ADDR	I2C slave current EZ address. Current address pointer. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable (during an ongoing transfer when I2C_EC_BUSY is '1'), as clock domain synchronization is not performed in the design. Default Value: Undefined
5	M_READ	I2C master read transfer ('1') or I2C master write transfer ('0'). When the I2C master is inactive/idle or transmitting START, REPEATED START, STOP or an address, this field is '0". Default Value: 0
4	S_READ	I2C slave read transfer ('1') or I2C slave write transfer ('0'). When the I2C slave is inactive/idle or receiving START, REPEATED START, STOP or an address, this field is '0". Default Value: 0

14.1.54 SCB1_I2C_STATUS (continued)

2	I2CS_IC_BUSY	Indicates whether the internally clocked slave logic is being accessed by external I2C master. --set at ADDR_MATCH --clear at START/RESET, STOP detection, or BUS_ERROR This bit can be used by SW to determine whether I2CS_IC is busy before entering DeepSleep. Default Value: 0
1	I2C_EC_BUSY	Indicates whether the externally clocked logic is potentially accessing the EZ memory and/or updating BASE_EZ_ADDR or CURR_EZ_ADDR (this is only possible in EZ mode). This bit can be used by SW to determine whether BASE_EZ_ADDR and CURR_EZ_ADDR are reliable. Default Value: Undefined
0	BUS_BUSY	I2C bus is busy. The bus is considered busy ('1'), from the time a START is detected or from the time the SCL line is '0'. The bus is considered idle ('0'), from the time a STOP is detected. If SCB block is disabled, BUS_BUSY is '0'. After enabling the block, it takes time for the BUS_BUSY to detect a busy bus. This time is the maximum high time of the SCL line. For a 100 kHz interface frequency, this maximum high time may last roughly 5 us (half a bit period). For single master systems, BUS_BUSY does not have to be used to detect an idle bus before a master starts a transfer using I2C_M_CMD.M_START (no bus collisions). For multi-master systems, BUS_BUSY can be used to detect an idle bus before a master starts a transfer using I2C_M_CMD.M_START_ON_IDLE (to prevent bus collisions). Default Value: 0

15 LCD Direct Registers

This section discusses the LCD Direct registers. It lists all the registers in mapping tables, in address order.

15.1 Register Details

Register	Address	Description
LCD_ID	0x40210000	ID & Revision
LCD_DIVIDER	0x40210004	LCD Divider Register
LCD_CONTROL	0x40210008	LCD Configuration Register
LCD_DATA00	0x40210100	LCD Pin Data Registers
LCD_DATA01	0x40210104	LCD Pin Data Registers. See LCD_DATA00 for the details of bit fields.
LCD_DATA02	0x40210108	LCD Pin Data Registers. See LCD_DATA00 for the details of bit fields.
LCD_DATA03	0x4021010C	LCD Pin Data Registers. See LCD_DATA00 for the details of bit fields.
LCD_DATA04	0x40210110	LCD Pin Data Registers. See LCD_DATA00 for the details of bit fields.
LCD_DATA05	0x40210114	LCD Pin Data Registers. See LCD_DATA00 for the details of bit fields.
LCD_DATA06	0x40210118	LCD Pin Data Registers. See LCD_DATA00 for the details of bit fields.
LCD_DATA07	0x4021011C	LCD Pin Data Registers. See LCD_DATA00 for the details of bit fields.
LCD_DATA10	0x40210200	LCD Pin Data Registers
LCD_DATA11	0x40210204	LCD Pin Data Registers. See LCD_DATA10 for the details of bit fields.
LCD_DATA12	0x40210208	LCD Pin Data Registers. See LCD_DATA10 for the details of bit fields.
LCD_DATA13	0x4021020C	LCD Pin Data Registers. See LCD_DATA10 for the details of bit fields.
LCD_DATA14	0x40210210	LCD Pin Data Registers. See LCD_DATA10 for the details of bit fields.
LCD_DATA15	0x40210214	LCD Pin Data Registers. See LCD_DATA10 for the details of bit fields.
LCD_DATA16	0x40210218	LCD Pin Data Registers. See LCD_DATA10 for the details of bit fields.
LCD_DATA17	0x4021021C	LCD Pin Data Registers. See LCD_DATA10 for the details of bit fields.

15.1.1 LCD_ID

ID & Revision

Address: 0x40210000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	ID [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	REVISION [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	REVISION [31:24]							

Bits	Name	Description
31 : 16	REVISION	The version number is 0x0001 Default Value: 1
15 : 0	ID	The ID of LCD controller peripheral is 0xF0F0 Default Value: 61680

15.1.2 LCD_DIVIDER

LCD Divider Register

Address: 0x40210004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SUBFR_DIV [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	SUBFR_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DEAD_DIV [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	DEAD_DIV [31:24]							

Bits	Name	Description
31 : 16	DEAD_DIV	Length of the dead time period in cycles. When set to zero, no dead time period exists. Default Value: 0
15 : 0	SUBFR_DIV	Input clock frequency divide value, to generate the 1/4 sub-frame period. The sub-frame period is 4*(SUBFR_DIV+1) cycles long. Default Value: 0

15.1.3 LCD_CONTROL

LCD Configuration Register

Address: 0x40210008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW		RW	RW	RW	RW	RW
HW Access	None	R		R	R	R	R	R
Name	None	BIAS [6:5]		OP_MODE	TYPE	LCD_-MODE	HS_EN	LS_EN

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				COM_NUM [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	LS_EN_STAT	None [30:24]						

Bits	Name	Description
31	LS_EN_STAT	Reserved. This bit must be 0. Default Value: 0
11 : 8	COM_NUM	The number of COM connections minus 2. So: 0: 2 COM's 1: 3 COM's ... 13: 15 COM's 14: 16 COM's 15: undefined Default Value: 0
6 : 5	BIAS	PWM bias selection Default Value: 0 **0x0: HALF :** 1/2 Bias

15.1.3 LCD_CONTROL (continued)

		0x1: THIRD : 1/3 Bias **0x2: FOURTH :** 1/4 Bias **0x3: FIFTH :** 1/5 Bias
4	OP_MODE	Driving mode configuration Default Value: 0 **0x0: PWM :** PWM Mode **0x1: CORRELATION :** Reserved
3	TYPE	LCD driving waveform type configuration. Default Value: 0 **0x0: TYPE_A :** Type A - Each frame addresses each COM pin only once with a balanced (DC=0) waveform. **0x1: TYPE_B :** Type B - Each frame addresses each COM pin twice in sequence with a positive and negative waveform that together are balanced (DC=0).
2	LCD_MODE	HS/LS Mode selection Default Value: 0 **0x0: LS :** Reserved. This bit must be 0. **0x1: HS :** Select High Speed (system clock) Generator (Works in Active and Sleep power modes only).
1	HS_EN	High speed (HS) generator enable 1: enable 0: disable Default Value: 0
0	LS_EN	Reserved. This bit must be 0. Default Value: 0

15.1.4 LCD_DATA00

LCD Pin Data Registers

Address: 0x40210100

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Bits [4i+3:4i] represent the pin data for pin [i] for COMS 1-4 (COM1 is lsb). Default Value: 0

15.1.5 LCD_DATA10

LCD Pin Data Registers

Address: 0x40210200

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DATA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DATA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	DATA [31:24]							

Bits	Name	Description
31 : 0	DATA	Bits [4i+3:4i] represent the pin data for pin [i] for COMS 5-8 (COM5 is lsb). Default Value: 0

16 Low-Power Comparator (LPCOMP) Registers

This section discusses the LPCOMP registers. It lists all the registers in mapping tables, in address order.

16.1 Register Details

Register	Address	Description
LPCOMP_ID	0x402B0000	ID & Revision
LPCOMP_CONFIG	0x402B0004	LPCOMP Configuration Register
LPCOMP_INTR	0x402B0010	LPCOMP Interrupt request register
LPCOMP_INTR_SET	0x402B0014	LPCOMP Interrupt set register
LPCOMP_INTR_MASK	0x402B0018	LPCOMP Interrupt request mask
LPCOMP_INTR_MASKED	0x402B001C	LPCOMP Interrupt request masked
LPCOMP_TRIM1	0x402BFF00	LPCOMP Trim Register
LPCOMP_TRIM2	0x402BFF04	LPCOMP Trim Register
LPCOMP_TRIM3	0x402BFF08	LPCOMP Trim Register
LPCOMP_TRIM4	0x402BFF0C	LPCOMP Trim Register

16.1.1 LPCOMP_ID

ID & Revision

Address: 0x402B0000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	ID [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	ID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	REVISION [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	REVISION [31:24]							

Bits	Name	Description
31 : 16	REVISION	the version number is 0x0001 Default Value: 1
15 : 0	ID	the ID of LPCOMP peripheral is 0xE0E0 Default Value: 57568

16.1.2 LPCOMP_CONFIG

LPCOMP Configuration Register

Address: 0x402B0004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	R	RW		RW	RW	RW	
HW Access	R	RW	R		R	R	R	
Name	ENABLE1	OUT1	INTTYPE1 [5:4]		FILTER1	HYST1	MODE1 [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW	R	RW		RW	RW	RW	
HW Access	R	RW	R		R	R	R	
Name	ENABLE2	OUT2	INTTYPE2 [13:12]		FILTER2	HYST2	MODE2 [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW	RW	None		RW	RW
HW Access	None		R	R	None		R	R
Name	None [23:22]		DSI_LEV-EL2	DSI_BY-PASS2	None [19:18]		DSI_LEV-EL1	DSI_BY-PASS1

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
21	DSI_LEVEL2	Opamp2 comparator DSI (trigger) out level : 0=pulse, 1=level Default Value: 0
20	DSI_BYPASS2	Opamp2 bypass comparator output synchronization for DSI output: 0=synchronize (level or pulse), 1=bypass (output async) Note that in DeepSleep mode this bit needs to be set to observe the DSI output on the dedicated pin. Default Value: 0
17	DSI_LEVEL1	Opamp1 comparator DSI (trigger) out level : 0=pulse, 1=level Default Value: 0
16	DSI_BYPASS1	Opamp1 bypass comparator output synchronization for DSI output: 0=synchronize (level or pulse), 1=bypass (output async) Note that in DeepSleep mode this bit needs to be set to observe the DSI output on the dedicated pin. Default Value: 0
15	ENABLE2	Enable comparator #2 Default Value: 0

16.1.2 LPCOMP_CONFIG (continued)

14	OUT2	Current output value of the comparator. Default Value: 0
13 : 12	INTTYPE2	Sets which edge will trigger an IRQ Default Value: 0 **0x0: DISABLE :** Disabled, no interrupts will be detected **0x1: RISING :** Rising edge **0x2: FALLING :** Falling edge **0x3: BOTH :** Both rising and falling edges
11	FILTER2	Deprecated, Reserved, must be written 0 Default Value: 0
10	HYST2	Add 10mV hysteresis to the comparator - 0: Enable Hysteresis - 1: Disable Hysteresis Default Value: 0
9 : 8	MODE2	Operating mode for the comparator Default Value: 0 **0x0: SLOW :** Slow operating mode (uses less power, <50uA) **0x1: FAST :** Fast operating mode (uses more power, <400uA) **0x2: ULP :** Ultra low power operting mode (uses ~2-4uA)
7	ENABLE1	Enable comparator #1 Default Value: 0
6	OUT1	Current output value of the comparator. Default Value: 0
5 : 4	INTTYPE1	Sets which edge will trigger an IRQ Default Value: 0

16.1.2 LPCOMP_CONFIG (continued)

		0x0: DISABLE : Disabled, no interrupts will be detected **0x1: RISING :** Rising edge **0x2: FALLING :** Falling edge **0x3: BOTH :** Both rising and falling edges
3	FILTER1	Deprecated, Reserved, must be written 0 Default Value: 0
2	HYST1	Add 10mV hysteresis to the comparator - 0: Enable Hysteresis - 1: Disable Hysteresis Default Value: 0
1 : 0	MODE1	Operating mode for the comparator Default Value: 0 **0x0: SLOW :** Slow operating mode (uses less power, <50uA) **0x1: FAST :** Fast operating mode (uses more power, <400uA) **0x2: ULP :** Ultra low power operting mode (uses ~2-4uA)

16.1.3 LPCOMP_INTR

LPCOMP Interrupt request register

Address: 0x402B0010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1C	RW1C
HW Access	None						RW1S	RW1S
Name	None [7:2]						COMP2	COMP1

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	COMP2	Comparator 2 Interrupt: hardware sets this interrupt when comparator 0 triggers. Write with '1' to clear bit. Default Value: 0
0	COMP1	Comparator 1 Interrupt: hardware sets this interrupt when comparator 0 triggers. Write with '1' to clear bit. Default Value: 0

16.1.4 LPCOMP_INTR_SET

LPCOMP Interrupt set register

Address: 0x402B0014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1S	RW1S
HW Access	None						A	A
Name	None [7:2]						COMP2	COMP1

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	COMP2	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	COMP1	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

16.1.5 LPCOMP_INTR_MASK

LPCOMP Interrupt request mask

Address: 0x402B0018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						COMP2_MASK	COMP1_MASK

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	COMP2_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	COMP1_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0

16.1.6 LPCOMP_INTR_MASKED

LPCOMP Interrupt request masked

Address: 0x402B001C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						W	W
Name	None [7:2]						COMP2_MASKED	COMP1_MASKED

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	COMP2_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
0	COMP1_MASKED	Logical and of corresponding request and mask bits. Default Value: 0

16.1.7 LPCOMP_TRIM1

LPCOMP Trim Register

Address: 0x402BFF00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			R				
Name	None [7:5]			COMP1_TRIMA [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4 : 0	COMP1_TRIMA	Trim A for Comparator #1 Default Value: 0

16.1.8 LPCOMP_TRIM2

LPCOMP Trim Register

Address: 0x402BFF04

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			R				
Name	None [7:5]			COMP1_TRIMB [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4 : 0	COMP1_TRIMB	Trim B for Comparator #1 Default Value: 0

16.1.9 LPCOMP_TRIM3

LPCOMP Trim Register

Address: 0x402BFF08

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			R				
Name	None [7:5]			COMP2_TRIMA [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4 : 0	COMP2_TRIMA	Trim A for Comparator #2 Default Value: 0

16.1.10 LPCOMP_TRIM4

LPCOMP Trim Register

Address: 0x402BFF0C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			R				
Name	None [7:5]			COMP2_TRIMB [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4 : 0	COMP2_TRIMB	Trim B for Comparator #2 Default Value: 0

17 External Clock (EXCO) Registers

This section discusses the EXCO registers. It lists all the registers in mapping tables, in address order.

17.1 Register Details

Register	Address	Description
EXCO_CLK_SELECT	0x402F0000	Clock Select Register
EXCO_ECO_CONFIG	0x402F0008	ECO Configuration Register
EXCO_ECO_STATUS	0x402F000C	ECO Status Register
EXCO_PLL_CONFIG	0x402F0014	PLL Configuration Register
EXCO_PLL_STATUS	0x402F0018	PLL Status Register
EXCO_PLL_TEST	0x402F001C	PLL Test Register
EXCO_EXCO_PGM_CLK	0x402F0020	EXCO Program Clock
EXCO_REF_CTL	0x402F0030	Clock Supervision Reference Contol
EXCO_REF_LIMIT	0x402F0034	Clock Supervision Reference Limits
EXCO_MON_CTL	0x402F0038	Clock Supervision Monitor Control
EXCO_INTR	0x402F0040	Interrupt Request Register
EXCO_INTR_SET	0x402F0044	Interrupt Set Register
EXCO_INTR_MASK	0x402F0048	Interrupt Mask Register
EXCO_INTR_MASKED	0x402F004C	Interrrupt Masked Register
EXCO_RSTDLY_CTL	0x402F0050	Programmable Delay Counter Control
EXCO_RSTDLY	0x402F0054	Programmable Delay Counter Initial Amount
EXCO_RSTDLY_COUNT_VAL	0x402F0058	Programmable Delay Counter Value
EXCO_ECO_TRIM0	0x402FFF00	ECO Trim0 Register
EXCO_ECO_TRIM1	0x402FFF04	ECO Trim1 Register
EXCO_ECO_TRIM2	0x402FFF08	ECO Trim2 Register
EXCO_PLL_TRIM	0x402FFF0C	PLL Trim Register

17.1.1 EXCO_CLK_SELECT

Clock Select Register

Address: 0x402F0000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW		RW
HW Access	None					R		R
Name	None [7:3]					REF_SEL [2:1]		CLK_SELECT

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2 : 1	REF_SEL	Select source for PLL reference 0: from ECO 1: from external reference 2: from clk_imo 3: from clk_imo Default Value: 0 **0x0: SEL_ECO :** From ECO **0x1: SEL_EXT_REF :** From external reference **0x2: SEL_CLK_IMO :** From CLK_IMO

17.1.1 EXCO_CLK_SELECT (continued)

0	CLK_SELECT	Select a clock source for clk_eco: If PLL_CONFIG.ENABLE=0, then clk_eco=clk_osc. When PLL_CONFIG.ENABLE=1, and PLL_CONFIG.BYPASS=2'b10: 0: clk_osc 1: clk_pll Default Value: 0

17.1.2 EXCO_ECO_CONFIG

ECO Configuration Register

Address: 0x402F0008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						AGC_EN	CLK_EN

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	ENABLE	None [30:24]						

Bits	Name	Description
31	ENABLE	Master enable for ECO oscillator. Refer to CLK_EN for sequencing. Default Value: 0
1	AGC_EN	Automatic Gain Control (AGC) enable. When set, the oscillation amplitude is controlled to the level selected by ECO_TRIM0.ATRIM. When low, the amplitude is not explicitly controlled and will grow until it saturates to the supply rail (1.8V nom). WARNING: use care when disabling AGC because driving a crystal beyond its rated limit can permanently damage the crystal. Default Value: 1
0	CLK_EN	Clock Enable. When enabling the clock, first write ENABLE=1, wait at least 10us, and then write CLK_EN=1. When disabling, clearing both CLK_EN=0 and ENABLE=0 can be done in the same AHB write Default Value: 0

17.1.3 EXCO_ECO_STATUS

ECO Status Register

Address: 0x402F000C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							W
Name	None [7:1]							WATCH-DOG_ER-ROR

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	WATCHDOG_ERROR	This bit is set to 1 if the oscillator is stuck. The ECO clock is gated off during a watchdog error condition. Due to internal synchonization, the clock is stopped two cycles after an error condition is observed and ungated two cycles after the error condition is resolved. Note: This bit setting reflected in INT.WD_ERR if Interrupts are enabled. Default Value: 0

17.1.4 EXCO_PLL_CONFIG

PLL Configuration Register

Address: 0x402F0014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	FEEDBACK_DIV [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW					
HW Access	R		R					
Name	OUTPUT_DIV [15:14]		REFERENCE_DIV [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW		None	RW		
HW Access	None		R		None	R		
Name	None [23:22]		BYPASS_SEL [21:20]		None	ICP_SEL [18:16]		

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None					
HW Access	R	R	None					
Name	ENABLE	ISOLATE_N	None [29:24]					

Bits	Name	Description
31	ENABLE	Master enable for PLL power gate. Refer to ISOLATE_N field for required sequencing. 0: Block is powered off, also forces clk_eco = clk_osc - See CLK_SELECT.CLK_SELECT description. 1: Block is powered on Default Value: 0
30	ISOLATE_N	Isolation control of PLL outputs. This also internally resets the PLL. De-assert >= 5us after ENABLE=1. Assertion can happen in same write as ENABLE=0. 0: Isolate outputs 1: Do not isolate outputs Default Value: 0
21 : 20	BYPASS_SEL	Selects the source of the system PLL0 clock. See also CLK_SELECT.CLK_SELECT for effect on clk_eco selection. Default Value: 0 **0x0: AUTO :** Automatic using lock indicator. When unlocked, automatically selects PLL reference input (bypass mode). When locked, automatically selects PLL output.

17.1.4 EXCO_PLL_CONFIG (continued)

		0x1: AUTO1 : Same as AUTO **0x2: PLL_REF :** Select PLL reference input (bypass mode). Ignores lock indicator **0x3: PLL_OUT :** Select PLL output. Ignores lock indicator.
18 : 16	ICP_SEL	Programmable charge pump current between 0uA and 7uA. For functional operation, the value must be set according to the PLL output frequency Fout (measured before the output divider): 0,1: Illegal 2: 2uA. Use when Fout <= 67MHz 3: 3uA. Use when Fout > 67MHz 4-7: Illegal Default Value: 2
15 : 14	OUTPUT_DIV	Control bits for Output divider: FOUT = FVCO / {1,2,4,8} Default Value: 0 **0x0: PASS :** Pass Through **0x1: DIV2 :** Divide by 2 **0x2: DIV4 :** Divide by 4 **0x3: DIV8 :** Divide by 8
13 : 8	REFERENCE_DIV	Control bits for reference divider: 0x00 = Divide by 1 0x01 - Divide by 2 ... 0x3F = Divide by 64 Must be set so that 1 MHz <= FPFD <= 3 MHz, where FPFD = FREF / (REFERENCE_DIV+1) Do not change while PLL output is selected. Default Value: 0

17.1.4 EXCO_PLL_CONFIG (continued)

7 : 0	FEEDBACK_DIV	Control bits for feedback divider: 0x08 = Divide by 8 (minimum legal value) 0x09 = Divide by 9 ... 0xFF = Divide by 255 Must be set so that 22.5MHz <= FVCO <= 104MHz, where FVCO = FREF * FEEDBACK_DIV / (REFERENCE_DIV+1) Do not change while PLL output is selected. Additional limitations on PLL output frequency apply if PLL is providing the system clock. Default Value: 0

17.1.5 EXCO_PLL_STATUS

PLL Status Register

Address: 0x402F0018

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							W
Name	None [7:1]							LOCKED

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	LOCKED	PLL Lock Indicator Default Value: 0

17.1.6 EXCO_PLL_TEST

PLL Test Register

Address: 0x402F001C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW1C	RW	RW		
HW Access	None			A	R	R		
Name	None [7:5]			UN-LOCK_OC-CURRED	FAST_LOCK_EN	TEST_MODE [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4	UNLOCK_OCCURRED	This bit is not retained. Default Value: 0
3	FAST_LOCK_EN	Reserved. Leave at default value. Default Value: 1
2 : 0	TEST_MODE	Reserved. Leave at default value. Default Value: 0 **0x0: NORMAL :** Reserved **0x1: TEST_VC_LKG :** Reserved

17.1.6 EXCO_PLL_TEST (continued)

0x2: TEST_CP_DN :

Reserved

0x3: TEST_CP_UP :

Reserved

0x4: USER_EXT_FL :

Reserved

0x5: TEST_CTR_PQ :

Reserved

0x6: TEST_LD_DLY :

Reserved

0x7: TEST_CTR_ALT :

Reserved

17.1.7 EXCO_EXCO_PGM_CLK

EXCO Program Clock

Address: 0x402F0020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	RW	R	RW	None
HW Access	None			R	R	RW	R	None
Name	None [7:5]			EN_-CLK_PLL0	CLK_PLL0_OUT	CLK_PLL0_IN	CLK_ECO	None

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	ENABLE	None [30:24]						

Bits	Name	Description
31	ENABLE	Enable bit-banging test capability in this register. Default Value: 0
4	EN_CLK_PLL0	Bit bang en_clk_pll0 Default Value: 0
3	CLK_PLL0_OUT	Bit bang clk_pll0_out Default Value: 0
2	CLK_PLL0_IN	Observation point for clk_pll0_in, not retained. Default Value: 0
1	CLK_ECO	Bit bang clk_eco Default Value: 0

17.1.8 EXCO_REF_CTL

Clock Supervision Reference Contol

Address: 0x402F0030

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	STARTUP [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	STARTUP [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [23:19]					CSV_-CLK_SW_EN	CSV_TRIG_EN	CSV_INT_EN

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	CSV_EN	None [30:24]						

Bits	Name	Description
31	CSV_EN	Enables clock supervision, both frequency and loss. CSV in Active domain: Clock supervision is reset during DeepSleep and Hibernate modes. When enabled it begins operating automatically after a DeepSleep wakeup, but it must be reconfigured after Hibernate wakeup. When CSV error detection occurs - the CSV_CLK_SW, CSV_INT_EN and CVS_TRIG_EN control where the error is reported. Default Value: 0
18	CSV_CLK_SW_EN	Enable CSV to cause Clock Switch to IMO when set. Default Value: 1
17	CSV_TRIG_EN	Enable CSV to cause trigger if a clock switch occurs to IMO. Default Value: 0
16	CSV_INT_EN	Enable CSV setting INT.CSV_CLK_SW if a clock switch occurs to IMO. Default Value: 0

17.1.8 EXCO_REF_CTL (continued)

15 : 0	STARTUP	Startup delay time -1 (in reference clock cycles), after enable or DeepSleep wakeup, from reference clock start to monitored clock start. At a minimum (both clocks running): STARTUP >= (PERIOD +3) * FREQ_RATIO - UPPER, with FREQ_RATIO = (Reference frequency / Monitored frequency) On top of that the actual clock startup delay and the margin for accuracy of both clocks must be added. Default Value: 0

17.1.9 EXCO_REF_LIMIT

Clock Supervision Reference Limits

Address: 0x402F0034

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	LOWER [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	LOWER [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	UPPER [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	UPPER [31:24]							

Bits	Name	Description
31 : 16	UPPER	Cycle time upper limit. Set the upper limit -1, in reference clock cycles, before (or same time) the next monitored clock event must happen. If a monitored clock event does not happen before this limit is reached, or does not happen at all (clock loss), a CSV error is detected. Default Value: 0
15 : 0	LOWER	Cycle time lower limit. Set the lower limit -1, in reference clock cycles, before the next monitored clock event is allowed to happen. If a monitored clock event happens before this limit is reached a CSV error is detected. LOWER must be at least 1 less than UPPER. In case the clocks are asynchronous LOWER must be at least 3 less than UPPER. Default Value: 0

17.1.10 EXCO_MON_CTL

Clock Supervision Monitor Control

Address: 0x402F0038

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	PERIOD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	PERIOD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	PERIOD	Period time. Set the Period -1, in monitored clock cycles, before the next monitored clock event happens. PERIOD <= (UPPER+1) / FREQ_RATIO -1, with FREQ_RATIO = (Reference frequency / Monitored frequency) In case the clocks are asynchronous: PERIOD <= UPPER / FREQ_RATIO -1 Additionaly margin must be added for accuracy of both clocks. Default Value: 0

17.1.11 EXCO_INTR

Interrupt Request Register

Address: 0x402F0040

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW1C	RW1C	RW1C
HW Access	None					RW1S	RW1S	RW1S
Name	None [7:3]					CSV_-CLK_SW	WD_ERR	PLL_LOCK

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	CSV_CLK_SW	Clock Supervisor Switched Clock Source to IMO Default Value: 0
1	WD_ERR	EXCO Watch Dog Error detected - Oscillator stopped oscillating Default Value: 0
0	PLL_LOCK	HW will set this bit when PLL loses lock (PLL "locked" output goes low). Default Value: 0

17.1.12 EXCO_INTR_SET

Interrupt Set Register

Address: 0x402F0044

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW1S	RW1S	RW1S
HW Access	None					A	A	A
Name	None [7:3]					CSV_-CLK_SW	WD_ERR	PLL_LOCK

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	CSV_CLK_SW	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
1	WD_ERR	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	PLL_LOCK	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

17.1.13 EXCO_INTR_MASK

Interrupt Mask Register

Address: 0x402F0048

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [7:3]					CSV_-CLK_SW	WD_ERR	PLL_LOCK

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	CSV_CLK_SW	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	WD_ERR	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	PLL_LOCK	Mask bit for corresponding bit in interrupt request register. Default Value: 0

17.1.14 EXCO_INTR_MASKED

Interrrupt Masked Register

Address: 0x402F004C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					R	R	R
HW Access	None					W	W	W
Name	None [7:3]					CSV_-CLK_SW	WD_ERR	PLL_LOCK

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2	CSV_CLK_SW	Logical and of corresponding request and mask bits. Default Value: 0
1	WD_ERR	Logical and of corresponding request and mask bits. Default Value: 0
0	PLL_LOCK	Logical and of corresponding request and mask bits. Default Value: 0

17.1.15 EXCO_RSTDLY_CTL

Programmable Delay Counter Control

Address: 0x402F0050

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1S
HW Access	None							RW1C
Name	None [7:1]							LOAD

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	EN	None [30:24]						

Bits	Name	Description
31	EN	Programmable Delay Counter Enable "0": Disable "1": Enable Default Value: 0
0	LOAD	Programmable Delay Counter Load - Reloads the DLYCOUNT into the COUNT_VAL register 0: No Action 1: Generate a 1 clock pulse that loads the Initial value into the COUNT_VAL register. Default Value: 0

17.1.16 EXCO_RSTDLY

Programmable Delay Counter Initial Amount

Address: 0x402F0054

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DLYCOUNT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	DLYCOUNT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	DLYCOUNT	Delay Count Value Default Value: 256

17.1.17 EXCO_RSTDLY_COUNT_VAL

Programmable Delay Counter Value

Address: 0x402F0058

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	COUNT_VAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	COUNT_VAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	COUNT_VAL	Current Programmable Delay Counter value Default Value: 256

17.1.18 EXCO_ECO_TRIM0

ECO Trim0 Register

Address: 0x402FFF00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW			RW	
HW Access	None			R			R	
Name	None [7:5]			ATRIM [4:2]			WDTRIM [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4 : 2	ATRIM	Amplitude trim to set the crystal drive level when ECO_CONFIG.AGC_EN=1. WARNING: use care when setting this field because driving a crystal beyond its rated limit can permanently damage the crystal. 0x0 - 0.3Vpp 0x1 - 0.4Vpp 0x2 - 0.5Vpp 0x3 - 0.6Vpp 0x4 - 0.7Vpp 0x5 - 0.8Vpp 0x6 - 0.9Vpp 0x7 - 1.0Vpp Default Value: 0
1 : 0	WDTRIM	Watch Dog Trim - Delta voltage below stead state level 0x0 - 0.05V 0x1 - 0.1V 0x2 - 0.15V 0x3 - 0.2V Default Value: 0

17.1.19 EXCO_ECO_TRIM1

ECO Trim1 Register

Address: 0x402FFF04

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW		RW		RW	
HW Access	None		R		R		R	
Name	None [7:6]		GTRIM [5:4]		RTRIM [3:2]		FTRIM [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 4	GTRIM	Gain Trim - Startup time Default Value: 1
3 : 2	RTRIM	Feedback resistor Trim Default Value: 1
1 : 0	FTRIM	Filter Trim - 3rd harmonic oscillation Default Value: 1

17.1.20 EXCO_ECO_TRIM2

ECO Trim2 Register

Address: 0x402FFF08

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		ITRIM [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	ITRIM	Current Trim Default Value: 32

17.1.21 EXCO_PLL_TRIM

PLL Trim Register

Address: 0x402FFF0C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW		RW		RW	
HW Access	None		R		R		R	
Name	None [7:6]		LOCK_DELAY [5:4]		LOCK_WINDOW [3:2]		VCO_GAIN [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 4	LOCK_DELAY	Selects the number of PLL phase frequency detector cycles that the phase error must be in range before declaring lock. (PFD clock cycle = Clock Reference Period/REFERENCE_DIV) Default Value: 1 **0x0: PFD_CLK_16 :** 16 PFD clock cycles **0x1: PFD_CLK_32 :** 32 PFD clock cycles **0x2: PFD_CLK_48 :** 48 PFD clock cycles

17.1.21 EXCO_PLL_TRIM (continued)

		0x3: PFD_CLK_64 : 64 PFD clock cycles
3 : 2	LOCK_WINDOW	This register determines how much phase error is tolerated before declaring the PLL unlocked (lock_out goes low). Phase error is a measure of the phase difference between the PLL feedforward path (CLK_REF PERIOD/REFERENCE_DIV[1:0]) and feedback path (CLK_VCO/FEEDBACK_DIV[1:0]). The average phase error when locked is zero, but accumulated jitter - particularly on CLK_REF - leads to the need for a relatively large allowed phase error window. Default Value: 0 **0x0: DELAY_25NS :** Delay 25 ns **0x1: DELAY_50NS :** Delay 50 ns **0x2: DELAY_75NS :** Delay 75 ns **0x3: DELAY_100NS :** Delay 100 ns
1 : 0	VCO_GAIN	Programmable VCO frequency characteristic at high freq - set to <10> Default Value: 2

18 Continuous Time Block Mini (CTBM) Registers

This section discusses the CTBM registers. It lists all the registers in mapping tables, in address order.

18.1 Register Details

Register	Address	Description
CTBM0_CTB_CTRL	0x40300000	global CTB and power control
CTBM0_OA_RES0_CTRL	0x40300004	Opamp0 and resistor0 control
CTBM0_OA_RES1_CTRL	0x40300008	Opamp1 and resistor1 control
CTBM0_COMP_STAT	0x4030000C	Comparator status
CTBM0_INTR	0x40300020	Interrupt request register
CTBM0_INTR_SET	0x40300024	Interrupt request set register
CTBM0_INTR_MASK	0x40300028	Interrupt request mask
CTBM0_INTR_MASKED	0x4030002C	Interrupt request masked
CTBM0_DFT_CTRL	0x40300030	Was 'Analog DfT controls', now used as Risk Mitigation bits (RMP)
CTBM0_OA0_SW	0x40300080	Opamp0 switch control
CTBM0_OA0_SW_CLEAR	0x40300084	Opamp0 switch control clear
CTBM0_OA1_SW	0x40300088	Opamp1 switch control
CTBM0_OA1_SW_CLEAR	0x4030008C	Opamp1 switch control clear
CTBM0_CTB_SW_HW_CTRL	0x403000C0	CTB bus switch control
CTBM0_CTB_SW_STATUS	0x403000C4	CTB bus switch control status
CTBM0_OA0_OFFSET_TRIM	0x40300F00	Opamp0 trim control
CTBM0_OA0_SLOPE_OFFSET_TRIM	0x40300F04	Opamp0 trim control
CTBM0_OA0_COMP_TRIM	0x40300F08	Opamp0 trim control
CTBM0_OA1_OFFSET_TRIM	0x40300F0C	Opamp1 trim control
CTBM0_OA1_SLOPE_OFFSET_TRIM	0x40300F10	Opamp1 trim control
CTBM0_OA1_COMP_TRIM	0x40300F14	Opamp1 trim control

18.1.1 CTBM0_CTB_CTRL

global CTB and power control

Address: 0x40300000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	None					
HW Access	R	R	None					
Name	ENABLED	DEEPS-LEEP_ON	None					

Bits	Name	Description
31	ENABLED	- 0: CTB IP disabled (put analog in power down, open all switches) - 1: CTB IP enabled Default Value: 0
30	DEEPSLEEP_ON	- 0: CTB IP disabled off during DeepSleep power mode - 1: CTB IP remains enabled during DeepSleep power mode (if ENABLED=1) Default Value: 0

18.1.2 CTBM0_OA_RES0_CTRL

Opamp0 and resistor0 control

Address: 0x40300004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	None	RW	RW	
HW Access	R	R	R	R	None	R	R	
Name	OA0_DSI_LEVEL	OA0_BYPASS_DSI_SYNC	OA0_HYST_EN	OA0_COMP_EN	None	OA0_DRIVE_STR_SEL	OA0_PWR_MODE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	None	RW	
HW Access	None				R	None	R	
Name	None [15:12]				OA0_PUMP_EN	None	OA0_COMPINT [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	OA0_PUMP_EN	Opamp0 pump enable Default Value: 0
9 : 8	OA0_COMPINT	Opamp0 comparator edge detect for interrupt and pulse mode of DSI (trigger) Default Value: 0 **0x0: DISABLE :** Disabled, no interrupts will be detected **0x1: RISING :** Rising edge

18.1.2 CTBM0_OA_RES0_CTRL (continued)

		0x2: FALLING : Falling edge **0x3: BOTH :** Both rising and falling edges
7	OA0_DSI_LEVEL	Opamp0 comparator DSI (trigger) out level : 0=pulse, each time an edge is detected (see OA0_COMPINT) a pulse is sent out on DSI 1=level, DSI output is a synchronized version of the comparator output Default Value: 0
6	OA0_BY-PASS_DSI_SYNC	Opamp0 bypass comparator output synchronization for DSI (trigger) output: 0=synchronize (level or pulse), 1=bypass (output async) Default Value: 0
5	OA0_HYST_EN	Opamp0 hysteresis enable (10mV) Default Value: 0
4	OA0_COMP_EN	Opamp0 comparator enable Default Value: 0
2	OA0_DRIVE_STR_SEL	Opamp0 output strenght select 0=1x, 1=10x Default Value: 0
1 : 0	OA0_PWR_MODE	Opamp0 power level Default Value: 0 **0x0: OFF :** Off **0x1: LOW :** Low compensation setting (smallest cap, highest GBW). For gain=10: PM=60deg @ Cload=50pF for the output to pin driver and 10pF for the internal only driver **0x2: MEDIUM :** Medium compensation setting. For gain=4: PM=60deg @ Cload=50pF for the output to pin driver and 10pF for the internal only driver. **0x3: HIGH :** Highest compensation (largest cap, lowest GBW). For gain=1: PM=60deg @ Cload=50pF for the output to pin driver and 10pF for the internal only driver

18.1.3 CTBM0_OA_RES1_CTRL

Opamp1 and resistor1 control

Address: 0x40300008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	None	RW	RW	
HW Access	R	R	R	R	None	R	R	
Name	OA1_DSI_LEVEL	OA1_BY-PASS_DSI_SYNC	OA1_HYST_EN	OA1_COM-P_EN	None	OA1_DRIVE_STR_-SEL	OA1_PWR_MODE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW	None	RW	
HW Access	None				R	None	R	
Name	None [15:12]				OA1_PUMP_EN	None	OA1_COMPINT [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
11	OA1_PUMP_EN	Opamp1 pump enable Default Value: 0
9 : 8	OA1_COMPINT	Opamp1 comparator edge detect for interrupt and pulse mode of DSI (trigger) Default Value: 0 **0x0: DISABLE :** Disabled, no interrupts will be detected **0x1: RISING :** Rising edge

18.1.3 CTBM0_OA_RES1_CTRL (continued)

		0x2: FALLING : Falling edge **0x3: BOTH :** Both rising and falling edges
7	OA1_DSI_LEVEL	Opamp1 comparator DSI (trigger) out level : 0=pulse, each time an edge is detected (see OA1_COMPINT) a pulse is sent out on DSI 1=level, DSI output is a synchronized version of the comparator output Default Value: 0
6	OA1_BY-PASS_DSI_SYNC	Opamp1 bypass comparator output synchronization for DSI output: 0=synchronize, 1=bypass Default Value: 0
5	OA1_HYST_EN	Opamp1 hysteresis enable (10mV) Default Value: 0
4	OA1_COMP_EN	Opamp1 comparator enable Default Value: 0
2	OA1_DRIVE_STR_SEL	Opamp1 output strenght select 0=1x, 1=10x Default Value: 0
1 : 0	OA1_PWR_MODE	Opamp1 power level: see description of OA0_PWR_MODE Default Value: 0

18.1.4 CTBM0_COMP_STAT

Comparator status

Address: 0x4030000C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							W
Name	None [7:1]							OA0_-COMP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							R
HW Access	None							W
Name	None [23:17]							OA1_-COMP

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
16	OA1_COMP	Opamp1 current comparator status Default Value: 0
0	OA0_COMP	Opamp0 current comparator status Default Value: 0

18.1.5 CTBM0_INTR

Interrupt request register

Address: 0x40300020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1C	RW1C
HW Access	None						RW1S	RW1S
Name	None [7:2]						COMP1	COMP0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	COMP1	Comparator 1 Interrupt: hardware sets this interrupt when comparator 1 triggers. Write with '1' to clear bit. Default Value: 0
0	COMP0	Comparator 0 Interrupt: hardware sets this interrupt when comparator 0 triggers. Write with '1' to clear bit. Default Value: 0

18.1.6 CTBM0_INTR_SET

Interrupt request set register

Address: 0x40300024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1S	RW1S
HW Access	None						A	A
Name	None [7:2]						COMP1_SET	COMP0_SET

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	COMP1_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
0	COMP0_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

18.1.7 CTBM0_INTR_MASK

Interrupt request mask

Address: 0x40300028

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						COMP1_MASK	COMP0_MASK

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	COMP1_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
0	COMP0_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0

18.1.8 CTBM0_INTR_MASKED

Interrupt request masked

Address: 0x4030002C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						W	W
Name	None [7:2]						COMP1_MASKED	COMP0_MASKED

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	COMP1_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
0	COMP0_MASKED	Logical and of corresponding request and mask bits. Default Value: 0

18.1.9 CTBM0_DFT_CTRL

Was 'Analog DfT controls', now used as Risk Mitigation bits (RMP)

Address: 0x40300030

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW		
HW Access	None					R		
Name	None [7:3]					DFT_MODE [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	DFT_EN	None [30:24]						

Bits	Name	Description
31	DFT_EN	this bit is combined with the 3 bits 2:0, to form RMP[3:0] Default Value: 0
2 : 0	DFT_MODE	this bit is combined with bit 31, to form RMP[3:0], it must always be written with '3' for correct operation. Default Value: 0

18.1.10 CTBM0_OA0_SW

Opamp0 switch control

Address: 0x40300080

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1S	RW1S	None	RW1S
HW Access	None				RW1C	RW1C	None	RW1C
Name	None [7:4]				OA0P_A30	OA0P_A20	None	OA0P_A00

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW1S	None					RW1S
HW Access	None	RW1C	None					RW1C
Name	None	OA0M_A81	None [13:9]					OA0M_A11

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW1S	None		RW1S	None	
HW Access	None		RW1C	None		RW1C	None	
Name	None [23:22]		OA0O_D81	None [20:19]		OA0O_D51	None [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
21	OA0O_D81	Opamp0 output switch to short 1x with 10x drive Default Value: 0
18	OA0O_D51	Opamp0 output sarbus0 (ctbbus2 in CTB) Default Value: 0
14	OA0M_A81	Opamp0 negative terminal Opamp0 output Default Value: 0
8	OA0M_A11	Opamp0 negative terminal P1 Default Value: 0
3	OA0P_A30	Opamp0 positive terminal ctbbus0 Default Value: 0
2	OA0P_A20	Opamp0 positive terminal P0 Default Value: 0
0	OA0P_A00	Opamp0 positive terminal amuxbusa Default Value: 0

18.1.11 CTBM0_OA0_SW_CLEAR

Opamp0 switch control clear

Address: 0x40300084

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1C	RW1C	None	RW1C
HW Access	None				A	A	None	A
Name	None [7:4]				OA0P_A30	OA0P_A20	None	OA0P_A00

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW1C	None					RW1C
HW Access	None	A	None					A
Name	None	OA0M_A81	None [13:9]					OA0M_A11

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW1C	None		RW1C	None	
HW Access	None		A	None		A	None	
Name	None [23:22]		OA0O_D81	None [20:19]		OA0O_D51	None [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
21	OA0O_D81	see corresponding bit in OA0_SW Default Value: 0
18	OA0O_D51	see corresponding bit in OA0_SW Default Value: 0
14	OA0M_A81	see corresponding bit in OA0_SW Default Value: 0
8	OA0M_A11	see corresponding bit in OA0_SW Default Value: 0
3	OA0P_A30	see corresponding bit in OA0_SW Default Value: 0
2	OA0P_A20	see corresponding bit in OA0_SW Default Value: 0
0	OA0P_A00	see corresponding bit in OA0_SW Default Value: 0

18.1.12 CTBM0_OA1_SW

Opamp1 switch control

Address: 0x40300088

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW1S	None		RW1S	RW1S
HW Access	None			RW1C	None		RW1C	RW1C
Name	None [7:5]			OA1P_A43	None [3:2]		OA1P_A13	OA1P_A03

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW1S	None					RW1S
HW Access	None	RW1C	None					RW1C
Name	None	OA1M_A82	None [13:9]					OA1M_A22

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW1S	None	RW1S	RW1S	None	
HW Access	None		RW1C	None	RW1C	RW1C	None	
Name	None [23:22]		OA1O_D82	None	OA1O_D62	OA1O_D52	None [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
21	OA1O_D82	Opamp1 output switch to short 1x with 10x drive Default Value: 0
19	OA1O_D62	Opamp1 output sarbus1 (ctbbus3 in CTB) Default Value: 0
18	OA1O_D52	Opamp1 output sarbus0 (ctbbus2 in CTB) Default Value: 0
14	OA1M_A82	Opamp1 negative terminal Opamp1 output Default Value: 0
8	OA1M_A22	Opamp1 negative terminal P4 Default Value: 0
4	OA1P_A43	Opamp1 positive terminal ctbbus1 Default Value: 0
1	OA1P_A13	Opamp1 positive terminal P5 Default Value: 0
0	OA1P_A03	Opamp1 positive terminal amuxbusb Default Value: 0

18.1.13 CTBM0_OA1_SW_CLEAR

Opamp1 switch control clear

Address: 0x4030008C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW1C	None		RW1C	RW1C
HW Access	None			A	None		A	A
Name	None [7:5]			OA1P_A43	None [3:2]		OA1P_A13	OA1P_A03

Bits	15	14	13	12	11	10	9	8
SW Access	None	RW1C	None					RW1C
HW Access	None	A	None					A
Name	None	OA1M_A82	None [13:9]					OA1M_A22

Bits	23	22	21	20	19	18	17	16
SW Access	None		RW1C	None	RW1C	RW1C	None	
HW Access	None		A	None	A	A	None	
Name	None [23:22]		OA1O_D82	None	OA1O_D62	OA1O_D52	None [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
21	OA1O_D82	see corresponding bit in OA1_SW Default Value: 0
19	OA1O_D62	see corresponding bit in OA1_SW Default Value: 0
18	OA1O_D52	see corresponding bit in OA1_SW Default Value: 0
14	OA1M_A82	see corresponding bit in OA1_SW Default Value: 0
8	OA1M_A22	see corresponding bit in OA1_SW Default Value: 0
4	OA1P_A43	see corresponding bit in OA1_SW Default Value: 0
1	OA1P_A13	see corresponding bit in OA1_SW Default Value: 0
0	OA1P_A03	see corresponding bit in OA1_SW Default Value: 0

18.1.14 CTBM0_CTB_SW_HW_CTRL

CTB bus switch control

Address: 0x403000C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW	None	
HW Access	None				R	R	None	
Name	None [7:4]				P3_HW_C-TRL	P2_HW_C-TRL	None	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	P3_HW_CTRL	for P33, D52, D62 (dsi_out[3]) Default Value: 0
2	P2_HW_CTRL	for P22, D51 (dsi_out[2]) Default Value: 0

18.1.15 CTBM0_CTB_SW_STATUS

CTB bus switch control status

Address: 0x403000C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None	R	R	R	None			
HW Access	None	W	W	W	None			
Name	None	OA1O_D62_STAT	OA1O_D52_STAT	OA0O_D51_STAT	None			

Bits	Name	Description
30	OA1O_D62_STAT	see OA1O_D62 bit in OA1_SW Default Value: 0
29	OA1O_D52_STAT	see OA1O_D52 bit in OA1_SW Default Value: 0
28	OA0O_D51_STAT	see OA0O_D51 bit in OA0_SW Default Value: 0

18.1.16 CTBM0_OA0_OFFSET_TRIM

Opamp0 trim control

Address: 0x40300F00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		OA0_OFFSET_TRIM [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	OA0_OFFSET_TRIM	Opamp0 offset trim Default Value: 0

18.1.17 CTBM0_OA0_SLOPE_OFFSET_TRIM

Opamp0 trim control

Address: 0x40300F04

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		OA0_SLOPE_OFFSET_TRIM [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	OA0_SLOPE_OFF-SET_TRIM	Opamp0 slope offset drift trim Default Value: 0

18.1.18 CTBM0_OA0_COMP_TRIM

Opamp0 trim control

Address: 0x40300F08

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	
HW Access	None						R	
Name	None [7:2]						OA0_COMP_TRIM [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1 : 0	OA0_COMP_TRIM	Opamp 0 Compensation Capacitor Trim Default Value: 0

18.1.19 CTBM0_OA1_OFFSET_TRIM

Opamp1 trim control

Address: 0x40300F0C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		OA1_OFFSET_TRIM [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	OA1_OFFSET_TRIM	Opamp1 offset trim Default Value: 0

18.1.20 CTBM0_OA1_SLOPE_OFFSET_TRIM

Opamp1 trim control

Address: 0x40300F10

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		OA1_SLOPE_OFFSET_TRIM [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	OA1_SLOPE_OFF-SET_TRIM	Opamp1 slope offset drift trim Default Value: 0

18.1.21 CTBM0_OA1_COMP_TRIM

Opamp1 trim control

Address: 0x40300F14

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	
HW Access	None						R	
Name	None [7:2]						OA1_COMP_TRIM [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1 : 0	OA1_COMP_TRIM	Opamp 1 Compensation Capacitor Trim Default Value: 0

19 SAR ADC Registers

This section discusses the SAR ADC registers. It lists all the registers in mapping tables, in address order.

19.1 Register Details

Register	Address	Description
SAR0_CTRL	0x403A0000	Analog control register.
SAR0_SAMPLE_CTRL	0x403A0004	Sample control register.
SAR0_SAMPLE_TIME01	0x403A0010	Sample time specification ST0 and ST1
SAR0_SAMPLE_TIME23	0x403A0014	Sample time specification ST2 and ST3
SAR0_RANGE_THRES	0x403A0018	Global range detect threshold register.
SAR0_RANGE_COND	0x403A001C	Global range detect mode register.
SAR0_CHAN_EN	0x403A0020	Enable bits for the channels
SAR0_START_CTRL	0x403A0024	Start control register (firmware trigger).
SAR0_DFT_CTRL	0x403A0030	DFT control register.
SAR0_CHAN_CONFIG0	0x403A0080	Channel configuration register.
SAR0_CHAN_CONFIG1	0x403A0084	Channel configuration register.. See SAR0_CHAN_CONFIG0 for the details of bit fields.
SAR0_CHAN_CONFIG2	0x403A0088	Channel configuration register.. See SAR0_CHAN_CONFIG0 for the details of bit fields.
SAR0_CHAN_CONFIG3	0x403A008C	Channel configuration register.. See SAR0_CHAN_CONFIG0 for the details of bit fields.
SAR0_CHAN_CONFIG4	0x403A0090	Channel configuration register.. See SAR0_CHAN_CONFIG0 for the details of bit fields.
SAR0_CHAN_CONFIG5	0x403A0094	Channel configuration register.. See SAR0_CHAN_CONFIG0 for the details of bit fields.
SAR0_CHAN_CONFIG6	0x403A0098	Channel configuration register.. See SAR0_CHAN_CONFIG0 for the details of bit fields.
SAR0_CHAN_CONFIG7	0x403A009C	Channel configuration register.. See SAR0_CHAN_CONFIG0 for the details of bit fields.
SAR0_CHAN_CONFIG8	0x403A00A0	Channel configuration register.. See SAR0_CHAN_CONFIG0 for the details of bit fields.
SAR0_CHAN_CONFIG9	0x403A00A4	Channel configuration register.. See SAR0_CHAN_CONFIG0 for the details of bit fields.
SAR0_CHAN_CONFIG10	0x403A00A8	Channel configuration register.. See SAR0_CHAN_CONFIG0 for the details of bit fields.
SAR0_CHAN_CONFIG11	0x403A00AC	Channel configuration register.. See SAR0_CHAN_CONFIG0 for the details of bit fields.
SAR0_CHAN_CONFIG12	0x403A00B0	Channel configuration register.. See SAR0_CHAN_CONFIG0 for the details of bit fields.
SAR0_CHAN_CONFIG13	0x403A00B4	Channel configuration register.. See SAR0_CHAN_CONFIG0 for the details of bit fields.
SAR0_CHAN_CONFIG14	0x403A00B8	Channel configuration register.. See SAR0_CHAN_CONFIG0 for the details of bit fields.
SAR0_CHAN_CONFIG15	0x403A00BC	Channel configuration register.. See SAR0_CHAN_CONFIG0 for the details of bit fields.
SAR0_CHAN_WORK0	0x403A0100	Channel working data register
SAR0_CHAN_WORK1	0x403A0104	Channel working data register. See SAR0_CHAN_WORK0 for the details of bit fields.

Register	Address	Description
SAR0_CHAN_WORK2	0x403A0108	Channel working data register. See SAR0_CHAN_WORK0 for the details of bit fields.
SAR0_CHAN_WORK3	0x403A010C	Channel working data register. See SAR0_CHAN_WORK0 for the details of bit fields.
SAR0_CHAN_WORK4	0x403A0110	Channel working data register. See SAR0_CHAN_WORK0 for the details of bit fields.
SAR0_CHAN_WORK5	0x403A0114	Channel working data register. See SAR0_CHAN_WORK0 for the details of bit fields.
SAR0_CHAN_WORK6	0x403A0118	Channel working data register. See SAR0_CHAN_WORK0 for the details of bit fields.
SAR0_CHAN_WORK7	0x403A011C	Channel working data register. See SAR0_CHAN_WORK0 for the details of bit fields.
SAR0_CHAN_WORK8	0x403A0120	Channel working data register. See SAR0_CHAN_WORK0 for the details of bit fields.
SAR0_CHAN_WORK9	0x403A0124	Channel working data register. See SAR0_CHAN_WORK0 for the details of bit fields.
SAR0_CHAN_WORK10	0x403A0128	Channel working data register. See SAR0_CHAN_WORK0 for the details of bit fields.
SAR0_CHAN_WORK11	0x403A012C	Channel working data register. See SAR0_CHAN_WORK0 for the details of bit fields.
SAR0_CHAN_WORK12	0x403A0130	Channel working data register. See SAR0_CHAN_WORK0 for the details of bit fields.
SAR0_CHAN_WORK13	0x403A0134	Channel working data register. See SAR0_CHAN_WORK0 for the details of bit fields.
SAR0_CHAN_WORK14	0x403A0138	Channel working data register. See SAR0_CHAN_WORK0 for the details of bit fields.
SAR0_CHAN_WORK15	0x403A013C	Channel working data register. See SAR0_CHAN_WORK0 for the details of bit fields.
SAR0_CHAN_RESULT0	0x403A0180	Channel result data register
SAR0_CHAN_RESULT1	0x403A0184	Channel result data register. See SAR0_CHAN_RESULT0 for the details of bit fields.
SAR0_CHAN_RESULT2	0x403A0188	Channel result data register. See SAR0_CHAN_RESULT0 for the details of bit fields.
SAR0_CHAN_RESULT3	0x403A018C	Channel result data register. See SAR0_CHAN_RESULT0 for the details of bit fields.
SAR0_CHAN_RESULT4	0x403A0190	Channel result data register. See SAR0_CHAN_RESULT0 for the details of bit fields.
SAR0_CHAN_RESULT5	0x403A0194	Channel result data register. See SAR0_CHAN_RESULT0 for the details of bit fields.
SAR0_CHAN_RESULT6	0x403A0198	Channel result data register. See SAR0_CHAN_RESULT0 for the details of bit fields.
SAR0_CHAN_RESULT7	0x403A019C	Channel result data register. See SAR0_CHAN_RESULT0 for the details of bit fields.
SAR0_CHAN_RESULT8	0x403A01A0	Channel result data register. See SAR0_CHAN_RESULT0 for the details of bit fields.
SAR0_CHAN_RESULT9	0x403A01A4	Channel result data register. See SAR0_CHAN_RESULT0 for the details of bit fields.
SAR0_CHAN_RESULT10	0x403A01A8	Channel result data register. See SAR0_CHAN_RESULT0 for the details of bit fields.
SAR0_CHAN_RESULT11	0x403A01AC	Channel result data register. See SAR0_CHAN_RESULT0 for the details of bit fields.
SAR0_CHAN_RESULT12	0x403A01B0	Channel result data register. See SAR0_CHAN_RESULT0 for the details of bit fields.
SAR0_CHAN_RESULT13	0x403A01B4	Channel result data register. See SAR0_CHAN_RESULT0 for the details of bit fields.
SAR0_CHAN_RESULT14	0x403A01B8	Channel result data register. See SAR0_CHAN_RESULT0 for the details of bit fields.
SAR0_CHAN_RESULT15	0x403A01BC	Channel result data register. See SAR0_CHAN_RESULT0 for the details of bit fields.
SAR0_CHAN_WORK_VALID	0x403A0200	Channel working data register valid bits
SAR0_CHAN_RESULT_VALID	0x403A0204	Channel result data register valid bits
SAR0_STATUS	0x403A0208	Current status of internal SAR registers (mostly for debug)
SAR0_AVG_STAT	0x403A020C	Current averaging status (for debug)
SAR0_INTR	0x403A0210	Interrupt request register.
SAR0_INTR_SET	0x403A0214	Interrupt set request register
SAR0_INTR_MASK	0x403A0218	Interrupt mask register.
SAR0_INTR_MASKED	0x403A021C	Interrupt masked request register
SAR0_SATURATE_INTR	0x403A0220	Saturate interrupt request register.
SAR0_SATURATE_INTR_SET	0x403A0224	Saturate interrupt set request register
SAR0_SATURATE_INTR_MASK	0x403A0228	Saturate interrupt mask register.
SAR0_SATURATE_INTR_MASKED	0x403A022C	Saturate interrupt masked request register

Register	Address	Description
SAR0_RANGE_INTR	0x403A0230	Range detect interrupt request register.
SAR0_RANGE_INTR_SET	0x403A0234	Range detect interrupt set request register
SAR0_RANGE_INTR_MASK	0x403A0238	Range detect interrupt mask register.
SAR0_RANGE_INTR_MASK	0x403A023C	Range interrupt masked request register
SAR0_INTR_CAUSE	0x403A0240	Interrupt cause register
SAR0_INJ_CHAN_CONFIG	0x403A0280	Injection channel configuration register.
SAR0_INJ_RESULT	0x403A0290	Injection channel result register
SAR0_MUX_SWITCH0	0x403A0300	SARMUX Firmware switch controls
SAR0_MUX_SWITCH_CLEAR0	0x403A0304	SARMUX Firmware switch control clear
SAR0_MUX_SWITCH1	0x403A0308	SARMUX Firmware switch controls
SAR0_MUX_SWITCH_CLEAR1	0x403A030C	SARMUX Firmware switch control clear
SAR0_MUX_SWITCH_HW_CTRL	0x403A0340	SARMUX switch hardware control
SAR0_MUX_SWITCH_STATUS	0x403A0348	SARMUX switch status
SAR0_PUMP_CTRL	0x403A0380	Switch pump control
SAR0_ANA_TRIM	0x403A0F00	Analog trim register.
SAR0_WOUNDING	0x403A0F04	SAR wounding register

19.1.1 SAR0_CTRL

Analog control register.

Address: 0x403A0000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW			None			
HW Access	R	R			None			
Name	VREF_BY-P_CAP_EN	VREF_SEL [6:4]			None [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	RW		RW	None	RW			None
HW Access	R		R	None	R			None
Name	PWR_CTRL_VREF [15:14]		SAR_HW_CTRL_NEGVREF	None	NEG_SEL [11:9]			None

Bits	23	22	21	20	19	18	17	16
SW Access	None			RW	RW			
HW Access	None			R	R			
Name	None [23:21]			BOOST-PUMP_EN	SPARE [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW	RW	RW	RW	RW	None	RW	
HW Access	R	R	R	R	R	None	R	
Name	ENABLED	SWITCH_-DISABLE	DSI_MODE	DSI_SYN-C_CONFIG	DEEPS-LEEP_ON	None	ICONT_LV [25:24]	

Bits	Name	Description
31	ENABLED	Before enabling always make sure the SAR is idle (STATUS.BUSY==0) - 0: SAR IP disabled (put analog in power down and stop clocks), also can clear FW_TRIGGER and INJ_START_EN (if not tailgaiting) on write. - 1: SAR IP enabled. Default Value: 0
30	SWITCH_DISABLE	Disable SAR sequencer from enabling routing switches (note DSI and firmware can always close switches independent of this control) - 0: Normal mode, SAR sequencer changes switches according to pin address in channel configurations - 1: Switches disabled, SAR sequencer does not enable any switches, it is the responsibility of the firmware or UDBs (through DSI) to set the switches to route the signal to be converted through the SARMUX Default Value: 0

19.1.1 SAR0_CTRL (continued)

29	DSI_MODE	SAR sequencer takes configuration from DSI signals (note this also has the same effect as SWITCH_DISABLE==1) - 0: Normal mode, SAR sequencer operates according to CHAN_EN enables and CHAN_CONFIG channel configurations - 1: CHAN_EN, INJ_START_EN and channel configurations in CHAN_CONFIG and INJ_CHAN_CONFIG are ignored Default Value: 0
28	DSI_SYNC_CONFIG	- 0: bypass clock domain synchronisation of the DSI config signals. - 1: synchronize the DSI config signals to peripheral clock domain. Default Value: 1
27	DEEPSLEEP_ON	- 0: SARMUX IP disabled off during DeepSleep power mode - 1: SARMUX IP remains enabled during DeepSleep power mode (if ENABLED=1) Default Value: 0
25 : 24	ICONT_LV	SARADC low power mode. Default Value: 0 **0x0: NORMAL_PWR :** normal power (default), max clk_sar is 18MHz. **0x1: HALF_PWR :** 1/2 power mode, max clk_sar is 9MHz. **0x2: MORE_PWR :** 1.333 power mode, max clk_sar is 18MHz. **0x3: QUARTER_PWR :** 1/4 power mode, max clk_sar is 4.5MHz.
20	BOOSTPUMP_EN	SARADC internal pump: 0=disabled: pump output is VDDA, 1=enabled: pump output is boosted. Default Value: 0
19 : 16	SPARE	Spare controls, not yet designated, for late changes done with an ECO Default Value: 0
15 : 14	PWR_CTRL_VREF	VREF buffer low power mode. Default Value: 0 **0x0: NORMAL_PWR :** normal power (default), bypass cap, max clk_sar is 18MHz. **0x1: HALF_PWR :** deprecated **0x2: THIRD_PWR :** Invalid for PSoC4A, otherwise 2X power, no bypass cap, max clk_sar is 1.8MHz

19.1.1 SAR0_CTRL (continued)

		0x3: QUARTER_PWR : deprecated
13	SAR_HW_C-TRL_NEGVREF	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for VREF to NEG switch. Default Value: 0
11 : 9	NEG_SEL	SARADC internal NEG selection for Single ended conversion Default Value: 0 **0x0: VSSA_KELVIN :** NEG input of SARADC is connected to "vssa_kelvin", gives more precision around zero. Note this opens both SARADC internal switches, therefore use this value to insert a break-before-make cycle on those switches when SWITCH_DISABLE is high. **0x1: ART_VSSA :** NEG input of SARADC is connected to VSSA in AROUTE close to the SARADC **0x2: P1 :** NEG input of SARADC is connected to P1 pin of SARMUX **0x3: P3 :** NEG input of SARADC is connected to P3 pin of SARMUX **0x4: P5 :** NEG input of SARADC is connected to P5 pin of SARMUX **0x5: P7 :** NEG input of SARADC is connected to P7 pin of SARMUX **0x6: ACORE :** NEG input of SARADC is connected to an ACORE in AROUTE **0x7: VREF :** NEG input of SARADC is shorted with VREF input of SARADC.
7	VREF_BYP_CAP_EN	VREF bypass cap enable for when VREF buffer is on Default Value: 0
6 : 4	VREF_SEL	SARADC internal VREF selection. Default Value: 0

19.1.1 SAR0_CTRL (continued)

0x0: VREF0 :

VREF0 from PRB (VREF buffer on)

0x1: VREF1 :

VREF1 from PRB (VREF buffer on)

0x2: VREF2 :

VREF2 from PRB (VREF buffer on)

0x3: VREF_AROUTE :

VREF from AROUTE (VREF buffer on)

0x4: VBGR :

1.024V from BandGap (VREF buffer on)

0x5: VREF_EXT :

External precision Vref direct from a pin (low impedance path).

0x6: VDDA_DIV_2 :

Vdda/2 (VREF buffer on)

0x7: VDDA :

Vdda.

19.1.2 SAR0_SAMPLE_CTRL

Sample control register.

Address: 0x403A0004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW			RW	RW	RW	RW
HW Access	R	R			R	R	R	R
Name	AVG_SHIFT	AVG_CNT [6:4]			DIFFEREN-TIAL_-SIGNED	SIN-GLE_END-ED_SIGNE D	LEFT_ALIG N	SUB_RES-OLUTION

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW	RW	RW	RW
HW Access	None				R	R	R	R
Name	None [23:20]				DSI_SYN-C_TRIG-GER	DSI_TRIG-GER_LEV-EL	DSI_TRIG-GER_EN	CONTINU-OUS

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	EO-S_DSI_OU T_EN	None [30:24]						

Bits	Name	Description
31	EOS_DSI_OUT_EN	Enable to output EOS_INTR to DSI. When enabled each time EOS_INTR is set by the hardware also a pulse is send on the dsi_eos signal. Default Value: 0
19	DSI_SYNC_TRIGGER	- 0: bypass clock domain synchronisation of the DSI trigger signal. - 1: synchronize the DSI trigger signal to the SAR clock domain, if needed an edge detect is done in the peripheral clock domain. Default Value: 1
18	DSI_TRIGGER_LEVEL	- 0: DSI trigger signal is a pulse input, a positive edge detected on the DSI trigger signal triggers a new scan. - 1: DSI trigger signal is a level input, as long as the DSI trigger signal remains high the SAR will do continuous scans. Default Value: 0

19.1.2 SAR0_SAMPLE_CTRL (continued)

17	DSI_TRIGGER_EN	- 0: firmware trigger only: disable hardware (DSI) trigger. - 1: enable hardware (DSI) trigger (e.g. from TCPWM, GPIO or UDB). Default Value: 0
16	CONTINUOUS	- 0: Wait for next FW_TRIGGER (one shot) or hardware (DSI) trigger (e.g. from TPWM for periodic triggering) before scanning enabled channels. - 1: Continuously scan enabled channels, ignore triggers. Default Value: 0
7	AVG_SHIFT	Averaging shifting: after averaging the result is shifted right to fit in the sample resolution. For averaging the sample resolution is the highest resolution allowed by wounding. Default Value: 0
6 : 4	AVG_CNT	Averaging Count for channels that have over sampling enabled (AVG_EN). A channel will be sampled back to back (1<<(AVG_CNT+1)) = [2..256] times before the result is stored and the next enabled channel is sampled (1st order accumulate and dump filter). If shifting is not enabled (AVG_SHIFT=0) then the result is forced to shift right so that is fits in 16 bits, so right shift is done by max(0,AVG_CNT-3). Default Value: 0
3	DIFFERENTIAL_SIGNED	Output data from a differential conversion as a signed value Default Value: 1 **0x0: UNSIGNED :** result data is unsigned (zero extended if needed) **0x1: SIGNED :** Default: result data is signed (sign extended if needed)
2	SINGLE_ENDED_-SIGNED	Output data from a single ended conversion as a signed value Default Value: 0 **0x0: UNSIGNED :** Default: result data is unsigned (zero extended if needed) **0x1: SIGNED :** result data is signed (sign extended if needed)
1	LEFT_ALIGN	Left align data in data[15:0], default data is right aligned in data[11:0], with sign extension to 16 bits if the channel is differential. Default Value: 0
0	SUB_RESOLUTION	Conversion resolution for channels that have sub-resolution enabled (RESOLUTION=1) (otherwise resolution is 12-bit). Default Value: 0 **0x0: 8B :** 8-bit. **0x1: 10B :** 10-bit.

19.1.3 SAR0_SAMPLE_TIME01

Sample time specification ST0 and ST1

Address: 0x403A0010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SAMPLE_TIME0 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						SAMPLE_TIME0 [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	SAMPLE_TIME1 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None						RW	
HW Access	None						R	
Name	None [31:26]						SAMPLE_TIME1 [25:24]	

Bits	Name	Description
25 : 16	SAMPLE_TIME1	Sample time1 Default Value: 4
9 : 0	SAMPLE_TIME0	Sample time0 (aperture) in ADC clock cycles. Note that actual sample time is half a clock less than specified here. The minimum sample time is 194ns, which is 3.5 cycles (4 in this field) with an 18MHz clock. Minimum legal value in this register is 2. Default Value: 4

19.1.4 SAR0_SAMPLE_TIME23

Sample time specification ST2 and ST3

Address: 0x403A0014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SAMPLE_TIME2 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	
HW Access	None						R	
Name	None [15:10]						SAMPLE_TIME2 [9:8]	

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	SAMPLE_TIME3 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None						RW	
HW Access	None						R	
Name	None [31:26]						SAMPLE_TIME3 [25:24]	

Bits	Name	Description
25 : 16	SAMPLE_TIME3	Sample time3 Default Value: 4
9 : 0	SAMPLE_TIME2	Sample time2 Default Value: 4

19.1.5 SAR0_RANGE_THRES

Global range detect threshold register.

Address: 0x403A0018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	RANGE_LOW [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	RANGE_LOW [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	RANGE_HIGH [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	RANGE_HIGH [31:24]							

Bits	Name	Description
31 : 16	RANGE_HIGH	High threshold for range detect. Default Value: 0
15 : 0	RANGE_LOW	Low threshold for range detect. Default Value: 0

19.1.6 SAR0_RANGE_COND

Global range detect mode register.

Address: 0x403A001C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None					
HW Access	R		None					
Name	RANGE_COND [31:30]		None [29:24]					

Bits	Name	Description
31 : 30	RANGE_COND	Range condition select. Default Value: 0 **0x0: BELOW :** result < RANGE_LOW **0x1: INSIDE :** RANGE_LOW <= result < RANGE_HIGH **0x2: ABOVE :** RANGE_HIGH <= result **0x3: OUTSIDE :** result < RANGE_LOW || RANGE_HIGH <= result

19.1.7 SAR0_CHAN_EN

Enable bits for the channels

Address: 0x403A0020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CHAN_EN [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CHAN_EN [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CHAN_EN	Channel enable. - 0: the corresponding channel is disabled. - 1: the corresponding channel is enabled, it will be included in the next scan. Default Value: 0

19.1.8 SAR0_START_CTRL

Start control register (firmware trigger).

Address: 0x403A0024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1S
HW Access	None							RW1C
Name	None [7:1]							FW_TRIG-GER

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	FW_TRIGGER	When firmware writes a 1 here it will trigger the next scan of enabled channels, hardware clears this bit when the scan started with this trigger is completed. If scanning continuously the trigger is ignored and hardware clears this bit after the next scan is done. This bit is also cleared when the SAR is disabled. Default Value: 0

19.1.9 SAR0_DFT_CTRL

DFT control register.

Address: 0x403A0030

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						HIZ	DLY_INC

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None	RW			RW			
HW Access	None	R			R			
Name	None	DFT_OUTC [22:20]			DFT_INC [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None	RW	RW	RW			
HW Access	R	None	R	R	R			
Name	ADFT_OVERRIDE	None	DCEN	EN_CSEL_DFT	SEL_CSEL_DFT [27:24]			

Bits	Name	Description
31	ADFT_OVERRIDE	During deepsleep/ hibernate mode keep SARMUX active, i.e. do not open all switches (disconnect), to be used for ADFT Default Value: 0
29	DCEN	Delay Control Enable for latch. - 0: doubles the latch enable time. - 1: normal latch enable time (default). Default Value: 0
28	EN_CSEL_DFT	Mux select signal for DAC control Default Value: 0
27 : 24	SEL_CSEL_DFT	Usage 1: DFT bits for DAC array Usage 2: For [0]=1 (when dcen=0): Delay timing for latch enable increased by 20% [1]=1: comparator preamp power level increased by 25% Default Value: 0
22 : 20	DFT_OUTC	DFT control for preamp outputs Default Value: 0

19.1.9 SAR0_DFT_CTRL (continued)

19 : 16	DFT_INC	DFT control for preamp inputs Default Value: 0
1	HIZ	DFT control for getting higher input impedance, must be 1 (0 is deprecated) Default Value: 1
0	DLY_INC	DFT control: Control for delay circuits on sampling phase, =1 doubes the non-overlap delay Default Value: 0

19.1.10 SAR0_CHAN_CONFIG0

Channel configuration register.

Address: 0x403A0080

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	PORT_ADDR [6:4]			None	PIN_ADDR [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW		None	RW	RW	RW
HW Access	None		R		None	R	R	R
Name	None [15:14]		SAMPLE_TIME_SEL [13:12]		None	AVG_EN	RESOLU-TION	DIFFEREN-TIAL_EN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	DSI_OUT_EN	None [30:24]						

Bits	Name	Description
31	DSI_OUT_EN	DSI data output enable for this channel. - 0: the conversion result for this channel is only stored in the channel data register and the corresponding CHAN_DATA_VALID bit is set. - 1: the conversion result for this channel is stored in the channel data register and the corresponding CHAN_DATA_VALID bit is set. The same data (same formating), together with the channel number, is sent out on the DSI communication channel for processing in UDBs. Default Value: 0
13 : 12	SAMPLE_TIME_SEL	Sample time select: select which of the 4 global sample times to use for this channel Default Value: 0
10	AVG_EN	Averaging enable for this channel. If set the AVG_CNT and AVG_SHIFT settings are used for sampling the addressed pin(s) Default Value: 0
9	RESOLUTION	Resolution for this channel. When AVG_EN is set this bit is ignored and always a 12-bit resolution (or highest resolution allowed by wounding) is used for this channel. Default Value: 0

19.1.10 SAR0_CHAN_CONFIG0 (continued)

		0x0: MAXRES : The maximum resolution is used for this channel (maximum resolution depends on wounding). **0x1: SUBRES :** The resolution specified by SUB_RESOLUTION in the SAR_SAMPLE_CTRL register is used for this channel.
8	DIFFERENTIAL_EN	Differential enable for this channel. - 0: The voltage on the addressed pin is measured (Single-ended) and the resulting value is stored in the corresponding data register. - 1: The differential voltage on the addressed pin pair is measured and the resulting value is stored in the corresponding data register. (PIN_ADDR[0] is ignored). Default Value: 0
6 : 4	PORT_ADDR	Address of the port that contains the pin to be sampled by this channel. Default Value: 0 **0x0: SARMUX :** SARMUX pins. **0x1: CTB0 :** CTB0 **0x2: CTB1 :** CTB1 **0x3: CTB2 :** CTB2 **0x4: CTB3 :** CTB3 **0x5: AROUTE_VIRT2 :** AROUTE virtual port2 (VPORT2) **0x6: AROUTE_VIRT1 :** AROUTE virtual port1 (VPORT1) **0x7: SARMUX_VIRT :** SARMUX virtual port (VPORT0)

19.1.10 SAR0_CHAN_CONFIG0 (continued)

2 : 0	PIN_ADDR	Address of the pin to be sampled by this channel. If differential is enabled then PIN_ADDR[0] is ignored and considered to be 0, i.e. PIN_ADDR points to the even pin of a pin pair. For differential the even pin of the pair is connected to Vplus and the odd pin of the pair is connected to Vminus. Default Value: 0

19.1.11 SAR0_CHAN_WORK0

Channel working data register

Address: 0x403A0100

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	WORK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	WORK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	None						
HW Access	W	None						
Name	CHAN_WORK_VALID_MIR	None [30:24]						

Bits	Name	Description
31	CHAN_WORK_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_WORK_VALID register Default Value: 0
15 : 0	WORK	SAR conversion working data of the channel. The data is written here right after sampling this channel. Default Value: Undefined

19.1.12 SAR0_CHAN_RESULT0

Channel result data register

Address: 0x403A0180

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	RESULT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	RESULT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	R	None				
HW Access	W	W	W	None				
Name	CHAN_RESULT_VALID_MIR	RANGE_INTR_MIR	SATURATE_INTR_MIR	None [28:24]				

Bits	Name	Description
31	CHAN_RESULT_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_RESULT_VALID register Default Value: 0
30	RANGE_INTR_MIR	mirror bit of corresponding bit in SAR_RANGE_INTR register Default Value: 0
29	SATURATE_INTR_MIR	mirror bit of corresponding bit in SAR_SATURATE_INTR register Default Value: 0
15 : 0	RESULT	SAR conversion result of the channel. The data is copied here from the WORK field after all enabled channels in this scan have been sampled. Default Value: Undefined

19.1.13 SAR0_CHAN_WORK_VALID

Channel working data register valid bits

Address: 0x403A0200

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	CHAN_WORK_VALID [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	CHAN_WORK_VALID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CHAN_WORK_VALID	If set the corresponding WORK data is valid, i.e. was already sampled during the current scan. Default Value: 0

19.1.14 SAR0_CHAN_RESULT_VALID

Channel result data register valid bits

Address: 0x403A0204

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	CHAN_RESULT_VALID [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	CHAN_RESULT_VALID [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	CHAN_RESULT_VALID	If set the corresponding RESULT data is valid, i.e. was sampled during the last scan. Default Value: 0

19.1.15 SAR0_STATUS

Current status of internal SAR registers (mostly for debug)

Address: 0x403A0208

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			R				
HW Access	None			W				
Name	None [7:5]			CUR_CHAN [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	None					
HW Access	W	W	None					
Name	BUSY	SW_VREF_NEG	None [29:24]					

Bits	Name	Description
31	BUSY	If high then the SAR is busy with a conversion. This bit is always high when CONTINUOUS is set. Firmware should wait for this bit to be low before putting the SAR in power down. Default Value: 0
30	SW_VREF_NEG	the current switch status, including DSI and sequencer controls, of the switch in the SARADC that shorts NEG with VREF input (see NEG_SEL). Default Value: 0
4 : 0	CUR_CHAN	current channel being sampled (channel 16 indicates the injection channel), only valid if BUSY. Default Value: 0

19.1.16 SAR0_AVG_STAT

Current averaging status (for debug)

Address: 0x403A020C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	CUR_AVG_ACCU [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	CUR_AVG_ACCU [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None				R			
HW Access	None				W			
Name	None [23:20]				CUR_AVG_ACCU [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	CUR_AVG_CNT [31:24]							

Bits	Name	Description
31 : 24	CUR_AVG_CNT	the current value of the averaging counter. Note that the value shown is updated after the sampling time and therefore runs ahead of the accumulator update. Default Value: 0
19 : 0	CUR_AVG_ACCU	the current value of the averaging accumulator Default Value: 0

19.1.17 SAR0_INTR

Interrupt request register.

Address: 0x403A0210

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
Name	INJ_COLLI-SION_INTR	IN-J_RANGE_I NTR	INJ_SATU-RATE_INTR	IN-J_EOC_IN-TR	DSI_COLLI-SION_INTR	FW_COLLI-SION_INTR	OVER-FLOW_IN-TR	EOS_INTR

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	INJ_COLLISION_INTR	Injection Collision Interrupt: hardware sets this interrupt when the injection trigger signal is asserted (INJ_START_EN==1 && INJ_TAILGATING==0) while the SAR is BUSY. Raising this interrupt is delayed to when the sampling of the injection channel has been completed, i.e. not when the preceeding scan with which this trigger collided is completed. When this interrupt is set it implies that the injection channel was sampled later than was intended. Write with '1' to clear bit. Default Value: 0
6	INJ_RANGE_INTR	Injection Range detect Interrupt: hardware sets this interrupt if the injection conversion result (after averaging) met the condition specified by the SAR_RANGE registers. Write with '1' to clear bit. Default Value: 0
5	INJ_SATURATE_INTR	Injection Saturation Interrupt: hardware sets this interrupt if an injection conversion result (before averaging) is either 0x000 or 0xFFF (for 12-bit resolution), this is an indication that the ADC likely saturated. Write with '1' to clear bit. Default Value: 0

19.1.17 SAR0_INTR (continued)

4	INJ_EOC_INTR	Injection End of Conversion Interrupt: hardware sets this interrupt after completing the conversion for the injection channel (irrespective of if tailgating was used). Write with '1' to clear bit. Default Value: 0
3	DSI_COLLISION_INTR	DSI Collision Interrupt: hardware sets this interrupt when the DSI trigger signal is asserted while the SAR is BUSY. Raising this interrupt is delayed to when the scan caused by the DSI trigger has been completed, i.e. not when the preceeding scan with which this trigger collided is completed. When this interrupt is set it implies that the channels were sampled later than was intended (jitter). Write with '1' to clear bit. Default Value: 0
2	FW_COLLISION_INTR	Firmware Collision Interrupt: hardware sets this interrupt when FW_TRIGGER is asserted while the SAR is BUSY. Raising this interrupt is delayed to when the scan caused by the FW_TRIGGER has been completed, i.e. not when the preceeding scan with which this trigger collided is completed. When this interrupt is set it implies that the channels were sampled later than was intended (jitter). Write with '1' to clear bit. Default Value: 0
1	OVERFLOW_INTR	Overflow Interrupt: hardware sets this interrupt when it sets a new EOS_INTR while that bit was not yet cleared by the firmware. Write with '1' to clear bit. Default Value: 0
0	EOS_INTR	End Of Scan Interrupt: hardware sets this interrupt after completing a scan of all the enabled channels. Write with '1' to clear bit. Default Value: 0

19.1.18 SAR0_INTR_SET

Interrupt set request register

Address: 0x403A0214

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	A	A	A	A	A	A	A	A
Name	INJ_COLLI-SION_SET	IN-J_RANGE_SET	INJ_SATU-RATE_SET	IN-J_EOC_SET	DSI_COLLI-SION_SET	FW_COLLI-SION_SET	OVER-FLOW_SET	EOS_SET

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	INJ_COLLISION_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
6	INJ_RANGE_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
5	INJ_SATURATE_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
4	INJ_EOC_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
3	DSI_COLLISION_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
2	FW_COLLISION_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0
1	OVERFLOW_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

19.1.18 SAR0_INTR_SET (continued)

0	EOS_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

19.1.19 SAR0_INTR_MASK

Interrupt mask register.

Address: 0x403A0218

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	INJ_COLLISION_MASK	INJ_RANGE_MASK	INJ_SATURATE_MASK	INJ_EOC_MASK	DSI_COLLISION_MASK	FW_COLLISION_MASK	OVERFLOW_MASK	EOS_MASK

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	INJ_COLLISION_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
6	INJ_RANGE_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
5	INJ_SATURATE_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
4	INJ_EOC_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
3	DSI_COLLISION_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
2	FW_COLLISION_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0
1	OVERFLOW_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0

19.1.19 SAR0_INTR_MASK (continued)

0	EOS_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0

19.1.20 SAR0_INTR_MASKED

Interrupt masked request register

Address: 0x403A021C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	INJ_COLLI-SION_MASKED	IN-J_RANGE_MASKED	INJ_SATU-RATE_MASKED	IN-J_EOC_MASKED	DSI_COLLI-SION_MASKED	FW_COLLI-SION_MASKED	OVER-FLOW_MASKED	EO-S_MASKED

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7	INJ_COLLI-SION_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
6	INJ_RANGE_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
5	INJ_SATU-RATE_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
4	INJ_EOC_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
3	DSI_COLLI-SION_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
2	FW_COLLI-SION_MASKED	Logical and of corresponding request and mask bits. Default Value: 0
1	OVERFLOW_MASKED	Logical and of corresponding request and mask bits. Default Value: 0

19.1.20 SAR0_INTR_MASKED (continued)

0	EOS_MASKED	Logical and of corresponding request and mask bits. Default Value: 0

19.1.21 SAR0_SATURATE_INTR

Saturate interrupt request register.

Address: 0x403A0220

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C							
HW Access	RW1S							
Name	SATURATE_INTR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1C							
HW Access	RW1S							
Name	SATURATE_INTR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	SATURATE_INTR	Saturate Interrupt: hardware sets this interrupt for each channel if a conversion result (before averaging) of that channel is either 0x000 or 0xFFF (for 12-bit resolution), this is an indication that the ADC likely saturated. Write with '1' to clear bit. Default Value: 0

19.1.22 SAR0_SATURATE_INTR_SET

Saturate interrupt set request register

Address: 0x403A0224

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S							
HW Access	A							
Name	SATURATE_SET [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1S							
HW Access	A							
Name	SATURATE_SET [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	SATURATE_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

19.1.23 SAR0_SATURATE_INTR_MASK

Saturate interrupt mask register.

Address: 0x403A0228

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SATURATE_MASK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	SATURATE_MASK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	SATURATE_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0

19.1.24 SAR0_SATURATE_INTR_MASKED

Saturate interrupt masked request register

Address: 0x403A022C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	SATURATE_MASKED [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	SATURATE_MASKED [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	SATURATE_MASKED	Logical and of corresponding request and mask bits. Default Value: 0

19.1.25 SAR0_RANGE_INTR

Range detect interrupt request register.

Address: 0x403A0230

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C							
HW Access	RW1S							
Name	RANGE_INTR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1C							
HW Access	RW1S							
Name	RANGE_INTR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	RANGE_INTR	Range detect Interrupt: hardware sets this interrupt for each channel if the conversion result (after averaging) of that channel met the condition specified by the SAR_RANGE registers. Write with '1' to clear bit. Default Value: 0

19.1.26 SAR0_RANGE_INTR_SET

Range detect interrupt set request register

Address: 0x403A0234

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S							
HW Access	A							
Name	RANGE_SET [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1S							
HW Access	A							
Name	RANGE_SET [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	RANGE_SET	Write with '1' to set corresponding bit in interrupt request register. Default Value: 0

19.1.27 SAR0_RANGE_INTR_MASK

Range detect interrupt mask register.

Address: 0x403A0238

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	RANGE_MASK [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	RANGE_MASK [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	RANGE_MASK	Mask bit for corresponding bit in interrupt request register. Default Value: 0

19.1.28 SAR0_RANGE_INTR_MASKED

Range interrupt masked request register

Address: 0x403A023C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	RANGE_MASKED [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	RANGE_MASKED [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 0	RANGE_MASKED	Logical and of corresponding request and mask bits. Default Value: 0

19.1.29 SAR0_INTR_CAUSE

Interrupt cause register

Address: 0x403A0240

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	INJ_COLLI-SION_MASKED_MIR	IN-J_RANGE_MASKED_MIR	INJ_SATU-RATE_MASKED_MIR	IN-J_EOC_MASKED_MIR	DSI_COLLI-SION_MASKED_MIR	FW_COLLI-SION_MASKED_MIR	OVER-FLOW_MASKED_MIR	EO-S_MASKED_MIR

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	None					
HW Access	W	W	None					
Name	RANGE_MASKED_RED	SATU-RATE_MASKED_RED	None [29:24]					

Bits	Name	Description
31	RANGE_MASKED_RED	Reduction OR of all SAR_RANGE_INTR_MASKED bits Default Value: 0
30	SATU-RATE_MASKED_RED	Reduction OR of all SAR_SATURATION_INTR_MASKED bits Default Value: 0
7	INJ_COLLI-SION_MASKED_MIR	Mirror copy of corresponding bit in SAR_INTR_MASKED Default Value: 0
6	IN-J_RANGE_MASKED_MIR	Mirror copy of corresponding bit in SAR_INTR_MASKED Default Value: 0
5	INJ_SATU-RATE_MASKED_MIR	Mirror copy of corresponding bit in SAR_INTR_MASKED Default Value: 0
4	INJ_EOC_MASKED_MIR	Mirror copy of corresponding bit in SAR_INTR_MASKED Default Value: 0

19.1.29 SAR0_INTR_CAUSE (continued)

3	DSI_COLLI-SION_MASKED_MIR	Mirror copy of corresponding bit in SAR_INTR_MASKED Default Value: 0
2	FW_COLLI-SION_MASKED_MIR	Mirror copy of corresponding bit in SAR_INTR_MASKED Default Value: 0
1	OVER-FLOW_MASKED_MIR	Mirror copy of corresponding bit in SAR_INTR_MASKED Default Value: 0
0	EOS_MASKED_MIR	Mirror copy of corresponding bit in SAR_INTR_MASKED Default Value: 0

19.1.30 SAR0_INJ_CHAN_CONFIG

Injection channel configuration register.

Address: 0x403A0280

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None	RW			None	RW		
HW Access	None	R			None	R		
Name	None	INJ_PORT_ADDR [6:4]			None	INJ_PIN_ADDR [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None		RW		None	RW	RW	RW
HW Access	None		R		None	R	R	R
Name	None [15:14]		INJ_SAMPLE_TIME_SEL [13:12]		None	INJ_AVG_EN	INJ_RESOLUTION	INJ_DIFFERENTIAL_EN

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1S	RW	None					
HW Access	RW1C	R	None					
Name	INJ_START_EN	INJ_TAILGATING	None [29:24]					

Bits	Name	Description
31	INJ_START_EN	Set by firmware to enable the injection channel. If INJ_TAILGATING is not set this bit also functions as trigger for this channel. Cleared by hardware after this channel has been sampled (i.e. this channel is always one shot even if CONTINUOUS is set). Also cleared if the SAR is disabled. Default Value: 0
30	INJ_TAILGATING	Injection channel tailgating. - 0: no tailgating for this channel, SAR is immediately triggered when the INJ_START_EN bit is set if the SAR is not busy. If the SAR is busy, the INJ channel addressed pin is sampled at the end of the current scan. - 1: injection channel tailgating. The addressed pin is sampled after the next trigger and after all enabled channels have been scanned. Default Value: 0
13 : 12	INJ_SAMPLE_TIME_SEL	Injection sample time select: select which of the 4 global sample times to use for this channel Default Value: 0

19.1.30 SAR0_INJ_CHAN_CONFIG (continued)

10	INJ_AVG_EN	Averaging enable for this channel. If set the AVG_CNT and AVG_SHIFT settings are used for sampling the addressed pin(s) Default Value: 0
9	INJ_RESOLUTION	Resolution for this channel. Default Value: 0 **0x0: 12B :** 12-bit resolution is used for this channel. **0x1: SUBRES :** The resolution specified by SUB_RESOLUTION in the SAR_SAMPLE_CTRL register is used for this channel.
8	INJ_DIFFERENTIAL_EN	Differential enable for this channel. - 0: The voltage on the addressed pin is measured (Single-ended) and the resulting value is stored in the corresponding data register. - 1: The differential voltage on the addressed pin pair is measured and the resulting value is stored in the corresponding data register. (INJ_PIN_ADDR[0] is ignored). Default Value: 0
6 : 4	INJ_PORT_ADDR	Address of the port that contains the pin to be sampled by this channel. Default Value: 0 **0x0: SARMUX :** SARMUX pins. **0x1: CTB0 :** CTB0 **0x2: CTB1 :** CTB1 **0x3: CTB2 :** CTB2 **0x4: CTB3 :** CTB3 **0x6: AROUTE_VIRT :** AROUTE virtual port **0x7: SARMUX_VIRT :** SARMUX virtual port

19.1.30 SAR0_INJ_CHAN_CONFIG (continued)

2 : 0	INJ_PIN_ADDR	Address of the pin to be sampled by this injection channel. If differential is enabled then PIN_ADDR[0] is ignored and considered to be 0, i.e. PIN_ADDR points to the even pin of a pin pair. Default Value: 0

19.1.31 SAR0_INJ_RESULT

Injection channel result register

Address: 0x403A0290

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	INJ_RESULT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	INJ_RESULT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	R	R	None			
HW Access	W	W	W	W	None			
Name	INJ_EOC_INTR_MIR	INJ_RANGE_INTR_MIR	INJ_SATURATE_INTR_MIR	INJ_COLLISION_INTR_MIR	None [27:24]			

Bits	Name	Description
31	INJ_EOC_INTR_MIR	mirror bit of corresponding bit in SAR_INTR register Default Value: 0
30	INJ_RANGE_INTR_MIR	mirror bit of corresponding bit in SAR_INTR register Default Value: 0
29	INJ_SATURATE_INTR_MIR	mirror bit of corresponding bit in SAR_INTR register Default Value: 0
28	INJ_COLLISION_INTR_MIR	mirror bit of corresponding bit in SAR_INTR register Default Value: 0
15 : 0	INJ_RESULT	SAR conversion result of the channel. Default Value: Undefined

19.1.32 SAR0_MUX_SWITCH0

SARMUX Firmware switch controls

Address: 0x403A0300

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
Name	MUX_FW_P7_VPLUS	MUX_FW_P6_VPLUS	MUX_FW_P5_VPLUS	MUX_FW_P4_VPLUS	MUX_FW_P3_VPLUS	MUX_FW_P2_VPLUS	MUX_FW_P1_VPLUS	MUX_FW_P0_VPLUS

Bits	15	14	13	12	11	10	9	8
SW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
Name	MUX_FW_P7_VMINUS	MUX_FW_P6_VMINUS	MUX_FW_P5_VMINUS	MUX_FW_P4_VMINUS	MUX_FW_P3_VMINUS	MUX_FW_P2_VMINUS	MUX_FW_P1_VMINUS	MUX_FW_P0_VMINUS

Bits	23	22	21	20	19	18	17	16
SW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
Name	MUX_FW_SARBUS1_VPLUS	MUX_FW_SARBUS0_VPLUS	MUX_FW_AMUXBUSB_VMINUS	MUX_FW_AMUXBUSA_VMINUS	MUX_FW_AMUXBUSB_VPLUS	MUX_FW_AMUXBUSA_VPLUS	MUX_FW_TEMP_VPLUS	MUX_FW_VSSA_VMINUS

Bits	31	30	29	28	27	26	25	24
SW Access	None		RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
HW Access	None		RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
Name	None [31:30]		MUX_FW_P7_COREIO3	MUX_FW_P6_COREIO2	MUX_FW_P5_COREIO1	MUX_FW_P4_COREIO0	MUX_FW_SARBUS1_VMINUS	MUX_FW_SARBUS0_VMINUS

Bits	Name	Description
29	MUX_FW_P7_COREIO3	Firmware control: 0=open, 1=close switch between P7 and coreio3 signal. Write with '1' to set bit. Default Value: 0
28	MUX_FW_P6_COREIO2	Firmware control: 0=open, 1=close switch between P6 and coreio2 signal. Write with '1' to set bit. Default Value: 0
27	MUX_FW_P5_COREIO1	Firmware control: 0=open, 1=close switch between P5 and coreio1 signal. Write with '1' to set bit. Default Value: 0
26	MUX_FW_P4_COREIO0	Firmware control: 0=open, 1=close switch between P4 and coreio0 signal. Write with '1' to set bit. Default Value: 0

19.1.32 SAR0_MUX_SWITCH0 (continued)

25	MUX_FW_SAR-BUS1_VMINUS	Firmware control: 0=open, 1=close switch between sarbus1 and vminus signal. Write with '1' to set bit. Default Value: 0
24	MUX_FW_SAR-BUS0_VMINUS	Firmware control: 0=open, 1=close switch between sarbus0 and vminus signal. Write with '1' to set bit. Default Value: 0
23	MUX_FW_SAR-BUS1_VPLUS	Firmware control: 0=open, 1=close switch between sarbus1 and vplus signal. Write with '1' to set bit. Default Value: 0
22	MUX_FW_SAR-BUS0_VPLUS	Firmware control: 0=open, 1=close switch between sarbus0 and vplus signal. Write with '1' to set bit. Default Value: 0
21	MUX_FW_AMUXBUS-B_VMINUS	Firmware control: 0=open, 1=close switch between amuxbusb and vminus signal. Write with '1' to set bit. Default Value: 0
20	MUX_FW_AMUX-BUSA_VMINUS	Firmware control: 0=open, 1=close switch between amuxbusa and vminus signal. Write with '1' to set bit. Default Value: 0
19	MUX_FW_AMUXBUS-B_VPLUS	Firmware control: 0=open, 1=close switch between amuxbusb and vplus signal. Write with '1' to set bit. Default Value: 0
18	MUX_FW_AMUX-BUSA_VPLUS	Firmware control: 0=open, 1=close switch between amuxbusa and vplus signal. Write with '1' to set bit. Default Value: 0
17	MUX_FW_TEMP_VPLUS	Firmware control: 0=open, 1=close switch between temperature sensor and vplus signal, also powers on the temperature sensor. Write with '1' to set bit. Default Value: 0
16	MUX_FW_VSSA_VMI-NUS	Firmware control: 0=open, 1=close switch between vssa_kelvin and vminus signal. Write with '1' to set bit. Default Value: 0
15	MUX_FW_P7_VMINUS	Firmware control: 0=open, 1=close switch between pin P7 and vminus signal. Write with '1' to set bit. Default Value: 0
14	MUX_FW_P6_VMINUS	Firmware control: 0=open, 1=close switch between pin P6 and vminus signal. Write with '1' to set bit. Default Value: 0
13	MUX_FW_P5_VMINUS	Firmware control: 0=open, 1=close switch between pin P5 and vminus signal. Write with '1' to set bit. Default Value: 0
12	MUX_FW_P4_VMINUS	Firmware control: 0=open, 1=close switch between pin P4 and vminus signal. Write with '1' to set bit. Default Value: 0
11	MUX_FW_P3_VMINUS	Firmware control: 0=open, 1=close switch between pin P3 and vminus signal. Write with '1' to set bit. Default Value: 0
10	MUX_FW_P2_VMINUS	Firmware control: 0=open, 1=close switch between pin P2 and vminus signal. Write with '1' to set bit. Default Value: 0

19.1.32 SAR0_MUX_SWITCH0 (continued)

9	MUX_FW_P1_VMINUS	Firmware control: 0=open, 1=close switch between pin P1 and vminus signal. Write with '1' to set bit. Default Value: 0
8	MUX_FW_P0_VMINUS	Firmware control: 0=open, 1=close switch between pin P0 and vminus signal. Write with '1' to set bit. Default Value: 0
7	MUX_FW_P7_VPLUS	Firmware control: 0=open, 1=close switch between pin P7 and vplus signal. Write with '1' to set bit. Default Value: 0
6	MUX_FW_P6_VPLUS	Firmware control: 0=open, 1=close switch between pin P6 and vplus signal. Write with '1' to set bit. Default Value: 0
5	MUX_FW_P5_VPLUS	Firmware control: 0=open, 1=close switch between pin P5 and vplus signal. Write with '1' to set bit. Default Value: 0
4	MUX_FW_P4_VPLUS	Firmware control: 0=open, 1=close switch between pin P4 and vplus signal. Write with '1' to set bit. Default Value: 0
3	MUX_FW_P3_VPLUS	Firmware control: 0=open, 1=close switch between pin P3 and vplus signal. Write with '1' to set bit. Default Value: 0
2	MUX_FW_P2_VPLUS	Firmware control: 0=open, 1=close switch between pin P2 and vplus signal. Write with '1' to set bit. Default Value: 0
1	MUX_FW_P1_VPLUS	Firmware control: 0=open, 1=close switch between pin P1 and vplus signal. Write with '1' to set bit. Default Value: 0
0	MUX_FW_P0_VPLUS	Firmware control: 0=open, 1=close switch between pin P0 and vplus signal. Write with '1' to set bit. Default Value: 0

19.1.33 SAR0_MUX_SWITCH_CLEAR0

SARMUX Firmware switch control clear

Address: 0x403A0304

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	A	A	A	A	A	A	A	A
Name	MUX_FW_P7_VPLUS	MUX_FW_P6_VPLUS	MUX_FW_P5_VPLUS	MUX_FW_P4_VPLUS	MUX_FW_P3_VPLUS	MUX_FW_P2_VPLUS	MUX_FW_P1_VPLUS	MUX_FW_P0_VPLUS

Bits	15	14	13	12	11	10	9	8
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	A	A	A	A	A	A	A	A
Name	MUX_FW_P7_VMINUS	MUX_FW_P6_VMINUS	MUX_FW_P5_VMINUS	MUX_FW_P4_VMINUS	MUX_FW_P3_VMINUS	MUX_FW_P2_VMINUS	MUX_FW_P1_VMINUS	MUX_FW_P0_VMINUS

Bits	23	22	21	20	19	18	17	16
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	A	A	A	A	A	A	A	A
Name	MUX_FW_SARBUS1_VPLUS	MUX_FW_SARBUS0_VPLUS	MUX_FW_AMUXBUSB_VMINUS	MUX_FW_AMUXBUSA_VMINUS	MUX_FW_AMUXBUSB_VPLUS	MUX_FW_AMUXBUSA_VPLUS	MUX_FW_TEMP_VPLUS	MUX_FW_VSSA_VMINUS

Bits	31	30	29	28	27	26	25	24
SW Access	None		RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
HW Access	None		A	A	A	A	A	A
Name	None [31:30]		MUX_FW_P7_COREIO3	MUX_FW_P6_COREIO2	MUX_FW_P5_COREIO1	MUX_FW_P4_COREIO0	MUX_FW_SARBUS1_VMINUS	MUX_FW_SARBUS0_VMINUS

Bits	Name	Description
29	MUX_FW_P7_COREIO3	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
28	MUX_FW_P6_COREIO2	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
27	MUX_FW_P5_COREIO1	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
26	MUX_FW_P4_COREIO0	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0

19.1.33 SAR0_MUX_SWITCH_CLEAR0 (continued)

25	MUX_FW_SAR-BUS1_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
24	MUX_FW_SAR-BUS0_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
23	MUX_FW_SAR-BUS1_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
22	MUX_FW_SAR-BUS0_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
21	MUX_FW_AMUXBUS-B_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
20	MUX_FW_AMUX-BUSA_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
19	MUX_FW_AMUXBUS-B_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
18	MUX_FW_AMUX-BUSA_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
17	MUX_FW_TEMP_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
16	MUX_FW_VSSA_VMI-NUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
15	MUX_FW_P7_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
14	MUX_FW_P6_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
13	MUX_FW_P5_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
12	MUX_FW_P4_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
11	MUX_FW_P3_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
10	MUX_FW_P2_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
9	MUX_FW_P1_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
8	MUX_FW_P0_VMINUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
7	MUX_FW_P7_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
6	MUX_FW_P6_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
5	MUX_FW_P5_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
4	MUX_FW_P4_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0

19.1.33 SAR0_MUX_SWITCH_CLEAR0 (continued)

3	MUX_FW_P3_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
2	MUX_FW_P2_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
1	MUX_FW_P1_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0
0	MUX_FW_P0_VPLUS	Write '1' to clear corresponding bit in MUX_SWITCH0 Default Value: 0

19.1.34 SAR0_MUX_SWITCH1

SARMUX Firmware switch controls

Address: 0x403A0308

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1S	RW1S	RW1S	RW1S
HW Access	None				RW1C	RW1C	RW1C	RW1C
Name	None [7:4]				MUX_FW_ADFT1_SARBUS1	MUX_FW_ADFT0_SARBUS0	MUX_FW_P5_DFT_INM	MUX_FW_P4_DFT_INP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	MUX_FW_ADFT1_SARBUS1	Firmware control: 0=open, 1=close switch between adft1 signal and sarbus1 signal. Write with '1' to set bit. Default Value: 0
2	MUX_FW_ADFT0_SARBUS0	Firmware control: 0=open, 1=close switch between adft0 signal and sarbus0 signal. Write with '1' to set bit. Default Value: 0
1	MUX_FW_P5_DFT_INM	Firmware control: 0=open, 1=close switch between P5 pin and dft_inm signal. Write with '1' to set bit. Default Value: 0
0	MUX_FW_P4_DFT_INP	Firmware control: 0=open, 1=close switch between P4 pin and dft_inp signal. Write with '1' to set bit. Default Value: 0

19.1.35 SAR0_MUX_SWITCH_CLEAR1

SARMUX Firmware switch control clear

Address: 0x403A030C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW1C	RW1C	RW1C	RW1C
HW Access	None				A	A	A	A
Name	None [7:4]				MUX_FW_ADFT1_SARBUS1	MUX_FW_ADFT0_SARBUS0	MUX_FW_P5_DFT_INM	MUX_FW_P4_DFT_INP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	MUX_FW_ADFT1_SARBUS1	Write '1' to clear corresponding bit in MUX_SWITCH1 Default Value: 0
2	MUX_FW_ADFT0_SARBUS0	Write '1' to clear corresponding bit in MUX_SWITCH1 Default Value: 0
1	MUX_FW_P5_DFT_INM	Write '1' to clear corresponding bit in MUX_SWITCH1 Default Value: 0
0	MUX_FW_P4_DFT_INP	Write '1' to clear corresponding bit in MUX_SWITCH1 Default Value: 0

19.1.36 SAR0_MUX_SWITCH_HW_CTRL

SARMUX switch hardware control

Address: 0x403A0340

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
HW Access	R	R	R	R	R	R	R	R
Name	MUX_HW_CTRL_P7	MUX_HW_CTRL_P6	MUX_HW_CTRL_P5	MUX_HW_CTRL_P4	MUX_HW_CTRL_P3	MUX_HW_CTRL_P2	MUX_HW_CTRL_P1	MUX_HW_CTRL_P0

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW	RW	None		RW	RW	RW	RW
HW Access	R	R	None		R	R	R	R
Name	MUX_HW_CTRL_SARBUS1	MUX_HW_CTRL_SARBUS0	None [21:20]		MUX_HW_CTRL_AMUXBUSB	MUX_HW_CTRL_AMUXBUSA	MUX_HW_CTRL_TEMP	MUX_HW_CTRL_VSSA

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23	MUX_HW_CTRL_SARBUS1	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for sarbus1 switches. Default Value: 0
22	MUX_HW_CTRL_SARBUS0	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for sarbus0 switches. Default Value: 0
19	MUX_HW_CTRL_AMUXBUSB	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for amuxbusb switches. Default Value: 0
18	MUX_HW_CTRL_AMUXBUSA	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for amuxbusa switches. Default Value: 0

19.1.36 SAR0_MUX_SWITCH_HW_CTRL (continued)

17	MUX_HW_CTRL_TEMP	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for temp switch. Default Value: 0
16	MUX_HW_CTRL_VSSA	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for vssa switch. Default Value: 0
7	MUX_HW_CTRL_P7	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for pin P7 switches. Default Value: 0
6	MUX_HW_CTRL_P6	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for pin P6 switches. Default Value: 0
5	MUX_HW_CTRL_P5	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for pin P5 switches. Default Value: 0
4	MUX_HW_CTRL_P4	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for pin P4 switches. Default Value: 0
3	MUX_HW_CTRL_P3	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for pin P3 switches. Default Value: 0
2	MUX_HW_CTRL_P2	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for pin P2 switches. Default Value: 0
1	MUX_HW_CTRL_P1	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for pin P1 switches. Default Value: 0
0	MUX_HW_CTRL_P0	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for pin P0 switches. Default Value: 0

19.1.37 SAR0_MUX_SWITCH_STATUS

SARMUX switch status

Address: 0x403A0348

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	MUX_FW_P7_VPLUS	MUX_FW_P6_VPLUS	MUX_FW_P5_VPLUS	MUX_FW_P4_VPLUS	MUX_FW_P3_VPLUS	MUX_FW_P2_VPLUS	MUX_FW_P1_VPLUS	MUX_FW_P0_VPLUS

Bits	15	14	13	12	11	10	9	8
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	MUX_FW_P7_VMINUS	MUX_FW_P6_VMINUS	MUX_FW_P5_VMINUS	MUX_FW_P4_VMINUS	MUX_FW_P3_VMINUS	MUX_FW_P2_VMINUS	MUX_FW_P1_VMINUS	MUX_FW_P0_VMINUS

Bits	23	22	21	20	19	18	17	16
SW Access	R	R	R	R	R	R	R	R
HW Access	W	W	W	W	W	W	W	W
Name	MUX_FW_SARBUS1_VPLUS	MUX_FW_SARBUS0_VPLUS	MUX_FW_AMUXBUSB_VMINUS	MUX_FW_AMUXBUSA_VMINUS	MUX_FW_AMUXBUSB_VPLUS	MUX_FW_AMUXBUSA_VPLUS	MUX_FW_TEMP_VPLUS	MUX_FW_VSSA_VMINUS

Bits	31	30	29	28	27	26	25	24
SW Access	None						R	R
HW Access	None						W	W
Name	None [31:26]						MUX_FW_SARBUS1_VMINUS	MUX_FW_SARBUS0_VMINUS

Bits	Name	Description
25	MUX_FW_SARBUS1_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
24	MUX_FW_SARBUS0_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
23	MUX_FW_SARBUS1_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
22	MUX_FW_SARBUS0_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0

19.1.37 SAR0_MUX_SWITCH_STATUS (continued)

21	MUX_FW_AMUXBUS-B_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
20	MUX_FW_AMUX-BUSA_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
19	MUX_FW_AMUXBUS-B_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
18	MUX_FW_AMUX-BUSA_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
17	MUX_FW_TEMP_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
16	MUX_FW_VSSA_VMI-NUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
15	MUX_FW_P7_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
14	MUX_FW_P6_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
13	MUX_FW_P5_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
12	MUX_FW_P4_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
11	MUX_FW_P3_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
10	MUX_FW_P2_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
9	MUX_FW_P1_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
8	MUX_FW_P0_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
7	MUX_FW_P7_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
6	MUX_FW_P6_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
5	MUX_FW_P5_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
4	MUX_FW_P4_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
3	MUX_FW_P3_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
2	MUX_FW_P2_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
1	MUX_FW_P1_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0
0	MUX_FW_P0_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default Value: 0

19.1.38 SAR0_PUMP_CTRL

Switch pump control

Address: 0x403A0380

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							CLOCK_-SEL

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	ENABLED	None [30:24]						

Bits	Name	Description
31	ENABLED	0=disabled: pump output is VDDA_PUMP, 1=enabled: pump output is boosted. Default Value: 0
0	CLOCK_SEL	Clock select: 0=external clock, 1=internal clock (deprecated). Default Value: 0

19.1.39 SAR0_ANA_TRIM

Analog trim register.

Address: 0x403A0F00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW	RW		
HW Access	None				R	R		
Name	None [7:4]				TRIMUNIT	CAP_TRIM [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3	TRIMUNIT	Attenuation cap trimming Default Value: 0
2 : 0	CAP_TRIM	Attenuation cap trimming Default Value: 0

19.1.40 SAR0_WOUNDING

SAR wounding register

Address: 0x403A0F04

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW1S	
HW Access	None						R	
Name	None [7:2]						WOUND_RESOLUTION [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1 : 0	WOUND_RESOLUTION	Maximum SAR resolution allowed Default Value: 0 **0x0: 12BIT :** unwounded: up to full 12-bit SAR resolution allowed **0x1: 10BIT :** wounded: max resolution upto 10-bit SAR resolution allowed **0x2: 8BIT :** wounded: only 8-bit SAR resolution allowed

19.1.40 SAR0_WOUNDING (continued)

0x3: 8BIT_TOO :

wounded: only 8-bit SAR resolution allowed

20 CapSense Registers

Note: Cypress recommends to use the CapSense middleware provided by the ModusToolbox IDE to implement CapSense designs. See the PSoC 4 and PSoC 6 MCU CapSense Design Guide for more details.

It is not recommended to directly access or modify CapSense registers. If you want to create custom register settings, contact Cypress technical support.

21 PASS MMIO Registers

This section discusses the Programmable Analog Sub System Memory Mapped IO (PASS MMIO) registers. It lists all the registers in mapping tables, in address order.

21.1 Register Details

Register	Address	Description
PASS0_INTR_CAUSE	0x403F0000	Interrupt cause register
PASS0_DFT_CTRL	0x403F0030	DFT control register
PASS0_PASS_CTRL	0x403F0108	PASS Control
PASS0_DSAB_DSAB_CTRL	0x403F0E00	global DSAB control
PASS0_DSAB_DSAB_DFT	0x403F0E04	DFT bits
PASS0_DSAB_TRIM	0x403F0F00	DSAB Trim bits

21.1.1 PASS0_INTR_CAUSE

Interrupt cause register

Address: 0x403F0000

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							W
Name	None [7:1]							CTB0_INT

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	CTB0_INT	CTB0 interrupt pending Default Value: 0

21.1.2 PASS0_DFT_CTRL

DFT control register

Address: 0x403F0030

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							DSAB_ADFT_RES_EN

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	DSAB_ADFT_RES_EN	Close the switch to connect the DSAB ADFT resistor to the AMUXBUS Default Value: 0

21.1.3 PASS0_PASS_CTRL

PASS Control

Address: 0x403F0108

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [7:2]						PMP-CLK_SRC	PMP-CLK_BYP

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	RMB_BITS [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15 : 8	RMB_BITS	Risk mitigation bits Default Value: 0
1	PMPCLK_SRC	- 0: Pump clk is clk_hf - 1: Pump clk is direct from SRSS Default Value: 0
0	PMPCLK_BYP	- 0: Pump clk is clk_hf/2 - 1: Pump clk is selected from PMPCLK_SRC Default Value: 0

21.1.4 PASS0_DSAB_DSAB_CTRL

global DSAB control

Address: 0x403F0E00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		CURRENT_SEL [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None				RW			
HW Access	None				R			
Name	None [15:12]				SEL_OUT [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	None				RW			
HW Access	None				R			
Name	None [23:20]				REF_SWAP_EN [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None		RW	None			RW
HW Access	R	None		R	None			R
Name	ENABLED	None [30:29]		START-UP_RM	None [27:25]			BYPASS_-MODE_EN

Bits	Name	Description
31	ENABLED	This field (along with SEL_OUT and REF_SWAP_EN) provides bitwise selection of the current sources that drive the DSAB ZTC and PTAT outputs. See SEL_OUT field for truth tables. In SRSSLT devices, in active mode, this bit is overridden to '1', that is - it is always enabled in active mode. Default Value: 0
28	STARTUP_RM	Risk mitigation control 1 - Force start the startup circuit Default Value: 0
24	BYPASS_MODE_EN	0 - DSAB PTAT generator is powered from DSAB regulator: VDDA must be at least 2.4V 1 - DSAB PTAT generator is pwoered directly from VDDA: VDDA cannot exceed 4.0V Default Value: 0
19 : 16	REF_SWAP_EN	This field (along with SEL_OUT and ENABLED) provides bitwise selection of the current sources that drive the DSAB ZTC and PTAT outputs. See SEL_OUT field for truth tables. Default Value: 0

21.1.4 PASS0_DSAB_DSAB_CTRL (continued)

11 : 8	SEL_OUT	This field (along with REF_SWAP_EN and ENABLED) provides bitwise selection of the current sources that drive the DSAB ZTC and PTAT outputs. The available current sources are a function of the type of SRSS. The SRSS current sources are disabled in chip DeepSleep mode which is indicated by () entries in the truth table. CTB(m) factory trim has SRSS-ZTC and either SRSS-PTAT (SRSSv2) or DSAB_PTAT (SRSS-LITE) enabled. If different settings are used, then a periodic re-trim of CTB(m) offset should be performed. Truth Table with SRSSv2 (backwards compatible with PSoC4A family) ENABLED SEL_OUT REF_SWAP_EN "Chip Power Mode" ZTC Output PTAT Output 0 X X Active SRSS-ZTC SRSS-PTAT 0 X X Deepsleep (SRSS-ZTC) (SRSS-PTAT) 1 0 0 Active SRSS-ZTC SRSS-PTAT 1 0 0 DeepSleep (SRSS-ZTC) (SRSS-PTAT) 1 0 1 Active SRSS-PTAT SRSS-ZTC 1 0 1 DeepSleep (SRSS-PTAT) (SRSS-ZTC) 1 1 0 Active DSAB-PTAT SRSS-PTAT 1 1 0 DeepSleep DSAB-PTAT (SRSS-PTAT) 1 1 1 Active SRSS-PTAT DSAB-PTAT 1 1 1 DeepSleep (SRSS-PTAT) DSAB-PTAT Truth Table with SRSS-LITE ENABLED SEL_OUT REF_SWAP_EN "Chip Power Mode" ZTC Output PTAT Output 0 X X Active SRSS-ZTC DSAB-PTAT 0 X X Deepsleep (SRSS-ZTC) -- 1 0 0 Active SRSS-ZTC DSAB-PTAT 1 0 0 DeepSleep (SRSS-ZTC) -- 1 0 1 Active DSAB-PTAT SRSS-ZTC 1 0 1 DeepSleep DSAB-PTAT (SRSS-ZTC) 1 1 0 Active DSAB-PTAT -- 1 1 0 DeepSleep DSAB-PTAT -- 1 1 1 Active -- DSAB-PTAT 1 1 1 DeepSleep -- DSAB-PTAT Default Value: 0
5 : 0	CURRENT_SEL	DSAB DAC control field Nominal DSAB Output Current = CURRENT_SEL * 0.075 uA In products with SRSS-LITE, this setting impacts the CTB(m) offset. A value of 0x20 is used during factory trim and is required to maintain low offsets across temperature variation. If a different setting is used then a periodic re-trim of CTB(m) offset should be performed. Default Value: 0

21.1.5 PASS0_DSAB_DSAB_DFT

DFT bits

Address: 0x403F0E04

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				RW			
HW Access	None				R			
Name	None [7:4]				EN_DFT [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
3 : 0	EN_DFT	- 0: DSAB DFT disabled - 1: DSAB DFT enabled (connect output to amuxbus) 0001 - PTAT<0> 0010 - PTAT<1> 0011 - PTAT<1:0> 0100 - PTAT<2> 0111 - PTAT<2:0> 1000 - PTAT<3> 1111 - PTAT<3:0> 1001 - DSAB Reg Out Default Value: 0

21.1.6 PASS0_DSAB_TRIM

DSAB Trim bits

Address: 0x403F0F00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW		RW			
HW Access	None		R		R			
Name	None [7:6]		DSAB_RMB_BITS [5:4]		IBIAS_TRIM [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 4	DSAB_RMB_BITS	Risk mitigation bits Default Value: 0
3 : 0	IBIAS_TRIM	1111=lowest, 0000=highest Default Value: 0

22 Cortex M0+ (CM0P) Registers

This section discusses the CM0+ registers. It lists all the registers in mapping tables, in address order.

22.1 Register Details

Register	Address	Description
CM0P_DWT_PID4	0xE0001FD0	Watchpoint Unit CoreSight ROM Table Peripheral ID #4
CM0P_DWT_PID0	0xE0001FE0	Watchpoint Unit CoreSight ROM Table Peripheral ID #0
CM0P_DWT_PID1	0xE0001FE4	Watchpoint Unit CoreSight ROM Table Peripheral ID #1
CM0P_DWT_PID2	0xE0001FE8	Watchpoint Unit CoreSight ROM Table Peripheral ID #2
CM0P_DWT_PID3	0xE0001FEC	Watchpoint Unit CoreSight ROM Table Peripheral ID #3
CM0P_DWT_CID0	0xE0001FF0	Watchpoint Unit CoreSight ROM Table Component ID #0
CM0P_DWT_CID1	0xE0001FF4	Watchpoint Unit CoreSight ROM Table Component ID #1
CM0P_DWT_CID2	0xE0001FF8	Watchpoint Unit CoreSight ROM Table Component ID #2
CM0P_DWT_CID3	0xE0001FFC	Watchpoint Unit CoreSight ROM Table Component ID #3
CM0P_BP_PID4	0xE0002FD0	Breakpoint Unit CoreSight ROM Table Peripheral ID #4
CM0P_BP_PID0	0xE0002FE0	Breakpoint Unit CoreSight ROM Table Peripheral ID #0
CM0P_BP_PID1	0xE0002FE4	Breakpoint Unit CoreSight ROM Table Peripheral ID #1
CM0P_BP_PID2	0xE0002FE8	Breakpoint Unit CoreSight ROM Table Peripheral ID #2
CM0P_BP_PID3	0xE0002FEC	Breakpoint Unit CoreSight ROM Table Peripheral ID #3
CM0P_BP_CID0	0xE0002FF0	Breakpoint Unit CoreSight ROM Table Component ID #0
CM0P_BP_CID1	0xE0002FF4	Breakpoint Unit CoreSight ROM Table Component ID #1
CM0P_BP_CID2	0xE0002FF8	Breakpoint Unit CoreSight ROM Table Component ID #2
CM0P_BP_CID3	0xE0002FFC	Breakpoint Unit CoreSight ROM Table Component ID #3
CM0P_SYST_CSR	0xE000E010	SysTick Control & Status
CM0P_SYST_RVR	0xE000E014	SysTick Reload Value
CM0P_SYST_CVR	0xE000E018	SysTick Current Value
CM0P_SYST_CALIB	0xE000E01C	SysTick Calibration Value
CM0P_ISER	0xE000E100	Interrupt Set-Enable Register
CM0P_ICER	0xE000E180	Interrupt Clear Enable Register
CM0P_ISPR	0xE000E200	Interrupt Set-Pending Register
CM0P_ICPR	0xE000E280	Interrupt Clear-Pending Register
CM0P_IPR0	0xE000E400	Interrupt Priority Registers

Register	Address	Description
CM0P_IPR1	0xE000E404	Interrupt Priority Registers. See CM0P_IPR0 for the details of bit fields.
CM0P_IPR2	0xE000E408	Interrupt Priority Registers. See CM0P_IPR0 for the details of bit fields.
CM0P_IPR3	0xE000E40C	Interrupt Priority Registers. See CM0P_IPR0 for the details of bit fields.
CM0P_IPR4	0xE000E410	Interrupt Priority Registers. See CM0P_IPR0 for the details of bit fields.
CM0P_IPR5	0xE000E414	Interrupt Priority Registers. See CM0P_IPR0 for the details of bit fields.
CM0P_IPR6	0xE000E418	Interrupt Priority Registers. See CM0P_IPR0 for the details of bit fields.
CM0P_IPR7	0xE000E41C	Interrupt Priority Registers. See CM0P_IPR0 for the details of bit fields.
CM0P_CPUID	0xE000ED00	CPUID Register
CM0P_ICSR	0xE000ED04	Interrupt Control State Register
CM0P_VTOR	0xE000ED08	Vector Table Offset Register
CM0P_AIRCR	0xE000ED0C	Application Interrupt and Reset Control Register
CM0P_SCR	0xE000ED10	System Control Register
CM0P_CCR	0xE000ED14	Configuration and Control Register
CM0P_SHPR2	0xE000ED1C	System Handler Priority Register 2
CM0P_SHPR3	0xE000ED20	System Handler Priority Register 3
CM0P_SHCSR	0xE000ED24	System Handler Control and State Register
CM0P_SCS_PID4	0xE000EFD0	System Control Space ROM Table Peripheral ID #4
CM0P_SCS_PID0	0xE000EFE0	System Control Space ROM Table Peripheral ID #0
CM0P_SCS_PID1	0xE000EFE4	System Control Space ROM Table Peripheral ID #1
CM0P_SCS_PID2	0xE000EFE8	System Control Space ROM Table Peripheral ID #2
CM0P_SCS_PID3	0xE000EFEC	System Control Space ROM Table Peripheral ID #3
CM0P_SCS_CID0	0xE000EFF0	System Control Space ROM Table Component ID #0
CM0P_SCS_CID1	0xE000EFF4	System Control Space ROM Table Component ID #1
CM0P_SCS_CID2	0xE000EFF8	System Control Space ROM Table Component ID #2
CM0P_SCS_CID3	0xE000EFFC	System Control Space ROM Table Component ID #3
CM0P_ROM_SCS	0xE00FF000	CM0+ CoreSight ROM Table Peripheral #0
CM0P_ROM_DWT	0xE00FF004	CM0+ CoreSight ROM Table Peripheral #1
CM0P_ROM_BPU	0xE00FF008	CM0+ CoreSight ROM Table Peripheral #2
CM0P_ROM_END	0xE00FF00C	CM0+ CoreSight ROM Table End Marker
CM0P_ROM_CSMT	0xE00FFFCC	CM0+ CoreSight ROM Table Memory Type
CM0P_ROM_PID4	0xE00FFFD0	CM0+ CoreSight ROM Table Peripheral ID #4
CM0P_ROM_PID0	0xE00FFFE0	CM0+ CoreSight ROM Table Peripheral ID #0
CM0P_ROM_PID1	0xE00FFFE4	CM0+ CoreSight ROM Table Peripheral ID #1
CM0P_ROM_PID2	0xE00FFFE8	CM0+ CoreSight ROM Table Peripheral ID #2
CM0P_ROM_PID3	0xE00FFFEC	CM0+ CoreSight ROM Table Peripheral ID #3
CM0P_ROM_CID0	0xE00FFFF0	CM0+ CoreSight ROM Table Component ID #0
CM0P_ROM_CID1	0xE00FFFF4	CM0+ CoreSight ROM Table Component ID #1
CM0P_ROM_CID2	0xE00FFFF8	CM0+ CoreSight ROM Table Component ID #2
CM0P_ROM_CID3	0xE00FFFFC	CM0+ CoreSight ROM Table Component ID #3

22.1.1 CM0P_DWT_PID4

Watchpoint Unit CoreSight ROM Table Peripheral ID #4

Address: 0xE0001FD0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #4 Default Value: 4

22.1.2 CM0P_DWT_PID0

Watchpoint Unit CoreSight ROM Table Peripheral ID #0

Address: 0xE0001FE0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #0 Default Value: 10

22.1.3 CM0P_DWT_PID1

Watchpoint Unit CoreSight ROM Table Peripheral ID #1

Address: 0xE0001FE4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #1 Default Value: 176

22.1.4 CM0P_DWT_PID2

Watchpoint Unit CoreSight ROM Table Peripheral ID #2

Address: 0xE0001FE8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #2 Default Value: 11

22.1.5 CM0P_DWT_PID3

Watchpoint Unit CoreSight ROM Table Peripheral ID #3

Address: 0xE0001FEC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #3 Default Value: 0

22.1.6 CM0P_DWT_CID0

Watchpoint Unit CoreSight ROM Table Component ID #0

Address: 0xE0001FF0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #0 Default Value: 13

22.1.7 CM0P_DWT_CID1

Watchpoint Unit CoreSight ROM Table Component ID #1

Address: 0xE0001FF4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #1 Default Value: 224

22.1.8 CM0P_DWT_CID2

Watchpoint Unit CoreSight ROM Table Component ID #2

Address: 0xE0001FF8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #2 Default Value: 5

22.1.9 CM0P_DWT_CID3

Watchpoint Unit CoreSight ROM Table Component ID #3

Address: 0xE0001FFC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #3 Default Value: 177

22.1.10 CM0P_BP_PID4

Breakpoint Unit CoreSight ROM Table Peripheral ID #4

Address: 0xE0002FD0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #4 Default Value: 4

22.1.11 CM0P_BP_PID0

Breakpoint Unit CoreSight ROM Table Peripheral ID #0

Address: 0xE0002FE0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #0 Default Value: 11

22.1.12 CM0P_BP_PID1

Breakpoint Unit CoreSight ROM Table Peripheral ID #1

Address: 0xE0002FE4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #1 Default Value: 176

22.1.13 CM0P_BP_PID2

Breakpoint Unit CoreSight ROM Table Peripheral ID #2

Address: 0xE0002FE8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #2 Default Value: 11

22.1.14 CM0P_BP_PID3

Breakpoint Unit CoreSight ROM Table Peripheral ID #3

Address: 0xE0002FEC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #3 Default Value: 0

22.1.15 CM0P_BP_CID0

Breakpoint Unit CoreSight ROM Table Component ID #0

Address: 0xE0002FF0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #0 Default Value: 13

22.1.16 CM0P_BP_CID1

Breakpoint Unit CoreSight ROM Table Component ID #1

Address: 0xE0002FF4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #1 Default Value: 224

22.1.17 CM0P_BP_CID2

Breakpoint Unit CoreSight ROM Table Component ID #2

Address: 0xE0002FF8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #2 Default Value: 5

22.1.18 CM0P_BP_CID3

Breakpoint Unit CoreSight ROM Table Component ID #3

Address: 0xE0002FFC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #3 Default Value: 177

22.1.19 CM0P_SYST_CSR

SysTick Control & Status

Address: 0xE000E010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW	RW	RW
HW Access	None					R	R	R
Name	None [7:3]					CLK-SOURCE	TICKINT	ENABLE

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							R
HW Access	None							RW
Name	None [23:17]							COUNT-FLAG

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
16	COUNTFLAG	Indicates whether the counter has counted to "0" since the last read of this register: '0': counter has not counted to "0". '1': counter has counted to "0". COUNTFLAG is set to '1' by a count transition from "1" to "0". COUNTFLAG is cleared to '0' by a read of this register, and by any write to the SYST_CVR register. Default Value: 0
2	CLKSOURCE	Indicates the SysTick counter clock source: '0': SysTick uses the low frequency clock "clk_lf". For this mode to function, "clk_lf" should be less than half the frequency of "clk_sys". Note that "clk_lf" is generated by a low accuracy ILO (Internal Low power Oscillator), with a target frequency of 32.768 kHz (frequency can be as low as 15 KHz and as high as 60 kHz). '1': SysTick uses the system/processor clock "clk_sys". If SysTick counter functionality is not present in the device. This field should be set to '1', such that SysTick uses the system clock "clk_sys". Default Value: 0

22.1.19 CM0P_SYST_CSR (continued)

1	TICKINT	Indicates whether counting to "0" causes the status of the SysTick exception to change to pending: '0': count to "0" does not affect the SysTick exception status. '1': count to "0" changes the SysTick exception status to pending. Changing the value of the counter to "0" by writing zero to the SYST_CVR register to "0" never changes the status of the SysTick exception. Default Value: 0
0	ENABLE	Indicates the enabled status of the SysTick counter: '0': counter is disabled. '1': counter is operating. Default Value: 0

22.1.20 CM0P_SYST_RVR

SysTick Reload Value

Address: 0xE000E014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	RELOAD [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	RELOAD [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	RELOAD [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 0	RELOAD	The value to load into the SYST_CVR register when the counter reaches 0. Default Value: X

22.1.21 CM0P_SYST_CVR

SysTick Current Value

Address: 0xE000E018

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CURRENT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CURRENT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	CURRENT [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
23 : 0	CURRENT	Current counter value. This is the value of the counter at the time it is sampled. Default Value: X

22.1.22 CM0P_SYST_CALIB

SysTick Calibration Value

Address: 0xE000E01C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	TENMS [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	TENMS [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	TENMS [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R	R	None					
HW Access		RW	None					
Name	NOREF	SKEW	None [29:24]					

Bits	Name	Description
31	NOREF	Indicates whether a implementation defined reference clock is provided: '0': the reference clock is provided. '1': the reference clock is not provided. When this bit is '1', the SYST_CSR.CLKSOURCEis forced to '1' and cannot be cleared to '0'. SysTick counter functionality on the low frequency clock is provided and this field is '0'. Default Value: 0
30	SKEW	Indicates whether the 10ms calibration value is exact: '0': 10ms calibration value is exact. '1': 10ms calibration value is inexact, because of the clock frequency. SysTick counter functionality on the low frequency clock is provided and this field is '1' (due to the low accuracy ILO). Default Value: X
23 : 0	TENMS	Optionally, holds a reload value to be used for 10ms (100Hz) timing, subject to system clock skew errors. If this field is "0", the calibration value is not known. SysTick counter functionality on the low frequency clock is provided and this field is 0x00:00147. Default Value: X

22.1.23 CM0P_ISER

Interrupt Set-Enable Register

Address: 0xE000E100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S							
HW Access	R							
Name	SETENA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1S							
HW Access	R							
Name	SETENA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW1S							
HW Access	R							
Name	SETENA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1S							
HW Access	R							
Name	SETENA [31:24]							

Bits	Name	Description
31 : 0	SETENA	Enables, or reads the enabled state of one or more interrupts. Each bit corresponds to the same numbered interrupt. Default Value: 0

22.1.24 CM0P_ICER

Interrupt Clear Enable Register

Address: 0xE000E180

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C							
HW Access	R							
Name	CLRENA [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1C							
HW Access	R							
Name	CLRENA [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW1C							
HW Access	R							
Name	CLRENA [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1C							
HW Access	R							
Name	CLRENA [31:24]							

Bits	Name	Description
31 : 0	CLRENA	Disables, or reads the enabled state of one or more interrupts. Each bit corresponds to the same numbered interrupt. Default Value: 0

22.1.25 CM0P_ISPR

Interrupt Set-Pending Register

Address: 0xE000E200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S							
HW Access	R							
Name	SETPEND [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1S							
HW Access	R							
Name	SETPEND [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW1S							
HW Access	R							
Name	SETPEND [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1S							
HW Access	R							
Name	SETPEND [31:24]							

Bits	Name	Description
31 : 0	SETPEND	Changes the state of one or more interrupts to pending. Each bit corresponds to the same numbered interrupt. Default Value: 0

22.1.26 CM0P_ICPR

Interrupt Clear-Pending Register

Address: 0xE000E280

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C							
HW Access	R							
Name	CLRPEND [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW1C							
HW Access	R							
Name	CLRPEND [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW1C							
HW Access	R							
Name	CLRPEND [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW1C							
HW Access	R							
Name	CLRPEND [31:24]							

Bits	Name	Description
31 : 0	CLRPEND	Changes the state of one or more interrupts to not pending. Each bit corresponds to the same numbered interrupt. Default Value: 0

22.1.27 CM0P_IPR0

Interrupt Priority Registers

Address: 0xE000E400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N0 [7:6]		None [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N1 [15:14]		None [13:8]					

Bits	23	22	21	20	19	18	17	16
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N2 [23:22]		None [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None					
HW Access	R		None					
Name	PRI_N3 [31:30]		None [29:24]					

Bits	Name	Description
31 : 30	PRI_N3	Priority of interrupt number N+3. Default Value: 0
23 : 22	PRI_N2	Priority of interrupt number N+2. Default Value: 0
15 : 14	PRI_N1	Priority of interrupt number N+1. Default Value: 0
7 : 6	PRI_N0	Priority of interrupt number N. Default Value: 0

22.1.28 CM0P_CPUID

CPUID Register

Address: 0xE000ED00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access								
Name	PARTNO [7:4]				REVISION [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	PARTNO [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R				R			
HW Access								
Name	VARIANT [23:20]				CONSTANT [19:16]			

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	IMPLEMENTER [31:24]							

Bits	Name	Description
31 : 24	IMPLEMENTER	Implementer code for ARM. Default Value: 65
23 : 20	VARIANT	Implementation defined. In ARM implementations this is the major revision number n in the rn part of the rnpn revision status, Product revision status on page xii. Default Value: 0
19 : 16	CONSTANT	Indicates the architecture, ARMv6-M Default Value: 12
15 : 4	PARTNO	Indicates part number, Cortex-M0+ Default Value: 3168
3 : 0	REVISION	Indicates revision. In ARM implementations this is the minor revision number n in the pn part of the rnpn revision status, see Product revision status on page xii. For release r0p1. Default Value: 1

22.1.29 CM0P_ICSR

Interrupt Control State Register

Address: 0xE000ED04

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	VECTACTIVE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R				None			R
HW Access	RW				None			RW
Name	VECTPENDING [15:12]				None [11:9]			VECTAC-TIVE

Bits	23	22	21	20	19	18	17	16
SW Access	R	R	None	R				
HW Access	RW	RW	None	RW				
Name	ISRPRE-EMPT	ISRPEND-ING	None	VECTPENDING [20:16]				

Bits	31	30	29	28	27	26	25	24
SW Access	RW1S	None		RW1S	RW1C	RW1S	RW1C	None
HW Access	RW	None		RW	R	RW	R	None
Name	NMIPEND-SET	None [30:29]		PENDS-VSET	PENDSV-CLR	PENDST-SETb	PENDST-CLR	None

Bits	Name	Description
31	NMIPENDSET	Activates an NMI exception or reads back the current state. Because NMI is the highest priority exception, it activates as soon as it is registered. Default Value: 0
28	PENDSVSET	Sets a pending PendSV interrupt or reads back the current state. Use this normally to request a context switch. Writing PENDSVSET and PENDSVCLR to '1' concurrently is UNPREDICTABLE. Default Value: 0
27	PENDSVCLR	Clears a pending PendSV interrupt. Default Value: 0
26	PENDSTSETb	Sets a pending SysTick or reads back the current state. Writing PENDSTSET and PENDSTCLR to '1' concurrently is UNPREDICTABLE. Default Value: 0
25	PENDSTCLR	Clears a pending SysTick, whether set here or by the timer hardware. Default Value: 0
23	ISRPREEMPT	Indicates whether a pending exception will be serviced on exit from debug halt state. Default Value: 0

22.1.29 CM0P_ICSR (continued)

22	ISRPENDING	Indicates if an external configurable, NVIC generated, interrupt is pending. Default Value: 0
20 : 12	VECTPENDING	The exception number for the highest priority pending exception. 0= No pending exceptions. The pending state includes the effect of memory-mapped enable and mask registers. It does not include the PRIMASK special-purpose register qualifier. Default Value: 0
8 : 0	VECTACTIVE	The exception number for the current executing exception. 0= Thread mode. This is the same value as IPSR[8:0] Default Value: 0

22.1.30 CM0P_VTOR

Vector Table Offset Register

Address: 0xE000ED08

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	TBLOFF [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	TBLOFF [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	TBLOFF [31:24]							

Bits	Name	Description
31 : 8	TBLOFF	Table offset address. All bits of the Vector table address that are not defined by the VTOR are zero. Default Value: 0

22.1.31 CM0P_AIRCR

Application Interrupt and Reset Control Register

Address: 0xE000ED0C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW1S	RW1C	None
HW Access	None					R	R	None
Name	None [7:3]					SYSRESE-TREQ	VECTCL-RACTIVE	None

Bits	15	14	13	12	11	10	9	8
SW Access	R	None						
HW Access		None						
Name	ENDIAN-NESS	None [14:8]						

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	VECTKEY [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	VECTKEY [31:24]							

Bits	Name	Description
31 : 16	VECTKEY	Vector Key. The value 0x05FA must be written to this register, otherwise the register write is UN-PREDICTABLE. Readback value is UNKNOWN. Default Value: X
15	ENDIANNESS	Indicates the memory system data endianness: 0 little endian 1 big endian. See Endian support on page A3-44 for more information. Default Value: 0
2	SYSRESETREQ	System Reset Request. Writing 1 to this bit asserts a signal to request a reset by the external system. This will cause a full system reset of the CPU and all other components in the device. See Reset management on page B1-240 for more information. Default Value: 0
1	VECTCLRACTIVE	Clears all active state information for fixed and configurable exceptions. The effect of writing a 1 to this bit if the processor is not halted in Debug state is UN-PREDICTABLE. Default Value: 0

22.1.32 CM0P_SCR

System Control Register

Address: 0xE000ED10

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW	None	RW	RW	None
HW Access	None			R	None	R	R	None
Name	None [7:5]			SEVON-PEND	None	SLEEP-DEEP	SLEEPON-EXIT	None

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
4	SEVONPEND	Determines whether an interrupt transition from inactive state to pending state is a wakeup event: 0: transitions from inactive to pending are not wakeup events. 1: transitions from inactive to pending are wakeup events. See WFE on page A6-197 for more information. Default Value: 0
2	SLEEPDEEP	An implementation can use this bit to select DeepSleep/Hibernate power modes upon execution of WFI/WFE: 0: Select Sleep mode 1: Select DeepSleep/Hibernate (depends on PWR_CONTROL.HIBERNATE) Default Value: 0
1	SLEEPONEXIT	Determines whether, on an exit from an ISR that returns to the base level of execution priority, the processor enters a sleep state: 0 do not enter sleep state. 1 enter sleep state. See Power management on page B1-240 for more information. Default Value: 0

22.1.33 CM0P_CCR

Configuration and Control Register

Address: 0xE000ED14

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None				R	None		
HW Access	None					None		
Name	None [7:4]				UN-ALIGN_TRP	None		

Bits	15	14	13	12	11	10	9	8
SW Access	None						R	None
HW Access	None							None
Name	None [15:10]						STKALIGN	None

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	STKALIGN	1: On exception entry, the SP used prior to the exception is adjusted to be 8-byte aligned and the context to restore it is saved. The SP is restored on the associated exception return. Default Value: 1
3	UNALIGN_TRP	1: unaligned word and halfword accesses generate a HardFault exception. Default Value: 1

22.1.34 CM0P_SHPR2

System Handler Priority Register 2

Address: 0xE000ED1C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None					
HW Access	R		None					
Name	PRI_11 [31:30]		None [29:24]					

Bits	Name	Description
31 : 30	PRI_11	Priority of system handler 11, SVCall Default Value: 0

22.1.35 CM0P_SHPR3

System Handler Priority Register 3

Address: 0xE000ED20

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW		None					
HW Access	R		None					
Name	PRI_14 [23:22]		None [21:16]					

Bits	31	30	29	28	27	26	25	24
SW Access	RW		None					
HW Access	R		None					
Name	PRI_15 [31:30]		None [29:24]					

Bits	Name	Description
31 : 30	PRI_15	Priority of system handler 15, SysTick Default Value: 0
23 : 22	PRI_14	Priority of system handler 14, PendSV Default Value: 0

22.1.36 CM0P_SHCSR

System Handler Control and State Register

Address: 0xE000ED24

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							
HW Access	None							
Name	None [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW	None						
HW Access	RW	None						
Name	SVCALL-PENDED	None						

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
15	SVCALLPENDED	0 SVCall is not pending. 1 SVCall is pending. This bit reflects the pending state on a read, and updates the pending state, to the value written, on a write. (Pending state bits are set to 1 when an exception occurs, and are cleared to 0 when an exception becomes active.) Default Value: 0

22.1.37 CM0P_SCS_PID4

System Control Space ROM Table Peripheral ID #4

Address: 0xE000EFD0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #4 Default Value: 4

22.1.38 CM0P_SCS_PID0

System Control Space ROM Table Peripheral ID #0

Address: 0xE000EFE0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #0 Default Value: 8

22.1.39 CM0P_SCS_PID1

System Control Space ROM Table Peripheral ID #1

Address: 0xE000EFE4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #1 Default Value: 176

22.1.40 CM0P_SCS_PID2

System Control Space ROM Table Peripheral ID #2

Address: 0xE000EFE8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #2 Default Value: 11

22.1.41 CM0P_SCS_PID3

System Control Space ROM Table Peripheral ID #3

Address: 0xE000EFEC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #3 Default Value: 0

22.1.42 CM0P_SCS_CID0

System Control Space ROM Table Component ID #0

Address: 0xE000EFF0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #0 Default Value: 13

22.1.43 CM0P_SCS_CID1

System Control Space ROM Table Component ID #1

Address: 0xE000EFF4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #1 Default Value: 224

22.1.44 CM0P_SCS_CID2

System Control Space ROM Table Component ID #2

Address: 0xE000EFF8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #2 Default Value: 5

22.1.45 CM0P_SCS_CID3

System Control Space ROM Table Component ID #3

Address: 0xE000EFFC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #3 Default Value: 177

22.1.46 CM0P_ROM_SCS

CM0+ CoreSight ROM Table Peripheral #0

Address: 0xE00FF000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Offset to SCS ROM Table Default Value: 4293980163

22.1.47 CM0P_ROM_DWT

CM0+ CoreSight ROM Table Peripheral #1

Address: 0xE00FF004

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Offset to DWT ROM Table Default Value: 4293926915

22.1.48 CM0P_ROM_BPU

CM0+ CoreSight ROM Table Peripheral #2

Address: 0xE00FF008

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Offset to BPU ROM Table Default Value: 4293931011

22.1.49 CM0P_ROM_END

CM0+ CoreSight ROM Table End Marker

Address: 0xE00FF00C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	End marker in peripheral list Default Value: 0

22.1.50 CM0P_ROM_CSMT

CM0+ CoreSight ROM Table Memory Type

Address: 0xE00FFFCC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Memory Type Default Value: 1

22.1.51 CM0P_ROM_PID4

CM0+ CoreSight ROM Table Peripheral ID #4

Address: 0xE00FFFD0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #4 Default Value: 4

22.1.52 CM0P_ROM_PID0

CM0+ CoreSight ROM Table Peripheral ID #0

Address: 0xE00FFFE0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #0 Default Value: 192

22.1.53 CM0P_ROM_PID1

CM0+ CoreSight ROM Table Peripheral ID #1

Address: 0xE00FFFE4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #1 Default Value: 180

22.1.54 CM0P_ROM_PID2

CM0+ CoreSight ROM Table Peripheral ID #2

Address: 0xE00FFFE8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #2 Default Value: 11

22.1.55 CM0P_ROM_PID3

CM0+ CoreSight ROM Table Peripheral ID #3

Address: 0xE00FFFEC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Peripheral ID #3 Default Value: 0

22.1.56 CM0P_ROM_CID0

CM0+ CoreSight ROM Table Component ID #0

Address: 0xE00FFFF0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #0 Default Value: 13

22.1.57 CM0P_ROM_CID1

CM0+ CoreSight ROM Table Component ID #1

Address: 0xE00FFFF4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #1 Default Value: 16

22.1.58 CM0P_ROM_CID2

CM0+ CoreSight ROM Table Component ID #2

Address: 0xE00FFFF8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #2 Default Value: 5

22.1.59 CM0P_ROM_CID3

CM0+ CoreSight ROM Table Component ID #3

Address: 0xE00FFFFC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access								
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access								
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access								
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access								
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component ID #3 Default Value: 177

23 Cryptographic Function Block Registers

This section discusses the Cryptographic Function Block registers. It lists all the registers in mapping tables, in address order.

23.1 Register Details

Register	Address	Description
CRYPTO_CTL	0x402C0000	Control
CRYPTO_STATUS	0x402C0004	Status
CRYPTO_CMD	0x402C0008	Command
CRYPTO_SRC_CTL0	0x402C0010	Source control 0
CRYPTO_SRC_CTL1	0x402C0014	Source control 1
CRYPTO_DST_CTL0	0x402C0020	Destination control 0
CRYPTO_DST_CTL1	0x402C0024	Destination control 1
CRYPTO_AES_CTL	0x402C0100	AES control
CRYPTO_PR_CTL	0x402C0200	Pseudo random control
CRYPTO_PR_CMD	0x402C0208	Pseudo random command
CRYPTO_PR_LFSR_CTL0	0x402C0210	Pseudo random LFSR control 0
CRYPTO_PR_LFSR_CTL1	0x402C0214	Pseudo random LFSR control 1
CRYPTO_PR_LFSR_CTL2	0x402C0218	Pseudo random LFSR control 2
CRYPTO_PR_RESULT	0x402C0220	Pseudo random status
CRYPTO_TR_CTL0	0x402C0280	True random control 0
CRYPTO_TR_CTL1	0x402C0284	True random control 1
CRYPTO_TR_RESULT0	0x402C0288	True random result 0
CRYPTO_TR_RESULT1	0x402C028C	True random result 1
CRYPTO_TR_CMD	0x402C0290	True random command
CRYPTO_TR_GARO_CTL	0x402C02A0	True random GARO control
CRYPTO_TR_FIRO_CTL	0x402C02A4	True random FIRO control
CRYPTO_TR_MON_CTL	0x402C02C0	True random monitor control
CRYPTO_TR_MON_CMD	0x402C02C8	True random monitor command
CRYPTO_TR_MON_RC_CTL	0x402C02D0	True random monitor RC control
CRYPTO_TR_MON_RC_STATUS0	0x402C02D8	True random monitor RC status 0
CRYPTO_TR_MON_RC_STATUS1	0x402C02DC	True random monitor RC status 1
CRYPTO_TR_MON_AP_CTL	0x402C02E0	True random monitor AP control

Register	Address	Description
CRYPTO_TR_MON_AP_STATUS0	0x402C02E8	True random monitor AP status 0
CRYPTO_TR_MON_AP_STATUS1	0x402C02EC	True random monitor AP status 1
CRYPTO_SHA_CTL	0x402C0300	SHA control
CRYPTO_CRC_DATA_CTL0	0x402C0400	CRC data control 0
CRYPTO_CRC_DATA_CTL1	0x402C0404	CRC data control 1
CRYPTO_CRC_POL_CTL	0x402C0410	CRC polynomial control
CRYPTO_CRC_LFSR_CTL	0x402C0414	CRC LFSR control
CRYPTO_CRC_REM_CTL0	0x402C0420	CRC remainder control 0
CRYPTO_CRC_REM_CTL1	0x402C0424	CRC remainder control 1
CRYPTO_CRC_REM	0x402C0428	CRC remainder status
CRYPTO_INTR	0x402C07C0	Interrupt request
CRYPTO_INTR_SET	0x402C07C4	Interrupt set request
CRYPTO_INTR_MASK	0x402C07C8	Interrupt mask
CRYPTO_INTR_MASKED	0x402C07CC	Interrupt masked
CRYPTO_MEM_BUFF0	0x402C0800	Memory buffer
CRYPTO_MEM_BUFF1	0x402C0804	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF2	0x402C0808	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF3	0x402C080C	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF4	0x402C0810	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF5	0x402C0814	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF6	0x402C0818	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF7	0x402C081C	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF8	0x402C0820	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF9	0x402C0824	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF10	0x402C0828	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF11	0x402C082C	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF12	0x402C0830	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF13	0x402C0834	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF14	0x402C0838	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF15	0x402C083C	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF16	0x402C0840	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF17	0x402C0844	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF18	0x402C0848	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF19	0x402C084C	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF20	0x402C0850	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF21	0x402C0854	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF22	0x402C0858	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF23	0x402C085C	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF24	0x402C0860	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF25	0x402C0864	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF26	0x402C0868	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF27	0x402C086C	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.

Register	Address	Description
CRYPTO_MEM_BUFF28	0x402C0870	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF29	0x402C0874	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF30	0x402C0878	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF31	0x402C087C	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF32	0x402C0880	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF33	0x402C0884	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF34	0x402C0888	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF35	0x402C088C	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF36	0x402C0890	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF37	0x402C0894	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF38	0x402C0898	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF39	0x402C089C	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF40	0x402C08A0	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF41	0x402C08A4	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF42	0x402C08A8	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF43	0x402C08AC	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF44	0x402C08B0	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF45	0x402C08B4	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF46	0x402C08B8	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF47	0x402C08BC	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF48	0x402C08C0	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF49	0x402C08C4	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF50	0x402C08C8	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF51	0x402C08CC	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF52	0x402C08D0	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF53	0x402C08D4	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF54	0x402C08D8	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF55	0x402C08DC	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF56	0x402C08E0	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF57	0x402C08E4	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF58	0x402C08E8	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF59	0x402C08EC	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF60	0x402C08F0	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF61	0x402C08F4	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF62	0x402C08F8	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF63	0x402C08FC	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF64	0x402C0900	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF65	0x402C0904	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF66	0x402C0908	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF67	0x402C090C	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF68	0x402C0910	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF69	0x402C0914	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.

Register	Address	Description
CRYPTO_MEM_BUFF70	0x402C0918	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF71	0x402C091C	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF72	0x402C0920	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF73	0x402C0924	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF74	0x402C0928	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF75	0x402C092C	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF76	0x402C0930	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF77	0x402C0934	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF78	0x402C0938	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF79	0x402C093C	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF80	0x402C0940	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF81	0x402C0944	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF82	0x402C0948	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF83	0x402C094C	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF84	0x402C0950	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF85	0x402C0954	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF86	0x402C0958	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF87	0x402C095C	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF88	0x402C0960	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF89	0x402C0964	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF90	0x402C0968	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF91	0x402C096C	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF92	0x402C0970	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF93	0x402C0974	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF94	0x402C0978	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF95	0x402C097C	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF96	0x402C0980	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF97	0x402C0984	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF98	0x402C0988	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF99	0x402C098C	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF100	0x402C0990	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF101	0x402C0994	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF102	0x402C0998	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF103	0x402C099C	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF104	0x402C09A0	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF105	0x402C09A4	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF106	0x402C09A8	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF107	0x402C09AC	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF108	0x402C09B0	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF109	0x402C09B4	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF110	0x402C09B8	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF111	0x402C09BC	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.

Register	Address	Description
CRYPTO_MEM_BUFF112	0x402C09C0	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF113	0x402C09C4	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF114	0x402C09C8	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF115	0x402C09CC	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF116	0x402C09D0	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF117	0x402C09D4	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF118	0x402C09D8	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF119	0x402C09DC	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF120	0x402C09E0	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF121	0x402C09E4	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF122	0x402C09E8	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF123	0x402C09EC	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF124	0x402C09F0	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF125	0x402C09F4	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF126	0x402C09F8	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_MEM_BUFF127	0x402C09FC	Memory buffer. See CRYPTO_MEM_BUFF0 for the details of bit fields.
CRYPTO_PRIV_BUF	0x402CFF00	Buffer Privilege register

23.1.1 CRYPTO_CTL

Control

Address: 0x402C0000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None			RW				
HW Access	None			R				
Name	None [7:5]			OPCODE [4:0]				

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW	None						
HW Access	R	None						
Name	ENABLED	None [30:24]						

Bits	Name	Description
31	ENABLED	IP enable: '0': Disabled. All non-retention registers (command and status registers) are reset to their default value when the IP is disabled. All retention registers retain their value when the IP is disabled. '1': Enabled. Default Value: 0
4 : 0	OPCODE	Specifies the operation: "0": AES forward block cipher. "1": AES inverse block cipher. "16": SHA operation. "24": CRC operation. otherwise: undefined. Default Value: 31

23.1.1 CRYPTO_CTL (continued)

0x0: AES_FORWARD :

SRC_CTL0.OFFSET specifies the offset of the key (as used in the first cipher round) in the memory buffer.
SRC_CTL1.OFFSET specifies the offset of the plaintext in the memory buffer.
DST_CTL0.OFFSET specifies the offset of the key (as used by the last cipher round) in the memory buffer.
DST_CTL1.OFFSET specifies the offset of the cipher in the memory buffer.

0x1: AES_INVERSE :

SRC_CTL0.OFFSET specifies the offset of the round key (as used in the first inverse cipher round) in the memory buffer.
SRC_CTL1.OFFSET specifies the offset of the ciphertext in the memory buffer.
DST_CTL0.OFFSET specifies the offset of the key (as used by the last inverse cipher round) in the memory buffer.
DST_CTL1.OFFSET specifies the offset of the plaintext in the memory buffer.

0x10: SHA :

SRC_CTL0.OFFSET specifies the offset of the message in the memory buffer.
SRC_CTL1.OFFSET specifies the offset of the input hash in the memory buffer.
DST_CTL0.OFFSET specifies the offset of a temporary buffer (to hold message schedule round constants) in the memory buffer.
DST_CTL1.OFFSET specifies the offset of the output hash in the memory buffer.

0x18: CRC :

SRC_CTL0.OFFSET specifies the offset of the data in the memory buffer.

When the operation has completed, the resulting CRC can be read from CRC_REM.

23.1.2 CRYPTO_STATUS

Status

Address: 0x402C0004

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							W
Name	None [7:1]							BUSY

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	BUSY	Reflects the state of the component: '0': IP (AES, SHA, CRC component) is not busy. '1': IP (AES, SHA, CRC component) is busy performing a operation. An operation is started through the CMD register or through the "tr_in" input trigger. When the IP is busy, it is NOT possible to start another operation. When the IP is busy, it is possible to access the memory buffer (to prepare for another operation). Default Value: 0

23.1.3 CRYPTO_CMD

Command

Address: 0x402C0008

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW1S
HW Access	None							RW1C
Name	None [7:1]							START

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	START	FW sets this field to '1' to start an operation as specified by CTL.OPCODE. HW sets this field to '0' to indicate that the operation has completed. HW can start an operation through the "tr_in" input trigger. A rising edge ('0' to '1' transition) on this trigger starts an operation (as specified by CTL.OPCODE). When an operation completes, a two cycle '1' pulse (on "clk_sys") is generated on the "tr_out" output trigger. SW and HW control over the start of an operation should not be mixed. When an operation is busy (STATUS.BUSY is '1'), no new operation can be started. A SW write to START is ignored and a HW input trigger "tr_in" rising edge is ignored. Default Value: 0

23.1.4 CRYPTO_SRC_CTL0

Source control 0

Address: 0x402C0010

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW						None	
HW Access	R						None	
Name	OFFSET [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	OFFSET [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	
HW Access	None						R	
Name	None [23:18]						OFFSET [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
17 : 2	OFFSET	Word (32-bit) offset of source 0 in the data buffer. Default Value: 0

23.1.5 CRYPTO_SRC_CTL1

Source control 1

Address: 0x402C0014

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW						None	
HW Access	R						None	
Name	OFFSET [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	OFFSET [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	
HW Access	None						R	
Name	None [23:18]						OFFSET [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
17 : 2	OFFSET	Word (32-bit) offset of source 1 in the data buffer. Default Value: 0

23.1.6 CRYPTO_DST_CTL0

Destination control 0

Address: 0x402C0020

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW						None	
HW Access	R						None	
Name	OFFSET [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	OFFSET [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	
HW Access	None						R	
Name	None [23:18]						OFFSET [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
17 : 2	OFFSET	Word (32-bit) offset of destination 0 in the data buffer. Default Value: 0

23.1.7 CRYPTO_DST_CTL1

Destination control 1

Address: 0x402C0024

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW						None	
HW Access	R						None	
Name	OFFSET [7:2]						None [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	OFFSET [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None						RW	
HW Access	None						R	
Name	None [23:18]						OFFSET [17:16]	

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
17 : 2	OFFSET	Word (32-bit) offset of destination 1 in the data buffer. Default Value: 0

23.1.8 CRYPTO_AES_CTL

AES control

Address: 0x402C0100

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	
HW Access	None						R	
Name	None [7:2]						KEY_SIZE [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1 : 0	KEY_SIZE	AES key size: "0": 128-bit key, 10 rounds AES (inverse) cipher operation. SRC_CTL0 and DST_CTL0 specify the offset of a 16 Byte key in the memory buffer. "1": 192-bit key, 12 rounds AES (inverse) cipher operation. SRC_CTL0 and DST_CTL0 specify the offset of a 24 Byte key in the memory buffer. "2": 256-bit key, 14 rounds AES (inverse) cipher operation. SRC_CTL0 and DST_CTL0 specify the offset of a 32 Byte key in the memory buffer. "3": undefined Default Value: 0

23.1.9 CRYPTO_PR_CTL

Pseudo random control

Address: 0x402C0200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	MAX [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	MAX [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	MAX [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	MAX [31:24]							

Bits	Name	Description
31 : 0	MAX	Specifies the maximum random value of the pseudo random number generator: "0": produces a random number in the range {0} "1": produces a random number in the range [0, 1] "2": produces a random number in the range [0, 1, 2] "3": produces a random number in the range [0, 3] ... "(2^32)-1": produces a random number in the range [0, (2^32)-1]. Default Value: 0

23.1.10 CRYPTO_PR_CMD

Pseudo random command

Address: 0x402C0208

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							RW1C
Name	None [7:1]							START

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	START	SW sets this field to '1' to start the pseudo ransom number generator. HW clears this field to '0' when the operation has completed and the resulting pseudo random number (in the range [0, PR_CTL.MAX]) can be read from PR_RESULT. Default Value: 0

23.1.11 CRYPTO_PR_LFSR_CTL0

Pseudo random LFSR control 0

Address: 0x402C0210

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	LFSR32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	LFSR32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	LFSR32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	LFSR32 [31:24]							

Bits	Name	Description
31 : 0	LFSR32	State of a 32-bit Linear Feedback Shift Registers (LFSR) that is used to generate a pseudo random bit sequence. This register needs to be initialized by SW. The initialization value should be different from "0". The three PR_LFSR_CTL registers represents the state of a 32-bit, 31-bit and 29-bit LFSR. Individually, these LFSRs generate a pseudo random bit sequence that repeats itself after (2^32)-1, (2^31)-1 and (2^29)-1 bits. The numbers (2^32)-1, (2^31)-1 and (2^29)-1 are relatively prime (their greatest common denominator is "1"). The three bit sequence are combined (XOR'd) into a single bitstream to create a pseudo random bit sequence that repeats itself after ((2^32)-1) * ((2^31)-1) * ((2*29)-1) bits. The following polynomials are used: - 32-bit irreducible polynomial: x^32+x^30+x^26+x^25+1. - 31-bit irreducible polynomial: x^31+x^28+1. - 29-bit irreducible polynomial: x^29+x^27+1. Default Value: 0

23.1.12 CRYPTO_PR_LFSR_CTL1

Pseudo random LFSR control 1

Address: 0x402C0214

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	LFSR31 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	LFSR31 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	LFSR31 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None	RW						
HW Access	None	RW						
Name	None	LFSR31 [30:24]						

Bits	Name	Description
30 : 0	LFSR31	State of a 31-bit Linear Feedback Shift Registers (LFSR) that is used to generate a pseudo random bit sequence. See PR_LFSR_CTL0. Default Value: 0

23.1.13 CRYPTO_PR_LFSR_CTL2

Pseudo random LFSR control 2

Address: 0x402C0218

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	LFSR29 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	LFSR29 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	LFSR29 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None			RW				
HW Access	None			RW				
Name	None [31:29]			LFSR29 [28:24]				

Bits	Name	Description
28 : 0	LFSR29	State of a 29-bit Linear Feedback Shift Registers (LFSR) that is used to generate a pseudo random bit sequence. See PR_LFSR_CTL0. Default Value: 0

23.1.14 CRYPTO_PR_RESULT

Pseudo random status

Address: 0x402C0220

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	A							
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	A							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Result of a pseudo random number generation operation. The resulting value DATA is in the range [0, PR_CTL.MAX]. HW generates the number in this field. Note that SW can write this field. This functionality can be used prevent information leakage from the privileged domain to the user domain. Default Value: 0

23.1.15 CRYPTO_TR_CTL0

True random control 0

Address: 0x402C0280

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	SAMPLE_CLOCK_DIV [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	RED_CLOCK_DIV [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	INIT_DELAY [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None		RW	RW	None			RW
HW Access	None		R	R	None			R
Name	None [31:30]		STOP_ON_RC_DETECT	STOP_ON_AP_DETECT	None [27:25]			VON_NEUMAN_N_CORR

Bits	Name	Description
29	STOP_ON_RC_DETECT	Specifies if TRNG functionality is stopped on a repetition count test detection (when HW sets INTR.TR_RC_DETECT to '1'): '0': Functionality is NOT stopped. '1': Functionality is stopped (TR_CMD fields are set to '0' by HW). Default Value: 0
28	STOP_ON_AP_DETECT	Specifies if TRNG functionality is stopped on an adaptive proportion test detection (when HW sets INTR.TR_AP_DETECT to '1'): '0': Functionality is NOT stopped. '1': Functionality is stopped (TR_CMD fields are set to '0' by HW). Default Value: 0

23.1.15 CRYPTO_TR_CTL0 (continued)

24	VON_NEUMANN_CORR	Specifies if the "von Neumann corrector" is disabled or enabled: '0': disabled. '1': enabled. The "von Neumann corrector" post-processes the reduced bits to remove a '0' or '1' bias. The corrector operates on reduced bit pairs ("oldest bit, newest bit"): "00": no bit is produced. "01": '0' bit is produced (oldest bit). "10": '1' bit is produced (oldest bit). "11": no bit is produced. Note that the corrector produces bits at a random pace and at a frequency that is 1/4 of the reduced bit frequency (reduced bits are processed in pairs, and half of the pairs do NOT produce a bit). Default Value: 0
23 : 16	INIT_DELAY	Specifies an initialization delay: number of removed/dropped samples before reduced bits are generated. This field should be programmed in the range [1, 255]. After starting the oscillators, at least the first 2 samples should be removed/dropped to clear the state of internal synchronizers. In addition, it is advised to drop the second 2 samples from the oscillators (to circumvent the semi-predictable oscillator startup behavior). This result in the default field value of "3". Field encoding is as follows: "0": 1 sample is dropped. "1": 2 samples are dropped. ... "255": 256 samples are dropped. The TR_INITIALIZED interrupt cause is set to '1', when the initialization delay is passed. Default Value: 3
15 : 8	RED_CLOCK_DIV	Specifies the clock divider that is used to produce reduced bits. "0": 1 reduced bit is produced for each sample. "1": 1 reduced bit is produced for each 2 samples. ... "255": 1 reduced bit is produced for each 256 samples. The reduced bits are considered random bits and shifted into TR_RESULT0.DATA32. Default Value: 0
7 : 0	SAMPLE_CLOCK_DIV	Specifies the clock divider that is used to sample oscillator data. This clock divider is wrt. "clk_sys". "0": sample clock is "clk_sys". "1": sample clock is "clk_sys"/2. ... "255": sample clock is "clk_sys"/256. Default Value: 0

23.1.16 CRYPTO_TR_CTL1

True random control 1

Address: 0x402C0284

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		R					
Name	None [7:6]		DATA_BIT_SIZE [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	DATA_BIT_SIZE	Specifies the number of desired of bits in the generated random number (legal range: [1, 32]). The TR_DATA_AVAILABLE interrupt cause is set to '1' when TR_RESULT1.DATA_BIT_SIZE >= DATA_BIT_SIZE. Default Value: 32

23.1.17 CRYPTO_TR_RESULT0

True random result 0

Address: 0x402C0288

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	A							
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	A							
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	A							
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	A							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Generated true random number. HW generates the number in this field. When a new random bit is generated, it is shifted into the lowest bit position (DATA32[0]) and the highest bit position (DATA32[31]) is shifted out. Note that SW can write this field. This functionality can be used prevent information leakage. Default Value: 0

23.1.18 CRYPTO_TR_RESULT1

True random result 1

Address: 0x402C028C

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW					
HW Access	None		A					
Name	None [7:6]		DATA_BIT_SIZE [5:0]					

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5 : 0	DATA_BIT_SIZE	Specifies the number of bits in the generated true random number (TR_RESULT0.DATA32). When a new random bit is generated, this field is incremented by '1'. The value is in the range [0, 32] (a saturating counter is used). Note that SW can write this field. This functionality can be used prevent information leakage. Typically, this field is updated/decremented in the interrupt handler. The interrupt handler decrements the field by the number of consumed bits. If the interrupt handler does NOT update this field (and TR_RESULT.DATA_BIT_SIZE is unchanged), the TR_DATA_AVAILABLE interrupt cause will remain activated. Therefore, proper interrupt based usage is as follows: - Consume bits from TR_RESULT0. - Write consumed bits in TR_RESULT0 to '0's (if information leakage needs to prevented). - Decrement TR_RESULT1 by the number of consumed bits. - Deactivate INTR.TR_DATA_AVAILABLE. Default Value: 0

23.1.19 CRYPTO_TR_CMD

True random command

Address: 0x402C0290

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None		RW	RW	RW	RW	RW	RW
HW Access	None		RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
Name	None [7:6]		START_-FIRO31	START_-FIRO15	START_GA-RO31	START_GA-RO15	START_RO 15	START_RO 11

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
5	START_FIRO31	SW sets this field to '1' to start the programmable Fibonacci ring oscillator with up to 31 inverters. The TR_FIRO_CTL register specifies the programmable polynomial. Default Value: 0
4	START_FIRO15	SW sets this field to '1' to start the fixed Fibonacci ring oscillator with 15 inverters. Default Value: 0
3	START_GARO31	SW sets this field to '1' to start the programmable Galois ring oscillator with up to 31 inverters. The TR_GARO_CTL register specifies the programmable polynomial. Default Value: 0
2	START_GARO15	SW sets this field to '1' to start the fixed Galois ring oscillator with 15 inverters. Default Value: 0
1	START_RO15	SW sets this field to '1' to start the ring oscillator with 15 inverters. Default Value: 0
0	START_RO11	SW sets this field to '1' to start the ring oscillator with 11 inverters. Default Value: 0

23.1.20 CRYPTO_TR_GARO_CTL

True random GARO control

Address: 0x402C02A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	POLYNOMIAL31 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	POLYNOMIAL31 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	POLYNOMIAL31 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None	RW						
HW Access	None	R						
Name	None	POLYNOMIAL31 [30:24]						

Bits	Name	Description
30 : 0	POLYNOMIAL31	Polynomial for programmable Galois ring oscillator. The polynomial is represented WITHOUT the high order bit (this bit is always assumed '1'). The polynomial should be aligned such that the more significant bits (bit 30 and down) contain the polynomial and the less significant bits (bit 0 and up) contain padding '0's. Default Value: 0

23.1.21 CRYPTO_TR_FIRO_CTL

True random FIRO control

Address: 0x402C02A4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	POLYNOMIAL31 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	POLYNOMIAL31 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	POLYNOMIAL31 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None	RW						
HW Access	None	R						
Name	None	POLYNOMIAL31 [30:24]						

Bits	Name	Description
30 : 0	POLYNOMIAL31	Polynomial for programmable Fibonacci ring oscillator. The polynomial is represented WITHOUT the high order bit (this bit is always assumed '1'). The polynomial should be aligned such that the more significant bits (bit 30 and down) contain the polynomial and the less significant bits (bit 0 and up) contain padding '0's. Default Value: 0

23.1.22 CRYPTO_TR_MON_CTL

True random monitor control

Address: 0x402C02C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	
HW Access	None						R	
Name	None [7:2]						BITSTREAM_SEL [1:0]	

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1 : 0	BITSTREAM_SEL	Selection of the bitstream: "0": DAS bitstream. "1": RED bitstream. "2": TR bitstream. "3": Undefined. Default Value: 2

23.1.23 CRYPTO_TR_MON_CMD

True random monitor command

Address: 0x402C02C8

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						RW	RW
HW Access	None						RW1C	RW1C
Name	None [7:2]						START_RC	START_AP

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
1	START_RC	Repetition count (RC) test enable: '0': Disabled. '1': Enabled. On a RC detection, HW sets this field to '0' and sets INTR.TR_RC_DETECT to '1. Default Value: 0
0	START_AP	Adaptive proportion (AP) test enable: '0': Stopped. '1': Started. On a AP detection, HW sets this field to '0' and sets INTR.TR_AP_DETECT to '1. Default Value: 0

23.1.24 CRYPTO_TR_MON_RC_CTL

True random monitor RC control

Address: 0x402C02D0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CUTOFF_COUNT8 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	CUTOFF_COUNT8	Cutoff count (legal range is [1, 255]): "0": Illegal. "1": 1 repetition. ... "255": 255 repetitions. Default Value: 255

23.1.25 CRYPTO_TR_MON_RC_STATUS0

True random monitor RC status 0

Address: 0x402C02D8

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							BIT

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	BIT	Current active bit value: '0': '0'. '1': '1'. This field is only valid when TR_MON_RC_STATUS1.REP_COUNT is NOT equal to "0". Default Value: 0

23.1.26 CRYPTO_TR_MON_RC_STATUS1

True random monitor RC status 1

Address: 0x402C02DC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	REP_COUNT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	REP_COUNT	Number of repetitions of the current active bit counter: "0": 0 repetitions. ... "255": 255 repetitions. Default Value: 0

23.1.27 CRYPTO_TR_MON_AP_CTL

True random monitor AP control

Address: 0x402C02E0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	CUTOFF_COUNT16 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	CUTOFF_COUNT16 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	WINDOW_SIZE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	WINDOW_SIZE [31:24]							

Bits	Name	Description
31 : 16	WINDOW_SIZE	Window size (minus 1) : "0": 1 bit. ... "65535": 65536 bits. Default Value: 65535
15 : 0	CUTOFF_COUNT16	Cutoff count (legal range is [1, 65535]). "0": Illegal. "1": 1 occurance. ... "65535": 65535 occurances. Default Value: 65535

23.1.28 CRYPTO_TR_MON_AP_STATUS0

True random monitor AP status 0

Address: 0x402C02E8

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							R
HW Access	None							RW
Name	None [7:1]							BIT

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	BIT	Current active bit value: '0': '0'. '1': '1'. This field is only valid when TR_MON_AP_STATUS1.OCC_COUNT is NOT equal to "0". Default Value: 0

23.1.29 CRYPTO_TR_MON_AP_STATUS1

True random monitor AP status 1

Address: 0x402C02EC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	RW							
Name	OCC_COUNT [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	RW							
Name	OCC_COUNT [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	RW							
Name	WINDOW_INDEX [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	RW							
Name	WINDOW_INDEX [31:24]							

Bits	Name	Description
31 : 16	WINDOW_INDEX	Counter to keep track of the current index in the window (counts down from TR_MON_AP_CTL.WINDOW_SIZE to "0"). Default Value: 0
15 : 0	OCC_COUNT	Number of occurances of the current active bit counter: "0": 0 occurances ... "65535": 65535 occurances Default Value: 0

23.1.30 CRYPTO_SHA_CTL

SHA control

Address: 0x402C0300

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW		
HW Access	None					R		
Name	None [7:3]					MODE [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2 : 0	MODE	SHA mode: "0": SHA1. The message is 16 32 bits words: 64 Bytes. The hash is 5 32-bit words: 20 Bytes. There are 80 32-bit message schedule round constants: 320 Bytes. "1": SHA2_224, SHA2_256. The message is 16 32-bit words: 64 Bytes. The hash is 8 32-bit words: 32 Bytes. There are 64 32-bit message schedule round constants: 256 Bytes. The difference between SHA2-224 and SHA2-256 is entirely in software. "2": undefined "3": SHA2-384 (NOT supported) "4": SHA2-512 (NOT supported) "5": SHA2-512/224 (NOT supported) "6": SHA2-512/256 (NOT supported) "7": undefined Default Value: 0

23.1.31 CRYPTO_CRC_DATA_CTL0

CRC data control 0

Address: 0x402C0400

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							DATA_REVERSE

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	DATA_SIZE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	DATA_SIZE [31:24]							

Bits	Name	Description
31 : 16	DATA_SIZE	Size of the data in bytes (the size is limited by the memory buffer size), the number bytes processed is DATA_SIZE+1: "0": 1 byte. "1": 2 bytes. ... "2047": 2048 bytes. Default Value: 0
0	DATA_REVERSE	Specifies the bit order in which a data byte is processed (reversal is performed after XORing): '0': Most significant bit (bit 1) first. '1': Least significant bit (bit 0) first. Default Value: 0

23.1.32 CRYPTO_CRC_DATA_CTL1

CRC data control 1

Address: 0x402C0404

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	DATA_XOR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	DATA_XOR	Specifies a byte mask with which each data byte is XOR'd. The XOR is performed before data reversal. Default Value: 0

23.1.33 CRYPTO_CRC_POL_CTL

CRC polynomial control

Address: 0x402C0410

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	POLYNOMIAL [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	POLYNOMIAL [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	POLYNOMIAL [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	POLYNOMIAL [31:24]							

Bits	Name	Description
31 : 0	POLYNOMIAL	CRC polynomial. The polynomial is represented without the high order bit (this bit is always assumed '1'). The polynomial should be aligned such that the more significant bits (bit 31 and down) contain the polynomial and the less significant bits (bit 0 and up) contain padding '0's. Some frequently used polynomials: - CRC32: POLYNOMIAL is 0x04c11db7. - CRC16: POLYNOMIAL is 0x80050000. - CRC16 CCITT: POLYNOMIAL is 0x10210000. Default Value: 0

23.1.34 CRYPTO_CRC_LFSR_CTL

CRC LFSR control

Address: 0x402C0414

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	LFSR32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	LFSR32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	LFSR32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	LFSR32 [31:24]							

Bits	Name	Description
31 : 0	LFSR32	State of a 32-bit Linear Feedback Shift Registers (LFSR) that is used to implement CRC. This register needs to be initialized by SW to provide the CRC seed value. The seed value should be aligned such that the more significant bits (bit 31 and down) contain the seed value and the less significant bits (bit 0 and up) contain padding '0's. Default Value: 0

23.1.35 CRYPTO_CRC_REM_CTL0

CRC remainder control 0

Address: 0x402C0420

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None							RW
HW Access	None							R
Name	None [7:1]							REM_REVERSE

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
0	REM_REVERSE	Specifies whether the remainder is bit reversed (reversal is performed after XORing): '0': No. '1': Yes. Default Value: 0

23.1.36 CRYPTO_CRC_REM_CTL1

CRC remainder control 1

Address: 0x402C0424

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	R							
Name	REM_XOR [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	R							
Name	REM_XOR [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	R							
Name	REM_XOR [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	R							
Name	REM_XOR [31:24]							

Bits	Name	Description
31 : 0	REM_XOR	Specifies a mask with which the LFSR register is XOR'd to produce a remainder. The XOR is performed before remainder reversal. Default Value: 0

23.1.37 CRYPTO_CRC_REM

CRC remainder status

Address: 0x402C0428

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	W							
Name	REM [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	W							
Name	REM [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	W							
Name	REM [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	W							
Name	REM [31:24]							

Bits	Name	Description
31 : 0	REM	Remainder value. The alignment of the remainder depends on CRC_REM_CTL0.REM_REVERSE: '0': the more significant bits (bit 31 and down) contain the remainder. '1': the less significant bits (bit 0 and up) contain the remainder. Default Value: Undefined

23.1.38 CRYPTO_INTR

Interrupt request

Address: 0x402C07C0

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1C	RW1C	None				RW1C	RW1C
HW Access	RW1S	RW1S	None				RW1S	RW1S
Name	TR_-DATA_AVAILABLE	TR_INI-TIALIZED	None [5:2]				AC-CESS_ER-ROR	DONE

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW1C	RW1C
HW Access	None						RW1S	RW1S
Name	None [15:10]						TR_RC_-DETECT	TR_AP_DE-TECT

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	TR_RC_DETECT	This interrupt cause is activated (HW sets the field to '1') when the true random number generator monitor adaptive proportion test detects a disproportionate occurrence of a specific bit value. Default Value: 0
8	TR_AP_DETECT	This interrupt cause is activated (HW sets the field to '1') when the true random number generator monitor repetition count test detects a repetition of a specific bit value. Default Value: 0
7	TR_DATA_AVAILABLE	This interrupt cause is activated (HW sets the field to '1') when the true random number generator has generated a data value of the specified bit size: (TR_RESULT.DATA_BIT_SIZE >= TR_CTL.DATA_BIT_SIZE). See TR_RESULT1.DATA_BIT_SIZE for proper deactivation of this interrupt cause. Default Value: 0
6	TR_INITIALIZED	This interrupt cause is activated (HW sets the field to '1') when the true random number generator is initialized. Default Value: 0

23.1.38 CRYPTO_INTR (continued)

1	ACCESS_ERROR	This interrupt cause is activated (HW sets the field to '1') when a command/operation is aborted due to a user/privileged mode violation of the buffer accesses. Default Value: 0
0	DONE	This interrupt cause is activated (HW sets the field to '1') when a command/operation completes. SW writes a '1' to this field to clear the interrupt cause. As an alternative to interrupt driven operation, SW can poll the STATUS.BUSY field to determine completion of an operation. Default Value: 0

23.1.39 CRYPTO_INTR_SET

Interrupt set request

Address: 0x402C07C4

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW1S	RW1S	None				RW1S	RW1S
HW Access	A	A	None				A	A
Name	TR_-DATA_AVAILABLE	TR_INI-TIALIZED	None [5:2]				AC-CESS_ER-ROR	DONE

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW1S	RW1S
HW Access	None						A	A
Name	None [15:10]						TR_RC_-DETECT	TR_AP_DE-TECT

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	TR_RC_DETECT	SW writes a '1' to this field to set the corresponding field in interrupt request register. Default Value: 0
8	TR_AP_DETECT	SW writes a '1' to this field to set the corresponding field in interrupt request register. Default Value: 0
7	TR_DATA_AVAILABLE	SW writes a '1' to this field to set the corresponding field in interrupt request register. Default Value: 0
6	TR_INITIALIZED	SW writes a '1' to this field to set the corresponding field in interrupt request register. Default Value: 0
1	ACCESS_ERROR	SW writes a '1' to this field to set the corresponding field in interrupt request register. Default Value: 0
0	DONE	SW writes a '1' to this field to set the corresponding field in interrupt request register. Default Value: 0

23.1.40 CRYPTO_INTR_MASK

Interrupt mask

Address: 0x402C07C8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW	RW	None				RW	RW
HW Access	R	R	None				R	R
Name	TR_-DATA_AVAILABLE	TR_INI-TIALIZED	None [5:2]				AC-CESS_ER-ROR	DONE

Bits	15	14	13	12	11	10	9	8
SW Access	None						RW	RW
HW Access	None						R	R
Name	None [15:10]						TR_RC_-DETECT	TR_AP_DE-TECT

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	TR_RC_DETECT	Mask bit for corresponding field in interrupt request register. Default Value: 0
8	TR_AP_DETECT	Mask bit for corresponding field in interrupt request register. Default Value: 0
7	TR_DATA_AVAILABLE	Mask bit for corresponding field in interrupt request register. Default Value: 0
6	TR_INITIALIZED	Mask bit for corresponding field in interrupt request register. Default Value: 0
1	ACCESS_ERROR	Mask bit for corresponding field in interrupt request register. Default Value: 0
0	DONE	Mask bit for corresponding field in interrupt request register. Default Value: 0

23.1.41 CRYPTO_INTR_MASKED

Interrupt masked

Address: 0x402C07CC

Retention: Not Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R	R	None				R	R
HW Access	W	W	None				W	W
Name	TR_-DATA_AVAILABLE	TR_INI-TIALIZED	None [5:2]				AC-CESS_ER-ROR	DONE

Bits	15	14	13	12	11	10	9	8
SW Access	None						R	R
HW Access	None						W	W
Name	None [15:10]						TR_RC_-DETECT	TR_AP_DE-TECT

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
9	TR_RC_DETECT	Logical and of corresponding request and mask bits. Default Value: 0
8	TR_AP_DETECT	Logical and of corresponding request and mask bits. Default Value: 0
7	TR_DATA_AVAILABLE	Logical and of corresponding request and mask bits. Default Value: 0
6	TR_INITIALIZED	Logical and of corresponding request and mask bits. Default Value: 0
1	ACCESS_ERROR	Logical and of corresponding request and mask bits. Default Value: 0
0	DONE	Logical and of corresponding request and mask bits. Default Value: 0

23.1.42 CRYPTO_MEM_BUFF0

Memory buffer

Address: 0x402C0800

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	RW							
HW Access	RW							
Name	DATA32 [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	RW							
HW Access	RW							
Name	DATA32 [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	RW							
HW Access	RW							
Name	DATA32 [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	RW							
HW Access	RW							
Name	DATA32 [31:24]							

Bits	Name	Description
31 : 0	DATA32	Default Value: Undefined

23.1.43 CRYPTO_PRIV_BUF

Buffer Privilege register

Address: 0x402CFF00

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None					RW		
HW Access	None					R		
Name	None [7:3]					BUF_PRIV_LIMIT [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
2 : 0	BUF_PRIV_LIMIT	Indicates how big the privileged area of the Buffer is in power of 2 bytes, i.e. first 2^(BUF_PRIV_LIMIT+4) Bytes are Privileged, with the exception of the 0 value. "0": Entire Buffer is user mode accessible "1": First 32 Bytes are Privileged. "2": First 64 Bytes are Privileged. ... "6": First 1024 Bytes are Privileged. "7": First 2048 Bytes are Privileged. 2^(BUF_PRIV_LIMIT+5) >= "Buffer capacity": Entire buffer is Privileged (note this disables the CRC operation which requires user memory to operate). Default Value: 0

24 ROM Table Registers

This section discusses the ROM Table registers. It lists all the registers in mapping tables, in address order.

24.1 Register Details

Register	Address	Description
ROMTABLE_ADDR	0xF0000000	Link to Cortex M0 ROM Table.
ROMTABLE_DID	0xF0000FCC	Device Type Identifier register.
ROMTABLE_PID4	0xF0000FD0	Peripheral Identification Register 4.
ROMTABLE_PID5	0xF0000FD4	Peripheral Identification Register 5.
ROMTABLE_PID6	0xF0000FD8	Peripheral Identification Register 6.
ROMTABLE_PID7	0xF0000FDC	Peripheral Identification Register 7.
ROMTABLE_PID0	0xF0000FE0	Peripheral Identification Register 0.
ROMTABLE_PID1	0xF0000FE4	Peripheral Identification Register 1.
ROMTABLE_PID2	0xF0000FE8	Peripheral Identification Register 2.
ROMTABLE_PID3	0xF0000FEC	Peripheral Identification Register 3.
ROMTABLE_CID0	0xF0000FF0	Component Identification Register 0.
ROMTABLE_CID1	0xF0000FF4	Component Identification Register 1.
ROMTABLE_CID2	0xF0000FF8	Component Identification Register 2.
ROMTABLE_CID3	0xF0000FFC	Component Identification Register 3.

24.1.1 ROMTABLE_ADDR

Link to Cortex M0 ROM Table.

Address: 0xF0000000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	None						R	R
HW Access	None						R	R
Name	None [7:2]						FOR-MAT_32BIT	PRESENT

Bits	15	14	13	12	11	10	9	8
SW Access	R				None			
HW Access	R				None			
Name	ADDR_OFFSET [15:12]				None [11:8]			

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	ADDR_OFFSET [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	ADDR_OFFSET [31:24]							

Bits	Name	Description
31 : 12	ADDR_OFFSET	Address offset of the Cortex-M0 ROM Table base address (0xe00f:f000) wrt. Cypress chip specific ROM Table base address (0xf000:0000). ADDR_OFFSET[19:0] = 0xe00f:f - 0xf000:0 = 0xf00f:f. Default Value: 983295
1	FORMAT_32BIT	ROM Table format: '0: 8-bit format. '1': 32-bit format. Default Value: 1
0	PRESENT	Entry present. Default Value: 1

24.1.2 ROMTABLE_DID

Device Type Identifier register.

Address: 0xF0000FCC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	. Default Value: 1

24.1.3 ROMTABLE_PID4

Peripheral Identification Register 4.

Address: 0xF0000FD0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	R				R			
Name	COUNT [7:4]				JEP_CONTINUATION [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	COUNT	Size of ROM Table is 2^COUNT * 4 KByte. Default Value: 0
3 : 0	JEP_CONTINUATION	JEP106 continuation code. This value is product specific and specified as part of the product definition in the CPUSS.JEPCONTINUATION parameter. Default Value: Undefined

24.1.4 ROMTABLE_PID5

Peripheral Identification Register 5.

Address: 0xF0000FD4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	. Default Value: 0

24.1.5 ROMTABLE_PID6

Peripheral Identification Register 6.

Address: 0xF0000FD8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	. Default Value: 0

24.1.6 ROMTABLE_PID7

Peripheral Identification Register 7.

Address: 0xF0000FDC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	. Default Value: 0

24.1.7 ROMTABLE_PID0

Peripheral Identification Register 0.

Address: 0xF0000FE0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	PN_MIN [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 0	PN_MIN	JEP106 part number. 4 lsbs of CPUSS.PARTNUMBER parameter. Default Value: Undefined

24.1.8 ROMTABLE_PID1

Peripheral Identification Register 1.

Address: 0xF0000FE4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	R				R			
Name	JEPID_MIN [7:4]				PN_MAJ [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	JEPID_MIN	JEP106 vendor id. 4 lsbs of CPUSS.JEPID parameter. Default Value: Undefined
3 : 0	PN_MAJ	JEP106 part number. 4 msbs of CPUSS.PARTNUMBER parameter. Default Value: Undefined

24.1.9 ROMTABLE_PID2

Peripheral Identification Register 2.

Address: 0xF0000FE8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				None	R		
HW Access	R				None	R		
Name	REV [7:4]				None	JEPID_MAJ [2:0]		

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	REV	Major REVision number (chip specific). Identifies the design iteration of the component. For first tape out: 0x1. This field is incremented on subsequent tape outs. Default Value: Undefined
2 : 0	JEPID_MAJ	JEP106 vendor id. 4 msbs of CPUSS.JEPID parameter. Default Value: Undefined

24.1.10 ROMTABLE_PID3

Peripheral Identification Register 3.

Address: 0xF0000FEC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R				R			
HW Access	R				R			
Name	REV_AND [7:4]				CM [3:0]			

Bits	15	14	13	12	11	10	9	8
SW Access	None							
HW Access	None							
Name	None [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	None							
HW Access	None							
Name	None [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	None							
HW Access	None							
Name	None [31:24]							

Bits	Name	Description
7 : 4	REV_AND	Minor REVision number (chip specific). For first tape out: 0x1. This field is is incremented on subsequent tape outs. Default Value: Undefined
3 : 0	CM	Customer modified field. This field is used to track modifications to the original component design as a result of componenet IP reuse. Default Value: 0

24.1.11 ROMTABLE_CID0

Component Identification Register 0.

Address: 0xF0000FF0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component identification byte 0 of 4-byte component identification 0xB105:100D. Default Value: 13

24.1.12 ROMTABLE_CID1

Component Identification Register 1.

Address: 0xF0000FF4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component identification byte 1 of 4-byte component identification 0xB105:100D. Component class: "ROM Table". Default Value: 16

24.1.13 ROMTABLE_CID2

Component Identification Register 2.

Address: 0xF0000FF8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component identification byte 2 of 4-byte component identification 0xB105:100D. Default Value: 5

24.1.14 ROMTABLE_CID3

Component Identification Register 3.

Address: 0xF0000FFC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
SW Access	R							
HW Access	R							
Name	VALUE [7:0]							

Bits	15	14	13	12	11	10	9	8
SW Access	R							
HW Access	R							
Name	VALUE [15:8]							

Bits	23	22	21	20	19	18	17	16
SW Access	R							
HW Access	R							
Name	VALUE [23:16]							

Bits	31	30	29	28	27	26	25	24
SW Access	R							
HW Access	R							
Name	VALUE [31:24]							

Bits	Name	Description
31 : 0	VALUE	Component identification byte 3 of 4-byte component identification 0xB105:100D. Default Value: 177

Revision History

Revision History

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Revision	**ECN#**	**Issue Date**	**Description of Change**
**	7150026	07/16/2021	Initial release
*A	8027154	05/20/2024	Fixed broken links.