Counter reset and latch with corresponding pulse timings for PROFET™+2 12V

About this document

Scope and purpose

This application note intends to provide information regarding how the internal counter and latch reset work after a fault condition.

Intended audience

This document is targeted for customers who are using the DEN pin to reset the internal fault counter in PROFET™+2 12V.

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1 Introduction

PROFET™+2 12V includes several features: among them the diagnosis with which the switch can provide a feedback to the microcontroller. Fault conditions are reported both in ON and OFF state.

PROFET™+2 12V devices with Intelligent Restart Control have an internal counter which counts the number of fault events (up to 7). When the device latches, a reset can be applied to restart the counter.

PROFET™ +2 12V devices with Intelligent Latch have an internal latch which protects the output stage in case of a fault event. When the device latches, a reset can be applied to restart the counter.

1.1 Diagnostic functions

In PROFET™+2 12V diagnosis is an important feature which provides a feedback to the microcontroller via the IS pin. The device status is reported as a variable current flowing out of the *IS* pin which is then converted into a voltage via an external resistor R_{IS}. During normal operation, the diagnosis feedback is the so- called sense current. The magnitude of the sense current I_{IS} is proportional to the load current: the proportionality constant is defined as: $k_{ILIS} = I_{LOAD} / I_{IS}$.

If the diagnosis is active, and the PROFET™+2 12V determines that there is a fault (overcurrent or overtemperature), I_{IS} changes to $I_{IS(FAULT)}$ and the internal counter is incremented (the affected channel is switched OFF). The parameters that trigger the fault condition are $I_{L(OVL)}$, $T_{J(DYN)}$ and $T_{J(ABS)}$. Furthermore, the device latches or restarts depending on the particular protection concept used (*Intelligent Restart Control* or *Intelligent Latch*). The details are described in each product specific datasheet.

1.2 DEN pin ("Diagnostic Enable")

The DEN pin of the device enables or disables the diagnostic functions. By putting it to “high” the diagnostic functions are enabled. A maximum allowed voltage and a current for the DEN pin, both given by the internal logic, have to be taken into account: a higher voltage may destroy the pin and therefore the device. The user has to ensure that in their application the voltage and the current do not exceed the maximum ratings.

Therefore Infineon recommends an external resistor with the value of R_{DEN} = 4.7 kΩ in order to limit the current. This external resistor is also used as a protection for the microcontroller during overvoltage and reverse polarity. In ***Figure 1*** below it is shown how a PROFET™ +2 12V could be configured in an application, and how R_{DEN} is connected.

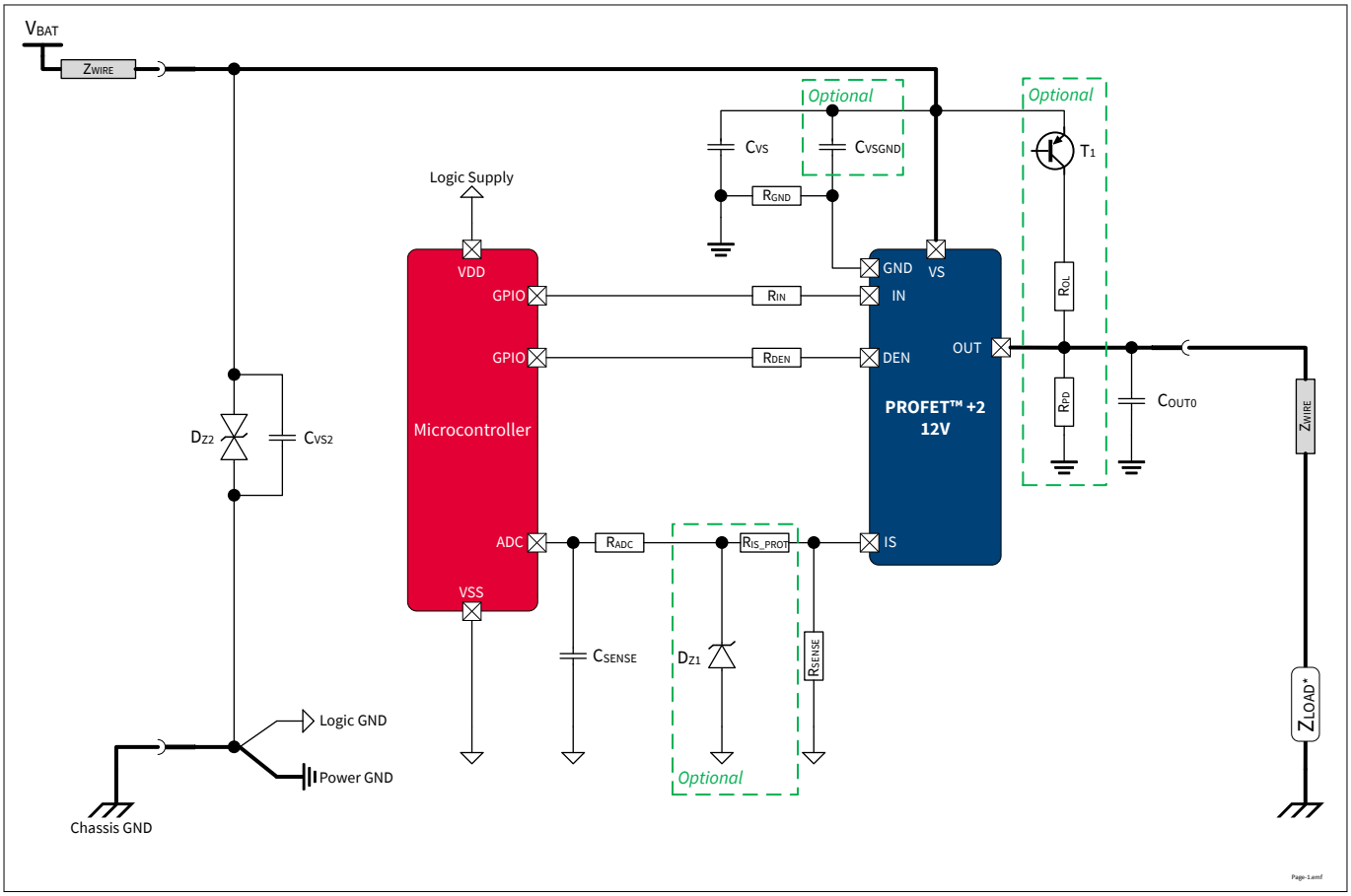

Figure 1 Application diagram for a single channel PROFET™+2 12V

2 Counter and latch reset

After a fault condition, there are 3 possibilities to reset the counter or the latch:

- disconnecting the battery
- toggling the IN pin meeting specific timing constraints
- DEN reset pulse

In case of a multichannel PROFET™+2 12V, each channel has its own counter, or latch, independent from the others.

2.1 Reset with battery disconnection

The internal counter or latch of PROFET™ +2 12V could be reset by disconnecting the device from the battery. In a real application, this is not practical therefore it is just listed for completeness.

2.2 Reset with IN toggling

If the input pin IN remains “low” for a time longer than $t_{DELAY(CR)}$ or $t_{DELAY(LR)}$ then the internal counter or latch is reset to the default value.

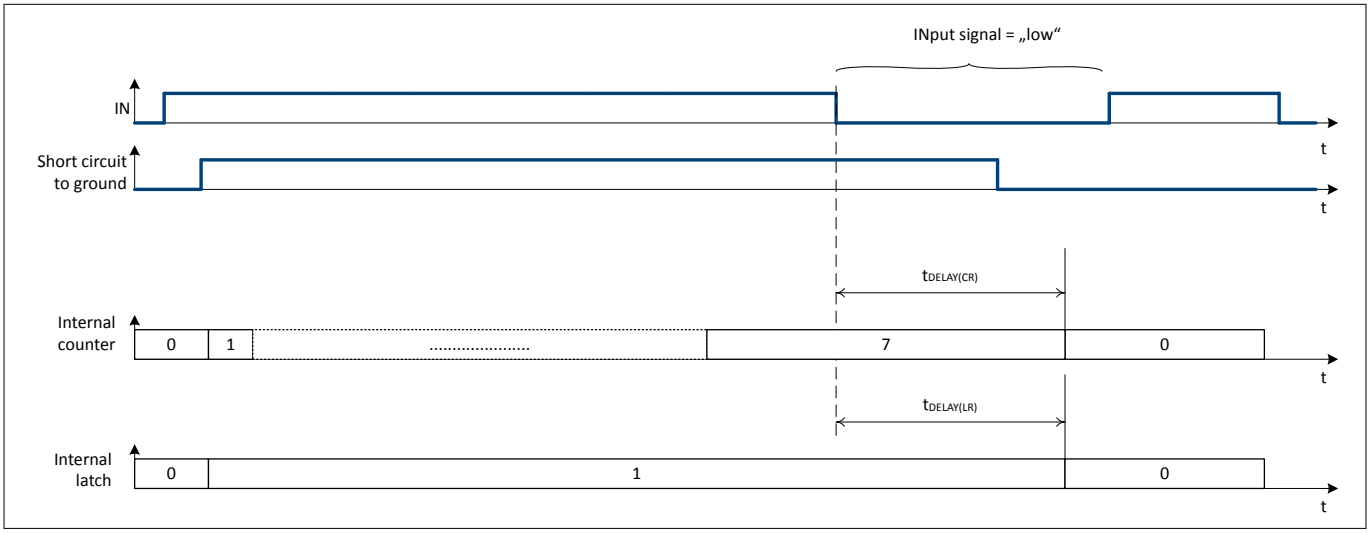

Figure 2 Time duration when the input signal is "low"

2.3 Reset with DEN pulse

It is possible to “force” a reset of the internal counter or latch without waiting for $t_{DELAY(CR)}$ or $t_{DELAY(LR)}$ by applying a pulse to the DEN pin while IN pin is “low”.

The pulse applied to DEN pin must have a duration longer than $t_{DEN(CR)}$ or $t_{DEN(LR)}$ to ensure a reset of the internal counter or latch, as specified in the datasheet.

There are also other parameters to take into account, as it can be seen in ***Figure 3***.

The parameters for Intelligent Latch devices (LR) are equivalent to those belonging to the device with the Intelligent Restart Control (CR) and are not shown in ***Figure 3***.

These two additional conditions have to be satisfied, in order to have a counter or latch reset:

- the time period between the previous falling edge and the actual rising edge of the DEN pulse is longer than $t_{DEN(LOW)\_CR\_DEN}$ or $t_{DEN(LOW)\_LR\_DEN}$
- the IN rising edge occurs after $t_{IN(LOW)\_CR\_DEN}$ or $t_{IN(LOW)\_LR\_DEN}$

At the end, to rise the next DEN pulse, it is not needed to wait for more than $t_{DEN(LOW)\_CR\_DEN}$ or $t_{DEN(LOW)\_LR\_DEN}$. This timing has to be respected only if a counter or latch reset is needed with the next DEN pulse. This means that DEN can be set to "high" at the same time as the input in this case.

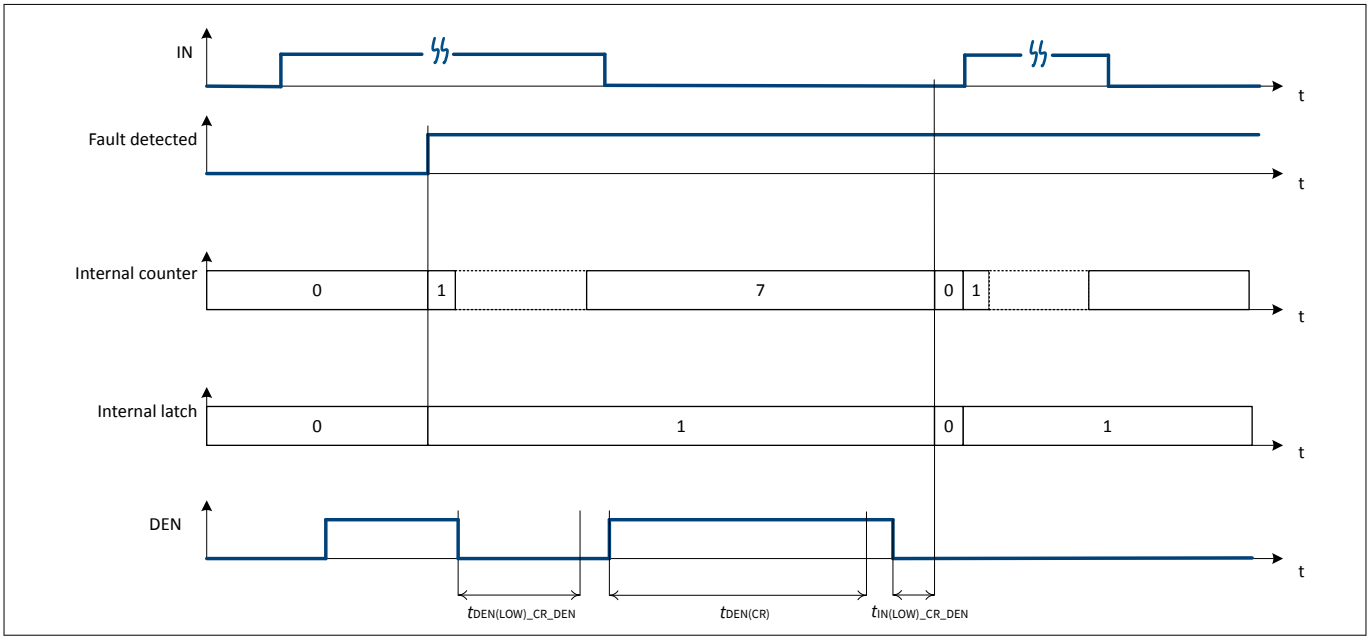

Figure 3 DEN pulse timings for counter or latch reset

2.3.1 DEN pulse delay with DSEL signal

When talking about multichannel devices, the channel targeted for the counter or latch reset must not change for at least $2xt_{DSEL(HOLD)\_CR\_DEN}+t_{DEN(LOW)\_CR\_DEN}$. The conditions explained in ***Figure 4*** and in ***Figure 5*** below must be fulfilled otherwise the reset may not happen.

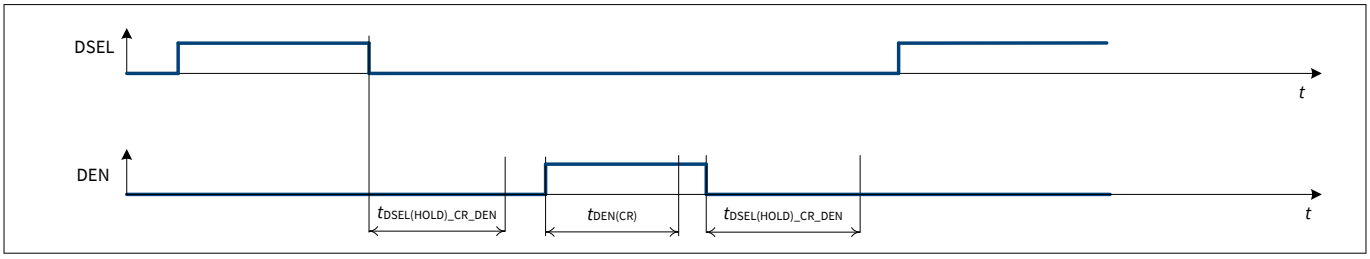

Figure 4 DEN pulse delay when channel 0 is selected

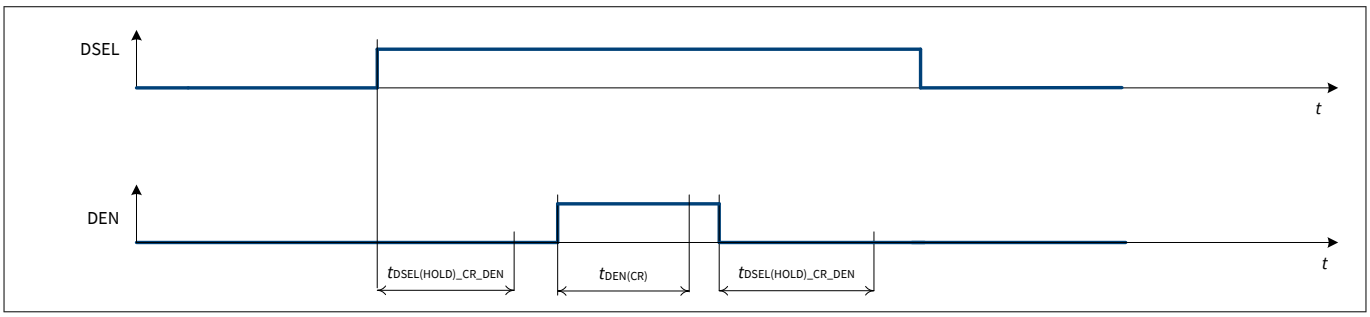

Figure 5 DEN pulse delay when channel 1 is selected

3 Electrical Characteristics: Protection - PROFET™

The following ***Table 1*** and ***Table 2*** show the parameters values contained in this application note.

Table 1 Electrical Characteristics: Protection for PROFET™+2 12V with Intelligent Restart Control

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Counter Reset delay Time after Fault Condition	$t_{DELAY(CR)}$	40	70	100	ms	*1)*
Minimum *DEN* Pulse Duration for Counter Reset	$t_{DEN(CR)}$	50	100	150	µs	*1)*
DEN Pulse Delay with *DSEL* for Counter Reset	$t_{DSEL(HOLD)\_CR\_DEN}$	–	–	1	µs	–
DEN Pulse Delay with *IN* for Counter Reset	$t_{IN(LOW)\_CR\_DEN}$	–	–	3	µs	–
DEN Pulse Delay for Counter Reset	$t_{DEN(LOW)\_CR\_DEN}$	–	–	10	µs	–

Table 2 Electrical Characteristics: Protection for PROFET™+2 12V with Intelligent Latch

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Latch Reset Delay Time after Fault Condition	$t_{DELAY(LR)}$	40	70	100	ms	*1)*
Minimum *DEN* Pulse Duration for Latch Reset	$t_{DEN(LR)}$	50	100	150	µs	*1)*
DEN Pulse Delay with *IN* for Latch Reset	$t_{IN(LOW)\_LR\_DEN}$	–	–	3	µs	–
DEN Pulse Delay for Latch Reset	$t_{DEN(LOW)\_LR\_DEN}$	–	–	10	µs	–

1 This parameter is part of the datasheet

4 Conclusion

In summary, multiple conditions have to be fulfilled in order to reset the internal counter or internal latch of the device. The first one (longer time method) concerns the time during which the input signal has to be “low”: this must be longer than the parameter $t_{DELAY(CR)}$ or $t_{DELAY(LR)}$ as specified in the datasheet.

An alternative shorter time method is also available for counter or latch reset period. In this way the DEN signal must be “high” during a “low” time slot of the input signal for a time which is longer than $t_{DEN(CR)}$ or $t_{DEN(LR)}$.

The time delay between consecutive DEN pulses must be longer than $t_{DEN(LOW)\_CR\_DEN}$ or $t_{DEN(LOW)\_LR\_DEN}$. A DEN pulse can rise at the same time of an input signal falling edge (with no timing restrictions) and must go "low" $t_{IN(LOW)\_CR\_DEN}$ or $t_{IN(LOW)\_LR\_DEN}$ before an input signal rising edge. A DEN pulse should occur while the DSEL signal is not changing (either it is “high” or “low”): the DEN must rise at least $t_{DSEL(HOLD)\_CR\_DEN}$ after the changing state (from “low” to “high” or viceversa) of the DSEL signal and must go "low" at least $t_{DSEL(HOLD)\_CR\_DEN}$ before the next changing state of DSEL.

5 Revision history

Table 3 Revision history

Document version	Date of release	Description of changes
Rev. 1.00	2020-01-27	Initial application note

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