EZ-PD™ PMG1-S0 Power Delivery MCU Gen1

EZ-PD™ PMG1 family general description

EZ-PD™ PMG1 (Power Delivery Microcontroller Gen1) is a family of high-voltage USB-C Power Delivery (PD) microcontrollers (MCU). These chips include an Arm® Cortex®-M0/M0+ CPU and USB-C PD controller along with analog and digital peripherals. EZ-PD™ PMG1 is targeted for any embedded system that provides/consumes powers to/from a high-voltage USB-C PD port and leverages the microcontroller to provide additional control capability. **Figure 1** shows the EZ-PD™ PMG1 family segmentation.

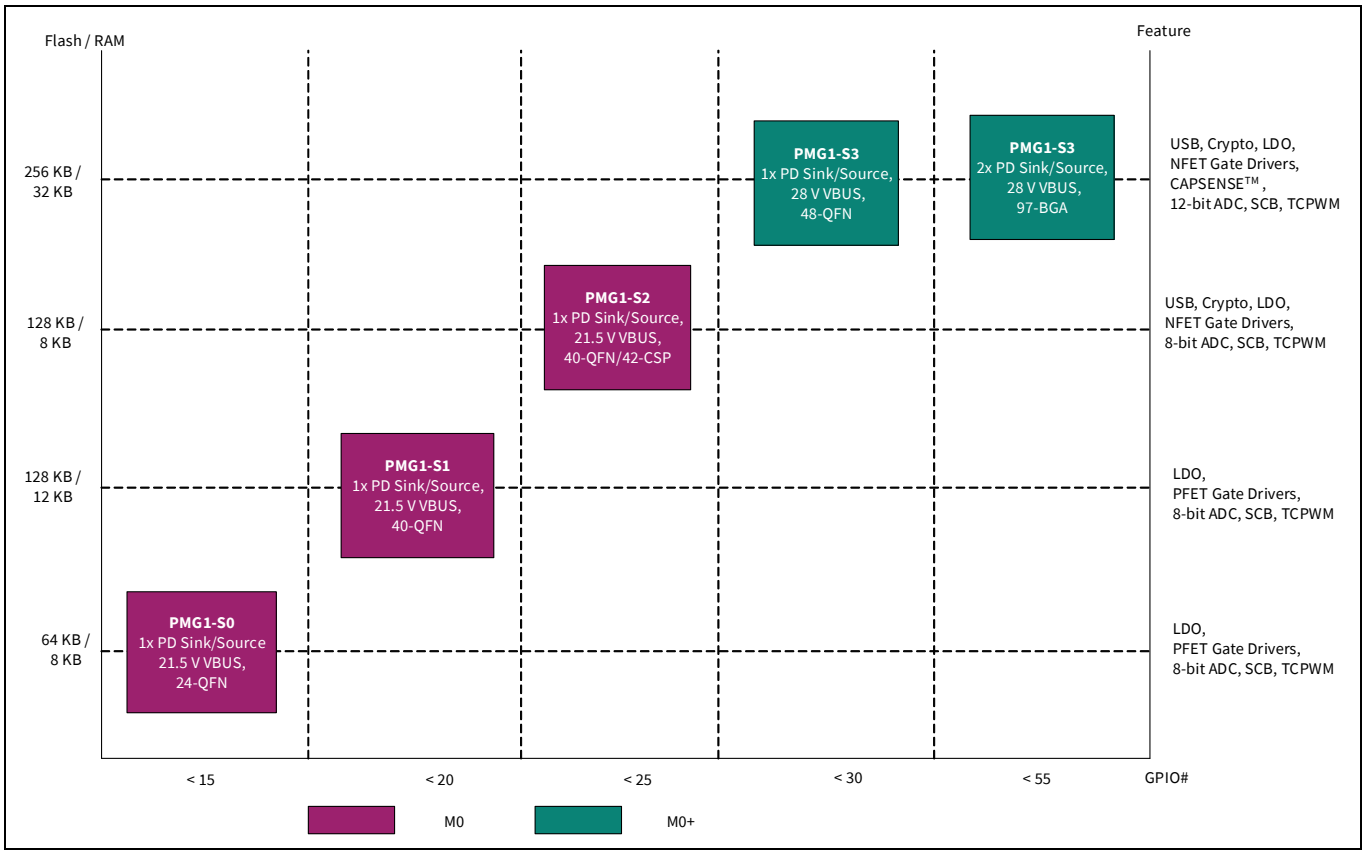


Figure 1 PMG1 family segmentation

Table 1 shows the comparison of features of different MCUs of the EZ-PD™ PMG1 family.

Table 1 Comparison of features of different MCUs of the EZ-PD™ PMG1 family

Subsystem or range	Item	PMG1-S0	PMG1-S1	PMG1-S2	PMG1-S3
CPU and Memory Sub-system	Core	Arm® Cortex®-M0	Arm® Cortex®-M0	Arm® Cortex®-M0	Arm® Cortex®-M0+
	Max. freq (MHz)	48	48	48	48
	Flash (KB)	64	128	128	256
	SRAM (KB)	8	12	8	32
Power delivery	Power delivery Ports	1	1	1	1 port for 48-QFN 2 ports for 97-BGA
	Role	DRP	DRP	DRP	DRP
	MOSFET gate drivers	2x PFET	2x PFET	2x NFET	Flexible 2x NFET
	Fault protections	VBUS OVP, UVP, and OCP. SCP (for source configuration only)	VBUS OVP, UVP, and OCP. SCP and RCP (for Source Configuration only)	VBUS, OVP, UVP, and OCP	VBUS OVP, UVP, and OCP. SCP and RCP (for Source Configuration only).
USB	Integrated full speed USB 2.0 Device with Billboard class support	No	No	Yes	Yes
Voltage Range	Supply (V)	VDDD (2.7–5.5) VBUS (4–21.5)	VSYS (2.75–5.5) VBUS (4– 21.5)	VSYS (2.7–5.5) VBUS (4–21.5)	VSYS (2.8–5.5) VBUS (4–28)
	IO (V)	1.71 - 5.5	1.71 - 5.5	1.71 - 5.5	1.71 - 5.5
Digital	SCB (configurable as I^2C/UART/SPI)	2	4	4	7 for 48-QFN (out of which only 5 can be configured as SPI and UART) 8 for 97-BGA
	TCPWM Block (configurable as timer, counter or pulse-width modulator)	4	2	4	8
	Hardware authentication block (Crypto)	No	No	Yes (AES-128/192/256, SHA1, SHA2-224, SHA2-256, PRNG, CRC)	Yes (AES-128, SHA2-256, TRNG, vector unit)

Table 1 Comparison of features of different MCUs of the EZ-PD™ PMG1 family *(continued)*

Subsystem or range	Item	PMG1-S0	PMG1-S1	PMG1-S2	PMG1-S3
Analog	ADC	2x 8-bit SAR	1x 8-bit SAR	2x 8-bit SAR	2x 8-bit SAR 1x 12-bit SAR
	On-chip Temperature Sensor	Yes	Yes	Yes	Yes
Direct memory access (DMA)	DMA	No	No	No	Yes
GPIO	Max # of I/Os	12 (10 + 2 Fail-safe)	17 (15 + 2 Fail-safe)	20 (18 + 2 Fail-safe)	26 (24 + 2 Fail-safe) for 48-QFN 50 (48 + 2 Fail-safe) for 97-BGA
Charging Standards	Charging source	BC 1.2, AC, AFC and QC 3.0	BC 1.2, AC	BC 1.2, AC	BC 1.2, AC, AFC, and QC 3.0
	Charging sink	BC 1.2, AC and QC 2.0	BC 1.2, AC	BC 1.2, AC	BC 1.2, AC and QC 2.0
ESD protection	ESD protection	Yes (Human body model and charged device model)	Yes (Human body model and charged device model)	Yes (Human body model and charged device model)	Yes (Human body model and charged device model)
Packages	Package options	24-QFN (4 × 4 mm, 0.5 mm pitch)	40-QFN (6 × 6 mm, 0.5 mm pitch)	40-QFN (6 × 6 mm, 0.5 mm pitch) 42-CSP (2.63 × 3.18 mm, 0.4 mm pitch)	48-QFN (6 × 6 mm, 0.5 mm pitch) 97-BGA (6 × 6 mm, 0.5 mm and 0.65 mm pitch)

The rest of the document discusses the EZ-PD™ PMG1-S0 device in detail.

EZ-PD™ PMG1-S0 general description

EZ-PD™ PMG1-S0 marks the beginning of PMG1 family with 64 KB flash, 8 KB SRAM, 12 GPIOs, a complete Type-C USB PD transceiver with all termination resistors RP, RD and can be used in dual-role power (DRP) applications. It is available in 24-lead QFN package.

Applications

- Smart speakers, portable electronics, power banks
- Battery powered applications
- Cordless power tools
- Home appliances such as vacuum cleaners
- Electric bikes, robots, and drones

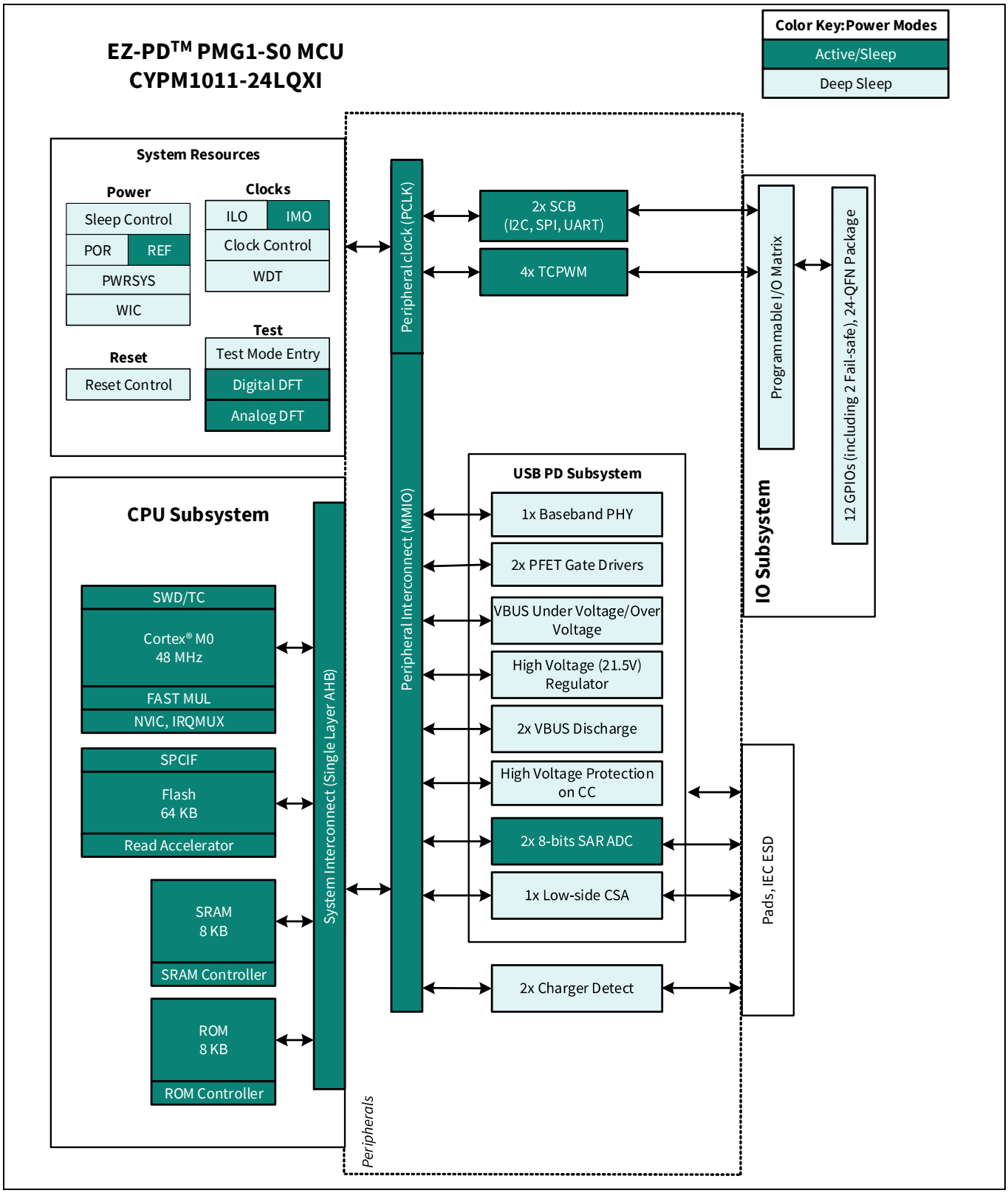
Features

- **32-bit MCU subsystem**
- **48-MHz Arm® Cortex®-M0 CPU**
- **Memory**
  - 64-KB Flash
  - 8-KB SRAM
  - 8-KB SROM
- **Type-C/PD blocks**
  - USB-IF certified (TID: 7915)
  - Integrated USB power-delivery (USB PD) 3.2 support
  - Termination resistor Rd and Rp
  - Supports one USB Type-C port and one Type-A port
- **Legacy charging (source and sink)**
- **System-level fault protection**
  - VBUS to CC short protection
  - Low-side current sense amplifier (CSA) for overcurrent protection (OCP) and short circuit protection (SCP)
- **Liquid detection and corrosion mitigation**
  - Supports moisture/liquid detection on Type-C connector
  - Integrated liquid detection blocks
  - Implements Corrosion Mitigation mode
- **Clocks and oscillators**
  - Integrated oscillator eliminating the need for external clock
- **Power**
  - VDDD (2.7 V–5.5 V)
  - VBUS (4.0 V–21.5 V)
- **System-Level ESD protection**
  - On CC, VBUS_MON, USBDP, USBDM, P2.2, and P2.3 pins
  - ± 8-kV contact discharge and ±15-kV air gap discharge based on IEC61000-4-2 level 4C
- **Packages**
  - 24-pin QFN
  - Supports extended industrial temperature range (–40°C to +105°C)

Block diagram

- **Software tool**
  - ModusToolbox™

Block diagram



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1 Development support

The EZ-PD™ PMG1 family has a rich set of documentation, development tools, and online resources to assist you during your development process. Visit **USB-C High Voltage Microcontrollers**.

1.1 Documentation

A suite of documentation supports the EZ-PD™ PMG1 family to ensure that you can find answers to your questions quickly. This section contains a list of some of the key documents.

ModusToolbox™ tools package user guide: A step-by-step guide for using ModusToolbox™ (MTB). The software user guide shows you how MTB build process works in detail, how to use source control with MTB, and much more.

Component datasheets: The flexibility of EZ-PD™ PMG1 allows the creation of new peripherals (components) long after the device has gone into production. Component data sheets provide all the information needed to select and use a particular component, including functional description, API documentation, example codes, and AC/DC specifications.

Application notes: This includes the Getting Started application note and the hardware design guidelines.

Reference manual: The reference manual contains all the technical detail you need to use EZ-PD™ PMG1 device, including a complete description of all EZ-PD™ PMG1 registers. The reference manual is available in the Documentation section at **USB-C High Voltage Microcontrollers**.

1.2 Online

In addition to print documentation, the **EZ-PD™ PMG1 forums** connect you with fellow users and experts in PMG1 from around the world, 24 hours a day, 7 days a week.

1.3 Tools

With industry standard cores, programming, and debugging interfaces, the EZ-PD™ PMG1 MCU family is part of a development tool ecosystem.

Visit us at **ModusToolbox™ software** for the latest information on the revolutionary, easy to use ModusToolbox™ IDE, supported third party compilers, programmers, debuggers, and development kits.

1.4 ModusToolbox™ IDE and the EZ-PD™ PMG1 SDK

ModusToolbox™ is an Eclipse-based development environment on Windows, macOS, and Linux platforms that includes the ModusToolbox™ IDE and the EZ-PD™ PMG1 SDK. The ModusToolbox™ IDE brings together several device resources, middleware, and firmware to build an application. Using ModusToolbox™, you can enable and configure device resources and middleware libraries, write C/C++/assembly source code, and program and debug the device.

The PMG1 SDK is the software development kit for the EZ-PD™ PMG1 MCU. The SDK makes it easier to develop firmware for supported devices without the need to understand the intricacies of the device resources.

For additional details on using the ModusToolbox™, see **Getting started with EZ-PD™ PMG1 MCU on ModusToolbox™ software** application note and the documentation and the help integrated into ModusToolbox™.

2 Functional overview

2.1 CPU and memory sub-system

2.1.1 CPU

The heart of the EZ-PD™ PMG1-S0 MCU is a 32-bit Cortex®-M0 CPU core running up to 48 MHz. It is optimized for low-power operation with extensive clock gating.

The CPU also includes a serial wire debug (SWD) interface. The debug configuration used for EZ-PD™ PMG1-S0 has four break-point (address) comparators and two watchpoint (data) comparators.

2.1.2 Flash

The EZ-PD™ PMG1-S0 device has a 64-KB flash module.

2.1.3 SRAM

EZ-PD™ PMG1-S0 supports 8-KB SRAM.

2.1.4 SROM (Supervisory ROM)

A supervisory ROM that contains boot and configuration routines is provided. 8-KB SROM.

2.2 USB PD subsystem (SS)

The USB PD subsystem provides the interface to the USB Type-C port. This subsystem comprises a high-voltage regulator, OVP, and supply switch blocks. This subsystem also includes all ESD required and supported on the Type-C port.

2.2.1 USB PD physical layer

The USB PD physical layer consists of a transmitter and receiver that communicate BMC-encoded data over the CC channel based on the PD 3.1 standard. All communication is half-duplex. The Physical Layer or PHY practices collision avoidance to minimize communication errors on the channel.

The USBPD block includes all termination resistors (Rp, Rd and Rd-db) and switch as required by the USB Type-C spec. The termination resistor is required to implement connection detection, plug orientation detection, and for establishing the sink/source power role. A dead-battery R_D termination enables identification as a sink while the EZ-PD™ PMG1-S0 device is not powered.

2.2.2 8-bit SAR ADC

The ADC is a low-footprint 8-bit 125 ksps SAR ADC that is available for general-purpose A-D conversion applications in the chip. This ADC can be accessed from all GPIOs and the USB DP/DM pins through an on-chip analog mux. EZ-PD™ PMG1-S0 contains two instances of the ADC. The voltage reference for the ADCs is generated either from the VDDD supply or from internal bandgap. When sensing the GPIO pin voltage with an ADC, the pin voltage cannot exceed the VDDD supply value.

2.2.3 Charger detection

As source supports - BC 1.2, Apple charging, AFC, and QC 3.0 and as Sink supports - BC 1.2, AC, and QC 2.0. Integrates all required terminations on USB DP/DM lines.

There are two charger detect blocks integrated in the device. The USB lines USBDP0 and USBDM0 are connected to charger detect 0 block, whereas USBDP1 and USBDM1 are connected to charger detect 1 block. The two charger detect blocks help in enabling charging through two different USB ports, a Type-C port and Type-A port.

2.2.4 VBUS UVP and OVP

The EZ-PD™ PMG1-S0 chip has an integrated hardware block for VBUS OVP/UVP with configurable thresholds and response times on the Type C port.

2.2.5 VBUS short protection

EZ-PD™ PMG1-S0 provides four VBUS short protection pins: CC1, CC2, P2.2, and P2.3. These pins are protected from accidental shorts to high-voltage VBUS. Accidental shorts may occur because the CC1 and CC2 pins are placed next to the VBUS pins in the USB Type-C connector. A Power Delivery controller without the high-voltage VBUS short protection will be damaged in the event of accidental shorts. When the protection circuit is triggered, EZ-PD™ PMG1-S0 can handle up to 17 V forever and between 17 V to 22 VDC for 1000 hours on the fail-safe pins. When a VBUS short event occurs on the CC pins, a temporary high-ringing voltage is observed due to the RLC elements in the USB Type-C cable. Without EZ-PD™ PMG1-S0 connected, this ringing voltage can be twice (44 V) the maximum VBUS voltage (21.5 V). However, when EZ-PD™ PMG1-S0 is connected, it is capable of clamping temporary high-ringing voltage and protecting the CC pin using IEC ESD protection diodes.

2.2.6 Low-side current sense amplifier (CSA)

EZ-PD™ PMG1-S0 chip also has an integrated low-side current sense amplifier that is capable of detecting current levels ranging from 100 mA to 5.5 A across a 5 mΩ external resistor, which can be used to implement overcurrent protection (OCP).

2.2.7 PFET gate drivers on VBUS path

EZ-PD™ PMG1-S0 has two integrated PFET gate drivers to drive external PFETs on the VBUS consumer paths. The VBUS_P_CTRL gate driver has an active pull-up, and thus can drive high, low or High-Z.

The VBUS_C_CTRL gate driver can drive only low or high-Z, thus requiring an external pull-up. These pins are VBUS voltage-tolerant.

2.2.8 VBUS discharge FETs

EZ-PD™ PMG1-S0 also has two integrated VBUS discharge FETs used to discharge VBUS to meet the USB PD specification timing on a detach condition.

2.2.9 Liquid Corrosion Mitigation on Type-C connector

EZ-PD™ PMG1-S0 supports moisture/liquid detection on the Type-C connector and enters into Corrosion Mitigation mode to minimize the possibility of corrosion on Type-C connector, according to the latest Type-C specifications. The device uses the integrated charger detect block with an unused pair of pins in the Type-C connector to detect the presence of moisture. The charger detect block applies a set of internal pull-up and pull-down resistors on the connected pair of lines. An internal comparator monitors the change in voltage on the particular Type-C connector pins, triggering an output that indicates the presence of liquid. Corrosion Mitigation mode is achieved using the single CC line pull-down method as shown in **Figure 2**, according to the Type-C specification.

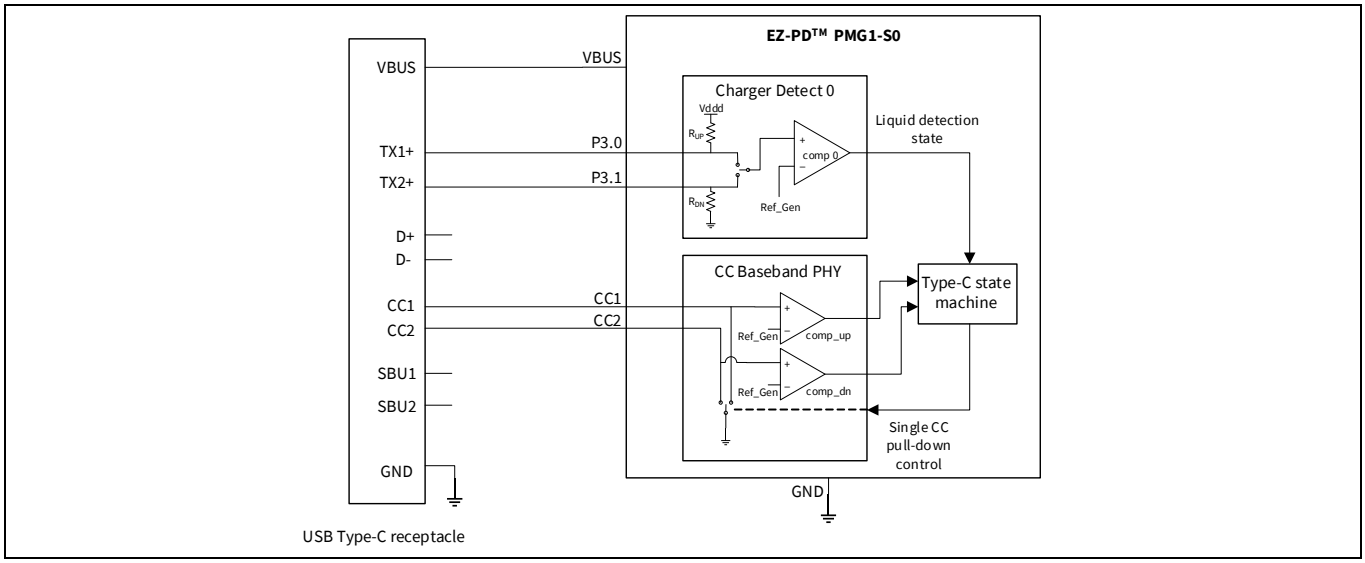


Figure 2 Block diagram for liquid detection and corrosion mitigation

2.3 Fixed-function digital

2.3.1 Serial communication blocks (SCB)

EZ-PD™ PMG1-S0 has two SCBs, which can be configured to implement an I^2C, SPI, or UART interface. The hardware I^2C blocks implement full multi-master and slave interfaces capable of multimaster arbitration. In the SPI mode, the SCB blocks can be configured to act as master or slave.

I^2C mode: I^2C is compatible with the standard Philips I^2C specification v3.0. These blocks operate at speeds of up to 1 Mbps and have flexible buffering options to reduce interrupt overhead and latency for the CPU. The SCB blocks support 8-deep FIFOs for Receive (RX) and Transmit (TX), which, by increasing the time given for the CPU to read data, greatly reduces the need for clock stretching caused by the CPU not having read data on time. Data throughput is not a critical consideration for I^2C.

UART mode: This is a full-featured UART operating at speeds of up to 1 Mbps. In addition, it supports the 9-bit multi-processor mode which allows address of peripherals connected over common RX and TX lines. Common UART functions such as parity error, break detect, and frame error are supported.

SPI mode: The SPI mode supports full Motorola SPI as well as TI SSP (essentially adds a start pulse used to synchronize SPI Codecs), and National Microwire (half-duplex form of SPI) variants. The SPI block can also utilize the FIFO.

2.3.2 Timer/counter/PWM block (TCPWM)

EZ-PD™ PMG1-S0 has four TCPWM blocks. Each implements a 16-bit timer, counter, pulse-width modulator (PWM), and quadrature decoder functionality. The block can be used to measure the period and pulse width of an input signal (timer), find the number of times a particular event occurs (counter), generate PWM signals, or decode quadrature signals.

2.3.3 GPIO interface

EZ-PD™ PMG1-S0 has up to 12 GPIOs of which, some of them can be re-purposed to support functions of SCB (I^2C, UART, SPI). GPIO pins P0.0 and P0.1 are fail-safe pins (up to 6 V).

The GPIO block implements the following:

- Eight drive strength modes including strong push-pull, resistive pull-up and pull-down, weak (resistive) pull-up and pull-down, open drain and open source, input only, and disabled.
- Input threshold select (CMOS or LVTTL)
- Individual control of input and output disables.
- Hold mode for latching previous state (used for retaining I/O state in Deep Sleep mode).
- Selectable slew rates for dV/dt related noise control.

During power-on and reset, the I/O pins are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix is used to multiplex between various signals that may connect to an I/O pin.

Port pins P1.0 and P1.1 can be configured to indicate fault for OVP/UVP conditions.

2.3.4 Fail-Safe GPIOs

EZ-PD™ PMG1-S0 has two pins which are fail-safe GPIOs. These are P0.0 and P0.1.

The fail-safe feature ensures that, in the absence of VBUS/VSYS power, a logic high level on these pins due to I^2C line activity will not back-power the MCU.

3 Power systems overview

EZ-PD™ PMG1-S0 can operate from two possible external supply sources: VBUS (4.0 V–21.5 V) or VDDD (2.7 V–5.5 V). When powered through VBUS, the internal regulator generates VDDD of 3.3 V for chip operation. The regulated supply, VDDD, is either used directly inside some analog blocks or further regulated down to VCCD (1.8 V), which powers majority of the core using the regulators. EZ-PD™ PMG1-S0 has three different power modes: Active, Sleep, and Deep Sleep. Transitions between these power modes are managed by the power system. When powered through the VBUS pin, VDDD cannot be used to power external devices and should be connected to a 1-µF capacitor for the regulator stability only. These pins are not supported as power supplies. Refer to the application diagrams for capacitor connections.

Table 2 EZ-PD™ PMG1-S0 power modes

Mode	Description
Power-on Reset (POR)	Power is valid and an internal reset source is asserted or SleepController is sequencing the system out of reset.
ACTIVE	Power is valid and CPU is executing instructions.
SLEEP	Power is valid and CPU is not executing instructions. All logic that is not operating is clock gated to save power.
DEEP SLEEP	Main regulator and most blocks are shut off. DeepSleep regulator powers logic, but only low-frequency clock is available.

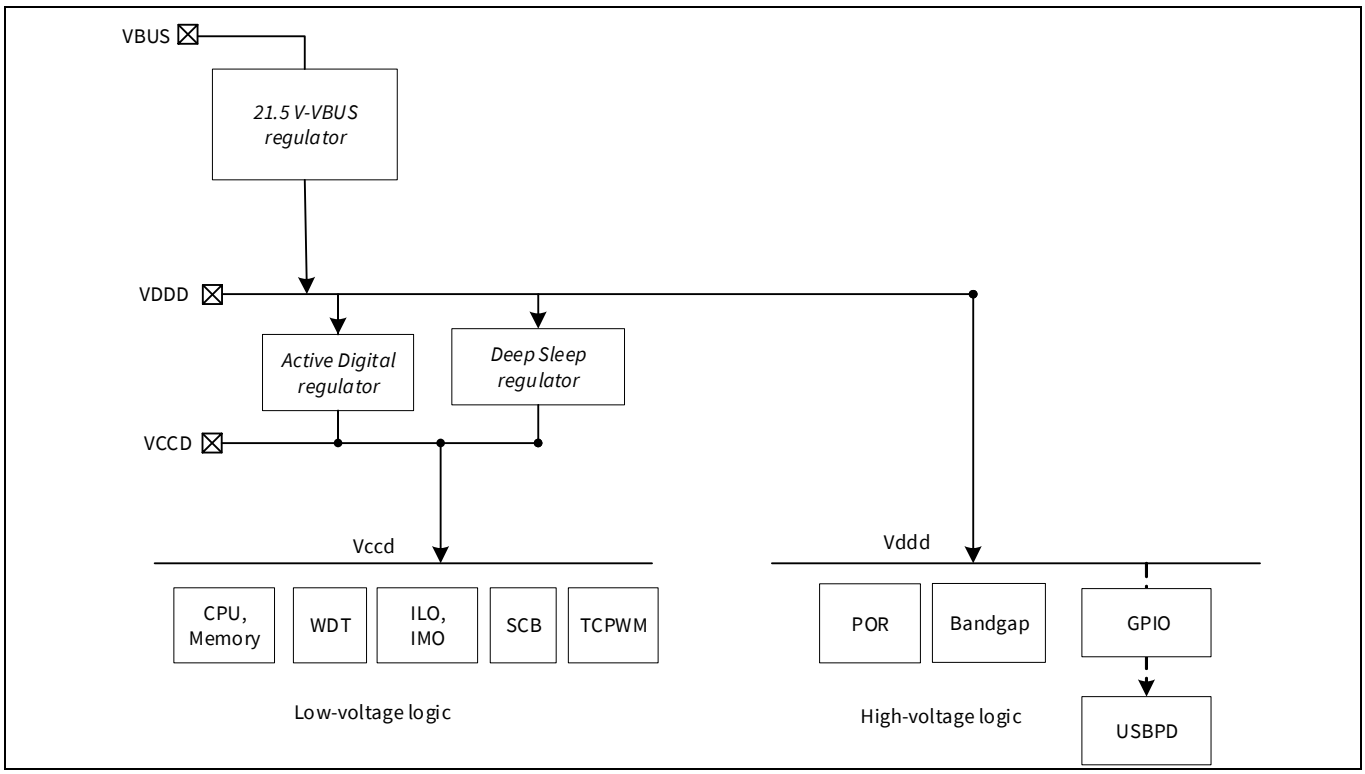


Figure 3 Power system requirement block diagram

4 Pinouts

Table 3 EZ-PD™ PMG1-S0 pin descriptions

Group	24-pin QFN	Pin name	ACT #0	ACT #1	ACT #2	ACT #3	DS #1	DS #2	DS #3	Description
GPIOs and serial interface	1	P1.0	–	tcpwm2_line	tcpwm0_overflow	scb1_uart_cts	–	scb0_spi_select	scb1_i2c_sda	Port 1 pin 0: GPIO/UART_1_CTS/SPI_0_SEL/I2C_1_SDA/ TCPWM_line_2, Programmable OVP/UVP Fault indication
	2	P1.1	tcpwmx_tr_in0	tcpwm3_line	tcpwm1_overflow	scb1_uart_rts	–	scb0_spi_miso	scb1_i2c_scl	Port 1 pin 1: GPIO/UART_1_RTS/SPI_0_MISO/I2C_1_SCL/ TCPWM_line_3, Programmable OVP/UVP Fault indication
	5	P1.2	–	–	tcpwm2_overflow	scb1_uart_tx	–	scb0_spi_mosi	–	Port 1 pin 2: GPIO/USB D+ line 1/UART_1_TX1/SPI_0_MOSI/ BC 1.2/Apple Charging/QC/AFC
	6	P1.3	–	–	tcpwm3_overflow	scb1_uart_rx	–	scb0_spi_clk	–	Port 1 pin 3: GPIO/USB D- line 1/UART_1_RX1/SPI_0_CLK/ BC 1.2/Apple Charging/QC/AFC
	7	P0.0	tcpwmx_tr_in1	tcpwm0_line	tcpwm0_compare_match	scb0_uart_cts	swd_data	scb1_spi_mosi	scb0_.i2c_sda	Port 0 pin 0: GPIO/fail-safe/SWD_IO/UART_0_CTS/SPI_1_MOSI/I2C_0_SD A/TCPWM_line_0
	8	P0.1	tcpwmx_tr_in2	tcpwm1_line	tcpwm1_compare_match	scb0_uart_rts	swd_clk	scb1_spi_miso	scb0_i2c_scl	Port 0 pin 1: GPIO/fail-safe/SWD_CLK/UART_0_RTS/SPI_1_MISO/I2C_0_S CL/TCPWM_line_1
	9	P2.0	tcpwmx_tr_in3	tcpwm2_line(alt)	tcpwm2_compare_match	scb0_uart_tx	–	scb1_spi_select	–	Port 2 pin 0: GPIO/TCPWM_line_2/UART_0_TX0/SPI_1_SEL This pin is internally pulled up during the Power-On I/O initialization time (see **Table 7** for more details). Also, this is an output only pin that can be used in open drain mode of operation only.
	10	P2.1	tcpwmx_tr_in4	tcpwm3_line(alt)	tcpwm3_compare_match	scb0_uart_rx	–	scb1_spi_clk	–	Port 2 pin 1: GPIO/TCPWM_line_3/UART_0_RX0/SPI_1_CLK
	12	P2.2	tcpwmx_tr_in5	tcpwm0_line(alt)	–	scb0_uart_tx(alt)	swd_data(alt)	–	scb1_i2c_sda(alt)	Port 2 pin 2: GPIO with Open drain with pull-up assist. Config- urable as GPIO_20VT/ UART_0_TX1/ I2C_1_SDA/TCPWM_line_0/IEC. Tolerant to temporary short to VBUS pin.
	13	P2.3	tcpwmx_tr_in6	tcpwm1_line(alt)	–	scb0_uart_rx(alt)	swd_clk(alt)	–	scb1_i2c_scl(alt)	Port 2 pin 3: GPIO with Open drain with pull-up assist. Config- urable as GPIO_20VT/ UART_0_RX1/ I2C_1_SCL/TCPWM_line_1/IEC. Tolerant to temporary short to VBUS pin.
	17	P3.0	–	ext_clk	–	scb1_uart_tx(alt)	swd_data(alt)	–	–	USB DP line 0/Port 3 pin 0: GPIO/UART_1_TX0/BC 1.2/Apple Charging/QC/AFC/IEC/pin for liquid detection on Type-C connector
	16	P3.1	–	–	–	scb1_uart_rx(alt)	swd_clk(alt)	–	–	USB DM line 0/Port 3 pin 1: GPIO/UART_1_RX0/BC 1.2/Apple Charging/QC/AFC/IEC/pin for liquid detection on Type-C connector
USB Type-C	14	CC2	–	–	–	–	–	–	–	Communication Channel 2 with Dead-battery R_D Bonding Option/IEC. Tolerant to temporary short to VBUS pin.
	15	CC1	–	–	–	–	–	–	–	Communication Channel 1 with Dead-battery R_D Bonding Option/IEC. Tolerant to temporary short to VBUS pin.
VBUS	3	VBUS_P_CTRL	–	–	–	–	–	–	–	External PMOS FET control (30-V Tolerant) with internal pull-up 0: Path ON 1: Path OFF
	4	VBUS_C_CTRL	–	–	–	–	–	–	–	External PMOS FET Control (30-V Tolerant) 0: Path ON Z: Path OFF To use this pin, provide external pull-up
	11	VBUS_MON	–	–	–	–	–	–	–	Type C VBUS Monitor with Internal Discharge FET

Table 3 EZ-PD™ PMG1-S0 pin descriptions *(continued)*

Group	24-pin QFN	Pin name	ACT #0	ACT #1	ACT #2	ACT #3	DS #1	DS #2	DS #3	Description
Power	18	VBUS	–	–	–	–	–	–	–	VBUS Power IN (4.0 V–21.5 V) with Internal Discharge FET
	23	VDDD	–	–	–	–	–	–	–	Output of internal 3.3-V regulator. Connect 1 µF and 2x 100 nF capacitors.
	24	VCCD	–	–	–	–	–	–	–	Output of internal 1.8-V regulator (not intended for use as a power source). Connect a 1 µF decoupling capacitor.
GND	19	CSP	–	–	–	–	–	–	–	Current Sense Positive input for low-side CSA
	22	GND	–	–	–	–	–	–	–	Ground
	EPAD	GND	–	–	–	–	–	–	–	Ground
NC	20	NC	–	–	–	–	–	–	–	Not connected
	21	NC	–	–	–	–	–	–	–	Not connected

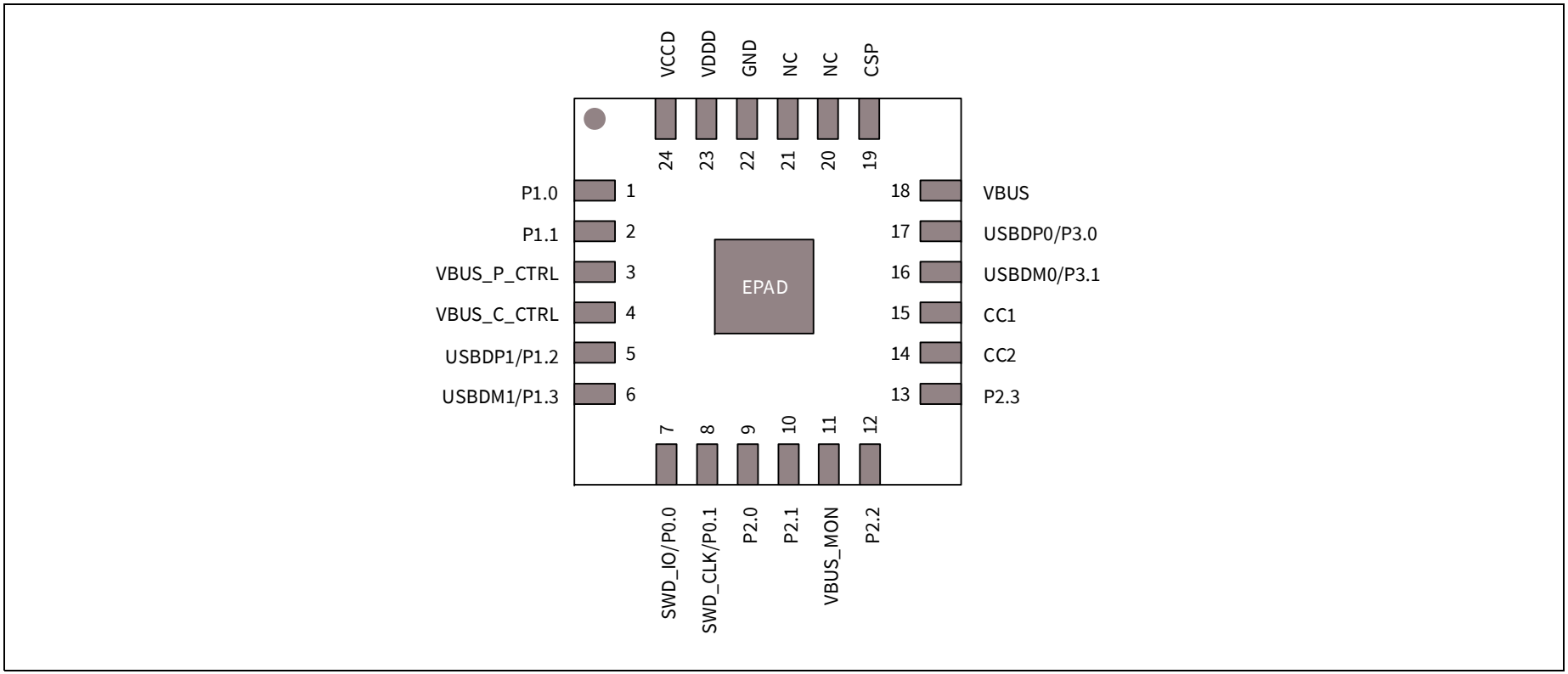


Figure 4 Pinout of 24-QFN package (top view)

5 Application diagram

Figure 5 illustrates the Sink application using EZ-PD™ PMG1-S0. It has two main parts: USB Type-C receptacle to provide the input power to the application and load used as the output power.

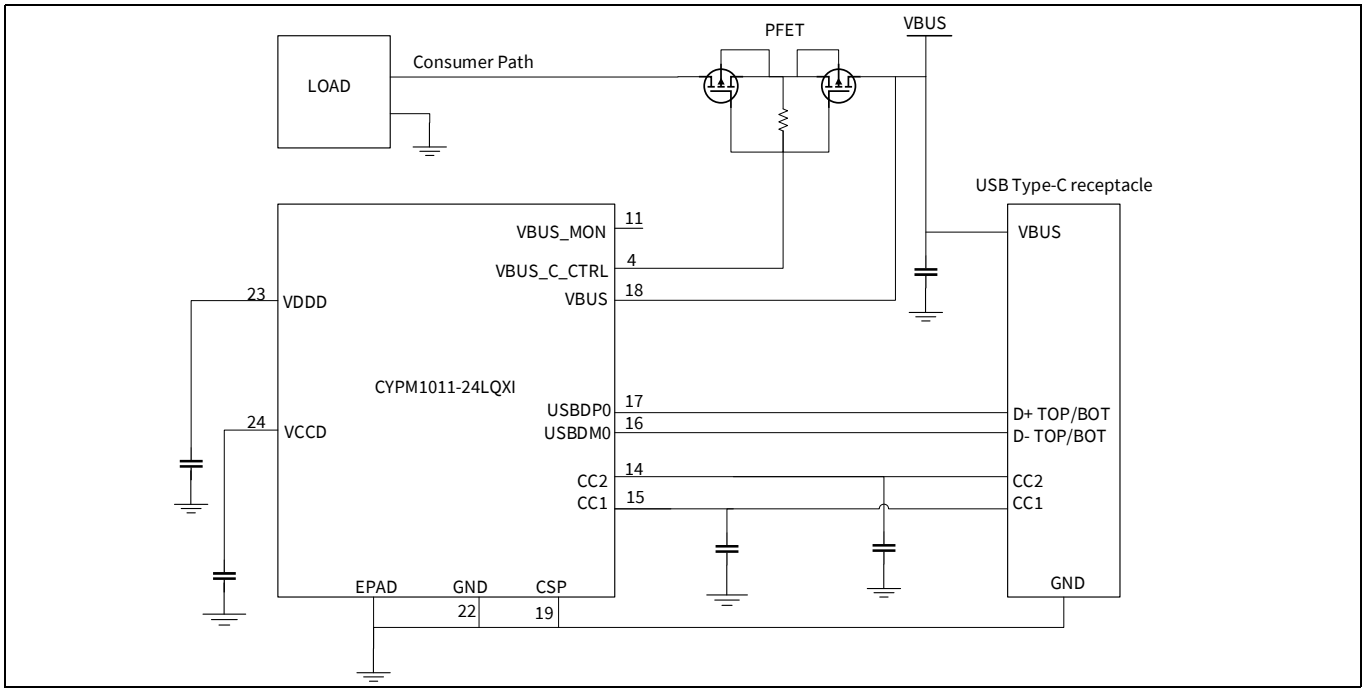


Figure 5 EZ-PD™ PMG1-S0 based sink application diagram

Figure 6 illustrates a DRP application using EZ-PD™ PMG1-S0. In such applications, the Type-C port is used as a power provider and a power consumer.

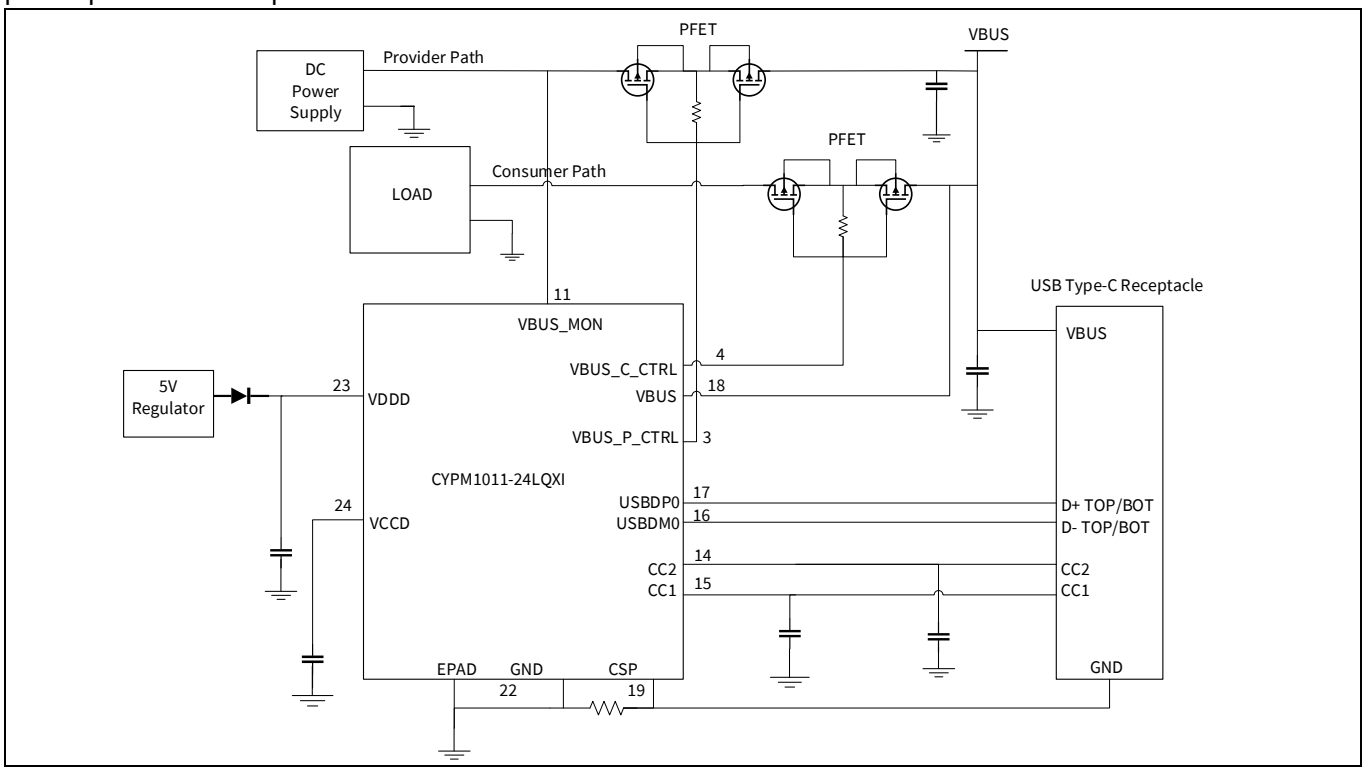


Figure 6 EZ-PD™ PMG1-S0 DRP application diagram

6 Electrical specifications

6.1 Absolute maximum ratings

Table 4 Absolute maximum ratings[1]

Parameter	Description	Min	Typ	Max	Units	Details/conditions
V_{BUS_MAX}	Max supply voltage relative to V_{SS} on VBUS and VBUS_MON pins	–	–	30	V[2]	Absolute max. Voltage of P2.2 and P2.3 (GPIO_20VT pins)
V_{DDD_MAX}	Max supply voltage relative to V_{SS}	–	–	6	V	
$V_{CC\_PIN\_ABS}$	Max voltage on CC1, CC2 pins and port pins P2.2 and P2.3 for applicable devices	–	–	22[3]	V	
V_{GPIO_ABS}	GPIO voltage	–0.5[4]	–	V_{DDD} +0.5	V	
I_{GPIO_ABS}	Maximum current per GPIO	–25	–	25	mA	
$I_{GPIO\_injection}$	GPIO injection current, Max for $V_{IH} > V_{DDD}$, and Min for $V_{IL} < V_{SS}$	–0.5	–	0.5	mA	Absolute max, current injected per pin
$V_{GPIO\_fail\text{-}safe\_ABS}$	Fail-safe GPIO voltage	–0.5	–	6	V	Applicable to port pins P0.0 and P0.1
ESD_HBM	Electrostatic discharge human body model (ESD-HBM)	2200	–	–	V	–
ESD_CDM	Electrostatic discharge charged device model (ESD-CDM)	500	–	–	V	–
LU	Pin current for latch-up	–100	–	100	mA	–
ESD_IEC_CON	Electrostatic discharge IEC61000-4-2	8000	–	–	V	Contact discharge on CC1, CC2, VBUS, P2.2 and P2.3 pins
ESD_IEC_AIR	Electrostatic discharge IEC61000-4-2	15000	–	–	V	Air discharge for USBDP, USBDM, CC1, CC2, VBUS, P2.2 and P2.3 pins

Notes

1. Usage above the absolute maximum conditions listed in **Table 4** may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods of time may affect device reliability. The maximum storage temperature is 150°C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When used below absolute maximum conditions but above normal operating conditions, the device may not operate to specification.
2. All voltages are relative to Ground unless otherwise specified.
3. As per USB PD specification, maximum allowed VBUS = 21.5 V.
4. In a system, if the negative spike exceeds the minimum voltage specified here, it is recommended to add Schottky diode to clamp the negative spike.

6.2 Pin based absolute maximum ratings

Table 5 Pin based absolute maximum ratings

S. No.	Pin (24 QFN)	Name	Absolute minimum (V)	Absolute maximum (V)	Remarks
1	1	P1.0	-0.5	6	Maximum voltage cannot exceed VDDD + 0.5
2	2	P1.1	-0.5	6	Maximum voltage cannot exceed VDDD + 0.5
3	5	P1.2	-0.5	6	Maximum voltage cannot exceed VDDD + 0.5
4	6	P1.3	-0.5	6	Maximum voltage cannot exceed VDDD + 0.5
5	7	P0.0	-0.5	6	Maximum voltage cannot exceed VDDD + 0.5
6	8	P0.1	-0.5	6	Maximum voltage cannot exceed VDDD + 0.5
7	9	P2.0	-0.5	6	Maximum voltage cannot exceed VDDD + 0.5
8	10	P2.1	-0.5	6	Maximum voltage cannot exceed VDDD + 0.5
9	12	P2.2	-0.5	22	–
10	13	P2.3	-0.5	22	–
11	16	P3.1	-0.5	6	Maximum voltage cannot exceed VDDD + 0.5
12	17	P3.0	-0.5	6	Maximum voltage cannot exceed VDDD + 0.5
13	14	CC2	-0.5	22	–
14	15	CC1	-0.5	22	–
15	3	VBUS_P_CTRL	-0.5	30	This is an output only pin
16	4	VBUS_C_CTRL	-0.5	30	This is an output only pin
17	11	VBUS_MON	–	30	–
18	18	VBUS	–	30	–
19	23	VDDD	–	6	–
20	24	VCCD	–	1.95	This is an output only pin
21	19	CSP	-0.5	6	Maximum voltage cannot exceed VDDD + 0.5
22	22	GND	–	–	–
23	EPAD	GND	–	–	–
24	20	NC	–	–	–
25	21	NC	–	–	–

6.3 Device-level specifications

All specifications are valid for –40°C ≤ T_A ≤ 105°C and T_J ≤ 120°C, except where noted.

Table 6 DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.PWR#1	V_{DDD}	Regulated output voltage when VSYS powered (not to be driven externally)	VSYS – 0.05	–	VSYS	V	-40°C to +85°C TA.
SID.PWR#2	V_{DDD}	Power supply input voltage	2.7	–	5.5	V	Sink mode, –40°C ≤ T_A ≤ 105°C.
SID.PWR#2_A	V_{DDD}	Power supply input voltage	3	–	5.5	V	Source mode, –40°C ≤ T_A ≤ 105°C.
SID.PWR#3	V_{BUS_IN}	Power supply input voltage	3	–	21.5	V	–40°C ≤ T_A ≤ 105°C.

Table 6 DC specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.PWR#5	V_{CCD}	Output voltage for core logic	–	1.8	–	V	–
SID.PWR#13	C_{exc}	Power supply decoupling capacitor for V_{DDD}	0.8	1	–	µF	X5R ceramic or better
SID.PWR#14	C_{exv}	Power supply decoupling capacitor for VBUS	–	0.1	–	µF	X5R ceramic or better
Active Mode. Typical values measured at V_{DDD} = 5.0 V or V_{BUS} = 5.0 V and T_A = 25°C.							
SID.PWR#8	I_{DD_A}	Supply current from V_{BUS} or V_{DDD}	–	10	–	mA	V_{DDD} = 5 V OR V_{BUS} = 5 V, T_A = 25°C. CC1/CC2 in Tx or Rx, no I/O sourcing current, 2 SCBs at 1 Mbps, ADC/UVOV ON, CPU at 24 MHz.
Sleep Mode. Typical values measured at V_{DD} = 3.3 V and T_A = 25°C.							
SID25A	I_{DD_S}	CC, I^2C, WDT wakeup on. IMO at 24 MHz.	–	3	–	mA	V_{DDD} = 3.3 V, T_A = 25°C, All blocks except CPU are on, CC IO on, ADC/UVOV On.
Deep Sleep Mode. Typical values measured at T_A = 25°C.							
SID_DS_A_SNK	$I_{DD\_PB\_DS\_A\_SNK}$	V_{BUS} = 4.0 to 21.5 V. CC, I^2C, WDT Wakeup on	–	500	–	µA	Power sink application V_{BUS} = 21.5 V, T_A = 25°C, Part is in deep sleep. Attached, CC I/O on, ADC/UVOV On.
SID_PB_DS_A_SRC	$I_{DD\_PB\_DS\_A\_SRC}$	V_{DDD} = 3.0 to 5.5 V. CC, I^2C, WDT Wakeup on	–	500	–	µA	Power bank source application V_{DDD} = 5 V, T_A = 25°C, Part is in deep sleep. Attached, CC I/O on, ADC/CSA/UVOV On.

Table 7 AC specifications

(guaranteed by characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/ conditions
SID.CLK#4	F_{CPU}	CPU input frequency	–	–	48	MHz	All V_{DDD}
SID.PWR#17	T_{SLEEP}	Wakeup from sleep mode	–	0	–	µs	–
SID.PWR#18	$T_{DEEPSLEEP}$	Wakeup from Deep Sleep mode	–	–	35	µs	–
SYS.FES#1	$T_{\_PWR\_RDY}$	Power-up to “Ready to accept I^2C/CC command”	–	5	25	ms	–
SID.PWR#18A	$T_{POR\_HIZ\_T}$	Power-on I/O Initialization Time	–	3	–	ms	–

6.3.1 I/O

Table 8 I/O DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID.GIO#37	V_{IH_CMOS}	Input voltage HIGH threshold	0.7 × V_{DDD}	–	–	V	CMOS input
SID.GIO#38	V_{IL_CMOS}	Input voltage LOW threshold	–	–	0.3 × V_{DDD}	V	CMOS input
SID.GIO#39	$V_{IH\_VDDD2.7-}$	LVTTL input, V_{DDD} < 2.7 V	0.7× V_{DDD}	–	–	V	VDDD = 2.4 V
SID.GIO#40	$V_{IL\_VDDD2.7-}$	LVTTL input, V_{DDD} < 2.7 V	–	–	0.3 × V_{DDD}	V	VDDD = 2.4 V
SID.GIO#41	$V_{IH\_VDDD2.7+}$	LVTTL input, V_{DDD} ≥ 2.7 V	2.0	–	–	V	VDDD = 2.7, 3.3, 5.5 V
SID.GIO#42	$V_{IL\_VDDD2.7+}$	LVTTL input, V_{DDD} ≥ 2.7 V	–	–	0.8	V	VDDD = 2.7, 3.3, 5.5 V
SID.GIO#33	V_{OH_3V}	Output voltage HIGH level	V_{DDD} – 0.6	–	–	V	I_{OH} = 4 mA at 3 V V_{DDD}
SID.GIO#36	V_{OL_3V}	Output voltage LOW level	–	–	0.6	V	I_{OL} = 10 mA at 3 V V_{DDD}
SID.GIO#5	R_{PU}	Pull-up resistor value	3.5	5.6	8.5	kΩ	+25°C T_A, all V_{DDD}
SID.GIO#6	R_{PD}	Pull-down resistor value	3.5	5.6	8.5	kΩ	+25°C T_A, all V_{DDD}
SID.GIO#16	I_{IL}	Input leakage current (absolute value)	–	–	2	nA	+25°C T_A, 3 V V_{DDD}
SID.GIO#17	C_{PIN_A}	Max pin capacitance	–	–	22	pF	Capacitance on USBDP, USBDM pins. Guaranteed by characterization.
SID.GIO#17A	C_{PIN}	Max pin capacitance	–	3	7	pF	–40°C to +85°C T_A, All V_{DDD}, all other I/O_S. Guaranteed by characterization.
SID.GIO#43	V_{HYSTTL}	Input hysteresis, LVTTL V_{DDD} > 2.7 V	15	40	–	mV	Guaranteed by characterization.
SID.GIO#44	$V_{HYSCMOS}$	Input hysteresis CMOS	0.05 × V_{DDD}	–	–	mV	V_{DDD} < 4.5 V. Guaranteed by characterization.
SID69	I_{DIODE}	Current through protection diode to V_{DDD}/V_{SS}	–	–	100	µA	Guaranteed by design.
SID.GIO#45	I_{TOT_GPIO}	Maximum total sink chip current	–	–	85	mA	Guaranteed by design.
Fail-safe							
SID.GIO#46	I_{IHS}	Input current when Pad > V_{DDD} for fail-safe inputs	–	–	10.00	µA	Per I^2C specification

Table 9 I/O AC specifications

(guaranteed by characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID70	T_{RISEF}	Rise time in Fast Strong mode	2	–	12	ns	3.3 V V_{DDD}, C_{load} = 25 pF
SID71	T_{FALLF}	Fall time in Fast Strong mode	2	–	12	ns	3.3 V V_{DDD}, C_{load} = 25 pF

Table 10 GPIO_20VT DC specifications (Applicable to port pins P2.2 and P2.3 only)

(guaranteed by characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID.GPIO_20VT#4	GPIO_20VT_I_LU	GPIO_20VT Latch up current limits	–140	–	140	mA	Max / min current in to any input or output, pin-to-pin, pin-to-supply
SID.GPIO_20VT#5	GPIO_20VT_RPU	GPIO_20VT Pull-up resistor value	1	–	25	kΩ	+25°C T_A, 1.4 V to GPIO_20VT_Voh(min)
SID.GPIO_20VT#6	GPIO_20VT_RPD	GPIO_20VT Pull-down resistor value	2.5	–	20	kΩ	+25°C T_A, 1.4-V to V_{DDD}
SID.GPIO_20VT#16	GPIO_20VT_IIL	GPIO_20VT Input leakage current (absolute value)	–	–	2	nA	+25°C T_A, 3 V V_{DDD}
SID.GPIO_20VT#17	GPIO_20VT_CPIN	GPIO_20VT pin capacitance	15	–	25	pF	–40°C to +85°C T_A, All V_{DDD}, F = 1 MHz
SID.GPIO_20VT#33	GPIO_20VT_Voh	GPIO_20VT Output voltage high level.	2	–	–		I_{OH} = 0.5 mA
SID.GPIO_20VT#36	GPIO_20VT_Vol	GPIO_20VT output voltage LOW level.	–	–	0.4	V	I_{OL} = 2 mA
SID.GPIO_20VT#41	GPIO_20VT_Vih_LVTTL	GPIO_20VT LVTTL input voltage HIGH level.	2	–	–	V	$V_{DDD} \geq 2.7$ V
SID.GPIO_20VT#42	GPIO_20VT_Vil_LVTTL	GPIO_20VT LVTTL input voltage LOW level.	–	–	0.8	V	$V_{DDD} \geq 2.7$ V
SID.GPIO_20VT#43	GPIO_20VT_Vhysttl	GPIO_20VT Input hysteresis LVTTL	15	40	–	mV	$V_{DDD} \geq 2.7$ V
SID.GPIO_20VT#69	GPIO_20VT_IDIODE	GPIO_20VT Current through protection diode to V_{DDD}/V_{SS}	–	–	100	µA	–

Table 11 GPIO_20VT AC specifications (applicable to port pins P2.2 and P2.3 only)

(guaranteed by characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID.GPIO_20VT#70	GPIO_20VT_-TriseF	GPIO_20VT Rise time in Fast Strong Mode	1	-	45	ns	All V_{DDD}, C_{load} = 25 pF
SID.GPIO_20VT#71	GPIO_20VT_T-fallF	GPIO_20VT Fall time in Fast Strong Mode	2	-	15	ns	All V_{DDD}, C_{load} = 25 pF

6.4 Digital peripherals

The following specifications apply to the Timer/Counter/PWM peripherals in the Timer mode.

6.4.1 Timer/counter/PWM

Table 12 TCPWM specifications

(guaranteed by characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID.TCPWM.3	$T_{CPWMFREQ}$	Operating frequency	–	–	Fc	MHz	Fc max = CLK_SYS. Maximum = 48 MHz.
SID.TCPWM.4	$T_{PWMENEXT}$	Input trigger pulse width	2/Fc	–	–	ns	For all trigger events
SID.TCPWM.5	T_{PWMEXT}	Output trigger pulse width	2/Fc	–	–	ns	Minimum possible width of Overflow, Underflow, and CC (Counter equals Compare value) outputs
SID.TCPWM.5A	T_{CRES}	Resolution of counter	1/Fc	–	–	ns	Minimum time between successive counts
SID.TCPWM.5B	PWM_{RES}	PWM resolution	1/Fc	–	–	ns	Minimum pulse width of PWM output
SID.TCPWM.5C	Q_{RES}	Quadrature inputs resolution	1/Fc	–	–	ns	Minimum pulse width between quadrature-phase inputs

6.4.2 I^2C

Table 13 Fixed I^2C DC specifications

(guaranteed by characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/ conditions
SID149	I_{I2C1}	Block current consumption at 100 kHz	–	–	100	µA	–
SID150	I_{I2C2}	Block current consumption at 400 kHz	–	–	135	µA	–
SID151	I_{I2C3}	Block current consumption at 1 Mbps	–	–	310	µA	–
SID152	I_{I2C4}	I^2C enabled in Deep Sleep mode	–	–	1.4	µA	–

Table 14 Fixed I^2C AC specifications

(guaranteed by characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/ conditions
SID153	F_{I2C1}	Bit rate	–	–	1	Mbps	–

Table 15 Fixed UART DC specifications

(guaranteed by characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/ conditions
SID160	I_{UART1}	Block current consumption at 100 kbps	–	–	10	µA	–
SID161	I_{UART2}	Block current consumption at 1000 kbps	–	–	312	µA	–

Table 16 Fixed UART AC specifications

(guaranteed by characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/ conditions
SID162	F_{UART}	Bit rate	–	–	1	Mbps	–

Table 17 Fixed SPI DC specifications

(guaranteed by characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/ conditions
SID163	I_{SPI1}	Block current consumption at 1 Mbps	–	–	360	µA	–
SID164	I_{SPI2}	Block current consumption at 4 Mbps	–	–	560	µA	–
SID165	I_{SPI3}	Block current consumption at 8 Mbps	–	–	600	µA	–

Table 18 Fixed SPI AC specifications

(guaranteed by characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/ conditions
SID166	F_{SPI}	SPI operating frequency (Master; 6X oversampling)	–	–	8	MHz	–

Table 19 Fixed SPI master mode AC specifications

(guaranteed by characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID167	T_{DMO}	MOSI Valid after SClock driving edge	–	–	15	ns	–
SID168	T_{DSI}	MISO Valid before SClock capturing edge	20	–	–	ns	Full clock, late MISO sampling
SID169	T_{HMO}	Previous MOSI data hold time	0	–	–	ns	Referred to slave capturing edge

Table 20 Fixed SPI slave mode AC specifications

(guaranteed by characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID170	T_{DMI}	MOSI Valid before Sclock capturing edge	40	–	–	ns	–
SID171	T_{DSO}	MISO Valid after Sclock driving edge	–	–	$42+3\times T_{CPU}$	ns	$T_{CPU} = 1/F_{CPU}$
SID171A	T_{DSO_EXT}	MISO Valid after Sclock driving edge in Ext Clk mode	–	–	48	ns	–
SID172	T_{HSO}	Previous MISO data hold time	0	–	–	ns	–
SID172A	$T_{SSELSCK}$	SSEL Valid to first SCK Valid edge	100	–	–	ns	–

6.5 System resources

6.5.1 Power-on reset (POR) with brownout reset (BOR)

Table 21 Power-on reset (POR)

(guaranteed by characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID185	$V_{RISEIPOR}$	Power-on reset (POR) rising trip voltage	0.80	–	1.50	V	–
SID186	$V_{FALLIPOR}$	POR falling trip voltage	0.70	–	1.4	V	–

Table 22 Brownout reset (BOR)

(guaranteed by characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID190	$V_{FALLPPOR}$	Brown-out detect (BOD) trip voltage in active/sleep modes	1.48	–	1.62	V	–
SID192	$V_{FALLDPSLP}$	Block current consumption at 1000 kbps	1.1	–	1.5	V	–

Table 23 SWD interface specifications

(guaranteed by characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID.SWD#1	F_SWDCLK1	3.3 V ≤ VDDD ≤ 5.5 V	–	–	14	MHz	SWDCLK ≤ 1/3 CPU clock frequency
SID.SWD#2	F_SWDCLK2	2.7 V ≤ VDDD ≤ 3.3 V	–	–	7	MHz	SWDCLK ≤ 1/3 CPU clock frequency
SID.SWD#3	T_SWDI_SETUP	T = 1/f SWDCLK	0.25 × T	–	–	ns	–
SID.SWD#4	T_SWDI_HOLD	T = 1/f SWDCLK	0.25 × T	–	–	ns	–
SID.SWD#5	T_SWDO_VALID	T = 1/f SWDCLK	–	–	0.50 × T	ns	–
SID.SWD#6	T_SWDO_HOLD	T = 1/f SWDCLK	1	–	–	ns	–

6.5.2 Internal main oscillator

Table 24 IMO DC specifications

(guaranteed by design)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID218	I_{IMO1}	IMO operating current at 48 MHz	–	–	1000	µA	–

Table 25 IMO AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID.CLK#13	F_{IMOTOL}	Frequency variation at 24, 36, and 48 MHz (trimmed)	–	–	±2	%	ALL VDDD. -25°C ≤ TA ≤ 85°C
SID226	$T_{STARTIMO}$	IMO start-up time	–	–	7	µs	Guaranteed by characterization.
SID228	$T_{JITRMSIMO2}$	RMS jitter at 24 MHz	–	145	–	ps	Guaranteed by characterization.
SID.CLK#1	F_{IMO}	IMO frequency	24	36	48	MHz	Only 3 frequencies supported: 24 MHz, 36 MHz, and 48 MHz. -40°C to +85°C TA, ALL VDDD

6.5.3 Internal low-speed oscillator power down

Table 26 ILO DC specifications

(guaranteed by design)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID231	I_{ILO1}	I_{LO} operating current	–	0.3	1.05	µA	–
SID233	$I_{ILOLEAK}$	I_{LO} leakage current	–	2	15	nA	–

Table 27 ILO AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID234	$T_{STARTILO1}$	I_{LO} start-up time	–	–	2	ms	Guaranteed by characterization
SID238	$T_{ILODUTY}$	I_{LO} duty cycle	40	50	60	%	Guaranteed by characterization
SID.CLK#5	F_{ILO}	I_{LO} frequency	20	40	80	kHz	–

Table 28 PD DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID.PD.1	Rp_std	DFP CC termination for default USB power	64	80	96	µA	–
SID.PD.2	Rp_1.5A	DFP CC termination for 1.5 A power	166	180	194.4	µA	–
SID.PD.3	Rp_3.0A	DFP CC termination for 3.0 A power	304	330	356.4	µA	–
SID.PD.4	R_D	UFP CC termination	4.59	5.1	5.61	kΩ	–

Table 28 PD DC specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID.PD.5	R_{D_DB}	UFP (Power Bank) Dead Battery CC Termination on CC1 and CC2	4.08	5.1	6.12	kΩ	All supplies forced to 0V and 1.32 V applied at CC1 or CC2
SID.PD.6	$V_{gndoffset}$	Ground offset tolerated by BMC receiver	–500	–	500	mV	Relative to the remote BMC transmitter.

Table 29 UV/OV specifications

(guaranteed by characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID.UVOV.1	V_{THOV1}	Overvoltage threshold accuracy, 4.0 V to 11.0 V	–3	–	3	%	Active mode
SID.UVOV.2	V_{THOV2}	Overvoltage threshold accuracy, 11 V to 27.4 V	–3.2	–	3.2	%	
SID.UVOV.3	V_{THUV1}	Undervoltage threshold accuracy, 2.7 V to 3.3 V	-4	–	4	%	
SID.UVOV.4	V_{THUV2}	Undervoltage threshold accuracy, 3.3 V to 4.0 V	–3.5	–	3.5	%	
SID.UVOV.5	V_{THUV3}	Undervoltage threshold accuracy, 4.0 V to 11.0 V	–3	–	3	%	
SID.UVOV.6	V_{THUV4}	Undervoltage threshold accuracy, 11.0 V to 22.0 V	–2.9	–	2.9	%	

Table 30 UV/OV AC specifications

(guaranteed by characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID.UVOV.AC.1	T_{OV_GPIO}	Delay from OV threshold trip to output GPIO toggle	–	–	20	µs	Available on P1.0 or P1.1
SID.UVOV.AC.2	T_{OV_GATE}	Delay from OV threshold trip to external PFET power gate turn off	–	–	50	µs	–
SID.UVOV.AC.3	T_{UV_GPIO}	Delay from UV threshold trip to output GPIO toggle	–	–	20	µs	Available on P1.0 or P1.1

Table 31 LS-CSA specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID.LSCSA.1	Cin_inp	CSP input capacitance	7	–	10	pF	Guaranteed by characterization

Table 31 LS-CSA specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID.LSCSA.2	Csa_Acc1	CSA accuracy 5 mV < Vsense < 10 mV	–15	–	15	%	Active mode
SID.LSCSA.3	Csa_Acc2	CSA accuracy 10 mV < Vsense < 15 mV	–10	–	10	%	
SID.LSCSA.4	Csa_Acc3	CSA accuracy 15 mV < Vsense < 20 mV	–6	–	6	%	
SID.LSCSA.5	Csa_Acc4	CSA accuracy 20 mV < Vsense < 30 mV	–5	–	5	%	
SID.LSCSA.6	Csa_Acc5	CSA accuracy 30 mV < Vsense < 50 mV	–4	–	4	%	
SID.LSCSA.7	Csa_Acc6	CSA accuracy 50 mV < Vsense	–4	–	4	%	
SID.LSCSA.8	Csa_SCP_Acc1	CSA SCP 80 mV	–16.5	–	16.5	%	
SID.LSCSA.9	Csa_SCP_Acc2	CSA SCP 100 mV	–13.4	–	13.4	%	Active mode
SID.LSCSA.10	Csa_SCP_Acc3	CSA SCP 150 mV	–9.4	–	9.4	%	
SID.LSCSA.11	Csa_SCP_Acc4	CSA SCP 200 mV	–7.5	–	7.5	%	
SID.LSCSA.12	Av	Nominal gain values supported: 5, 10, 20, 35, 50, 75, 125, 150	5	–	150	V/V	Guaranteed by characterization
SID.LSCSA.24	Av1_E_Trim	Gain Error	–3	–	3	%	Guaranteed by characterization
SID.LSCSA.31	Av_E_SCP	Gain Error of SCP stage after trim	–3	–	3	%	Guaranteed by characterization

Table 32 LS-CSA AC specifications
(Guaranteed by characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID.LSCSA.AC.1	T_{OCP_GPIO}	Delay from OCP threshold trip to output GPIO toggle	–	–	20	µs	Available on P1.0 or P1.1
SID.LSCSA.AC.2	T_{OCP_Gate}	Delay from OCP threshold trip to external PFET power gate turn off	–	–	50	µs	–
SID.LSCSA.AC.3	T_{SCP_GPIO}	Delay from SCP threshold trip to output GPIO toggle	–	–	15	µs	Available on P1.0 or P1.1
SID.LSCSA.AC.4	T_{SCP_Gate}	Delay from SCP threshold trip to external PFET power gate turn off	–	–	50	µs	–
SID.LSCSA.AC.5	T_{SR_GPIO}	Delay from SR threshold trip to output GPIO toggle	–	–	20	µs	Available on P1.0 or P1.1

6.5.4 Gate driver specifications

Table 33 Gate driver DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID.GD.1	R_{PD}	Pull-down resistance	–	–	3	kΩ	Applicable on VBUS_P_CTRL and VBUS_C_CTRL to turn ON external PFET.
SID.GD.2	R_{PU}	Pull-up resistance	–	–	4	kΩ	Applicable on VBUS_P_CTRL to turn OFF external PFET
SID.GD.3	I_{PD0}	Pull-down current sink at drive strength of 1	25	–	75	µA	I-mode (current mode) pull down at 5 V. Applicable on VBUS_P_CTRL and VBUS_C_CTRL to turn ON external PFET
SID.GD.4	I_{PD1}	Pull-down current sink at drive strength of 2	50	–	150	µA	
SID.GD.5	I_{PD2}	Pull-down current sink at drive strength of 4	140	–	300	µA	
SID.GD.6	I_{PD3}	Pull-down current sink at drive strength of 8	280	–	580	µA	
SID.GD.7	I_{PD4}	Pull-down current sink at drive strength of 16	560	–	1200	µA	
SID.GD.8	I_{PD5}	Pull-down current sink at drive strength of 32	1120	–	2300	µA	
SID.GD.9	I_leak_p1	Pin leakage on VBUS_P_CTRL	–	–	0.003	µA	+25°C T_J, 5 V V_{DDD}, 20 V V_{BUS}
SID.GD.10	I_leak_c1	Pin leakage on VBUS_C_CTRL	–	–	0.003	µA	+25°C T_J, 5 V V_{DDD}, 20 V V_{BUS}
SID.GD.11	I_leak_p2	Pin leakage on VBUS_P_CTRL	–	–	2	µA	+25°C T_J, 5 V V_{DDD}, 20 V V_{BUS}
SID.GD.12	I_leak_c2	Pin leakage on VBUS_C_CTRL	–	–	2	µA	+25°C T_J, 5 V V_{DDD}, 20 V V_{BUS}
SID.GD.13	I_leak_p3	Pin leakage on VBUS_P_CTRL	–	–	7	µA	+25°C T_J, 5 V V_{DDD}, 20 V V_{BUS}
SID.GD.14	I_leak_c3	Pin leakage on VBUS_C_CTRL	–	–	7	µA	+25°C T_J, 5 V V_{DDD}, 20 V V_{BUS}

Table 34 Gate driver AC specifications

(guaranteed by characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID.GD.15	T_{PD1}	Pull down delay on VBUS_C_CTRL	–	–	2	µs	Cload = 2 nF, Delay to VBUS –1.5 V from initiation of falling edge, VBUS = 5 V to 20 V, 50 KΩ tied between VBUS_C_CTRL and VBUS
SID.GD.16	$T_{r\_discharge}$	Discharge rate of output node on VBUS_C_CTRL	–	–	5	V/µs	80% to 20%, 50 KΩ tied between VBUS_C_CTRL and VBUS, Cload = 2 nF, Vinitial = 24 V
SID.GD.17	T_{PD2}	Pull down delay on VBUS_P_CTRL	–	–	2	µs	Cload = 2 nF, Delay to VBUS –1.5 V from initiation of falling edge, V_{BUS} = 5 V to 20 V, 50 KΩ tied between VBUS_P_CTRL and VBUS
SID.GD.18	T_{PU}	Pull up delay on VBUS_P_CTRL	–	–	18	µs	Cload = 2 nF, Delay to VBUS–1.5 V from initiation of rising edge, VBUS = 5 V to 20 V, 50 KΩ tied between VBUS_P_CTRL and VBUS
SID.GD.19	SR_{PU}	Output slew rate on VBUS_P_CTRL	–	–	5	V/µs	Cload = 2 nF, 20% to 80% of VBUS_P_CTRL range
SID.GD.20	SR_{PD}	Output slew rate on VBUS_P_CTRL	–	–	5	V/µs	Cload = 2 nF, 80% to 20% of VBUS_P_CTRL range

Table 35 VBUS discharge specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details / conditions
SID.VBUS.DISC.6	I1	20 V NMOS ON current for DS = 1	0.15	–	1	mA	Measured at 0.5 V
SID.VBUS.DISC.7	I2	20-V NMOS ON current for DS = 2	0.4	–	2	mA	
SID.VBUS.DISC.8	I4	20-V NMOS ON current for DS = 4	0.9	–	4	mA	
SID.VBUS.DISC.9	I8	20-V NMOS ON current for DS = 8	2	–	8	mA	
SID.VBUS.DISC.10	I16	20-V NMOS ON current for DS = 16	4	–	10	mA	
SID.VBUS.DISC.11	VBUS_Stop_Error	Error percentage of final V_{BUS} value from setting	–	–	10	%	When V_{BUS} is discharged to 5 V. Guaranteed by characterization.

Table 36 VBUS short protection specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/ conditions
SID.VSP.1	V_SHORT_TRIGGER	Short-to-VBUS system-side clamping voltage on the CC/P2.2/P2.3 pins	–	9	–	V	Guaranteed by characterization.

Table 37 VBUS DC regulator specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID.VREG.2	VBUS_DETECT	VBUS detect threshold voltage	1.08	–	2.62	V	–

Table 38 VBUS AC regulator specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID.VREG.3	T_{start}	Total startup time for the regulator supply outputs	–	–	200	µs	Guaranteed by characterization.

6.5.5 8-bit SAR ADC

Table 39 8-bit SAR ADC DC specifications

(guaranteed by characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID.ADC.1	Resolution	ADC resolution	–	8	–	Bits	–
SID.ADC.2	INL	Integral non-linearity	–2.5	–	2.5	LSB	Reference voltage generated from VDDD
SID.ADC.2A	INL	Integral non-linearity	–1.5	–	1.5	LSB	Reference voltage generated from bandgap
SID.ADC.3	DNL	Differential non-linearity	–2.5	–	2.5	LSB	Reference voltage generated from VDDD
SID.ADC.3A	DNL	Differential non-linearity	–1.5	–	1.5	LSB	Reference voltage generated from bandgap
SID.ADC.4	Gain Error	Gain error	–1.5	–	1.5	LSB	–
SID.ADC.6	V_{REF_ADC2}	ADC reference voltage when generated from band gap.	1.96	2.0	2.04	V	Reference voltage generated from bandgap

Table 40 8-bit SAR ADC AC specifications

(guaranteed by design)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID.ADC.7	SLEW_Max	Rate of change of sampled voltage signal	–	–	3	V/ms	–

6.5.6 Memory

Table 41 Flash AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/ conditions
SID.MEM#3	FLASH_ERASE	Row erase time	–	–	15.5	ms	–40°C ≤ T_A ≤ 85°C, all V_{DDD}
SID.MEM#4	FLASH_WRITE	Row (Block) write time (erase and program)	–	–	20	ms	–40°C ≤ T_A ≤ 85°C, all V_{DDD}
SID.MEM#8	FLASH_ROW_PGM	Row program time after erase	–	–	7	ms	25°C ≤ T_A ≤ 55°C, all V_{DDD}
SID178	$T_{BULKERASE}$	Bulk erase time (32 KB)	–	–	35	ms	–
SID180	$T_{DEVPROG}$	Total device program time	–	–	7.5	s	–
SID182	F_{RET1}	Flash retention, T_A ≤ 55°C, 100K P/E cycles	20	–	–	years	–
SID182A	F_{RET2}	Flash retention, T_A ≤ 85°C, 10K P/E cycles	10	–	–	years	–
SID182B	F_{RET3}	Flash retention, T_A ≤ 105°C, 10K P/E cycles	3	–	–	years	–

7 Ordering information

Table 42 lists the EZ-PD™ PMG1-S0 part numbers and features.

Table 42 EZ-PD™ PMG1-S0 ordering information

Product	Application	Type-C ports	Termination resistor	Role	Package type	Si ID
CYPM1011-24LQXI CYPM1011-24LQXIT	Power sink/source applications	1	R_P, R_D, R_{D-DB}	UFP/DFP	24-pin QFN	0x2020

7.1 Ordering code definitions

The part numbers are of the form CYPM1ABC-DEFGHIJ, where the fields are defined as shown in Table 43.

Table 43 EZ-PD™ PMG1-S0 ordering code definitions

Field	Description	Values	Meaning
CY	Infineon prefix	CY	Company ID
PM	Marketing code	PM	PM = Power Delivery MCU family
1	MCU Family generation	1	Product Family Generation
A	Family	0	S0
		1	S1
		2	S2
		3	S3
B	PD ports	1	1-PD port
		2	2-PD port
C	Application specific	X	Application specific
DE	Pin	XX	Number of pins in the package
FG	Package code	LQ	QFN
		BZ	BGA
		FN	CSP
H	Lead free	X	Lead: X = Pb-free
I	Temperature range	I	Industrial
J	Only for T&R	T	Tape and reel

8 Packaging

Table 44 Package characteristics

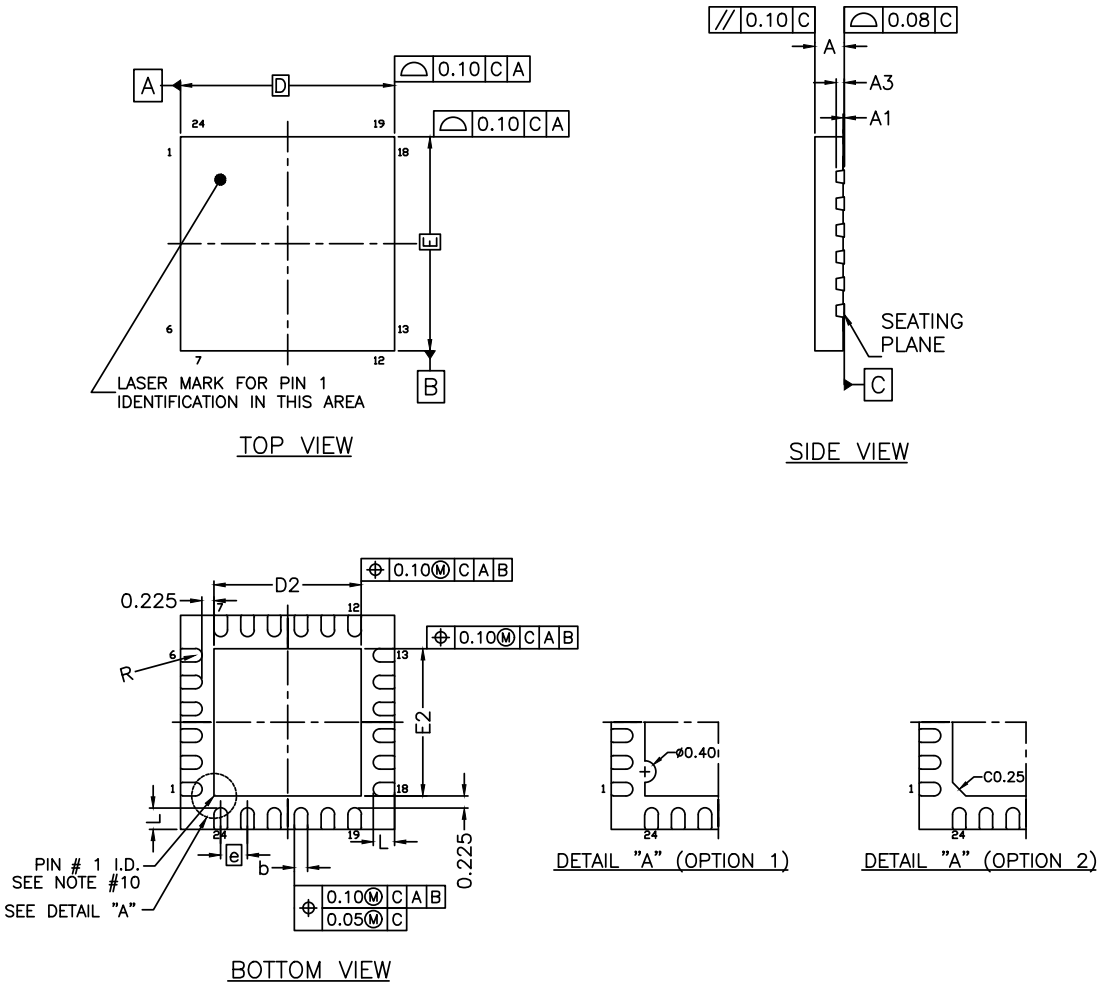
Parameter	Description	Conditions	Min	Typ	Max	Units
T_A	Operating ambient temperature	Extended Industrial	-40	25	105	°C
T_J	Operating junction temperature	Extended Industrial	-40	25	120	°C
T_{JA}	Package θ_{JA} (24-QFN)	–	–	–	19.98	°C/W
T_{JC}	Package θ_{JC} (24-QFN)	–	–	–	4.78	°C/W

Table 45 Solder reflow peak temperature

Package	Maximum peak temperature	Maximum time within 5°C of peak temperature
24-pin QFN	260°C	30 seconds

Table 46 Package moisture sensitivity level (MSL), IPC/JEDEC J-STD-2

Package	MSL
24-pin QFN	MSL3



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	0.60
A1	0.00	—	0.05
A3 (Option 1)	0.152 REF		
A3 (Option 2)	0.127 REF		
b	0.18	0.25	0.30
D	4.00 BSC		
D2	2.65	2.75	2.85
E	4.00 BSC		
E2	2.65	2.75	2.85
L	0.30	0.40	0.50
e	0.50 BSC		
R	0.09	—	—

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIE THICKNESS ALLOWABLE IS 0.305 mm MAXIMUM(.012 INCHES MAXIMUM)
3. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. -1994.
4. THE PIN #1 IDENTIFIER MUST BE PLACED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
5. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
6. PACKAGE WARPAGE MAX 0.08 mm.
7. APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
8. APPLIED ONLY TO TERMINALS.
9. JEDEC SPECIFICATION NO. REF: N.A.
10. INDEX FEATURE CAN EITHER BE AN OPTION 1 : "MOUSE BITE" OR OPTION 2 : CHAMFER.

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Figure 7 24-pin QFN package outline (PG-VQFN-24)

9 Acronyms

Table 47 Acronyms used in this document

Acronym	Description
AC	Apple charging
ADC	analog-to-digital converter
AES	advanced encryption standard
AFC	adaptive fast charging
API	application programming interface
Arm®	advanced RISC machine, a CPU architecture
BC	battery charging
BMC	Bi-phase Mark Coding
CC	configuration channel
CPU	central processing unit
CS	current sense
CSA	current sense amplifier
CRC	cyclic redundancy check, an error-checking protocol
DFP	downstream facing port
DIO	digital input/output, GPIO with only digital capabilities, no analog. See GPIO.
DRP	dual role port
EEPROM	electrically erasable programmable read-only memory
EMCA	electronically marked cable assembly, a USB cable that includes an IC that reports cable characteristics (e.g., current rating) to the Type-C ports
EMI	electromagnetic interference
ESD	electrostatic discharge
FS	full-speed
GPIO	general-purpose input/output
IC	integrated circuit
IDE	integrated development environment
I^2C, or IIC	Inter-Integrated Circuit, a communications protocol
ILO	internal low-speed oscillator, see also IMO
IMO	internal main oscillator, see also ILO
I/O	input/output, see also GPIO
LDO	low-dropout regulator
LS-CSA	Low-side current sense amplifier
LVD	low-voltage detect
LVTTL	low-voltage transistor-transistor logic
MCU	microcontroller unit
NC	no connect
NMI	nonmaskable interrupt
NVIC	nested vectored interrupt controller

Table 47 Acronyms used in this document *(continued)*

Acronym	Description
OCP	over current protection
opamp	operational amplifier
OTP	over temperature protection
OVP	overvoltage protection
PCB	printed circuit board
PD	power delivery
PHY	physical layer
POR	power-on reset
PRES	precise power-on reset
PRNG	pseudo random number generation
PWM	pulse-width modulator
QC	quick charge
RAM	random-access memory
RCP	reverse current protection, supported in Source Configuration only
RISC	reduced-instruction-set computing
RMS	root-mean-square
RTC	real-time clock
RX	receive
SAR	successive approximation register
SCB	serial communication block
SCL	I^2C serial clock
SCP	short circuit protection, supported in Source Configuration only
SDA	I^2C serial data
S/H	sample and hold
SHA	secure hash algorithm
SPI	Serial Peripheral Interface, a communications protocol
SRAM	static random access memory
SWD	serial wire debug, a test protocol
TCPWM	timer counter pulse-width modulator
TRNG	true random number generation
TX	transmit
Type-C	a new standard with a slimmer USB connector and a reversible cable, capable of sourcing up to 100 W of power
UART	Universal Asynchronous Transmitter Receiver, a communications protocol
USB	Universal Serial Bus
USBIO	USB input/output, PMG1-S0 pins used to connect to a USB port
UVP	undervoltage protection
XRES	external reset I/O pin

10 Document conventions

10.1 Units of measure

Table 48 Units of measure

Symbol	Unit of measure
°C	degrees celsius
Hz	hertz
KB	1024 bytes
kHz	kilohertz
kΩ	kiloohm
Mbps	megabits per second
MHz	megahertz
MΩ	megaohm
Msps	mega samples per second
µA	microampere
µF	microfarad
µs	microsecond
µV	microvolt
µW	microwatt
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
Ω	ohm
pF	picofarad
ppm	parts per million
ps	picosecond
s	second
sps	samples per second
V	volt

Revision history

Document revision	Date	Description of changes
**	2020-10-23	New datasheet.
*A	2021-02-24	Updated **Figure 1** and **Figure 2**. Updated **Table 1** with latest values for GPIO, TCPWM, and SCB counts for PMG1-S3. Added note in **Figure 1** and **Table 1**. Added links in **Development support**. Updated **Application diagram**. Changed D+/D- pin names to USBDP/USBDM. Added Notes 7, 8, and 10 in **Electrical specifications**. Updated **Acronyms**. Updated Copyright year.
*B	2021-05-27	Updated **Table 3**. Changed datasheet status from preliminary to final.
*C	2022-05-18	Added **Pin based absolute maximum ratings**. Updated **Figure 7**. Migrated to IFX template.
*D	2022-07-21	Updated MOSFET gate drivers for EZ-PD™ PMG1-S0 in **Table 1** Addition of CSP pin for current measurement: • Updated **Figure 1**, **Block diagram**, **Figure 4**, and **Figure 5** • Updated **Table 1**, **Table 3**, **Table 5**, **Table 47**, and **Table 48** • Added **Table 31** and **Table 32**. • Added section **"Low-side current sense amplifier (CSA)"** on page 10
*E	2025-04-01	Updated **Figure 1**, **Figure 3** and **Figure 5** Updated Power delivery in **Table 1** Updated **EZ-PD™ PMG1-S0 general description** Updated **Features** Updated **Block diagram** Updated OVT to Fail-safe Updated **Development support** Updated **CPU and memory sub-system** Updated **USB PD subsystem (SS)** Updated **Fixed-function digital** Updated **GPIO interface** Updated Absolute maximum (V) in **Table 5** Updated details/conditions in **Table 8**, **Table 9**, **Table 25** and **Table 33** Updated **Power-on reset (POR) with brownout reset (BOR)** Updated Min, Max, detail/conditions in **Table 31** Updated **Ordering information** Updated **Acronyms** Added **Fail-Safe GPIOs** Updated **Pinouts**.

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