Release Notes SRN061

PSoC Designer Version 5.0 Service Pack 2

Release Date: November 21, 2008

Thank you for your interest in PSoC Designer™ version 5.0 Service Pack 2. These release notes list installation requirements and describe software updates and changes.

System Requirements and Recommendations

System Requirements	Minimum	Recommended
▪ Processor Speed	1 GHz	2 GHz Dual Core
▪ MB of RAM	256 MB	1 GB
▪ MB of Free Hard Drive Space	300 MB	500 MB
▪ Screen Resolution	1024x768	1280x1024
▪ CD-ROM Drive	✓	✓
▪ USB Port, preferably Open Host Controller or Universal	✓	✓
▪ Windows® 2000, XP (SP1, 2 or 3), or Vista	✓	✓
▪ Microsoft Internet Explorer 6.0 (See note in the installation section)	6.0 (SP1)	7.0
▪ .NET Framework	2.0	2.0 (SP1 or higher)
▪ Adobe Reader (For Viewing of .PDF Documentation)	6	9
▪ PSoC Programmer	3.00.0.92	3.00.0.92

Updates

Check http://www.cypress.com/psocdesigner for the latest downloads of software and documentation.

New for PSoC Designer 5.0 Service Pack 2

PSoC Designer 5.0 allows you to create chip-level (PSoC Designer) projects, or system-level (Express) projects that can also be used as chip-level projects. Included in Service Pack 2 are many bug fixes and support for many new product families listed below.

Please note that in many cases, new product support may be in the beta test phase. This is called out below (beta) and indicates that production release support will follow in the near future.

New Product and Kit Support Included in PSoC Designer 5.0 Service Pack 2

The following is a list of all the new product support provided in Service Pack 2. For specific new user module and product device model numbers, see the appropriate sections below.

- CY8C20X66, CY7C604xx and CY7C643xx Product Families (production release)

- OvationONS™ II (CYONS2xxx) Product Family (beta)
- OvationONS™ SLIM (CYONS2xLxx) Product Family (beta)
- CY8CLED03Dxx and CY8CLED04Dxx Product Family (beta)
- CY8CNPxxx Product Family (beta)
- CY8CTxx110 Product Family (beta)

Installation

If an ICE-Cube is connected to the installation machine it must be disconnected and then reconnected after installing PSoC Designer 5.0 SP2.

Note: PSoC Designer SP2 is not presently compatible with the internet browser, Microsoft Internet Explorer 8 beta (any beta version). If Microsoft Internet Explorer 8 beta is installed on your system, it must be uninstalled and an earlier version of Microsoft Internet Explorer installed in its place. Refer to the Microsoft Internet Explorer 8 beta for instructions of how to perform this operation.

To Install:

1. Shut down any currently running instances of PSoC Designer.
2. If PSoC Designer 5.0 is currently installed, uninstall it.Click Start, click Control Panel, and then double click Add or Remove Programs.
3. Download and install PSoC Designer 5.0 SP2 by running the provided installer.
4. Download and install the latest PSoC Programmer 3.00 by running the provided installer.

   Note: During the installation, if you have not already installed the HI-TECH compiler v9.61 PL4, a dialog will present you with the option of upgrading to the new version. The patch is necessary to support new devices and features in PSoC Designer 5.0 SP2.

   To revert to an earlier version of the HI-TECH compiler after an update is installed, select the compiler version under **Tools → Options → Compiler** in PSoC Designer.

   If you choose to decline the compiler update, you must manually update the psoc.ini file to add device support before you can compile projects that use the new devices. The HI-TECH "psoc.ini" file is found in the HI-Tech installation folder. The default location of the psoc.ini is here:

   ```
   C:\Program Files\HI-TECH Software\HCPSOC\PRO\9.61\dat\psoc.ini
   ```

   The default location of the replacement "psoc.ini" file that adds support for the new devices is here:

   ```
   C:\Program Files\Cypress\Common\CypressSemiBuildMgr\tools\psoc.ini
   ```

Part Support

PSoC Designer 5.0 Service Pack 2 provides support for the following new devices.

CY8NPxxx Product Family

Family	Device	Description

Family	Device	Description
CY8NPxxx	CY8NP512-24SPI	512KB, 48-pin SSOP, 24 MHz
	CY8NP001-24SPI	1MB, 48-pin SSOP, 24 MHz
	CY8NP512-12SPI	512KB, 48-pin SSOP, 12 MHz
	CY8NP001-12SPI	1MB, 48-pin SSOP, 12 MHz
	CY8NP512-24AGI	512KB, 100-pin TQFP, 24 MHz
	CY8NP001-24AGI	1MB, 100-pin TQFP, 24 MHz
	CY8NP512-12AGI	512KB, 100-pin TQFP, 12 MHz
	CY8NP001-12AGI	1MB, 100-pin TQFP, 12 MHz

CY8C20X66, CY7C604xx, and CY7C643xx Product Families

Name	Pin Package	Notes
CY8C20246	16-pin QFN	8k flash
CY8C20346	24-pin QFN	8k flash
CY8C20446	32-pin QFN	8k flash
CY8C20546	48-pin SSOP	8k flash, Full Speed USB
CY8C20266	16-pin QFN	16k flash
CY8C20366	24-pin QFN	16k flash
CY8C20466	32-pin QFN	16k flash
CY8C20566	48-pin SSOP	16k flash, Full Speed USB
CY8C20666	48-pin QFN	16k flash, Full Speed USB
CY7C64315	16-pin QFN	16K flash, Full Speed USB
CY7C64316	16-pin QFN	32K flash, Full Speed USB
CY7C64345	32-pin QFN	16K flash, Full Speed USB
CY7C64355	48-pin QFN	16K flash, Full Speed USB
CY7C64356	48-pin QFN	32K flash, Full Speed USB
CY7C60445	32-pin QFN	16K flash, Full Speed USB
CY7C60455	48-pin QFN	16K flash, Full Speed USB
CY7C60456	48-pin QFN	32K flash, Full Speed USB

New CY8CLED03Dxx and CY8CLED04Dxx Parts

Part Name	Pin Package	Notes
CY8CLED03D01	48-pin QFN	16K Flash

Part Name	Pin Package	Notes
CY8CLED03D02	48-pin QFN	16K Flash
CY8CLED04D01	56-pin QFN	16K Flash
CY8CLED04D02	56-pin QFN	16K Flash

New OvationsONS devices

Part Name	Pin Package	Notes
CYONS2000-LBXC	43-pin lead PQFN	Desktop Wired
CYONS2001-LBXC	43-pin lead PQFN	Desktop Wireless
CYONS2100-LBXC	43-pin lead PQFN	High Performance Wired
CYONS2101-LBXC	43-pin lead PQFN	High Performance Wireless
CYONS2110-LBXC	43-pin lead PQFN	High Performance Wired & Wireless
CYONS20L0-AAXC	52-pin TQFP	Wired OEM Laser Mouse
CYONS20L1-AAXC	52-pin TQFP	Wireless OEM Laser Mouse
CYONS20L1T-AAXC	52-pin TQFP	Trackball without CapSense
CYONS21L1T-AAXC	52-pin TQFP	Trackball with CapSense

New User Modules

Included in PSoC Designer 5.0 SP2 are several new user modules. The service pack includes user modules for configuring the power handling (PWR) and navigation functions (NAV) of the OvationONS II devices, user modules for accessing specific hardware features of the CY8CLED0xDx product family, multiple capacitive sensing methods (CSD and CSA) customized to work with new device families, and others.

New STDUM User Modules		
Name	**Devices Supported**	**Description**
NVSRAM 1.0	CY8CNP102x	Configure parallel interface between PSoC and NVSRAM. Provide API's for NVSRAM read and write.
TRUETOUCH_GESTURE 1.0	CY8CTMG110	Implements a projected capacitance touch screen on a CY8CTMTG110 device with support for gestures.

TRUETOUCH_SINGLE 1.0	CY8CTST110	Implements projected capacitance touch screen on a CY8CTST110 PSoC device with support for single finger touches.
New SHAREDUM User Modules		
Name	**Devices Supported**	**Description**
CYFISPI 1.0	CY8C601xx CY7C602xx CY7C603xx CY7C638xx CY7C64215 CY8C21x23 CY8C21x34 CY8C24x23 CY8C24x94 CY8C27x43 CY8C29x66 CY8CLED02 CY8CLED04 CY8CLED08 CY8CLED16	CyFi™ radio low level interface.
CYFISNP 1.0	CY7C601xx (node only) CY7C602xx (node only) CY7C603xx (node only) CY7C64215 CYRF69103 (node only) CY8C21x34 (node only) CY8C24x94 CY8C27x43 CY8C29x66 CY8CLED04 CY8CLED08 CY8CLED16	CyFi™ Star Network Protocol hub and node functionality.
New CY8C20060 User Modules		
Name	**Devices Supported**	**Description**

ADCINC 1.1	CY8C20x66, CY7C643xx, CY7C60424, CY7C6053x, CYONS2xxx, and CYONS2xLx	Analog to Digital Converter
CSD 0.2	CY8C20x66, CYONS21L1T, and CYONS2110	An updated version of the CapSense™ Sigma-Delta User Module
E2PROMx128 1.1	CY8C20x66, CY7C645xx, CY7C643xx, CY7C60424, CYONS2xxx and CYONS2xLx	Improved over CY8C20x34 by using an on-chip temperature sensor to optimize flash memory endurance
EzI2Cs 1.1	CY8C20x66, CY7C645xx, CY7C643xx, CY7C60424, CYONS2xxx and CYONS2xLx	Supports I2C Hardware address detection in active and sleep modes
I2CHW 1.1	CY8C20x66, CY7C645xx, CY7C643xx, CY7C60424, CYONS2xxx and CYONS2xLx	Supports I2C Hardware address detection in active and sleep modes
NAV 0.2	CYONS2xxx and CYONS2xLx	Controls the optical navigation system on the CYONS2xxx and CYONS2xLx devices.
PWR 0.2	CYONS2xxx and CYONS2xLx	Configures and controls the power system on the CYONS2xxx and CYONS2xLx devices.
TIMER16 1.1	CY8C20x66, CY7C645xx, CY7C643xx, CY7C60424, CYONS2xxx and CYONS2xLx	16-bit timer.
New PPSoC User Modules		
Name	**Devices Supported**	**Description**
CMPHW 1.0	CY8CLED03Dxx CY8CLED04Dxx	Hardware Comparator
CURSENSEHW 1.0	CY8CLED03Dxx CY8CLED04Dxx	Hardware Current Sense Amplifier
DMM16HW 1.0	CY8CLED03Dxx CY8CLED04Dxx	16-bit Hardware Density Modulated PWM
DualDAC8HW 1.0	CY8CLED03Dxx CY8CLED04Dxx	Dual 8-bit Hardware Dual DAC

HYSTCTRL 1.0	CY8CLED03Dxx CY8CLED04Dxx	Hysteretic Controller
PRISM16HW 1.0	CY8CLED03Dxx CY8CLED04Dxx	16-bit Hardware PrISM
PWM16HW 1.0	CY8CLED03Dxx CY8CLED04Dxx	16-bit Hardware Pulse Width Modulator
FLBUCK 1.0	CY8CLED03Dxx CY8CLED04Dxx	Floating Load Buck Regulator
BOOST 1.0	CY8CLED03Dxx CY8CLED04Dxx	Boost Regulator

Known Limitations for PSoC Designer 5.0 Service Pack 2

CY8C20X66/CY7C604xx/CY7C643xx Limitations

1. Problems with the debugger in combination with hardware interrupts including I^2C, CMP, and Timer16 have been reported. Best performance may be achieved by using only CPUCLK = SysClk/1 settings. Some dependence on board layout have been observed. A future update to the Silicon is expected to address these problems.
    a. I^2C is operational with the following limitations:
        i. When using the ICE-CUBE debugger, if Interrupts are used with the I2CHW User Module, the CPUCLK setting should only be used with a setting of SYSCLK/1. Suggested IMO frequencies are 12MHz and 6 MHz.
        ii. If the I2CHW User Module is used with Polled data acquisition, no limitations exist with respect to the ICE-CUBE, or CPUCLK. See the I2CHW data sheet for a discussion of polled data acquisition.
        iii. EZI2C only supports interrupts for acquiring data.
    b. SPI operation.
        i. When used with the ICE-CUBE and SPI-interrupts, CPUCLK should only be set to SYSCLK/1. Suggested IMO settings are 12 MHz or 6MHz. Problems have been reported using the SPI slave function, although a specific fault has not been identified.
        ii. An implementation using polling for RXBufferFull or SPI_TX_COMPLETE is suggested to avoid ICE-CUBE related interrupt difficulties.
2. Setting the IMO to 24 MHz has been reported to cause debugger failures particularly in combination with the USBFS User Module.
3. The ADC User Module is not functional for some combinations of CPU clock and DataClock. The CPU clock (after clock division) must be running at least as fast as the data clock or the ADC will not function correctly.

4. The EEPROM User Module may not write properly when blocks of size less than 128 bytes are written.
5. The LED User Module may not be used on PORT4 (if it exists on the part in use)
6. CSD User Module fails at some SysClk settings

	IMO >> (in MHz)		
CPU_Clock	24	12	6
SysClock / 1	F		
SysClock / 2			
SysClock / 4			
SysClock / 8	F	F	F
SysClock / 16			
SysClock / 32			
SysClock / 128		F	F
SysClock / 256		F	F

7. CSA User Module fails at some SysClk settings

	IMO >> (in MHz)		
CPU_Clock	24	12	6
SysClock / 1	F	F	
SysClock / 2			
SysClock / 4			
SysClock / 8			
SysClock / 16	F		
SysClock / 32	F		
SysClock / 128	F		F
SysClock / 256	F	F	F

8. In order for the HiTech compiler to support some of the listed part numbers, you will have to replace the psoc.ini file in the compiler installation folder.

   Replace this file:
   `<HI-TECH Installpath>\HCPSOC\PRO\9_61\dat\psoc.ini`

   with this one:
   `<PD50 installpath>\Cypress\Common\CypressSemi\BuildMgr\tools\psoc.ini`

OvationONS™ II Limitations

9. The ADC User Module is not functional for some combinations of CPU clock and DataClock. The CPU clock (after clock division) must be running at least as fast as the data clock or the ADC will not function correctly.

10. The EEPROM User Module may not write properly when blocks of size less than 128 bytes are written.

PSoC Designer 5.0 SP2 ColorLock Limitations

11. There is no resource tracking for High Brightness LED drivers. You must be aware of the quantity of HBLED drivers and PSoC pin limitations. Currently there are no warnings issued when too many HBLED drivers are added to your project.
12. When using the 3 HBLED 700 mA Rebel driver, naming the Trigger Valuator “ColorLockTrigger” creates Transfer Function errors.
13. When assigning pins to the 700 mA Luxeon Rebel ColorLock driver, the pins must be unassigned and applied in reverse order. The driver has the pin name pse_TCS230SHARED_# S#. You must apply pin S3 first followed by S2, S1, and ending with S0.
14. For any 3-LED color mixing drivers in simulation mode, the Current Value display box displays CIEx and CIEy irrespective of any color space parameters.
15. If you calibrate the color sensor inside the tuner, you must restart the EZ-Color device.

CY8CLED03Dx and CY8CLED04Dx Product Family Known Limitations

16. Pin names overlap each other in the ‘Pinout Editor’. If any of the names cannot be discerned, the part datasheet may be used for required information.
17. Parameter descriptions are not available in the parameter window. The required content can be found in the corresponding User Module datasheet.
18. The ‘Help me choose a part’ link on the device catalog points to a file that does not contain information regarding Power PSoC parts exclusively designed for lighting market. This information currently may be found at www.cypress.com
19. The context menu features are disabled for Power PSoC parts. Typically right clicking a placed User Module instance in the chip level view provides user with Datasheet, Properties options. This feature is currently disabled for Power PSoC parts.
20. VGND0 and VGND1 parameters used by the HYSTCTRL UM’s Trip Input option have been merged to VGND. If the value of the Trip Input parameter built in earlier extension packs was set to either VGND0 or VGND1, it will default to first available option. You must reset this parameter to VGND.
21. The wizard of Buck and Boost UMs cannot be accessed by right-clicking on UM instance in interconnect view. User must select it from right-clicking on the UM instance in the Workspace explorer.
22. When an external FET option is used, the Buck and Boost UM allow a maximum FET current of 2A. This value may be increased in production release after a higher current is validated.
23. The Buck and Boost UM contain references to an Application Note that contains formulae and description of the Efficiency Calculator. This application note is not available in beta software.
24. All PPSoC UMS have been consolidated to Power folder.

25. Boost User Module allows for selection of SysClk*2. This option is however produces a clock signal higher then the maximum allowed value for a ADC User Module. The required clock settings are described in the datasheet.
26. Warnings indicated in Buck and Boost User Module shown in the wizard are not displayed after the wizard is closed and re-opened. The wizard will display errors only after a value is changed. This defect will be fixed in the production release.
27. The 4-Channel option of the Boost UM appears in the 3-channel part. The 4-Channel version of the Boost UM does not place in the 3-channel part as required. This option will be made unavailable in the production release.
28. The Boost UM uses current feedback from RSense2 resistors. Thiese resistors are connected to the following pins

    P0[3] - Channel 1

    P0[5] - Channel 2

    P0[7] - Channel 3

    P0[4] - Channel 4

    The beta version of the User Module does not present information regarding the pins. The BOOST UM in production release will contain a schematic that will dynamically update show the correct pin number.

Known Problems for PSoC Designer 5.0 Service Pack 2

General Problems

	Problem	Work Around
1.	Slow behavior in monitor mode for High Brightness LED drivers. Performance of the communication interface with the target hardware and updates of the driver GUI widgets can be slow when in monitor mode for a project that includes a High Brightness LED driver. It can take from 1 to 2 seconds for keystrokes entered in a text box to be reflected in the GUI. Values entered in the text entry box to be sent to the target hardware can take from 3 to 5 seconds to be transmitted to the target hardware and be read back and displayed in the High Brightness LED driver monitor widget. [26693]	No work around at this time.

Problems with Chip-Level Projects

	Problem	Work Around
2.	When cloning a project you must be aware that some devices do not share user module capabilities. If you clone a project for one device to another device certain user modules may not appear. [27409]	Check what user modules are available for the cloned device.
3.	The I2CHW and EZI2Cs User Modules are unable to detect whether I^2C bus pins are consumed by the CSD User Module. Therefore, it is possible to configure the I2CHW or EZI2Cs User Module to use pins already consumed by the CSD User Module. [22470]	Place and configure the applicable I2CHW, or EZI2Cs User Module prior to placing the CSD User Module. The CSD User Module wizard will detect that the I^2C pins have been consumed.

Problems with System-Level Projects

	Problem	Work Around
4.	When the monitor is running for System-level projects, some of the GUI elements (such as menu items or dialog buttons) may not update properly or may be disabled. [27057]	If this occurs, stop the Monitor before initiating other activities.

5.	The literal code transfer function does not support multiple variable declarations on a single line of code. [27225]
	Example:
	`int a, b;`
		Declare one variable per line of code.
		Example:
		`int a;`
		`int b;`

6.	PSoC Designer 5.0 allows you to add additional analog input drivers after adding a CSDR CapSense driver. [27385]	When using a CSDR driver you cannot add an additional analog driver even though this is allowed by the program.
7.	A Discrete interface valuator cannot be an input for a TableLookup transfer function if the Discrete interface valuator's state values are not defined in the state list as an unbroken numeric sequence of constants starting at 0. [27342]	When defining state values, define the first state value as 0, the second state value as 1, and so on until the last state is defined. Ensure that each successive value in the list is greater than the previous value by 1.

	Problem	Work Around
8.	When a State Machine transfer function valuator's name contains an underscore character (_) and an input driver, output driver, or other valuator's name is identical to the portion of the State Machine valuator's name before the underscore (ex. State Machine valuator named abc_def and LED output driver named abc) , the System Level editor tool might show a transfer function relationship line between these two even though there is no relationship. The project will also fail to build. [27010]	Avoid using the underscore (_) character in driver and valuator names. Also avoid naming drivers or valuators with substrings of other driver and valuator names.
9.	When a System-level project created on a system with high display resolution is open on a system with lower display resolution some of the design elements (drivers, valuator) may appear outside of the viewport. [27356]	Use Zoom Out to bring all design elements into the viewport. Then relocate items as necessary. Or switch to higher display resolution.
10.	Half-Line LCD drivers allow up to 7 characters to be entered, while Full-Line LCD drivers allow up to 16 characters. PSoC Designer 5.0 does not limit you to the number characters that can be entered into a Half-Line and Full-Line LCD driver label edit box. The characters beyond the maximum number are disregarded by the PSoC Designer 5.0. [27343]	You can select the label in the Half-Line and Full-Line properties window and see the description detailing how many characters can be placed in the selected label.

Problems with Compilation and Debug

	Problem	Work Around
11.	Although the Chip Level view indicates that the CY7C63803's CPU speed and sleep timer interval can be configured, PSoC Designer does not generate the applicable firmware initialization. [25756]	Manually add a line of code in the application program to initialize the value of OSC_CR0, the register that sets CPU speed and sleep timer interval.
12.	System-level projects do not allow compiler selection before the first "Generate/Build Project" invocation. [26969]	Set the desired compiler to be the default PSoC Designer 5.0 compiler using Tools → Options → Build → Compiler before creating a System-level project.

	Problem	Work Around
13.	Multiple instances of PSoC Designer and PSoC Programmer can be open at the same time, but only a single instance is allowed to access the ICE at a given time. An error message stating "ICE Unavailable" will result when instances of either application attempt to access the ICE if it is already connected. [23569]	Press the disconnect button in the application that is currently connected to the ICE or close it completely to free it for connection in one of the other open instances.
14.	There are known problems in the debugger when viewing function parameter variables with immediate values. [25847] For example foo(2,3)	The work-around is to assign values to variables instead and then pass the variables into the function. For example, foo(a,b)
15.	PSoC Designer 5.0 may not recognize a second ICE-Cube. [26513]	Go to Project → Setting → Debugger where the new ICE-Cube is listed and select it for use.
16.	If you move a project from one location to another and you try to compile an individual file, the compile will fail because the compiler's path to the file is absolute. If you move the project from one location and then rebuild the entire project, the absolute file paths are regenerated and compilation will succeed. The bug only affects individual file compilation. [26059]	There are build files generated that include explicit paths. These files are rebuilt when the overall project is re-built. You should rebuild the entire project after copying the project before performing individual file compilation.

OvationONS™ II Known Problems

	Problem	Work Around
17.	I/O registers banks 2 and 3 may not be displayed during debug. [21468]	It may be necessary to add test code to read the relevant registers into a location that is readable for debug. Fix planned.

Problems with CYFISPI and CYFISNP User Modules

	Problem	Work Around
18.	Touch screen projects will not build or compile unless the TrueTouch™ wizard has first been run. [30116]	Run the wizard and assign all pins before attempting to build and compile.

	Problem	Work Around
19.	CY8CTST110 projects will not compile using the ImageCraft compiler. [30092]	Download and install either the HI-TECH Pro or the HI-TECH Lite compiler. HI-TECH Lite is free, while a 45-day free trial is available for HI-TECH Pro.
20.	CY8CTMG110 projects will not compile using the ImageCraft or HI_TECH Lite compilers. [30092]	Download and install the HI-TECH Pro compiler. A 45-day free trial is available.

Problems with Touchscreen User Modules

	Problem	Work Around
21.	On PSoC devices, CYFISPI and CYFISNP configures the MISO row input synchronizer to Async. The row input synchronizer display does not refresh immediately. [30078]	No work-around. However, the row input synchronizer display will eventually refresh, and generated code functions properly.
22.	On enCoRe II devices, the ClockDivider parameter of the CYFISPI and CYFISNP user modules can be configured to result in unacceptable SPI data rates. [30814]	Follow the CYFISPI and CYFISNP data sheet recommendations for SPI data rate configuration.
23.	It is possible to assign the CYFISPI and CYFISNP IRQ Pin and nSS Pin parameters to the same pin, which is not a valid configuration. When one of the parameters is re-assigned to a new pin, the configuration specified by the unchanged parameter is not retained, so the generated code remains non-functional. [32884]	If you mistakenly assign both the IRQ Pin and nSS Pin parameters to the same pin, reconfigure both of these parameters to different pins before proceeding to configure them according to the desired configuration.

Considerations Using HI-TECH as the Default C Compiler with System-Level Designs

This section refers to a project that was either done originally in PSoC Express 3.0 or using PSoC Designer 5.0 in the system-level mode (formerly called Express) to generate the design.

- When recompiling an old project with the HI-TECH Lite C compiler, it is unlikely that you will get an error due to any change in compilers. This is because of the standardized and modular programming model of PSoC Express. However, if the base device runs out of available ROM space, a compile error does occur. To remedy this condition:
    - Choose a device with more resources
    - Upgrade to the Pro version of the HI-TECH C compiler
    - Revert to the ImageCraft C compiler

- Compiler settings are saved in individual PSoC projects. When you open an existing project that you built with the ImageCraft C compiler, the project is built with ImageCraft. To change this behavior, you must switch the compiler vendor to HI-TECH (**Build → Select Compiler Vendor** for *project*) for all previously built projects. There is a default compiler selection as well (**Build → Select Default Compiler Vendor**). The default compiler applies to all new projects, not previously built projects.
- The default compiler selection is applied to a project when it is created. After creating a new project, the compiler vendor cannot be changed until the project is built once. Changing the default compiler vendor with a project open does not alter the compiler setting for the open project.
- Because of the amount of code and floating point math required, ColorLock and ColorMix driver operations may exceed the timing of the 64Hz system loop timer, resulting in "Free Run" operation. When compiled with the HI-TECH Lite C Compiler, the behavior of the system may appear to be sluggish when compared to the same code compiled using the HI-TECH Pro C Compiler. The Lite compiler produces less optimized code than Pro, resulting in longer execution time.
- Under **Project → Settings → Build → Compiler** with HI-TECH C compiler selected as the default, there is a button that allows you to switch between HI-TECH Pro mode and HI-TECH Lite mode. The correct control code will be entered by PSoC Designer 5.0 automatically when the button is pressed.

Considerations Using HI-TECH as the Default C Compiler with Chip Level

This section refers to a project that was either created originally in PSoC Designer 4.x or using PSoC Designer 5.0 exclusively in the chip level mode to generate the design. The issues relate to PSoC Designer 5.0 with version 9.61 of the HI-TECH C compiler. For additional help with the HI-TECH compiler, see the docs folder in the HI-TECH installation directory.

- Opening projects created with PSoC Designer version 4.1 or earlier and building them with the HI-TECH compiler may result in the loss of any ImageCraft custom compiler/linker settings.
- The UART_szGetParam() function for the UART User Module currently does not function as expected using the HI-TECH C Compiler. The function is supposed to return a null pointer if there are no more parameters left. Under certain circumstances, when returning a null pointer through a fastcall16 function such as szGetParam(), the pointer is returned to C as a 16-bit pointer with the most significant bit set to 1. See HI-TECH Manual Section 3.3.11.2 Data Pointers. This causes a test against 0 to return as FALSE. The workaround is to include a terminator token in the command string sent to the UART and check for the existence of the token rather than using szGetParam() to terminate the processing loop.
- The HI-TECH C Compiler operates on 7-bit ASCII source code. Extended ASCII characters in source code cause errors. If you need to use extended characters, enter them as \x*FF* where *FF* is the hex value of the extended ASCII character.
- When passing a structure pointer to a fastcall16 function, you may receive a warning if any of the members of the structure are uninitialized, (350) unused member. This is true even if the target function writes values to those members.

- Reusable Local Labels using the HI-TECH C compiler may only contain 1 period. Extraneous periods result in a compile error. See HI-TECH Manual section 4.3.5.5 Symbolic Labels.

Documentation

User guides and key documents are located in the `\Documentation` subdirectory of the PSoC Designer installation directory. The default location is:

C:\Program Files\Cypress\PSoC Designer 5\Documentation

Also included in this documentation folder is a documentation guide which can assist you in understanding all the documentation that is included with PSoC Designer 5.0.

Supporting documents for PSoC Designer's public-domain functionality, using "Find in Files" text search (*grep.pdf*) and the build utility (*make.pdf* and *sed.pdf*), are located in:

…\Program Files\Cypress \PSoC Designer 5\Documentation\Supporting Documents

PSoC Training

We recommend that first time users download and take PSoC Designer *Module 1: Introduction to PSoC* for free by visiting www.cypress.com/psoctraining.

Silicon Errata

The most up-to-date versions of the silicon errata are available on the web site at http://www.cypress.com/psoc and navigating to **Errata Update → PSoC Mixed-Signal Array**.

For assistance go to http://www.cypress.com or contact our Applications Team at 425.787.4814.

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