

Release Notes SRN060

PSoC Designer Version 5.0 Service Pack 1

Release Date: September 11, 2008

Thank you for your interest in PSoC Designer™ version 5.0 Service Pack 1. These release notes lists installation requirements and describe software updates and changes.

System Requirements and Recommendations

System Requirements	Minimum	Recommended
▪ Processor Speed	1 GHz	2 GHz Dual Core
▪ MB of RAM	256 MB	1 GB
▪ MB of Free Hard Drive Space	300 MB	500 MB
▪ Screen Resolution	1024x768	1280x1024
▪ CD-ROM Drive	✓	✓
▪ USB Port, preferably Open Host Controller or Universal	✓	✓
▪ Windows® 2000, XP (SP1, 2 or 3), or Vista	✓	✓
▪ Microsoft Internet Explorer 6.0 (SP1)	✓	✓
▪ .NET Framework	2.0	3.5
▪ Adobe Reader (For Viewing of .PDF Documentation)	6	9
▪ PSoC Programmer	3.00.0.92	3.00.0.92

Updates

Check <http://www.cypress.com/psocdesigner> for the latest downloads of software and documentation.

New for PSoC Designer 5.0 Service Pack 1

PSoC Designer 5.0 allows you to create chip-level (PSoC Designer) projects, or system-level (Express) projects that can also be used as chip-level projects. Included in Service Pack1 are many bug fixes and support for many new product families listed below.

Please note that in many cases, new product support may be in the beta test phase. This is called out below (beta) and indicates that production release support will follow in the near future.

New Product and Kit Support Included in PSoC Designer 5.0 Service Pack 1

The following is a list of all the new product support provided in Service Pack 1. For specific new user module and product device model numbers, see the appropriate sections below.

- CY8C20X66 Product Family (beta)
- CY7C604xx Product Family (beta)
- CY7C643xx Product Family (beta)
- OvationONS™ II (CYONS2xxx) Product Family (beta)
- OvationONS™ SLIM (CYONS2xLxx) Product Family (beta)
- CY8CLED03D and CY8CLED04Dxx Product Family (beta)

- CY8CNPxxx Product Family (beta)
- CY8CTxx110 Product Family (beta)
- CY3271-PSoC FirstTouch RF Kit Support (beta)

Installation

If you participated in the PSoC Designer SP1 beta, please uninstall PSoC Designer completely before you install this service pack. Reinstall PSoC Designer 5.0 SP1 using the full installer.

If you did not participate in the beta you may safely install SP1 without uninstalling any other Cypress provided software. You should install all programs in their default installer locations to prevent any unintended interactions due to file interactions, etc.

If an ICE-Cube is connected to the installation machine it must be disconnected and then reconnected after installing PSoC Designer 5.0 SP1.

To Install:

1. Shut down any currently running instances of PSoC Designer.
2. Download and install PSoC Designer 5.0 SP1 by running the provided installer.
3. Download and install the latest PSoC Programmer 3.00 by running the provided installer

Note: To enable some devices added by this service pack so they work with the HI_TECH compiler, it's necessary to replace the HI-TECH "psoc.ini" initialization file with the Cypress provided version. The HI-TECH version of "psoc.ini" file is found in a location similar to the following, depending on the original installation drive, compiler release, and so on:

- The file from HI-TECH to be replaced is found here:
- "C:\Program Files\HI-TECH Software\HCPSOC\PRO\9.61\dat\psoc.ini"
- The Cypress replacement "psoc.ini" file is located in the Cypress tools directory:
"C:\Program Files\Cypress\Common\CypressSemiBuildMgr\tools\psoc.ini"

Replace the HI-TECH initialization psoc.ini file with the newer Cypress psoc.ini file by renaming the HI-TECH version and then copying the Cypress version into the same directory to replace it. Devices added by the service pack will now be recognized by the HI-TECH compiler.

Part Support

PSoC Designer 5.0 Service Pack 1 provides support for the following new devices.

CY8NPxxx Product Family

Family	Device	Description
CY8NPxxx	CY8NP512-24SPI	512KB, 48-pin SSOP, 24 MHz
	CY8NP001-24SPI	1MB, 48-pin SSOP, 24 MHz
	CY8NP512-12SPI	512KB, 48-pin SSOP, 12 MHz
	CY8NP001-12SPI	1MB, 48-pin SSOP, 12 MHz
	CY8NP512-24AGI	512KB, 100-pin TQFP, 24 MHz

Family	Device	Description
	CY8NP001-24AGI	1MB, 100-pin TQFP, 24 MHz
	CY8NP512-12AGI	512KB, 100-pin TQFP, 12 MHz
	CY8NP001-12AGI	1MB, 100-pin TQFP, 12 MHz

CY8C20X66, CY7C604xx, and CY7C643xx Product Families

Name	Pin Package	Notes
CY8C20246	16-pin QFN	8k flash
CY8C20346	24-pin QFN	8k flash
CY8C20446	32-pin QFN	8k flash
CY8C20546	48-pin SSOP	8k flash, Full Speed USB
CY8C20266	16-pin QFN	16k flash
CY8C20366	24-pin QFN	16k flash
CY8C20466	32-pin QFN	16k flash
CY8C20566	48-pin SSOP	16k flash, Full Speed USB
CY8C20666	48-pin QFN	16k flash, Full Speed USB
CY7C64315	16-pin QFN	16K flash, Full Speed USB
CY7C64316	16-pin QFN	32K flash, Full Speed USB
CY7C64345	32-pin QFN	16K flash, Full Speed USB
CY7C64355	48-pin QFN	16K flash, Full Speed USB
CY7C64356	48-pin QFN	32K flash, Full Speed USB
CY7C60445	32-pin QFN	16K flash, Full Speed USB
CY7C60455	48-pin QFN	16K flash, Full Speed USB
CY7C60456	48-pin QFN	32K flash, Full Speed USB

New CY8CLED03Dxx and CY8CLED04Dxx Parts

Part Name		
CY8CLED03D01	48-pin QFN	16K Flash
CY8CLED03D02	48-pin QFN	16K Flash
CY8CLED04D01	56-pin QFN	16K Flash
CY8CLED04D02	56-pin QFN	16K Flash

Updated User Modules and Drivers

A number of chip level user modules and system level drivers are upgraded or have bug fixes in PSoC Designer 5.0 Service Pack 1. The user modules and drivers are continuously upgraded between releases to provide improved functionality. The following are lists of those user modules and drivers grouped by major categories used within PSoC Designer:

Updated and their revision numbers are included in several PSoC Designer UM categories in individual subdirectories located under the default installation directory at C:\Cypress\Common\CypressSemiDeviceEditor\Data\xxx (e.g., xxx = \STDUM, etc. subdirectory).

Updated STDUM User Modules		
AMPINV 4.3 (was 4.2)	BootLdrI2C 1.2 (was 1.1)	BootLdrUSBFS 1.2 (was 1.1)
CMP 1.2 (was 1.1)	CSD 1.3 (was 1.2)	CSDADC 1.1 (was 1.0)
DAC6 4.3 (was 4.2)	DelSig 1.2 (was 1.1)	E2PROM 1.7 (was 1.6)
EzI2Cs 1.1 (was 1.0)	I2CHW 1.6 (was 1.5)	IrDARX 2.4 (was 2.5)
LED7SEG 1.1 (was 1.0)	LPF2 2.5 (was 2.4)	OneWire 1.1 (was 1.0)
prs16 3.4 (was 3.3)	prs24 3.4 (was 3.3)	prs32 3.4 (was 3.3)
prs8 3.4 (was 3.3)	SAR6 1.5 (was 1.4)	ShadowRegs 1.1 (was 1.0)
SPIM 2.6 (was 2.5)	TachTimer16 1.1 (was 1.0)	Timer16 2.6 (was 2.5)
Timer24 2.6 (was 2.5)	Timer32 2.6 (was 2.5)	Timer8 2.6 (was 2.5)
USBFS 1.5 (was 1.4)	USBUART 1.2 (was 1.1)	BPF2 5.5 (was 5.4)

Updated PSoC_100 User Modules		
CSA 1.2 (was 1.1)	CMP 1.1 (was 1.0)	I2Cm 1.5 (was 1.4)

Updated enCoRE User Module		
E2PROM 0.2 (was 0.1)		

Updated System Level Drivers

The following are updated system level drivers. No new driver support was added in PSoC Designer 5.0 SP1.

Updated General System Level Drivers		
LOGICOUT 1.1 (was 1.0)	MPX 1.1 (was 1.0)	USBUART 1.4 (was 1.3)

Updated CapSense Express System Level Drivers		
GPIOCBUTSLIDER 1.1 (was 1.0)	GPIOCBUTTON04 1.1 (was 1.0)	GPIOCBUTTON04COMP 1.1 (was 1.0)
GPIOCBUTTON06 1.1 (was 1.0)	GPIOCBUTTON08 1.1 (was 1.0)	GPIOCBUTTON10 1.1 (was 1.0)
SLIDER10SEG 1.1 (was 1.0)		

New User Modules

Included in PSoC Designer 5.0 SP1 are several new user modules. The service pack includes user modules for configuring the power handling (PWR) and navigation functions (NAV) of the OvationONS II devices, user modules for accessing specific hardware features of the CY8CLED0xDx product family, multiple capacitive sensing methods (CSD and CSA) customized to work with new device families, and others.

New STDUM User Modules		
Name	Devices Supported	Description
NVSRAM 1.0	CY8CNP102x	Configure parallel interface between PSoC and NVSRAM. Provide API's for NVSRAM read and write.
TRUETOUCH_GESTURE 1.0	CY8CTMG110	Implements a projected capacitance touch screen on a CY8CTMG110 device with support for gestures.
TRUETOUCH_SINGLE 1.0	CY8CTST110	Implements projected capacitance touch screen on a CY8CTST110 PSoC device with support for single finger touches.
New SHAREDUM User Modules		
Name	Devices Supported	Description
CYFISPI 1.0	CY8C29/27xxx, CY8C24x94, CY8C21x34, CY8C21x23, CY8C24x43, CY8CLED02/04/08/16, CY7C638/639xx, CY7C601/602xx, CYRF69103, CYRF69213	A low level hardware interface that provides an API operating the CYRF7936 CyFi™ radio.
CYFISNP 1.0	CY8C29/27xxx, CY8C24x94, CY8C21x34, CY7C603xx, CY7C64215, CY8CLED04/08/16, CY7C638/639xx, CY7C601/602xx, CYRF69103, CYRF69213	Implements a hub or node for the Cypress CyFi™ star network protocol.
New CY8C20060 User Modules		
Name	Devices Supported	Description
ADCINC 1.1	CY8C20x66, CY7C643xx, CY7C60424, CY7C6053x, CYONS2xxx, and CYONS2xLx	Analog to Digital Converter

CSD 0.2	CY8C20x66, CYONS21L1T, and CYONS2110	An updated version of the CapSense™ Sigma-Delta User Module
E2PROMx128 1.1	CY8C20x66, CY7C645xx, CY7C643xx, CY7C60424, CYONS2xxx and CYONS2xLx	Improved over CY8C20x34 by using an on-chip temperature sensor to optimize flash memory endurance
EzI2Cs 1.1	CY8C20x66, CY7C645xx, CY7C643xx, CY7C60424, CYONS2xxx and CYONS2xLx	Supports I2C Hardware address detection in active and sleep modes
I2CHW 1.1	CY8C20x66, CY7C645xx, CY7C643xx, CY7C60424, CYONS2xxx and CYONS2xLx	Supports I2C Hardware address detection in active and sleep modes
NAV 0.2	CYONS2xxx and CYONS2xLx	Controls the optical navigation system on the CYONS2xxx and CYONS2xLx devices.
PWR 0.2	CYONS2xxx and CYONS2xLx	Configures and controls the power system on the CYONS2xxx and CYONS2xLx devices.
TIMER16 1.1	CY8C20x66, CY7C645xx, CY7C643xx, CY7C60424, CYONS2xxx and CYONS2xLx	16-bit timer.
New PPSoC User Modules		
Name	Devices Supported	Description
CMPHW 1.0	CY8CLED03Dxx CY8CLED04Dxx	Hardware Comparator
CURSENSEHW 1.0	CY8CLED03Dxx CY8CLED04Dxx	Hardware Current Sense Amplifier
DMM16HW 1.0	CY8CLED03Dxx CY8CLED04Dxx	16-bit Hardware Density Modulated PWM
DualDAC8HW 1.0	CY8CLED03Dxx CY8CLED04Dxx	Dual 8-bit Hardware Dual DAC
HYSTCTRL 1.0	CY8CLED03Dxx CY8CLED04Dxx	Hysteretic Controller

PRISM16HW 1.0	CY8CLED03Dxx CY8CLED04Dxx	16-bit Hardware PrISM
PWM16HW 1.0	CY8CLED03Dxx CY8CLED04Dxx	16-bit Hardware Pulse Width Modulator

Known Limitations for PSoC Designer 5.0 Service Pack 1

CY8C20X66/CY7C604xx/CY7C643xx Limitations

1. Problems with the debugger in combination with hardware interrupts including I²C, CMP, and Timer16 have been reported. Best performance may be achieved by using only CPUCLK = SysClk/1 settings. Some dependence on board layout has been observed. A future update to the Silicon is expected to address these problems.
 - a. I²C is operational with the following limitations:
 - i. When using the ICE-CUBE debugger, if Interrupts are used with the I2CHW User Module, the CPUCLK setting should only be used with a setting of SYSCLK/1. Suggested IMO frequencies are 12MHz and 6 MHz.
 - ii. If the I2CHW User Module is used with Polled data acquisition, no limitations exist with respect to the ICE-CUBE, or CPUCLK. See the I2CHW data sheet for a discussion of polled data acquisition.
 - iii. EZI2C only supports interrupts for acquiring data.
 - b. SPI operation.
 - i. When used with the ICE-CUBE and SPI-interrupts, CPUCLK should only be set to SYSCLK/1. Suggested IMO settings are 12 MHz or 6MHz. Problems have been reported using the SPI slave function, although a specific fault has not been identified.
 - ii. An implementation using polling for RXBufferFull or SPI_TX_COMPLETE is suggested to avoid ICE-CUBE related interrupt difficulties.
2. Setting the IMO to 24 MHz has been reported to cause debugger failures particularly in combination with the USBFS User Module.
3. The ADC User Module is not functional for some combinations of CPU clock and DataClock. The CPU clock (after clock division) must be running at least as fast as the data clock or the ADC will not function correctly.
4. The EEPROM User Module may not write properly when blocks of size less than 128 bytes are written.
5. The LED User Module may not be used on PORT4 (if it exists on the part in use)

6. CSD User Module fails as some SysClk settings

	IMO >> (in MHz)		
CPU_Clock	24	12	6
SysClock / 1	F		
SysClock / 2			
SysClock / 4			
SysClock / 8	F	F	F
SysClock / 16			
SysClock / 32			
SysClock / 128		F	F
SysClock / 256		F	F

7. CSA User Module fails as some SysClk settings

	IMO >> (in MHz)		
CPU_Clock	24	12	6
SysClock / 1	F	F	
SysClock / 2			
SysClock / 4			
SysClock / 8			
SysClock / 16	F		
SysClock / 32	F		
SysClock / 128	F		F
SysClock / 256	F	F	F

8. In order for the HiTech compiler to support some of the listed part numbers, you will have to replace the psoc.ini file in the compiler installation folder.

Replace this file:

<HI-TECH Installpath>\HCPSOC\PRO\9_61\dat\psoc.ini

with this one:

<PD50

installpath>\Cypress\Common\CypressSemi\BuildMgr\tools\psoc.ini

OvationONS™ II Limitations

- The ADC User Module is not functional for some combinations of CPU clock and DataClock. The CPU clock (after clock division) must be running at least as fast as the data clock or the ADC will not function correctly.
- The EEPROM User Module may not write properly when blocks of size less than 128 bytes are written.

PSoC Designer 5.0 SP1 ColorLock Limitations

- There is no resource tracking for High Brightness LED drivers. You must be aware of the quantity of HBLED drivers and PSoC pin limitations. Currently there are no warnings issued when too many HBLED drivers are added to your project.
- When using the 3 HBLED 700 mA Rebel driver, naming the Trigger Valuator "ColorLockTrigger" creates Transfer Function errors.

13. When assigning pins to the 700 mA Luxeon Rebel ColorLock driver, the pins must be unassigned and applied in reverse order. The driver has the pin name pse_TCS230SHARED_# S#. You must apply pin S3 first followed by S2, S1, and ending with S0.
14. For any 3-LED color mixing drivers in simulation mode, the Current Value display box displays CIE_x and CIE_y irrespective of any color space parameters.
15. If you calibrate the color sensor inside the tuner, you must restart the EZ-Color device.

CY8CLED03Dx and CY8CLED04Dx Product Family Known Limitations

16. The following user modules available in other PSoC devices are not supported by the CY8CLED03D and CY8CLED04D family of parts:

	User Module Name	Description
1.	LCD	LCD Tool Box
2.	LED	LED
3.	LED7SEG	7-Segment LED Controller

17. Pin names overlap each other in the 'Pinout Editor'. If any of the names cannot be discerned, the part datasheet may be used for required information.
18. Parameter descriptions are not available in the parameter window. The required content can be found in the corresponding User Module datasheet.
19. The configuration datasheet is not generated for projects built using the Power PSoC device. The purpose of a configuration datasheet collects all parameters set throughout the interconnect view and presents them in a html file.
20. The 'Help me choose a part' link on the device catalog points to a file that does not contain information regarding Power PSoC parts exclusively designed for lighting market. This information currently may be found at www.cypress.com
21. DMX512Rx User Module datasheet does not indicate that it is also applicable to CY8CLED03D/04D parts. The User Module is applicable to abovementioned parts and is tested.
22. The datasheets for all User Modules do not contain a block diagram that provides a high level view of its purpose in the overall design. This content will be provided in the next service pack of PSoC Designer.
23. The context menu features are disabled for Power PSoC parts. Typically right clicking a placed User Module instance in the chip level view provides user with Datasheet, Properties options. This feature is currently disabled for Power PSoC parts.

Known Problems for PSoC Designer 5.0 Service Pack 1

General Problems

Problem	Work Around
<p>1. Slow behavior in monitor mode for High Brightness LED drivers. Performance of the communication interface with the target hardware and updates of the driver GUI widgets can be slow when in monitor mode for a project that includes a High Brightness LED driver. It can take from 1 to 2 seconds for keystrokes entered in a text box to be reflected in the GUI. Values entered in the text entry box to be sent to the target hardware can take from 3 to 5 seconds to be transmitted to the target hardware and be read back and displayed in the High Brightness LED driver monitor widget. [26693]</p>	<p>No work around at this time.</p>

Problems with Chip-Level Projects

Problem	Work Around
<p>2. When cloning a project you must be aware that some devices do not share user module capabilities. If you clone a project for one device to another device certain user modules may not appear. [27409]</p>	<p>Check what user modules are available for the cloned device.</p>
<p>3. The I2CHW and EZI2Cs User Modules are unable to detect whether I²C bus pins are consumed by the CSD User Module. Therefore, it is possible to configure the I2CHW or EZI2Cs User Module to use pins already consumed by the CSD User Module. [22470]</p>	<p>Place and configure the applicable I2CHW, or EZI2Cs User Module prior to placing the CSD User Module. The CSD User Module wizard will detect that the I²C pins have been consumed.</p>

Problems with System-Level Projects

Problem	Work Around
<p>4. When Monitor is running for System-level projects, some of the GUI elements (such as menu items or dialog buttons) may not update properly or may be disabled. [27057]</p>	<p>If this occurs, stop the Monitor before initiating other activities.</p>
<p>5. The literal code transfer function does not support multiple variable declarations on a single line of code. [27225]</p> <p>Example:</p> <pre>int a, b;</pre>	<p>Declare one variable per line of code.</p> <p>Example:</p> <pre>int a; int b;</pre>
<p>6. PSoC Designer 5.0 allows you to add additional analog input drivers after adding a CSDR CapSense driver. [27385]</p>	<p>When using a CSDR driver you cannot add an additional analog driver even though this is allowed by the program.</p>
<p>7. A Discrete interface valuator cannot be an input for a TableLookup transfer function if the Discrete interface valuator's state values are not defined in the state list as an unbroken numeric sequence of constants starting at 0. [27342]</p>	<p>When defining state values, define the first state value as 0, the second state value as 1, and so on until the last state is defined. Ensure that each successive value in the list is greater than the previous value by 1.</p>
<p>8. When a State Machine transfer function valuator's name contains an underscore character (_) and an input driver, output driver, or other valuator's name is identical to the portion of the State Machine valuator's name before the underscore (ex. State Machine valuator named abc_def and LED output driver named abc), the System Level editor tool might show a transfer function relationship line between these two even though there is no relationship. The project will also fail to build. [27010]</p>	<p>Avoid using the underscore (_) character in driver and valuator names. Also avoid naming drivers or valutors with substrings of other driver and valuator names.</p>
<p>9. When a System-level project created on a system with high display resolution is open on a system with lower display resolution some of the design elements (drivers, valuator) may appear outside of the viewport. [27356]</p>	<p>Use Zoom Out to bring all design elements into the viewport. Then relocate items as necessary. Or switch to higher display resolution.</p>

Problem

Work Around

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|---|---|
| <p>10. Half-Line LCD drivers allow up to 7 characters to be entered, while Full-Line LCD drivers allow up to 16 characters. PSoC Designer 5.0 does not limit you to the number of characters that can be entered into a Half-Line and Full-Line LCD driver label edit box. The characters beyond the maximum number are disregarded by the PSoC Designer 5.0. [27343]</p> | <p>You can select the label in the Half-Line and Full-Line properties window and see the description detailing how many characters can be placed in the selected label.</p> |
|---|---|

Problems with Compilation and Debug

Problem

Work Around

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|---|---|
| <p>11. Although the Chip Level view indicates that the CY7C63803's CPU speed and sleep timer interval can be configured, PSoC Designer does not generate the applicable firmware initialization. [25756]</p> | <p>Manually add a line of code in the application program to initialize the value of OSC_CR0, the register that sets CPU speed and sleep timer interval.</p> |
| <p>12. System-level projects do not allow compiler selection before the first "Generate/Build Project" invocation. [26969]</p> | <p>Set the desired compiler to be the default PSoC Designer 5.0 compiler using Tools → Options → Build → Compiler before creating a System-level project.</p> |
| <p>13. Multiple instances of PSoC Designer and PSoC Programmer can be open at the same time, but only a single instance is allowed to access the ICE at a given time. An error message stating "ICE Unavailable" will result when instances of either application attempt to access the ICE if it is already connected. [23569]</p> | <p>Press the disconnect button in the application that is currently connected to the ICE or close it completely to free it for connection in one of the other open instances.</p> |
| <p>14. There are known problems in the debugger when viewing function parameter variables with immediate values. [25847]

For example <code>foo(2,3)</code></p> | <p>The work-around is to assign values to variables instead and then pass the variables into the function.

For example, <code>foo(a,b)</code></p> |
| <p>15. PSoC Designer 5.0 may not recognize a second ICE-Cube. [26513]</p> | <p>Go to Project → Setting → Debugger where the new ICE-Cube is listed and select it for use.</p> |

Problem

Work Around

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|--|--|
| <p>16. If you move a project from one location to another and you try to compile an individual file, the compile will fail because the compiler's path to the file is absolute. If you move the project from one location and then rebuild the entire project, the absolute file paths are regenerated and compilation will succeed. The bug only affects individual file compilation. [26059]</p> | <p>There are build files generated that include explicit paths. These files are rebuilt when the overall project is re-built. You should rebuild the entire project after copying the project before performing individual file compilation.</p> |
|--|--|

OvationONS™ II Known Problems

These items are a listing of all known issues at release. The number in brackets is a unique Cypress control number used to track each documented item listed here.

Problem

Work Around

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|---|---|
| <p>17. I/O registers banks 2 and 3 may not be displayed during debug. [21468]</p> | <p>It may be necessary to add test code to read the relevant registers into a location that is readable for debug. Fix planned.</p> |
| <p>18. The NAV and PWR User Modules do not have sample code. [29817]</p> | <p>There is no workaround. Documentation will be updated</p> |

Problems with Touchscreen User Modules

Problem

Work Around

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|---|---|
| <p>19. Touch screen projects will not build or compile unless the TrueTouch™ wizard has first been run. [30116]</p> | <p>Run the wizard and assign all pins before attempting to build and compile.</p> |
| <p>20. CY8CTST110 projects will not compile using the ImageCraft compiler. [30092]</p> | <p>Download and install either the HI-TECH Pro or the HI-TECH Lite compiler.</p> <p>HI-TECH Lite if free, while a 45-day free trial is available for HI-TECH Pro.</p> |
| <p>21. CY8CTMG110 projects will not compile using the ImageCraft or HI_TECH Lite compilers. [30092]</p> | <p>Download and install the HI-TECH Pro compiler. A 45-day free trial is available.</p> |

Problems with the CYFISPI User Module

Problem	Work Around
22. Selection of the SDIO/SCK option for the SPI Mode parameter on CY7C60113-PVXC results in a corruption of the displayed SPI pin assignments. [22159]	After building the project, the pin assignment corrects itself. The defect in the pin assignment display does not propagate to generated source code.

Considerations Using HI-TECH as the Default C Compiler with System-Level Designs in PSoC Designer 5.0 SP1

This section refers to a project that was either done originally in PSoC Express 3.0 or using PSoC Designer 5.0 in the system-level mode (formerly called Express) to generate the design.

- When recompiling an old project with the HI-TECH Lite C compiler, it is unlikely that you will get an error due to any change in compilers. This is because of the standardized and modular programming model of PSoC Express. However, if the base device runs out of available ROM space, a compile error does occur. To remedy this condition:
 - Choose a device with more resources
 - Upgrade to the Pro version of the HI-TECH C compiler
 - Revert to the ImageCraft C compiler
- Compiler settings are saved in individual PSoC projects. When you open an existing project that you built with the ImageCraft C compiler, the project is built with ImageCraft. To change this behavior, you must switch the compiler vendor to HI-TECH (**Build → Select Compiler Vendor** for *project*) for all previously built projects. There is a default compiler selection as well (**Build → Select Default Compiler Vendor**). The default compiler applies to all new projects, not previously built projects.
- The default compiler selection is applied to a project when it is created. After creating a new project, the compiler vendor cannot be changed until the project is built once. Changing the default compiler vendor with a project open does not alter the compiler setting for the open project.
- Because of the amount of code and floating point math required, ColorLock and ColorMix driver operations may exceed the timing of the 64Hz system loop timer, resulting in "Free Run" operation. When compiled with the HI-TECH Lite C Compiler, the behavior of the system may appear to be sluggish when compared to the same code compiled using the HI-TECH Pro C Compiler. The Lite compiler produces less optimized code than Pro, resulting in longer execution time.
- Under **Project → Settings → Build → Compiler** with HI-TECH C compiler selected as the default, there is a button that allows you to switch between HI-TECH Pro mode and HI-TECH Lite mode. The correct control code will be entered by PSoC Designer 5.0 automatically when the button is pressed.

Considerations Using HI-TECH as the Default C Compiler with Chip Level Designs in PSoC Designer 5.0 SP1

This section refers to a project that was either created originally in PSoC Designer 4.x or using PSoC Designer 5.0 exclusively in the chip level mode to generate the design. The issues relate to PSoC Designer 5.0 with version 9.61 of the HI-TECH C compiler. For additional help with the HI-TECH compiler, see the docs folder in the HI-TECH installation directory.

- Opening projects created with PSoC Designer version 4.1 or earlier and building them with the HI-TECH compiler may result in the loss of any ImageCraft custom compiler/linker settings.
- The `UART_szGetParam()` function for the UART User Module currently does not function as expected using the HI-TECH C Compiler. The function is supposed to return a null pointer if there are no more parameters left. Under certain circumstances, when returning a null pointer through a fastcall16 function such as `szGetParam()`, the pointer is returned to C as a 16-bit pointer with the most significant bit set to 1. See HI-TECH Manual Section 3.3.11.2 Data Pointers. This causes a test against 0 to return as FALSE. The workaround is to include a terminator token in the command string sent to the UART and check for the existence of the token rather than using `szGetParam()` to terminate the processing loop.
- The HI-TECH C Compiler operates on 7-bit ASCII source code. Extended ASCII characters in source code cause errors. If you need to use extended characters, enter them as `\xFF` where `FF` is the hex value of the extended ASCII character.
- When passing a structure pointer to a fastcall16 function, you may receive a warning if any of the members of the structure are uninitialized, (350) unused member. This is true even if the target function writes values to those members.
- Reusable Local Labels using the HI-TECH C compiler may only contain 1 period. Extraneous periods result in a compile error. See HI-TECH Manual section 4.3.5.5 Symbolic Labels.

Documentation

User guides and key documents are located in the `\Documentation` subdirectory of the PSoC Designer installation directory. The default location is:

C:\Program Files\Cypress\PSoC Designer 5\Documentation

Also included in this documentation folder is a documentation guide which can assist you in understanding all the documentation that is included with PSoC Designer 5.0.

Supporting documents for PSoC Designer's public-domain functionality, using "Find in Files" text search (*grep.pdf*) and the build utility (*make.pdf* and *sed.pdf*), are located in:

... \Program Files\Cypress \PSoC Designer 5\Documentation\Supporting Documents

PSoC Training

We recommend that first time users download and take PSoC Designer *Module 1: Introduction to PSoC* for free by visiting www.cypress.com/psoctraining.

Silicon Errata

The most up-to-date versions of the silicon errata are available on the web site at <http://www.cypress.com/psoc> and navigating to **Errata Update → PSoC Mixed-Signal Array**. For assistance go to <http://www.cypress.com> or contact our Applications Team at 425.787.4814.

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