State of the Art of Bipolar Semiconductors for Very High Power Applications

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Abstract

The outstanding performance and technologies of state-of-the-art high power thyristors and diodes for applications like HVDC, FACTS or large drives are described.
HVDC transmission systems up to 11 GW and voltages of ±1100 kV are planned **[1]** and drives in the power range up to 100 MW and more are designed and built using those power semiconductors. Different features (e.g. integrated protection functions) or technologies like Low Temperature Sintering (LTS) for highest rating and surge currents at highest blocking voltages are presented. In addition, a new voltage definition according to application demand is introduced to decrease the number of devices in series connections. Finally, the 6-inch Light Triggered Thyristor (LTT) is presented **(Fig. 1)**.

1. Application driven demands for Bipolar Semiconductors

To enable economic transmission of large amounts of electrical energy from power generation centres to load centres High Voltage Direct Current (HVDC) transmission using Line Commutated Converters (LCC) has been established as the preferred technology. Although in recent years Voltage Sourced Converters (VSC) with IGBTs have gained increasing importance, thyristor devices are still favoured for applications in which ultra high voltages and high currents have to be controlled, because they have the best performance in terms of on-state losses and symmetric blocking capability. Thyristors are also used in Static Var Compensators (SVCs), like Thyristor Switched Capacitor (TSC) and Thyristor Controlled Reactor (TCR). In addition, bipolar semiconductor discs are applied as bypass thyristors (Crow Bar) or freewheeling diodes in HVDC VSC.

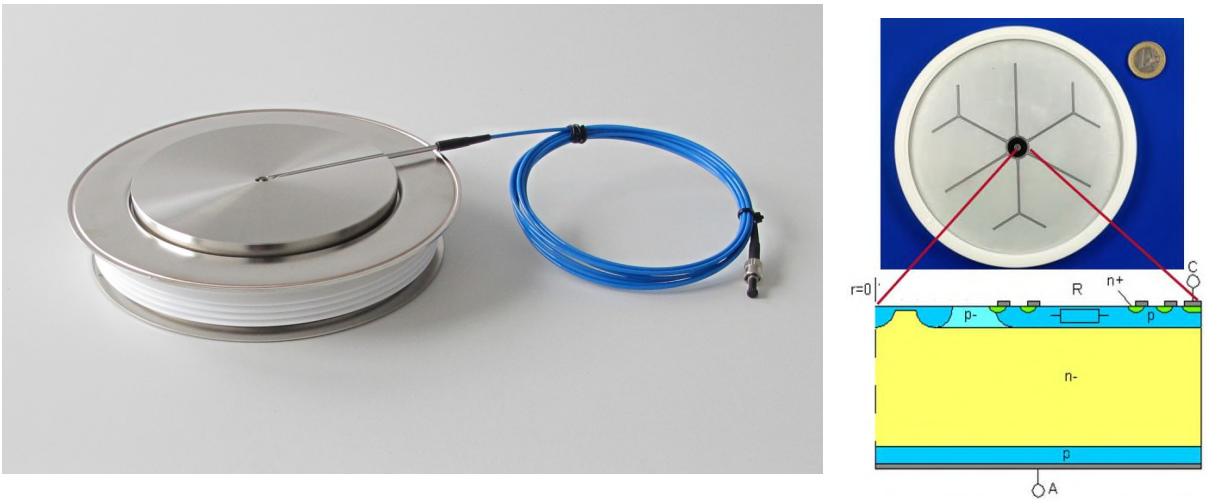

Fig. 1: 6-inch Light Triggered Thyristor LTT with integrated self-protection functions (a) V_{RRM}=9.5 kV; I_{DC}=6250 A; I_{TSM}>140 kA and corresponding Semiconductor Wafer (b)

While HVDC transmission is becoming more and more important and installed transmission capacities are growing on a rapid pace many customers are asking for lower costs along with increased reliability and availability, aiming also at extended maintenance periods. A feasible way to meet both goals is to reduce the complexity of the thyristor converters. This can on one hand be achieved by reducing the number of series connected elements which will also

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reduce the number of auxiliary components at the thyristor levels. The required higher blocking voltage capability of the thyristors can not only be implemented by increasing the thickness of the silicon wafers (which would also increase the losses) but also by more realistic definition and application of testing procedures. The real voltage wave shapes in an operating converter are non-sinusoidal containing steep voltage changes as well as repetitive transient voltage peaks caused by current extinction of thyristors. Testing is usually performed using pure sine wave voltages, which are easily available in test facilities, with amplitudes corresponding to the ones of the transient stresses. This procedure leads to higher stress of the tested elements than in the actual application. The use of more realistic wave shapes for thyristor testing helps to enable better utilization of thyristor voltage capabilities. Corresponding investigations have been performed leading to a test procedure using a sine wave blocking voltage with a superimposed short peak voltage **"Pulse Peak Measurement" (chapter 3)**.

Another possibility to reduce complexity of the valves is to integrate electronic functions into the thyristor which up to now are implemented in the valves as separate electronics boards. After eliminating the need for electric trigger circuits and external overvoltage protection as well as dv/dt protection now the last issue, namely the protection against forward transient voltages during the recovery period **(Forward Recovery Protection FRP)**, is solved.
A combination of thyristor modification together with application of an additional optical trigger pulse is used to replace the previously necessary electronics board (**chapter 4**). To omit this external electronic circuitry saves costs and improves the reliability ("Whatever is not present cannot fail").

For Ultra high power UHVDC links (e.g. 10 GW, 800 kV), DC-transmission currents of 6250A and very high surge currents are required. In case one thyristor valve loses its blocking capability the valve which fires next in the same half bridge will initiate a two phase transformer short circuit. Due to the low impedance of the high power transformers necessary for this kind of links short circuit currents will increase from 50kA in the "conventional" 800kV links to > 60kA in this future application.
To meet this requirement and to simultaneously improve performance and reliability of the thyristor converters the 6-inch electrically triggered thyristor **[2]** used up to now was enhanced to a **6-inch Light Triggered Thyristor**. While meeting the nominal DC current requirements **(6250 A)** as well as the short circuit current requirements **(>70 kA) (Tab. 1, chapter 5.1)** the voltage withstand capability could be maintained (in fact, it could even be slightly increased to $\mathbf{V_{RRM}=9.5\ kV}$). Typically, low loss design and technology (on-state and turn-off) by optimised charge carrier lifetime control are becoming more important for advanced HVDC transmission **(chapter 5.2)**.

2. Key Design and Technology of Bipolar Semiconductors for Ultra High Power Applications

2.1. Integrated Protection Functions for Overvoltage and dv/dt

Full advantage of the Light Triggered Thyristor is achieved, when safe fault triggering structures are introduced which protect the device in case the limits of the forward breakdown voltage or voltage rate of rise dv/dt are exceeded. The integrated overvoltage protection function realised by Break Over Diode (BOD) provides an efficient and reliable controlled turn on when the forward blocking voltage reaches values between 8 kV-9.5 kV **[3]**. Apart from the overvoltage protection function also a dv/dt protection function was integrated into the thyristor **[4]**.

2.2. Key Parameters for Silicon Wafers

State of the art silicon wafer technology enables the production of highly pure und defect free n-type float zone silicon wafers needed for high blocking voltages up to 9.5 kV. These wafers are doped via neutron transmutation to obtain a homogeneous resistivity distribution across the entire wafer in the n^--zone **(Fig 2a)**. The resistivity is in the range of 430 Ω·cm to

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500 Ω·cm. The typical standard deviation for a pre- processed wafer is < 1%.

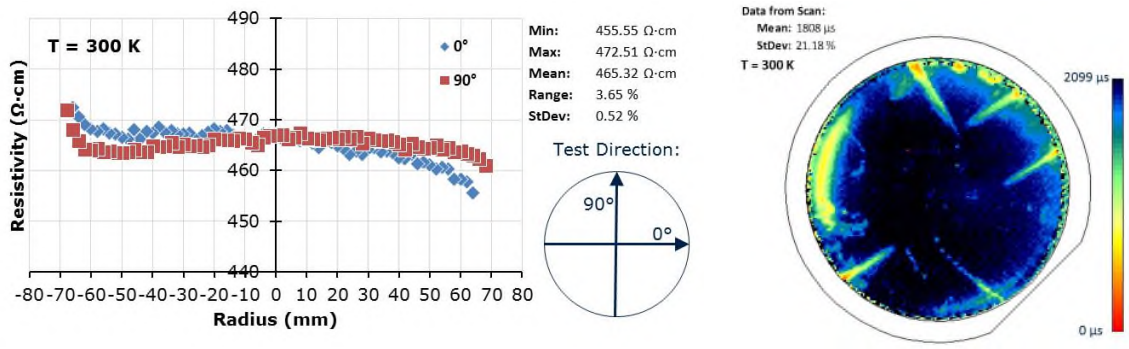

Fig. 2: Lateral distribution of resistivity (a) and distribution of carrier lifetime (ELYMAT) (b) of a pre- processed 6-inch wafer (thickness: ~1.5 mm)

An extremely low concentration of impurities in the base region of power devices is very important to obtain low leakage currents and on-state voltages and to enable well-defined control by means of lifetime controlling like electron irradiation. Therefore, high-purity processing in diffusion is absolutely necessary.

Vacancy agglomerates such as D-defects in the starting material and, consequently, their decoration by impurities have to be avoided by using a pre-processing step like oxidation or $POCl_3$ diffusion **[5]**. Wafers, which are pre-processed in this way show a very high carrier lifetime up to 2000 µs **(Fig. 2b)** and therefore a reproducible behaviour after lifetime controlling with respect to a defined relationship between reverse recovery charge and on-state voltage.

In order to achieve the highest possible active device area for the cathode and anode, resistivity and lifetime need to be very homogeneous up to the very edge of the wafers, even after the diffusion.

2.3. Low Temperature Sintering Technology (LTS)

The Low Temperature Sintering Technology (LTS), which is based on the principle of diffusion welding ensures, compared to a Free Floating (FF) interface, an excellent thermal contact between silicon and molybdenum carrier due to the metallurgical interface. Therefore the maximum operating temperature can be raised. Surge current capability (I_{TSM}), especially needed for HVDC applications, as well as blocking capability (V_{RRM}) and long term blocking stability increase significantly **[2]**. This can be proven as follows:

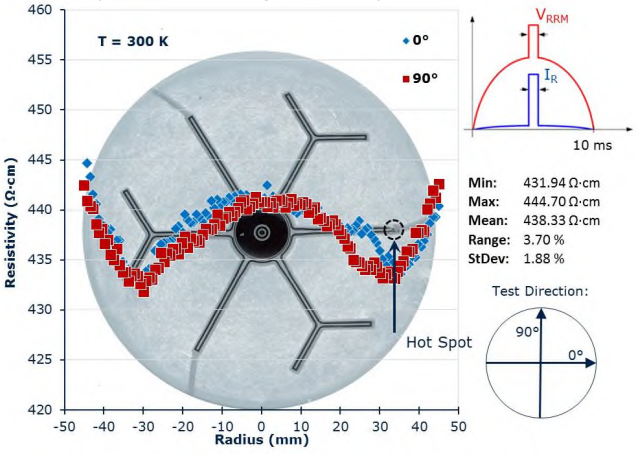

Fig. 3: Metallized surface of a 4-inch LTT and corresponding distribution of resistivity

4-inch 8 kV Light Triggered Thyristors have been purposely tested to destruction in order to evaluate the maximum blocking capability. The device **(Fig. 3)** had been exposed to a very high repetitive reverse voltage stress for several seconds at 50 Hz and a temperature of 373 K before it failed. The applied voltage waveform is composed of a base sine wave with chosen amplitude of 8 kV, superimposed with a voltage peak of 2.2 kV and a pulse width of 300 µs. This represents a V_{RRM} of 10.2 kV. The blocking current at the voltage peak reached very high values between 2 A and 12 A.

The thyristors did not fail as one would expect in the junction termination region, which is outside of the metallized wafer and

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not shown in Fig. 3, but they failed in the p-base at the end of a gate finger. This hot spot is caused by a local thermal runaway which is accelerated by the lack of thermal coupling between gate finger area and the contact disc and by the reduced blocking capability in the wafer area around the minimum of resistivity.
To confirm this very high reverse blocking voltage capability, about 1800 devices of 4-inch 8 kV LTTs were stressed successfully with a repetitive peak reverse voltage V_{RRM} of 9.6 kV@RT and 10.0 kV@373 K, in both cases with a base sine wave of 8.0 kV. The test period was 6 s, which corresponds to a number of 300 surge voltage pulses.

This outstanding periodic blocking voltage capability can only be reached by means of LTS technology, where the whole wafer including the junction termination is bonded with the molybdenum carrier and therefore the power loss during high reverse current flow is sufficiently dissipated.

3. Pulse Peak Test

The voltage stresses for thyristor applications are determined by periodic and non-periodic voltage stresses defined in IEC 60747 **(Fig. 4a)**. The stress caused by the fundamental line voltage is superimposed by periodic voltage peaks, such as commutation peaks within the converter and other sporadic events, e.g. switching over-voltages.

In the application, the width of the peaks is only a few hundred microseconds. Nevertheless these peaks are the major design criteria for the blocking voltage design of the thyristors because the working voltages V_{DWM} and V_{RWM} are typically in the range of only 40 % to 60 % of that peak voltage stresses.

Traditionally the established procedure is to test the maximum periodic blocking voltage of a thyristor at 50 Hz half sine wave (10 ms) routine production-test.

For this reason a new waveform for blocking voltage test is introduced in order to meet precisely the requirements of the application. **(Fig. 4b)**

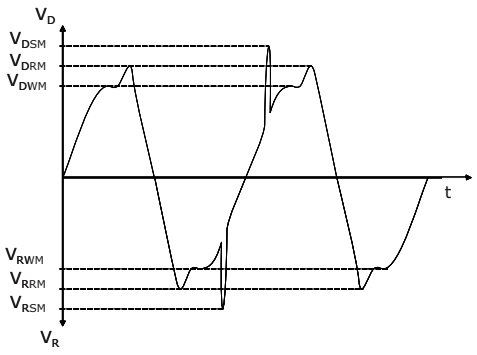

Fig. 4a: Typical blocking voltage wave forms in thyristor applications as defined according to standard IEC 60747

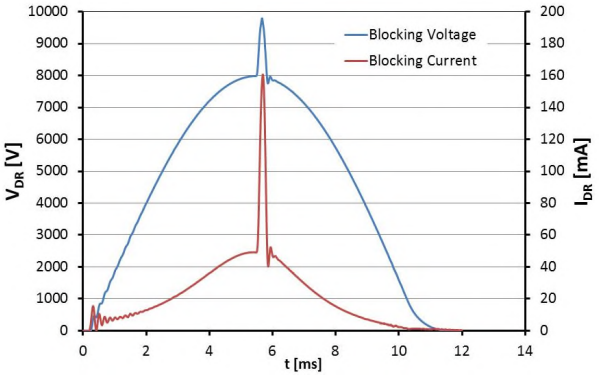

Fig. 4b: Measured blocking voltage and blocking current of a V_{RRM}=9.8kV thyristor according to new routine blocking test at T_{vj}=125°C

Fig. 4b as an example shows the blocking current of about 50 mA at blocking voltage of 8.0 kV, which is the chosen amplitude of the base voltage sine wave. This base sine wave is now superimposed by a surge voltage with higher amplitude, but with a short pulse width. The blocking current is allowed to rise significantly which enables higher repetitive peak surge voltages V_{DRM} and V_{RRM}. A very high peak surge voltage of 9.8 kV with a pulse width of e.g. 300 µs is reached.

Some thyristor manufacturers use a 60% fundamental sine wave (10 ms) to test their devices. However, to ensure a high level of inherent voltage withstand capability, which is especially present when using press pack LTS devices, a higher level of e.g. 80 % of the new defined pulse peak V_{DRM} or V_{RRM} values is recommended. The proposed combination of the high level fundamental sine wave and the superimposed pulse peak stress applied during its routine test to each thyristor allows for a reliable operation of these devices in customers applications under all relevant voltage stress conditions with a sufficient safety margin.

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Benefit for the applications: The number of series connected devices and corresponding components and thus the overall system cost can be significantly reduced, if the blocking voltage is increased from 8 kV to 9.5 kV. The on-state losses are not increased, since the pulse peak tested devices do not use a thicker silicon wafer.

4. Forward Recovery Protection (FRP)

A conventional thyristor is vulnerable during recovery time, because the middle p-n junction needs a certain period of time to reach its full blocking capability. If a forward voltage pulse occurs during this recovery time t_a, the response of the thyristor depends on the amplitude, the dv/dt, the duration, and the exact moment of the start of the voltage pulse. Most critical is the case, when large regions of the device have fully recovered and only a small part at the main cathode area is turned on by the voltage pulse. This may lead to current filamentation and may destroy the device. In order to avoid such a destructive failure, HVDC thyristors are protected by an external PC-board called a Recovery Protection Unit (RPU) that monitors the voltage across the device and generates a trigger pulse in case of any critical events.

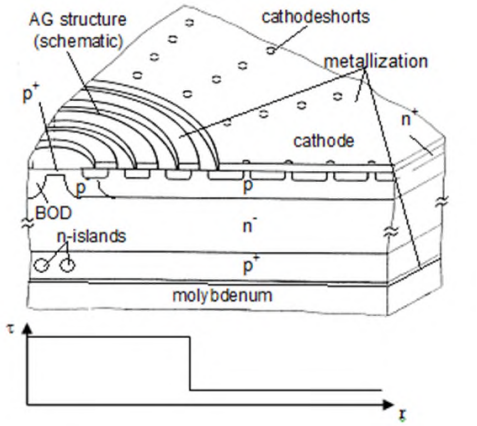

Fig. 5: Schematic sketch of the LTT and lifetime distribution $\tau(r)$ at a radial cross section **[4]**

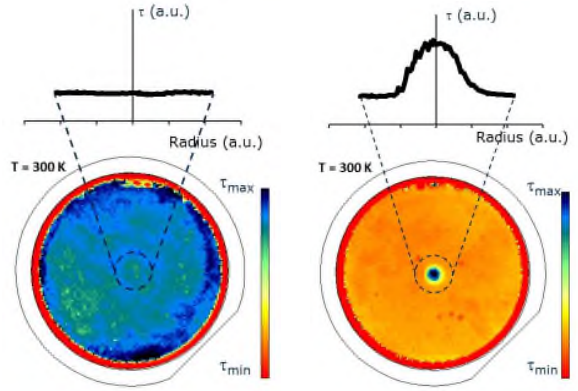

Fig. 6: Lifetime mapping (ELYMAT) of the cathode area of a 5- inch 8kV LTT without (a) and with FRP (b) after irradiation and appropriate preparation

4.1. Integrated Forward Recovery Protection

The protection can also be realized by an integrated FRP. Two crucial measures have to be combined:
Firstly, the distribution of the charge carrier lifetime has to be modified such that it is reduced in the main cathode area of the device compared to the amplifying gate (AG) region **(Fig. 5)**. This measure protects the initial phase of the recovery period, up to about 300 µs to 400 µs after commutation.

Secondly, to cover the remaining time of the recovery period, up to about 1000 µs, more carriers must be generated or injected, e. g. by implemented phosphorus islands in the p-emitter of the inner AG structure **[4]**.

However, up to now it has not yet been possible to manufacture such devices with sufficient reproducibility. Therefore, another solution has to be found based on this principle **(chapter 4.3.)**

4.2. Technological Preconditions and Wafer Design for New FRP

The locally increased lifetime in the gate centre can be implemented by using a metal mask during electron irradiation.

The 2D lifetime mappings of conventional 5-inch 8kV LTT with integrated BOD and dv/dt protection **(Fig. 6a)** and with the new FRP **(Fig. 6b)** based on a modified lifetime in the centre of the gate are compared.

The lifetime had been adjusted properly by electron irradiation at 10 MeV to meet the HVDC requirements for the dynamic characteristics, in particular the reverse recovery charge and the circuit commutated turn-off time. In the centre within the region of the gate very high lifetimes were achieved, which is very close to the conditions prior to irradiation.

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4.3. New Forward Recovery Protection by an Additional Light Pulse

The prevailing concept of FRP only triggers when a critical surge voltage occurs. In this case an additional light pulse is immediately generated by the Recovery Protection Unit (RPU). Due to the long transit time of the light pulse the RPU has to be placed near the thyristor.

In contrast, the idea behind the New FRP concept is the combination of a technological measure for realizing a higher lifetime in the amplifying gate (AG) of the thyristor **(chapter 4.1 and 4.2)** and a modification of the optical triggering on the user side.

The new FRP concept is based on an additional periodic light pulse which is applied to the LTT at a certain time t_{LI} after current extinction **(Fig. 7)**. The protection light pulse is not only generated on demand, but always during the whole operating time. It generates charge carriers in the optical gate with its higher lifetime which will safely turn on the thyristor only when a fault surge forward blocking voltage pulse occurs. Thus, the RPU and related auxiliary components are not needed for the new FRP concept.

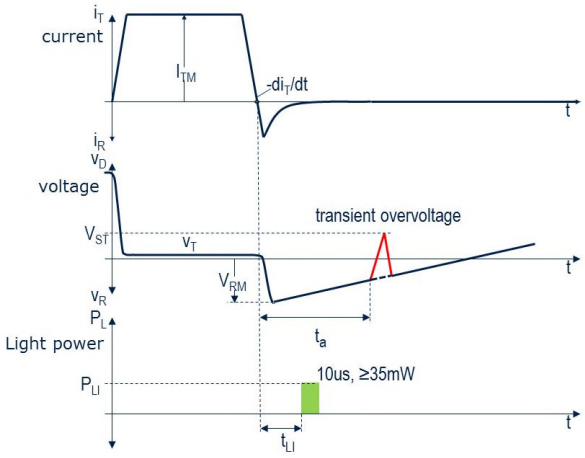

Fig 7: New FRP light pulse scheme

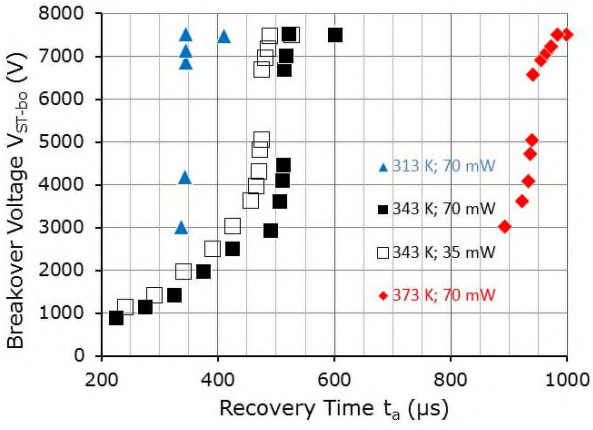

Fig. 8: FRP Robustness Test of one device at different test conditions

During the verification of the new FRP with a large amount of 8 kV LTTs, all components were charged with a bias current (I_T=3kA). The time between current extinction and the application of the protection light pulse, t_{LI}, was adjusted to a value, that represents the most severe protection condition. The smallest time t_{LI}, taking the application jitter of the light pulse into account, was chosen.
Pre-examination on insufficiently protected components had been done which made sure that the tested devices are destroyed (surge voltage V_{ST}=7.5 kV, dV_{ST}/dt= 500 V/µs to 1000 V/µs). Most critical to a thyristor when it is turned on unexpectedly during its recovery time is the height of the current level at the first few microseconds. The current waveform corresponds to that of a di/dt event with a very high current rate of rise in the range of 3 kA/µs. If the thyristor is not turned on in the defined area within the inner AG region, the thyristor will surely be destroyed by such an inrush current.

While the amplitude of the surge voltage V_{ST} applied to the thyristor during its recovery period remained constant at about 7.5 kV, the amplitude of the voltage that the thyristor was able to block till breakover $V_{ST\text{-}bo}$ was influenced by different parameters **(Fig. 8)**. Those parameters are t_a, the time between the extinction of the bias current and the beginning of the surge voltage, the temperature and the light power P_{LI}.

At breakover voltages below 3 kV $V_{ST\text{-}bo}$ increases slowly with increasing t_a. There are still enough excess charge carriers in the whole thyristor area to turn on the thyristor at even smaller values of V_{ST}. Once the residual charge is almost emptied, at certain t_a above approximately 3 kV there is an abrupt steep increase in $V_{ST\text{-}bo}$ up to the maximum blocking voltage. In this time range, it is crucial whether there are enough charge carriers, which are increased by the additional light pulse within the optical gate for a safe turn on by FRP.

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A study on several hundred 5-inch LTTs tested at a fixed temperature and light power resulted in a spread of the time for this abrupt increase of the breakover voltage of about 200 µs. Therefore it is assumed that in case of a fault event in a converter valve only single thyristors will be triggered by FRP, but never all at once.

For all tested parameters (t_a,T and P_{LI}) it could be demonstrated by this Robustness Test **(Fig. 7 and 8)**, that all devices were successfully protected by the new FRP method against surge voltages during the recovery time.

Even if P_{LI} is reduced to 35 mW, the FRP still worked sufficiently, stating, that there is a huge margin for tolerances of the light power due to the individually different power level of the laser diodes used as light sources and the other optical components. On the other side, the injected light power for the protection pulse must not take arbitrarily large values because it has a direct impact on the circuit commutated recovery time t_q of the thyristor. P_{LI} has to be chosen in a range, that t_q does not increase to undesired values e.g. above 400µs.

If not triggered by the additional protection pulse within the recovery period, LTTs with New FRP have the same behaviour as the previous ones. They are 100% backward compatible without restriction and can be used in existing applications where the new FRP-concept has not yet been applied. The increased carrier lifetime in the gate centre is only effective, if the LTT is illuminated with an additional protective light pulse during its recovery time.

5. 6-Inch Light triggered Thyristor

5.1. Surge Current Capability at Highest Blocking Voltages

Tab. 1: I_{TSM} of 3 different surge current wave forms; Clamping force and junction temperature before surge were 135 kN and $T_{vj,max}$ = 90°C

Pulses:	Single	Single	Triple
Waveform	sin	1-cos	3 x (1-cos)
V_{DM}:	0 V	> 5 kV	0 V
V_{RM}:	0 V	> 5 kV	> 2,0 kV
t_p:	10 ms	16,5 ms	16,5 ms
I_{TSM}	> 140 kA	> 74 kA	> 70 kA

The peak single pulse surge current with reapplied voltage for the 6-inch 9.5 kV Light Triggered Thyristors has been tested. It subjects to the temperature dependent forward voltage blocking capability and reaches more than 70 kA **(Tab. 1)**. No destruction or undesired forward voltage triggering occurred. The corresponding peak single pulse current (t_p = 10 ms) reaches very high values of more than 140 kA **[2]**.

5.2. Capabilities of Existing and Improved Technologies

The impact of technological measures on the performance of thyristors can be clearly represented by the technology curve of turn-on voltage V_T and the reverse recovery charge Q_r, which can be described by the following approach $Q_r = (V_T - V_{ref})^m \times 10^b$ **(Fig. 9)**.

This also applies to a comparison between different manufacturers. For example: A reduction in the silicon thickness is very beneficial to both parameters, so that the corresponding technology curve shifts towards smaller V_T and Q_r values. Of course, this makes sense only if the associated reduction of the blocking capability, which is determined by the silicon thickness, is acceptable.

More interesting, however, is an evaluation of measures which have, at a fixed silicon thickness, meaning without this significant negative compromise in the blocking capability, a favourable effect on V_T and Q_r. Controlling of carrier lifetime by means of high-energy electron irradiation (4 MeV and 10 MeV) is a usual procedure, whereby a higher energy shows a more advantageous effect on the technology curve **[6]**. **Curve B** of Fig. 9 shows the graph for a 6-inch 9.5 kV LTT when the components were treated only by electron irradiation at 10 MeV.

Further improvement **(Curve A)** can be achieved by a combined irradiation with electrons and light ions to locally reduce the carrier lifetime on the anode side. This improves the turn-

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off behaviour while still maintaining low on- state voltage (> 0.05 V is gained at fixed Q_r).

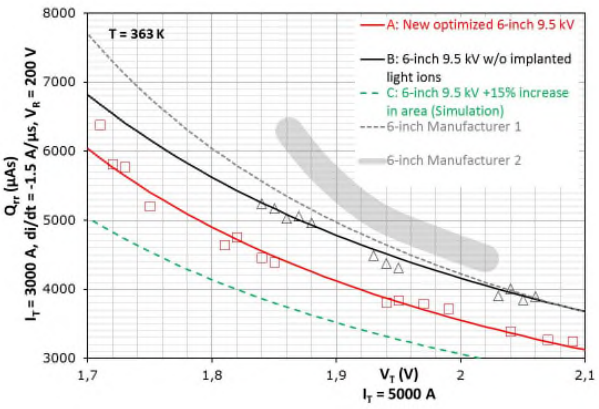

Fig 9: Trade- off curves between V_T and Q_r for different technologies and manufacturers

Finally, **Fig. 9** shows currently available curves of 6-inch devices of other manufacturers for UHVDC thyristors. The abscissa shows the on-state voltage tested at I_T=5kA due to availability of data of other manufacturers. Usually 6-inch devices are measured at a current of 6 kA or slightly above. The same does apply to those measurement conditions for Q_r given in Fig. 9, too.

6. Summary and Outlook

The improvements in thyristor technology described will contemporarily lead to more efficient HVDC thyristor valves.

The 6-inch-LTT is ready for application in all future transmission projects with DC-currents of 5000 A to 6250 A considerably reducing the complexity of the valves by eliminating electrical trigger and protection functions. Using the pulse peak method for routine testing of the voltage withstand capability will enable utilization of 9.5 kV reverse blocking capability. This enables a reduction of the number of series connected elements in a valve or at least to keep the number of devices constant if voltage stresses on single elements increase due to higher stresses of the valves at increased currents up to 6250 A. The increased blocking capability in line with the high current and surge current capability (140 kA/70 kA) due to the Low Temperature Sintering Technology (LTS) makes it possible to cover the whole range of feasible applications of 6-inch-thyristors with one single device. Other manufacturers need to use different classes of blocking voltages to cover the individual current and voltage requirements.

The integrated forward recovery protection function (FRP) has been successfully verified during routine testing of several hundred LTTs. As all other features of the thyristor remain unchanged the FRP function can now also be implemented in all other types of LTTs.

With completion of this step only three types of LTTs (4-, 5- and 6-inch with 9.5 kV reverse blocking voltage capability) will be available to cover the whole power and voltage range of HVDC transmission technology without the need for any electrical triggering or protection function leading to simple and reliable thyristor valve design.

Further improvement of the new 6-inch 9.5 kV/6250 A device can be reached by increase of active cathode area by about 15 % using a improved junction termination **(Fig. 9, Curve C)**.

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