Slew rate control of discrete IGBT and CoolMOS reaches targets far beyond the gate resistor regime

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Abstract

The control of power semiconductors with respect to turn-on is usually a matter of the gate resistance selection. This paper proposes a different way of gate turn-on by utilizing a current source, which charges the gate structure of MOS-controlled power transistors with a constant current. This results in an improved controllability towards slower turn-on in terms of d*i*/dt. Double-pulse measurements show the behavior during turn-on of a selected reverse conducting IGBT and a CoolMOS transistor with fast body diode. The results are compared to a standard gate driver including various gate resistors.

1. Introduction

High slew rates of IGBT´s collector-emitter voltage during PWM operation in motor drive inverters cause displacement currents over the parasitic capacitance of the motor to protected earth. These currents dominantly flow through the bearings, which leads to an accelerated aging of the bearings. This is a well known failure mechanism and explained in [**1**]. The aging therefore is a function of the switching frequency of the inverter as well as of the switching speed of the inverter´s IGBT. The less switching instants the less current is being measured. The same effect has the slower ramping of the collector-emitter voltage of IGBT. The slower the turn-on and turn-off, the less current flows through the bearings. Switching slowly is always correlated with increased switching losses. This measure is therefore not preferred in combination with high switching frequency.

The target is to reduce the switching frequency and to tune the switching processes towards low swiching speed for all applications where high availability or little maintenance is a high value. The dominant application for these considerations is room air-conditioning. The compressor of these systems incorporates the motor encapsulated inside the compressor case. Maintenance of the motor is not possible at all.

It is common sense that a slow switching speed by gate resistance variation also affects the turn-on propagation delay in a negative way. A gate resistor value of several 100 Ω results in turn-on propagation delays of 100 ns or even more [2].

A different method to turn-on power transistors is investigated in this paper. The turn-on is controlled by a constant current instead of a constant voltage and gate resistor. This technique was formerly introduced with large power modules, like the 600A/1200V half bridge module FF600R12ME4 from Infineon, with excellent results concerning controllability of d*v*/dt at turn-on ([3], [4], [5]). The method is now applied to low current rating discrete reverse conducting IGBT IKD03N60R and CoolMOS™ IKD65N1K4CFD transistors. The turn-on method is explained in detail and the results are discussed and compared with a standard gate driver.

ISBN 978-3-8007-3924-0

2. Turn-on scheme with gate current control

The new gate current control is implemented in Infineon´s gate driver IC 1EDS20I12SV. It divides the turn-on process into three sections according to in Figure 1: a). The first section t_0 to t_1 is the charging of the gate from 0 to a defined value in the range lower than the gate-emitter threshold voltage of the power transistor, which results in $v_{ge} < v_{ge(th)}$. This section is called the pre-boost section and lasts for a fixed duration of t_{PRB} = 135ns. The preboost current level I_{PRB} during this phase is adjustable for each individual IGBT type. The second section t_1 to t_3 is the gate turn-on section. The instantaneous constant gate drive current I_{gg} can be adjusted within 11 different values. The IGBT gate voltage passes the Miller voltage level during this time. The practical application of the device proposes a smaller turn-on gate current I_{gg} compared to the preboost current I_{PRB}. It is possible to achieve even larger turn-on currents I_{gg} than the preboost current I_{PRB}. This is displayed in b) within **Figure 1** Finally, the gate is fully charged up to the desired gate voltage level in section 3 (t_3 to end).

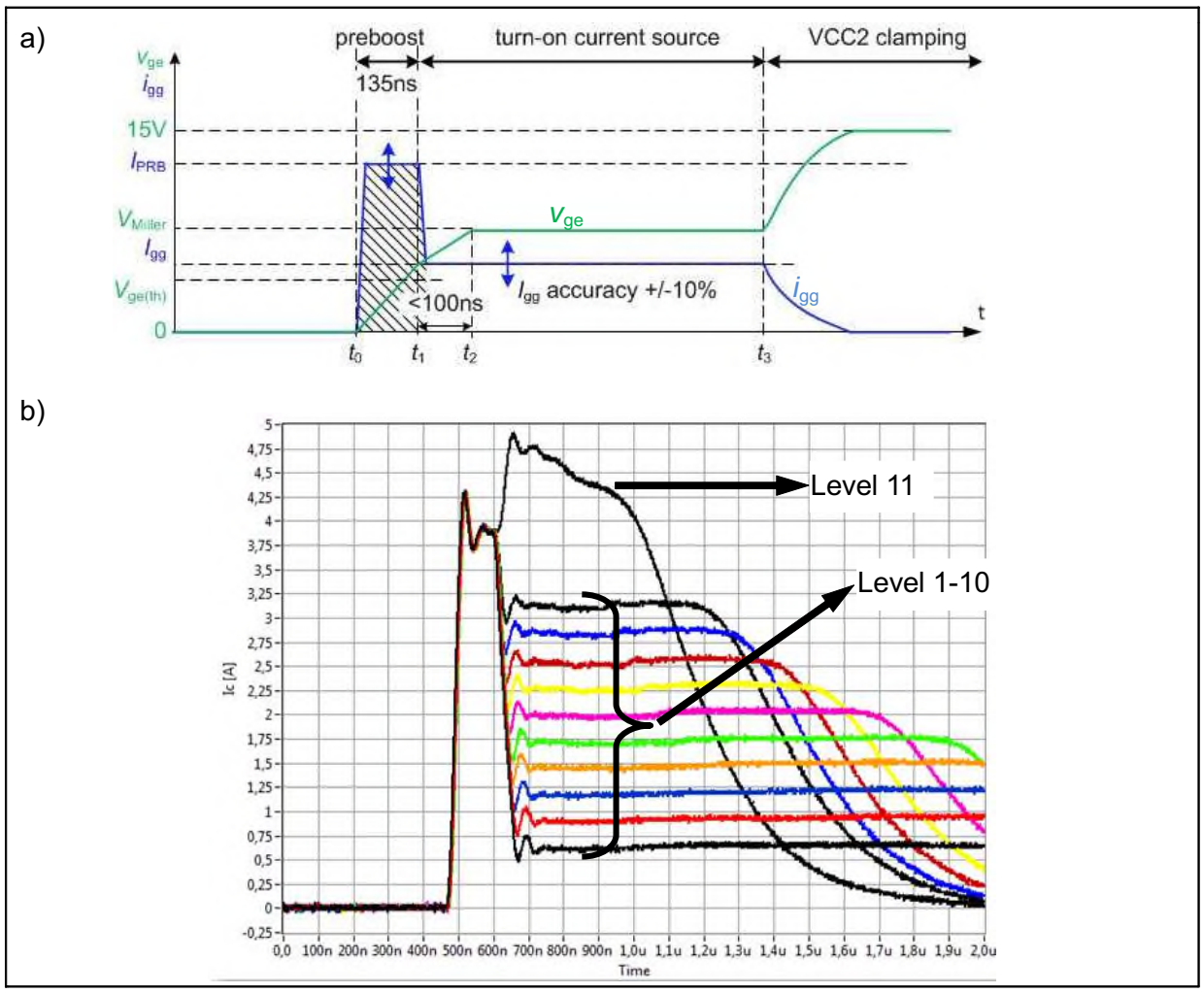

Figure 1: The three phases of a turn-on process with (a) theoretical waveforms for gate current (blue) and voltage (green) and (b) measurement example of gate currents for speed levels 1-11 [4]

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The preboost phase is not used for the measurements in this paper for simplicity reasons, as only the turn-on energy E_{on}, the di/dt and dv/dt are of interest here. Only the turn-on current is applied, which results in a long turn-on propagation delay time, when using the current source method for turn-on.

The IC controls the gate current by means of closed loop current source circuit, which consists of a p-channel MOSFET BSD314SPE and a current sense resistor.

3. Turn-on evaluation of a reverse conducting IGBT

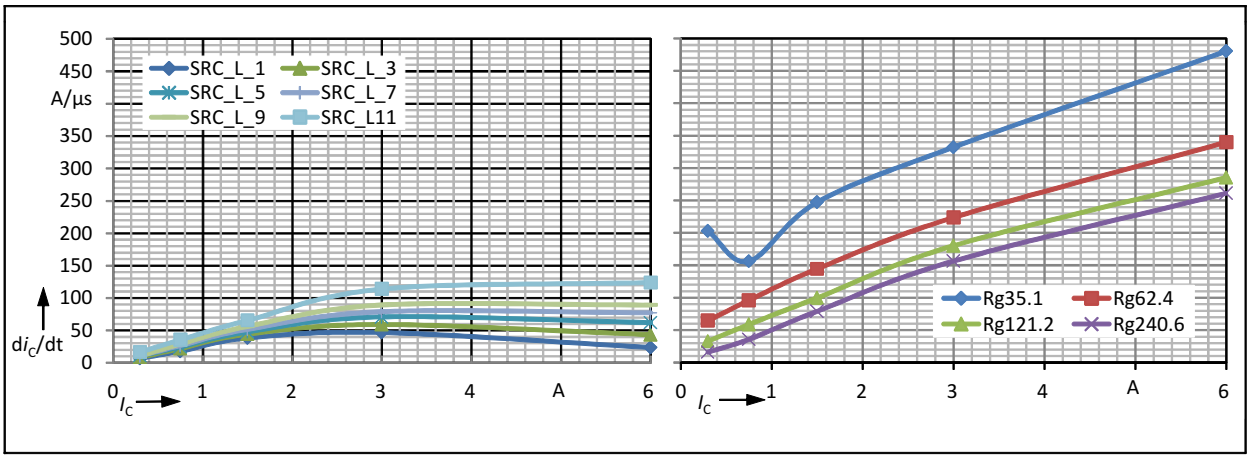

Figure 2: Current slew rate di_C/dt of IKD03N60RF using gate current control (“SRC”, left) and gate resistors (right)

It can be concluded from Figure 2 that the used setup of the slew rate control turn-on is much less collector current dependent compared to the standard gate drive turn-on. There is even a kind of a saturation visible after reaching the nominal current level of 3 A. The standard gate drive using gate resistors shows an almost linear increase of the collector current slew rate di_C/dt over the range of gate resistors between 35 Ω and 240 Ω and collector currents. The di_C/dt at nominal current differs by a factor of 2 or even higher, when comparing level 11 (SRC) with Rg = 240 Ω. The lower current commutation speed also has several positive effects in the application, such as less susceptibility to negative static voltages, which may occur at the gate driver IC and reduced tendency to generate oscillations.

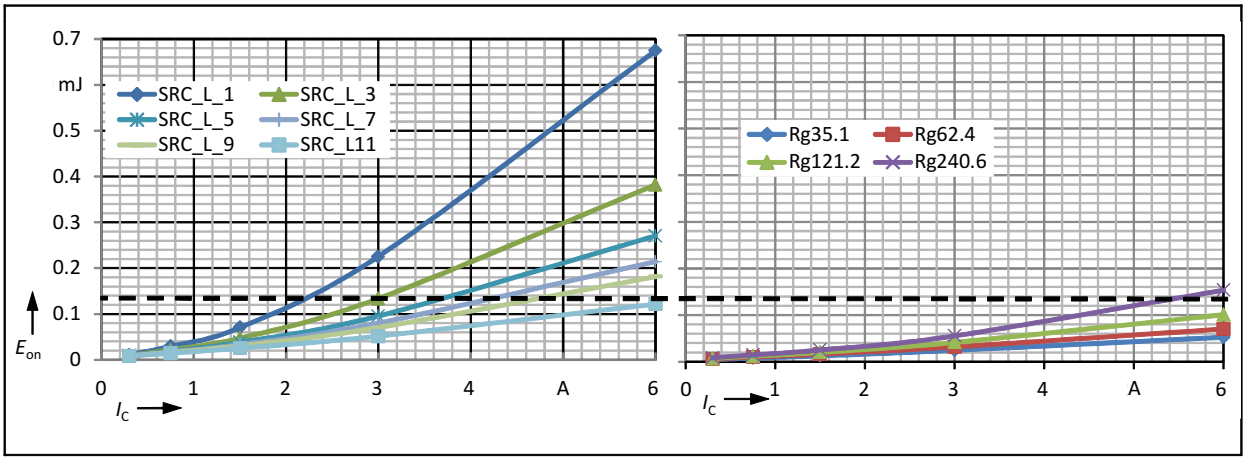

Figure 3: Turn-on energy E_{on} of IKD03N60RF using gate current control (“SRC”, left) and gate resistors (right)

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The fastest turn-on using a gate current is level 11. This level matches best to the standard turn-on using *Rg* = 240 Ω in terms of turn-on energy according to Figure 3. In combination with Figure 2 it can be seen that low switching speed in terms of di_C/dt is not mandatorily related to a high turn-on energy E_{on}. Level 11 shows much slower di_C/dt performance.

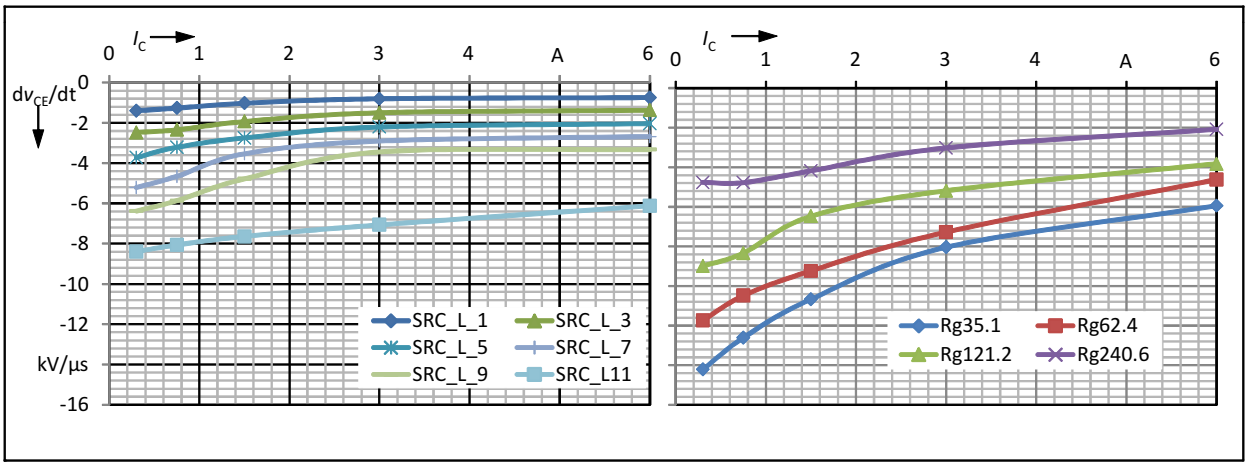

Figure 4: Collector-emitter voltage slew rate dv_{CE}/dt of IKD03N60RF using gate current control (“SRC” left) and gate resistors (right)

Figure 4 shows the evaluation results of the with respect to the collector-emitter voltage slew rate. The dv_{CE}/dt slew rate at level 11 of the gate current control method is a little higher than the comparable curve of the standard gate drive using. A setup of a SRC gate driver using level 9 brings results which match better to the curve of *Rg* = 240 Ω when applying a standard gate driver. The little increase of the turn-on energy of level 11 compared to level 9 according to Figure 3 is acceptable.

The turn-on waveforms of the IKD03N60RF are given in Figure 5 for 10% of the nominal current, which is 0.3 A and a DC bus voltage of 300 V. The results of the SRC method are shown in the left column and the results of the standard method using *Rg* = 240 Ω. on the right column. The collector current shows considerably less oscillations and a lower reverse recovery current I_{rr}. This improves the EMI behavior of the application, while the turn-on energy E_{on} remains the same as given in Figure 3.

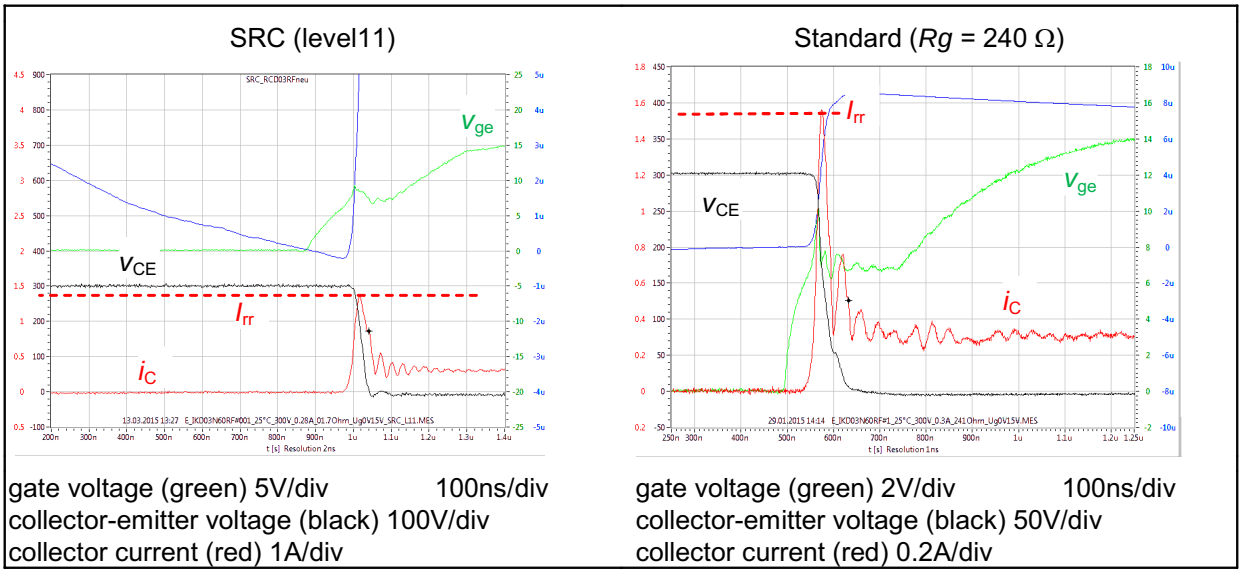

Figure 5: Turn-on at 10% and 100% of nominal current with the SRC method (left) and standard (right)

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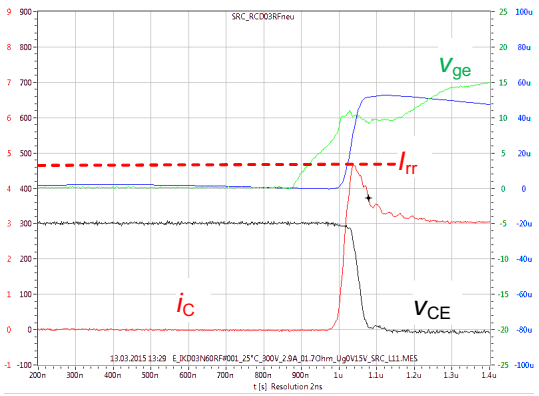
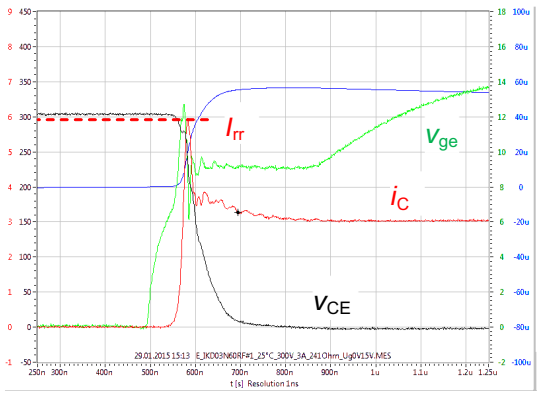
Figure 5 depicts the turn-on waveforms of the IKD03N60RF for 100% of the nominal current, which is 3 A at a DC bus voltage of 300 V. The results of the SRC method are left and the results of the standard method are on the right. The collector current shows again considerably less oscillations. The reduction of the reverse recovery current is much stronger at nominal current than at 10% of nominal current. The SRC gate current method results in a reverse recovery current of I_{rr} = 4.5 A, while the standard method results in I_{rr} = 5.9 A, which is 24% higher.



gate voltage (green) 5V/div 100ns/div
collector voltage (black) 100V/div
collector current (red) 1A/div



gate voltage (green) 2V/div, 100ns/div
collector voltage (black) 50V/div,
collector current (red) 1A/div

Figure 6: Turn-on at 10% and 100% of nominal current with the SRC method (left) and standard (right)

4. Turn-on evaluation of CoolMOS™ CFD IKD65R1K4CFD

The investigated drain current range is from 0.3 ≤ I_D ≤ 3 A for this transistor. The turn-on energy E_{on} in the left column in Figure 7 reaches similar values when comparing the results of SRC level 10 with a standard gate drive which applies an Rg = 240 Ω (right diagram). This is indicated by the horizontal, dashed line in Figure 7, which indicates E_{on} = 0.1 mJ.

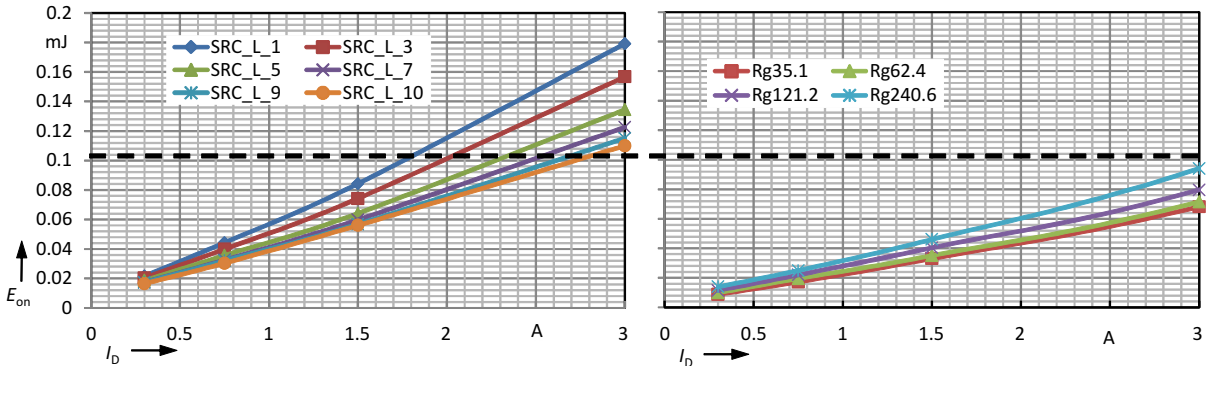


Figure 7: Current slew rate di_D/dt, turn-on energy E_{on} and collector-emitter voltage slew rate dv_D/dt of the IKD65R1K4CFD using the gate current control (“SRC”, left) and gate resistors (“Standard”, right)

The correlated drain-source voltage slew rate dv_D/dt is almost constant in the range of 15 – 20 kV/µs. It would be very simple with the SRC method to achieve even lower dv_D/dt rates as it is shown in Figure 8, such as SRC levels 1 – 9.

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The dv_D/dt rates decrease continuously down to 5 kV/µs with lower gate current levels. This would be comparable to using gate resistance in the kΩ regime.

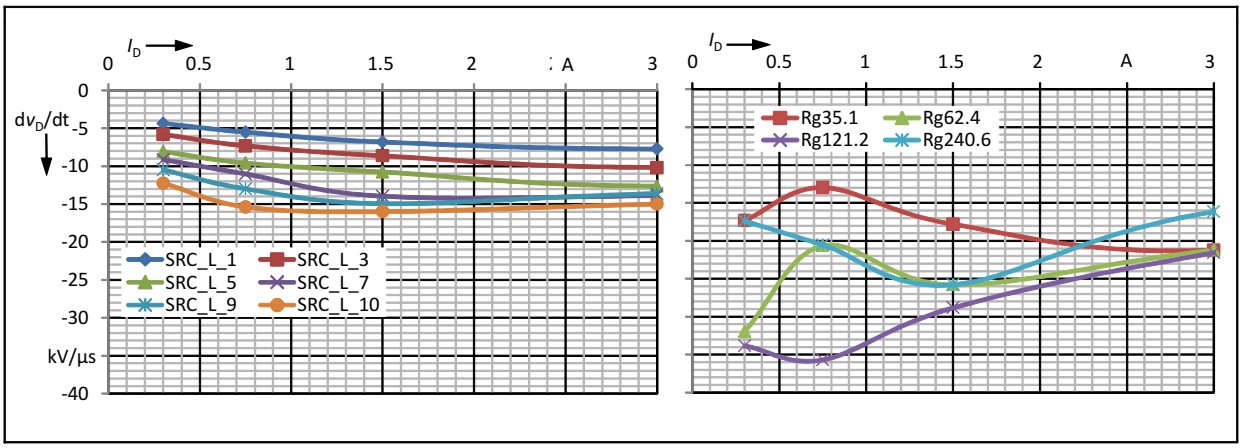

Figure 8: Current slew rate di_D/dt, turn-on energy E_{on} and collector-emitter voltage slew rate dv_D/dt of the IKD65R1K4CFD using the gate current control (“SRC”, left) and gate resistors (“Standard”, right)

The diagrams of the drain current slew rates di_D/dt as a function of the drain current i_D are given in Figure 9. Similar to the RCD-IGBT, the drain current slew rate of the CoolMOS CFD transistor is lower by a factor of 2 when using the SRC gate current control instead compared to the standard gate driver curve related to *Rg* = 240 Ω. The SRC gate current method poses an excellent way to control the di_D/dt,for MOSFETs while the turn-on energy E_{on} remains same as with the standard gate resistance control.

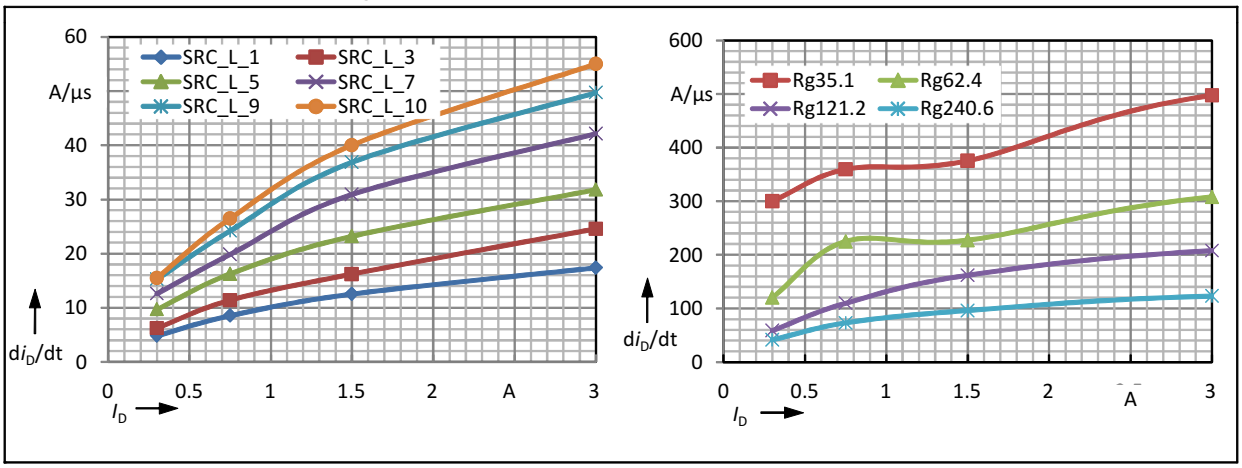

Figure 9: Current slew rate di_D/dt of the IKD65R1K4CFD using the gate current control (“SRC”, left) and gate resistors (“Standard”, right)

Similar as for IGBTs, the CoolMOS transistor IKD65R1K4CFD generates much lower reverse recovery currents when using the SRC method as it is depicted in Figure 10 and Figure 11. The SRC method only generates small oscillations after the commutation from the body diode. The SRC gate current control method results in less noise and therefore improved EMI. These advantages are achieved keeping the same or even lower turn-on energy E_{on}.

The reverse recovery peak is reduced as well in case of the SRC gate current control Especially at low drain current values, such as given in Figure 10, the reverse recovery current is approximately I_{rr} = 1.8 A. This is 35% lower compared to the related case, when using a standard gate driver with *Rg* = 240 Ω. The reverse recovery current value for the standard gate drive is I_{rr} = 2.8 A.

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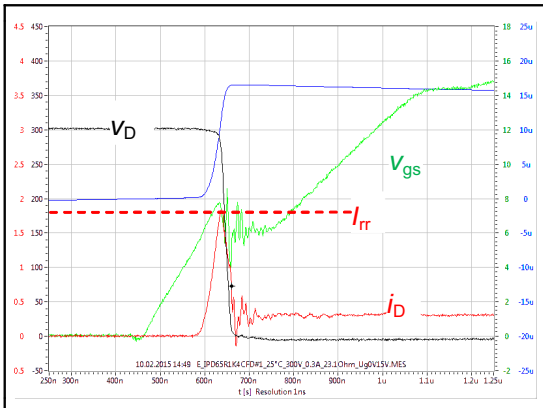
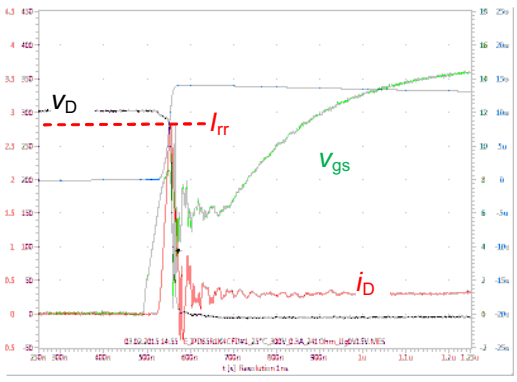
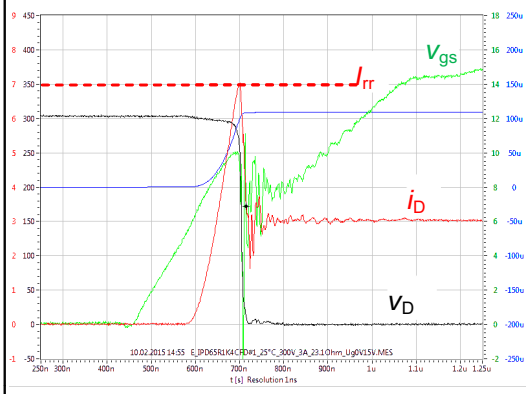


gate voltage (green) 5V/div 100ns/div
collector voltage (black) 100V/div
collector current (red) 0.5A/div

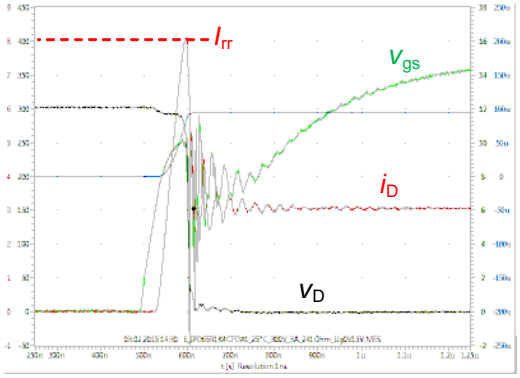


gate voltage (green) 2V/div 100ns/div
collector voltage (black) 50V/div
collector current (red) 0.5A/div

Figure 10: Turn-on at drain current I_D = 0.3 A with SRC method (level 10, left) and Standard (*Rg* = 240 Ω, right)



gate voltage (green) 5V/div 100ns/div
collector voltage (black) 100V/div
collector current (red) 1A/div



gate voltage (green) 2V/div, 100ns/div
collector voltage (black) 50V/div,
collector current (red) 1A/div

Figure 11: Turn-on at drain current I_D = 3 A with SRC method (level 10, left) and Standard (*Rg* = 240 Ω, right)

5. Conclusion

The SRC gate current control method is an effective way to improve the turn-on behavior of both discrete IGBTs and power MOSFETs. Especially the current slew rates can be reduced dramatically, while keeping the turn-on energy constant for comparable cases. Furthermore, the SRC gate current control method results in smoother waveforms with respect to gate voltage, drain current / collector current and drain voltage / collector-emitter voltage. This results in an overall improved EMI behavior. The SRC gate current control method is superior to any kind of gate resistance control for reaching low levels of current slew rates or voltage slew rates.

ISBN 978-3-8007-3924-0

6. References

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