Robustness of level shifter gate driver ICs concerning negative voltages

Jinsheng Song, Wolfgang Frank, Infineon Technologies AG, Am Campeon 1-12, 85579 Neubiberg, Germany, jinsheng.song@infineon.com

Abstract

In power electronic field, the level shifter gate driver IC suffers heavily from the negative voltage especially at the high side reference pin, which is normally connected with the load. Three half bridge level shifter gate driver ICs are tested under static and transient negative voltage condition. This paper will show the test method and point out the performance of each gate driver IC under the negative voltage condition.

1. Introduction

Integrated circuits based on standard silicon technology exhibit low tolerance to negative voltages presented to their inputs and outputs. A small negative voltage (-1V to -2V) at one of the IC pins may already result in uncontrolled substrate currents (e.g. due to forward biased PN junction from substrate to active area) which may trigger an unwanted IC behavior. This erratic behavior may lead to further issues in the circuit where the IC is being used.

In case of gate driver ICs, negative voltages may be very problematic in particular. Gate driver ICs are used to control power transistors which operate at high voltages and currents. The switching nature of such circuits combined with circuit parasitics may lead to oscillations and voltage swings which often expose IC pins to a negative voltage. Figure 1 shows an examples about how this negative voltage happens in power electronic field.

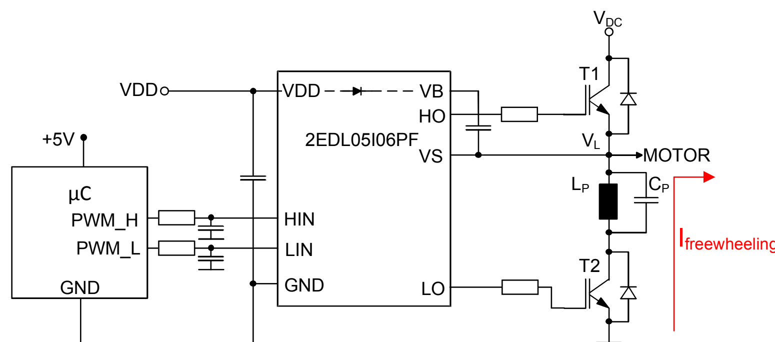

Fig. 1. Typical half bridge topology

This is a typical half bridge topology which consist two power transistors (IGBT) T1 and T2 which is used to drive for instance a motor as load. When high side transistor T1 is on, the load is getting power from DC link power supply. When T1 is off, due to the inductive load, the load current direction will not immidiately change, which means the freewheeling diode of the low side power transistor T2 will conduct the freewheeling current $I_{freewheeling}$. Since the emitter of T2 is grounded, the collector of T2 will show a negative voltage. Combining with the circuit parastic L_P and C_P which is defined by the layout, the output voltage of this half bridge circuit V_L could be a considerablely large transient negative voltage. This V_L is connected to the high side reference voltage pin VS of the driver IC. The negative voltage appears at this VS pin will generate big impact on the normal operation of the driver IC which could lead to mulfuction or even chip damaged.

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So the pins of the gate driver IC must be tolerant to such behaviour and internal protective structures are often used to accommodate static negative voltages as well as transient negative pulses up to a certain extent. The purpose of this paper is to document the sensitivity of various gate driver ICs to negative voltages.

The study was performed on half bridge gate driver ICs from various manufacturers. The tested gate drivers and their main operating parameters are listed in Table 1. The main difference is: one of the driver ICs is basing on Silicon-On-Insulator technology and others are basing on bulk silicon technology.

Table 1: Tested Half Bridge Drivers

	Infineon 2EDL05N06PF [1]	**Reference device 1**	**Reference device 2**
Technology	Silicon-On-Insulator	Bulk silicon	Bulk silicon
Isolation level	600V	600V	600V
Isolation method	Level shifter	Level shifter	Level shifter
$V_{s\ tran\ (t<500ns)}$ [V]	-50	Unknown*	Unknown*
V_{static} [V]	-0.5	-0.3	-0.3
Bootstrapping	Internal diode	Internal FETs	External diode
I_{Opk+} [A]	0.36	0.4	0.35 (min 0.25)
I_{Opk-} [A]	0.70	0.65	0.65 (min 0.5)

* Not specified in respective product datasheet

As can be seen from the listed parameters, each of the devices is tolerant to negative voltages of various amplitudes and durations. The tests which are documented in this report were designed in order to push the tested ICs to their limits and to uncover possible anomalies in gate driver operation induced by static and dynamic/pulsed negative voltages.

2. Silicon-On-Insulator Technology

The Silicon-On-Insulator (SOI) is an advanced technology for fabricating power integrated circuits because the buried oxide provides an effective way of isolating the low power integrated circuits from the power devices. Based on conventional bulk process the SOI technology uses an insulator called buried oxide underneath the active device layer, as shown in Fig. 2.

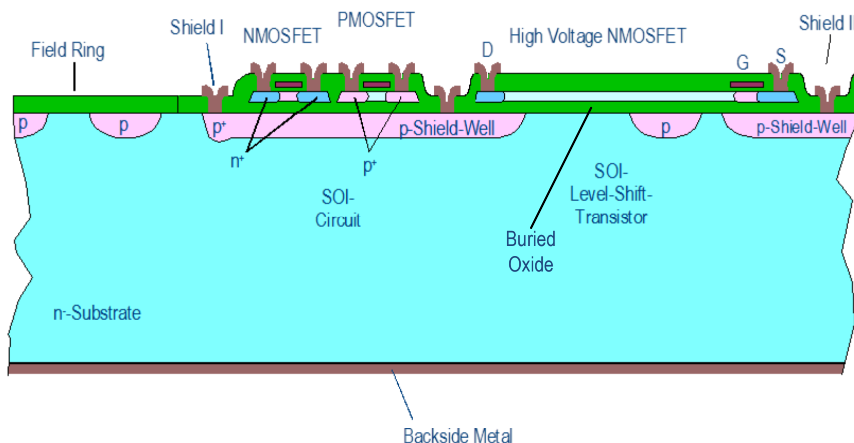

Fig. 2. Silicon-On-Insulator transistor

The lateral insulation of elements inside the silicon film is achieved by a simple local oxidation of silicon (LOCOS) process. In this way, all active device regions are fully insulated from

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each other. The parasitic bipolar transistors are eliminated. Thus, there is no need for CMOS-wells for preventing the “latch-up” effect.

Most important, since the buried oxide is insulating the active area from the substrate, this structure intrinsically has good immunity for the negative voltages, which can appear for instance at the Drain or Source region, as described at beginning of this paper.

3. Test setup

The susceptibility of gate driver ICs to negative voltages was studied by using DC/static tests as well as pulse/dynamic tests. This was done in order to cover various situations which may occur in practical applications. The ICs may be exposed to negative voltages in a static way in case of a malfunction of other circuits. As mentioned above, the driver ICs may also be regularly exposed to short negative pulses in case of circuit transients. These may be of high amplitude (up to tens of volts) and of relatively short duration (up to hundreds of ns). Such pulses may regularly appear at the VS pin (as shown in Fig. 1) of the gate driver during a normal circuit operation due to circuit parasitics. In both cases the driver ICs should be able to maintain a normal operation without a malfunction in order to prevent damage to power devices.

The static tests were performed using the circuit shown in Fig. 3. The negative voltage was always connected to one of the IC pins and the negative voltage –V was ramped up. In the same time, PWM inputs were supplied by a PWM signal generator. The IC was supplied from power supplies to enable normal run of the gate driver outputs. The input as well as the output signals were monitored by using an oscilloscope and any anomaly respectively failure was recorded.

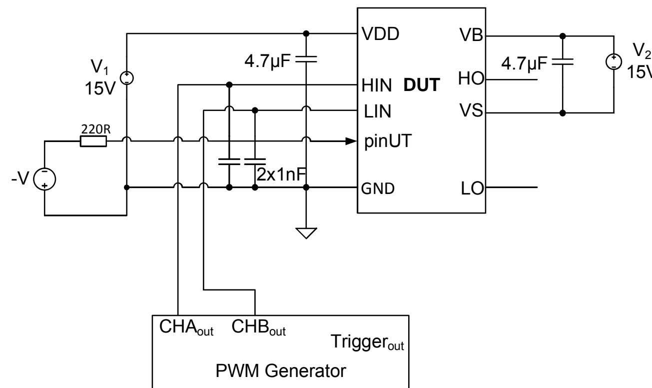

Fig. 3. Simplified test circuit for static tests

The dynamic tests were performed using the circuit shown in Fig. 4. As can be seen, the negative pulses were applied directly to VS pin of the device under test. The reason for that is that this pin is the most likely one to experience such high amplitude and short duration negative pulses. The input side of DUT IC was supplied by PWM signals from a PWM generator. The circuit was supplied from two 15V power supplies V_1 and V_2 to establish a normal circuit operation. The second power supply V2 was required since the bottom switch in the phase arm was not available for bootstrapping. The bottom switch was replaced by pull down resistors in order to enable effective injection of negative voltages to the VS pin during intervals when the bottom switch would be normally on. The PWM generator was manually triggered to generate a nine pulse PWM sequence. The middle (fifth) pulse in the sequence (as shown in Fig. 5) was triggering the second pulse generator which was used to drive the negative pulse generator. This synchronisation was done in order to maintain the negative pulse generation to the time interval when the upper switch is off. During the on-state of the

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upper switch, the VS voltage is clamped to the DC link voltage (100V in the test circuit) and injection of negative voltages is restricted. The amplitude of the negative pulse was controlled by the voltage supply –V where as the duration of the pulse was controlled by settings of the pulse generator. The amplitude of the pulse was varied from –10 to –60V where as the duration of the pulse from 50 to 600ns.

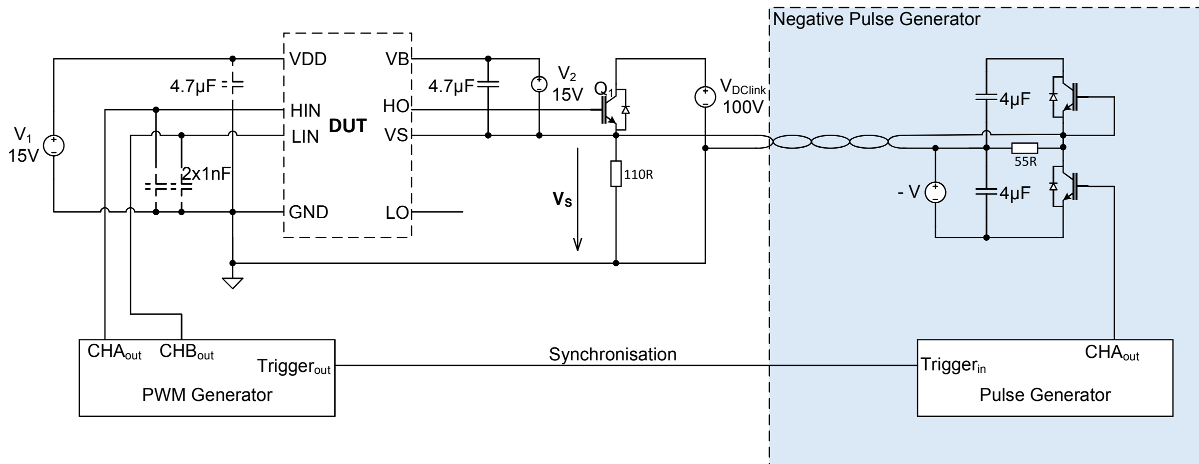

Fig. 4. Test circuit for dynamic tests with negative voltage pulses

The test pulse configuration which was studied is shown in Fig. 5. The negative pulse is applied in the moment just after the turn-off of the upper switch. This pulse configuration was chosen since in a practical application it is most probable that negative voltage pulses would be injected to VS pin in this instant due to changes of switching states of power switches and freewheeling effect. The appeared occasion dt of the negative pulse (see the Fig. 5) was varied in a wide range when the device under test showed sensitivity to negative pulses further away from the switching transitions. This was done in order to include cases when the negative pulses are generating in other locations in the power circuit, for example in other circuit phases.

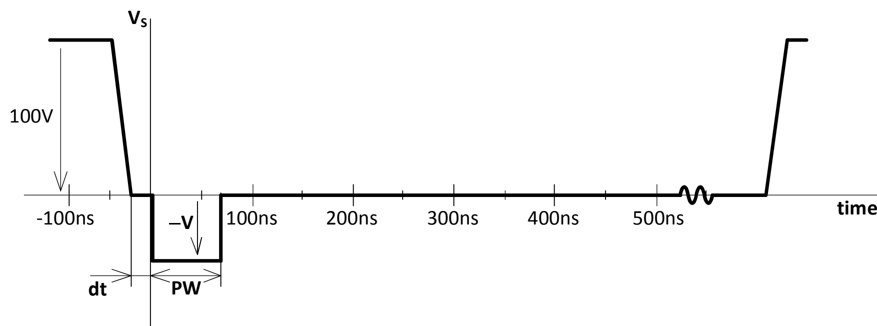

Fig. 5. Test pulse configuration, negative pulse at turn-off of the upper switch

4. Test result of static negative voltage

Infineon 2EDL05N06PF

max. values	$-V_{PSU}$ [V]	$-V_{pin}$ [V]	I_{PSU} [mA]	ANOMALIES
Hi_in	-31	-1,27	133	No
Lo_in	-31	-1,23	134	No

The device passed the test without any anomaly. The negative voltages were pushed to the maximum of the available power supply and no misbehaviour was detected.

Reference device 1

max. values	$-V_{PSU}$ [V]	$-V_{pin}$ [V]	I_{PSU} [mA]	ANOMALIES
Hi_in	-11,6	-0,95	45	Hi_out: Stuck at High
Hi_in	-14,5	-1,03	58	Hi_out: Stuck at High Lo_out: Stuck at Low
Lo_in	-6,3	-0,76	22	Hi_out: Stuck at Low

The device failed in normal operation with the negative voltage connected to Hi and Lo inputs. The operating failure is that the PWM sequence at the output stopped and got stuck. The misbehaviour occurred with negative voltages as low as –6.3 V.

Reference device 2

max. values	$-V_{PSU}$ [V]	$-V_{pin}$ [V]	I_{PSU} [mA]	ANOMALIES
Hi_in	-8,4	-0,8	31	Lo_out: Stuck at Low
Hi_in	-10,5	-0,86	40	Lo_out: Stuck at High
Lo_in	-14,9	-0,91	61	Hi_out: Stuck at Low
Lo_in	-16	-0,92	66	Hi_out: Stuck at High

The device failed in normal operation with the negative voltage connected to Hi and Lo inputs. The observed behaviour is that the PWM sequence at the output stopped with output going to L state at first. If the negative voltage continues to increase, the same output later goes into H state. This misbehaviour occurred with negative voltages as low as –8.4 V for Hi input pin.

5. Test result of transient negative voltage

Infineon 2EDL05N06PF

Vs[V] \ PW[ns]	50	100	200	300	400	500	600
-10	OK	OK	OK	OK	OK	OK	OK
-20	OK	OK	OK	OK	OK	OK	OK
-30	OK	OK	OK	OK	OK	OK	OK
-40	OK	OK	OK	OK	OK	OK	OK
-50	OK	OK	OK	OK	OK	OK	OK
-60	OK	OK	OK	OK	OK	OK	OK

The device performed very well in the tests when the negative pulse arrives right after the turn-off. There were no anomalies detected in the driver function. An example of the waveform with a negative pulse of –60V lasting for 600ns is shown in the figure below.

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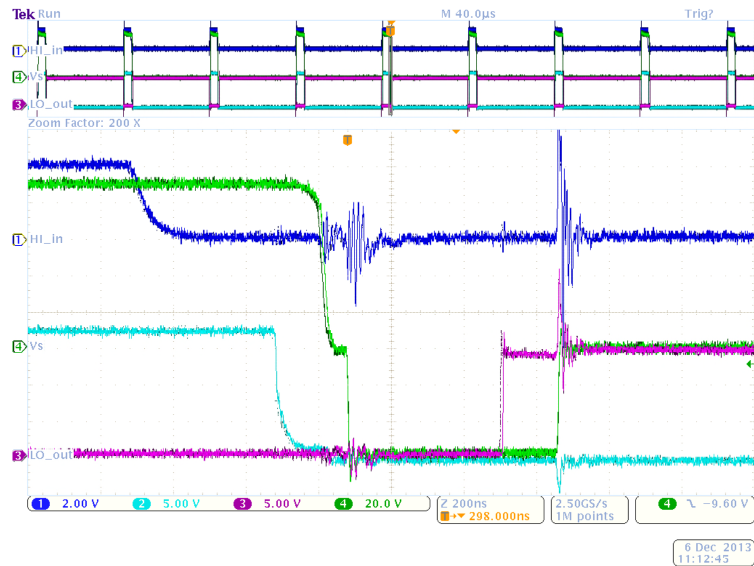

Fig. 6. Waveforms measured with negative pulse of –60V and 600ns duration; CH1 (Blue) – HIN, CH2 (Cyan) – HO, CH3 (Magenta) – LO, CH4 (Green) – VS

Reference device 1

Vs[V] \ PW[ns]	50	100	200	300	400	500	600
-10	**OK**	**OK**	**OK**	**OK**	**OK**	**OK**	**OK**
-20	**OK**	**OK**	**OK**	**OK**	**OK**	**Abnormal**	**Abnormal**
-30	**Abnormal**	**Abnormal**	**Abnormal**	**Abnormal**	**Abnormal**		
-40	**Abnormal**	**Abnormal**	**Abnormal**				
-50	**Abnormal**	**Abnormal**					
-60	**Abnormal**						

The device behaves as expected at negative pulses with amplitude lower than –20V respectively pulses shorter than approx. 400ns. In case of pulses with higher amplitude or longer duration, High side output HO tends to change from L to H state even if not requested by the input signal. This behavior is illustrated in the figure below.

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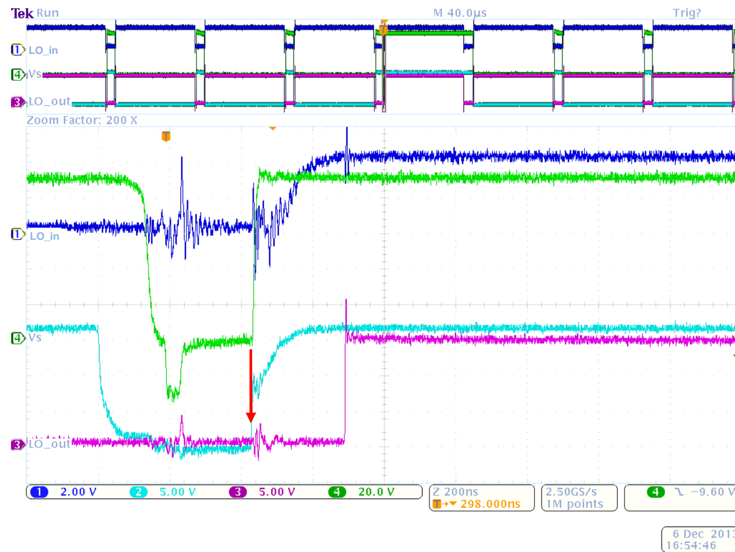

Fig. 7. Waveforms measured with negative pulse of –30V and 50ns duration; CH1 (Blue) – LIN, CH2 (Cyan) – HO, CH3 (Magenta) – LO, CH4 (Green) – VS; HO changes from L to H state even if the input signal requests L state, as shown with red arrow

Reference device 2

Vs[V] \ PW[ns]	50	100	200	300	400	500	600
-10	OK	OK	OK	OK	OK	OK	OK
-20	OK	OK	OK	OK	OK	OK	OK
-30	OK	OK	OK	OK	OK	OK	OK
-40	OK	OK	OK	OK	OK	OK	OK
-50	OK	OK	OK	OK	OK	OK	Abnormal
-60	OK	OK	OK	OK	OK	Abnormal	Abnormal

The device performed well in the test. There were no anomalies detected in the driver function as long as the negative pulse is not over -50V and 500ns.

6. Conclusion

This paper compares three level shifter half bridge driver ICs with focus on the negative voltage influence. The performed tests include static tests and dynamic/pulse tests in order to cover various situations which may occur in practical applications. The test result shows the Silicon-On-Insulator (SOI) based driver IC offer better negative voltage immunity capability comparing with conventional bulk silicon technology based driver ICs.

7. Literature

[1] Infineon Technologies: 2EDL05N06PF, datasheet, Infineon Technologies, Germany

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