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Performance of power semiconductor devices and the impact on system level

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Abstract

The performance of power modules is based on both the internal configuration, i.e. layout and used semiconductors, and the external operating conditions including the cooling concept. This mutual interaction between power module and application is investigated to provide a guideline for configuring appropriate power modules and building of optimized systems. Using present diode technologies and operating conditions for a given switch, a relation is established towards achievable power density, switching frequency, and power-cycling capability. Based on these findings, a decision strategy on system level is provided, and recommendations for the use and operation of different diode types are given.

1. Introduction

Power semiconductors and especially power modules are widely used in today's electrified world: in variable speed drives, in traction, in wind and solar systems. Although the focus is different in all these applications, the overall key requirements are the same: switching as well as conduction losses should be low, a good thermal performance is desired, the overall dimensions should be small, and reliability is mandatory [1],[2]. Thus, the performance of the power module can mainly be described using power losses, junction temperatures, and number of cycles at a given temperature ripple.

However, with respect to the different applications, the requirements are prioritized diversely. While low switching losses and high efficiency is a must in solar applications, for example [3], the focus is on the temperature ripple and power-cycling capability in servo drives [4]. Independent of the specific application, the thermal interface has a significant impact on the performance of both the power module and the system. An adequate choice enables the operation of the system at the given operating conditions and within the power module limits, and guarantees the required performance in the respective application.

The performance of the power module is based on both, typical system parameters like output current, switching frequency, or cooling conditions, and parameters of the power module itself like static characteristics, switching energies, maximum junction temperature and thermal resistance. Due to the interplay between system and power module parameters, achieving the optimal power module performance based on the requirements of a specific application is both highly crucial and non-trivial. At the same time, in particular for high-performance inverter systems, different realization strategies for a power module may provide benefits or have significant drawbacks with respect to the chosen technologies. The mutual interdependency between power module and application is intimately determined through the aforementioned parameters. Hence, a thorough understanding of both is indispensable to obtain an optimized power module and system performance, and to generate the highest benefit on system level.

In this paper, the overall system performance is discussed in terms of maximal output current – or power density –, achievable switching frequency, and power-cycling capability. Focus is set on the diode performance and its impact on the system with a given fast-switching IGBT. Therefore, several combinations with fast-switching diodes are investigated, which alter power module parameters such as the conduction losses, switching energies, thermal resistance, and maximum junction temperature of both switch and diode. Subsequently,

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these experimental results are combined with system parameters like cos phi or output frequency to analyze, on the one hand, the interplay between current, switching frequency, and reactive power, and, on the other hand, the impact on total power losses, junction temperature, and power-cycling capability. An overview on the accessible parameter space for power modules with different fast-switching diodes is given.

2. Power module design

The starting point is measuring the switching losses of power modules with double-pulse configuration at constant switching conditions. In this scenario, a 650 V TRENCHSTOP™ 5 IGBT is used as a switch [5]. The diode is integrated in the commutation path and, within the comparison, the diode characteristics are used as a free parameter. In detail, fast-switching 650 V Rapid1 Si diodes and 650 V SiC Schottky diodes Generation 2 (Gen 2) are operated in parallel whereas a mixing of different technologies was avoided [6],[7]. Table 1 gives an overview. This approach allows comparing the altered switching performance of both IGBT and diode with respect to the chosen diode technology. Due to the parallel operation of diodes, several forward voltage values V_F are covered for each technology.

Design A	75 A, 650V TRENCHSTOP™ 5 IGBT	2 x 40 A, 650 V Si Rapid 1 Diode
Design B	75 A, 650V TRENCHSTOP™ 5 IGBT	1 x 40 A, 650 V Si Rapid 1 Diode
Design C	75 A, 650V TRENCHSTOP™ 5 IGBT	3 x 8 A, 650 V SiC Schottky Diode, Gen 2
Design D	75 A, 650V TRENCHSTOP™ 5 IGBT	2 x 8 A, 650 V SiC Schottky Diode, Gen 2
Design E	75 A, 650V TRENCHSTOP™ 5 IGBT	1 x 8 A, 650 V SiC Schottky Diode, Gen 2

Table 1: Five power module concepts were investigated with different combinations of diode.

Operating several diodes in parallel leads to a reduction of V_F for a given diode current I_F (see figure 1, left). Thus conduction losses are reduced independently of the diode technology. The conduction losses of the switch are not altered within the test, while those in the diode are consequently smaller for paralleled devices due to the current sharing.

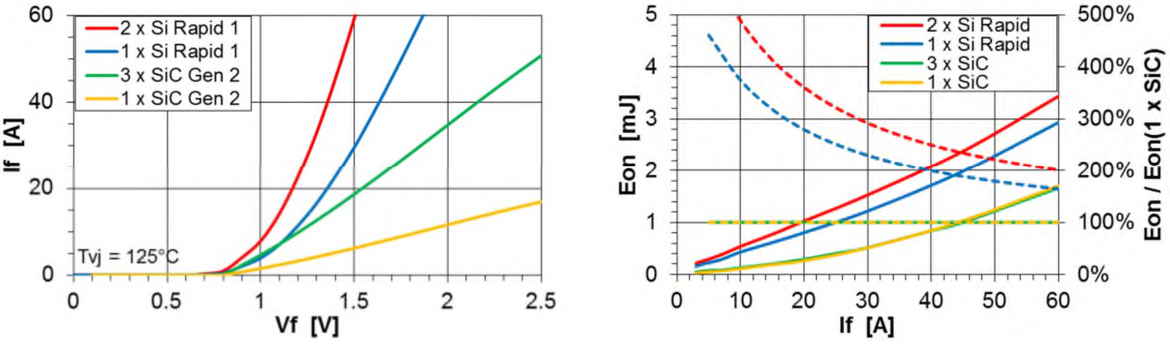

Figure 1: Diode characteristics (left) and IGBT switching losses E_{ON} (right) for the different diode solutions. For E_{ON}, values are given on an absolute and relative scale with solid and dashed lines, respectively. While the Si solutions have lower V_F and thus conduction losses for a given current, the switching losses are higher and depend on the number of paralleled devices.

The turn-on switching losses of the IGBT for the respective diodes in the commutation loop are shown in the right part of figure 1. Solid lines represent absolute values, whereas dotted lines show E_{ON} values scaled to E_{ON} using SiC diodes. It is immediately clear that the SiC diodes reduce the absolute E_{ON} losses. Also a paralleling does not alter the switching losses. This is different using Si diodes. Here higher losses occur with reduced V_F due to the increased area and thus Q_{rr}.

For the SiC diodes, the turn-on losses are solely given by the switch and thus serve as a reference. The differences in relative losses contribution when using Si diodes originate only from the choice of technology and accompanying Q_{rr}. The effect of diode configuration on E_{ON} is predominant at small currents and visible throughout the whole range. In all cases, a reduction in turn-on losses is countered by an increase in V_F for the different configurations. Depending on load current and switching frequency, these two effects are competing. Notably, at high f_{sw}, solutions with minimal E_{ON} will be superior despite higher conduction losses.

3. Power module parameters

The IPOSIM tool [8] is used to evaluate the impact of the different diode technologies during operation. Power losses, junction temperature T_{vj}, and temperature ripple are calculated based on the aforementioned power module configurations while covering typical values for sinusoidal output current, switching frequency, and cos phi. All other parameters are fixed, like ambient temperature at 40°C, sine-triangular control, and a DC-link voltage of 400 V. Figure 2 summarizes power module parameters using the different designs, together with the power losses and junction temperatures for operation at I_C = 20 A and f_{sw} = 20 kHz. Total power losses P_{tot} are comprised of conduction and switching losses of both switch and diode. The right scale displays temperatures and losses, while all other parameters are scaled on the left using the units given in brackets in the legend. The red bars indicate the allowed, maximum operation junction temperature $T_{vj,op,max}$ for the respective diode. A positive correlation between forward voltage V_F and thermal resistance $R_{th,jh}$ of the diode is recognized within each diode technology. These parameters are connected through the total chip area. The diode junction temperature $T_{vj,D}$ is increasing accordingly. Especially, for cos phi = -0.85, the temperature limit of the diode is exceeded for Design D and E. In general, there is a tendency of reduced total power losses for the SiC diode solutions if $T_{vj,op,max}$ is not exceeded – at the cost of higher temperatures at the diode.

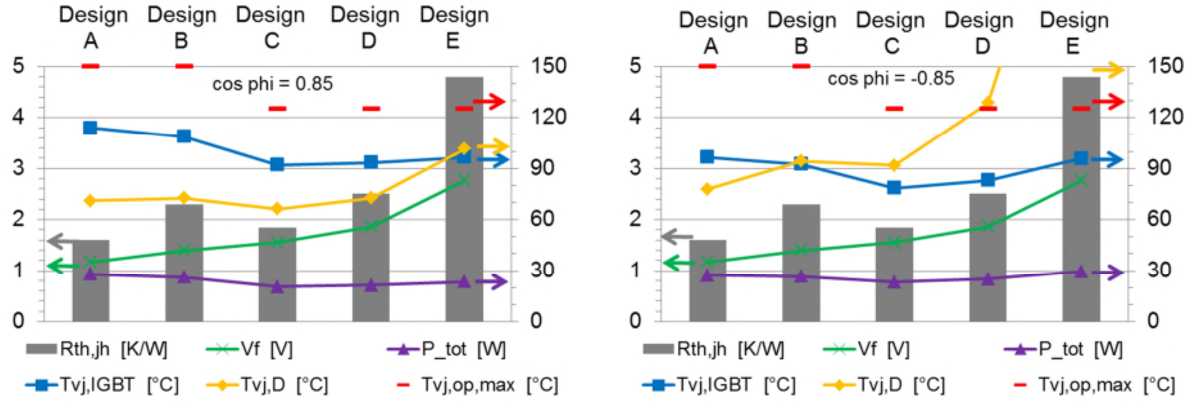

Figure 2: Summary of power module parameters and performance for operation at I_C = 20 A and f_{sw} = 20 kHz. The red bars indicate the respective maximum junction temperature for the diodes.

Based on the above given example, Figure 3 shows the achievable output current for the five designs as function of switching frequency f_{sw}. The current at either IGBT (I_C, solid lines) or diode (I_F, dotted lines) is limiting the operation due to the respective maximum junction temperature for diode and switch, which is 125 °C for SiC Gen 2 diodes and 150 °C for Si Rapid 1 diodes and IGBT. For cos phi = 0.85 (left graph), the losses are mainly generated at the switch, and the output current is limited by the IGBT except for small SiC areas. This is different for cos phi = -0.85, where the diode is determining the output current except for Design A and high f_{sw}.

For cos phi = 0.85, the overall power density is clearly better if SiC diodes can be used at adequate area: The reduced switching losses allow for more than 15% higher output current at the switch. Consequently the power density increases by 15% on power module level. For cos phi = -0.85, the diode is here in general limiting the output current and thus power density, which is therefore closely linked to a proper choice of diode configuration in this scenario. For the examined designs and technologies, Si has an improved performance especially due to the higher $T_{vj,op,max}$, while other parameters like $R_{th,jh}$ are varied in the same range except for Design E (compare Figure 2).

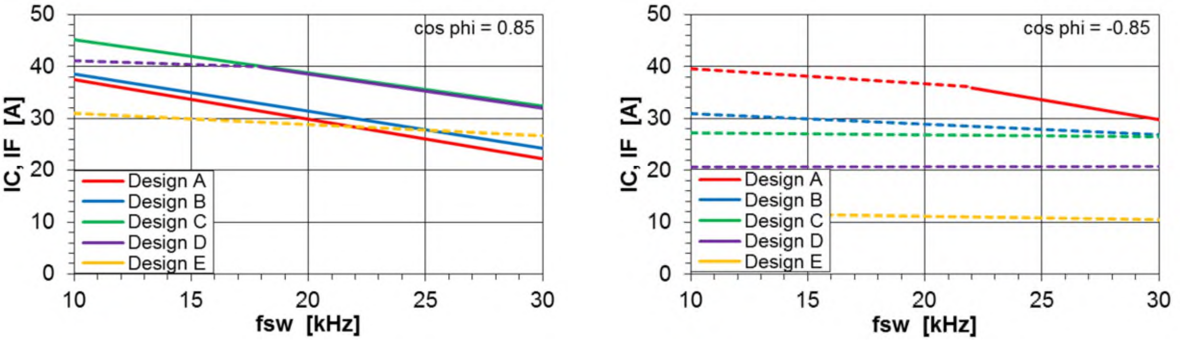

Figure 3: Dotted and solid lines show the maximum power module current, limited by diode and switch, respectively. For cos phi = 0.85 (left) the IGBT is limiting the current except for Design E and in the high frequency regime also for Design D. For cos phi = -0.85 (right), the diode is the limiting device except for Design A at high switching frequency.

4. Power module performance in the application

In a solar inverter, main parameters for system design are the trade-off between achievable switching frequency, current and power losses. The output frequency equals the grid operating frequency, thus $f_{out} \approx 50$ Hz for Europe, and cos phi is close to one. Figure 4 shows the resulting power losses in this application for 16 A and 32 A (dash-dotted and solid lines) as a function of f_{sw}. While the power losses generally increase with output current and f_{sw}, the configurations with SiC diodes always have lower losses at a given operating point. Alternatively, a higher switching frequency can be used while operating at constant power losses and thus constant efficiency.

The right part of Figure 4 shows the interplay between generated total power losses and the resulting junction temperatures for diodes (dotted) and switches (solid lines) for f_{sw} from 10 to 30 kHz. At high power density, $T_{vj} = 150$ °C is reached at the switch which results in a limit for f_{sw} as indicated by the full circles. The difference between Si and SiC configurations clearly shows that small Q_{rr} is supporting high f_{sw}. As one consequence, SiC diodes allow for higher efficiency and/or higher switching frequency; this in turn lead to reduced magnetics costs and generates a positive impact on total system costs [9].

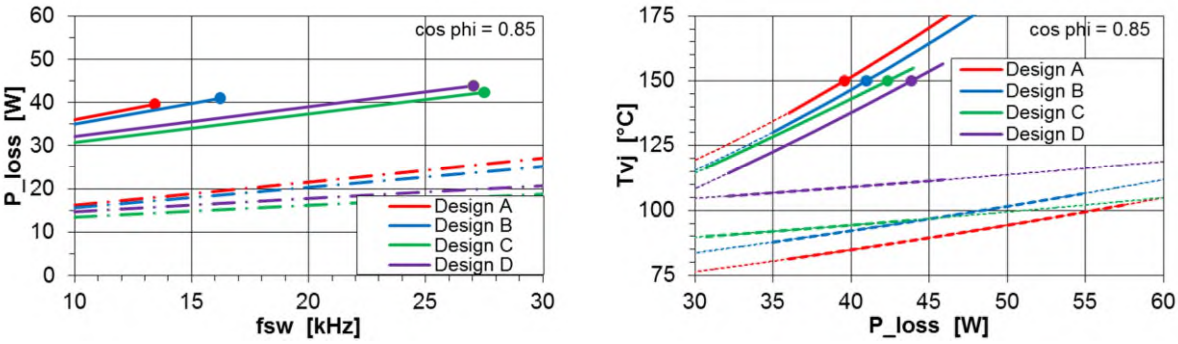

Figure 4: The left-hand side displays the total power losses (switch and diode) for 16 and 32 A (dash-dotted and solid lines) at varying switching frequency. The right-hand side shows the interplay between generated power losses and resulting T_{vj} of switch (solid) and diode (dashed) for f_{sw} from 10 to 30 kHz. The circles indicate the termination condition $T_{vj,op,max}$ =150°C for the switch.

Solar applications are very specific in their requirements and operating regime. In particular, output frequency f_{out} and cos phi are varied in a very limited way. This is generally not the case in drives applications, where these parameters may be varied in a broad range.

A variation in cos phi is mainly transferring losses from switch to diode and vice versa, while a reduction in f_{out} increases the thermal load for both devices at a given cos phi. Besides this impact on power losses and device temperature, also the temperature ripple for the devices is altered and may become critical, especially with respect to the diode. The resulting power-cycling capability is then another performance parameter that may limit the operation.

Figure 5 shows temperatures and temperature ripple for varying output frequency, while f_{sw} = 10 kHz and I_C = 20 A. Under these conditions, the different power module configurations operate always below their respective $T_{vj,op,max}$, except Design E in the lower left graph as indicated by the red bars. The column heights represent the resulting T_{vj}, whereas the light top part of each column indicates the temperature ripple. The latter is directly connected to the power-cycling capability according to the respective power-cycling curves [10].

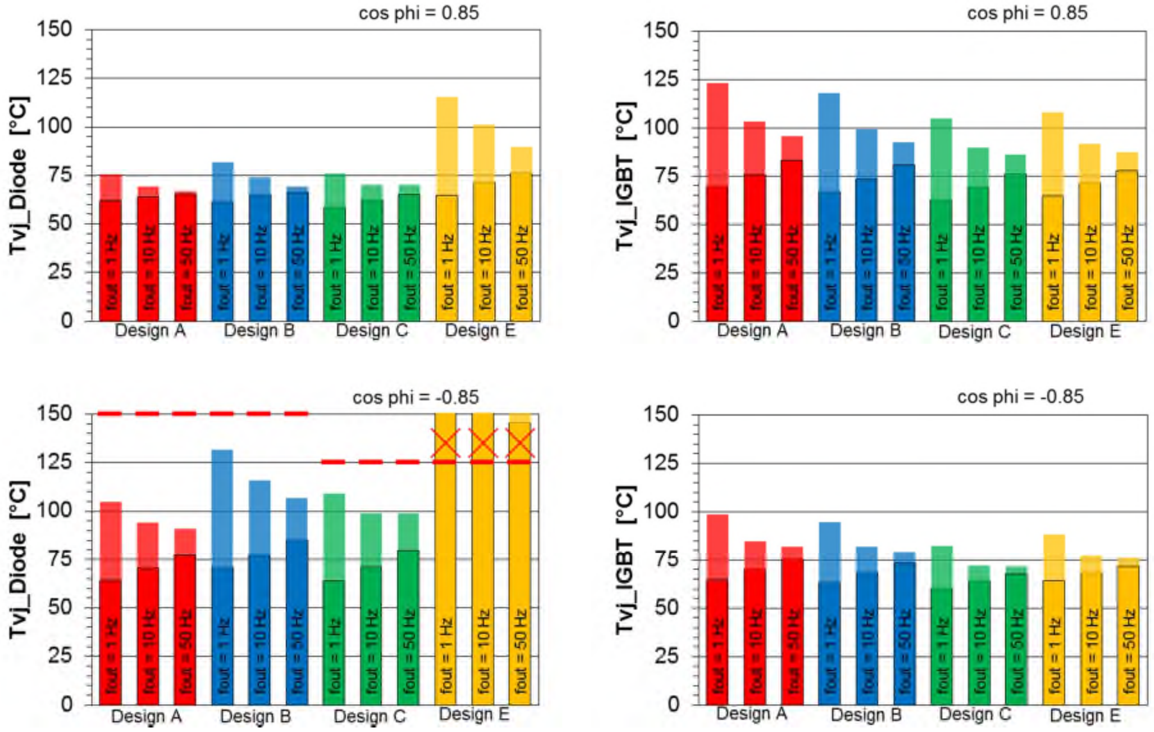

Figure 5: These graphs show the effect of output frequency f_{out} and cos phi on T_{vj} of diode (left) and switch (right) for I_C = 20 A and f_{sw} = 10 kHz. The total column height represents T_{vj}, while the top part in light colors indicates the temperature ripple during one cycle of f_{out}. Design E exceeds $T_{vj,op,max}$ (indicated by the red bars) in the lower left graph, thus no number of cycles are given.

Several trends become immediately visible: The junction temperature of both diode and switch is increasing upon reduced output frequency for all operating conditions and Designs, and so does the temperature ripple. Comparing the upper and lower row, the aforementioned load shift from the switch towards the diode is recognized for negative cos phi. Independent of f_{out}, the diodes reach higher T_{vj}, while the switch temperature is reduced in all Designs. The temperature ripple follows this trend, putting higher demand on the diode and relieving the switch. The consequence is a pronounced imbalance between the two devices for cos phi = -0.85. This leads to the situation that Design E can be operated at cos phi = 0.85, but not at cos phi = -0.85 due to the diode limitation.

The temperature ripple is seen to be very sensitive to the $R_{th,jh}$ and thus to the available diode area, independent of the technology. The power-cycling capability correlates directly with the temperature ripple, but the different technologies impact the explicit conversion. Comparing the investigated Si Rapid 1 and SiC Gen 2 technologies, the former have in general a better power-cycling capability at equivalent temperature ripple than the latter. However, as the ripple is intimately linked to the respective available diode area, similar performance can be reached with operating more devices in parallel (e.g., Design C), especially at low f_{out}. The temperature ripple and thus power-cycling capability of the switch is hardly altered at cos phi = 0.85, whereas in the bottom right graph there is even a lower ripple for designs using SiC diodes. Thus, the power-cycling discussion is limited to the diode in the following.

In general, the importance of power-cycling is given by the application and respective typical mission profiles. If power-cycling is not critical, even a variable f_{out} may be allowed for a power module solution with a single SiC diode per switch (Design E) and at cos phi close to one. The limitations are then given by the operating conditions and available diode area. Decreasing cos phi results in a higher T_{vj}, which becomes the limiting factor for small SiC devices. With present technology, only with a higher degree of parallelization the temperature limit can be fulfilled. If the application calls for high power-cycling capability and low f_{out}, the Si solution is to be chosen. Also here, operating more devices in parallel avoids higher temperature for the device. As a result, the operating conditions define whether SiC Generation 2 diodes may be used in order to benefit from reduced losses and higher switching frequency, or whether Si Rapid 1 diodes enable a variation of cos phi and f_{out} together with a high power-cycling capability. For upcoming designs, also the improved performance of future SiC diodes (e.g. $T_{vj,op,max}$ = 150 °C for SiC Generation 5) and interconnection technologies have to be taken into account. The impact especially on power-cycling has to be reviewed.

5. Diode performance and consequences for the application

Figure 6 shows the achievable output current using Si and SiC diodes under most demanding operating conditions at cos phi = -0.85. Thick lines indicate the region covered with presented power module configurations. Thin lines indicate a trend towards higher parallelization of diodes. At identical $R_{th,jh}$, the Si devices can utilize an additional temperature budget of 25°C before reaching $T_{vj,max}$ (see Figure 2). Based on Generation 2, a similar output current performance for SiC diodes can only be reached with a larger degree of parallelization.

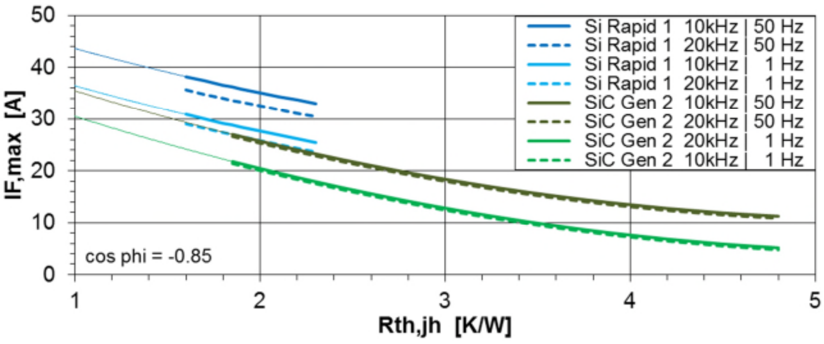

Figure 6: The variation of achievable output current is followed as function of diode area and cooling conditions. Blue colors indicate the Si Rapid 1 technology, whereas red represents SiC Gen 2 devices. cos phi = -0.85 is a worst case scenario, where the diode is the limiting device.

At the same time, the maximum current at the switch is ranging between 30 A and 50 A for the different operating conditions. Thus, the utilization of the IGBT may be less than 20%, depending on the power module configuration and operating conditions. Although an over-dimensioning of either switch or diode can hardly be avoided totally – this requires a singular point of operation –, knowledge about the application must be gathered for an appropriate configuration of the power module.

The accessible parameter space for Design B (1 x Si Rapid 1 diode, blue colors) and Design C (3 x SiC Gen 2 diode, green colors) is visualized in the left part of Figure 7 for f_{sw} = 30 kHz. The lower edge of each color area indicates that the temperature limit of the diode is reached for the respective current range. Any limitations due to the maximum IGBT temperature are not included. Starting in the upper right corner, the allowed current is continuously decreasing in all directions. The full parameter space (cos phi = -0.85 to 0.85; $f_{out} \geq 1$ Hz) can only be addressed utilizing Si diodes at a maximum current of 20 A. A SiC diode configuration which supports these operating conditions would require more parallelization than used in Design C. In combination with the results obtained from Figure 6, Design B is preferable here.

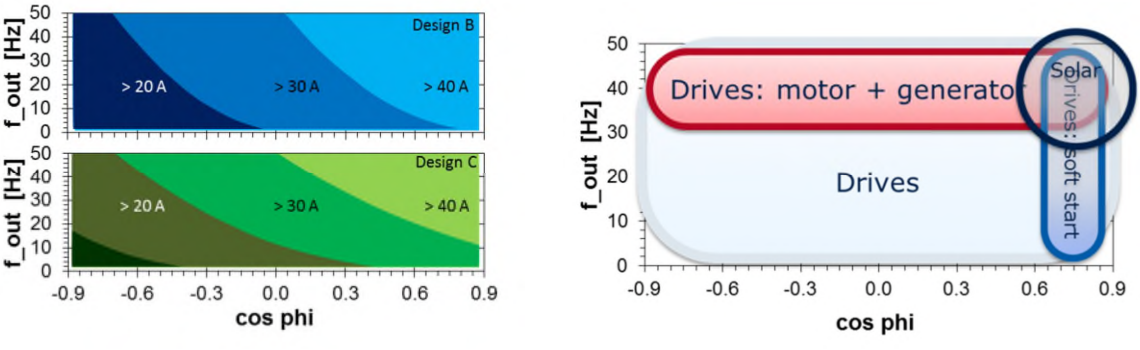

Figure 7: Left: Accessible parameter space in the f_{out}–cos phi– plane for Design B (blue colors) and Design C (green) at varying current. The right graph visualizes the parameter region typically covered by the respective applications.

The colored areas in the left part of Figure 7 automatically provide a view on typical usage of present SiC devices: SiC diodes are used best in the upper right corner, where losses can be reduced or accepted to operate at higher f_{sw}. Varying f_{out} is an option if the maximum current is reduced. The advantage is a reduction in power losses and possibly a higher switching frequency. At high f_{out} and variable cos phi, SiC may be used if power-cycling is not crucial in the application. In contrast to this, Si Rapid 1 diodes are the best choice if the full f_{out} – cos phi parameter space needs to be addressed by an inverter. The degree of parallelization is defined by the requirements towards temperature ripple and T_{vj}. For future generations of SiC diodes, the increase of $T_{vj,op,max}$ is a clear objective. This will lead to a shift in the above described accessible parameter space, and thus power density. At the same time, advanced interconnection technologies will improve the power-cycling capability. In turn, this will also impact the required degree of parallelization and, therefore, can alter the presented results and thus the given conclusion.

The right part gives a simple schematic overview on the requirements for the respective applications. Far away from representing all demands of drives applications, it visualizes the respective application regions for the investigated diode technologies: In solar applications, the request for low losses and high switching frequency make SiC diodes the devices of choice, and this is also where the performance of power modules with SiC diodes is best. Inverter systems with soft-start may also benefit from SiC diodes, especially where power losses are more critical, like in motor-integrated inverters. In contrast to this, for pure 50 Hz operation with recuperation, Si Rapid 1 diodes are proven state-of-the-art. SiC diodes may be used technically, but only at reduced current or with a higher degree of parallelization. A clarification of these different requirements and a specification of target applications is therefore crucial to design appropriate modules and yield an optimal system performance.

6. Summary

The performance of the diode and thus the whole system is shown to be driven by the interaction between device characteristics and operation conditions. Choosing the ideal power module for a system design is consequently related to a distinct knowledge of both the operating conditions in the application and the power module performance. From a system point of view, power modules need to be designed bearing the different requirements and their impact on the module performance in mind; then, the power module can serve to yield optimal system performance.

Therefore, the present paper shows the interaction between general diode device properties, power module configurations and application-specific parameters. For this investigation, diode technology, chip size, thermal power module criteria, and operating conditions for solar and drives applications were included as parameters. The impact and interaction of these parameters were analyzed and interpreted, and conclusions on the achievable current, power-cycling capability and minimum cos phi were presented.

The analysis clarifies that the common understanding of using SiC diodes in solar applications is supported: in this way, the total system can be significantly improved with respect to efficiency and switching frequency. In drives, the results are more heterogeneous and point towards a separation into different regions of operation for the investigated technologies: On the one hand, SiC diodes enable low-loss operation in the regime of soft-start inverters and at 50 Hz output frequency with variable cos phi. In both cases, the trade-off needs to be made between reduced power losses and additional costs. As one example, this may be attractive for motor-integrated and other compact inverter systems. On the other hand, for a full variation of f_{out} and cos phi, Si Rapid 1 diodes are the ideal choice at present. The degree of parallelization depends directly on the power-cycling requirements. Thus the two investigated diode technologies, namely SiC Gen 2 and Si Rapid 1, have their strengths in different regions of the parameter space. However, future generations of SiC diodes will require an updated analysis of the accessible parameter space. From a system point of view, there exist different application-specific requirements. A mutual understanding of power module performance and application needs is therefore indispensable to develop both appropriate power modules and optimized systems.

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