End-of-life investigation on the .XT interconnect technology

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Abstract

To meet the requirements of Infineon's 5th generation IGBT and diode, the .XT technology has been introduced [1,2]. It comprises a set of new packaging technologies - namely Cu wire bonding, diffusion soldering or silver sintering and soldering with strengthened Sn-based alloys. These technologies address all reliability relevant levels within the power module package in order to realize high lifetimes under thermo-mechanical stress. To explore the technology's full potential, active and passive thermal cycling test data were correlated with the responsible failure mechanisms. Thereby, a shift of the major damage location from the near-to-die interconnects towards the more distant interconnect layers (i.e., substrate and substrate solder joint) was observed. At the same time, by using .XT technologies it was possible to almost completely suppress bond wire lift-off and die attach degradation.

1. Introduction

For today's state-of-the-art power module packages soft soldering and Al wedge bonding are reference technologies that are widely used. With melting temperatures T_m of about 230-280°C for Sn based soft solders and operation temperatures of $T_{j,max} \leq 150°C$ reasonable reliabilities with respect to active or passive cycling can be realized. For higher operation temperatures, e.g., $T_{j,max}=175°C$, premature solder fatigue and bond wire lift-off are the observed failure mechanisms as creeping effects become more and more dominant (Fig. 1).

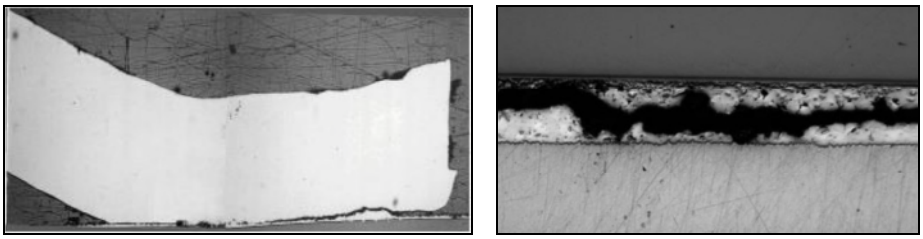

Fig. 1: Bond wire lift-off (left) and soft solder fatigue (right) after end-of-life power cycling with $T_{j,max}=150°C$ using standard Al wire bonding and Sn based soft solders.

Due to the current trend to increase the power densities on chip as well as on module level, there is an apparent need for robust packaging technologies to withstand cyclic thermo-mechanical stress at $T_{j,max}=175°C$ and above. An analysis of the failure mechanisms for Al wedge bonding and soft soldering revealed creeping fatigue of the interconnect materials as the dominant failure mechanism. From the materials point of view, the failure is caused by low cycle fatigue due to accumulation of plastic deformation during cyclic stress.

In order to overcome these limitations, the .XT technology platform has been developed with major attention towards the mechanical properties of the used materials. As a result, a new

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set of packaging technologies for future temperature demands of high power module packages has been developed and successfully tested with respect to its power cycling and thermal shock reliability [1-3].

In the present paper the end-of-life failure modes for the .XT technology platform under active and passive thermal cycling test conditions will be presented and discussed. It will be shown, that the resistance to thermo-mechanical fatigue is significantly improved with the new technologies. Furthermore, a shift of the major failure mode under short current pulse testing from the near-to-die interconnects (die top- and back-side) towards the substrate will be presented.

2. The .XT Technology Platform

Based on the above discussion, the .XT technology platform has been developed as a robust set of packaging technologies. It uses Cu, Ag, high melting intermetallics and strengthened Sn alloys as advanced packaging materials.

In a typical module set up today's interconnect technologies for the die top- and back-side as well as the substrate-to-baseplate interconnect will be replaced by new .XT technologies.

In detail, for the wedge bonding process the soft Al is replaced by Cu as a more robust wire material. To establish a stable and reliable Cu wire bonding process, Cu had to be introduced as a new top-side metal for the 5th generation of Infineon's high power IGBTs and diodes [4].

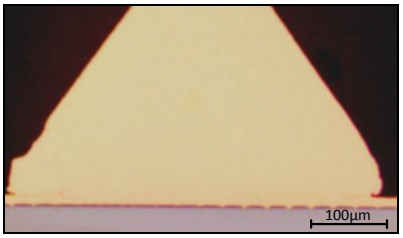

Fig. 1: Microsection of a Cu wedge bond on Si with Cu top-side metallization.

As can be seen in Tab. 1, Cu has a higher yield and tensile strength as well as a higher melting temperature compared to Al. These parameters already indicate an improved robustness against thermo-mechanical stress as well as a reduced impact of creeping effects on the fatigue life. In addition, the reduced coefficient of thermal expansion (CTE) improves the stress conditions at a constant temperature.

	Aluminium	Copper
Yield strength $\mathbf{R_e}$ [N/mm²]	20...50	50...90
CTE [1/K]	$23*10^{-6}$	$16*10^{-6}$
Tensile strength $\mathbf{R_m}$ [N/mm²]	30...70	210...250
Melting temp. $\mathbf{T_m}$ [°C]	660	1083

Tab. 1: Physical properties for aluminium and copper.

At the die-substrate interconnect level the .XT technology platform offers two new interconnect technologies.

On the one hand, there is diffusion soldering (DS) that exploits the formation of intermetallic compounds during soldering to establish a high melting joint between die and substrate.

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Here, the Sn based solder layer is completely consumed and transformed into a pure intermetallic joint. For the Cu/Sn system Cu_6Sn_5 and Cu_3Sn with T_m=416°C and 676°C, respectively, are the dominant phases that are formed during the process. In the case of Ag/Sn as soldering partners Ag_3Sn with a melting temperature of 480°C is formed [5].

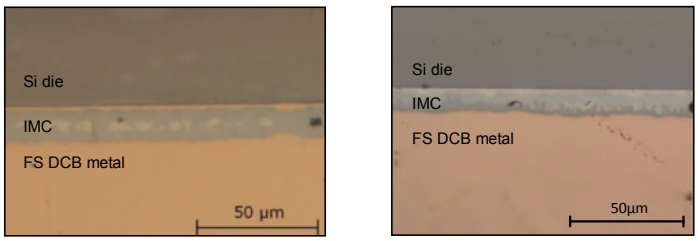

Fig. 2: Microsection of typical diffusion soldered die attach layers using Cu/Sn (left) and Ag/Sn (right) as intermetallic materials (IMC).

On the other hand, for the low temperature joining technology (LTJT) the sintering of small Ag particles is employed to form a monometallic bond between die and substrate. Here, under moderate temperatures (200-270°C) and high pressure (5-30MPa) a silver (Ag) filling with micron-sized particles is transformed into a compact and porous Ag joint having a melting temperature of 962°C [6]. While for the diffusion soldered joints a void free interface and a homogeneous formation of intermetallics are the major parameters to be controlled, the quality of the sintered joint directly relates to its porosity. With increasing porosity the elastic modulus as well as the strength of the LTJT layer are reduced. As a result, a reduction in fatigue strength with increasing porosity is observed.

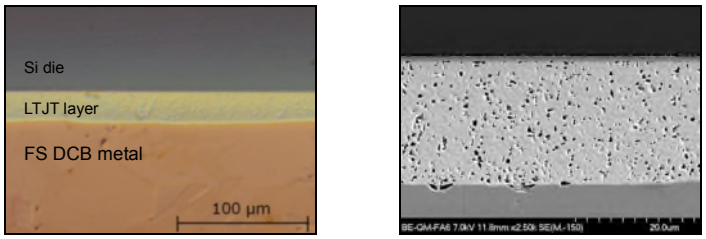

Fig. 3: Microsection of a sintered die attach layer with low porosity (left: optical, right: SEM).

Because of the high remelting temperatures of DS and LTJT interconnects creep effects have only negligible impact on the fatigue life at $T_{j,max}$=175°C. This is in strong contrast to standard soft solder joints.

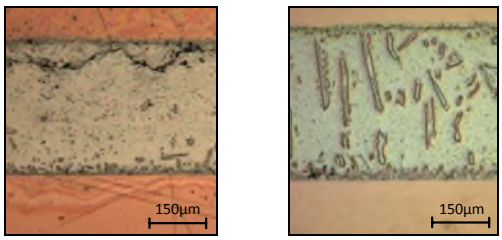

Fig. 4: Microsection of a standard Sn-Ag solder joint (left; after cyclic stress test) and a strengthened Sn based solder alloy.

For the substrate-to-baseplate interconnect the .XT technology platform features an improved solder material to meet the reliability demands at this interface. In detail, to improve the fatigue resistance of the solder matrix, a Sn-based solder was strengthened by means of solid solution and precipitation hardening to suppress the dislocation motion under thermo-mechanical stress. By this, the crack propagation velocity under cyclic testing can be

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significantly reduced. Nevertheless, similarly to standard Sn solders, for this material system creeping effects have to be taken into account.

As in most of today's standard power module packages, in the .XT technology the current and control terminals are welded to the substrates by ultrasonic power. Similarly to Cu wire bonding, the Cu-Cu interconnect is the ideal material choice for the current and control terminals.

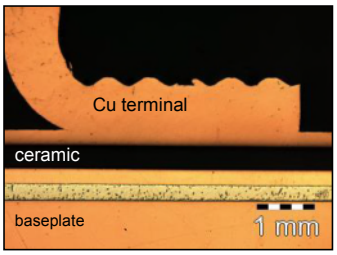

Fig. 5: Microsection of an ultrasonically (US) welded current terminal.

3. Reliability and Failure Mechanisms

3.1. Reliability

To prove the reliability of the .XT packaging technologies, several active and passive thermal cycling tests have been performed in the past. It was a strong objective of these tests to identify the end-of-life failure mode for a better understanding of the opportunities and limitations of the .XT technology platform.

Generally, all active and passive thermal cycling tests induce mechanical stress at all relevant interfaces within the power module due to differences in the CTE of the adjacent materials. As a consequence, the temperature difference as well as the duration of the cycle are the dominant parameters that control the created damage. A more detailed discussion on the influencing parameters during cyclic testing can be found in [7-8]. For the following discussion two test modes will be discussed.

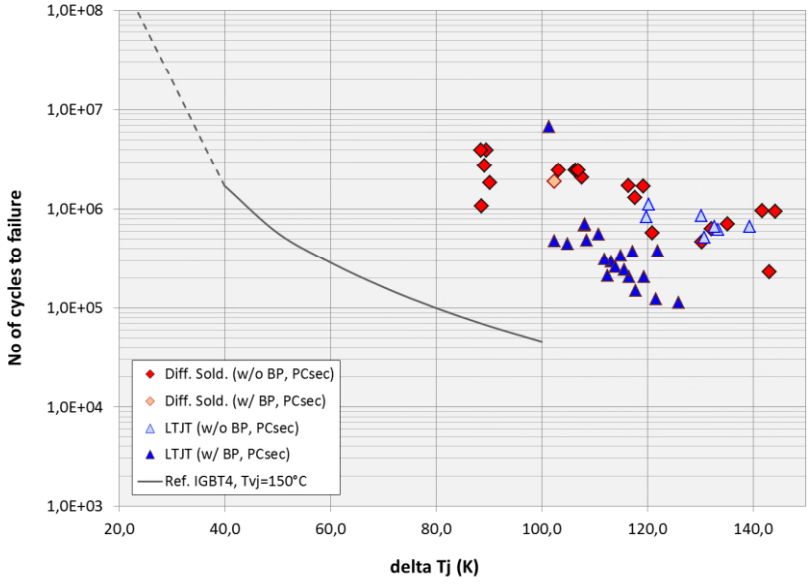

Fig. 6: Power cycling diagram for power modules w/ and w/o baseplates using .XT technologies. All samples use Cu wire bonding as top-side interconnect technology.

First, during passive thermal cycling (TC) tests and thermal shock tests (TST) a homogeneous temperature distribution is realized within the test specimen. Under these conditions the CTE mismatch in combination with the geometrical boundaries produce a maximum shear strain at the edges of the die- and substrate interconnect layer.

Second, under active power cycling conditions with a pulse duration t_{on}<5sec (PC_{sec}) an inhomogeneous temperature distribution with a distinct maximum at the center of the die will be established during the test. Here, the maximum fatigue area is located below the die's center.

The so-called PC_{min} test with t_{on} of several seconds to several minutes represents a hybrid test type. Depending on the actual runtime of the current pulses a mixed fatigue pattern could be expected with crack formation at the edges as well as below the center of the interconnect. For t_{on} in the range of several minutes the PC_{min} tests becomes similar to passive thermal cycling tests.

In Fig. 6, a summary of all PC_{sec} data is shown. All tests have been done with 1200V IGBTs or diodes. The maximum chip temperature T_{jmax} was at 165-171°C. The used failure criterion was an increase in thermal resistance of 20%. In comparison to the IGBT4 reference line an increase in PC reliability of a factor of ten and above is visible.

3.2. Failure Mechanisms

i) PC_{sec} Test (modules without baseplate)

As can be seen in Fig. 7 and 8, in PC_{sec} tests with t_{on}<3sec very similar degradation patterns for specimen using DS or LTJT as die attach layer can be found. For none of the tested samples degradation of the Cu top-side interconnect (Fig. 8a) is observed.

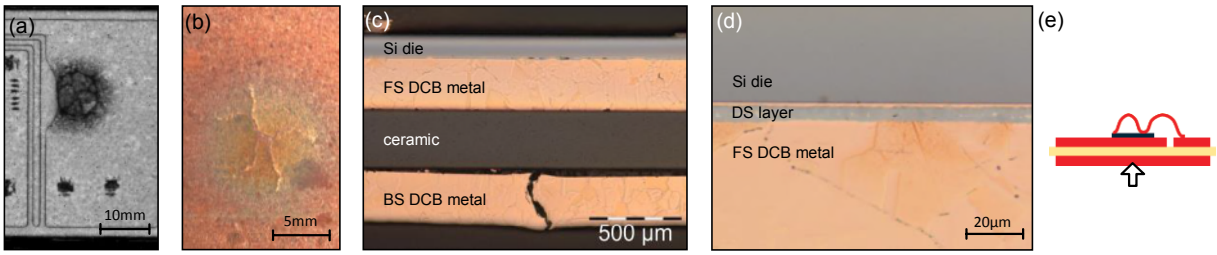

Fig. 7: .XT test sample with DS die attach w/o baseplate after 2.1mio short cycles at dT=107K. Acoustic image of the DCB interface (a), optical image of the DCB back-side (b), microsection of the test sample (c), the DS layer in detail (d) and location of major damage (e).

Furthermore, even after 2.1mio cycles the DS die attach layer shows no aging effects (Fig. 7d). In the LTJT layer minor degradation can be found after 665k cycles below the die's center (Fig. 8d).

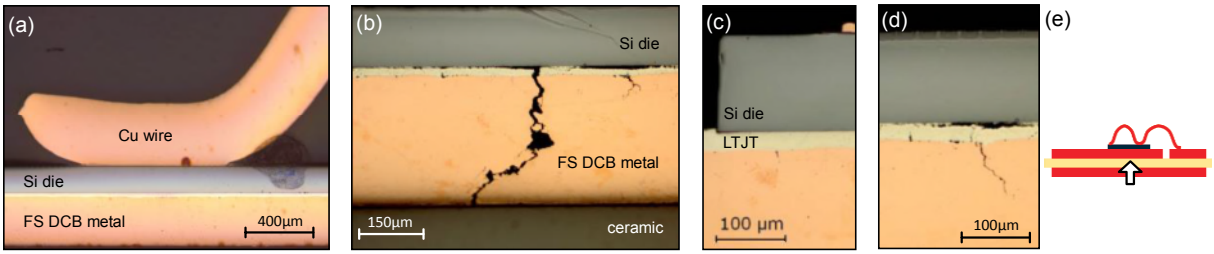

Fig. 8: .XT test sample with LTJT die attach w/o baseplate after 665k short cycles at dT=130K. Microsection of bond wire interconnect (a), fatigued area of substrate metallization (b), microsection of LTJT layer at edge (c) and at center (d) and location of major damage (e).

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Nevertheless, in all tested samples the end-of-life criterion was only reached due to fatigue and delamination of the substrate's Cu metallization (Fig. 7c, 8b). In agreement with the theory, in these samples for short thermal cycles the main damage is located below the thermal hot spot (Fig. 7e, 8e)

ii) PC_{sec} Test (modules with baseplate)

When adding a baseplate and the respective solder interconnect to the module the substrate is mechanically stabilized and due to creeping effects a shift of the damaged area towards the substrate-baseplate solder joint can be observed.

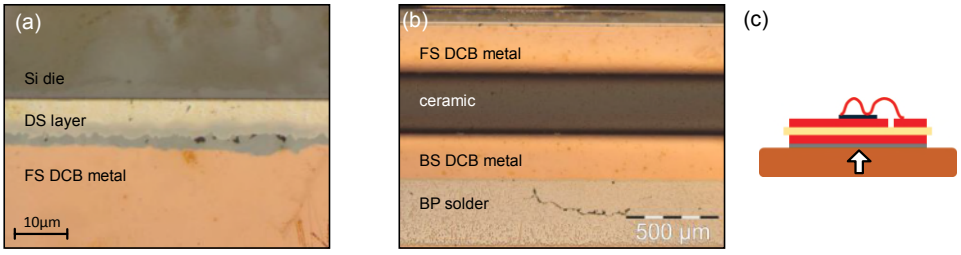

Fig. 9: Microsection of a test specimen w/ baseplate and DS die attach after 1.88mio cycles PCsec with dT=102K. Detailed microsection of DS layer (a), baseplate (BP) solder interconnect (b) and location of major damage (c).

As can be seen in Fig. 9b-c and 10c-d, depending on the maximum temperature difference a failure of the substrate-baseplate interconnect due to creeping fatigue can be found directly underneath the thermal hot spot after about 380k to 1.88mio cycles at dT=122K and 102K, respectively. In accordance with the samples without baseplate neither for the top-side interconnect (Fig. 10a) nor the die attach (Fig. 9a and 10b) any significant degradation can be found after testing.

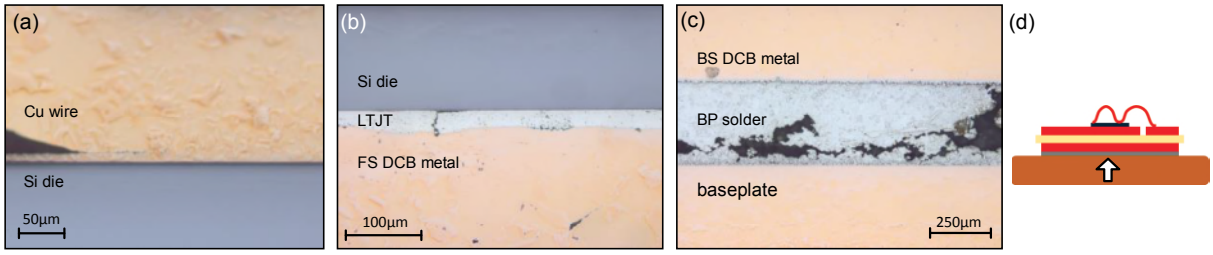

Fig. 10: Microsection of a test specimen w/ baseplate and LTJT die attach after 380k cycles PCsec with dT=122K. Detailed microsection of bond interconnect (a), LTJT interconnect (b), substrate-baseplate solder joint (c) and location of major damage (d).

iii) PCmin Test

As explained in Sec. 3.1, for long cycle times a homogenization of the temperature distribution within the power module leads to a shift of the load maximum towards the edges of the samples (e.g., die edge, substrate edge). This is in accordance with the experimental fact that for cycling times of 150sec a delamination of the substrate from the baseplate starting at the substrate edges can be found as the major damage (Fig. 11a-b). Neither the LTJT layer nor the bond wire interconnect show any degradation during this test (Fig. 11c). Furthermore, even for such long cycling times no aging of the terminal interconnect layer is visible (Fig. 11d).

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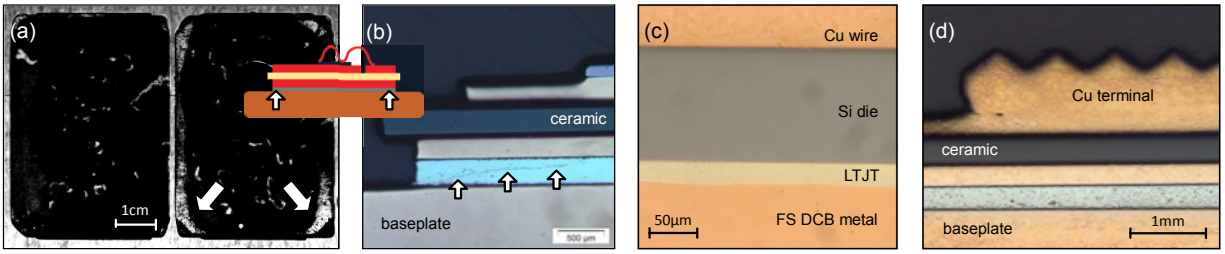

Fig. 11: .XT power module after 30kc PC_{min} with t_{on}=150sec, dT=80K and $T_{case,max}$=105°C. Acoustic microscopy image of substrate-baseplate interconnect (a) and cross-sections of substrate-baseplate joint (b), LTJT layer and top-side interconnect (c) and terminal (d).

iv) TST test

During thermal shock testing the samples are homogenously tempered between -40°C and 150°C. As in the PC_{min} test this procedure induces a load maximum at the sample's edges (e.g., substrate). As a result, neither the die attach layer nor the top-side interconnects, such as terminals and bond wires, show any degradation after 2000cycles. Using the strengthened Sn alloy as substrate interconnect material only minor delamination can be seen after the test (Fig. 12).

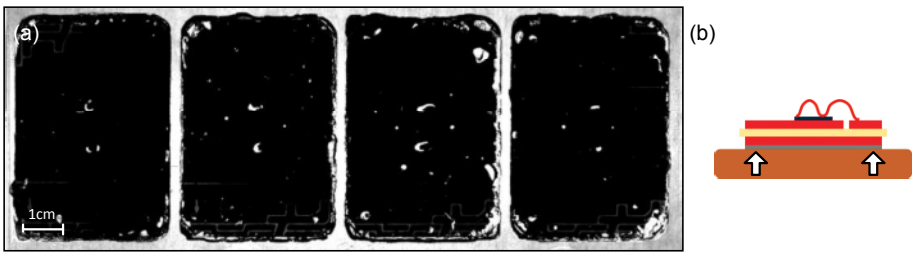

Fig. 12: Acoustic microscopy image of the .XT substrate-baseplate interconnect after 2000cycles TST (-40°C – 150°C). Delaminated areas and voids are visible as white areas within the substrate region (a) and location of major damage (b).

4. Conclusion

In the present paper, a thorough study on the degradation mechanisms of all reliability relevant interconnects within the .XT power modules under cyclic thermal load is presented. In depth failure analysis after the reliability testing has been used to localize areas of degradation and to identify the life-time limiting interconnects. To get a full picture on the degradation effects under different test conditions, active as well as passive thermal cycling tests with different cycling times were performed. In order to standardize the results, a distinction between modules with and without baseplates has been done.

For all type of modules and all test conditions neither the bond wire nor the terminal interconnect show any degradation. In the die attach interconnect layer (either LTJT or DS) degradation effects are only visible as secondary damage due to the degradation of the substrate's Cu metallization.

In the case of baseplate-free modules the metallized ceramic substrate is clearly limiting the lifetime of the samples.

Looking at modules with baseplates the major degradation can be found in the substrate-baseplate solder joint. Here, depending on the duration of the thermal pulse, the main damage location shifts from the position of the die (PC_{sec}) towards the substrate edges (TST, PC_{min}) with increasing pulse duration (t_{on}).

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In summary, it has been shown, that with the .XT technology platform standard degradation mechanisms, such as bond wire lift-off and die attach degradation, can be almost completely suppressed. By this, the main damage location shifts away from the near-to-die interconnects towards the more distant interconnect layers. Tab. 2 shows a condensed summary of the degradation effects in .XT test samples.

Module	Test	Die Attach Technology	
		Diffusion Soldering	**Low Temperature Joining Technology**
w/ baseplate	PC_{sec}	- *degradation in system solder below die* - no degradation at die attach visible - no degradation at wire bond visible - no degradation at welded terminals	- *degradation in system solder below die* - no degradation at die attach visible - no degradation at wire bond visible - no degradation at welded terminals
	PC_{min}	- *degradation in system solder at DCB edges* - no degradation at die attach visible - no degradation at wire bond visible - no degradation at welded terminals	- *degradation in system solder at DCB edges* - no degradation at die attach visible - no degradation at wire bond visible - no degradation at welded terminals
	TST	- *degradation in system solder at DCB edges* - degradation of terminal interconnect far above spec. limit - no degradation at die attach visible - no degradation at wire bond visible	- *degradation in system solder at DCB edges* - degradation of terminal interconnect far above spec. limit - no degradation at die attach visible - no degradation at wire bond visible
w/o baseplate	PC_{sec}	- *delamination of DCB back-side metal* - no degradation at die attach visible - no degradation at wire bond visible	- *delamination of DCB top-side metal* - above 665kc (dT= 130K) minor degradation at LTJT layer below die - no degradation at wire bond visible
	PC_{min}	- not tested	- not tested

Tab. 2: Summary of the degradation effects in .XT test specimens after end-of-life failure.

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