Correlating NTC-Reading and Chip-Temperature in Power Electronic Modules

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Abstract

In power electronic designs, the instantaneous chip temperature is of major importance to the user. In case the chip can't be accessed, additional sensors like NTCs can be used to measure a temperature that depends on the chip temperature. From this value, a chip temperature can be estimated. Determining the thermal correlation between chip temperature and sensor reading is not a trivial task. The present paper gives an insight into a basic but reliable procedure to extract the necessary information using an experimental setup.

1 Introduction

Designing a power electronic system usually starts with simulation both in electrical and thermal functionality. For the thermal simulation, the task is to determine the chip temperature as accurately as possible as this is a mayor parameter for the life time prediction. Though there is a JEDEC-standard [1] that defines the in-situ measurement as a method of choice to capture the chip temperature, the setup to do so is difficult to handle and the test procedure can barely be implemented in an application under operation. A further possibility poses as simplified approach to estimate the chip temperature. It is derived from the experiment given in the left part of figure 1

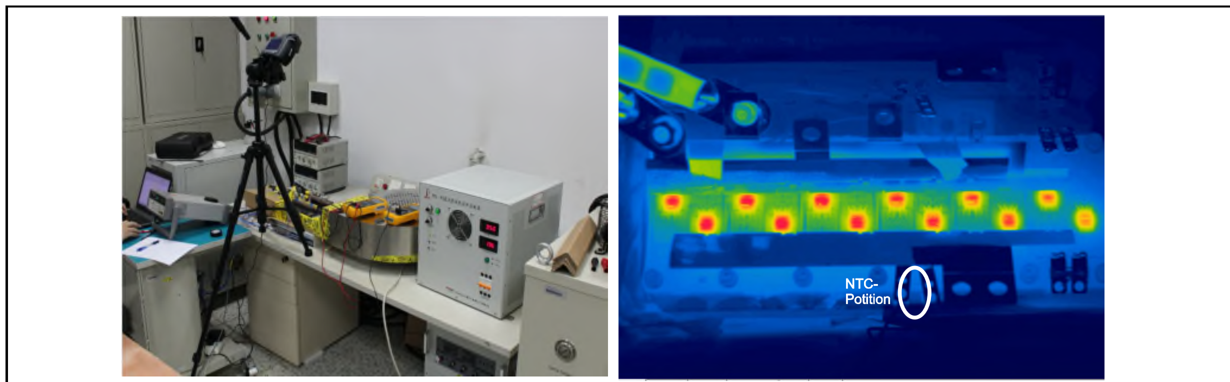

Figure 1: Left Part - Experimental Setup consisting of power module, power source, data acquisition, cooling and temperature measurement equipment. Right part - IR-Image of the device under test with power applied to the diodes only

Device under test (DUT) is a power module 1000A / 1700V, mounted to a heat sink with well-controlled forced air cooling. The air stream is measured as well to establish cooling conditions as known from the application. The chip temperature is recorded by IR-Camera. Furthermore, the case temperature below the chip is measured by thermocouples attached to the power module's base plate. The NTC's resistance is captured by data acquisition instruments and the resistance is transferred to temperature by math acc. to the semiconductor's data sheet [2]. Additionally, the NTC's resistance in Ohm is recorded to calculate the resulting temperature offline in order to generate the according correlations. The IR-Camera also allows measuring the NTC's temperature. Power to the DUT is applied from a controlled DC-source, heating up the silicon by injecting a high current at low voltage levels. From the IR-Camera, the setup can be observed as seen on the right side in figure 1.

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The current can be adjusted to achieve different temperature levels and keep the system in static condition to conduct the measurement. The values recorded are given in the table 1:

Air flow $[m^3/h]$	Current [A]	NTC $[\Omega]$	NTC by IR $[^oC]$	NTC by math $[^oC]$	T_{diode_max} $[^oC]$
206.3	50	4045	30	29.3	33
206.3	100	3500	34.5	33.4	43
206.3	200	2455	43.6	41.8	66
206.3	300	1570	57.5	53.7	96
206.3	400	1020	66.5	65.8	130
206.3	460	790	80	73.5	153

Table 1: Measurements taken from the forced air cooled setup

Correlating the values taken from the NTC $[\Omega]$ and the diode $[^oC]$, a diagram can be generated using proper calculating software. The result for $T_{Diode} = f(R_{NTC})$ is displayed in figure 2, including an equation for interpolation:

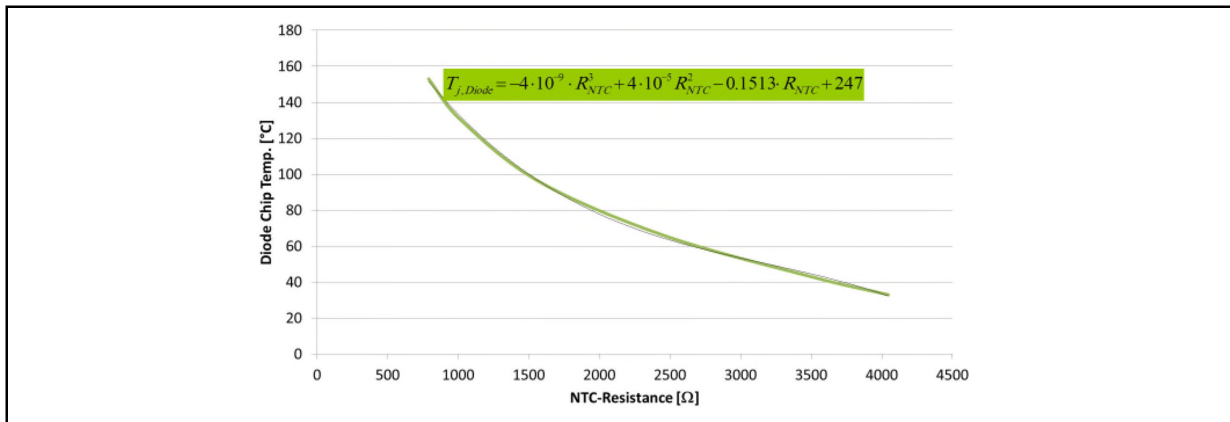

Figure 2: Correlation between chip temperature and the NTC's resistance, taken from the experiment

The nonlinear influence from the NTC can clearly be seen, a third-order polynomial is needed to accurately interpolate the values. As the NTC's characteristic commonly is given in the semiconductor's data sheet, the resistive value can be transferred into a temperature easily. In case this temperature information is correlated to the reading taken from the silicon-die, the result for $T_{Diode} = f(T_{NTC})$ reveals a linear function as depicted in figure 3:

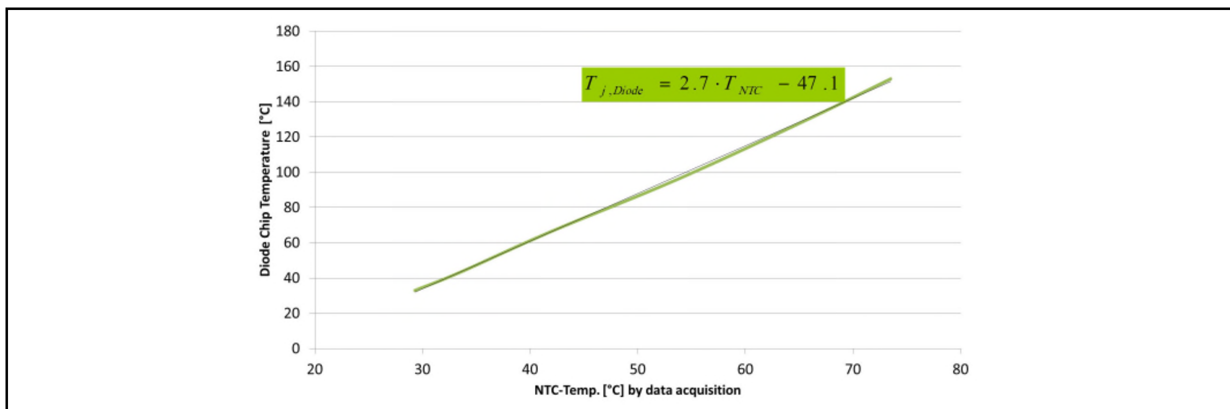

Figure 3: Correlation between chip temperature and the NTC's temperature, taken from the experiment

One major impact arises from the cooling system itself. While in forced air cooled systems the heat can spread to efficiently reach the NTC's position, sophisticated cold plates extract the heat from the die with almost no spreading. This leads to a different thermal development regarding the NTC.

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As a consequence, the difference in temperature between silicon die and NTC grows. The experiment was repeated using the same PrimePACK^{TM}3 [2] power device, this time mounted to a cold plate as can be seen in figure 4.

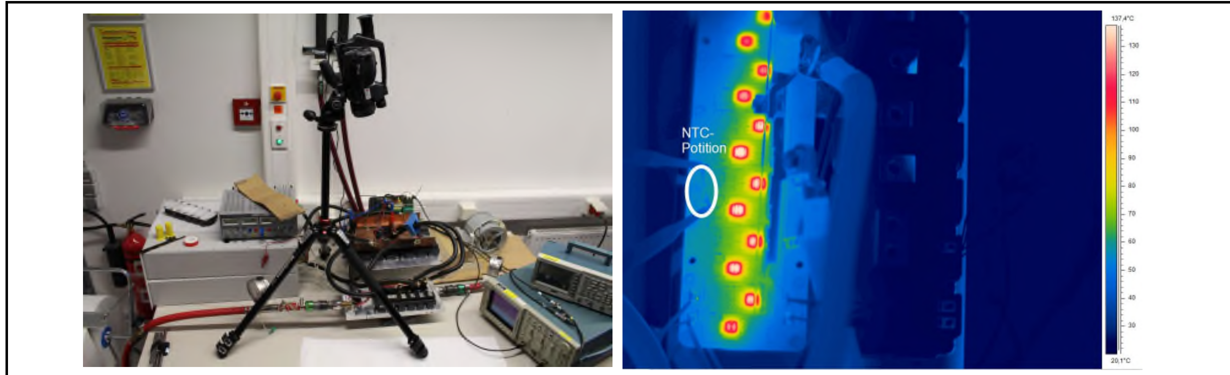

Figure 4: Left:Experimental setup utilizing a cold plate, Right: IR-Picture

Two series of measurements were conducted to examine the influence of the different cooling conditions along with a change in the liquid's flow rate. For two different flow rates, the current was tuned to achieve similar thermal conditions for the chips during the measurement. Table 2 summarizes the data gathered:

Flow rate [L/min]	Current [A]	T_{diode_max} [^oC]	NTC [Ω]	NTC by math [^oC]
5.6	300	67.5	3400	35.5
	500	115	2080	50.0
	610	145	1950	58.5
12.8	350	68	4330	28.8
	570	115	1770	37.9
	680	143	2250	42.2

Table 2: Measurements taken from the experiment using a cold plate

To compare the results, all three correlations are combined in figure 5

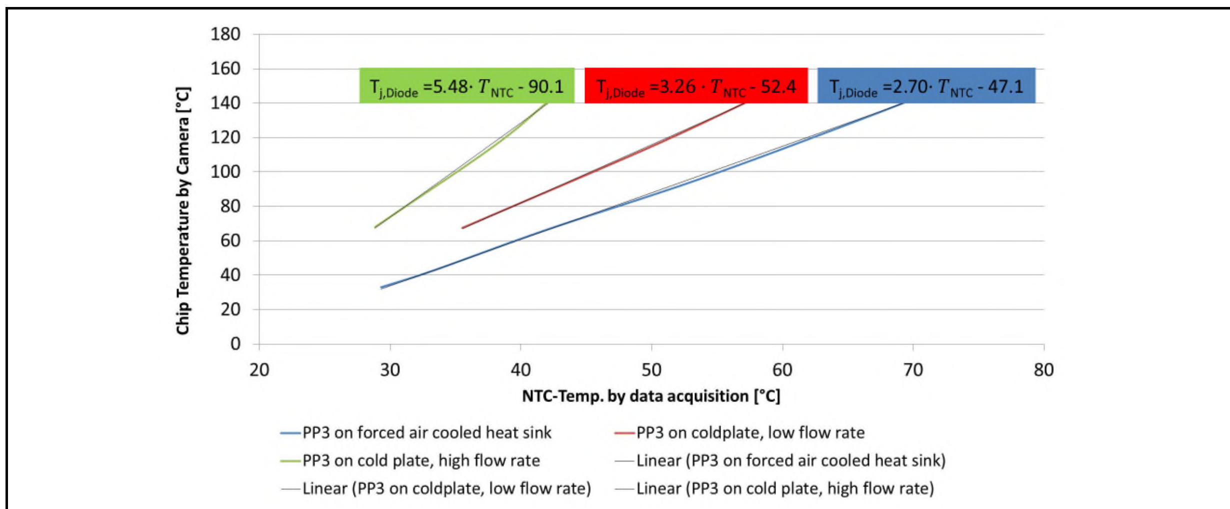

Figure 5: Chip temperature vs. NTC temperature using different cooling conditions

Consistently, higher performance of the cooling system leads to an increase in the difference between chip- and NTC-temperature. As a consequence, no generic thermal model for a bare power module can be given to satisfy every possible application. Trying to find a correlating factor in terms of thermal resistance will lead to further difficulties [3].

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2 Model Limitations

The model as described poses a basic setup to get a first impression of the thermal correlations inside the power module. However, the procedure presented contains some details that need to be considered if a more accurate model has to be generated. Especially if a trip level for overload protection has to be determined, a closer view to the temperatures has to be done.

2.1 Validity of the Approach

All the experiments conducted for this work are valid solely for static points of operation. The time constants as a consequence of the design's thermal capacitance have been eliminated by simply waiting for the setup to become static. This correlates to a duration in a range of minutes to take effect, if a forced air cooling is used. On a cold plate, static conditions are well established in a matter of 30-60 seconds. This translates to a very long reaction time of the NTC-reading, rendering it rather useless in trying to observe transient phenomena. It is common to use the NTC's data to protect a design from overload conditions. These may arise from failing cooling system like soiled heat sinks, malfunctioning fans or damaged pumps. As these are slowly growing effects, the NTC's data can be used if a proper trip level is chosen. To do so, operating the experiment with conditions closer to the real application's behavior is advised.

2.2 Hot-Spot vs. $T_{vj,max}$

For the purpose of generating a thermal model, the correlations need to refer to a *maximum chip temperature*. Using a thermographic imaging system like the infrared camera, there is a difference between the measured hot spot on a chip and what is considered the chip's junction temperature $T_{vj,max}$. The in-situ measurement described in the standards reveals a maximum chip temperature $T_{vj,max}$ as an average, covering the whole chip surface. This value is the one used to predict the lifetime of a power module regarding power cycling [4]. The IR-Camera as used in the experiment detects a hottest spot on a single pixel. A thermal model generated based on this particular value would be a very conservative one. Especially in a larger power module, the value captured by the in-situ measurement is the average of all chips. To generate a model closer to the standard, a more detailed analysis of the IR-data is required, taking averaging of all active areas into account. The details depicted in figure 6 reveal, that the maximum value detected by the IR-camera is at a bond wire, reaching 104^oC. The hot-spot on the chip's surface is slightly lower in temperature resulting in about 100^oC. The average as determined by the in-situ test would return 93^oC only.

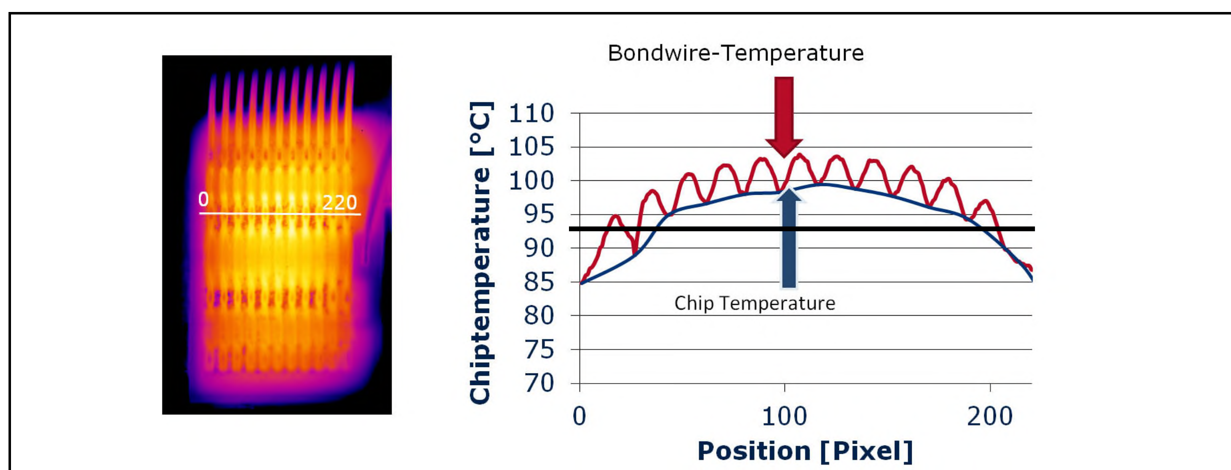

Figure 6: Detailed view to an IR-Image of a single chip revealing local temperature dependencies

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2.3 DC-Power vs. AC-Power

The experiment, for the sake of convenience, was conducted using a DC-source. This eliminates the possible cross-coupling of heat generated by the close proximity of IGBT and diode dies. As in a real application losses occur in both parts, driving the DUT by an AC-source would represent an operation closer to the real world condition. As described in [5], this can be done by using an AC-source capable to provide the power levels demanded. As an alternative, the DUT can be installed as a load into a H-bridge configuration. In this case, it would also be possible to control the point of operation in regards to the application's power factor $\cos(\varphi)$.

3 Conclusions

For a power module as a bare component, there is no general model correlating the NTC-reading to a die's temperature. To get an accurate insight into this correlation, measurements conducted in the individual design remain a inevitable necessity. Even features often regarded as being of little or even no influence have to be considered to generate a robust and reliable statement concerning chip- and NTC-temperature. IR-measurements of the temperatures developing in a power module give the most comprehensive information about thermal gradients and hot spots. It also remains the method of choice when taking all thermal influences from a given design into account in a holistic manner. Interpreting these measurements carefully allows finding a proper thermal model to correlate NTC-reading and die temperatures in static or quasi-static points of operation.

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