SiC-JFET in half-bridge configuration – parasitic turn-on at current commutation

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Abstract

This paper describes the effect of parasitic turn-on in SiC-semiconductors. The device under test is a half-bridge with 1700V normally-on SiC-JFETs. The half bridge contains 32 chips in parallel, 64 chips in total, resulting in a current rating of 480A. The module design follows the strip-line concept as published in [1]. Parasitic inductance in the power circuit amplifies the effect of parasitic turn-on. Gate inductance outside the module as well the inductance of gate and source sub-circuits inside the module play an important role in minimizing the parasitic turn-on [2, 3, 4]. To fully utilize SiC-devices in fast switching applications, an overall low inductance design is absolutely required. Thus, in combination with a special gate-drive concept, the effect of the parasitic turn-on will be reduced. The SiC-JFET shows superior performance in terms of switching losses even with some parasitic turn-on.

1. Introduction

Superior material characteristics of SiC lead to superior $R_{DSON}$ of high voltage unipolar devices, e.g. JFET. Switching speed of unipolar semiconductors is anyway as high as controlled through their gate, resulting in significant loss reduction when compared to Si devices. The low $R_{DSON}$ is also related to a much lower thickness of the active vertical zone in SiC devices. The thinner active zones lead to higher parasitic capacitance (Fig. 1) within SiC devices. Whereas most important is the ratio of gate drain capacitance ($C_{GD}$) to gate source capacitance ($C_{GS}$). This ratio is roughly twice as high as for Si-IGBT, for example. Data of Si-IGBT may be found in several available data sheets.

![Fig. 1: Parasitic capacitance Crss ($C_{GD}$) and $C_{GS}$ of a 15A/1700V SiC-JFET](image)

Within half bridges as used in motor drive application parasitic turn-on can happen during current commutation out of freewheeling mode. Parasitic turn-on can also happen within half bridges containing Si-switches (IGBT, MOSFET). For Si devices, a simple measure against
parasitic turn-on is the use of negative gate voltage in off-state, which enlarges the margin between gate off-voltage and threshold for turn-on. This option is not the applicable for SiC devices as for the normally-on JFET the negative voltage is limited by its punch through (approx. V= -22V) and for the today’s MOSFETs negative Gate voltage may cause shifts in threshold voltages towards normally-on.

2. Parasitic turn-on
A simple half-bridge configuration (Fig. 2a) equipped with a single SiC-JFET in each leg, is used to simulate the parasitic turn-on, neglecting parasitic inductance. Figure 2b shows the simulation results in case of parasitic turn-on. The curves start prior to 2nd turn-on of the low side JFET where the upper JFET is in freewheeling mode. The turn-on of the bottom JFET causes a voltage rise (drain to source) at the high side JFET. The high positive dV_DS/dt injects current into the gate through the gate-drain capacitance C_GD. If the gate resistor is too high the gate current generates a voltage at the gate, which exceeds the pinch of voltage. A transient shoot through within the half bridge is the consequence. At an off voltage of -19V (specified value) at the gate a gate resistor of 22Ω turns out to be too high to prevent parasitic turn-on, in this example.

Fig. 2a: Simple equivalent circuit with no parasitic inside. Fig. 2b: Result of the simulation at 2nd turn-on. The light green curve represents the gate-source voltage of the top JFET in the half bridge configuration. At -dV_DS/dt at the bottom JFET, i.e. +dV_DS/dt the top JFET the gate of the top JFET is pulled up by C_GD and a transient turn-on of the JFET occurs. Also seen at the peak current in I_DS, top (orange curve) and I_DS, bot (red curve), |dV_DS,bot/dt| = |dV_DS,top/dt|.

3. Experimental investigation on parasitic turn-on
3.1. Half bridge including parasitic inductance and capacitance
The circuit representing the real setup is shown in Fig. 3. The parasitic inductance and capacitance, which are affecting the peak current during 2nd turn-on of the low side switch, are included. A significant contribution (12nH) to the parasitic inductance L_p in the DC-bus comes from a coaxial shunt (10mΩ), which interrupts the strip line around the shunt. The capacitor bank consists of series connected capacitors. Four pairs of series connected capacitors are in parallel. The contribution to L_p is 6nH (12nH per individual capacitor). The inductance of the module is 5nH and the PCB (DC-bus) has approx. 1.7nH. Gate resistors,
gate inductance and $L_2$ have been varied to study their impact on parasitic turn-on. Values of Fig. 3 are just examples.

**Fig. 3:** Half bridge circuit containing parasitic inductance and capacitance. Parasitic inductance in the gates ($L_G$, $L_2$, $L_3$) and in the DC-Bus; the inductance of the DC-Bus ($L_0$) consists of the inductance in the module ($L_{10}$), the Shunt ($L_9$), the PCB ($L_4$) and the capacitors ($L_5$... $L_8$); the parasitic capacitance ($C_1$) of the load; the gate of the high side JFET is biased to -19V and the bottom JFET receives a double pulse by $V_2$.

### 3.2. 480A/1700V SiC JFET-module under test

Per leg, the half-bridge module as indicated in Fig. 4a contains 32 SiC-JFET in parallel, i.e. 64 chips in total. It results in a rated current of approx. 480A. The module design follows the rules for low inductance and symmetry according to [1] and the investigation was made with a special power-board for a press-fit interface (Fig. 4b). Gate drivers are integrated on the same board.

**Fig. 4a:** Low inductance full SiC half bridge module. 2 rows of press-fit pins for DC+ and DC-, one row of pins for phase output, 2 pairs of control terminals per leg; **Fig. 4b:** Top view on the power-board including integrated driver circuits; the shunt is placed between DC-link and module.
A slot in the $\text{DC}_{\text{minus}}$ conductor accepts the shunt. The total parasitic inductance of the setup, as concluding out of measurement, is approx. 25nH. The largest share on this magnitude has the shunt with about 12nH. The tracks on the PCB, between gate terminals and driver, are arranged as a strip-line, as well. Furthermore there are two pairs of drive terminals per switch coming out of the module. Both measures lower the gate inductance.

### 3.3. Effect different circuit parameters on parasitic turn-on

In Figure 5a the 2$^{nd}$ turn-on of the bottom JFET at $V_{\text{CC}}=900\text{V}$, $I_D=400\text{V}$ and $R_G=0\Omega$ (for top and bottom JFET) is presented. It is obvious, that for SiC devices the peak current is too high to be a reverse recovery peak of the JFET's intrinsic diode. It is a sum of different contributions. These are displacement current from parasitic capacitance of the high side switch, the load as well as current which is caused by parasitic turn-on in the upper leg.

![Fig. 5a: 2$^{nd}$ turn-on bottom JFET at $V_{\text{CC}}=900\text{V}$, $I_D=400\text{V}$, $R_G=0\Omega$; Fig. 5b: Current during 2$^{nd}$ turn-on of the bottom JFET for different gate resistors of the bottom JFET.](image)

Varying circuit parameters allow separating the different contributions. The $dV_{DS}/dt$ of the SiC-JFET is determined by the gate resistor. By increasing the gate resistance of just the active (bottom) switch, the $dV_{DS}/dt$ will be reduced from $\sim8\text{kV/µs}$ at $R_G=0\Omega$ to $\sim2\text{kV/µs}$ at $R_G=5.6\Omega$ ($V_{\text{CC}}=900\text{V}/I_D=400\text{A}$).

The parasitic turn-on reduces with $dV_{DS}/dt$ (Fig. 5b), but the dynamic losses are rising from $E_{\text{tot,0Ω}}=62\text{mJ}$ to $E_{\text{tot,5.6Ω}}=115\text{mJ}$. During turn-off the $dV_{DS}/dt$ is in general higher under the same conditions driving conditions, $\sim36\text{kV/µs}$ will be achieved. The reason for this is a different margin of the positive and negative driver voltage to the miller plateau.

Figure 6a, again, shows the current during 2$^{nd}$ turn-on of the bottom JFET. The variation is due to different impedance in the gate circuit of just the upper JFET. The first experiment was made by replacing the 0Ω SMD resistor by higher resistors. In the second experiment the gate inductance was increased by replacing the 0Ω SMD resistor by 10cm and 20cm wires. A comparison of the peak current shows a significant difference between these setups and illustrates the impact of the gate circuit impedance on the parasitic turn-on. High impedance in the gate loop hinders fast discharge of the gate during the positive $dV_{DS}/dt$. 

![Image showing current during 2$^{nd}$ turn-on of the bottom JFET for different gate resistors of the bottom JFET.](image)
Fig. 6a: Current during 2nd turn-on of the bottom JFET at different impedances just in the gate of the upper JFET. See the variation in peak current by changing the setup from replacement the 0Ω SMD resistors by 20cm wire or 5.6Ω SMD resistor. Fig. 6b: Current during 1st turn-on of the bottom JFET at different values the off state voltage at the gate of the upper JFET.

In Figure 6b the current during the 1st turn-on of the bottom JFET is presented. The variation is due to different off-state voltages on the gate of the upper JFET form -22V to -17V. By going from -22V to -17V the margin between the off-state- and pinch-off-voltage becomes reduced, more and more. The peak-current increases step by step. The dV_{DS}/dt of the active switch is kept constant. Therefore the parasitic turn-on is only affected by the off voltage at the gate. In the sections above it was shown that the effect of parasitic turn on depends on the dV_{DS}/dt across the switch, on the impedance in the gate loop and on the margin between static off-state and pinch off gate voltage.

The impact of the parasitic capacitance C_{Load} in the load (winding capacitance of the inductor) on the current peak is presented in Figure 7. The comparison of a measurement with and without the inductive load delivers the contribution by C_{Load}, i.e. 90A which is the difference of the two measurements. C_{Load} turns out to be approx. 10nF.

Fig. 7: Current during 1st turn-on of the bottom JFET. With and without load: see effect of the winding capacitance C_{Load} on the current peak.

In Figure 8 a comparison of the first and second turn on is presented. It was expected that the 1st and the 2nd turn-on will give rise to identical peak currents. As dV_{DS}/dt of the active
switch is even lower at second turn-on the peak current should be even lower at this condition. However, the comparison indicates that the peak current, and thus the effect of the parasitic turn-on are significantly higher during the 2nd turn-on.

![Fig. 8: 1st turn-on and 2nd turn-on of the bottom JFET Vcc=900V, I_D=400V, R_G=0Ω](image)

![Fig. 9: 2nd turn-on of the bottom JFET Vcc=800V, I_D=400A, R_G=0Ω. Illustrated is the drain source voltage of the top and bottom JFET. Difference in dV/dt: 8kV/µs to 26kV/µs.](image)

Figure 9 shows the 2nd turn-on of the bottom JFET in detail. The voltage V_{CC} at the module and the drain source voltage of the top and bottom JFET is illustrated. A comparison of the dV_{DS}/dt shows a significant difference from 8kV/µs of the bottom JFET to 26kV/µs of the top JFET. This can be explained by the influence of the stray-inductance of the power circuit. It is caused by the parasitic inductance in the power circuit. The dV_{DS}/dt at the top switch is different from that of the bottom switch.

\[
V_{DS_{top}} = V_{DC-link} - V_{DS_{bot}} - V_L \quad (1)
\]

ideal: \( V_L = 0 \)

\[
V_{DS_{top}} = V_{DC-link} - V_{DS_{bot}} \quad (2)
\]

\[
|dV_{DS_{top}}/dt| = |dV_{DS_{bot}}/dt| \quad (3)
\]

real: \( V_L \neq 0 \)

\[
|dV_{DS_{top}}/dt| = |dV_{DS_{bot}}/dt| - (d''I_D(t)/dt \cdot L_σ) \quad (4)
\]
Prior to the inflection point of $I_D(t)$, i.e. $d''I_D(t)/dt > 0$ and after the turning point of $I_D(t)$, i.e. $d''I_D(t)/dt < 0$. Figure 10 shows the comparison of the 2nd turn-on of the bottom JFET under the variation of the stray inductance $L_\sigma$ in the DC-link. The $dl_D/dt$ is adjusted to the same value by selection of the gate resistor. In addition to the drain source voltage of the bottom JFET and the drain current the drain source voltage of the top JFET and the voltage across the half bridge are shown. The comparison of the drain currents shows, for minimizing the parasitic turn-on, beside the gate loop inductance also the parasitic inductance in the commutation path needs to be extremely low.

**Fig. 10:** Comparison of the 2nd turn-on during variation of stray inductance by reducing the numbers of capacitors. $L_\sigma$: 25nH up to 43nH and constant $dl/dt$, $V_{CC}=800V$, $I_D=400A$, $R_{G_bot}=2.2\Omega$ to 0$\Omega$ for keeping the $dl_D/dt$ constant.

### 4. Conclusion

In this paper the effect of parasitic turn on was investigated in detail. The high current peak will cause additional dynamic losses. The dynamic losses of the 1700V/480A JFET module are compared to the dynamic losses of a 1700V/400A Si standard module (FF400R17KF6, table 1). Even though, some losses are added by parasitic turn-on, in the case of JFET, the total switching losses are approx. by a factor of approx. 7 smaller than for the Si-IGBT module.

<table>
<thead>
<tr>
<th>1700V normally-on SiC-JFET 480A module</th>
<th>1700V IGBT2 400A module</th>
</tr>
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<tr>
<td>$R_G$ [$\Omega$]</td>
<td>$E_{on}$ [mJ]</td>
</tr>
<tr>
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<td>17.6</td>
</tr>
<tr>
<td>1700V IGBT2 400A module</td>
<td>180.0</td>
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**Table 1:** Dynamic losses of a 1700V normally-on SiC-JFET 480A module a versus Si standard module type FF400R17KF6 at 125°C, $V_{CC}=900V$, $I=400A$. 
To further lower the switching losses measures should be taken to prevent parasitic turn-on in a half bridge. Low impedance in the gate drive circuit, minimum parasitic inductance in the DC-bus, lowest off voltage at the gate and some $dV_{ds}/dt$ control by different gate resistors for turning-on and –off are the measures to be taken.

5. Reference


[4] D. Domes et. al.: 1st industrialized 1200V SiC JFET module for high energy efficiency applications, PCIM 2011, Nuremberg, Germany