Real-time adjustable gate current control IC solves dv/dt problems in electric drives

Wolfgang Frank, Infineon Technologies AG, Germany, Wolfgang.frank@infineon.com
André Arens, Infineon Technologies AG, Germany , Andre.arens@infineon.com
Stephan Hörold, Infineon Technologies AG, Austria, Stephan.hoerold@infineon.com

Abstract

The tuning of commutation speed of currents between freewheeling diodes and IGBT plays an important role in respect of the EMI behavior of power electronics ([1] [6]). High dv/dt means a large stress for the motor winding insulation and motor bearings ([7], [8]) as well as it causes conducted and radiated interferences with the supply in general. Many works for speed control of IGBT turn-on are known ([2], [3], [4]) and solutions result in large and complex control units. This paper presents the benefits of a novel gate drive IC ([5]), which offers an online adjustment feature for collector emitter voltage transient dv_{CE}/dt in respect of the switching waveforms. The paper also shows, that the IC allows targeting new design tradeoffs in the application.

1. Introduction

The operation of modern inverter with pulse width modulation techniques brings a lot of negative side effects to motor drive applications. These are e.g. degradation of the winding insulation in both non-potted windings and especially in potted ones, inverter operation with shielded cables [9], PCB layout, motor bearing degradation. Fast switching devices promise lower and lower switching losses. On the other hand EMI problems and side effects increase, if one fully uses the offered switching performance. It is state of the art to solve the tradeoff between switching performance and EMI with the design of the gate resistor including an optional gate-emitter capacitor. This procedure results in a fixed compromise, which must cover low load operation and high load operation as well. However, performance and therefore also efficiency is lost by the fixed gate resistor. An adjustable gate resistor is needed to close that gap.

A recently proposed concept for a gate current controlled turn-on of IGBT [5] is used in this paper, which is realized now as an integrated IC as a part of Infineon´s EiceDRIVER™ portfolio. The paper investigates the dv_{CE}/dt and di_C/dt transients during current commutation from diode to IGBT. The effects are described and functions of the IC for controlling the slew rates of current and voltage of IGBT during turn-on are explained in detail. A number of innovative, additional functions for controlling efficiently modern power electronic systems such as three level inverters are described as well. Practical measurements show the advantages of an online adjustment of the slew rate control. Furthermore, specific IC features for overcurrent and desaturation detections for the use in 3-level-inverters are explained.

2. Pin configuration and clustering

The turn-on gate current control IC provides two different voltage domains on the input side. The 5 V power supply domain (dark blue) supplies the main parts of the IC as well as the coreless transformer insulation barrier. This covers the terminals VCC1, GND1, SIGI and SIGO.

ISBN 978-3-8007-3603-4

There is additionally the control domain comprising the terminals /FLT, RDY1, RDY2, PADP, INP, INN, EN, PADN and SPEED (green shaded), which can be supplied with the voltage levels of 3.3 V, 5 V, and 15 V. This allows designing this device into moderate noise environments with the 3.3 V and 5 V levels, but also into harsh noise environments by using control signals of a 15 V level. This voltage domain is supplied by the terminals PADP and PADN.

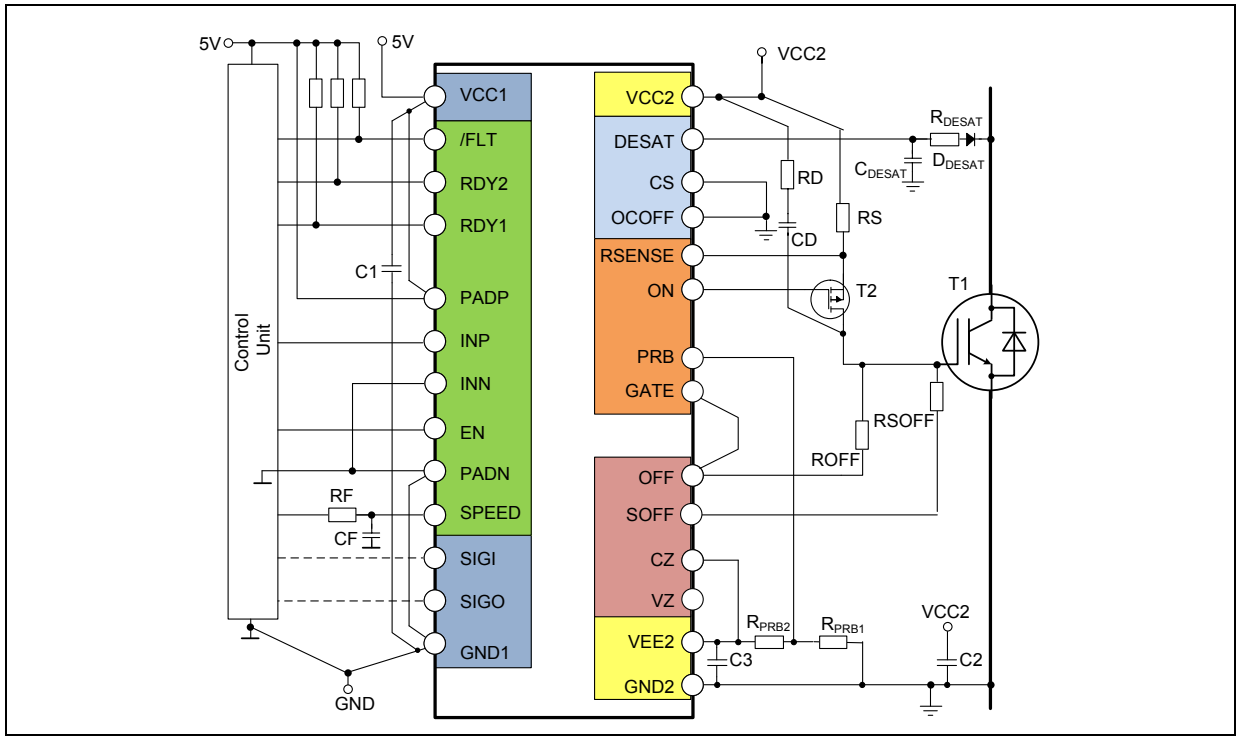

Fig. 1: Pin configuration of the new EiceDRIVER™ IC with gate current control in a typical application

The supply terminals on the output side are VCC2, GND2 and VEE2 (yellow shaded). The output side allows a bipolar gate voltage supply for avoiding dv/dt triggered parasitic turn-on. The red shaded terminals RSENSE, ON, PRB, and GATE belong to the gate current turn-on control loop. The light blue shaded area comprising the terminals DESAT, CS, and OCOFF are dedicated protection terminals for short circuit detection, overcurrent detection by shunts or sense IGBT and three-level inverter support, respectively.

The turn-off cluster (purple shaded) of terminals on the outside contains the two-level turn-off function (terminals CZ, VZ), the turn-off terminal OFF and the soft turn-off terminal SOFF. The latter is activated only in case of desaturation of current sense triggering, when initiated from the output side.

The typical application circuit shows that the additional circuit for the gate current control loop needs only a limited small number of components. It is even the same complexity, when comparing to state-of-the-art gate drive circuits which use gate resistor control and external booster circuits for the gate current amplification.

3. Three level inverter support (NPC 1 topology)

It is the major advantage of three level inverters in NPC 1 topology that IGBT with lower breakdown voltage compared to the total DC link voltage can be selected. IGBT with a breakdown voltage of 650 V can be selected for a DC link voltage of e.g. V_{DC} = 800 V. Such IGBT offer much better switching and conduction performance. However, critical conditions

ISBN 978-3-8007-3603-4

in terms of blocking voltage can occur as it is shown in Fig. 2 in cases of overload conditions. Many gate driver IC offer protection functions, e.g. the desaturation detection, which results in an automated turn-off of this particular transistor.

The positive DC link voltage is applied to the load, when transistors T1 and T2 are turned on according to a) in Fig. 2. A critical situation can occur, when an overload is detected at transistor T2 and T2 is automatically turned off by the driver IC. This means, that the current will commutate to diodes D3 and D4. The phase voltage is the negative DC link rail now. The transistor T2 is therefore stressed by the full DC link voltage, since transistor T1 is still turned on, which can break down this transistor according to b) in Fig. 2.

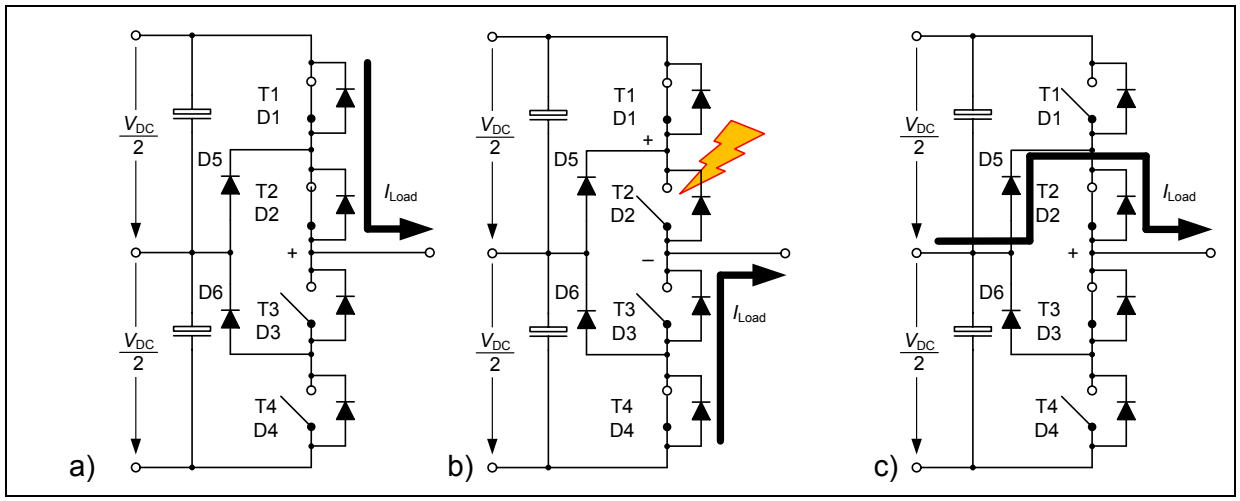

Fig. 2: Phase leg of a three level inverter in NPC1 topology in normal operation (a), condition of inner switches off (b) and arm short circuit safe condition (c)

A safe state in this case is to control a zero voltage to the phase according to c) in Fig. 2. It is mandatory in this case that the driver IC detects the overload condition, but does not turn-off transistor T2 automatically.

The described gate current control IC offers the option to suppress the automatic short circuit shut down mechanism by pulling up the terminal OCOFF to the output supply voltage VCC2. Only a fault signal is transmitted to the control side, so that the application control can manage this situation properly and in time. Therefore, the two control IC for T1 and T4 according to Fig. 2 are turned-off by default, while the gate driver IC of T2 and T3 respectively wait for instruction. One can turn-off T2 and T3 by means of deactivating the enable function in that case. This results as well in a soft turn-off.

4. Gate current control IC during turn-on process

The most innovative feature is the gate current control function. The new gate current control IC divides the turn-on process into three sections according to a) in Fig. 3: The first section (t0 to t1) is the charging from a negative voltage to a defined value in the range of v_{GE} = 0. This section is called the pre-boost section and lasts for a fixed duration of t_{PRB} = 135ns. The preboost current level I_{PRB} during this phase is adjustable for each individual IGBT type. The second section (t1 to t3) is the gate control section. The instantaneous constant gate drive current I_{gg} can be adjusted within 11 different values. The IGBT gate voltage passes the Miller voltage level during this time. The practical application of the device proposes usually a smaller turn-on gate current I_{gg} compared to the preboost current I_{PRB}. Nevertheless, it is possible also to achieve even larger turn-on currents I_{gg} than the preboost current I_{PRB}. This is shown in b) of Fig. 3. Finally, the gate is fully charged up to the desired gate voltage level in section 3 (t3 to t4).

ISBN 978-3-8007-3603-4

The used gate drive IC is able to control the dv_{CE}/dt transient of IGBT by selecting a suitable current level during phase 2. The selection of the gate resistor is therefore more tolerant with an adjustable gate current source compared to a pure resistive gate control, which only applies a constant gate voltage to the gate resistor. Please note that the turn-on delay time $t_{d(on)}$ is now very constant and predictable. This has effect on the design of the dead time, which can be smaller now.

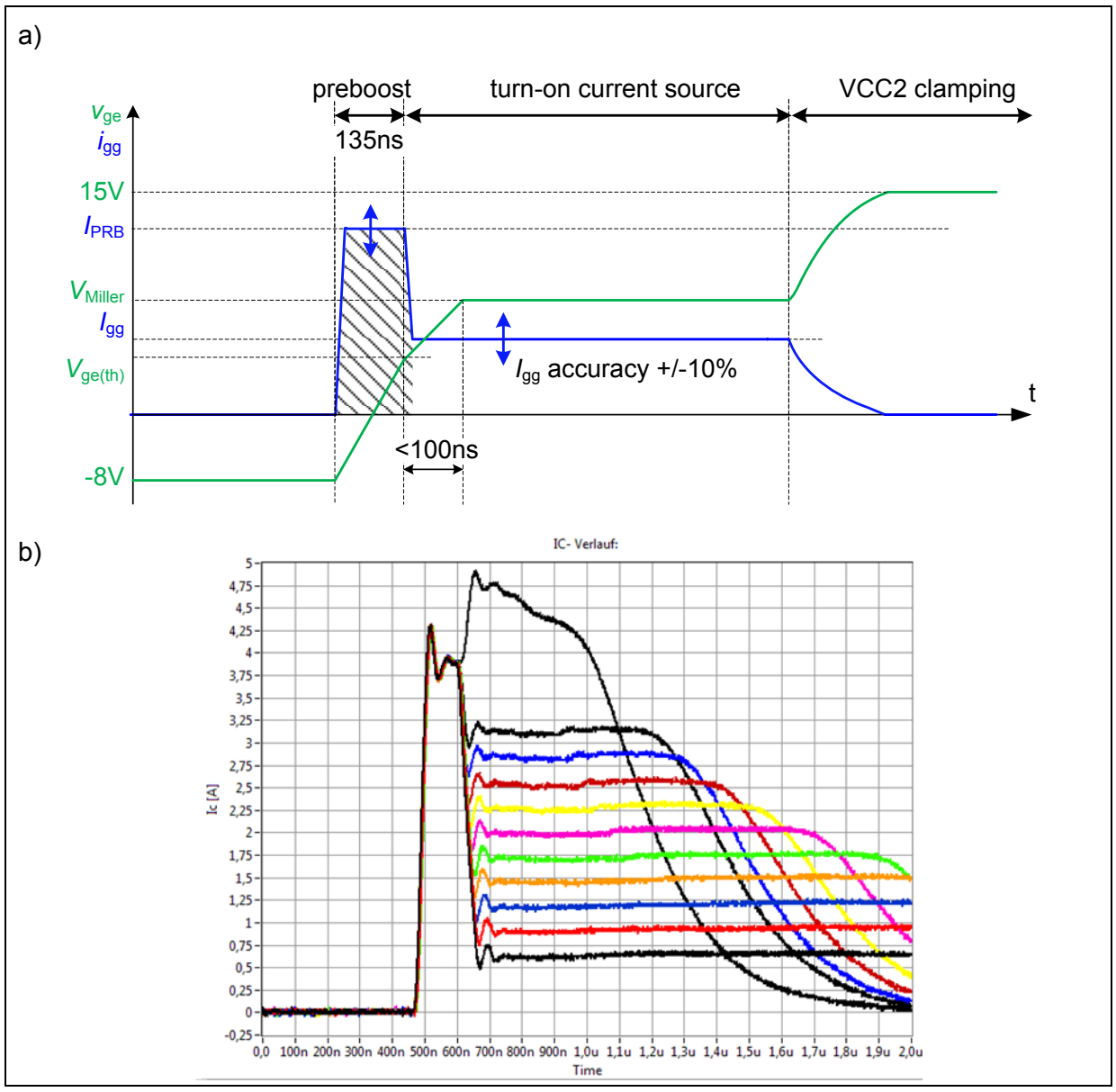

Fig. 3: The three phases of a turn-on process with (a) theoretical waveforms for gate current (blue) and voltage (green) and (b) measured waveforms of gate current for speed levels 1-11

The IC controls the gate current by means of closed loop current source circuit, which consists of a p-channel MOSFET and a current sense resistor. The current source is extremely precise with a tolerance of ± 10% during the turn-on phase. This solution is cheaper than a similar setup using bipolar transistors. Additionally, the p-channel MOSFET provides a rail-to-rail capability, which is not possible with bipolar transistors. The EiceDRIVER™ IC can control in total up to 3 p-channel MOSFET BSD314SPE in parallel, which covers a range of current classes up to 900 A of 1200 V modules.

ISBN 978-3-8007-3603-4

5. Effect of gate current control IC on transient collector-emitter voltage at turn-on

The adjustability of the controlled gate current allows the design engineer to change paradigms concerning the switching speed of the diode. The controlled gate current results in a much smoother transition voltage from transistor to the freewheeling diode. Another advantage is, that the turn-on propagation delay is more predictable compared to a pure resistive turn-on as discussed in section 4.

Fig. 4 shows the range of dv_{CE}/dt rate over various speed setting and over temperature. It can be seen, that the control range of the gate current control IC is sufficient to cover the same range as with a common fixed gate resistor control, while having the advantage to change the dv_{CE}/dt rate online during operation. So the commutation speed is not limited to a single curve, but rather can now cover an area of possible dv_{CE}/dt values.

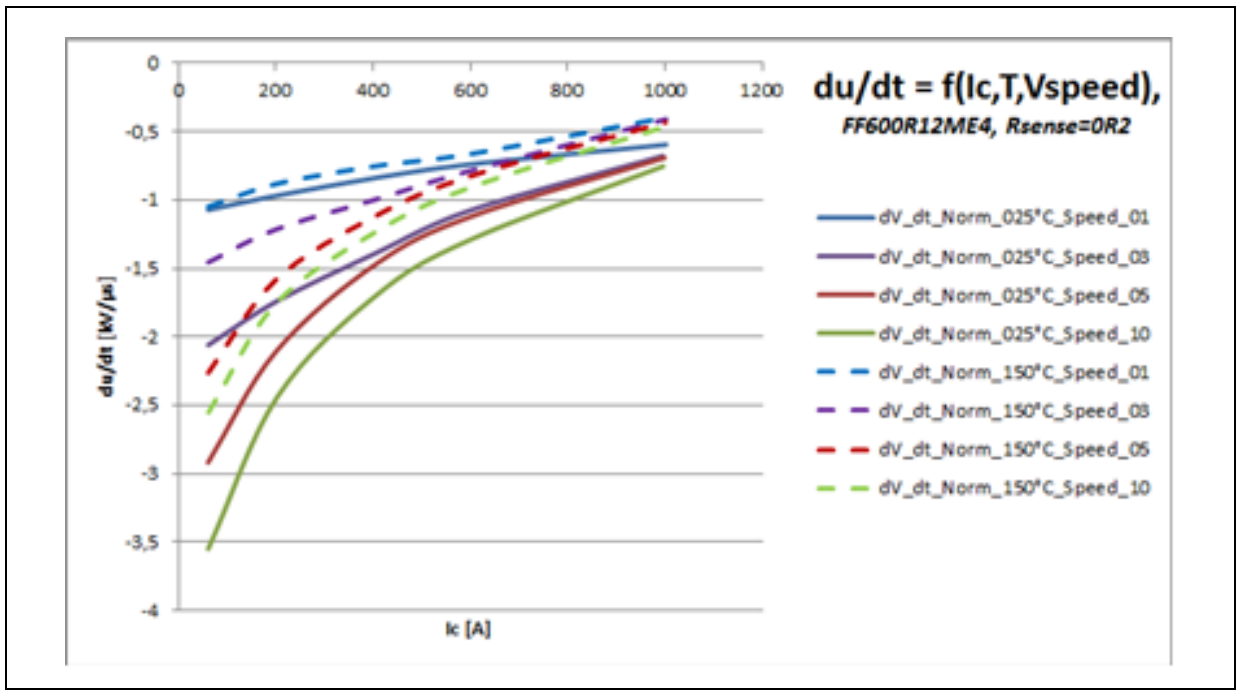

Fig. 4: Coverage of dv_{CE}/dt range by gate current control IC for speed step 1,3, 5, and 10 at IGBT junction temperature of 25°C

The fact of the new adjustability of dv_{CE}/dt has a high importance for the lifetime of motor windings and motor bearings. Investigations already showed that the cost for filters or other countermeasures to limit the dv/dt are expensive ([10]) relative to the cost of the drive. A control of the dv_{CE}/dt means that countermeasures for reducing the dv_{CE}/dt (e.g. filters) can be reduced or even skipped, which is an important step towards system cost reduction. Also maintenance cycles for motors may be longer. Fig. 4 proves that it is now possible stay below the critical values of dv_{CE}/dt in the application by setting the commutation speed according to the instantaneous electrical conditions of the application.

6. Application test

The behavior of the real-time adjustable closed loop gate current control is shown in Fig. 5. The individual applied speed steps are indicated with “x” and the amplitude corresponds to the voltage at terminal SPEED. It can easily be seen, that the speed steps follow the sine

waveform of the motor current. Therefore the switching speed and thus the switching losses are following the motor current: A higher motor current is related to a relatively lower switching loss. However, some deviation is visible. The interval of higher speed steps is shorter compared to interval of low speed steps. This is caused by a delay in the transmission of the speed step into the output section the control IC. The delay is defined with a maximum of 120µs. The delay can be treated as kind of a dead time. It is therefore possible to correct it by a predictive setting of the voltage at terminal SPEED.

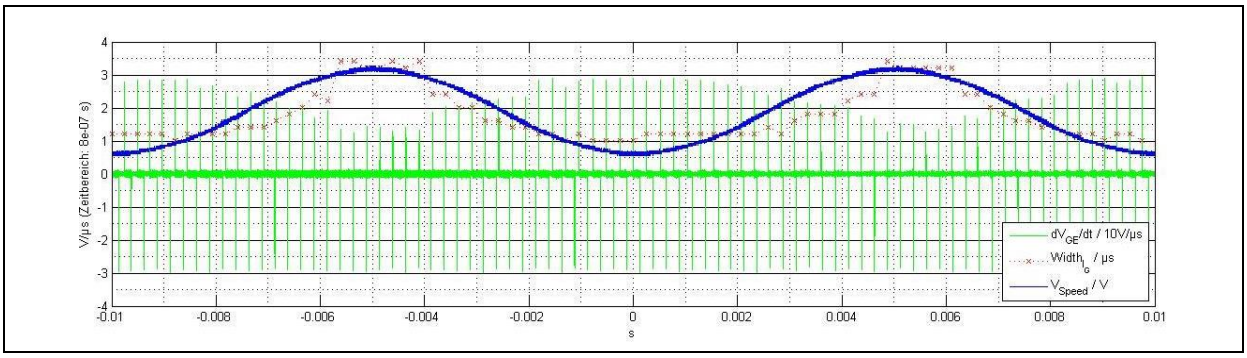

Fig. 5: Application measurement (collector-emitter voltage 100V/div green, collector current 10A/div red)

7. Conclusion

This paper discusses the advantages of a novel gate current control IC concept, which uses a closed loop gate current control for turn-on. The turn-on properties can be adjusted in real-time during operation of the IC. It is shown by a switching test example, that gate drive IC can control a wide range of collector-emitter transient voltage dv_{CE}/dt. In the discussed example, values from 1kV/µs up to 3.5 kV/µs at small collector currents is achieved, which is superior over only 1 trade-off line when using a common gate resistor control. This result helps to reduce the size of motor and EMI filters or omits them at all and therefore reduces the system cost significantly.

Commonly used gate resistor driven IGBT show also a strong variation of the turn-on propagation delay over the collector current. It is shown here that the turn-on process is now predictable in respect of turn-on propagation delay and independent on collector current.

8. Reference

[1] E.R. Motto, J.F. Donlon: Speed Shifting Gate Drive for Intelligent Power Modules; Proceedings of the Advanced Power Electronic Conference 2006, USA, 2006

[2] Y. Lobsiger, J.W. Kolar: Closed-Loop IGBT Gate Drive Featuring Highly Dynamic di/dt and dv/dt Control; Proceedings of ECCE 2012 conference; Ort, Land, 2012.

[3] Y. Lobsiger, J.W. Kolar: Closed-Loop di/dt & dv/dt Control and Dead Time Minimization of IGBTs in Bridge Leg Configuration; Proceedings of the 14th IEEE Workshop on Control and Modeling for Power Electronics (COMPEL 2013), Salt Lake City, USA, 2013.

[4] V. John, B.S. Suh, T.A. Lipo: High-Performance Active Gate Drive for High-Power IGBT's; IEEE transactions on industry applications, Vol. 35, No. 5, USA, 1999

[5] A. Arens, et al.: Get tuned – A new generation of driver IC including safe isolation by coreless transformer technology; Proceedings of PCIM Europe 2013; Nuremberg, Germany, 2013.

[6] F. Hille, W. Frank: A new high voltage diode technology with reduced switching losses and improved softness; Proceedings of PCIM Europe 2007, Nuremberg, Germany, 2007.

[7] A. v. Jouanne, P. N: Enjeti: “Design considerations for an Inverter Output Filter to Mitigate the Effects of long Motor leads in ASD applications”; IEEE transactions on industry application, Vol. 33, No. 5; 1997

[8] A. v. Jouanne, H. Zhang, A. Wallace: „An evaluation of mitigation techniques for bearing currents, EMI and over-voltages in ASD applications”; IEEE 1997

[9] J.O. Krah, et al.: „Besonders energieeffizienter, motorintegrierter Umrichter mit SiC-MOSFETs”; Proceedings of SPS/drives/IPC conference, Nuremberg, Germany, 2013

[10] Gambica.: „Variable speed drives and motors”; Technical report No.1, 3rd edition, GAMBICA Association Limited, London, Great Britain, 2006