

Improving Efficiency in AC drives: Comparison of Topologies and Device Technologies

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Abstract

New standards for power losses measurements for variable speed drives are presented. The power losses of typical variable speed drives are analyzed and future alternatives to increase their efficiency investigated. Solutions with Silicon (Si) technology in Three-Level or Silicon/Silicon Carbide (SiC) as well as full SiC systems in Two-Level topology are shown to increase the inverter efficiency.

Introduction

Gradually standards have been created defining methods to measure the efficiency of variable speed drives VSD and motors at different speed and load torque values. Future requirements of efficiency classes for general purpose drives (GPD) are also foreseen, similarly what has been established for industrial motors in Europe since 2009 with the Ecodesign Directive [1] [2]. Once those techniques and requirements for measuring the efficiency of VSD are established, the drive companies will focus on increasing the efficiency of their products accordingly. This will be achieved through the use of modern and more efficient power switches, more efficient pulse width modulation PWM techniques, more complex power circuit topologies, and the reduction of the energy losses in other components of the drive system.

This article analyses the distribution of power losses in three typical VSD applications: general purpose drives (GPD) used in industry, VSD for elevators (lifts), and VSD for high-speed motors. These drives applications show different requirements for the power semiconductors. Possible scenarios are discussed based on current and future power switching devices and topologies, and using typical operating conditions for the different drive types. The impact of new components and technologies is compared for the mentioned application fields.

Applicable Standards and Requirements

The current requirements from IEC are focused on the influence of the VSD on the motor efficiency at speeds close to motor rated speed. The IEC 60034-25 defines the method of summation of losses in order to evaluate the impact of a VSD control on the efficiency of a motor with sinusoidal supply.

In March 2013, the C838-13 standard was issued in Canada [3]. This standard defines a methodology based on the output/input power measurement to evaluate the efficiency of VSD and motors up to 750V AC at different speed and torque values. All the requirements from AC power supply, the instrumentation and the dynamometer used to impose the load torque in the motor shaft are carefully defined in this standard. In this way the differences of the results from test laboratory to test laboratory are minimized and the results comparable.

Typical VSD losses and Efficiency values

Three different VSD types driving 22 kW motors and fed from 400V three-phase line are analyzed and their typical loss distribution is shown. The main components of the VSD, the operating conditions and the main motor data used in the subsequent analysis are collected in the Table I. The selected IGBT modules represent the current state-of-the-art solution.

TABLE I

Current state-of-the-art reference VSD components and conditions for three different applications

Parameter	GPD	Elevator	High Speed
Line supply	400 V / 50 Hz / Z=1 %	400 V / 50 Hz / Z=1 %	400 V / 50 Hz / Z=1 %
Rectifier	DDB6U144N16	DDB6U144N16	DDB6U144N16
DC reactor	6 %	6 %	6 %
DC capacitor	1410µF/400V	1410µF/400V	1410µF/400V
IGBT inverter	FS75R12KT4	FS100R12KT4	FS150R12KT4
f_{sw} [kHz]	5	10	16
U_{dc} [V]	621	621	621
U_{out} [V]	400	400	400
Modulation index (m)	0.91	0.91	0.91
Heatsink temperature [°C]	90	90	90
Motor type	AC-Induction	AC-Induction	PM
Fundamental Frequency [Hz]	50	50	1500
$\cos(\varphi)$	0.85	0.85	0.56
η_{motor} [%]	92.3	92.3	95.0
I_{out} [Arms]	40.5	40.5	60.0
Motor output power [kW]	22	22	22

VSD have specific requirements depending on the intended application. The switching frequency of the power switches is an important parameter and has a significant influence on the VSD efficiency.

In Figure 1 the typical power circuit for GPD, elevators and high-speed drives is depicted.

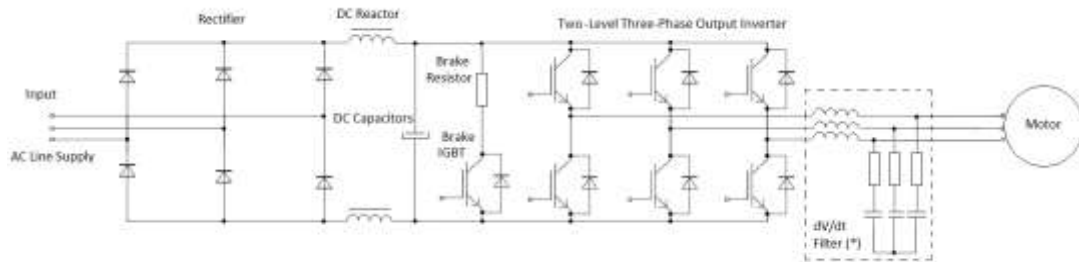


Figure 1: Typical power circuit topology of a three-phase VSD. The dv/dt Filter is typically requires in high-speed drives application only.

The losses for the inverter semiconductors were calculated with IPOSIM [7], the losses of the other VSD components were calculated with computer simulations using a simplified circuit diagram, where the output inverter is modeled by current sources. The results are shown in Figure 2.

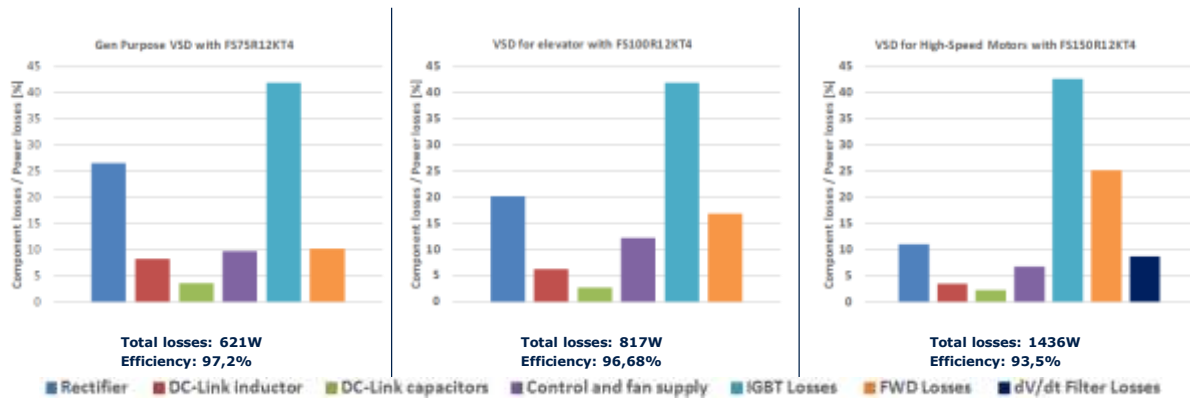


Figure 2: Losses distribution in the VSD for different applications. Operating conditions are given in Table 1.

GPD

It can be seen that in the GPD 52 % of the VSD losses are related to the IGBTs and FWDs conduction and switching losses. The rated VSD efficiency $\eta_{VSD-GPD1}$ is 97.2 % in this case, with 5 kHz switching frequency.

Elevator

The diagram in the middle of Figure 2 shows the loss distribution of a 22kW elevator VSD operating at 10 kHz switching frequency. The higher switching frequency compared to the GPD is to explain with the need of low audible noise in this application. Based on this Figure it is visible that the losses are even more concentrated in the IGBTs and FWDs, 59%, and thus the rated VSD efficiency $\eta_{VSD-LFT1}$ is 96.68 %.

High-Speed Drives

The high-speed drives require higher switching frequencies. An AC induction motor or a Permanent Magnet motor (PM motor) with 2 poles specially designed for high speed operation can achieve up to 90,000 rpm, requiring a fundamental frequency (f_0) of 1.5 kHz. Typically the PWM switching frequency (f_{sw}) requirement is $f_{sw} \geq 10 \times f_0$. In order to achieve 1.5 kHz fundamental frequency at VSD output a PWM switching frequency higher than 15 kHz is required. Here the value of 16 kHz was chosen for the losses analysis. The standard topology can be used but, in order to deal with the switching losses, the IGBTs must switch faster in comparison to the GPD, leading to higher values of dV/dt. A LC filter is normally used in between the VSD output and the motor to protect the motor winding insulation (Figure 1). The Figure 2 (right) shows a typical loss distribution of a 22 kW VSD at 16 kHz switching frequency. The power module chosen was the FS150R12KT4 EconoPACK™ 3 due to the higher current and switching frequency when compared to the GPD example of the same power. The IGBT junction temperature is kept below the maximum allowed value according to the IGBT datasheet. The output dV/dt filter losses are additionally considered in this case. The VSD efficiency $\eta_{VSD-HS1}$ is 93.5 %.

Alternatives to increase the efficiency of the VSD

Two ways for the loss reduction in the power electronic part of the standard converters are possible: the use of other topologies or the use of new semiconductor technologies. The result of the loss calculations for the semiconductors in the inverter part using different solutions is depicted in Figure 3. The selected devices for the comparison are shown in Table II.

Table II

Top.	GPD	Elevator	High-Speed
2L Si	FS75R12KT4	FS100R12KT4	FS150R12KT4
3L Si	F3L75R07W2E3_B11	F3L100R07W2E3_B11	F3L150R07W2E3_B11
2L Si/SiC	80A HS3 + SiC FWD	80A HS3 + SiC FWD	80A HS3 + SiC FWD
2L SiC	45A SiC Switch	45A SiC Switch	60A SiC Switch

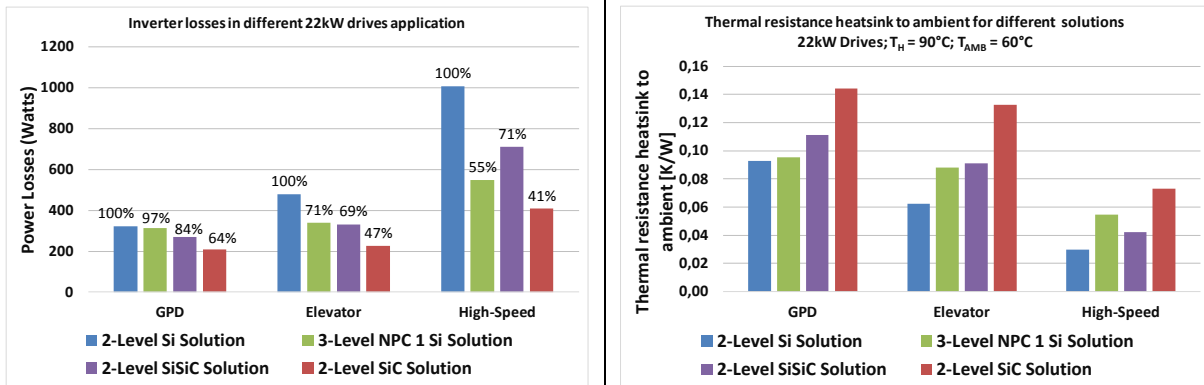


Figure 3: Left: Typical power switching losses of 22 kW VSDs, 2-Level Si Solution as 100% reference: GPD ($f_{SW}=5$ kHz), Elevator ($f_{SW}=10$ kHz) and high-speed ($f_{SW}=16$ kHz). The power modules are according to Table II. Right: Cooling effort for the different solutions

GPD

On the left side of Figure 3 is visible how much the power losses can be reduced using a Three-Level topology or 2-Level topologies with hybrid module or full SiC solution. The GPD application operates at 5 kHz and profit least from a NPC 1 solution. The higher conduction losses of the NPC1 Three-Level topology make the efficiency similar to the standard topology in the lower switching frequency region.

Elevator

The elevator inverter profits more from a Three-Level Silicon or Two-Level Silicon Carbide solution due to the with 10 kHz higher switching frequency. With the Three-Level Si and the Two-Level Si/SiC topology the losses are reduced by ca. 30% and with the Two-Level SiC system this reduction reaches 53%.

High-speed Drives

With even higher switching frequency the benefits of the new systems are more pronounced. The calculation for the VSD for high-speed motors results in the biggest loss reduction compared to the other two examples. A Three-Level Si solution achieves 45% loss reduction compared to a today's Two-Level Si system. The Two-Level full SiC solution achieves 59% loss reduction. The hybrid-solution, Si IGBT and SiC Free-Wheeling Diode (FWD), decreases

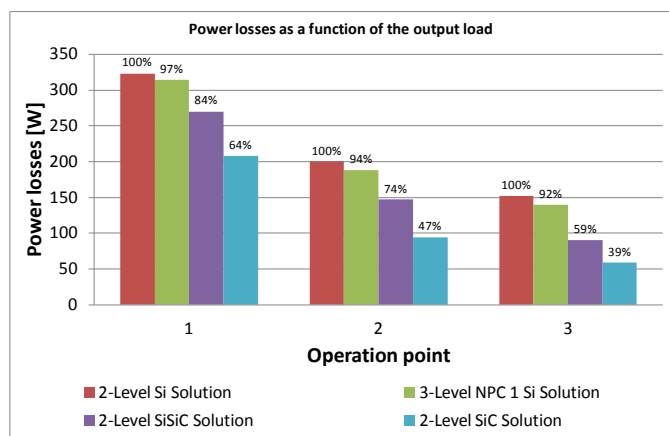
29% the losses. It becomes clear that the higher the switching frequency in the application the higher is the energy savings from the use of a NPC 1 Three-Level or of a full SiC Two-Level solution.

The reduction of the power losses brings the advantage of reducing the cooling effort of the system. In the right side of Figure 3 a diagram is depicted that shows the required heatsink performance. The thermal resistance can be increased accordingly for the more efficient solutions, which lead to a reduction in inverter size and costs [4].

Losses at different operation points

No application that uses an inverter to control a motor is working only in one torque x speed operation point. Therefore, it is important so evaluate the power losses of the system also at different load conditions. Figure 4 shows the losses of the GPD system at the operation conditions documented in Table III:

Operation point	1	2	3
Motor speed (100%= rated motor speed) [%]	100	75	50
Motor Torque (100%= rated motor torque) [%]	100	56	25
Inverter Fundamental Frequency [Hz]	50	37,5	25
Inverter Output Voltage U _{out} [V]	400	300	200
Inverter Modulation index (m)	0,91	0,75	0,5
Motor Current I _{out} [Arms]	40,5	27	21
Motor Power Factor Cos(φ)	0,85	0,8	0,51



Right: Table III: Operation conditions considered. Left: Figure 4: Power losses at different load and speed conditions for the 22kW GPD example

All evaluated solutions have at reduced speed and torque conditions higher saving in power losses then compared to the full load conditions. The fact that the most of the drives applications are operated at medium load enhanced the advantages of the use of new topologies and technologies to reduce the losses. At operation point 3 a loss reduction of 61% was with the Full-SiC Two-Level Solution. The same improvement at this load conditions is expected in the elevator and high-speed drives.

Impact of three-level and Silicon Carbide devices

The new approaches will bring benefits for the inverter manufactures: the reduction of power losses will enable lower energy consumption during the application and better classification of the VSD in the efficiency standard. Also the cooling efforts can be decreased, reducing the heat sink, size and volume and so increasing the inverter power density.

Three-Level Topology

The Three-Level topology has some advantages, like lower stress of the motor insulation and lower motor current ripple, compared to a Two-Level solution with same switching frequency. However, the change to this topology requires more development resources from the drives manufacturers and higher number of IGBTs and gate-drivers.

Etot = f (dV/dt)

With the use of wide-gap-band devices like SiC the dynamic and static losses of the semiconductors can be reduced significantly. The Two-Level SiC topology does not require, in principle, significant changes at the driver controller. The Figure 5 illustrates the dV/dt and the corresponding switching losses for a 1200V SiC 45A switch [5]. The single points show the maximum achievable values for a High-Speed 3 IGBT and SiC FWD combination.

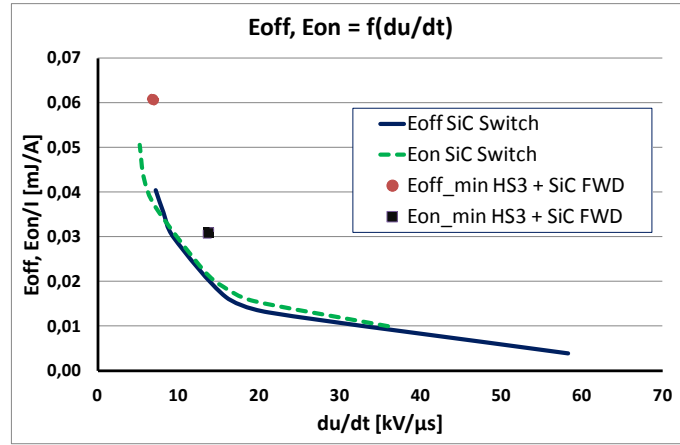


Figure 5: Eoff respectively Eon as a function of dv/dt. The switching energy is scaled with current.

It becomes visible, that a 1200V SiC Switch can achieve dv/dt values in the range of 60kV/μs at turn-off and 36kV/μs at turn-on. This leads to 1/10 of turn-off and 1/3 of turn-on losses compared to an IGBT High-Speed 3 and SiC FWD combination. The variation of the dV/dt was achieved by changing the gate resistor value.

Motor windings, bearings and inverter dV/dt

If at one side, the fast switching behavior of the SiC switch leads to lower switching losses, on the other side the high dV/dt will be a challenge to the driven electrical motor. The issues related to the PWM signals with higher dV/dt obtained with SiC switches applied to the motor cables and motor windings must be considered. Also the risk of damage of the motor bearings [6] has to be taken into account.

The lifetime of the insulation system of industrial motors is typically reduced at higher dV/dt and at higher peak voltages. The operation with dV/dt values higher than 5 kV/μs, although allowed from IEC 60034-25 [8] are frequently restricted by motor manufacturers. Table IV shows an example of the maximum allowed dV/dt for different rated motor voltages:

Motor nominal voltage	Maximum overvoltage peak on the motor terminal	Maximum dV/dt on the inverter terminal
460V	1600V	5.2 kV/μs
460V – 575V	1800V	6.5 kV/μs
575V – 690V	2200V	7.8 kV/μs

Table IV: Maximum allowed dV/dt for different motor voltage classes [9].

A maximum dV/dt of approximately 8kV/μs also for 460V motors could be achieved with the use of the insulation system from 575-690V motors. This is far away from the 60 kV/μs value possible with 1200V SiC-Switch. The slowdown of the switching behavior of the SiC Switch is possible, but this is questionable due to the increased losses. The reduction to 8kV/μs for the

full SiC can be achieved, but the losses will be then comparable to the losses from a IGBT and SiC FWD combination, making the full SiC solution non attractive.

dV/dt Filter

A way to use the whole potential of losses reduction with the fast switch is the implementation of a dV/dt filter on the inverter output. Doing that, the semiconductor can switch at maximum speed and the filter avoids that the motor windings are stressed with high dV/dt and peak voltages. This is already implemented in high-speed drives. In various studies [10,11,12,13,14,15] dV/dt filters are presented and an improved filter solution can be achieved with connection of the dV/dt filter to the middle potential of the DC-Link. Therefore a dV/dt filter implemented inside the inverter and planned during the inverter development is a good way to use the whole potential of SiC-Switches. The negative aspects with this solution are the additional components and the losses at the dV/dt filter.

New motors with reinforced insulation system together with a minimized dV/dt filter will be alternatives to use the full potential of SiC switches.

EMC Behavior and dV/dt

The higher dV/dt tends to worsen the EMC, in particular the electromagnetic emission. Also the risk of damage of the motor bearings [6] has to be taken into account. The study in [16] shows that, for short motor cables, emissions are mainly related to the inverter output common mode voltage and the dV/dt at turn-on. The EMC performance has to be taken into account during the development and test of the inverter, since the SiC Switch can achieve during turn-on a dV/dt of 36kV/μs.

Low inductance system design

The geometry of the interconnection of DC-Link, bus bars and chips will play an important role with the use of very fast switches with high current density. The DC-link circuit must have low stray inductance to avoid high overvoltage and oscillations during turn-off [17]. A careful selection of the DC capacitors, IGBT modules and bus bar design is required [18].

Conclusion

The current work in the standard organizations as IEC and CSA focused in the development of standards for the power loss measurement and classification of motor drive systems. These regulations will enable the comparison of the efficiency from different VSD for the end-user. This, together with the general trend towards lower energy consumption, will lead to a higher pressure on the drives manufacturer to improve the VSD efficiencies. In addition, the users should take the data from GPD efficiencies and losses at different speeds and loads as defined in the standards, to estimate the efficiency at different application conditions and according to the speed-torque load curve. By this approach, it should be possible to compare different GPD at realistic operating conditions including load characteristics, not only at rated conditions.

This paper presented three ways of efficiency improvement for three different VSD applications. The Three-Level topology, the Two-Level Si/SiC and the Two-Level SiC solution will allow for a significant reduction of the semiconductor losses. Depending on the drives application and the operation point of the connected motor, the losses of the inverter can be reduced by 61% using SiC switches compared to today's standard solutions. The search for a better efficiency classification level according to the future standards together with the benefits of lower losses, like smaller heat sink, lower energy consumption, and smaller housing, will overcome the technical challenges pointed out in this study.

The dependence of the switching losses from the dV/dt will play an important role in the drives application in the future. This, together with the combination of improved motor

insulation and dV/dt filter can provide more optimized solutions for the motor windings insulation challenge.

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