Impact of module parasitics on the performance of fast-switching devices

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Abstract

The interplay between the switching performance and parasitic inductances is analyzed. A fast-switching high-voltage power MOSFET is integrated in a power module with variable and distinct controllable parasitic inductances. By the help of a full-factorial approach, the interdependency between module-internal inductances and external ones like the gate inductance is described. It is shown that beyond critical values of the parasitic inductances, the switching losses of the power MOSFET are raised significantly and the switching performance of the devices is altered tremendously. As a result, the mechanisms leading to such critical values for the parasitic inductances are identified. These lead to general restrictions for the utilization of fast-switching devices in the application.

1. Trends and basic requirements for power modules

In power electronics, the reduction of overall system costs is an ongoing trend which will more and more dominate the development of upcoming products [1]. With focus on power modules, there are two common approaches which are currently considered. On the one hand, the reduction of the system costs can be realized by increasing the system’s power density. This requires more sophisticated power-module concepts together with an improved thermal management [2], [3]. On the other hand, raising the operating frequency of the system, i.e. especially by the utilization of fast-switching power semiconductors, will lead to benefits with focus on reduced inductor size and filtering effort to avoid electromagnetic interference. Here, the main challenge is the control of the fast-switching power semiconductors which requires an understanding of individual effects to obtain optimal performance of the devices [4].

2. Impact of parasitics on the switching performance

For both approaches, parasitics in the system and the power module influence the performance in several ways and need to be considered [5]. Parasitics, e.g. stray inductance, induce an enhanced overvoltage peak during the turn-off or can lead to an unintended parasitic turn-on during the switching event and, hence, influence the switching performance significantly. In addition, parasitics also limit the maximum achievable switching speed, e.g. by adding an inhibiting momentum to the gate circuit. In contrast to this, it is common understanding that the switching losses can be reduced by adding inductance to the gate circuit due to the current-source characteristic of the inductance. The questions are now, whether this understanding is still applicable for fast-switching devices and how the switching performance of such a fast-switching device interacts with parasitics and other external parameters?
2.1. Switching characteristics within an ideal setup

For an ideal setup, the switching characteristics are purely defined by the parameters of the switch itself and are not influenced by parasitics. Therefore, switching losses are directly related to the device current, e.g. the drain current $I_D$, and the device voltage, e.g. the drain-source voltage $V_{DS}$. Hence, the losses are given by $E = \int I_D(t) \cdot V_{DS}(t) \, dt$. The transient behavior of $I_D$ and $V_{DS}$ is correlated to the device characteristics. These depend mainly on design parameters like the cell structure, the doping profiles, or the used semiconductor materials. On the one hand, these design parameters can enhance the switching speed; by increasing the channel width, the steepness of the transfer characteristics is raised. On the other hand, design parameters like the cell structure influence the device-internal capacitive coupling, e.g. the gate-source capacitance $C_{GS}$ and the drain-gate capacitance $C_{DG}$, and control the switching speed within the used setup.

![Schematic drawing of an ideal setup](image1)

![Schematic drawing of a setup with parasitic inductances](image2)

Fig. 1. (a) Schematic drawing of an ideal setup, i.e. without any stray inductances. (b) Schematic drawing of a setup with parasitic inductances.

Fig. 1(a) shows the ideal setup of a power-semiconductor MOSFET without any stray inductances, with a free-wheeling diode in parallel to the inductive load. The gate voltage $V_G$ is applied to the gate terminal via the gate resistor $R_G$. Within this ideal setup, the gate-source voltage $V_{GS}$ of the MOSFET is given by:

$$V_{GS} = V_G + R_G C_{DG} \frac{dV_{DS}}{dt} - \frac{dV_{GS}}{dt} - R_G C_{GS} \frac{dV_{GS}}{dt} \quad (1)$$

During the switching event, i.e. the turn-on or turn-off, $V_{GS}$ is not only determined by $V_G$ and the corresponding voltage drop across $R_G$ but also by the feedback of $V_{DS}$ on the gate. This feedback is opposite to the transient of $V_G$ and its impact increases for large $R_G$ and $C_{DG}$. Hence, even in an ideal setup, the switching characteristics are influenced not only by the design parameters of the device but also by external parameters like the gate circuit which can increase the switching losses significantly.

2.2. Impact of parasitics on the switching characteristics

In reality, parasitics will exist in the setup and influence the switching characteristics. Fig. 1(b) shows a setup together with typical parasitics. $L_G$ is the inductance in the gate circuit and includes the inductance of the gate driver and the inductance of the gate circuit inside the power module. $L_S$ is the inductance in the source circuit. Both inductances, $L_G$ and $L_S$, will induce a voltage drop which is directly related to the changes in the corresponding currents $dI_G/dt$ and $dI_D/dt$, respectively, with the gate current $I_G$. In addition to this, $L_{couple}$ is the inductance which is integrated in both, the gate circuit and the source circuit. Hence, the voltage drop across $L_{couple}$ is determined by the sum of $dI_G/dt$ and $dI_D/dt$ and is seen in both circuits: While the gate current $I_G$ has a minor effect on $V_{DS}$, $I_D$ has a significant effect on $V_{GS}$. Thus gate and load circuit are coupled.
In addition to the feedback of $V_{DS}$ on $V_{GS}$, which has been shown in Eq. 1, the parasitic inductances $L_G$, $L_S$, and $L_{couple}$ will affect $V_{GS}$ in the following ways:

- Ultimately, $L_G$ will lead to a delay of reaching full $V_{GS}$ and reduce the maximum achievable switching frequency at the gate terminal. With focus on the turn-on, a larger $L_G$ will lead to an overshoot of $V_{GS}$ due to the dissipation of the energy stored in $L_G$ at the beginning of the Miller phase. This will reduce the length of the Miller plateau. Hence, for this case, the switching is accelerated and the switching losses are lowered.

- $L_S$ will lead to an additional voltage drop and reduce $V_{DS}$ during the turn-on. For the turn-off, large $L_S$ will lead to an increased overvoltage at the device. In both cases, $L_S$ will affect the feedback of $V_{DS}$ on $V_{GS}$.

- $L_{couple}$ serves as an additional voltage source in the gate circuit, which is in opposite to the transient of $V_G$. During the turn-on, the $dI_D/dt$ induces a voltage drop across $L_{couple}$ which effectively reduces $V_{GS}$. For the turn-off, the opposite will take place due to the negative $dI_C/dt$.

Accordingly, the parasitic inductances influence the switching characteristics. Depending on the relative size of the current slope and the inductances, this results in significant changes of the switching losses. Fig. 2 displays simulation results of a fast-switching 650-V IGBT for different values of $L_G$, $L_S$, and $L_{couple}$.

![Simulation results](image)

Fig. 2. Simulation results to compare the effects of $L_G$ (left-hand side), $L_S$ (center), and $L_{couple}$ (right-hand side). A fast-switching IGBT was used with the collector-emitter voltage $V_{CE}$, the collector current $I_C$, and the gate-emitter voltage $V_{GE}$.

The results illustrate qualitatively the impact of the parasitics on the switching event. From the simulation, the following relative impact on the turn-on losses $E_{ON}$ is extracted:

<table>
<thead>
<tr>
<th>Condition</th>
<th>$L_G = L_{G,0}$</th>
<th>$L_S = L_{S,0}$</th>
<th>$L_{couple} = L_{couple,0}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Condition 1</td>
<td>$L_G = 3L_{G,0}$</td>
<td>$L_S = 5L_{S,0}$</td>
<td>$L_{couple} = 4L_{couple,0}$</td>
</tr>
<tr>
<td>$E_{ON \ Cond2}/E_{ON \ Cond1}$</td>
<td>0.97</td>
<td>0.95</td>
<td>3.5</td>
</tr>
</tbody>
</table>

Table 1: Relative impact on the turn-on losses of $L_G$, $L_S$, and $L_{couple}$.

Based on the simulation, the extracted values in Table 1 confirm that an increase of $L_G$ will lower $E_{ON}$ slightly, whereas a larger $L_{couple}$ leads to a massive increase of $E_{ON}$. The impact of $L_S$ is purely related to a reduction of $V_{DS}$ and, hence, does not influence the switching speed. Therefore, the question arises whether the impact of the parasitics superimpose and partially...
compensate each other, e.g. when large $L_G$ and $L_{\text{couple}}$ are combined, and which inductances dominate?

3. Experiments

3.1. Test setup

A fast-switching high-voltage power MOSFET with a nominal-blocking voltage of 650 V, an on-state resistance $R_{\text{DSon}}$ of 37 mΩ, and a typical gate-threshold voltage $V_{\text{GS(th)}}$ of 3 V was implemented in the test setup (see Fig. 1(b)). In the free-wheeling path, a SiC diode without reverse recovery charge $Q_{rr}$ was used in parallel to the load inductance. The test setup allows measuring $I_D$ by an integrated current probe. As a result of this, a stray inductance of 25 nH for the setup is provided. $V_{\text{DC}}$ was set to 450 V, which is a typical operating voltage in the application, and $I_D$ was varied from 3 to 60 A. A gate driver with a low internal inductance $L_{\text{Driver}} = 20$ nH was used and $V_G$ was in the range from -5 to 10 V. The measurements were performed at a virtual-junction temperature of 25 °C.

Within the test setup, the parasitic inductances can be varied systematically. Due to the inherent limitations in the design of a power module, a fully independent variation of $L_G$, $L_S$, and $L_{\text{couple}}$ cannot be realized. To evaluate the relative impact of $L_G$, $L_S$, and $L_{\text{couple}}$, a screening experiment was done using a full-factorial approach. For this approach, the following four parameters were investigated: $L_{\sigma g} = L_G - L_{\text{Driver}} + L_{\text{couple}}$, $L_{\sigma s} = L_S + L_{\text{couple}}$, $I_D$, and $R_G$. While $I_D$ and $R_G$ are continuous, the inductance values are discrete and given by the setup.

By performing double-pulse measurements, the switching characteristics were determined and characteristic parameters like the turn-on losses $E_{\text{ON}}$, the maximum-drain current during turn-on $I_{\text{Peak}}$, and the turn-off losses $E_{\text{OFF}}$ were extracted.

![Fig. 3. $E_{\text{ON}}$ and $E_{\text{OFF}}$ versus $I_D$ for low $L_{\text{total}}$, i.e. $L_{\sigma g} = 26$ nH and $L_{\sigma s} = 17$ nH, and for high $L_{\text{total}}$, i.e. $L_{\sigma g} = 54$ nH and $L_{\sigma s} = 31$ nH. (a) The switching losses are displayed for $R_G = 5.1 \, \Omega$. (b) The switching losses are displayed for $R_G = 51 \, \Omega$.](image_url)

In Fig. 3, $E_{\text{ON}}$ and $E_{\text{OFF}}$ are shown for $R_G = 5.1 \, \Omega$ and $R_G = 51 \, \Omega$. For both gate resistances, the switching losses were determined versus $I_D$ for large and low values of both, $L_{\sigma g}$ and $L_{\sigma s}$. Independent of $R_G$ and the parasitic inductances, larger $I_D$ leads to an increase of $E_{\text{ON}}$ and $E_{\text{OFF}}$. For small $R_G$ and high values of $L_{\sigma g}$ and $L_{\sigma s}$, a superlinear increase of $E_{\text{ON}}$ and $E_{\text{OFF}}$ is observed. For the turn-on, this leads to an increase of $E_{\text{ON}}$ by a factor of five. Such a significant increase is not seen for large $R_G$. Here, the impact of $L_{\sigma g}$ and $L_{\sigma s}$ is less dominant and leading to an increase by only 25%. Based on these findings, the analysis of the impact of parasitic inductances on the switching characteristics is focused on $E_{\text{ON}}$ and small $R_G$. At the very end, an explanation will be given why it is not surprising that $E_{\text{OFF}}$ is not changing so dramatically.
3.2. Experimental results and interpretation

From the previous figure, the effect of stray inductance is seen to be negligible for small $I_D$ and $R_G$, while an important effect is seen at $R_G = 5.1 \, \Omega$ and $I_D = 60 \, A$. Fig. 4 illustrates the impact of $L_{ag}$ and $L_{as}$ on switching losses under these conditions:

If either of the parameters is small, the losses are small as well. The combination of high stray inductance for both the gate and load circuit, however, leads to a tremendous increase of the losses by up to a factor of five as discussed at Fig. 3 already. This increase has been seen in the simulations as well (see Table 1). Interestingly, it is not a continuous increase of the switching losses, but rather a transition from almost constant losses for small inductance towards a high-loss regime at elevated inductances. This is an indication for a change in switching behavior from a low-loss to a high-loss regime. In the following, experimental results are used to separate the two regimes. An explanation on the basis of switching curves will be given afterwards.

![Graph](image)

Fig. 4. (a) $E_{ON}$ versus $L_{os}$ and $L_{sg}$ for $I_D = 60 \, A$. (b) $E_{ON}$ versus $L_{ag}$ for different values of $L_{os}$. (c) $E_{ON}$ versus $L_{os}$ for different values of $L_{ag}$.

At small $L_{os}$, an increase in gate inductance leads to a well-known reduction of switching losses (indicated by the dashed line in Fig. 4 (b)). The inductance is supporting a current-source behavior for the driver. This effect, however, is small in comparison to the high-loss regime. Upon increased $L_{os}$, this behavior changes for medium values of $L_{ag}$ and $E_{ON}$ increases. The rather abrupt change happens instantly once both values exceed a certain value. This increase of the switching losses is directly linked to a reduced current peak for $L_{ag} > 50 \, nH$, which will be shown in detail later in Fig. 6.

From the design of the test-setup, $L_{couple}$ is estimated. This allows analyzing directly the impact of $L_{couple}$ on $E_{ON}$. The upper row of Fig. 5 covers the standard parameters $R_G$ and $I_D$ at low (left-hand side), medium (center), and high (right-hand side) $L_{couple}$. In the first two cases, the general behavior is a linear increase of losses along the two axes. The interaction of $R_G$ and $I_D$ leads to raised losses especially for high values of $R_G$ and $I_D$. This is common knowledge, as the switching losses should increase with both, switched current $I_D$ and $R_G$, especially as the latter is dominating the slope $dI_D/dt$. However, in the third graph a different behavior is recognized. At large currents, the switching losses are very high even for low values of $R_G$, and saturate towards large gate resistance. The starting point of this behavior may already be recognized at the middle graph.
Fig. 5. The upper row shows $E_{\text{ON}}$ versus $I_D$ and $R_G$ for $L_{\text{couple}} = 0$ (left-hand side) to $L_{\text{couple}} = \text{max}$ (right-hand side). The transition to high losses is easily recognized in the picture on the right-hand side. The lower row shows the evolution of $E_{\text{ON}}$ vs $L_{\text{couple}}$ and $I_D$ for $R_G = 5.1 \, \Omega$ (left-hand side) and of $E_{\text{ON}}$ versus $R_G$ and $L_{\text{couple}}$ for $I_D = 30 \, \text{A}$ (right-hand side).

The transition is exposed in the lower row of Fig. 5, where $L_{\text{couple}}$ is used as a parameter. While at low current and gate resistance values, there is no effect of $L_{\text{couple}}$, it becomes a decisive factor beyond a value of $L_{\text{couple}} \sim 7\, \text{nH}$ and $I_D > 30 \, \text{A}$ or $R_G > 5.1 \, \Omega$. The two pictures in the lower row of Fig. 5 indicate that the modification of $V_{\text{GS}}$ through direct ($R_G$) and indirect ($I_D$ through an induced voltage drop $L_{\text{couple}} \cdot \text{d}I_D/\text{d}t$) contributions is a decisive factor. Especially, at large $L_{\text{couple}}$, $V_{\text{GS}}$ is affected strongly and, hence, the switching performance is modified. Therefore, $V_{\text{GS}}$ is eventually falling below $V_{\text{GS(th)}}$ which ultimately changes the switching performance.

Fig. 6. (a) The appearance of the high-loss regime as a function of drain current for $R_G = 5.1 \, \Omega$. (b) Different representation of the same measurements including the peak current. Here, the separation is also recognized.

In Fig. 6, the two regimes of operation are visualized by showing $E_{\text{ON}}$ versus $I_D$ and the correlation between $I_{\text{peak}}$ and $E_{\text{ON}}$. Fig. 6(a) shows again the losses as a function of $I_D$. As mentioned before, the high-loss regime starts at $30 \, \text{A}$ for high $L_{\text{og}}$ and $L_{\text{os}}$. Fig. 6(b) displays
$E_{\text{ON}}$ correlated to $I_{\text{peak}}$. As soon as the switching behavior changes and the MOSFET is operated in the high-loss regime, $I_{\text{peak}}$ is reduced significantly and the switching losses increase (dashed line). In contrast to this, the typical switching behavior results in large values of $I_{\text{peak}}$ and low switching losses (dotted line).

From these results it is clear that stray inductance is a significant parameter, depending on the settings of the other parameters. At $V_{\text{DC}} = 150$ V, no such behavior has been seen. The switching losses follow completely one, namely the low-loss regime. Results at 150 °C show no general difference to the results obtained at 25 °C except an expected weak overall increase of switching losses.

Fig. 7(a) shows the switching characteristics of the MOSFET for low $L_{\text{couple}}$ and for $L_G$ from 26 to 58 nH. Due to the increase of $L_G$, a lowering of $E_{\text{ON}}$ from 0.40 to 0.39 mJ and an increase of $I_{\text{peak}}$ from 113 to 116 A is observed. Both findings correlate with the effect of a large $L_G$ on the turn-on. In Fig. 7(b), the switching characteristics are shown for high $L_G$ and for $L_{\text{couple}}$ from 3.5 to 14 nH. With increasing $L_{\text{couple}}$, the oscillations on $V_{\text{DS}}$ and $I_D$ become damped which, in turn, is directly related to a slowing down of the switching speed. With increasing $L_{\text{couple}}$, $E_{\text{ON}}$ is raised from 0.39 to 1.76 mJ. For $I_D$, the recovery-current peak is reduced significantly from 116 to 70 A with increasing $L_{\text{couple}}$ (displayed in the inset). Especially for large $L_{\text{couple}}$, a peak on $V_{\text{DS}}$ is observed directly after the turn-on of the device.

![Fig. 7(a) Measurement of the turn-on with increasing $L_G$ for fixed $L_{\text{couple}}$ at $I_D = 60$ A and $V_{\text{DC}} = 450$ V. Additional offsets of 150 V and 60 A were added to $V_{\text{DS}}$ and $I_D$, respectively.](image)

![Fig. 7(b) Measurement of the turn-on with increasing $L_{\text{couple}}$ for fixed large $L_G$ at $I_D = 60$ A and $V_{\text{DC}} = 450$ V. Also here, additional offsets of 150 V and 60 A were added to $V_{\text{DS}}$ and $I_D$, respectively.](image)

For large $L_{\text{couple}}$, $V_{\text{GS}}$ is reduced due to the voltage drop across $L_{\text{couple}}$ arising from the d$I_D$/dt and the switching is slowed down. This leads to an increase of the reference potential for $V_{\text{GS}}$. At the same time, $V_{\text{DS}}$ has a feedback to $V_{\text{GS}}$ through $C_{DG}$ and affects directly $V_{\text{GS}}$. In the experimental results, this interplay is indicated by the peak (highlighted by orange circles in Fig. 7(b)) on $V_{\text{DS}}$ which comes along with an abrupt turn-off of the device which is not entirely related to $L_{\text{couple}}$. Due to the large $L_G$, the impact of the feedback is not counterbalanced by $V_G$ and $V_{\text{GS}}$ is pulled below $V_{\text{GS(th)}}$. The device is partially turned off, $V_{\text{DS}}$ increases and, in turn, $I_{\text{peak}}$ is reduced.

For $E_{\text{off}}$, no such extreme changes in the switching losses are observed for varying $L_{\text{couple}}$. Due to the operating conditions, the MOSFET provides a d$I_D$/dt for the turn-on which is up to a factor of three larger than the d$I_D$/dt during the turn-off. The induced voltage is hence smaller, while, at the same time, the gap between $V_G$ (-5 V during turn-off) and $V_{\text{GS(th)}}$ is larger than during turn-on ($V_G = 10$ V). Such a scenario where $V_{\text{GS}}$ is raised above $V_{\text{GS(th)}}$ again during the turn-off is not observed in the switching curves. This can be attributed to the off-centered position of $V_{\text{GS(th)}}$ in the range of $V_G$ used for the experiment. If the range is modified, e.g. by using $V_G$ from 0 to 10 V, the impact is expected to be different.

However, due to the smaller d$I_D$/dt during the turn-off, the interplay between the switching losses and the parasitic inductances will be more dominant for the turn-on than for the turn-
off. Especially for fast switching, i.e. small $R_G$, the impact of $L_{og}$ and $L_{os}$ leads to a factor of five larger turn-on losses.

4. Conclusion

This paper emphasizes the effects of parasitic stray inductances in the gate and drain circuit on the switching performance of fast-switching devices. Using an experimental setup with a fast-switching high-voltage power MOSFET and tunable $L_{os}$ and $L_{og}$, switching losses have been determined in a broad range of operating conditions. The experimental results show a clear transition from a low-loss regime towards a high-loss regime. The coupling inductance $L_{couple}$ is found to play a decisive role which is explained as follows: Depending on $R_G$ and $I_D$, the voltage drop across $L_{couple}$ due to the $dI_D/dt$ in combination with the coupling for $V_{DS}$ through $C_{DG}$ reduces $V_{GS}$ below the threshold voltage $V_{GS(th)}$ and leads to a partial switching off during the turn-on. In this scenario, the resulting switching losses are larger by about a factor of five in comparison to small inductance values. On the other hand, when $L_{couple}$ is small, changes in the other inductances do not alter the switching curves nor losses significantly.

The understanding of these mechanisms is valuable in the design of power modules and for the integration of discrete products using fast-switching devices. Although the avoidance of stray inductances improves the switching performance, in some cases, e.g. when operating several switches in parallel or for controlling short-circuit operation, the specific implementation of small $L_{couple}$ is advantageous. Therefore, the general rule that stray inductances should be reduced to a minimum is not altered. Especially for discrete products, the reduction of the stray inductances must be accomplished by using an appropriate low-inductive layout on the PCB. If not possible, however, the focus should be on reducing $L_{couple}$, or one of the two $L_{og}$ and $L_{os}$ in order to avoid entering the high-loss regime.

In the application, it is important to understand that a change of the gate resistance, e.g. with the purpose to reduce the switching speed, may result in a huge increase in switching losses due to the existing $L_{couple}$. Both, large $L_{og}$ and $R_G$, lead in combination with a large $L_{couple}$ to an increased feedback of $V_{DS}$ on $V_{GS}$ which can force the transition towards the high-loss regime. The user needs to be aware of this possible scenario and consider alternative countermeasures to limit the switching speed. If switching losses are of minor importance and a limitation of overcurrents is the predominant issue, this may be realized by choosing a large common inductance for the gate circuit.

5. References


