Comparison between active and passive thermal cycling stress with respect to substrate solder reliability in IGBT modules with Cu baseplates

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Abstract:

The reliability of the solder joint between substrate and base plate of an IGBT module can be tested using passive thermal cycling (TC) or active power cycling (PC). Naturally the active power cycling is more relevant for most applications. On the other side, the passive test serves better to separate the substrate solder aging from other fatigue mechanisms observed in power cycling. This paper focuses on a common understanding of the most relevant stress parameters that dominate the solder aging in both types of tests. This is done by end of life investigations and thermal modeling supported by measurements.

1. Introduction:

During their life time IGBT modules see much thermal stress, mostly caused by internal heating of the dies but also by external thermal cycles, like day night cycles or varying temperature levels of the cooling system during operation. To ensure the module reliability especially with respect to the large area solder joints between substrate and baseplate two different test methods are used at Infineon. The first method is active power cycling. As second method there is thermal cycling (TC) by means of externally heating and cooling the device.

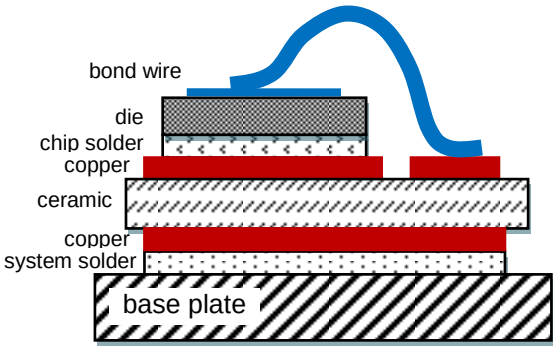

Figure 1: Schematic cross section of an IGBT module

There are many different ways in performing a power cycling test [1]. Due to the higher application relevance we prefer the method that applies constant cycle times (t_{on} / t_{off}) and constant load current during the test. Power loss increases only as a result of a rising forward voltage or device temperature.

Furthermore one should differentiate between two regimes of power cycling test conditions. The first one is realized by the so called PC(sec), which uses cycle times typically smaller than 15s. These short cycles mainly stress the die connections, i.e. the bond wires or the interconnection between die and substrate. The other one is the PC(min) test with longer cycle times (2-10 min) and smaller currents compared to PC(sec). The latter primarily affects solder layers beneath the die including the solder between substrate and baseplate. Using a Zth monitoring during the test [2] or by doing intermediate scanning acoustic microscopy (SAM) measurements, the delamination of the solder layer and its propagation during PC(min) can be investigated. The temperatures (T_j, T_c) and their corresponding temperature ripple (ΔT_j, ΔT_c) can be adjusted by decreasing or increasing cycle time or current during the test startup phase. To accelerate the PC test the resulting temperature swing is usually higher than in the application. Nevertheless the same failure modes shall be triggered as occurring in the application. Typically the ΔT_j value in the laboratory tests ranges from 50 K up to 110 K which is high enough to trigger either bond wire or chip solder fatigue under laboratory conditions. If acceleration of the substrate solder fatigue shall be achieved to impose it as the dominant failure mechanism. While the test duration shall be kept within

feasible limits on a scale of some months the ΔT_c must be raised to 60…80K. Due to the thermal impedance given by the thermal network of an IGBT module with baseplate this implies the application of long cycle times. Thus the PC(min) is the method in focus of this work.

As mentioned before there is another possible method to stress the substrate solder layer of an IGBT module. This passive thermal cycling (TC) test is performed by mounting the module on a combination of electrical heater and water cooling block. Usually the modules are tested from T_{min} = 25 °C to T_{max} = 105 °C. The cycle time in this test depends on the thermal capacity of the test module and ranges from 4-6 min.

To compare these two test methods concerning substrate solder degradation the trigger of the aging mode needs to be known. The delamination of the substrate solder usually starts in the corners of the substrate solder and grows linear to the substrate center. The speed of the crack growth depends on the applied temperature swing in the substrate corner. [3]

The main difference between the test methods PC(min) and TC is the different temperature swing at the substrate corners. In the passive TC test this swing is easy to obtain because the module is heated from the outside so every part in the module reaches the same temperature level ΔT_c = 80 K. The determination of the substrate corner temperature in a PC test is more complicated. The following chapter introduces the used methods to determine the temperature at the substrate corners.

2. Measurement methods with local temperature resolution

Two different measurement methods are employed to determine temperatures at different locations in the module.

a. Below each corner of a substrate and below one chip the temperature is monitored using thermocouples inside the baseplate. To enable this measurement for each package within the scope of this investigation a test module is prepared by drilling five holes into its base plate. In each of these holes a thermocouple is placed (Figure 2)

b. In addition the temperature at the same positions in the xy-plane is measured on the upper surface using an infrared camera. For this purpose the modules are mounted without silicone gel and the surfaces are painted black to provide a proper infrared emission.

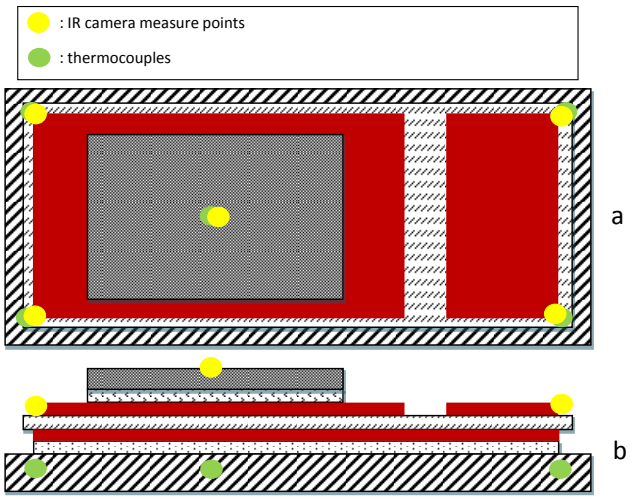

Figure 2: Used measurement points, in a schematic module top view (a) and cross section (b), same layer colors as in Figure 1

To estimate the actual temperature in the solder joint and determine the influence of the drilled holes on the heat flow FEM simulations are performed. In order to achieve a proper agreement between measured and simulated temperatures only the heat sink boundary conditions need to be adjusted in the FEM model. As a result the temperature swing in the solder joint ranges typically between the temperature on top and the temperature under the substrate corner. Another outcome is that the influence of the drilled holes on the temperature profiles is negligible.

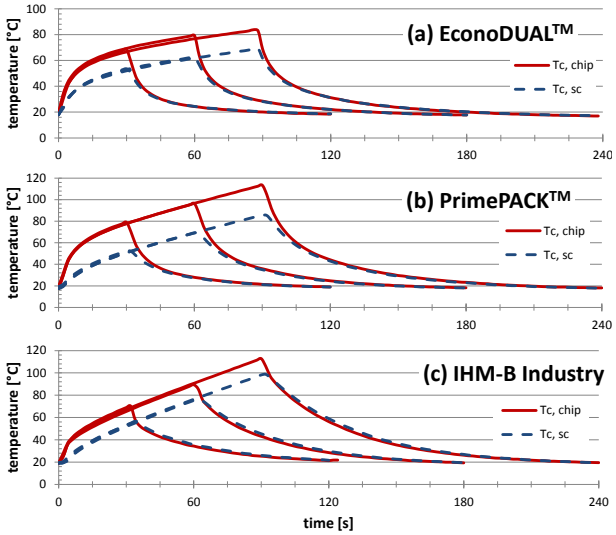

Figure 3: Thermocouple measurements for different packages, I = 2/3*I_{nom} , water cooling is turned off during heating

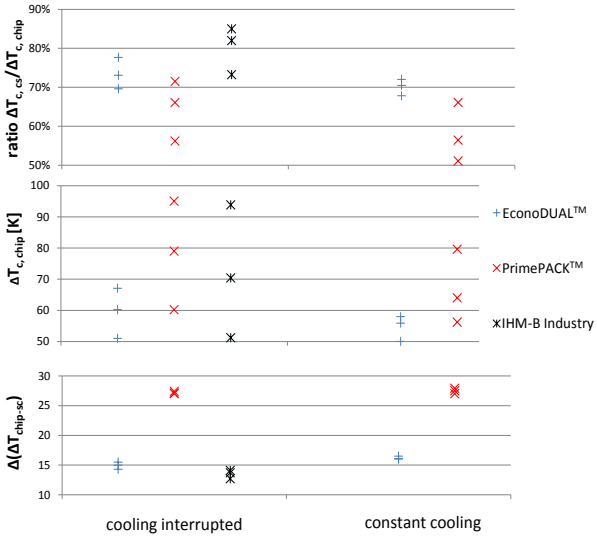

Figure 4: $T_{c,chip,max}$ and $\Delta(\Delta T_{c\text{-}sc})$, for different cooling conditions, I = 2/3*I_{nom} , t_{on} 30s, 60s and 90s

3. Transient temperature profiles for different IGBT modules

Figures 3a,b,c show the results of the thermal measurements which are performed on a water cooled heat sink with three different module types. Every measured package consists of a similar material stack. The specific differences between the module types are the DCB layout and the base plate thickness with d_{BP}=5mm for IHM-B and d_{BP}=3mm for PrimePACK™ and EconoDUAL™. All three module types are mounted on the same heat sink.

The measurements are done at about 2/3 of the modules nominal currents. The heating phase starts with every package at 20 °C and stops after 30, 60 and 90 seconds. The water flow through the heat sink is interrupted intentionally only during the heating phase to generate a higher temperature level especially at the base plate. The cooling time varies in the range from 90-150s to reach the regime of the actual starting temperature.

The following entities are used for the further discussion.

$T_{c,chip}$, $\Delta T_{c,chip}$: case temperature and swing underneath an active die

$T_{c,sc}$, $\Delta T_{c,sc}$: case temperature and swing underneath substrate corner for those substrate corners that are located closest to the heat generating dies.

For all packages a significantly lower temperature and temperature swing is seen at the substrate corner compared to the measurement position under the chip. This difference is defined as

$\Delta(\Delta T_{chip\text{-}sc}) = \Delta T_{c,chip} - \Delta T_{c,sc}$.

Since $\Delta T_{c,sc}$ underneath the substrate corner is regarded as the relevant stress parameter for substrate solder fatigue the question is raised how much $\Delta T_{c,sc}$ lags behind $\Delta T_{c,chip}$ if the test conditions are altered. This is analyzed in figure 4 which shows the maximal temperature ripple $\Delta T_{c,chip}$ underneath the chips and their corresponding $\Delta(\Delta T_{chip\text{-}sc})$, for the heating time interval t_{on}=30…90s. Unlike figure 3 both versions for applying water cooling (turned off during heating and constant water flow) are compared against each other. For each package with 3mm baseplate the $\Delta(\Delta T_{chip\text{-}sc})$ is fairly independent on the mentioned variation of the test conditions and stabilized at $\Delta(\Delta T_{chip\text{-}sc})$~15K for EconoDUAL™ and ~28K for PrimePACK™. This can be reasoned by assuming that the thermal capacities of the packages are saturated within 30s including the

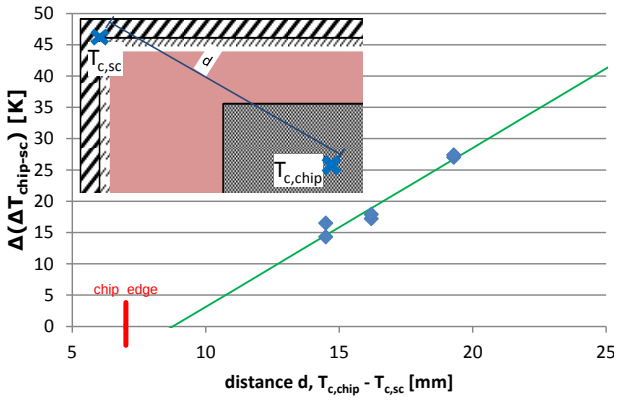

Figure 5: $\Delta(\Delta T_{chip\text{-}sc})$ versus the distance between the measurement point of $T_{c,\,chip}$ and $T_{c,sc}$, for 3mm baseplate modules, heating by $I=2/3I_{nom}$

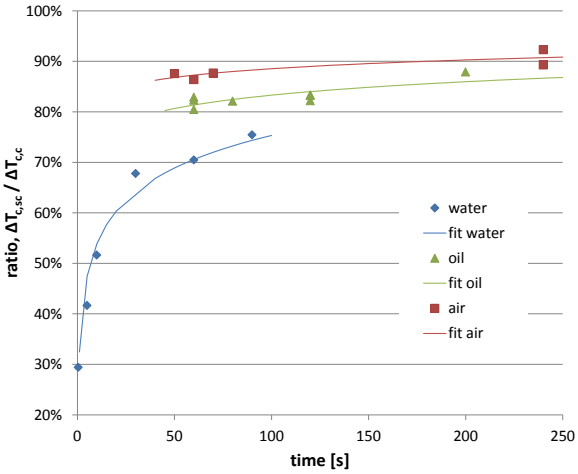

Figure 6: ratio of $\Delta T_{c,sc}$ and $\Delta T_{c,\,chip,}$ for different cooling strategies plotted against the turn on time (t_{on}) for EconoDUAL^{TM}

positions at the corner of the substrates. As expected the measurements with cooling turned off during heating show higher temperatures $T_{c,chip}$ than the measurements using permanent activated cooling. The $\Delta(\Delta T_{chip\text{-}sc})$ values is in the same range for both cooling conditions.

The PrimePACK^{TM} module shows a higher temperature difference between $T_{c,chip}$ and $T_{c,sc}$ than the other measured packages. Practically this means that the substrate corners undergo lower thermo mechanical stress under PC(min) cycling conditions if compared to the other packages. This can be explained by the larger distance between an active die and the substrate corner. Figure 5 shows $\Delta(\Delta T_{chip\text{-}sc})$ plotted versus the actual distance between these two measurement points. The red line labeled chip edge in this figure symbolizes the minimum possible distance that is given when the chip corner is located directly above the substrate corner. A linear correlation between $\Delta(\Delta T_{chip\text{-}sc})$ and the distance can be assumed from this data. The gap on the x-axis between the red line and the fitted green line could be explained by the heat spreading between die and baseplate. All points seen in Figure 5 are measured in module packages using the same layers and same baseplate thicknesses only the DCB layout differs in the measurements. Because of the thicker baseplate the IHM-Cu module slightly differs from the other measurements and is not plotted in this figure.

4. Influence of different cooling technique

In applications several different cooling techniques can be found. Mostly water cooled and air cooled heat sinks are used depending on the application specific power density and mission profile. In order to understand the impact of cooling technique on the substrate solder stress again the temperature conditions underneath the substrate corner have to be analyzed in comparison to the conditions underneath those chips that dominate the power dissipation. Usually the case temperature conditions underneath the chips $T_{c,chip}$ are used for the thermal design of the inverters because they can be calculated by means of the thermal network given in datasheets.

Figure 6 plots a ratio between the measured $\Delta T_{c,sc}$ and $\Delta T_{c,chip}$ values against the heating time t_{on}. All measurements were done with permanently activated cooling as relevant for real applications on different test benches that utilize different cooling techniques using the same EconoDUAL^{TM} power module. It can be assumed that the cooling power reduces as we go from water to oil towards air as cooling medium due to the decreasing thermal capacity of the cooling medium. It should be emphasized that the width of the air cooled heatsink was hardly

exceeding the width of the power module thus representing rather the worst case geometry in terms of cooling power. The fit curves through the measured points for each cooling technique indicate different ratios $\Delta T_{c,sc}/\Delta T_{c,chip}$ dependent on the cooling medium. In the regime of cycles times which is relevant for PC(min) practically the stress on the solder layer increases using air cooled compared to water cooled devices due to the stronger extent of heat spreading of an air cooled heat sink. For example at t_{on}=60s only ~70% of $\Delta T_{c,chip}$ reaches the substrate corner for water cooling in comparison to ~85% for the air cooled system. For oil as a cooling medium the ratio lies somewhere between the water and air heat sinks.

These observations raise the question of how to design accelerated PC(min) tests properly. The worst case in terms of ΔT-stress on the substrate solder edge is expected for heatsinks with rather small cooling power like air cooled systems. The disadvantage for a laboratory test with air cooling is the long cycle time needed because after each temperature cycle the system has to be cooled long enough to reach its starting point again. We propose a method where liquid water cooling is applied but water flow is switched off during the heating phase of each cycle as explained in chapter 3. As already shown in figure 4 the ratio $\Delta T_{c,sc}/\Delta T_{c,chip}$ can be increased by roughly 5% for t_{on}=90s if cooling flow is switched off during the heating phase. This does not suffice to reach the conditions of air cooled operation. Therefore in qualification tests also the heating time has to be further increased into the regime 3…5min. A simulation using the model which is introduced in the next chapter results in a ratio $\Delta T_{c,sc}/\Delta T_{c,chip}$ of ~82% if the heating phase is extended to 200s. Higher values are difficult to achieve in an accelerated test using water cooled heat sinks. Therefore the passive TC test is also applied in power module qualifications where $\Delta T_{c,sc}=\Delta T_{c,chip}$ is achieved. This is further discussed in chapter 6.

In addition short cycle times using water cooling were tested. The blue line in figure 6 indicates a ratio between $\Delta T_{c,sc}$ and $\Delta T_{c,chip}$ smaller than 50% for t_{on}<10s. This leads to very small temperature swings at the substrate corners in PC(sec) test. This temperature swing is low enough to ensure that substrate solder fatigue starting at the corners does not limit the module's lifetime in PC(sec). This is valid for common soft solder die interconnects. For new future technologies the substrate solder might limit the PC(sec) lifetime[4].

For longer cycle times (t_{on}≥30s) several measurements with different current or power dissipation levels were performed using different cooling media. As expected a linear dependency between $\Delta(\Delta T_{chip\text{-}sc})$ and the dissipated power in the module was found. This is a natural matter of the fact that thermal systems behave as linear networks if conditions with different power levels are compared. The ratio between the $\Delta T_{c,sc}$ and $\Delta T_{c,chip}$ stays rather constant for varying test currents.

5. Extended Cauer model

An extended thermal Cauer model (Figure 7a) can be used to get a quick estimation of the temperature and temperature swing at the substrate corner for known cooling systems. The model consists of a standard Cauer model which can be split in an IGBT module part and a heat sink part. The RC values of the IGBT module part can be calculated using the given Foster model from the semiconductor datasheet by the method explained in [5]. Two RC elements representing the heat sink are obtained by fitting the simulated $T_{c,chip}(t)$-transient to the measurement data.

The extension of the model to obtain the temperature at the substrate corners is done by adding another branch. This branch is decoupled using an ideal operation amplifier (OpAmp) in P-Spice simulations. This ideal OpAmp is needed because the lower branch must not change the behavior of the upper one. As seen in Figure 7a the input for the second branch is the case temperature T_c from the upper branch. The first RC element represents the thermal conductivity and capacitance between the measured points ($T_{c,chip}$, $T_{c,sc}$) in the power

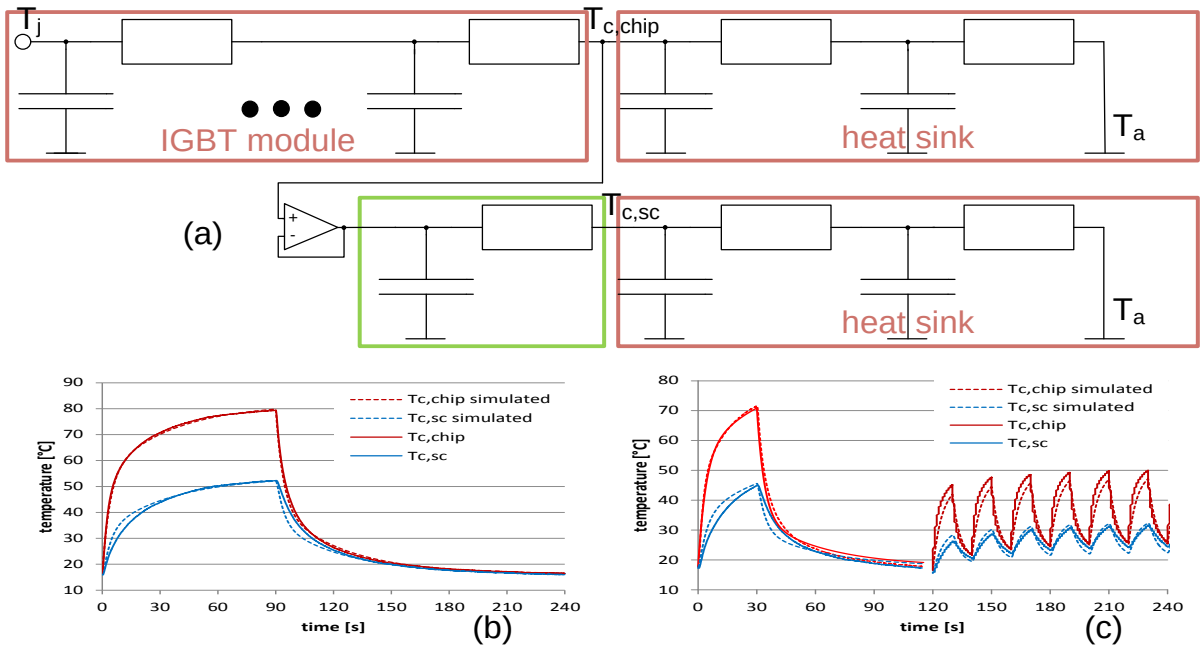

Figure 7: (a) schematic view of the extended Cauer model for temperature estimation at the substrate corner, (b) comparative plot of the measured and simulated values, (c) model used with different heating times (t_{on} = 30s, t_{on}=10s)

module baseplate. This RC element is again obtained by fitting the measurement data from the previous chapters to the simulated temperatures for the substrate corner. In series connection to this RC element the used heat sink part from the upper branch is employed again leading to the ambient temperature T_a. As presented in figure 7 (b) the model yields a satisfying agreement for the heating and cooling phase of one cycle. Figure 7 (c) reveals the comparison of the fitted RC element with other heating times and power densities. For the shorter t_{on}=30s cycle the model delivers satisfying results. The much shorter 10s cycles show a small deviation between the simulated and measured values for both $T_{c,sc}$ and $T_{c,chip}$. But as figure 4 indicates the strong decline in the ratio $\Delta T_{c,sc}/\Delta T_{c,chip}$ is clearly visible in this simulation if heating times below 10s are applied.

The main idea for this model is a rather quick estimation of the temperature transients under the substrate corners. This could be a faster way compared to building a complete FEM model, especially without exact knowledge of the internal module structure. Of course there needs to be at least one measurement of the transient temperatures for $T_{c,chip}$ and $T_{c,sc}$ for each cooling system under investigation. At the moment it seems that the distance between the measured points ($T_{c,chip}$, $T_{c,sc}$) is the main influence factor for the RC values right after the OpAmp. The dependency looks linear at least for comparable module structures. But this needs to be further evaluated using more measurements.

6. Substrate solder fatigue in PC(min) and TC

Figure 8 shows exemplary scanning acoustic microscopy (SAM) images of substrate solder joint after 10.000 passive thermal cycles and 10.000 active power cycles. Both test modules achieved a $\Delta T_{c,chip}$ of 80K and have not reached their end of life yet. The crack length has been measured from the corners in a 45° angle until the end of the delamination area. Here EconoDUAL^{TM} modules are evaluated after different number of cycles in TC and PC(min). In both test the $\Delta T_{c,chip}$ was adjusted to 80K.

In Figure 9 the measured crack lengths are plotted against the number of cycles. These raw values differ strongly depending on the performed type of cycling test.

As seen in the previous chapter the $\Delta T_{c,sc}$ differs between PC (min) and TC if the temperature change under the dies $\Delta T_{c,chip}$ is assumed as a common reference point for both test types. Assuming a Coffin Manson Law for the acceleration model the crack length for the PC(min) related data points can be normalized to $\Delta T_{c,sc}$=80K. The Coffin Manson acceleration law $N_{cyc} \sim \Delta T^{-4,5}$ is taken from the Infineon thermal cycling specification [6]. It is assumed that the growth speed of crack length dl_{crack}/dt behaves inversely to the reachable cycle number N_{cyc}, which results in a dependence $dl_{crack}/dt \sim \Delta T^{4,5}$. The same correlation obviously applies for the absolute value of crack length l_{crack}:$l_{crack}/dt \sim \Delta T^{4,5}$.

After normalizing the measured PC(min) crack length by this procedure and assuming a linear crack growth the PC(min) points lie in the same regime as the corresponding TC crack length (Figure 9 b).

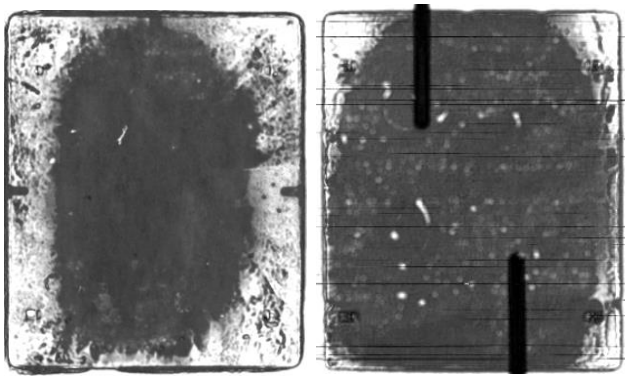

Figure 8: Exemplary SAM images after 10.000 cycles TC (left) and 10.000 cycles PC(min)(right) ΔT_c underneath active dies 80K

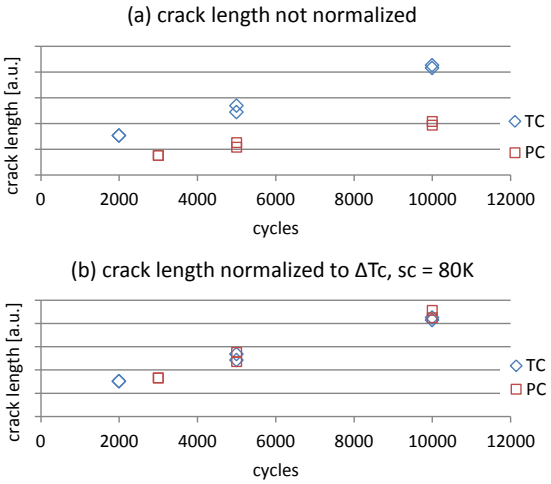

Figure 9: crack length evaluation, TC and PC(min) for EconoDUAL™

7. Summary / Outlook

It has been shown that passive thermal cycles induce a stronger solder delamination underneath the substrate edges of IGBT modules compared to thermal cycles triggered by internal active heating. The difference in delamination progression speed cannot be described by one simple correlation factor because it depends both on layout of the test devices and on cooling conditions. The amplitude of the temperature cycle underneath the substrate corner $\Delta T_{c,sc}$, where the delamination starts, is a very good universal parameter that dominates the rate of substrate solder delamination. This is exemplarily deduced in this work for an EconoDUAL™ IGBT module with a lead free substrate solder.

In the thermal design of power electronic systems like inverters usually the magnitudes of the occurring temperature cycles are calculated for locations underneath the IGBT and diode dies as main heat sources (e.g. $\Delta T_{c,chip}$ for case temperature underneath the chips). For a variety of constellations we have investigated how much the temperature ripple underneath the substrate corner is reduced in comparison to the position directly underneath the heating dies. Obviously the distance from die center to substrate corner plays an important role: by investigations of different productive IGBT module designs it is shown that there is a linear correlation between the relevant distance and the ΔT-reduction: The further away the dies are placed from the substrate edges the higher the active thermal cycling capability will be.
Furthermore the cooling power of the heat sink plays an important role. Low cooling power, as represented by air cooled systems, allows for higher heat spreading. In this case up to 90% of the temperature ripple underneath the dies reaches also the substrate edges in case

of the EconoDUAL™ package. For the same system a water cooled heat sink reduced the ratio significantly in the regime 70…80% if heating duration of 1…2min is applied.
Another important result is that for small heating times below 10s the temperature ripple at substrate corner is so low that substrate solder delamination is not expected to limit the performance.

Evaluations for other products such as high power traction modules using AlSiC baseplates and new solder technologies will be done in the future. The introduced extended Cauer model will also be further refined.

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