1ED Compact – A new high performance, cost efficient, high voltage gate driver IC family

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Abstract
This paper describes the new Infineon EiceDRIVER™ family 1EDI Compact and its benefits for achieving higher power density in a continuously demanding market for cost efficient solutions. This new general purpose high voltage gate driver IC family includes four output current variants optimized for IGBTs, one variant optimized for MOSFETs and three additional variants with an active miller clamp feature for IGBTs. The new optimized coreless transformer technology ensures undisturbed operation at offset voltages up to +/- 1200V and a common mode transient immunity (CMTI) of output to input of 100kV/µs. It later shows performance aspects of the different variants and their benefits on a PCB.

1 Introduction
It is generally known, that the market of power electronics is driven by shrinking footprints, form factors and higher power density all the time. This statement is also valid for isolated high voltage gate driver products and companies in the solar inverter market start to ask for optimized driver products to reduce complexity.

With the development of the new 1200V EiceDRIVER™ Compact family, Infineon is able to close this gap and provide a high performance but cost efficient and compact driver IC.

2 Features

2.1 Coreless Transformer
The optimized coreless transformer design requires less space on the chip. It enables higher output currents compared to previous designs and therefore higher power density within the same compact SO8 package. The robust design of this new coreless transformer also ensures a high CMTI at a dV/dt operation of up to 100kV/µs as tested in an application circuit with Infineon’s CoolMOS™ transistors. The principle of the measurement setup with a silicon carbide diode complementing the CoolMOS™ can be seen in Fig 1. It also shows a detailed oscilloscope diagram of a turn off transition reaching a dV/dt of 99.55kV/µs at a HV supply voltage of \( V_{\text{DC}} = 400 \text{V} \) and a load current of \( I_L = 13 \text{A} \). These rapid transitions have normally a huge impact on the isolated gate driver supply propagating even to the primary supply which are visible as ringing on the logic input signal without interrupting the drivers normal operation. It is easy to see that the ringing is minor according to Fig 1. Anyway, the noise filter of the Input pulse suppression will cancel any crosstalk or EMI up to a pulse duration of \( T_{\text{MININ+/-}} = 40 \text{ns} \) for MOSFET and \( T_{\text{MININ+/-}} = 240 \text{ns} \) for IGBT variants. At this evaluation there was no need for an additional input RC-Filter, however an external filter can further improve signal quality.
2.2 Output configuration

The 1EDI Compact family targets a broad application range. Different variants where needed to support their individual demand. The variants with separate output for sourcing and sinking support a voltage supply of up to \( V_{CC2} = 35 \) V as needed in applications with bipolar gate voltages. The customer can reference the supply voltage externally to the gate to achieve a user defined gate supply. The separate outputs according to Fig 2 also enable the customer to select individual gate resistors for tuning turn on and turn off behavior while saving the space for a bypass diode. This method simplifies the gate circuit layout and minimizes parasitics in the gate loop.

The second output configuration as seen on the right in Fig 2 hosts an active miller clamping feature for gate supply voltages up to \( V_{CC2} = 20 \) V. Typical applications use the clamp function to avoid parasitic turn on of the power switch due to displacement currents of output dV/dt. Bipolar supply concepts as with the above driver configuration can also compensate for this however it requires a more advanced power supply. To further reduce circuit complexity and PCB space in half-bridge configurations the unipolar supply for 1EDI Clamp variants is often implemented with a bootstrap circuit. The low quiescent current consumption of the output chip makes it possible to operate this driver with a high modulation index without the need to have a huge bootstrap capacitor. An additional benefit of the CLAMP variant is the integrated diode which clamps the pin CLAMP to \( V_{CC2} \). Since this pin is directly connected to the gate of the power switch there is no additional resistive path compared to the body diode of the general gate output and gate resistor path as in a usual configuration. It therefore saves the space for another external diode on the PCB. The CLAMP function itself has the same current capability as the output. The 1EDI30I12MF has here a minimum peak current of \( I_{OUT} = 3 \) A. The Clamp circuit becomes active at turn off when the voltage at the CLAMP pin drops below \( V_{GATE} = 2 \) V for the first time. At the next turn on it will be shut off again.
2.3 Wide input voltage range

The input logic was designed for a wide operating range while the input threshold voltage levels are always linked to the positive input supply voltage. The integrated under voltage lockout circuit will activate the chip at 3V and from this level onward the input high threshold voltage will always be at $V_{IN,H}=0.7*V_{CC1}$. The input low threshold voltage is set at $V_{IN,L}=0.3*V_{CC1}$ accordingly. This linear scaling enables operation directly from a 3.3V digital signal processor but is also capable of accepting output signals from a 12V PFC controller to boost its signal. See Fig 3 on how this linear behavior also increases hysteresis for improved noise immunity at higher input levels. The maximum input voltage rating is $V_{CC1,max}=17V$.

![Fig 2 Output block diagram (left: separate output variant; right: Clamp variant)](image)

2.4 Inverting and non-inverting input

The new 1EDI Compact family members provide the option to use two input signals, one inverting and one non-inverting. These inputs can be used in various combinations depending on the application needs. Apart from using a single PWM input and tying the other one to GND or VCC for permanent activation of the driver, Fig 4 shows further application usage including (A) Input with low voltage differential signals for increased noise immunity,
(B & C) Enable or Shutdown functionality and (D) a simple interlocking function for half-bridge operation.

The IN+ terminal is internally pulled down to favor off state and the IN- terminal is pulled up respectively. This setup also ensures off state in all other configurations where an input signal might be connected to a high impedance output, a weak solder joint or a wire break.

![Diagram showing logic input configurations](image)

**Fig 4** Application usage of logic input

### 3 Performance

#### 3.1 Thermal performance

The dual chip design of this family creates two independent sections of power loss within the package. The input section has been evaluated on its own to exclude effects from the output chip. In the second step of the evaluation input and output operation have been combined as described in Fig 5.

![Diagram showing thermal performance](image)

**Fig 5** Application usage of logic input

The temperature increase of a 1EDI60N12AF as a function of input switching frequency up to $f=5\text{MHz}$ and the supply voltage up to $VCC1=17\text{V}$ can be seen in Fig 6. It clearly shows a temperature increase in the area of the input chip. It is located in the lower right corner of the black rectangular which estimates the body of the SO8 package.
At the evaluation of the output section, the input was supplied with a constant voltage of VCC1=5V. However this influence is minor compared to the power loss in the output chip at VCC2=15V and 50% duty cycle. The thermal effects of capacitive load (CLOAD) variation and different switching frequencies are recorded in Fig 7. The power loss was shared between the driver output stage and the two external gate resistors of 1.2Ω each.

3.2 Output current capability

The strongest drivers of the family 1EDI60I12AF and 1EDI60N12AF are rated with a minimum peak current of Igate=6A at VDS=15V across the output device as hinted in the diagramm in Fig 8. This rating is valid over the whole temperature range so typical values nearly double during a short circuit test without external gate resistors.
3.3 CoolMOS™ C7 switching

The CoolMOS™ IPZ65R095C7 has been evaluated in a boost circuit running at 50% duty cycle and $f_{\text{sw}}=1\text{MHz}$ while driven by the 1EDI60N12AF. At this operation the maximum temperature at the CoolMOS™ was registered with $T_{\text{CM}}=81^\circ\text{C}$ and at the Driver with $T_{\text{Drv}}=64^\circ\text{C}$. At this operation it can be stated that the 1EDI Compact strength is more than sufficient to drive the CoolMOS™ C7 to its full potential.
4 Conclusion
The performance evaluation of the Infineon single channel EiceDRIVER™ Compact family shows its capabilities for applications in a cost-driven, high performance and high power density markets. Wide input supply range and flexible input signal configurations minimize external circuit requirements, complexity and PCB space. The strong driver output and high switching frequency capability eliminates the need for booster stages which again saves PCB space and increases overall power density.

References