Application based modified reliability tests and their physical correlation with lifetime assessment models

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The Power Point Presentation will be available after the conference.

Abstract

Lifetime assessment models for IGBT based power modules used in electric drive applications are extremely useful for preliminary dimensioning and selection of the associated system. Failure estimation is usually modeled on the basis of data from multiple sets of characteristic stress tests like power cycling (PC), thermal cycling (TC) and thermal shock (TST). During real application environment the overall load/stress is usually a combination of these tests with varied durations. Consequently fundamental understanding of the mapping between reliability tests and field application is extremely important. In this paper we have verified the necessity of different parameters used in lifetime assessment models and their limitations. Finite element analysis and analytical models were used to understand such models using laboratory assessable simplified drive cycle stress tests.

1. Introduction

Interconnection failures (e.g. wire bond failure, solder damage etc.) can occur due to thermal loadings caused during operation of IGBT modules. Several physical parameters such as junction temperature (T_j), temperature swing (ΔT_j), case temperature (T_c), on and off times (t_{on}/t_{off}) [1, 2] have been usually associated with such failures. At the same time it is as well important to understand the damage models for these interconnect materials. The damage is usually associated with an accumulation of inelastic (plastic/creep) deformation in materials for interconnects. Proper correlation between the physical parameters and damage relevant parameters needs to be established for improved modeling and validation of lifetime models.
Predicted lifetime is usually based on a mapping of conditions during operation (mission profile) to laboratory based reliability tests for similar module construction. Standard stress tests like PC, TC and TST usually cover the complete range of requirements for mission profile with a certain degree of limitation. Consequently it is important to design simplified driving cycle tests to evaluate and validate models for lifetime prediction. This would be further useful for understanding the accuracy and limitations of lifetime modelling approach currently in use. A simplified driving cycle might consist of three phases: a) Cold start; b) Warm up (or turn on); and c) steady driving. Calculation based on finite element method (FEM) has been used to correlate such driving cycle tests with PC/TC/TST. Actual assessment of lifetime for such a drive cycle has been further assessed with optimized load calculation methods like rain flow counting technique.

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2. Lifetime analysis

2.1. Mission profile analysis

Lifetime analysis of IGBT modules comprises of mission profile based thermal load calculation and calculation of accumulated damage based on lifetime models (Figure 1). Temperature variations in IGBT power module under different mission profile conditions usually involves the following set of equations

$$P_{loss}(t,T) = P_{loss}^{dynamic}(t,T) + P_{loss}^{static}(t,T) \tag{1}$$

$$\Delta T_j(t) = \int_0^t P_{loss}^{IGBT}(\tau, T_j) \cdot dZth_{j-a}^{IGBT}(t-\tau)d\tau + \int_0^t P_{loss}^{Diode}(\tau, T_j) \cdot dZth_{j-a}^{Diode-IGBT}(t-\tau)d\tau \tag{2}$$

where dZth refers to the time derivative of Zth function.

Mission profile description often consists of several thousand of data points, in which case an efficient method for calculation needs to be used for carrying out multiple convolution operations. One such method is based on frequency domain convolution calculation (FFT/IFFT) of equation (2) and update iteratively equations (1) – (2) till convergence. Usually dZth(t) function is of rapidly decaying nature and using methods such as overlap-add convolution, big data sets can be handled easily.

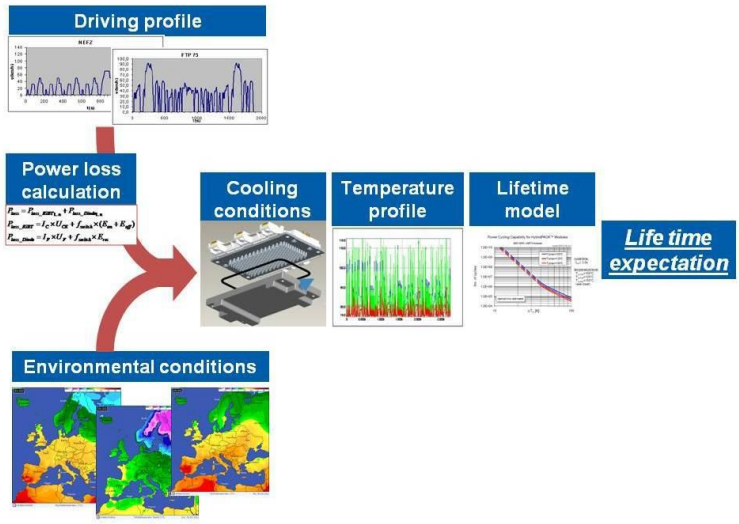

Figure 1. Steps involved in lifetime calculation of IGBT module

Cycle counting algorithm is then applied on this temperature profile to obtain different characteristic parameters for the lifetime model.

2.2. Lifetime models

Lifetime models are based on data from active power cycling and passive thermal cycling tests. Different electrical failure criteria are used for assessment and Arrhenius models are used to fit the failure data. At present the following models are accepted widely for calculation of cycles to failure [1].

PC: $$N_{PC} \propto \Delta T_j^{-n_1} \cdot \exp\left(\frac{n_2}{T_{j\max} - \frac{\Delta T}{2}}\right) \cdot t_{on}^{-n_3} \qquad t_{on} = 1 \ldots 60s \tag{3a}$$

TC: $$N_{TC} \propto \Delta T_j^{-n_1} \tag{3b}$$

The cumulative damage is then calculated using Miners law based on contribution from individual counted cycles.

3. Failure during PC/TC test

3.1. Different loading conditions (PC v/s TC)

During active loading (PC) the temperature rise at any point in the IGBT module is given by the following equation:

$$T_i(t) = T_c + \int_0^t P_{loss}^{IGBT}(\tau) \cdot dZth_{i-c}^{IGBT}(t-\tau)d\tau + \int_0^t P_{loss}^{Diode}(\tau) \cdot dZth_{i-c}^{Diode}(t-\tau)d\tau \quad (4)$$

The temperature distribution in PC is non-uniform in the complete package. However in thermal cycling (TC) the temperature is almost constant in the complete package. Hence the mechanical loading in PC is both an effect of temperature mismatch and CTE mismatch whereas in TC only CTE mismatch plays a role. From mechanical stress point of view, the stress consists of mainly three components: in-plane axial, out-of-plane peeling and out-of-plane shear stress.

For the case of TC, the in-plane axial stress results from CTE mismatch between individual layers and the apparent/average CTE of the module stack. The same is true also for PC however the non-uniform temperature distribution results in an additional stress. The average CTE (α) of a multiple material stack under uniform temperature conditions with bending restrictions can be calculated using

$$\alpha_{CTE}^{avg} = \frac{\sum E \cdot \alpha_{CTE} \cdot h}{\sum E \cdot h} \quad (5)$$

For the case of a typical IGBT power module package with copper base plate this value lies between 14-15 ppm/K. An approximate model to calculate the in-plane axial stress occurring in any layer (*i*) of the IGBT module can be written as

$$\sigma_{xx}^{i} = E_i \cdot (\alpha_i - \alpha_{CTE}^{avg}) \cdot (T_c - T_{ref}) + E_i \cdot (\alpha_i - 0) \cdot (T_i - T_c) \quad (6)$$

The first component in the above equation corresponds to a uniform TC thermal load whereas the second component accounts for the non-uniform PC thermal load. As an example we can compare the stresses resulting in chip solder layer (Elastic modulus = 40GPa; CTE = 20e-6ppm/K) from T_j = 100°C for both PC and TC however T_c = 65°C for PC as follows:

1) PC: σ_{xx} = 40e3.(20e-6 – 14e-6).(65-25) + 40e3.(20e-6 – 0).(100-65) = 37.6MPa
2) TC: σ_{xx} = 40e3.(20e-6 – 14e-6).(100-25) + 40e3.(20e-6 – 0).(100-100) = 18MPa

Clearly we can see that for same junction temperature, PC introduces an extra stress component as compared to TC depending on Zth_{j-c} and applied power.

Peeling and out-of-plane shear stress is usually distributed near the free edges and is dependent on the interfacial stiffness.

3.2. Solder fatigue during PC/TC

Stress during PC/TC

Stress during PC/TC test in chip and system solder as calculated using linear elastic stress analysis is shown in the following figure.

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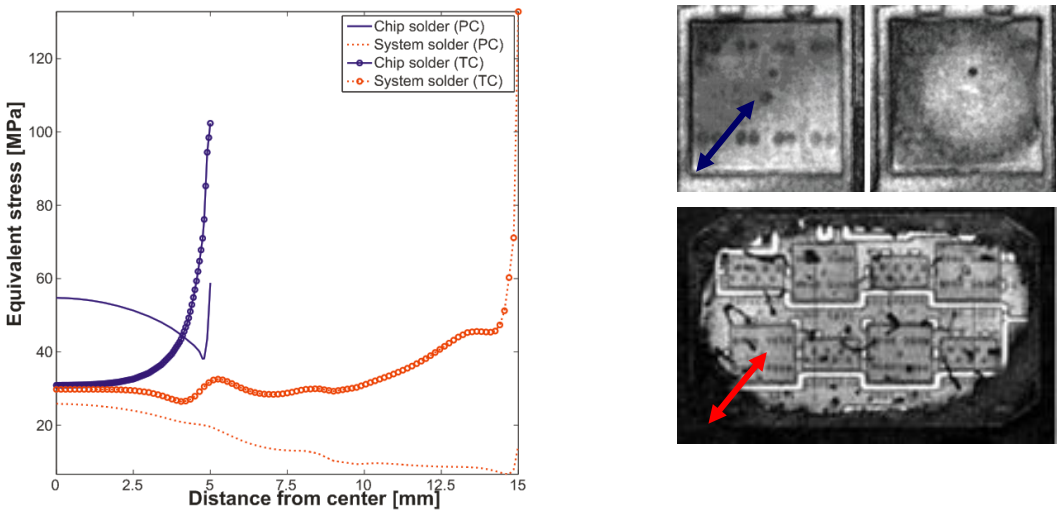

Figure 2. Stress distribtion in chip and system under PC/TC loading resulting in chip and system solder fatigue.

PC load results in highest stress at the centre of chip solder and further a stress peak at its edge resulting from peeling stress. During PC, stress in system solder is extremely low. In contrary TC results in high peeling stress at the free edge of system solder which is greater than that of at chip solder edge. The stress inside the body of both the solder layers is same in the case of TC. These results correlate well with the experimentally observed failure location after PC and TC test (Figure 2). Exact value of peeling stress mainly depends on the shape of solder fillet and its thickness near the edge (not included in FE analysis).

However stress is only a preliminary factor to understand the damage locations and for detailed understanding an inelastic creep analysis was done.

Solder fatigue is defined in terms of creep strain (or energy) accumulation during a stress cycle. A model describing the inelastic creep behaviour of solder material is given by:

$$\frac{d\varepsilon^{cr}}{dt} = A_1\left[\sinh\left(A_2\sigma(t)\right)\right]^{A_3}\exp\left(\frac{-A_4}{T_{abs}(t)}\right) \tag{7}$$

where, A_i refers to the different material parameters as obtained from isothermal stress experiments on solder specimen [4], σ refers to the equivalent stress in solder and T_{abs} refers to temperature in absolute scale. The total strain behaviour of the solder material is described by the following equation

$$\varepsilon^{tot} = \varepsilon^{el} + \varepsilon^{cr} + \varepsilon^{th} \tag{8}$$

Equation (7) and (8) can be solved simultaneously to calculate the accumulated creep strain (either using FEM or analytical 1D relation).

Creep accumulation during PC/TC

During PC, creep strain occurs in chip solder due to the fact that the “free” thermal expansion of solder is largely hindered by the relatively cooler base plate. Stress evolves in chip solder joints in three stages: (1) During the initial transient phase of the active load cycle, the stress in solder usually reaches a peak value within a very short time of approximately 1-2s; (2) after this time stress relaxation occurs in solder; (3) and eventually the stress reaches steady state (about 60-70s). Creep accumulation mainly usually occurs during the first and second stage and is very limited during last stage. A simple analytical model combining equations (1) and (2) was developed as follows:

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$$\dot{\sigma} = -EA_1\left[\sinh\left(A_2\sigma\right)\right]^{A_3} \exp\left(\frac{-A_4}{T_{ref} + Zth_{j-a}(t)\cdot P_{loss}}\right) + E\frac{dZth_{j-a}(t)}{dt}\Delta\alpha_{CTE}\cdot P_{loss} \quad (9)$$

The resulting creep strain in the chip solder layer is shown in Figure 3. It shows that for active loading with longer on time (ton > 60-70s) the influence of on time is relatively low.

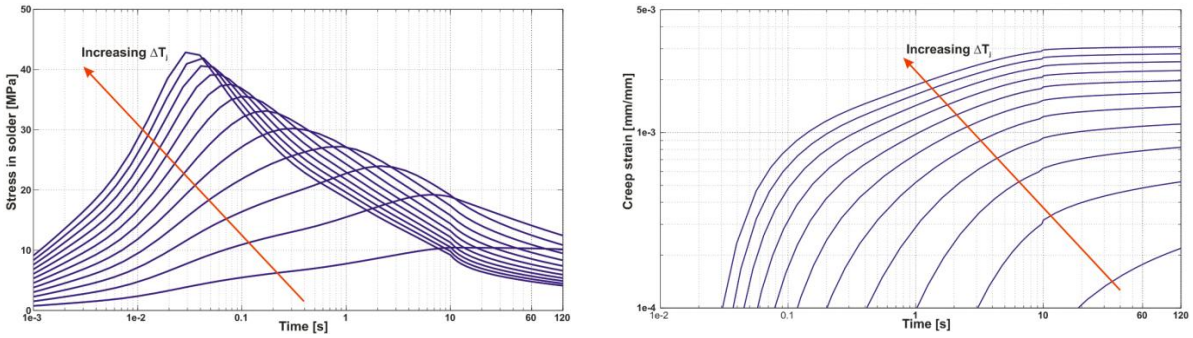

Figure 3. Stress relaxation and creep „saturation“ in chip solder for different on time

Fatigue occurring during TC is usually more dominant in system solder layer as mentioned in the previous section. The stress/creep in system solder is mainly controlled by the temperature swing (ΔT_j) and to a certain extent on the ramp rate.

3.3. Wire bond fatigue during PC

Stress during PC/TC test in wire bond interface as calculated using linear elastic stress analysis is shown in the Figure 4. The stress is mainly dependent on the local CTE mismatch between wire bond and silicon.

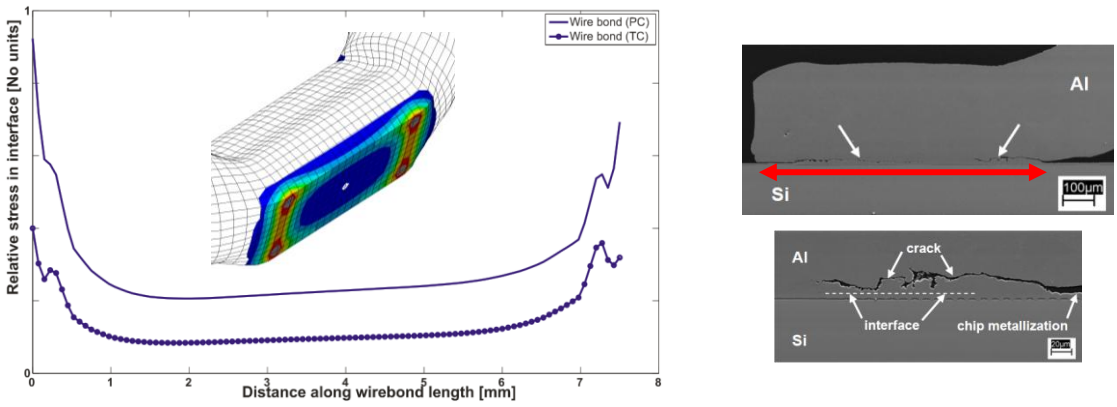

Figure 4. Relative stresses in wire bond under PC and TC loading and related damage location

It can be clearly seen that the equivalent stress during PC is much higher and is the responsible cause for wire bond failure. Further the peeling stress component is extremely high at the edge which usually causes the observed wire bond liftoff. For conditions where the equivalent stress exceeds the characteristic yield strength, plastic strain accumulates in wire bond ultimately resulting in fatigue failure.

4. Application relevant mission profile

A simplified driving cycle (Figure 5) might consist of three phases: a) Cold start; b) Warm up (or turn on); and c) steady driving. Such a cycle can be thought of as multiple smaller tem-

perature swings (Power cycling) superimposed on an extremely large temperature swing (Thermal cycling) which is hereafter referred as IOL (Intermittent Operating Life) test.

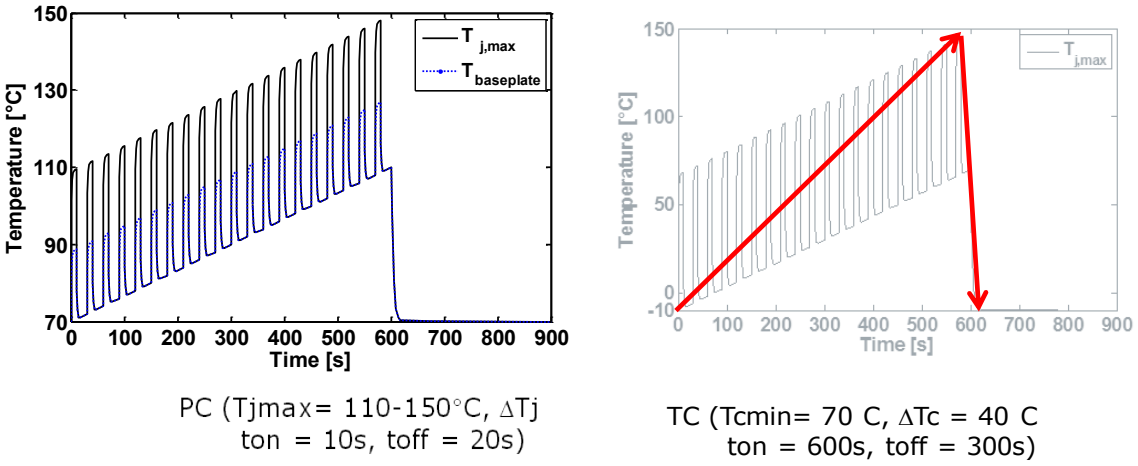

Figure 5. Application relevant mission profile with superposition of PC and TC cycles

Three dimensional finite element analyses were performed to physically correlate the inelastic strain accumulation in the solder and wire bonds. Figure 6 shows the contribution from individual PC and TC as compared to a complete IOL test cycle. The results show that for wire bond the damage accumulation from individual cycles is straightforward. However for chip solder due to nonlinear dependence of creep on stress, fatigue accumulation is not exactly linear. Further it is shown that there is slight contribution of TC on chip solder creep however the main contribution comes from the active PC. This results correlate well with experimental observation reported in Ref [6] where it was shown that TC is dominant failure mode for similar IOL profile. In lifetime calculation model, the effect of TC on chip solder is not directly modeled however the influence is captured by one big cycle marked with red in Figure 5.

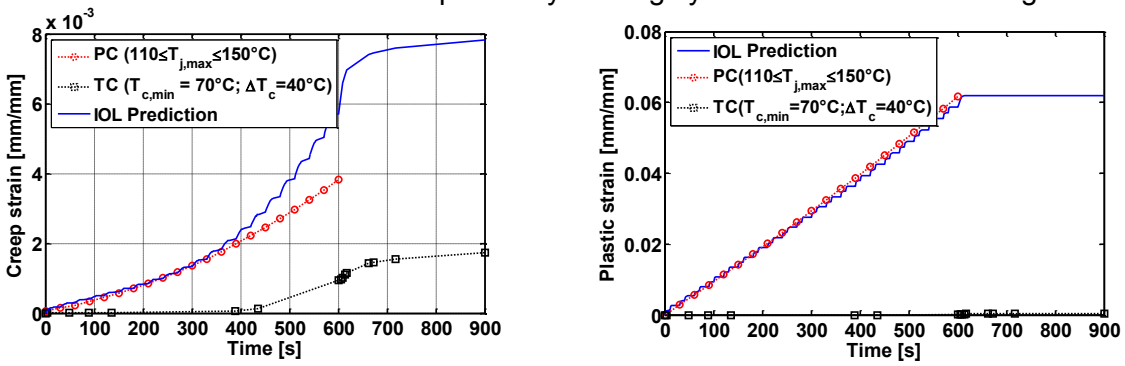

Figure 6. Individual contribution from PC and TC in comparison to overall creep/plastic strain

Using measured junction and case temperatures on the tested modules, lifetime calculation method predicted a cycle count of 14095 big cycles (cycle time = 900s) which was quite close to the observed cycles to failure of around 12500 cycles. Further vertification tests are currently undergoing using a similar cycle like illustrated in Figure 5 with a stationary operating phase. The results will be presented during the oral session at PCIM.

5. Conclusion

Different parameters involved in the models used for lifetime assessment of IGBT based modules were assessed. Finite element method along with analytical models was used for this purpose. The main conclusion can be stated as follows:

- Stress in chip solder mainly occurs during PC and to a less extent during TC. Spatial stress distribution shows mainly higher values at the centre of the chip and peeling stresses at the edge of the chip. The peeling stress at the edge can be influenced by the nearness of the chips as well [5].
- Stress in system solder exclusively occurs during TC. Peeling stress near the edges is responsible for the delamination of system solder.
- During power cycling, stress relaxation usually starts very early (t ~1-2s), and the dependence of creep strain on ton saturates after t>50-60s.
- Peeling and shear stress in wire bond mainly occurs during thermal cycling.

A simplified driving cycle was used to correlate stress during a complex application scenario with stress tests like PC, TC and TST.

Acknowledgment

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6. Literature

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