IGBT inverter with increased power density by use of a high-temperature-capable and low-inductance design
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Abstract

Increasing the power density is a key development factor for power electronic inverter systems. In [1] a converter system enabling a power density of 20kW/l with the use of novel devices like SiC JFET switches and efficient matrix converter topology was demonstrated. The point of interest is how much power density is possible in a present commercial, classical full bridge inverter system through the design optimization of the IGBT module and the inverter. The output power of such a system is not only limited by the semiconductors’ power losses and their maximum operation temperature, but also by stray inductances defining maximum switchable currents in a given set-up. At the same time peripheral devices like control electronics and passive components can also limit the power density through their temperature limit. This paper demonstrates the power density enhancements achievable through usage of devices with higher operation temperatures in an ultra-low inductance design also taking care of peripheral temperature requirements.

1. Introduction

IGBT chips are developed to fit into a commercial power module and inverter setups which incorporate a certain parasitic inductance in the commutation circuitry. To avoid destructive overvoltage during IGBT turn-off, technological parameters like doping profiles are adapted. However, such measures lead to an increased tail current and consequently cause higher turn-off losses. The occurring IGBT collector overvoltage is directly proportional to the stray inductance and to the current slope and is described by the equation $\Delta U = -L_\sigma\frac{di}{dt}$. The current shape is also dependent on the applied voltage between collector and emitter. Higher voltage applied to the IGBT during turn-off causes an earlier removal of charges from the device and the tail current disappears [3]. This means that the parasitic inductance that causes an overvoltage in turn accelerates the current fall and this again causes a higher over-voltage.

In addition, high $\frac{di}{dt}$ and $L_\sigma$ can lead to oscillations that cause electromagnetic interference (EMI). This is a consequence of exciting a resonant circuit, consisting of the parasitic inductance in the commutation loop and the chip capacitance, by the high frequency components of current and voltage.

Figure 1 illustrates exemplary the overvoltage peak and resulting voltage oscillatory behavior at IGBT turn-off in a setup with too large stray inductance.

Figure 1: IGBT turn-off with $\Delta U$ peak voltage and oscillations
An increase of the IGBT operation temperature $T_{J\text{\text{-}V}}$ of today's 150°C at IGBT 4 to 175°C at IGBT 5 allows increased power dissipation and a higher amount of switching current per device. Increased current ratings, though, require reduced stray inductance of the commutation loop in total in order to avoid serious problems with voltage and EMI requirements. This requirement may be summarized by the simple constraint $L_{\sigma} \cdot I = \text{constant}$ [3].

Hence, available package platforms and inverter setups may prevent enhanced inverter operation due to the built-up overvoltage and oscillations during turn-off, especially at overload conditions. To avoid this, the IGBT could be developed with lower switching speed and increased tail current. This would lead to higher power losses and is in contradiction to the demand of higher power density. The elegant solution to cope with this challenge is to reduce the parasitic inductance to a minimum, such that the IGBT and freewheeling diode can be driven faster by higher currents without any restriction. The increase of power losses at turn-on due to lower parasitic inductances [7], [8] has to be compensated with chips having faster turn-on behavior and freewheeling diodes with lower reverse recovery charge.

The conclusion is that a low inductance system is necessary to obtain higher power density with IGBTs operating at higher junction temperature and optimized dynamic losses without EMI and overvoltage peak restrictions.

2. Low inductance and high temperature capable inverter setup

Today’s standard inverter setup in the power range of 200kVA with 1200V IGBTs and in B6 topology are in many cases constituted of a laminated bus bar to connect the DC-Link capacitors and the power module. An example for this type of design is the Infineon Stack 6PS0400R12KE3-3F-C4V, visible in figure 2.

![Figure 2](image_url)

This inverter stack is designed with 62mm FF400R12KE3 half bridge modules comprising 1200V IGBT3 400A IGBTs, electrolyte DC-Link capacitors and a bus bar with strip line geometry [3]. All devices are interconnected with screws; at this point the strip line geometry is interrupted. This setup achieves an overall system inductance of 70nH and a maximum output power of 164kVA. This system serves as basis to compare with a low inductance and high temperature capable design.
2.1 Low inductance design

The optimum way to reduce the system inductance as much as possible is to keep a strip line structure in the whole system of capacitors, bus bar and module [3]. This is unfortunately not possible with today’s usual devices due to intersectional screw connections caused by the interfaces between the capacitors respectively the power modules and the DC bus bar. These interruptions result in segments with geometry like two-wire connectors and lead to a dominating effect regarding the inductance. For this study a new system design with prototype devices has been designed and the benefits have been evaluated.

The newly developed power module [3] follows the strip line concept, using the principle of a laminar layout and multiple connection points in an interleaved structure to minimize the total system inductance. To contact the module, the proven Pressfit technology [4] of Infineon was used. Arranging pins in a line-wise way allows a very low-inductive connection to the rest of the system.

Following the idea of avoiding bolt connections [3] a prototype DC-Link capacitor in power capacitor chip (PCC) [10], [11] concept with Infineon’s Pressfit contact has been provided by the company Epcos. Due to the usage of this type of connectors, a high current PCB was chosen to interconnect the devices. This allows a continuous strip line design in the whole power electronic system. The PCC concept has also a very low equivalent series inductance (ESL) and due to the high voltage capability [10] no series connection of capacitors is necessary. These are two advantages for the reduction of the parasitic inductance compared to electrolytic devices.

Figure 3 shows the module prototype and the whole inverter system.

Figure 3: Left side, low inductive IGBT half bridge module prototype with press-fit connections. Right side, B6 inverter system design with low inductance modules and PCC capacitors, connected via a high current PCB using multiple press fit contacts.
Overall, all measures result in a system inductance below 10nH, about 60nH lower than the reference stack with 70nH. The effect in the turn-off behavior using fast IGBT 3 1200V chips at nominal conditions by different stray inductance values can be seen in figure 4.

Figure 4: Different switching behavior by different parasitic inductance

Figure 4a depicts the switching behavior of a FF400R12KT3, a 62mm module with IGBT3 fast technology. The system inductance has a value of 70nH. It is visible, that with this parasitic inductance the fast IGBT3 chip tends to oscillate. The overvoltage is 280V. It is clear why the reference stack is mounted with a slower FF400R12KE3 with more tail current – and therefore with higher turn-off losses and softer switching – instead of the FF400R12KT3.

By reducing the inductance of the DC-Link setup to 5nH the overvoltage with the 62mm module is reduced down to 160V, see figure 4b. The oscillation has almost been eliminated. The result of the same measurement setup, but with the new low-inductance module instead of the 62mm module is shown in figure 4c. A further reduction of the overvoltage during the IGBT turn-off to 80V only is achieved. No oscillation occurs. The current falls with softer tail due to the lower overvoltage compared to the system with higher inductance.

This low-inductance setup allows the use of faster switching IGBTs with higher current carrying capability and reduced power losses.

2.2 High temperature capable setup

The maximum operation temperature of the prototype IGBT 5 chip is 175°C, therefore the module is based on Infineon’s new .XT technology [2] [5] [6] to work without lifetime restriction at such high temperature level. Several Pressfit pins in parallel are reducing the ohmic and thermal contact resistance and the thermal conductivity is improved [9]. Furthermore this technology has an advantage at high temperature cycling application regarding lifetime compared to solder joint technique [4].

High current PCBs offer the possibility of a maximum operation temperature of 150°C, while typical laminated bus bars have 105°C; specially devices 125°C. To allow a high current carrying capability the chosen internal conductor has a thickness of 800µm per pole.

PCC DC-Link capacitors have a very low equivalent series resistance (ESR), therefore a high capacitor current per volume unit is possible. Another important advantage of this type of device is the thermal property, especially regarding maximum ambient temperature and lifetime compared to electrolyte technology [10], [11].

The IGBT driver circuit is positioned mechanically decoupled from the power part of the stack. This is done to take the expected hot spots into consideration. The study in [2] shows that a maximum temperature of 84°C is achieved on the PCB during an operation of the IGBT at 175°C and a cooling air inlet temperature of 25°C. The allowed worst case air temperature of 40°C of the reference stack would result in a maximum PCB temperature of 90°C. Therefore the components selected to drive the IGBT module have to withstand such condition without life time restriction. Infineon’s IGBT driver 2ED02012FA allows a maximum ambient temperature of 125°C and was chosen to control the IGBTs.
3. Increased inverter output power with faster chips at higher junction temperature

Having reduced the system’s commutation inductance to a value of less than 10nH, increased current and power densities enabled by increased junction temperatures may easily be handled. Moreover, even fast switching devices comprising reduced power losses may be implemented without coming into trouble with overvoltage and softness restrictions.

An oscilloscope picture of the turn-off event at 1200A - two times the module nominal current - and increased DC-Link voltage of 800V in the low inductance system is depicted in figure 5.

![Figure 5: Fast IGBT turn-off at 1200A - two times module nominal current - and 800V DC-Link voltage](image)

It is visible that the fast IGBT at overload condition has still enough tail current, the overvoltage peak has a value of 1090V and no oscillation is visible. A further optimization step on the chip design regarding lower tail current and consequently lower turn off losses is possible.

Figure 6 shows a comparison of the relation between IGBT junction temperatures and output current of the reference stack with IGBT E3 and E4 versus the low inductance prototype with fast IGBT 5 chips and $T_{VJ,max}$ of 175°C.

![Figure 6: Relation between IGBT junction temperatures and stack inverter output current at different chip technologies and system inductance](image)

It is clear that the new design allows an increase of the output current by 24% as compared to the IGBT 3 and 12% as compared to IGBT 4 at $T_{VJ}$ 125°C respectively $T_{VJ}$ 150°C. The increase of the maximum junction temperature to 175°C result in 75% higher output current than an IGBT 3 solution and 30% more current as compared to IGBT 4.
Concerning power density the prototype low inductance and high temperature capable stack converter achieved a 50% higher value compared to the reference stack with IGBT 4. In absolute numbers the low-inductance air-cooled prototype stack achieves circa 24 kVA/l.

4. Conclusion

The increase of the maximum operation temperature leads to higher current capability per chip area. This can bring inverter designs with high parasitic inductance to the limit concerning overvoltage peak and oscillations during turn-off. The application of fast IGBT chips at higher current is only possible with low-inductive module and system design. This is a door opener and requirement for the application of other fast chips like SiC JFET with reduced electrical magnetic interference and lower overvoltage peaks.

Beside this, care must be taken regarding the temperature raise seen at other system components to guarantee that the frequency inverter’s lifetime does not suffer from an elevated temperature. A good thermal management also considering the surrounding area of the module becomes mandatory.

The study shows that the usage of chips with optimized energy losses and higher operation temperature resulted in 50% higher power density compared to today’s state of the art technology. An advance step is possible through further tuning of the IGBT chip design or usage of new die technologies.

5. Acknowledgment

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6. Literature

[9] Tao Hong, Current capability enhancement of busbars or PCBs by thermal conduction, PCIM 2012, Nuremberg, Germany