

1st industrialized 1200V SiC JFET module for high energy efficiency applications

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Abstract

Reducing losses is one of the most challenging trends in power electronics. Wide bandgap devices like SiC switches are known to show best performance in terms of lowering conduction and switching losses. It is one decade ago, that Infineon introduced the SiC Schottky barrier diode to the market. Now the SiC JFET is matured and convinces with low power loss, high reliability and robustness, ease of use and right cost position [1]. This paper presents the first industrialized power module making use of the excellent JFET properties.

1. Introduction

The integration of SiC power devices into a power module is not a completely new task. Some years ago the loss saving potential of SiC Schottky barrier diodes in an Infineon PrimePACK™ 2 module was demonstrated [2] reducing the turn-on energy of IGBTs and the recovery losses of the diodes, respectively. Since the SiC JFET is available as a product very soon, the full SiC loss saving potential will be available by getting rid of IGBTs tail current losses as well. Target applications for the new SiC JFET module will be the efficiency sensitive field of renewable energy and UPS systems.

2. Module topology

For the new 1200V/30A SiC JFET module a half bridge topology was chosen to suit most customer needs. In Fig. 1 the module schematic, the easy1B module itself and an exemplary chip arrangement can be seen. One switch consists of three single SiC JFET chips with maximum on-state resistance at room temperature of 100mΩ each. In order to overcome the normally-on issue of the pure JFET, two parallel low voltage p-channel MOSFETs are connected in series to the JFET group. The MOSFET part is very low ohmic and causes only a 3-4% total $R_{DS(on)}$ increase at JFET operating temperature of 125°C.

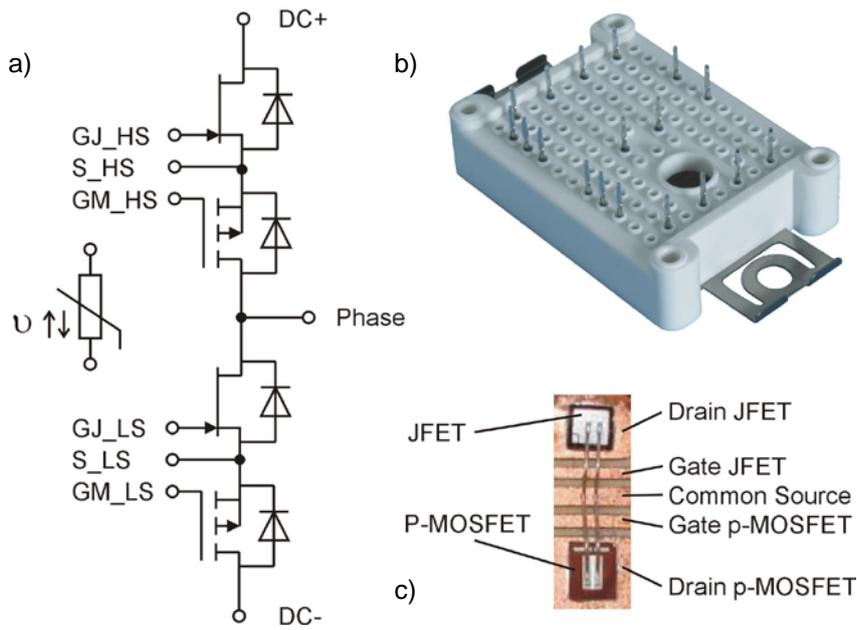


Fig. 1
 Direct Driven JFET:
 a) module schematic
 b) 1200V/30A Easy1B module
 c) exemplary chip arrangement

3. Gate Drive Aspects

The basic approach of the so-called "Direct Driven JFET" was demonstrated in [3]. The main idea behind this is to permanently turn on the low voltage MOSFET in normal operation. Then, the JFET is controlled by means of its own gate drive stage (JFET driver in Fig. 2) performing the desired switching caused by the logic signal "ctrl". Compared to a conventional cascode circuit, the Direct Driven JFET approach allows lowest dynamic losses combined with a good controllability of the JFET switching transients.

In case of startup or malfunction of the JFET driver circuitry, the JFET gate driver stage may not be able to support sufficient voltage to pinch off the JFET. Then, the p-channel MOSFET is turned off and allows conventional Cascode operation by means of diode D1.

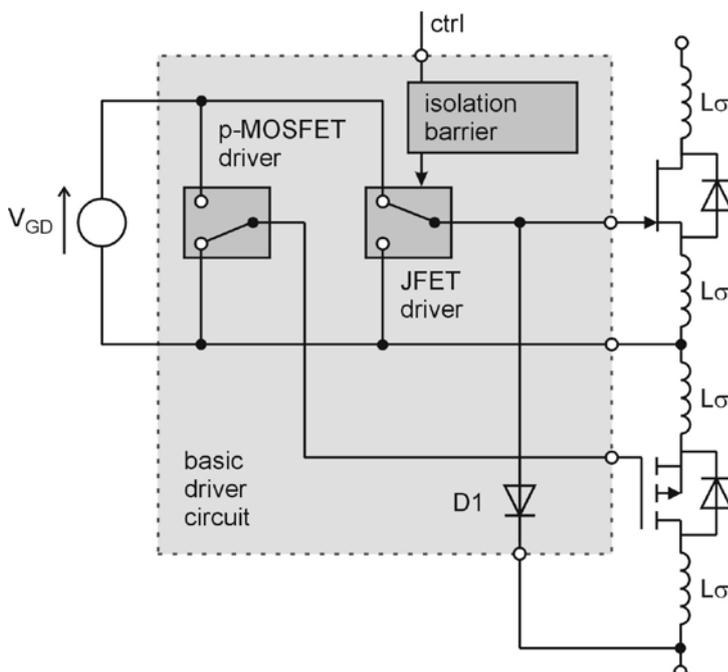


Fig. 2 The basic Direct Driven JFET scheme for controlling the normally-on JFET and its series connected low voltage p-channel MOSFET
 L_σ : stray inductance elements

The p-channel MOSFET was chosen because it allows the lowest stray inductance in the JFET gate drive path and makes an integration of the whole driver circuitry in one single gate drive IC most simple.

Regarding the last mentioned aspect, Infineon is currently developing an IC solution, which allows the customer to operate the Direct Driven JFET circuit like a conventional normally-off switch. Furthermore, all the safety aspects will be managed inside the IC without the need of taking care from customer side. An important aspect for the JFET gate drive is the Gate-Source-voltage-window shown in Fig. 3. The upper line corresponds to the JFET threshold-voltage, which becomes smaller the higher the junction temperature T_J is. The lower graph stands for the so called punch-through voltage, which is the lowest gate-source-voltage leading to a gate leakage current of less than 1mA. The area between both lines indicates the reasonable gate driver supply voltage. Although with increasing T_J both lines come more close to each other, even at $T_J=175^\circ\text{C}$ a sufficiently large voltage window of approx. 7V is open.

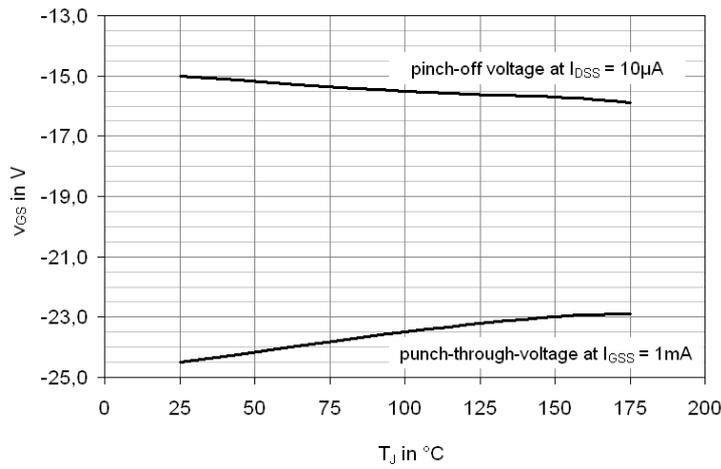


Fig. 3 Gate voltage window for safe JFET turn-off state as function of junction temperature T_J
 I_{DSS} : Drain-Source leakage current,
 I_{GSS} : Gate-Source leakage current

4. Static behavior

The output characteristic of the 1200V/30A SiC JFET module can be seen in Fig. 4. Regardless whether the module is operated in forward or reverse direction, for the gate-source-voltage $v_{GS}=0$ the JFET behaves pure ohmic. If the JFET is turned off in reverse conduction mode (e.g. $v_{GS}=-19\text{V}$), the intrinsic body diode can take over the load current. This is a very important fact, since there is no need for an additional freewheeling diode which would result in additional module area and costs.

Because of the relatively high voltage drop across the JFET device in body diode mode, the duration of this operation will be restricted to typical values of interlock times of fast inverter systems. The consequence must be to turn on the JFET device even if it conducts load current in reverse direction. Then, the body diode conduction time is limited to the interlock time of the target system.

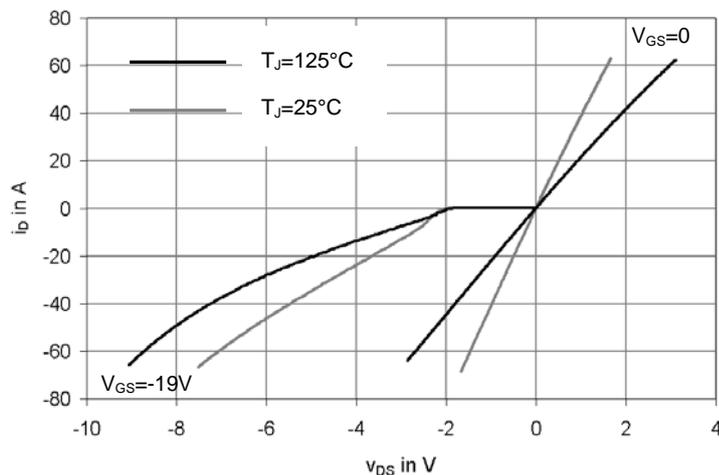


Fig. 4 Static behavior of the 1200V/30A SiC JFET module

5. Laboratory setup

In Fig. 5 the test setup for characterizing the prototype half bridge module is shown. The current was measured using a 200MHz Bergoz current transducer [4]. The gate driver for the high and low side switches were built on a single PCB each. The PCBs are equipped with Infineon's 1ED020112-F gate driver IC with coreless transformer technology, a 6A emitter follower stage for driving all the three parallel JFETs of one single switch and some small signal parts for p-channel MOSFET control. Latter is ideally switched only once the circuit starts up and thus needs no strong gate drive.

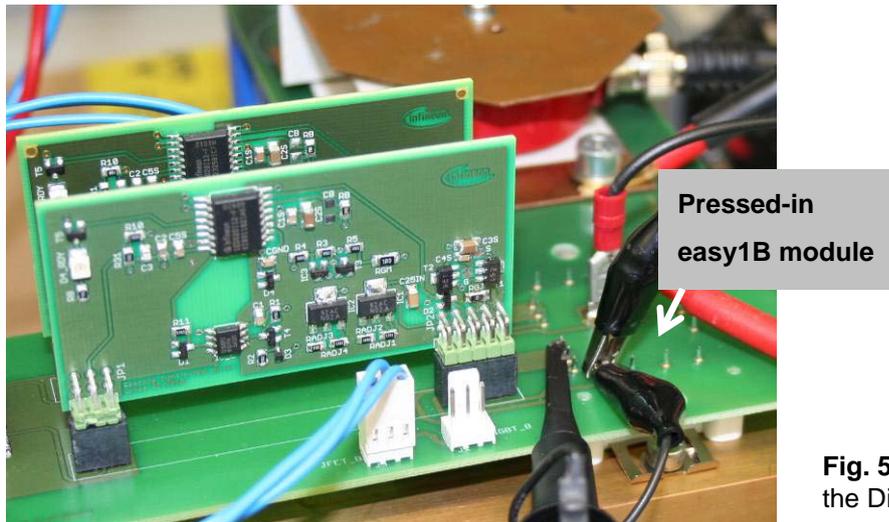


Fig. 5 Laboratory test setup for the Direct Driven JFET module

Furthermore, the voltage V_{GD} (refer to Fig. 2) is supported by an on-board LDO voltage regulator, its output voltage is monitored by a special circuit.

The operation of the Direct Driven JFET gate drive under full DC-link voltage is shown in Fig. 6. Between t_0 and t_1 V_{GD} drops below a certain limit and the JFET driver becomes disabled. If the driver input signal would be logical one, immediately the connected JFETs are turned off. Further PWM input signals are ignored from here on. At t_1 the p-MOSFET is turned off. It is worth to notice, that the p-MOSFET stays in the off-state, even if no voltage is applied to the gate drive. After t_1 the driver voltage V_{GD} further drops until at t_2 the JFET pinch-off-voltage is reached. Then the JFET becomes slightly conductive and charges the p-MOSFETs output capacitance. At t_3 the system is in full Cascode-operation mode and the Direct Driven JFET switch is normally-off without gate drive supply voltage.

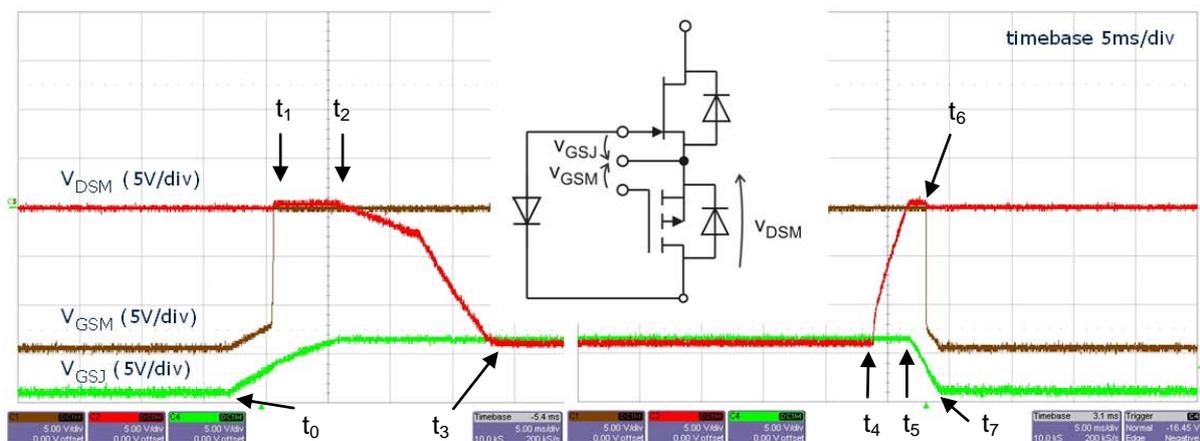


Fig. 6 Direct Driven JFET approach in case of gate driver supply voltage fails (left) and returns (right), both operations under 600V DC-link voltage, driver input signal is logical zero

In the right part of Fig. 6 the above explained process is shown vice versa. At t_4 the voltage V_{GD} comes back. In the way V_{GD} rises, the MOSFETs voltage v_{DSM} increases. The driver supply voltage has reached the JFETs pinch-off-level at t_5 . Further increase in V_{GD} leads to trigger the p-MOSFET turn-on threshold at t_6 . At t_7 the system is in normal mode and PWM pulses would be transmitted again.

To sum up, thanks to the implemented Cascode operation the system behaves like pure normally-off device. Like explained above, the driver circuit handles all the safety aspects internally resulting in no need for additional normally-on protection measures. From the customer point of view, the Direct Driven JFET topology acts like a conventional normally-off device.

6. Dynamic behavior

The switching waveforms of the JFET module can be seen in Fig. 7. Compared to the Direct Driven JFET topology with n-channel MOSFET [3], the p-channel MOSFET solution introduces no additional stray inductances to the JFET's gate drive circuit resulting in very fast turn-on and turn-off responses.

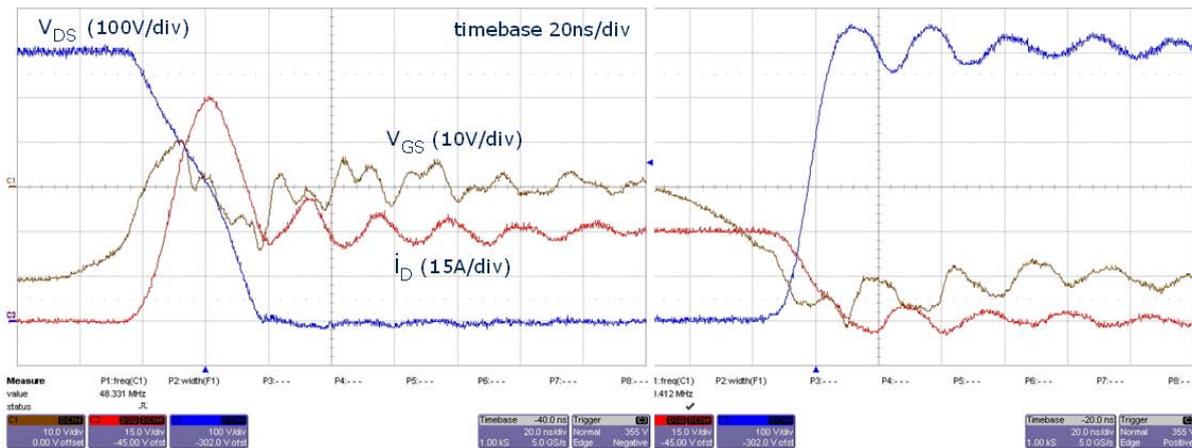


Fig. 7 Switching waveforms of the Direct Driven JFET module at $T_J=125^\circ\text{C}$, $V_{DC}=600\text{V}$, $i_D=30\text{A}$ and $R_{G,ext}=0$

The switching waveforms show the current commutation between lowside JFETs and highside JFET body diodes. With respect to the recovery current in the turn on waveform, current only changes while the Drain-Source-voltage drops. Therefore, the main part of the reverse recovery current is of capacitive nature. The commutation against the JFET body diode can be regarded as quite similar compared to low loss Schottky diode commutation.

In Fig. 8 the low switching losses of the Direct Driven JFET module are depicted. Due to the absence of diode tail current, no recovery-losses occur.

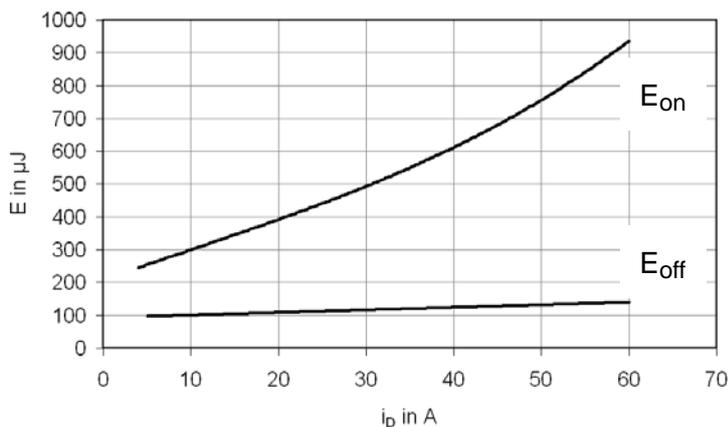


Fig. 8 Dynamic losses of the half bridge JFET module at $T_J=125^\circ\text{C}$ and $R_{G,ext}=0$

7. Inverter loss and efficiency calculation

To demonstrate the loss-saving-potential of the SiC JFET module, a total loss calculation for a 22kVA three-phase two-level inverter was done. As a challenger for the JFET-module, a 1200V/25A HighSpeed3-IGBT equipped with two 1200V/7.5A SiC Schottky barrier diodes was chosen. For fastest switching, the external gate resistor of the JFET and the IGBT circuits were set to zero.

The turn-on and turn-off energies for switching the HighSpeed3-IGBT at 600V, 30A and $T_J=125^\circ\text{C}$ are measured to be 916 μJ (JFET 490 μJ) and 1480 μJ (JFET 117 μJ), respectively. Like shown in Fig. 9, the excellent JFET properties enable loss reduction down to 35% of those of fastest IGBT technology combined with SiC-diodes. Up to approximately 35kHz switching frequency, the JFET inverter's efficiency exceeds 99%.

Apart from the efficiency point of view, the JFET module is ideally suited for power electronic designs with high switching frequencies targeting the decrease of passives volume for achieving high power densities and lowered overall system costs.

Lab-tests with a SiC JFET module based inverter confirm these high potentials [5].

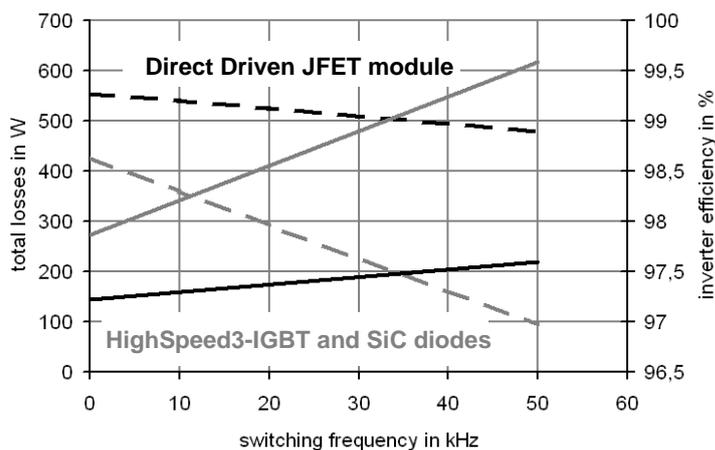


Fig. 9 Calculated total inverter losses (solid lines) and efficiency (dashed lines), $S=22\text{kVA}$, $V_{\text{DC}}=600\text{V}$, $U_{\text{ph}}=230\text{V}$, $I_{\text{ph}}=31.8\text{A}$, $\cos\varphi=0.9$, $T_J=125^\circ\text{C}$

8. Summary

A new normally-on SiC JFET based half bridge module was shown. The Direct Driven JFET topology makes use of series connected p-channel MOSFETs. Combined with an adequate gate drive circuit, the Direct Driven JFET approach can be regarded as practically normally-off. The very low switching losses of the JFET module enable ultra low loss power electronic designs. Benchmarked on fastest IGBT technology combined with SiC Schottky barrier diodes, the SiC JFET module can decrease overall inverter losses down to 35% by providing efficiencies of more than 99% for switching frequencies up to 35kHz.

9. References

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