Reliability of Substrate Solder Joints from Power Cycling Tests

Thomas Hunger, Infineon Technologies AG, Warstein, Germany
Reinhold Bayerer, Infineon Technologies AG, Warstein, Germany

Abstract

The lifetime of the solder joint between base plate and ceramic substrate is usually tested by passively heating and cooling the IGBT module (thermal cycling). This provokes failures (delamination) in that solder layer. But, the IGBT and diode dies are actively heated in the application. Other failure modes (e.g. bond wire lift off) are addressed and limit the lifetime. This kind of stress is usually tested via power cycling. In the present paper the power cycling test results are evaluated with respect to failures in the substrate solder. Those tests with their high number of cycles are utilized as an effective thermal cycling test for the substrate solder. Key factor is the prediction of the solder temperature during power cycling. A comparison of the solder joint lifetime from passive thermal and active power cycling at low temperature swings was carried out.

1. Introduction

IGBT modules are subjected to heavy thermal loading in the application caused by the switching and conduction losses of the semiconductor dies during e.g. inverter action. The loading is varying with time thus causing mechanical stress in the mechanical parts of the module, especially in wire bonds and solder joints. This is the reason for crack formation and propagation in the solder layers [1-5]. One of the known consecutive faults is the increase of the thermal resistance which is considered as an end-of-life (EOL) criteria. Therefore, it is important to know how long an IGBT module can be used under certain operating conditions. This is estimated taking the number of cycles from lifetime curves gathered from several accelerated tests into account [6].

Depending on the actual mission profile different failure modes occur. It is known, when dealing with a module having a base plate, that longer power cycles can lead to a delamination of the solder joint between base plate and the ceramic substrate (referred as “substrate solder”). The accelerated lifetime test applied is a thermal cycling test with cycle times in the minute range and around ΔT=80K. In the application the majority of cycles are in a rather low ΔT range. But, cycle times vary.

The paper deals with a comparison of accelerated thermal cycling and power cycling tests with respect to the substrate solder. Because active cycling (power cycling) allows for shorter cycle times a higher number of cycles can be reached in a reasonable time frame, especially when the lower ΔT range is considered.

The paper is organized as follows. After a short introduction to passive and active cycling tests the experimental findings in power cycling tests regarding the substrate solder are given. The investigation is restricted on modules with copper base plates and solders containing lead. To determine the case temperature and its swing in power cycling tests, accurately, the temperature distribution within the module is investigated by means of a thermal finite element simulation taking the properties of the heat sink and heat transfer to ambient into account. The results allow for an assessment of the temperatures within the module. Especially, the relation between junction, base plate and solder temperatures is investigated. As a conclusion, the lifetime curve is extended towards smaller temperature swings.

1.1. Passive Thermal Cycling

In this test the IGBT module is mounted via a layer of thermal grease onto a combined heater and heat sink assembly and undergoes passive temperature swings. Because the cycle time is in the minute range, the module (base plate, ceramic substrates and dies) has a uniform temperature following the external setting. The temperature excursion is expressed in terms of the temperature at the bottom of the base plate, T_C. Typically, ΔT_C is set within the range of 60K to 100K. The failure criterion is the increase of the thermal resistance of 20%.

1.2. Power Cycling

In this test the IGBT module is mounted on a heat sink. The dies are actively heated by a current causing power loss in the dies. The typical

on-time spans from seconds to minutes depending on the maximum junction temperature and swing excursion desired. During off-state the module cools down, afterwards the cycle is repeated. The time to cool down depends on the performance of the cooling system. Due to the direct heating of the dies power cycling allows very fast ramp up of the junction temperature T_J and the case temperature T_C. In combination with an efficient cooling system, the power cycling test allows a very high repetition speed of cycling. The cycle numbers which are practically accessible are by far higher than those of a passive thermal cycling, namely $N>10^6$.

Usually, the EOL failure mechanisms in power cycling and thermal cycling are different. Power cycling addresses bond wire lift off or chip solder fatigue. The first leads to a forward voltage drop increase whereas the second to a thermal resistance increase.

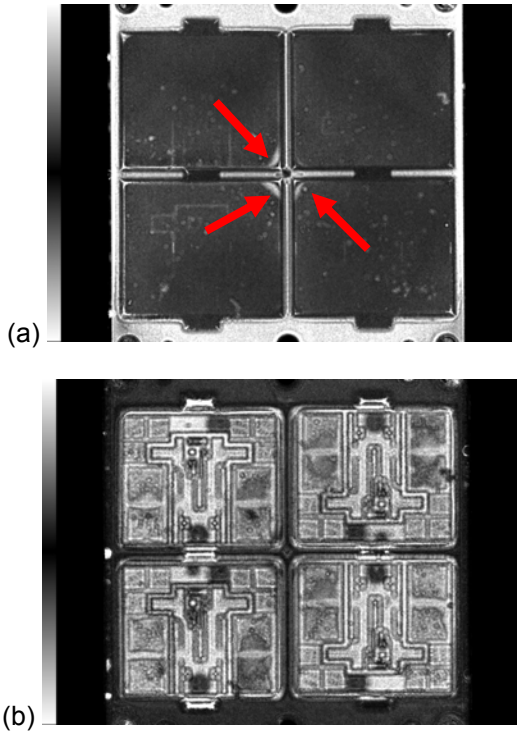

Fig. 1. Ultrasonic images of (a) substrate solder and (b) chip surfaces. The system solder shows starting delamination (red arrows). The chip solder of the IGBT dies shows signs of heavy damage.

The major difference of power cycling to thermal cycling is the non-uniformity of the temperature within the module, i.e. the temperature in the junction differs significantly from those at the case and in the solder layers. Heat spreading causes a temperature profile throughout the module. The temperature swings depend on the position relative to the active dies. The temperature across the base plate is not constant. It reaches the maximum values below the die positions. The same holds true for the substrate solder. The corners and edges have lower temperatures than below the dies and thus undergo lower temperature swings.

2. Experimental findings on system solder in Power Cycling

In PC tests with $\Delta T_J<100K$ the substrate solder typically shows no significant fatigue. Only in rare cases, a beginning delamination at the corners of the substrate solder is found as shown in fig. 1. The EOL, however, is caused here by damaged chip solder leading to a substantially increased thermal resistance and bond wire lift offs. The amount of delamination of the substrate solder is not limiting the lifetime because there is no increased thermal resistance due to substrate solder fatigue.

3. Temperature distribution and data assessment

The temperature is non-uniform in the module during the PC test. The temperature distribution inside the module can be calculated via the thermal impedance formalism. The thermal impedance Z_{th} for the specific regions in the module and at the base plate can either be measured by IR thermography or calculated (via finite element methods) [7,8]. The first method allows the knowledge of temperatures at the surface of the opened module only whereas the second also gives access to temperatures in inner layers, e.g. solder layers.

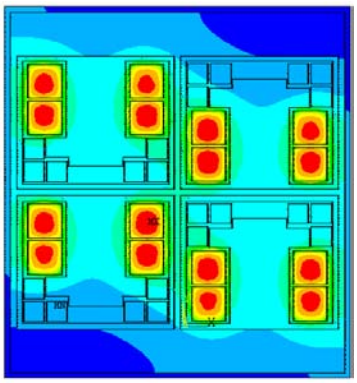

Fig. 2. Temperature distribution in an IGBT module with powered IGBT dies. The color plot ranges from blue (cold) to red (hot).

Fig. 2 shows an example of the static temperature distribution within an IGBT module when all IGBT dies are powered equally. The non-uniformity of the temperatures is clearly visible, especially between the die locations and the corners of the substrates.

The finite element calculations need a proper calibration of the cooling environment, namely the thermal impedance behavior of the heat sink. This is performed by fitting free parameters like thickness of grease in the simulation to impedance curves favorably measured with IR thermography.

Having the thermal impedance curves allows for the calculation of the temperatures according to the load profile applied in the PC test. The Z_{th} curves are calculated as the temperature response of the regions-of-interest (ROI) to a step-like power pulse P_0 in the dies.

$$Z_{th} = \frac{T_{ROI}(t) - T_{ambient}}{P_0} \qquad (1)$$

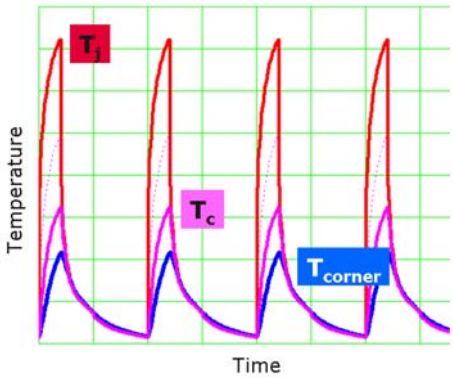

Fig. 3. A load profile (power pulses) in the dies gives rise of temperature inside a module monitored at the junction (T_j), the case below the chips (T_c) and at the corner in the substrate solder layer (T_{corner}).

The convolution of the Z_{th} curves with the load profile $P(t)$ directly give the transient temperature response at ROI.

$$T_{ROI}(t) = \int_{-\infty}^{t} d\tau \cdot \dot{Z}_{th}(t-\tau) \cdot P(\tau) \qquad (2)$$

Fig. 3 exemplarily shows a temperature profile of a PC test monitored at different places inside the module.

The temperature swing in the solder corners is lower than that at the case below the chip positions. However, cracks in the solder start at the corners.

4. Extended life time curve and discussion

It is known from experiments or simulations how much delamination in the substrate solder corresponds to the EOL criterion of a R_{th}-increase by 20% [3,4]. A scaling factor S is defined comparing the EOL crack length L (or delaminated area) from the thermal cycling tests with that from the PC experiments under investigation. The lifetime from thermal cycling, $N_{TC,EOL}$, is related to the cycle number in the power cycling via S accordingly (eq. 2), i.e. if the delamination of the substrate solder had been limiting the EOL the module could withstand a five times higher cycle number.

$$S = L_{PC} / L_{TC,EOL} = N_{PC} / N_{TC,EOL} \approx 1/5 \qquad (2)$$

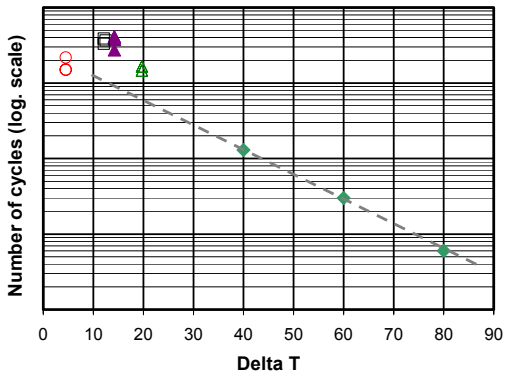

Fig. 4. Lifetime curve for module with copper base plate extended towards low temperature swings by data from power cycling. The *Delta T* refers to the case temperature swing ΔT_C for the thermal cycling data and ΔT_{Corner} for the power cycling data. The temperature swing at the corner of the solder is used in case of PC data. ◆: original TC data; open symbols: PC data with no system solder delamination; ▲: PC data with beginning delamination. The dashed line is only a guide to the eye.

This procedure needs some induced delamination for "calibrating" the method. If there is no delamination at the end of the PC test then the scaling factor cannot be determined. The lifetime is considered as a lower boundary, i.e. the "real" lifetime for the substrate solder is much higher.

While applying this procedure an extension of the lifetime curves for small temperature swings is possible. Fig. 4 shows the results. The data

sets with open symbols correspond to the modules where the EOL in PC was reached, but no signs for a substrate solder delamination were visible. Therefore, these data are considered as a lower lifetime boundary. Only one sample set showed beginnings of delamination (full triangle).

The data show a larger lifetime than expected from an extrapolation of the thermal cycling data in fig. 4. However, a power law (Coffin-Manson approach) is better suited for describing the lifetime as long as dealing with solder materials:

$$N = C_1 \cdot (\Delta T_C)^{C_2} \quad (3)$$

Fig. 5 shows the data from fig. 4 in a double-logarithmic plot considering the power law behavior. Note, the original temperature swing of the PC data evaluated is taken at the solder corners.

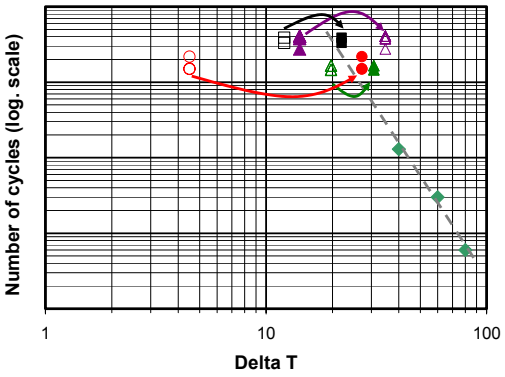

Fig. 5. Data from fig. 4 plotted double-logarithmically. The PC data are shifted in the temperature scale taking into account the temperature swing measured at the case of the module directly below the chip positions. ◆: original TC data; □,○,△,▲: from fig. 4, temperature swing taken at corner of solder layer ΔT_{Corner}. ■,●,▲,△: data moved with respect to temperature swing at case T_C.

The data sets are shifted with respect to the temperature excursion measured at the case of the module directly below the hottest chips. This point is the reference for $R_{th,JC}$ and $Z_{th,JC}$ in the data sheets. This reference temperature is accessible in experiments as well as in thermal calculations based on the Z_{th} characteristics for e.g. mission profile simulations or inverter dimensioning.

The experimental data from the PC test suggest that the substrate solder at low temperature swings behaves as expected from a power law extrapolation of the passive thermal cycling data gathered at higher temperature excursions.

One drawback of the method is the error in the ΔT_C determination. It depends on the modeling of not only the module but also on the cooling environment. An error in the determination of ΔT<5K seems to be realistic.

Another obstacle is the fact of scaling the EOL cycle numbers onto each other. As explained before, the PC shows substrate solder damage only in a few cases. When comparing to other tests the actual crack length depends on the solder thickness and other influences which might vary between the samples.

In the discussion of the accelerated lifetime tests only ΔT_C is discussed. Dwell times and ramp rates are not considered in detail here.

5. Summary and Conclusion

The paper studies the behavior of the substrate solder under power cycling conditions. The experimental focus was on IGBT modules with copper base plates. The non-uniform temperature distribution in PC is – beside of cycle times – the major difference to the passive thermal cycling test.

Using simulated thermal impedance curves access to the inner temperature distribution of the module is possible. This allows for the determination of the temperature swing of any part in the module during the power cycling.

The PC data are utilized to assess the lifetime of the substrate solder. From the experimental point of view it seems that the life time of the system solder can be described by a power law extrapolation of the thermal cycling test data down to small temperature swings.

6. Literature

[1] T. Schütze, H. Berg and M. Hierholzer: Ind. Appl. Conf., IEEE, 1998
[2] T. Herrmann et. al.: Proc. EPE 2007
[3] K. Guth and P. Mahnke: Proc. CIPS 2006
[4] J.-P. Sommer et al.: Proc. CIPS 2006
[5] R. Bayerer et al.: Proc. CIPS 2008
[6] M. Thoben et al.: Proc. PCIM Europe 2008
[7] T. Hunger and O. Schilling: Proc. PCIM Europe 2008
[8] W. Brekel et al.: to be published in Proc. PCIM Europe 2009