IGBT power modules utilizing new 650V IGBT[3] and Emitter Controlled Diode[3] chips for three level converter

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Abstract

Recently the three level **N**eutral-**P**oint-**C**lamped topology (NPC) known from high power applications is also applied in low and medium power applications to exploit specific advantages in system level design. Applications requiring filters, like UPS systems or PV inverters benefit from improved spectral performance and lower specific switching loss of lower voltage class devices. Up to now setting up a three level phase leg has only been possible by applying discrete devices or combining at least three modules. By integrating a three level phase leg into a single module, adapting chip technology for slightly higher breakdown voltage and providing a simple solution for driving this topology becomes more appealing for new projects.

1. Introduction to three level NPC inverters

The three level Neutral-Point-Clamped inverter has been first presented by Nabae et al. in 1981 [1] using bipolar power transistors. Later this topology was successfully applied in designing inverters for traction applications operating from 750 V DC and industrial inverters connected to the 690 V AC mains before 1700 V IGBTs became available [2], [3], [4]. Today this topology is used in many designs of variable speed drives operating on medium voltage and using GTOs, IGCTs or high voltage IGBTs [5], [6]. In the aforementioned applications the three level topology has been chosen because either the voltage rating or the power rating exceeds the level that could be covered by standard two level topology without series connection of devices. Compared to the two level topology with series connection the three level approach here provides improved spectral performance at little additional expenses. But there are also recent designs applying the topology to a general purpose drive connected to the low voltage mains [7], an application that easily can be covered by the standard topology. Here the three-level design is favored because it reduces the stress that the inverter causes to machine windings and bearings. Other low voltage/low power applications where three level inverters are considered today are transformerless UPS systems and PV inverters [8], [9]. While in a drives application the inductance for smoothing the output current is provided for free by the machine these applications need dedicated filters. Three level topology allows to reduce the size and the cost of the filter by better spectral performance of the output voltage and the option to increase the switching frequency without too much penalty in switching loss. Typical range of switching frequency targeted to achieve these benefits is 16 to 30 kHz.

Typical issues to deal with when designing three level converters are the complex loss calculation [10], [11] and ensuring voltage balance on the DC-link [12]. When three level inverters are built using dual modules or single switch modules it is difficult to keep the commutating inductance within reasonable limits for both relevant commutation loops. The resulting complexity of the mechanical structure of the DC-link is a significant challenge [3], [11].

When three level topology is adapted to low power applications one important economic requirement is to keep the control and driving effort low and to consider some specific requirements for protection. Up to now these topics have only been sparsely covered in literature.

2. Power Section

2.1. Commutation Loops in a Three Level Phase Leg

The three level phase leg in NPC topology consists of four IGBTs with its associated anti-parallel diodes, all arranged in series, and two additional diodes D_H and D_L connecting intermediate nodes to the neutral point of the DC-link. All power semiconductors used exhibit the same blocking voltage, which is usually below the maximum value of DC-link voltage. Depending on sign of output voltage and current, four different commutation loops are in operation during one period of the output base frequency. With voltage and current in positive direction T_1 and D_H operate like a buck chopper whereas T_2 just conducts the output current without switching as shown in Fig. 1a). For voltage and current being both negative T_4 and D_B operate like a boost chopper with T_3 just conducting the current. For these conditions only two devices are within the commutation loop and this will be referred to as short commutation. But with the output current being negative combined with positive voltage, current flowing through T_3 and D_B has to commutate to D_2 and D_1 as shown in Fig. 1b). This commutation involves four devices and will be designated as long commutation. For the remaining case another path of long commutation exists. Managing stray inductances and overvoltages for the long commutation is one of the demanding tasks when designing three-level converters.

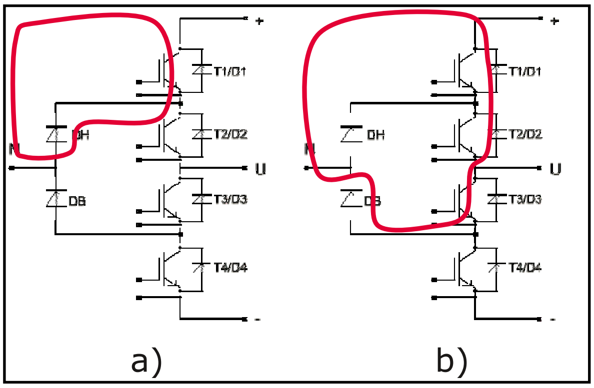

Fig. 1. Commutation loops in a three level phase leg

When using standard IGBT modules, e.g. chopper modules and halfbridge modules as shown in Fig. 2, the long commutation, involves devices located in two different modules.

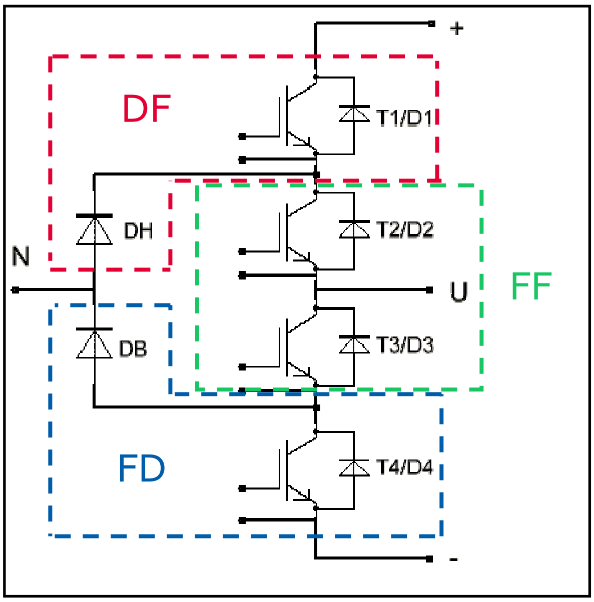

Fig. 2. Set up of a three level phase leg using standard modules

With such a setup, the inductance in the long commutation loop is expected to be significantly higher than in the short loop or within a two level inverter phase leg.

2.2. IGBT Module for Three Level Converters

While integrating in total four IGBTs and six diodes is not an option for high power applications, this is feasible in the low power and medium power range as long as number of available power and control pins does permit the use of a standard package.

For the low power range, the EasyPACK 2B package as shown in Fig. 3 offers sufficient DBC area to integrate a complete 150 A three level phase leg. Due to the facts that pins can be placed freely within the given grid and the pins can be assigned to provide either a power or a control function, suitable interconnection means are provided. There are auxiliary emitter terminals available to enable fast switching. For power terminals up to eight pins are used in parallel to achieve the required current rating as well as to minimize stray inductance and PCB heating.

Fig. 3. EasyPACK 2B package

For the medium power range, where typically screw connections are used for the load terminals, none of the established standard packages is able to provide the required number of four terminals. However the new EconoPACK™ 4 package as shown in Fig. 4, mainly intended to house the sixpack 3-phase full bridge configuration, can also be used to accommodate a three-level phase leg.

Fig. 4. EconoPACK™ 4 package

The three terminals usually employed as output terminals are used to enable a low inductance connection to a split DC-link as it is needed for three level converters, whereas the two terminals on the opposite side are used in parallel as output terminals. A driver PCB is to be connected directly to the control terminals visible at the edge of the module frame. This package is intended to be used for three level phase legs with chip currents up to 300 A.

2.3. New 650V IGBT^3 and Emitter Controlled Diode^3 Chip

Integrating all devices of a three level phase leg into one module is very promising in regard to minimizing stray inductance, but with only 600 V of blocking voltage it is still very difficult to meet typical application requirements of applications usually served by 1200 V IGBTs in two level topology. This stems from two issues:

- Non-perfect balance of DC-link voltages
- Faster switching of 600 V devices

Even if appropriate control of DC-link voltages is employed there will always be a dynamic imbalance between positive and negative section of the DC-link. On the other hand, as the three level topology is being chosen to benefit from the lower specific switching loss of lower voltage class devices, it has to be considered that this can only be fully exploited with accepting higher di/dt at turn-off. Considering this the three level phase leg modules, that have been presented here are equipped with enhanced IGBT and diode chips that exhibit a higher blocking voltage of 650 V without concession in regard to conduction and switching losses compared to the well know 600 V IGBT3 devices. Also the softness and robustness of both devices (SOA, RBSOA, SCSOA) stays unchanged. This is enabled by the development of new termination structures for IGBT and diode, the ultra thin thickness of 70µm is not changed.
Therefore V_{CESat} of the IGBT stays at its excellent value of 1.45V (1.70V) at 25°C (150°C) [13] with low switching losses that contribute only 1/3 of the total inverter losses for switching frequencies of 16kHz. Also the IGBT still has its smooth current tail that even at critical conditions shows no snap-off [14].

The diode also stays at the optimized V_F-Q_{rr} trade-off at 1.55V (1.45V) at 25°C (150°C) [13] and its soft switching behavior.

3. Driver Section

3.1. Specific Driver requirements

The application of three level NPC topology in low and medium power applications creates some specific driver requirements that have to be considered for optimum system performance. Partially these requirement stem just from the intended high switching frequency that was the motivation to use three level topology, partially they stem from the topology itself.

Arising from high Switching Frequency

The following requirement originates just from the increase in switching frequency:

- Due to switching frequencies covering a range form 16 kHz to 30 kHz the driver has to provide small and consistent propagation delay so that the deadtime can be minimized. Considering the fast switching times of 650 V devices the main contribution to deadtime requirement arises from variation in driver propagation delay [15]. If deadtime is too large compared to the period of the switching frequency this will lead to nonlinear behavior of the inverter stage creating new challenges in control algorithm[16], [17].

Arising from topology

These requirements are a consequence of the topology:

- Although the devices used only have a blocking voltage of 600 V or 650 V the isolation requirements for the driver are similar to a 1200 V application
- Since the number of driver circuits doubles, it is mandatory to use a design for the driver and it's power supply with low part count and low board space requirement.
- Protection features like short circuit detection and turn off have to match with three level NPC topology. Turning off an inner IGBT first (T2, T3 in Fig 1) would expose this device to the full DC-link voltage and lead to immediate device failure due to SCSOA or RBSOA violation.

With the new integrated IGBT drivers of the *EiceDRIVER*™ family these requirements can be met without big effort [18], [19]:

- The integrated microtransformer provides basic isolation up to a repetitive isolation voltage of 1420 V_{peak}.
- With the integrated Active Miller Clamp feature this driver can be used with a single supply at high switching speed without the risk of parasitic turn on [20].
- Compared to typical optocoupler based drivers tolerances and variation of propagation delay are significantly reduced by the microtransformer technology.
- The integrated Vcesat-protection may be used for the outer switches, but has to be disabled for the inner IGBTs.

4. Test Setup and Results

4.1. Power Section

For the test setup an Easy2B three level module with a current rating of 150 A has been placed on a double layer PCB of 2.4 mm thickness and connected to a DC-link consisting of a single 1000 µF electrolytic capacitor. A current transformer is placed in positive DC-link connection as well as in the negative DC-link connection.

4.2. Driver

The four driver stages are placed on the same PCB that carries the power section. Each driver consists of a 1ED020I12-F driver IC supported by a small bipolar booster stage housed in a single SOT23-6 to provide gate currents up to 5 A. Isolated power supply of 16 V to each driver is provided externally. The Clamp-pin of the 1ED020I12-F is connected directly to the gate to avoid parasitic turn-on. Fig. 5 shows the schematic of a driver for one of the inner switches (T2/T3).

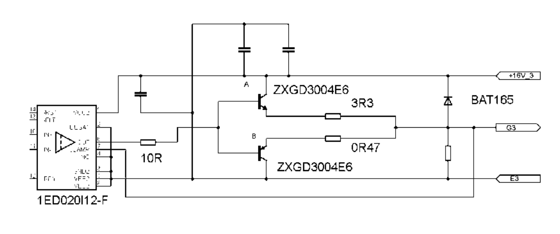

Fig. 5. Driver for inner switch

Desat-detection has been disabled here to avoid wrong turn-off sequence in case of a short circuit. For the outer switches Desat-detection is enabled and this will be sufficient to provide short circuit protection for faults to other phases external to the module. Furthermore the outer drivers supply voltage is reduced slightly by an additional series diode. This will avoid wrong turn off sequence in case of an undervoltage failure of the driver supply voltage.

4.3. Short Commutation

Fig. 5 shows the switching waveforms of a short commutation at nominal current, a voltage of 400 V and 25°C junction temperature.

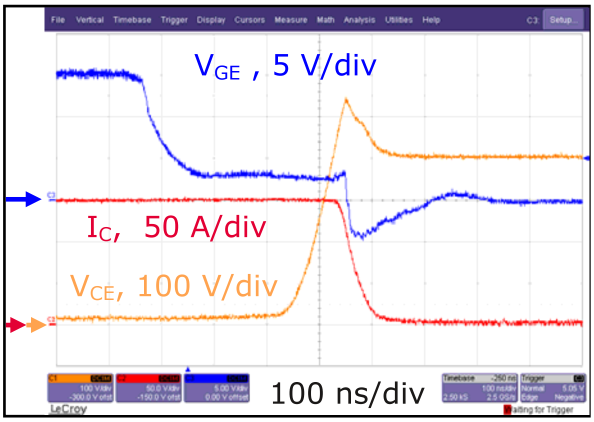

Fig. 6. Switching waveforms of a short commutation

With a peak value of 550 V the voltage stays well within limits.

4.4. Long Commutation

Fig. 6 shows the switching waveforms of a long commutation at the same conditions.

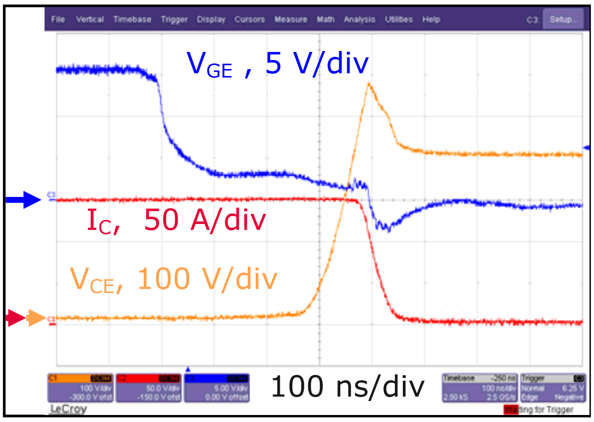

Fig. 7. Switching waveforms of a long commuation

With a voltage peak of 580 V this voltage is only about 30 V higher than for the short commutation and still fairly below the 650 V breakdown voltage.

4.5. Comparison and Outlook

First measurement results show that due to integration of a complete three-level phase leg into a single module switching behavior nearly similar to the short commutation can be achieved for the long commutation. However, to achieve enough headroom to switch at higher currents a further reduction of circuit stray inductance would be necessary. This can be achieved easily by using several capacitors in parallel and using a multilayer board reducing the spacing between the coplanar power layers connecting module and capacitors. Furthermore it has to be considered that a real application circuit would not contain current transformers within the DC-link connections. The current transformers used here contribute to stray inductance with 15 nH, increasing the overvoltage by 45 V.

5. Conclusion

With integrating a complete phase leg into one single module, increasing blocking voltage from 600 V to 650 V and providing a highly integrated driver solution the three level inverter proofs to be an attractive candidate for low and medium power low voltage applications requiring high switching frequency, filtering and high efficiency like double conversion UPS and PV inverters.

6. Literature

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