6.5kV IGBT and FWD with Trench and VLD Technology for reduced Losses and high dynamic Ruggedness

Thomas Duetemeyer\(^1\), Josef-Georg Bauer\(^2\), Elmar Falck\(^2\), Carsten Schaeffer\(^3\), G. Schmidt\(^3\), Burkhard Stemmer\(^1\),

\(^1\) Infineon Technologies AG, Max-Planck-Straße 5, D-59581 Warstein Germany
\(^2\) Infineon Technologies AG, Am Campeon 1-12, D-85579 Neubiberg, Germany
\(^3\) Infineon Technologies AG, Siemensstr. 2, A-9500 Villach, Austria

Abstract

Potentials offered by introducing trench technology into the 6.5kV voltage regime are investigated. In addition a VLD edge termination is presented with significantly reduced termination width compared to a field plate termination design. Both technologies result in significantly reduced on state losses and dynamic losses. At the same time improved robustness and a soft switching behaviour of the IGBT and diode are achieved. The surge current integral \(I^2t\) of the diode can be extended more than a factor of two and excellent rugged short circuit behaviour of the IGBT is proven.

1 Introduction

The availability of 6.5kV IGBTs makes it possible to reduce the complexity of inverter designs that had to be built with 3.3kV modules or GTOs in former times, thus resulting in lower system costs and better reliability. The market has an increased demand for 6.5kV modules with higher current rating to avoid or reduce the necessity of paralleling modules in the application.

Inverters in industrial and traction applications in the upper voltage regime are typically characterized by comparatively low switching frequencies in the range below 1 kHz. Therefore the contribution of on state losses plays the dominant role. To reduce the on state and switching losses of IGBTs in traction applications the trench concept has successfully been introduced for 1.7kV and 3.3kV modules. This is now supplemented by a 6.5kV module with trench concept for the IGBTs. The implementation of VLD edge termination structure\(^1\) with low reverse current behaviour allows an additional increase of the active chip area for IGBT and diode chips.

Further important aspects concerning application in the high power regime are very strong requirements as far as device ruggedness is concerned. Special care in device optimisation is taken with respect to surge current and switching ruggedness.

2 Static Characteristics IGBT & Diode

2.1 Static Characteristic Diode

In Fig. 1 it is shown that due to improvement of the vertical design and the smaller edge termination very low on state losses of the optimized diode have been achieved.

![Fig. 1 On state voltages of optimized 3rd generation diode for RT and +125°C. The inset shows \(V_F\) of emitter controlled (EC) diodes of 2nd versus 3rd generation at \(T_{j}=125°C\)](image)

The forward voltage of the diode shows a positive temperature coefficient for currents higher than 1.2 times the rated current. Compared to the state of the art diode the forward voltage at rated current is reduced by more than 25% while at the same time the rated current is increased by 25% without changing the outer chip dimensions.

2.2 Static Characteristic IGBT

The combination of the smaller VLD edge termination system with larger active area and trench concept in the new IGBT result in significantly reduced on state losses. As shown in Fig. 2 the forward voltage is reduced more than 30% at 125°C temperature in comparison to the planar 6.5kV IGBT. The achieved positive temperature coefficient over the whole current range eases the paralleling of chips and modules.
3 VLD Termination System for IGBT and Diode

As a further improvement a narrow VLD (variation of lateral doping) edge structure is implemented in place of the current p ring field plate termination system (pFP). A sketch of the structure is presented in Fig. 3.

![Schematic cross section of diode with the VLD termination system](image)

Linked to the p-emitter of the anode is a p⁺ zone with decreasing doping concentration towards the outside of the chip. With an optimized doping gradient the edge termination is about 25% smaller compared to a pFP termination while reducing the maximum electrical field strength. With an improved VLD profile a high breakdown voltage over a wide temperature range can be realized as shown in Fig. 4.

![Module reverse-blocking current versus 1/T for pFP (p ring field plate termination system) and VLD termination system (24 IGBT and 12 diode chips in parallel)](image)

The reliability of the termination structure is successfully proven with passed 1000h high temperature reverse bias (HTRB) and high temperature, humidity and voltage tests (H3TRB).

4 Dynamic Characteristics under nominal conditions

4.1 Softness and Switching Energies

Fig. 6 shows the turn off waveforms of a 6.5kV/750A module at rated current I_C= 750A at V_CE= 4.5kV for -40°C, room temperature (RT) and +125°C.

![Turn-off waveforms of a 6.5kV/750A trench IGBT3 module for V_CE=4.5kV, I_C=750A, L_c=280nH at -40°C, 25°C and 125°C temperature](image)
It can be seen that soft switching behaviour is achieved over the whole temperature range even at that high voltage level. The increase of switching losses between 25° and 125°C as plotted in Fig. 8 is mainly caused by the evolution of the tail current. Even at lower temperatures the dIC/dt is still low enough to ensure that VCE,max stays in the same regime like at 125°C. Soft switching behaviour is also observed for the diode with improved vertical structure.

Fig. 7 Diode recovery waveform of a 6.5kV/750A trench IGBT3 module at room temperature. IC=750A, VCE=3.6kV, Lσ=280nH

4.2 Switching Losses

The trade off optimization of the emitter controlled diode and the trench IGBT is already described in an earlier publication1. In the following the switching losses in dependency of the driving condition will be presented. All values are given for a 6.5kV/750A module with 24 IGBT and 12 diode chips in parallel. All measurements are performed with a stray inductance Lσ of 280nH.

4.2.1 Turn-Off Losses (Eoff) IGBT

The turn-off losses of the new 6.5kV/750A module are given in Fig. 8. A dVCE/dt of 2.5kV/µs which is common for traction applications results in losses of about 3.8 mJ. The losses per amp are 20% lower than for the state of the art planar IGBT2. A further significant reduction of the turn-off losses can be achieved by increasing dVCE/dt up 5 kV/µs.

4.2.2 Turn-On Losses (Eon) IGBT and Recovery Losses Diode (Erec)

The dependency of turn-on and recovery losses against current slope for the new 6.5kV/750A trench IGBT3 module is plotted in Fig. 9. For a typical dIC/dt of 3 kA/µs the losses per amp are about 10% lower than for the current 6.5kV/600A planar IGBT2 module.

At the same time the level of recovery losses rises, but is still on a low level. These increased losses are well overcompensated by the reduced on state losses of the diode. As will be later shown the thermal limitation of the module is still caused by the IGBT chip losses if a realistic inverter operation is regarded.

4.3 IGBT Turn Off at varying driving conditions

Fig. 10 shows the dependency dVCE/dt=f(RGoff) for a 750A/6.5kV IGBT3 module if a resistive driver is applied and VGE switches from +15V to -15V. Depending on IC there is a regime in which dVCE/dt doesn’t depend on RGoff and a 2nd regime in which dVCE/dt decreases with rising RGoff. The behaviour is also observed in other HV IGBT3 specimen e.g. in the 3.3kV voltage class2. An explanation for the dVCE/dt self limiting behaviour, that is observed for IGBT3 technology under certain operation conditions can be given as follows: In order to enable VCE to rise at a defined slope, a space charge region has to build up in the base region. The driving force for the extraction of charge carriers which is necessary for the formation of the depletion zone is the collector current IC itself. Thus the reachable dVCE/dt becomes small if a low current far below the rated current
is turned off and vice versa. Consequently for small currents a regime is observed, in which \( \frac{dV_{CE}}{dt} \) doesn’t depend on \( R_{Goff} \). In principle this effect should be observable for all IGBTs with very high on-state charge carrier concentration at the emitter side pn junction (e.g. IGBT3) because for these class of devices the rate by which the depletion zone can form is effectively impeded by the presence of the excessive carrier concentration close to the pn junction.

Once the field stop layer is reached the further charging of the collector-emitter capacity happens almost without requiring the depletion zone to extend deeper which leads to the observed high \( \frac{dV_{CE}}{dt} \). This high \( \frac{dV_{CE}}{dt} \) is completely harmless because it doesn’t lead to critical field strength in the chip.

5 Switching under extreme conditions

5.1 Short Circuit

Fig. 12 shows the short circuit waveforms at 125°C temperature of 750A IGBT3 module. The short circuit is limited to less than 7 times the nominal current. The short circuit is proven to be free from \( V_{CE} \) and \( I_{C} \) oscillations in the full operation voltage range of 1000V to 4500V and the temperature range of -40°C to +125°C using a gate-emitter voltage clamping of 17V. As shown in Fig. 12 tests are performed with a pulse time of 14µs giving an additional safety limit to the spec limit of 10µs.

5.2 IGBT Dynamic Robustness /RBSOA IGBT

Previous investigations\(^3,4\) addressed techniques in order to improve the robustness of the planar 6.5kV IGBT. The extraordinary robustness of the IGBT3 is visible in Fig. 13. It shows the turn-off waveform for \( I_{C}=2250A \) which corresponds to 3 times rated current at \( V_{CE}=4.5kV \). Fig. 13 proves that the turn-off is passed successfully 50% above the specified limit. RBSOA tests are performed under a variety of boundary conditions. It can be concluded that excellent device ruggedness is observed in an extended temperature range (-50°C...+125°C), a wide range of operation voltages (up to 4.5kV) and high stray inductance.
5.3 IGBT Dynamic Self Clamping

Dependent on how the IGBT is controlled by the driver a dynamic self clamping is seen for switching off high currents with a high stray inductance. Measurements are performed with a 500A/6.5kV module with 16 IGBT\(^3\) chips in parallel.

![Fig. 13 Turn-off waveform for 3 times I\(_{\text{Nom}}\) (I\(_c\)=2250A) for IGBT3. V\(_{\text{CE}}\)=4.5kV, L\(_o\)=280nH, T\(_{vj}\)=RT](image)

5.4 Diode Robustness/SOA Diode

The decisive parameter for diode robustness is the maximum power P\(_{\text{max}}\) during switch off. The optimization of the carrier profile of the diode and the improved ruggedness of the termination structure leads to a substantial increase of P\(_{\text{max}}\). P\(_{\text{max}}\) values of more than 4 MW for a unit rated at 250 A (4 diodes in parallel) have been reached without destruction.

![Fig. 15 Diode recovery waveform of a 6.5kV/250A module. I\(_c\)=250A, V\(_{\text{CE}}\)=4.5kV, T\(_{vj}\)=125°C, P\(_{\text{max}}\)=4.5MW](image)

The high safety margin allows turn-on of the IGBT with high dI\(_c\)/dt without exceeding the allowed P\(_{\text{max}}\) of the diode. This is a necessary prerequisite to minimize the total switching energies as depicted in Fig. 9.

5.5 Surge Current

In fault conditions of inverter applications high surge currents can occur at the diode. The ability to withstand these high currents is an important criterion for the usability of the module.

![Fig. 16 On state losses of state of the art diode compared to optimized diode up to 10 times nominal current for same chip size in an ensemble of 12 parallel chips at T\(_{vj}\)=125°C](image)
In Fig. 16 the forward characteristic of the new diode with improved vertical design is compared to the state of the art diode to about 10 times the rated current of a module. That current regime is relevant for surge current limitation. It can be seen that the voltage drop is reduced by more than 30% over the presented regime. This reduction directly corresponds to a better surge current capability.

Furthermore the surge capability benefits from the small VLD edge termination which enlarges the active chip area and at the same time reduces the Rth value without changing the outer chip dimension.

Fig. 17 proves the dramatic improvement in surge current capability that can be reached by an optimized vertical design and application of the VLD concept. The strongly reduced on state voltage leads to beyond 40% higher IFSM (forward surge current maximum) values corresponding to more than a two times increased I^2t value.

**6 Simulation of Inverter Output Current**

Fig. 18 shows the calculated maximum achievable output current using thermal calculations. The simulations were performed with maximum allowed Tvj of 125°C, Ta=40°C and a water-cooled heat sink. The RMS output current is given as a function of the switching frequency for the conventional 600A module with planar IGBT in comparison to the new 750A module with trench IGBT. Both modules are of the same housing size and footprint.

As can be seen the inverter output current is limited by the IGBT chip losses in both case. Therefore the improvement of the maximum output current for the whole module is given by the ratio of the respective maximum output currents for the IGBT chips.

**Fig. 18** Inverter output current RMS versus PWM frequency by a thermal calculation for 6.5kV modules using planar and trench IGBT. cos φ=+0.85 (IGBT) and -0.85 (diode), VCE=3.6kV, f_o=50Hz, Rth(H-A)=6°K/kW

The improvement achieved is bigger than 20% for very high switching frequencies and more than 30% in the lower frequency regime. The usability at low frequencies is of major importance in traction applications.

**7 Conclusion**

It is shown that by using trench technology and VLD termination structure the switching robustness can be increased substantially whereas dynamic and on state losses are considerably reduced. The reliability is furthermore enhanced due to the improvements in short circuit behaviour and the higher surge current capability.

**8 Literature**


