Overview of Level 3 power FET PSpice simulation models

Applicable to SIMetrix and Cadence OrCAD Capture

About this document

Scope and purpose

This application note presents International Rectifier (IR HiRel)'s Level 3 PSpice simulation models for the following IR HiRel discrete product groups:

- Radiation hardened (RH) R8 and R9 power MOSFETs
- RH GaN HEMTs (RG1)
- Radiation tolerant (RT) power MOSFETs

These models have been optimized for SIMetrix and Cadence OrCAD Capture simulator platforms. Several R9 MOSFETs will be used as an example to highlight new features and example applications.

Intended audience

This document targets application engineers and designers who wish to explore several product groups within IR HiRel's discrete product portfolio via simulation models that can emulate a typical electrical and thermal characteristics of these transistors. The goal of this document is to help guide the designer in understanding the capabilities of Level 3 power FET models.

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1 Introduction

Level 3 PSpice models offer a realistic representation of IR HiRel's power FETs through the integration of a thermal network and typical power FET electrical parameters within each model. These thermal networks offer engineers the opportunity to assess the dynamic behavior of a power FET's junction temperature (T_j) and case temperature (T_{case}) during real-time operation of power systems such as a buck converter. Several temperature-dependent electrical parameters such as drain-to-source on-resistance $R_{DS(ON)}$ are also designed to respond to fluctuations in T_j to better align the behavior of these power FET models with their physical counterparts.

2 PSpice model library files

These models for IR HiRel power transistors are intended to be evaluated with SIMetrix or Cadence OrCAD Capture PSpice simulators.

All IR HiRel Power transistor models are supported by benchtop measurement data and are constructed using PSpice simulation code. For SIMetrix, each IR HiRel Power transistor has a dedicated model library file (*.lib*) to support circuit simulation. A set of object library files (*.olb*) have been created to support Cadence OrCAD Capture.

Released Level 3 *.lib* and *.olb* files are available on the Infineon simulation model finder web page.

2.1 Integration of *.lib* files into SIMetrix

To design any circuit simulation that will incorporate IR HiRel power transistors, the necessary model library files must be installed into the simulator tool. This section details the necessary steps to install a PSpice *.lib* file into SIMetrix (using version 8.4, however these guidelines will be applicable for earlier software versions)[1].

The following images detail the process to install a new *.lib* file into the SIMetrix simulator.

1. Select a library file, then drag and drop the file into the program window **Command Shell**.

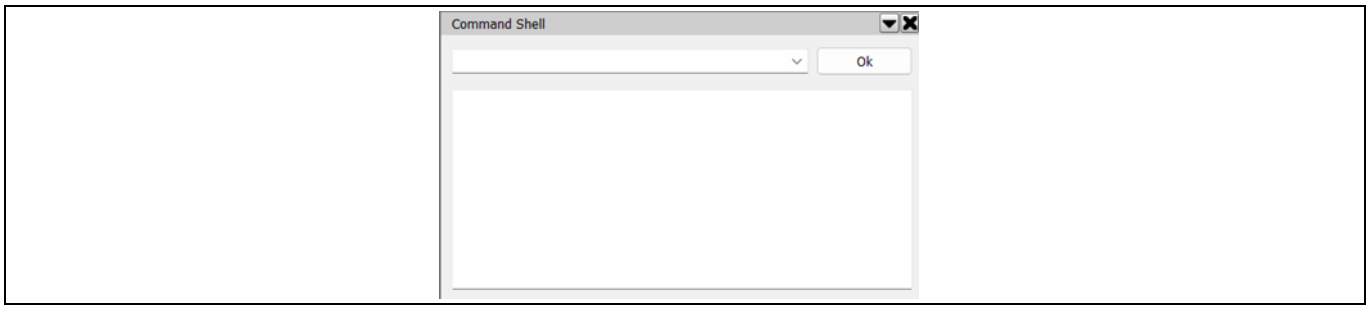

Figure 1 Drag and drop file into the command shell

2. Select **Install** and click **Ok** in the generated prompt and you will be notified if successful.

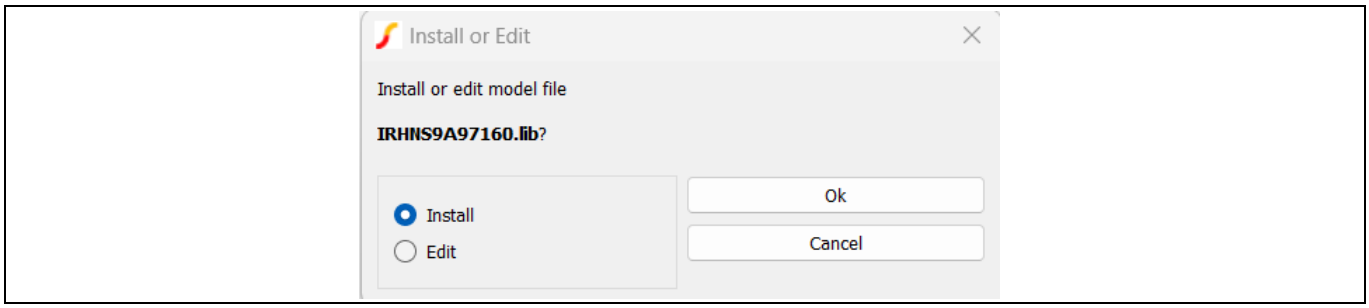

Figure 2 Select Install

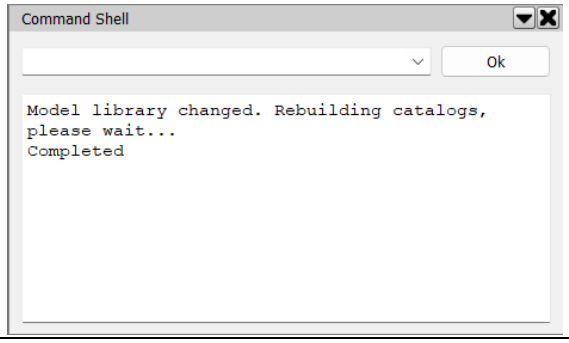

Figure 3 Model library changed successfully

3. Access **File**->**Associate Models and Symbols**.
4. Select the required *.lib* file in the **Unknown** category of devices.
5. Choose the category of device and pick a symbol definition. Level 3 models will be five terminals.
6. Select **Apply Changes** to confirm the symbol to library association and symbol definitions.

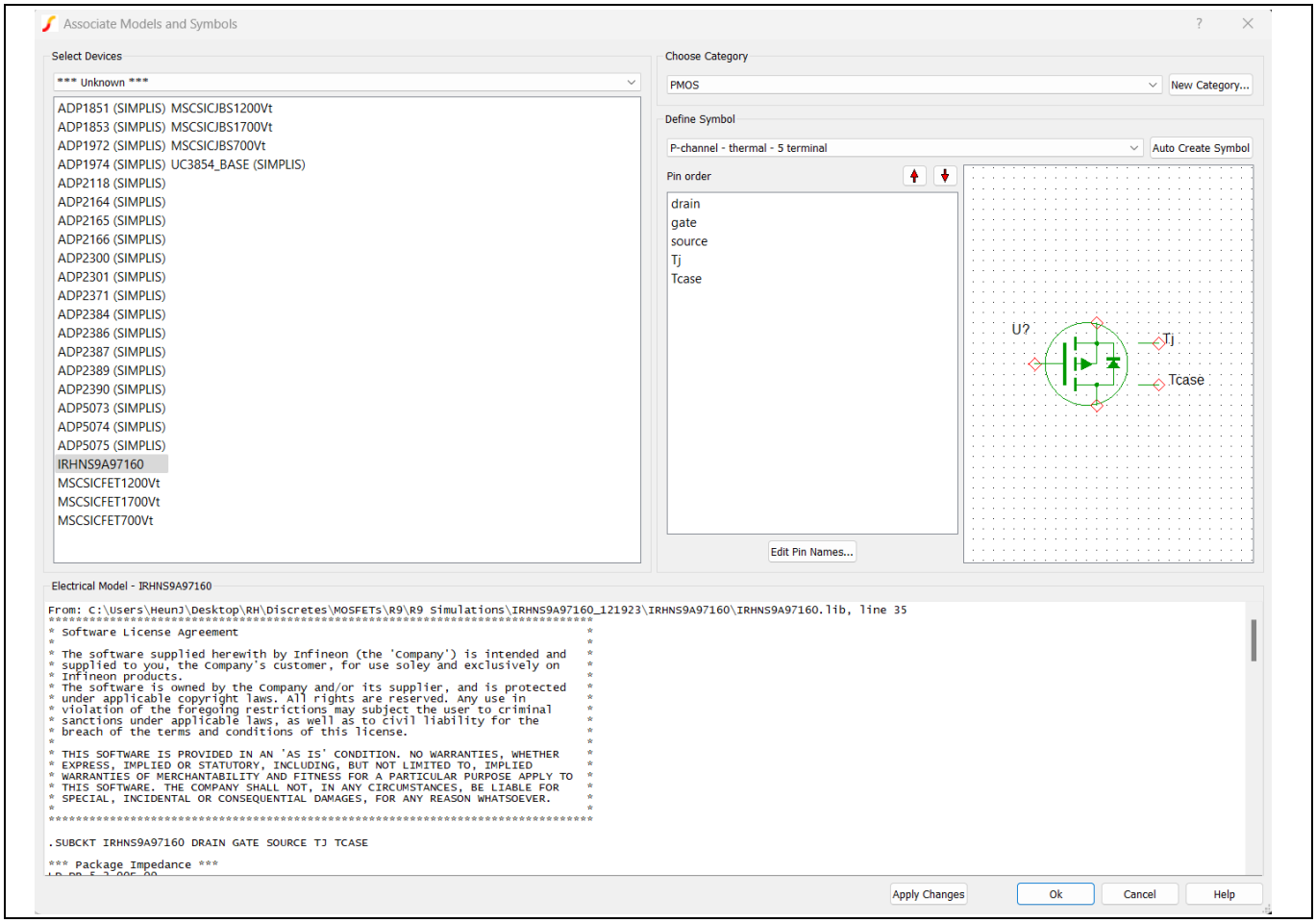

Figure 4 Process to associate PSpice library model to circuit symbol in SIMetrix

7. Select **Apply Changes** to confirm the symbol to library association and symbol definitions.

2.2 Integration of *.olb* files into Cadence OrCAD Capture

This section details the necessary steps to install a PSpice *.olb* file into Cadence OrCAD Capture (using version 22.1-2022, however these guidelines will be applicable for other software versions).

The following images detail a basic process to integrate a *.olb* file into the default library folder of a Cadence OrCAD Capture project.

1. Right-click on the library folder under **Design Resources** and select **Add file**.

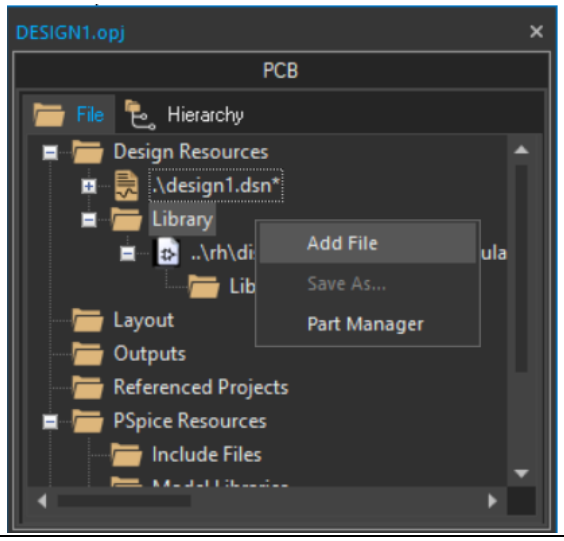

Figure 5 Add file from the library folder

2. Locate the desired *.olb* file in the local file path and select it to be integrated in the project's standard library.

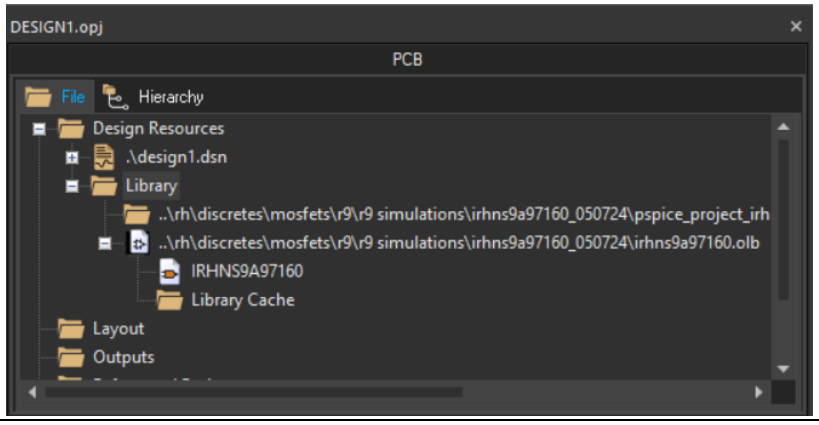

Figure 6 Select file to be integrated in the library

Once integrated, the part exists as a library that can be found in the **Part List** of the project and can now be used in a schematic.

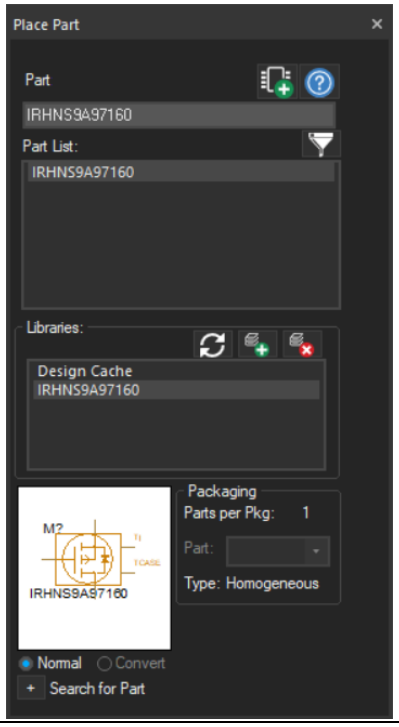

Figure 7 Part added to the library

3 Overview of Level 3 power FET PSpice models

3.1 Level 3 model pin description

Figure 8 shows the symbols that represent PSpice Level 3 models in SIMetrix for N-Channel and P-Channel power FETs, respectively. The additional two non-standard pins attached to the symbols are denoted as T_j and T_{case} to represent the device's junction temperature and case temperature respectively. Both temperature connections function as voltage pins where a measured voltage refers to temperature in a 1:1 conversion ratio (i.e. 25 V = 25°C). Typically, T_j is left open whereas T_{case} cannot be left floating. To directly control a model's T_j, set $T_{case} \leq -301$ V, and connect a voltage source to the T_j pin for it to operate at the desired T_j (see Figure 9).

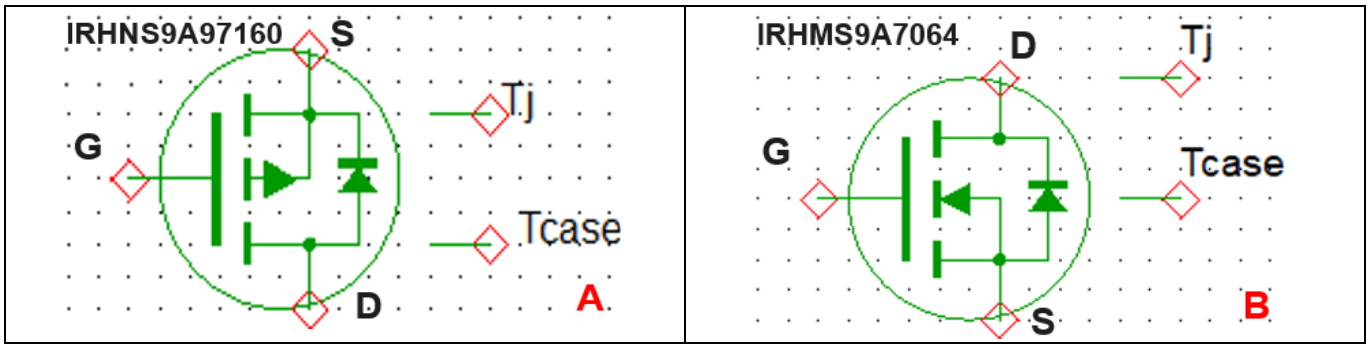

Figure 8 Level 3 power MOSFET circuit symbols in SIMetrix, (A): PMOS, (B): NMOS

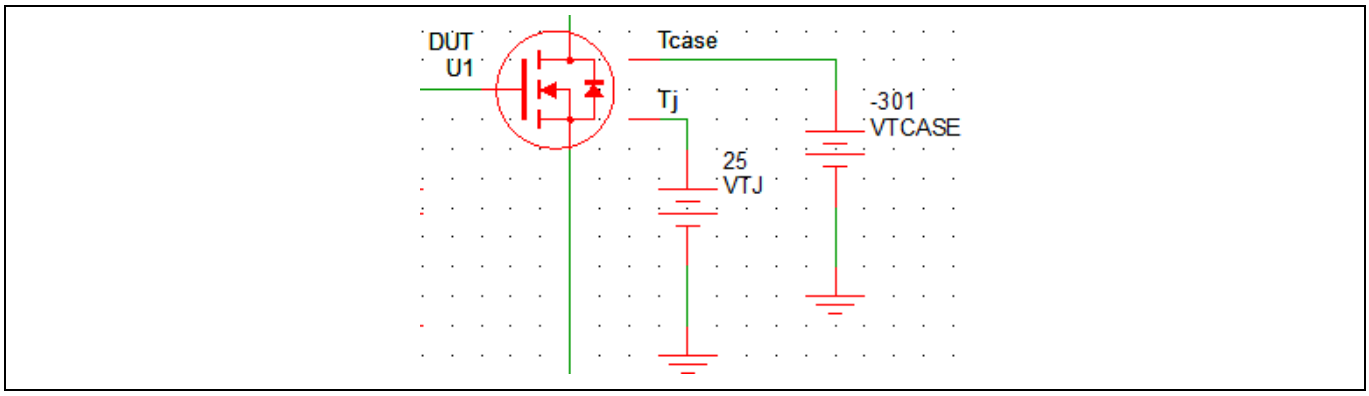

Figure 9 Direct control over T_j requires $T_{case} \leq -301$ V

3.2 Electro-thermal model description

To emulate dynamic self-heating and the subsequent shift in power FET electrical parameters, a Level 3 power FET contains a Cauer thermal network (generated from thermal impedance measurements of the part) coupled to the electrical model within the library file [2]. Dynamic self-heating is executed via Equation 1 where power dissipation is modeled as a current source that is fed into an appropriate Cauer network, (see Figure 10). The voltage measured at the T_j node represents the time-dependent junction temperature of the device that will subsequently influence temperature-sensitive electrical parameters.

$$T_j = T_c + Z_{thjc} * P_{diss}$$

Equation 1 Junction temperature (T_j) calculation from power dissipation (P_{diss}) and thermal impedance junction-to-case (Z_{thjc})

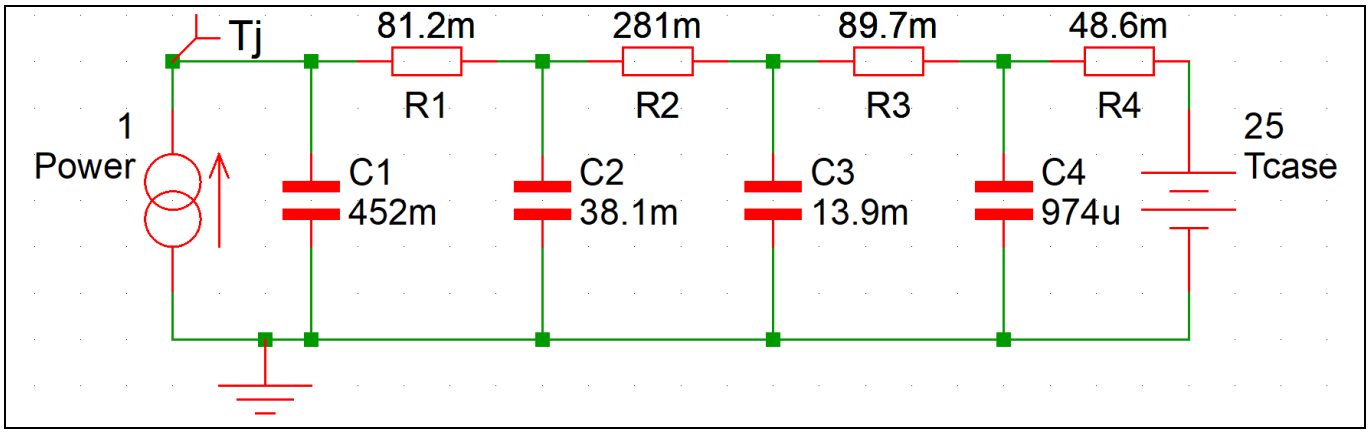

Figure 10 Example Cauer thermal network within IRHNS9A97160 library model

3.3 Implementation of an external heat sink

Figure 11 shows a heat sink (represented as a Cauer thermal network) connected to the model. The resistor components refer to the Z_{th} between the model case and the surrounding environment whereas the shunt capacitors represent thermal capacitance. The voltage source (V1) acts as the case temperature the device is subjected to.

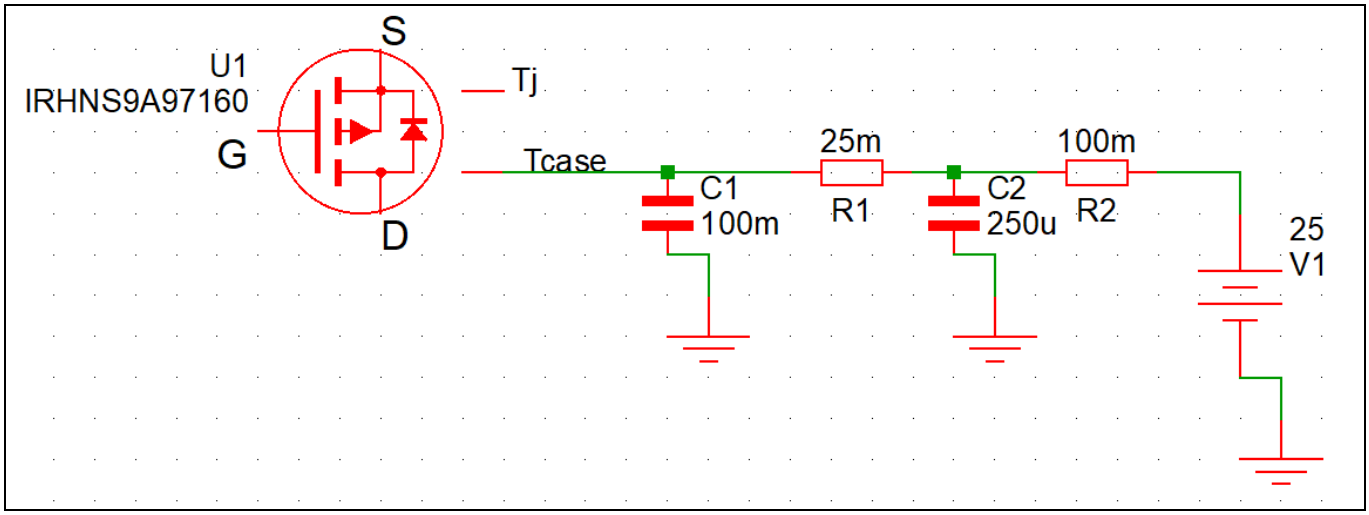

Figure 11 IRHNS9A97160 model attached to an external heat sink in a 25°C environment

4 Simulated representation of several power FET characteristics

The following subsections highlight several power FET T_j-dependent electrical characteristics that a Level 3 power FET model can emulate because of its electro-thermal model:

- Drain-to-source breakdown voltage (V_{BRDSS}) vs T_j
- Transconductance curves for various T_j
- Drain-to-source on-resistance ($R_{DS(ON)}$) vs T_j
- Threshold voltage ($V_{GS(th)}$) vs T_j with a small drain current (I_{DS})

IRHNS9A97160 serves as a case study. The simulated outputs are compared to their measured counterparts found in the datasheet (DS). The curve tracing software WebPlotDigitizer, was utilized to generate datasets from curve images extracted from the DS in order to overlay them with simulated datapoints for comparison.

Note: The three highlighted characteristics do not form an exhaustive list of all electrical parameters supported by these Level 3 Power FET models.

4.1 IRHNS9A97160: (V_{BRDSS}) vs T_j

Figure 12 shows the circuit created to evaluate V_{BRDSS} vs T_j for IRHNS9A97160 with identical test conditions as specified in the part's DS. The measurement curve obtained from the DS was overlayed with the simulation output for direct comparison as seen in Figure 13.

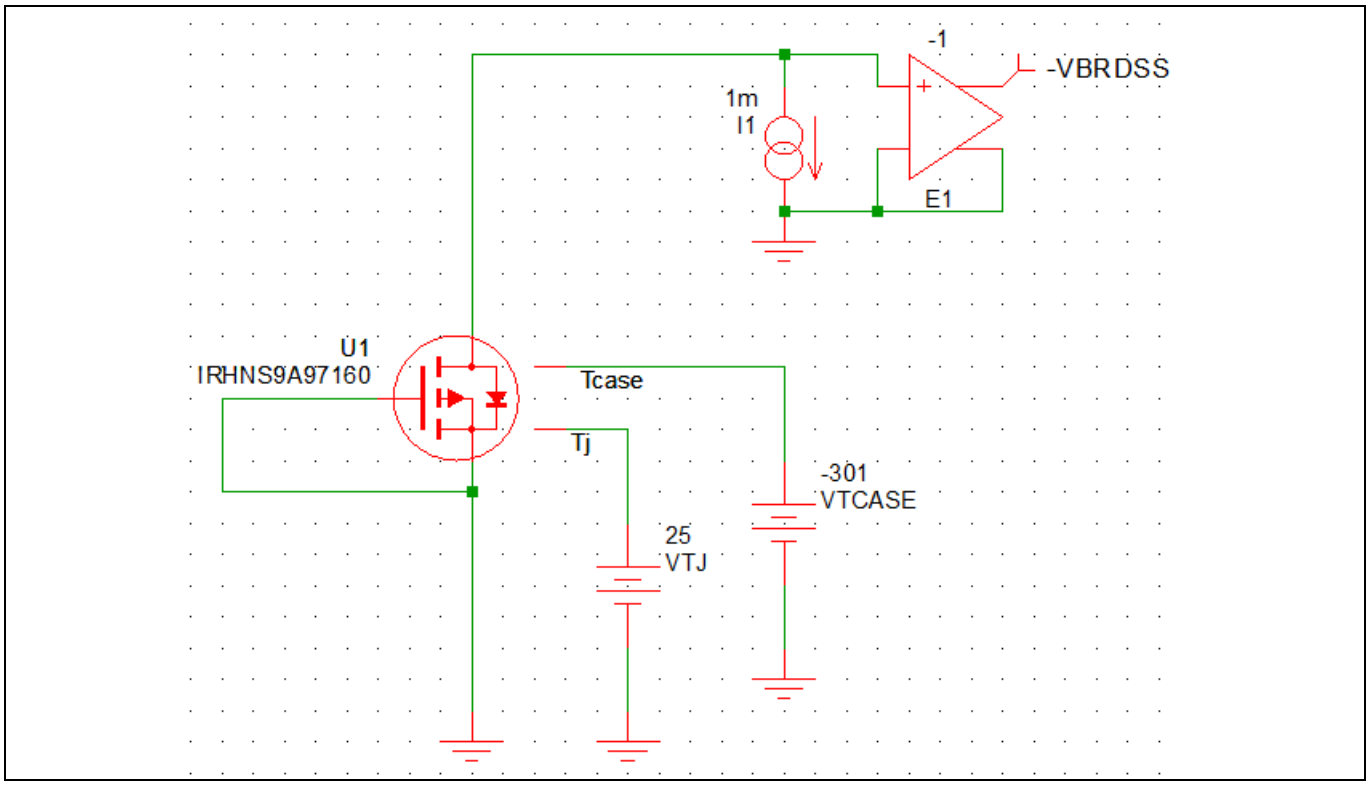

Figure 12 V_{BRDSS} vs T_j test circuit for IRHNS9A97160

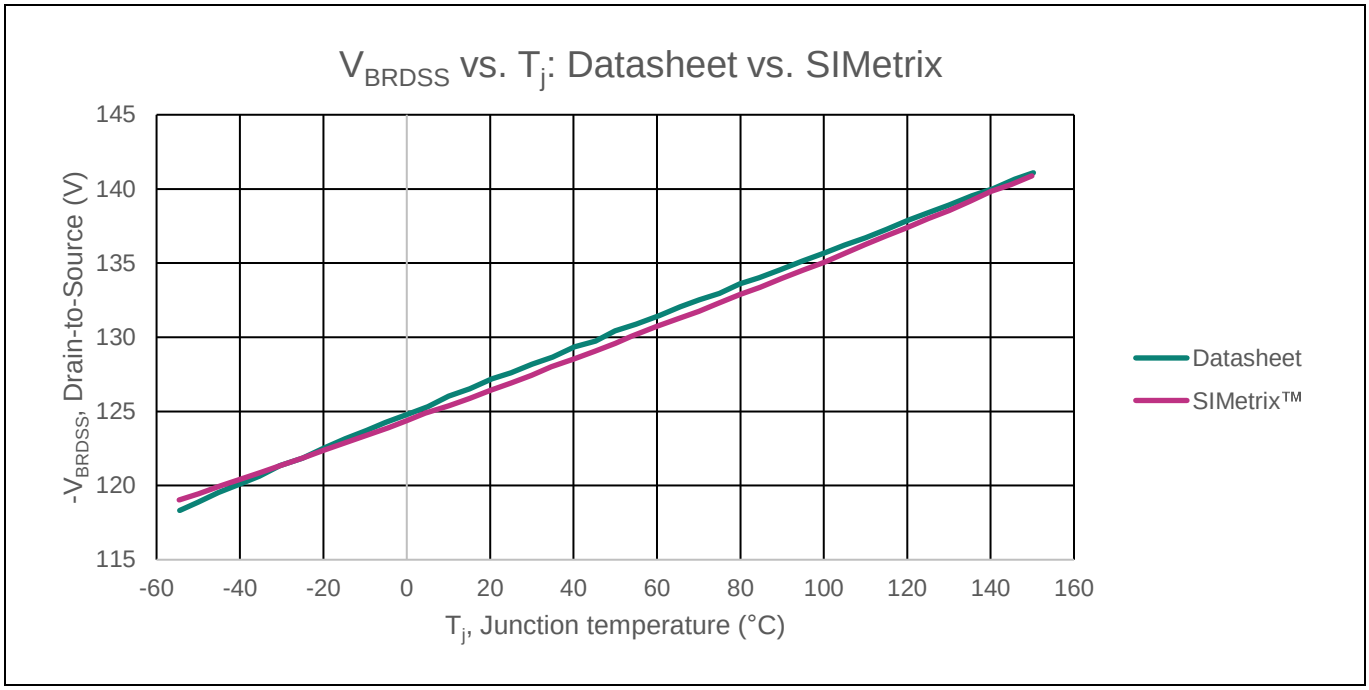

Figure 13 Overlay of V_{BRDSS} vs. T_j curves from IRHNS9A97160 DS and simulation output

Both curves show consistent agreement over the entire operating range of T_j for IRHNS9A97160.

4.2 IRHNS9A97160: Transconductance for various T_j

Figure 14 shows the circuit created to evaluate the transconductance of IRHNS9A97160 for T_j = 25°C and 150°C with identical test conditions as specified in the part's DS. The measurement curves for T_j = 25 °C and 150°C depicted in the DS are overlayed with the simulation output for direct comparison as seen in Figure 15 and Figure 16 respectively. As mentioned in Section 3.1, T_{case} was set to -301 V to force the model of IRHNS9A97160 to operate at different junction temperatures.

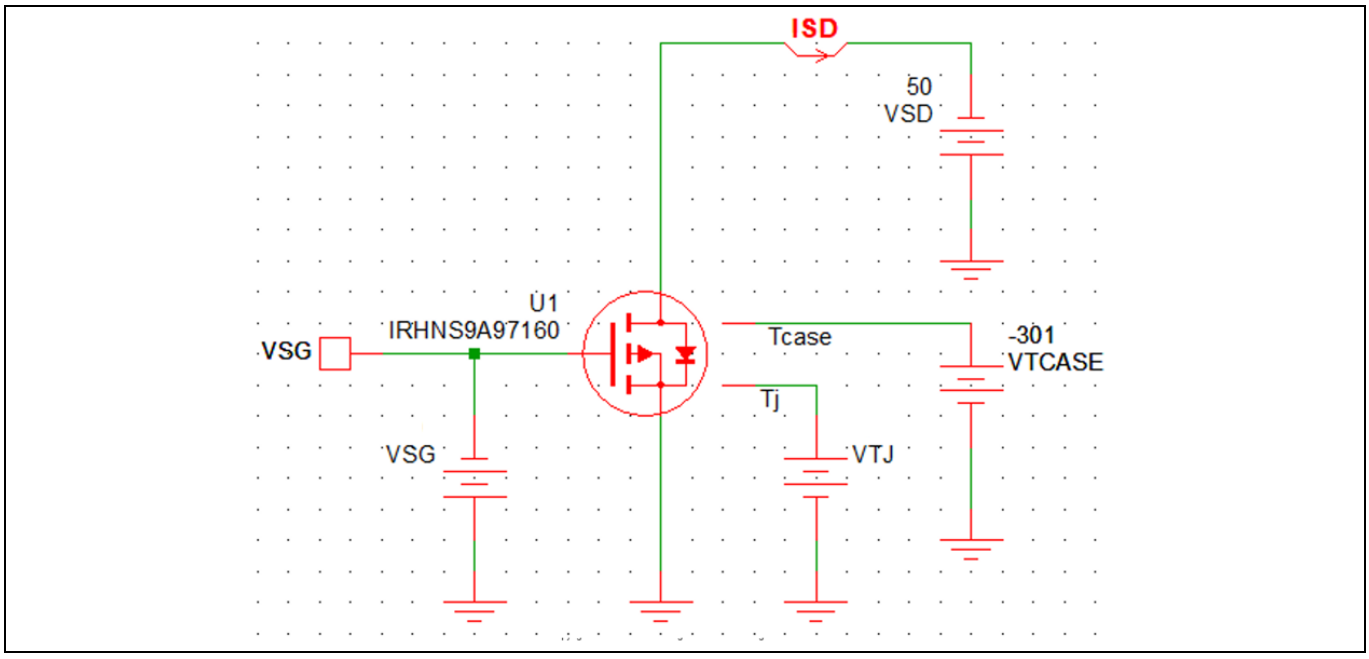

Figure 14 Transconductance test circuit for IRHNS9A97160

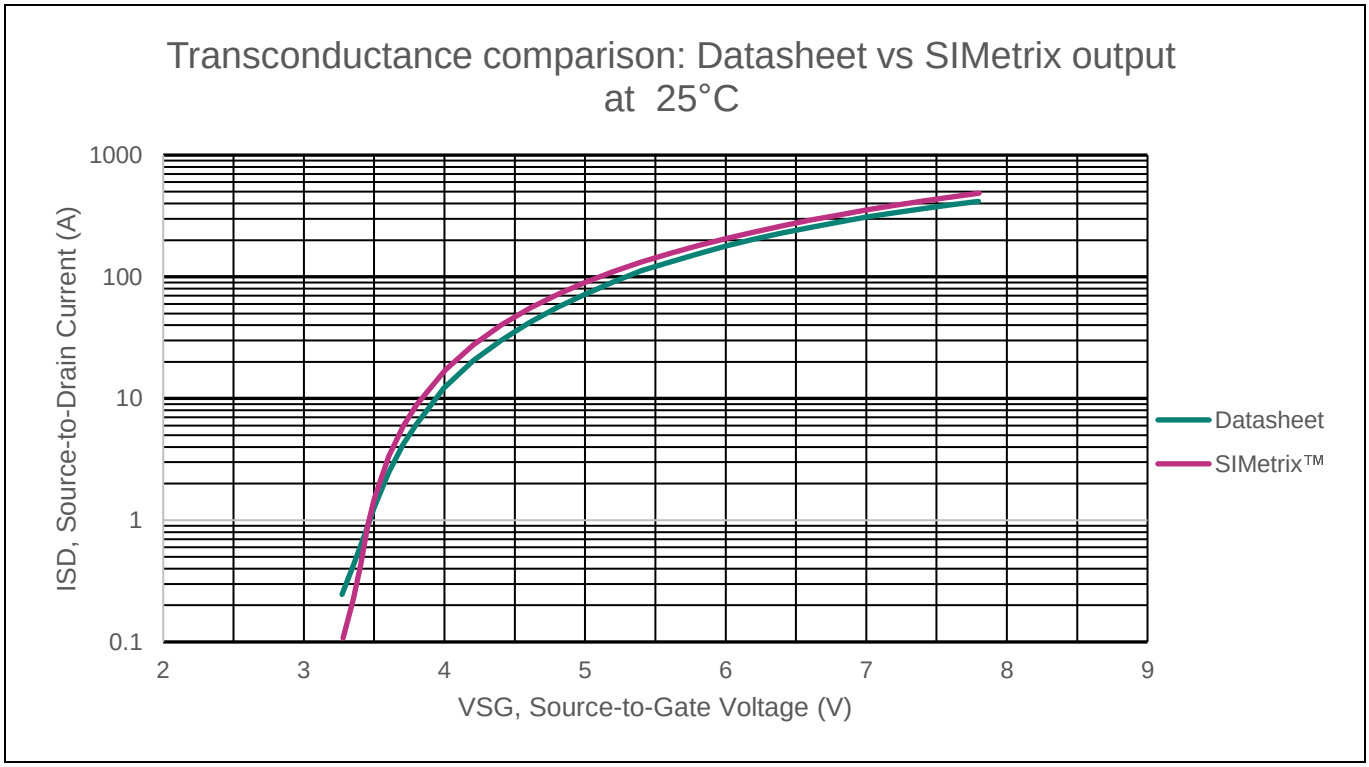

Figure 15 Overlay of transconductance curves from IRHNS9A97160 DS and simulation output at 25°C

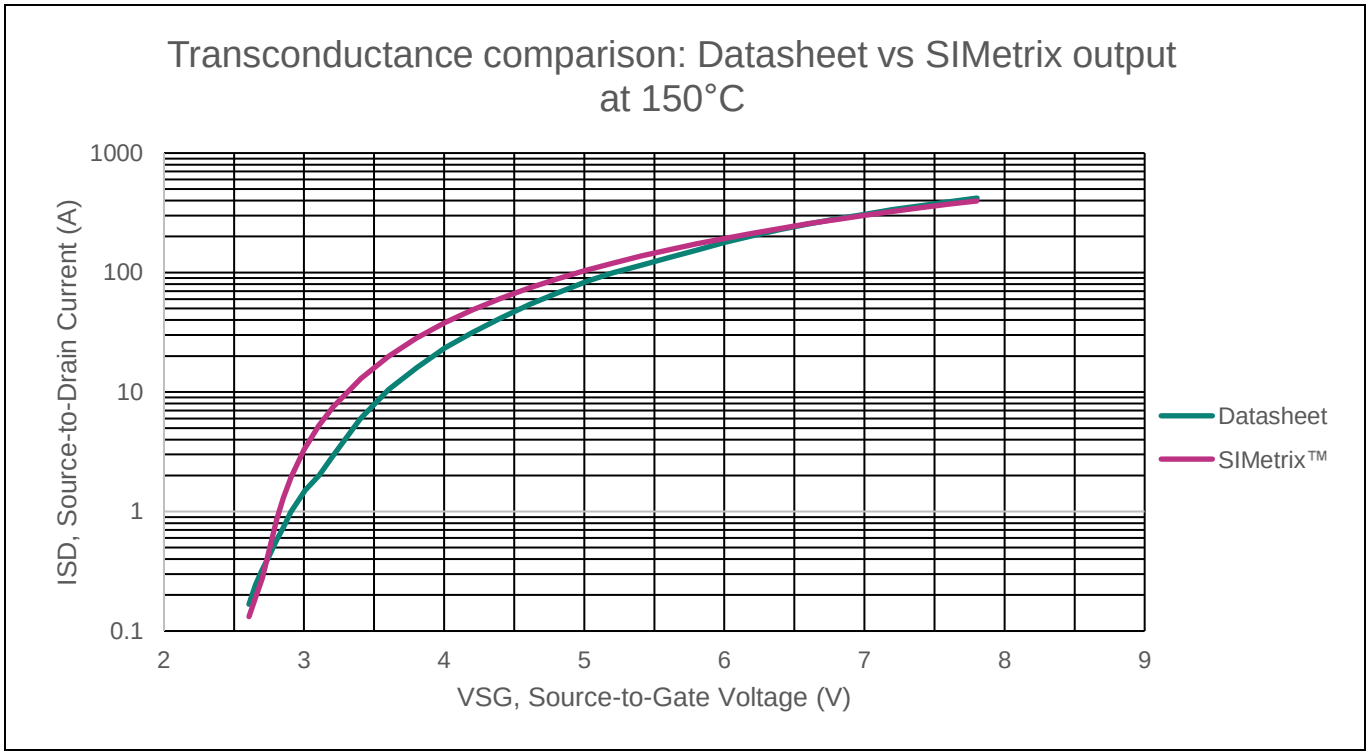

Figure 16 Overlay of transconductance curves from IRHNS9A97160 DS and simulation output at 150°C

The simulated transconductance of IRHNS9A97160 provides a reasonable approximation of measurement data across a range of source-gate voltages (V_{SG}). At edge-case T_j values such as 150°C, the simulated transconductance displays more deviation from measurement values.

4.3 IRHNS9A97160: $(R_{DS(ON)})$ vs T_j

Figure 17 shows a circuit created to induce a significant increase of the T_j within IRHNS9A97160 via a drain-to-source current injection of 91 A during a -10 V VGS pulse that activates the MOSFET for 1 s. As shown in Figure 20, the $R_{DS(ON)}$ of IRHNS9A97160 (like many other MOSFETs) is sensitive to changes in T_j. Three arbitrary probes were implemented to accomplish the following measurements (see Table 1).

Table 1 Arbitrary Probe Functions

Probe Ref	Function	Units
ARB1	$R_{DS(ON)} = \frac{V_{DS}}{I_{DS}}$	mΩ
ARB2	$P_{DISS} = V_{DS} * I_{DS}$	W
ARB3	$ZTH_{jc} = \frac{T_j - T_{case}}{P_{DISS}}$	K/W

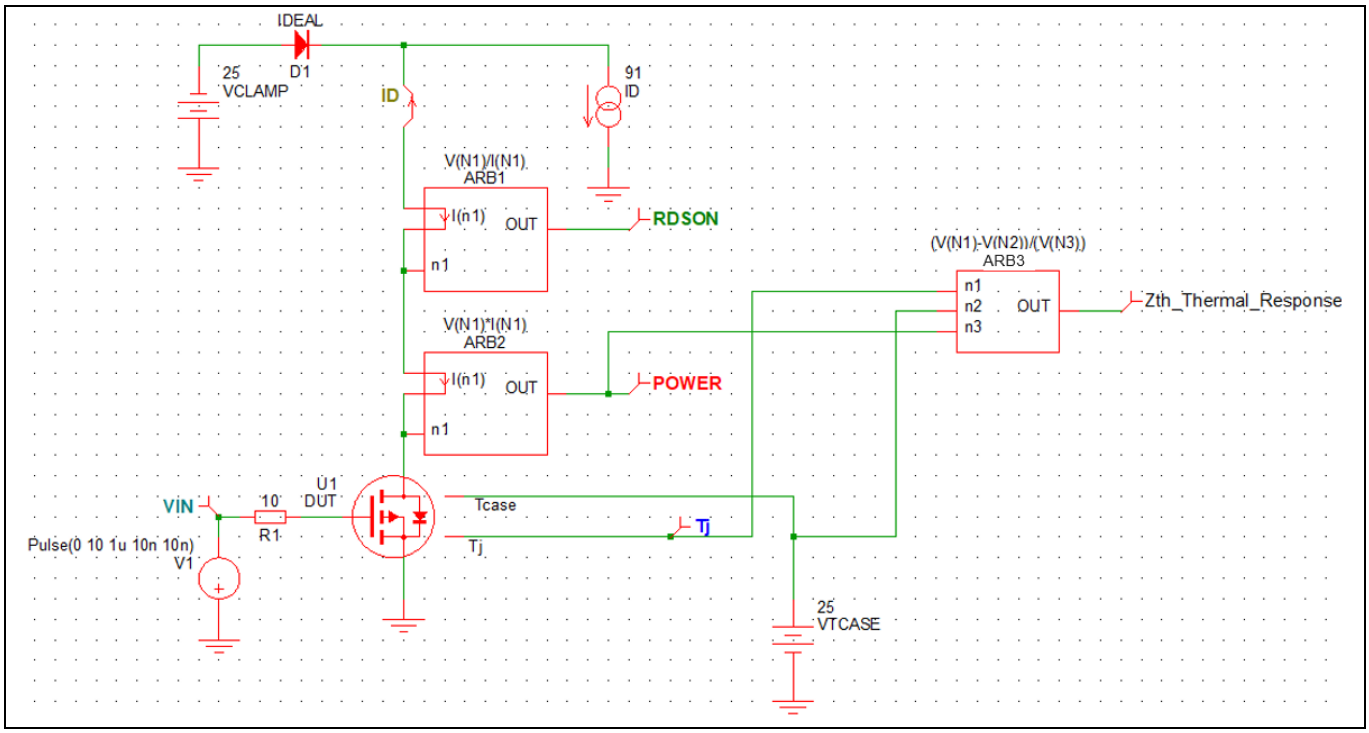

Figure 17 Circuit constructed to induce heating of IRHNS9A97160 junction and alter $R_{DS(ON)}$

A recreation of the single-pulse thermal impedance (Z_{THjc}) of IRHNS9A97160 is implemented within this MOSEFT model to utilize Equation 1 and calculate the expected rise in T_j, (see Figure 18 for a comparison between DS Z_{THjc} and the simulated version).

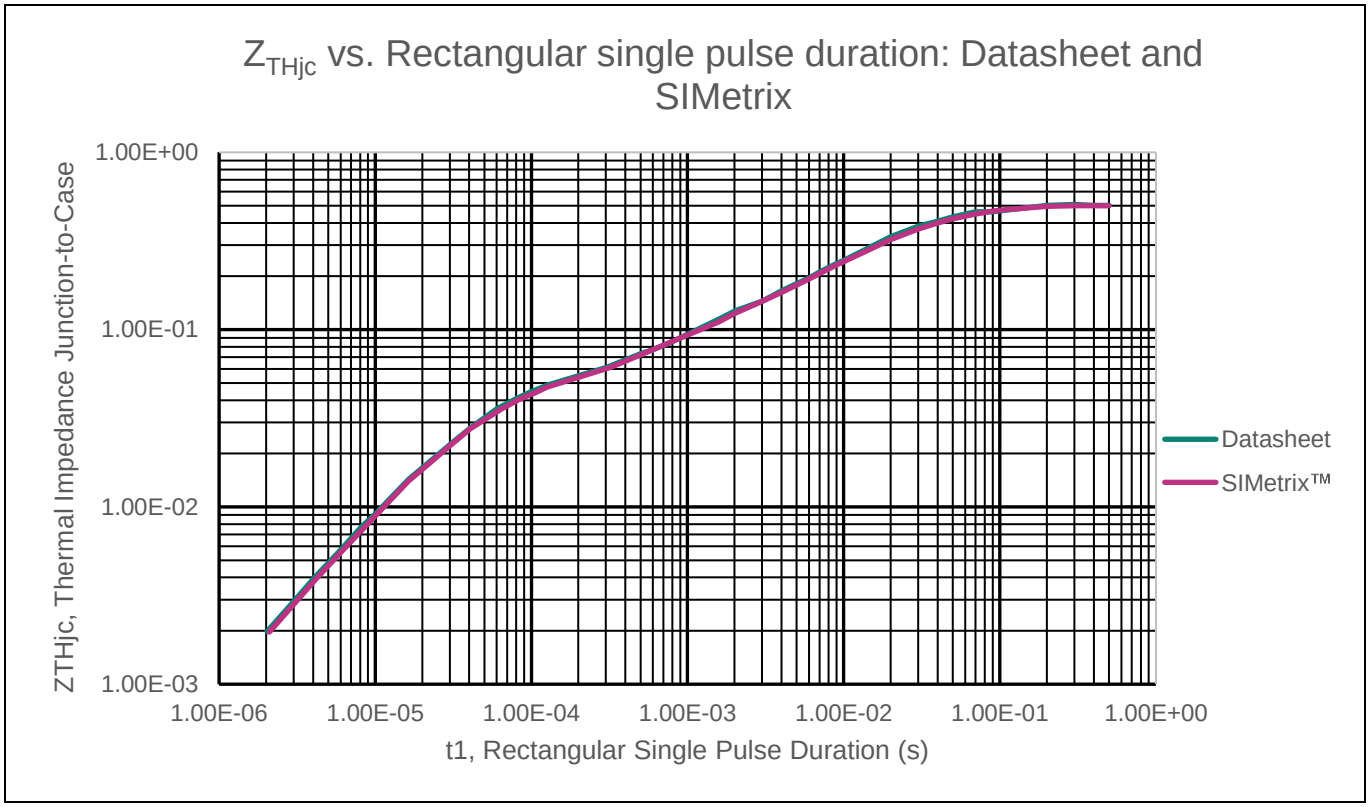

Figure 18 Overlay of Z_{THjc} curves from IRHNS9A97160 DS and simulation output for a single V_{GS} pulse

The Cauer thermal network constructed to emulate the single-pulse Z_{THjc} of IRHNS9A97160 results in consistent agreement between the Z_{THjc} found in the DS and simulation across a broad range of pulse widths.

Figure 19 shows the simulation outputs for the circuit shown in Figure 17. The simulated P_{diss} of IRHNS9A97160 was calculated via Equation 2 to ultimately determine T_j as described in Equation 1. Once IRHNS9A97160 achieves steady-state operation, the T_j and $R_{DS(ON)}$ of the device stabilizes.

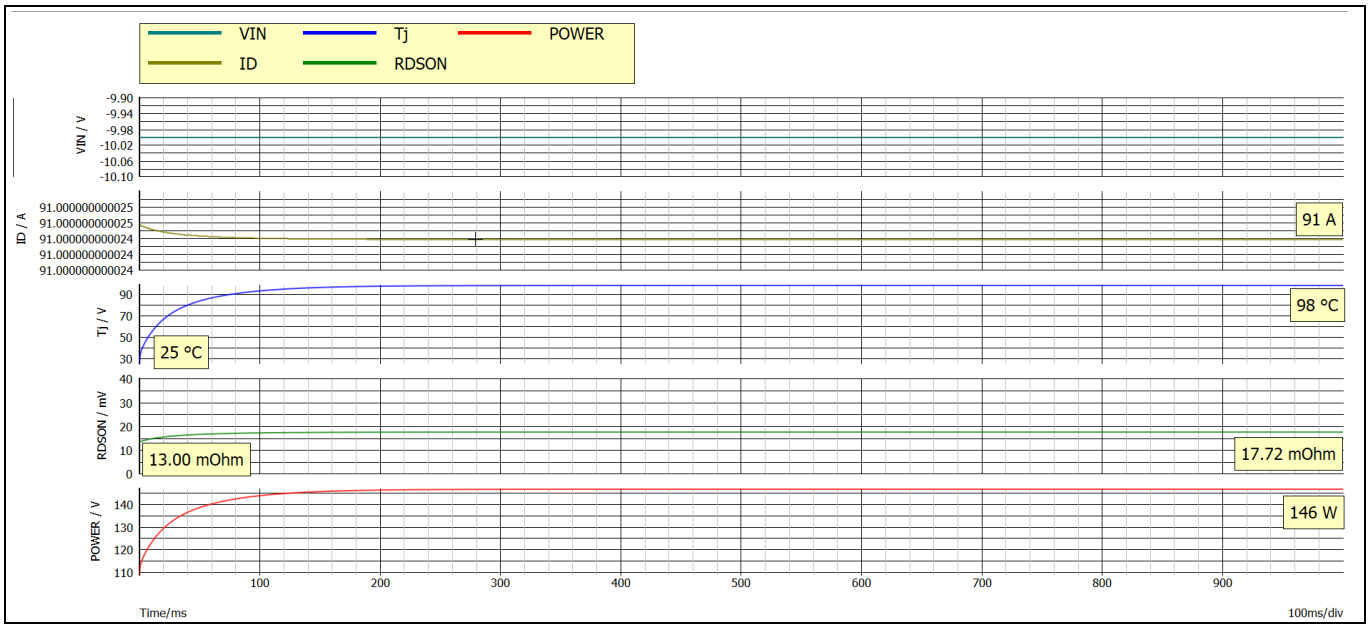

Figure 19 Simulation results of 91 A current injection into IRHNS9A97160

$$P_{diss} = I_{DS}^2 * R_{DS(ON)}$$

Equation 2 Calculation to determine P_{diss} of IRHNS9A97160 in full conduction state of operation

Several additional T_j values were also utilized to investigate changes in $R_{DS(ON)}$ vs a range of T_j. The simulated effects of T_j on $R_{DS(ON)}$ were then compared to the measured changes via curve overlays, (see Figure 20). The worst-case discrepancy between simulation and measurement occurs at edge-case temperature values.

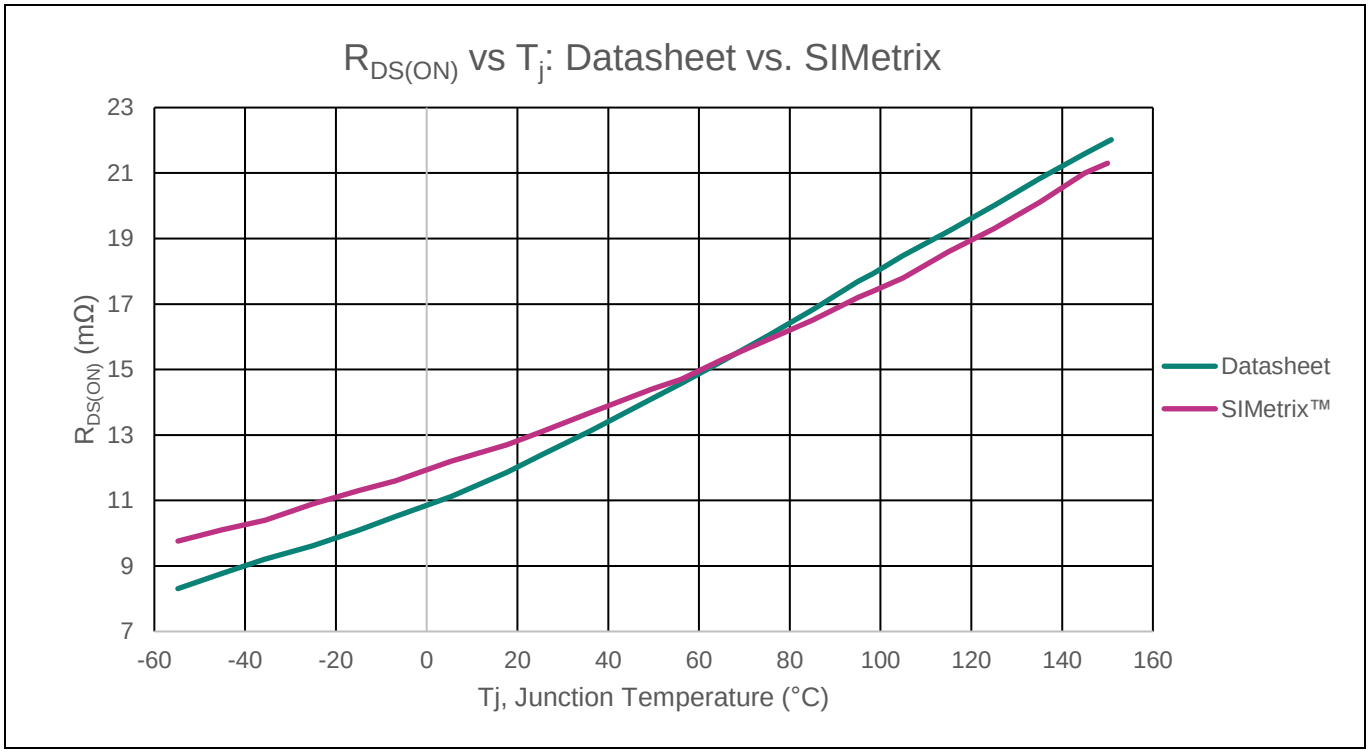

Figure 20 $R_{DS(ON)}$ vs T_j from DS and SIMetrix simulations of IRHNS9A97160

4.4 Threshold voltage ($V_{GS(th)}$) vs T_j with a small drain current (I_{DS})

Figure 21 shows the circuit constructed to investigate the temperature-dependent drift of VGS(th). An I_{DS}= -5 mA measurement curve obtained from the DS was overlayed with the simulation output for direct comparison as seen in Figure 22. The probe designated as “VGS-TH with ID=5 mA” performs the function “XatNthY(V(in), -1, 1)*10e3” which selects the V_{GS} that corresponds with V_{DS} equal to -1 V. The threshold voltage has been achieved once IRHNS9A97160 has an IDS = –5 mA when VGS = VDS.

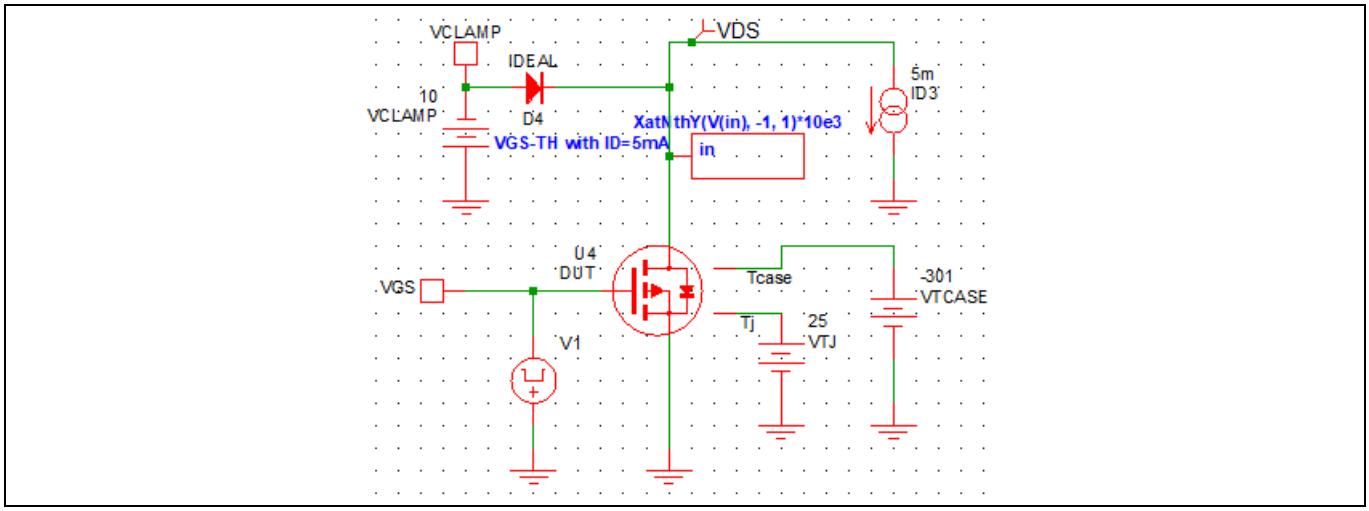

Figure 21 **Circuit constructed to portray the relationship between $V_{GS(th)}$ and T_j at a -5 mA I_{DS} current**

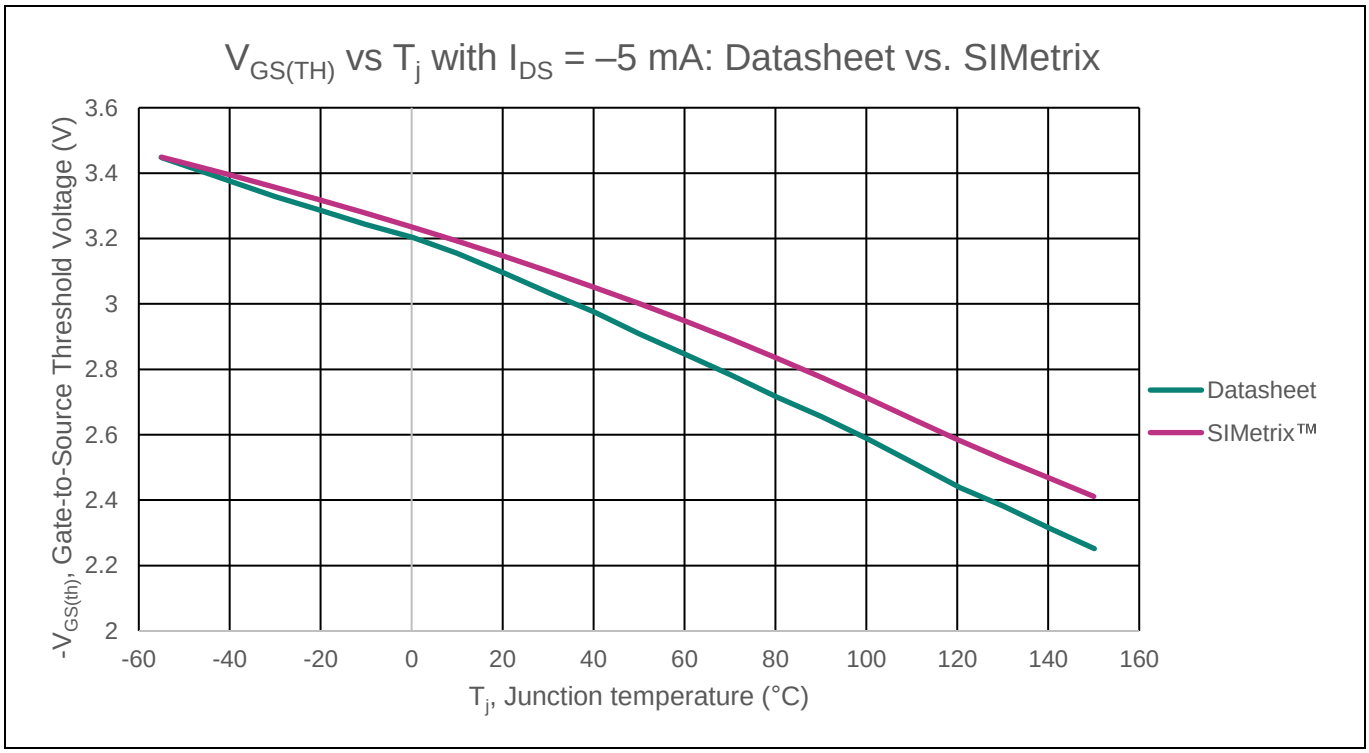

Figure 22 **$V_{GS(th)}$ vs T_j from DS and SIMetrix simulations**

Both curves show consistent agreement until $T_j \geq 50°C$, then the curves deviate. Despite the deviation, both curves portray a similar relationship between $V_{GS(th)}$ and T_j.

5 Simulated applications of Level 3 R9 models

The following subsections showcase the simulation of three applications:

- A 100 kHz open loop half bridge buck converter utilizing a PSpice model of RIC7S113 and Level 3 PSpice models of IRHNJC9A7130
- A Level 3 PSpice model of IRHNKC9A97130 used as an in-rush current limiter
- A 20 kHz open loop half bridge buck converter using Level 3 PSpice models of IRHNS9A97160 in SIMetrix and Cadence OrCAD Capture for comparison of the two simulators

5.1 Open-loop half-bridge buck converter using RIC7S113 and IRHNJC9A7130 in SIMetrix

A RIC7S113EVAL1 evaluation board with IRHNJC9A7130 in place of BUY65CS08J-01 was attached to a low-pass filter to construct a 100 kHz, 28 V to 12 V synchronous buck converter as depicted in Figure 23. An on-board dead time circuit was used to generate ~25 ns of dead time to ensure both IRHNJC9A7130 MOSFETs were operating safely.

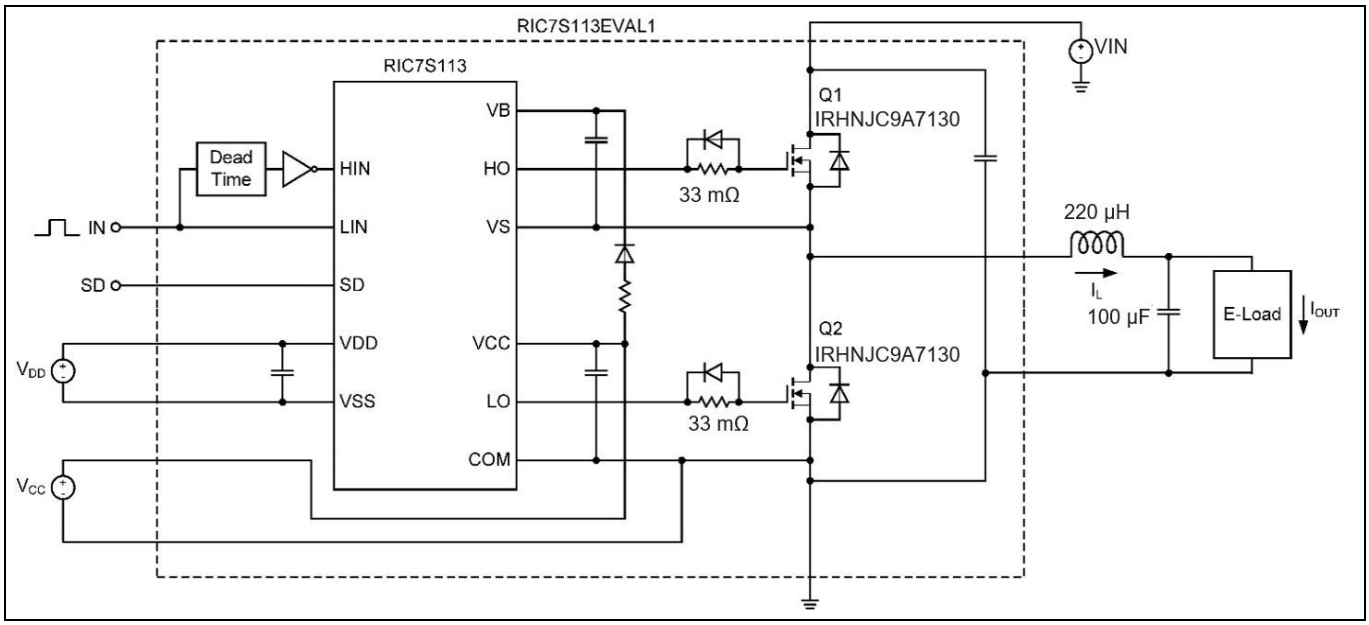

Figure 23 Circuit schematic of a 100 kHz 28 V to 12 V synchronous buck converter using RIC7S113 and two IRHNJC9A7130 MOSFETs

The same synchronous buck-converter circuit was then reconstructed in SIMetrix using a PSpice model of RIC7S113 and Level 3 PSpice models of IRHNJC9A7130 as shown in Figure 24. DMM6500 multimeters were utilized to measure V_{IN} and V_{OUT}. Both MOSFETs (Q1 and Q2) were attached to a second thermal-impedance network to emulate the case-ambient thermal impedance they would experience. A value of 50 thermal-ohms was selected to account for small amount of heat sinking that RIC7S113EVAL1 provided.

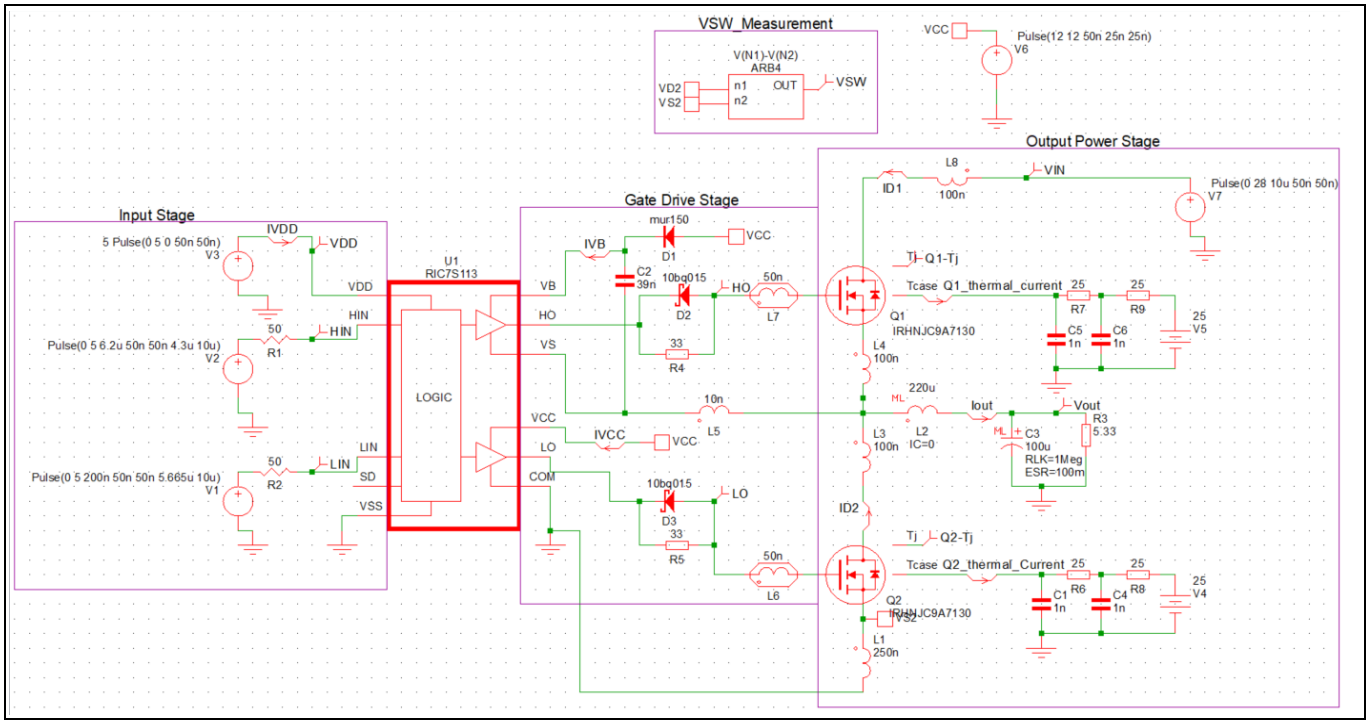

Figure 24 SIMetrix reconstruction of circuit in Figure 22

Figure 25 shows the four key voltage and current measurements (V_{IN}, V_{SW}, V_{OUT}, and I_{OUT}) during 18 µs of buck converter operation in both scenarios. V_{IN}, V_{SW}, and Iout show consistent agreement between simulation and bench top measurement. The simulated measurement of V_{OUT} did not predict the voltage ripple captured from the corresponding benchtop measurement because the simulation utilized an idealized output bulk capacitor to simplify circuit construction. However, the average value of V_{OUT} between benchtop and simulation agreed at ~ 11.16 V. Several parasitic inductances were incorporated within Figure 24 to reflect the relatively long current loop within the physical power stage layout of RIC7S11EVAL1, contributing to the voltage ringing shown in the simulation.

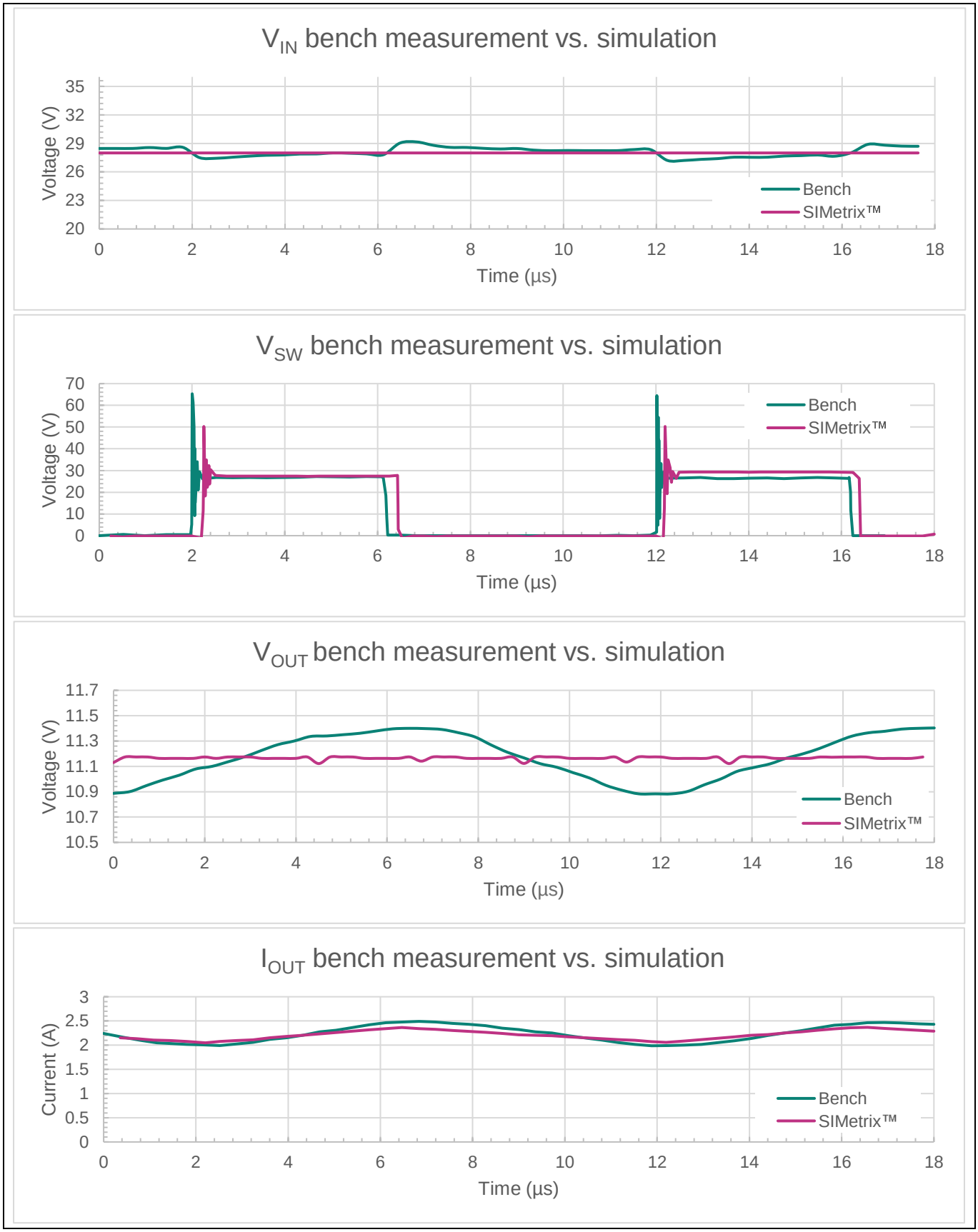

Figure 25 **Physical measurements vs simulation of V_{IN}, V_{SW}, V_{OUT}, and I_{OUT} for a 100 kHz 28 V to 12 V buck converter**

Figure 26 and Figure 27 showcase a comparison between the T_j of both IRHNJC9A7130 devices when implemented in a benchtop prototype circuit and in simulation of the buck converter shown in Figure 23. The electro-thermal network integrated within Level 3 PSpice models allows users to understand how a transistor's T_j will be affected by circuit operation. Both scenarios demonstrated that the high-side MOSFET (Q1) would be more thermally stressed than the low-side MOSFET (Q2) during steady-state operation. Therefore, the simulation did accurately reflect the discrepancy in thermal stresses both MOSFETs would experience. Through simulation, designers are armed with useful knowledge about which MOSFET may degrade faster if not properly supported with a heat sink during the prototyping stage of their application.

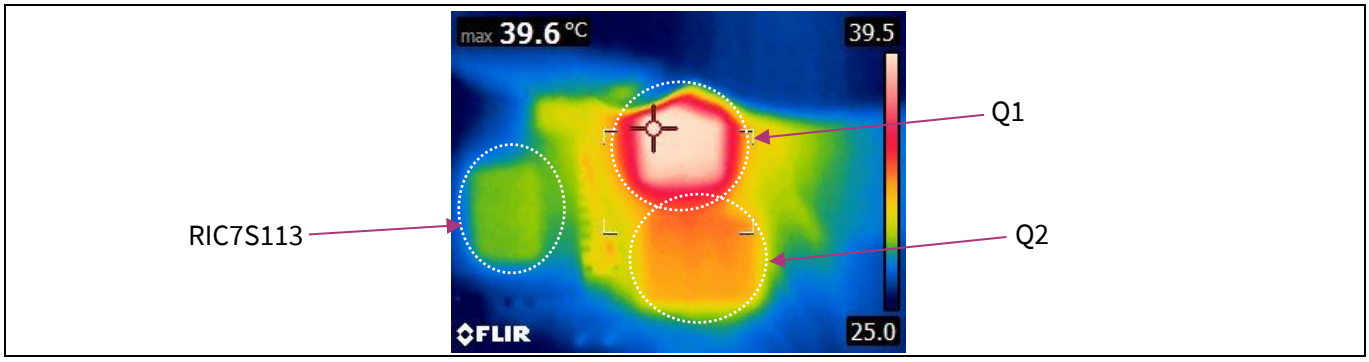

Figure 26 Thermal capture of the two IRHNJC9A7130 MOSFETs and RIC7S113 during operation

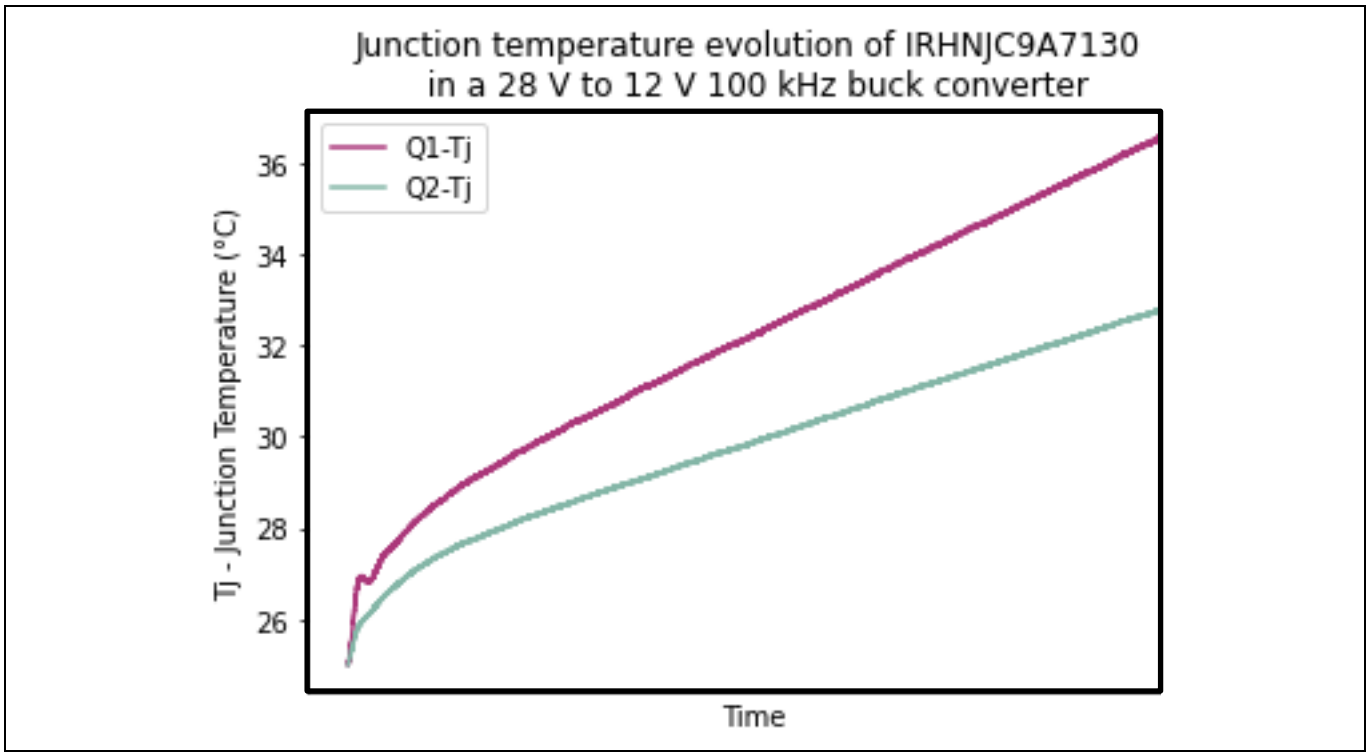

Figure 27 Simulated changes in T_j of both IRHNJC9A7130 MOSFETs during 28 V to 12 V synchronous buck converter operation using RIC7S113EVAL1 within SIMetrix

5.2 IRHNKC9A97130 as in-rush current limiter in SIMetrix

IRHYS9A97034EVAL1 is an evaluation board developed by IR HiRel to showcase IRHYS9A97034CM (60 V/30 A P-Channel R9 MOSFET) as an in-rush current limiter. Figure 28 shows the schematic of the evaluation board.

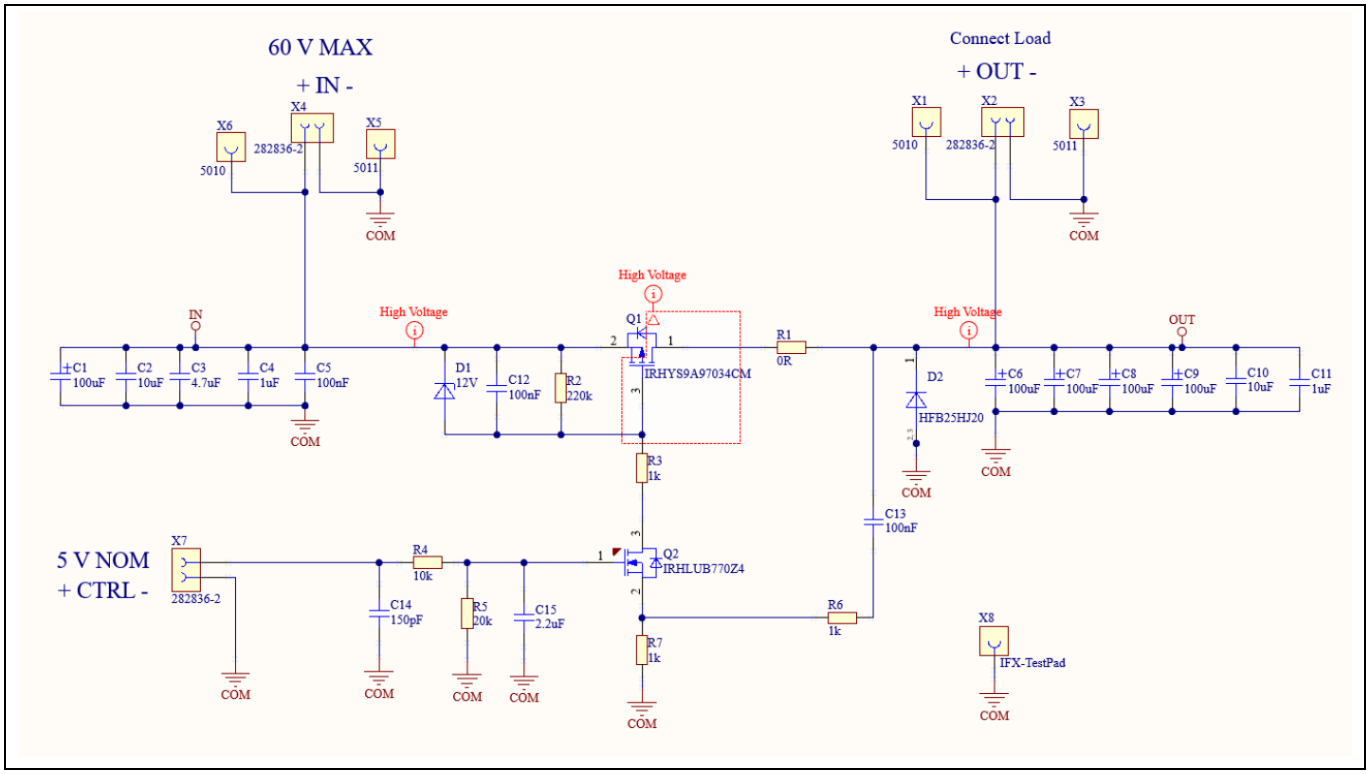

Figure 28 IRHYS9A97034EVAL1 circuit schematic

The electro-thermal model integrated within Level 3 Power FET PSpice models allows you to simulate other P-Channel R9 MOSFETs in a similar application to understand their potential as in-rush current limiters before developing any prototypes and performing benchtop measurements. For example, in Figure 29, a simulated circuit of IRHYS9A9EVAL1 has been created with IRHNKC9A97130 in place of IRHYS9A97034CM to compare the performance between both R9 MOSFETs to see if IRHNKC9A97130 could be a viable alternative. Simulating the behavior of IRHNKC9A97130 would a low-cost first step in evaluating this R9 MOSFET.

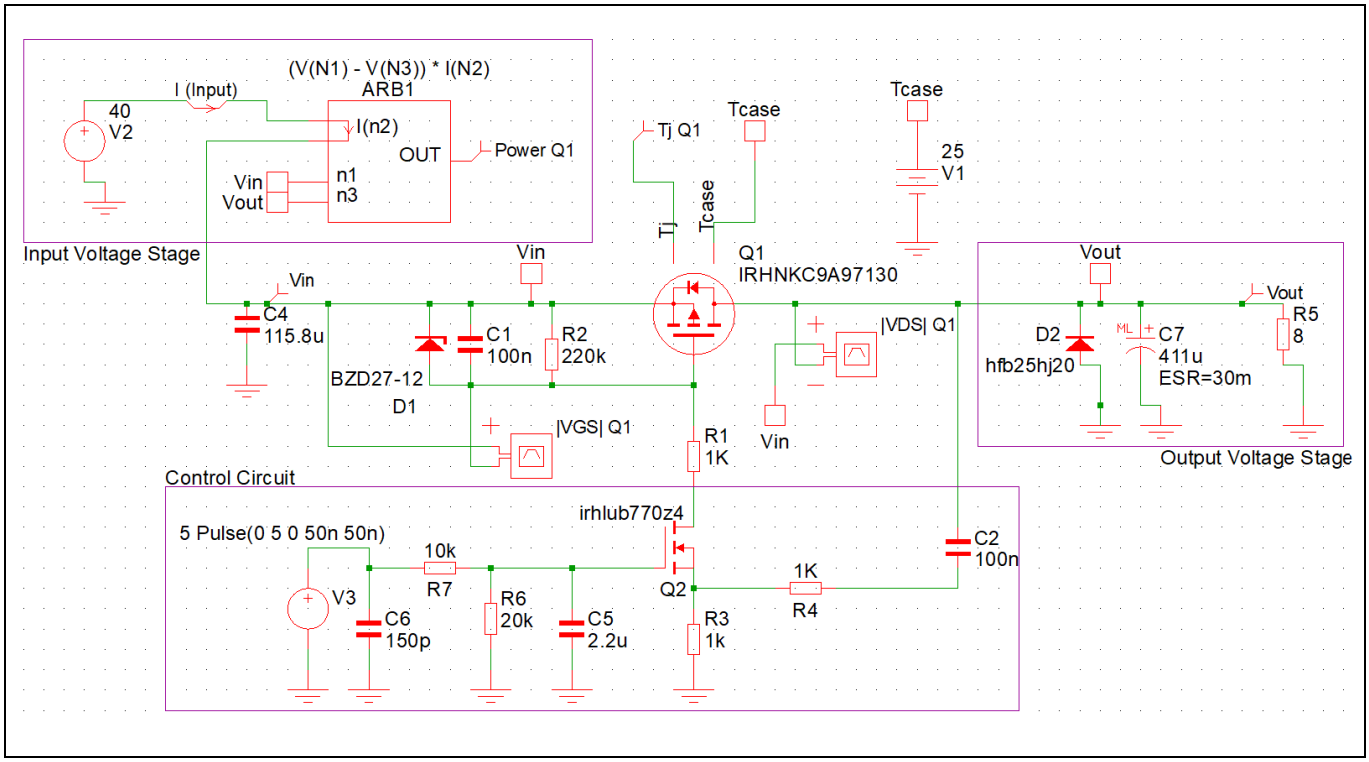

Figure 29 Circuit model of IRHYS9A97034EVAL1 with IRHNKC9A97130 (U1) to prevent overcurrent

Figure 30 depicts the key simulated waveforms of IRHNKC9A97130 overlayed with corresponding benchtop measurements of IRHYS9A97034CM to compare the capabilities of both R9 MOSFETs as in-rush current limiters. The control circuit (Q2) in both scenarios' forces Q1 to gradually enter the ohmic region of operation to ensure a safe in-rush current. During this transitory period, both R9 variants experienced the greatest amount of power dissipation, but the thermal characteristic of each device ensures they will survive and continue to operate normally. Table 2 compares some key metrics between the benchtop of performance of IRHYS9A97034CM against IRHNKC9A97130 in a simulation.

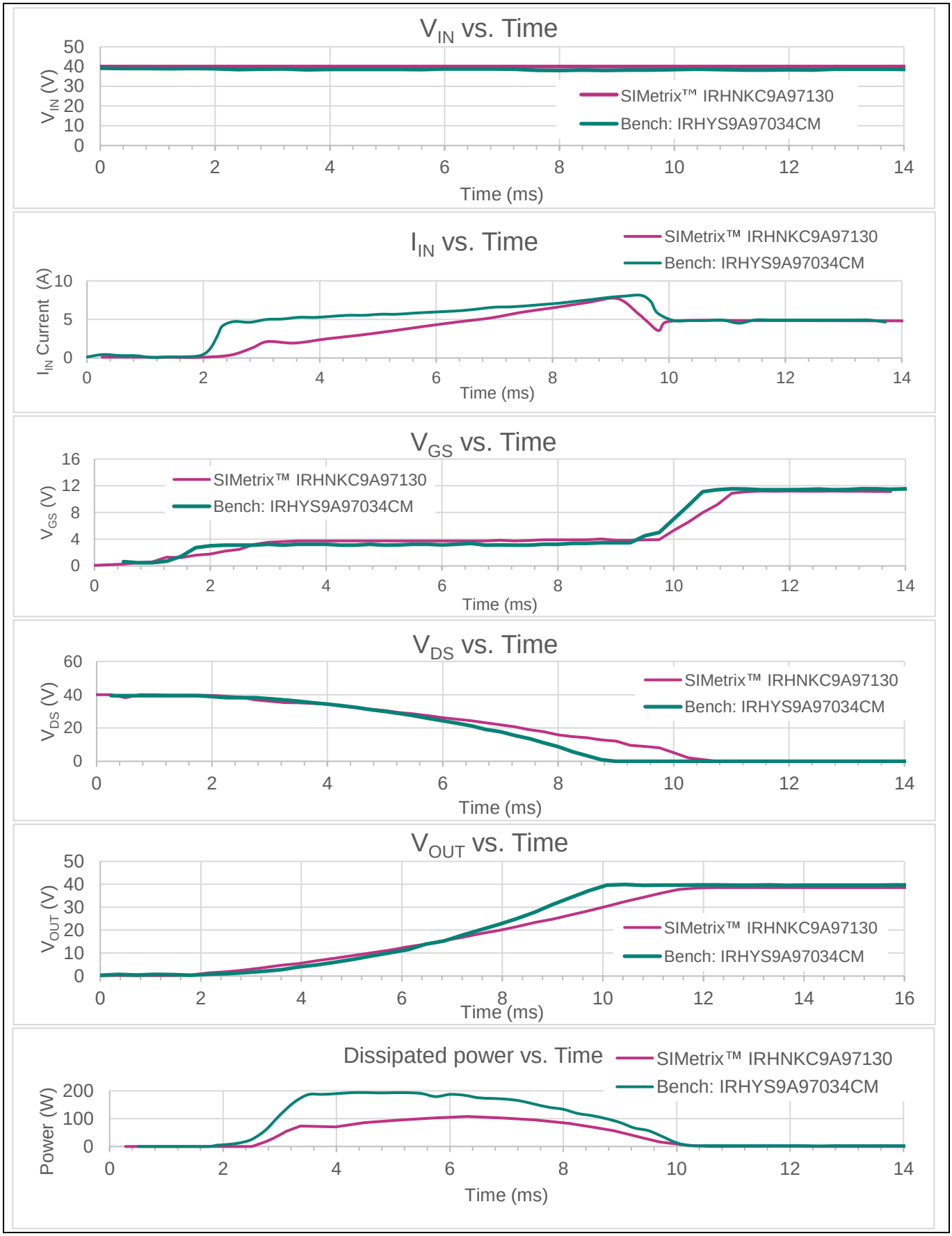

Figure 30 Benchtop measurement of IRHYS9A97034CM vs simulation of IRHNKC9A97130 during similar inrush events

Table 2 Key metrics for IRHYS9A97034CM benchtop circuit vs IRHNKC9A97130 simulation counterpart

Metric	IRHYS9A97034CM benchtop	IRHNKC9A97130 simulation
Duration of operation (ms)	8.0	7.3
Peak in-rush current (A)	8.1	7.7
Peak power dissipated (W)	190	110

In both scenarios, the duration of the in-rush event and the peak in-rush current are in relatively close agreement. Therefore, designers are equipped to expect ~ 8 A of current to pass through IRHNKC9A97130 when the MOSFET is activated to connect load and input supply. The simulation of IRHNKC9A97130 experienced approximately 60 percent of the peak power dissipation that IRHYS9A97034CM was calculated to experience from measurement. This discrepancy was due to the relatively slower input current rise that IRHNKC9A97130 was subjected to in simulation vs IRHYS9A97034CM on a benchtop circuit while the VDS of both MOSFETs was still significant during the initial ms of operation.

During the simulated in-rush event of IRHNKC9A97130, the average VDS and IDS experienced by this MOSFET were calculated to be 25 V and 4 A respectively. According to the maximum safe operating area (SOA) of single-pulse events for IRHNKC9A97130 (see Figure 31), an average power dissipation of 100 W will not put the MOSFET at risk. Therefore, IRHNKC9A97130 is a possible alternative to IRHYS9A97034CM and building a prototype in-rush circuit would be the next step to prove out the viability of IRHNKC9A97130.

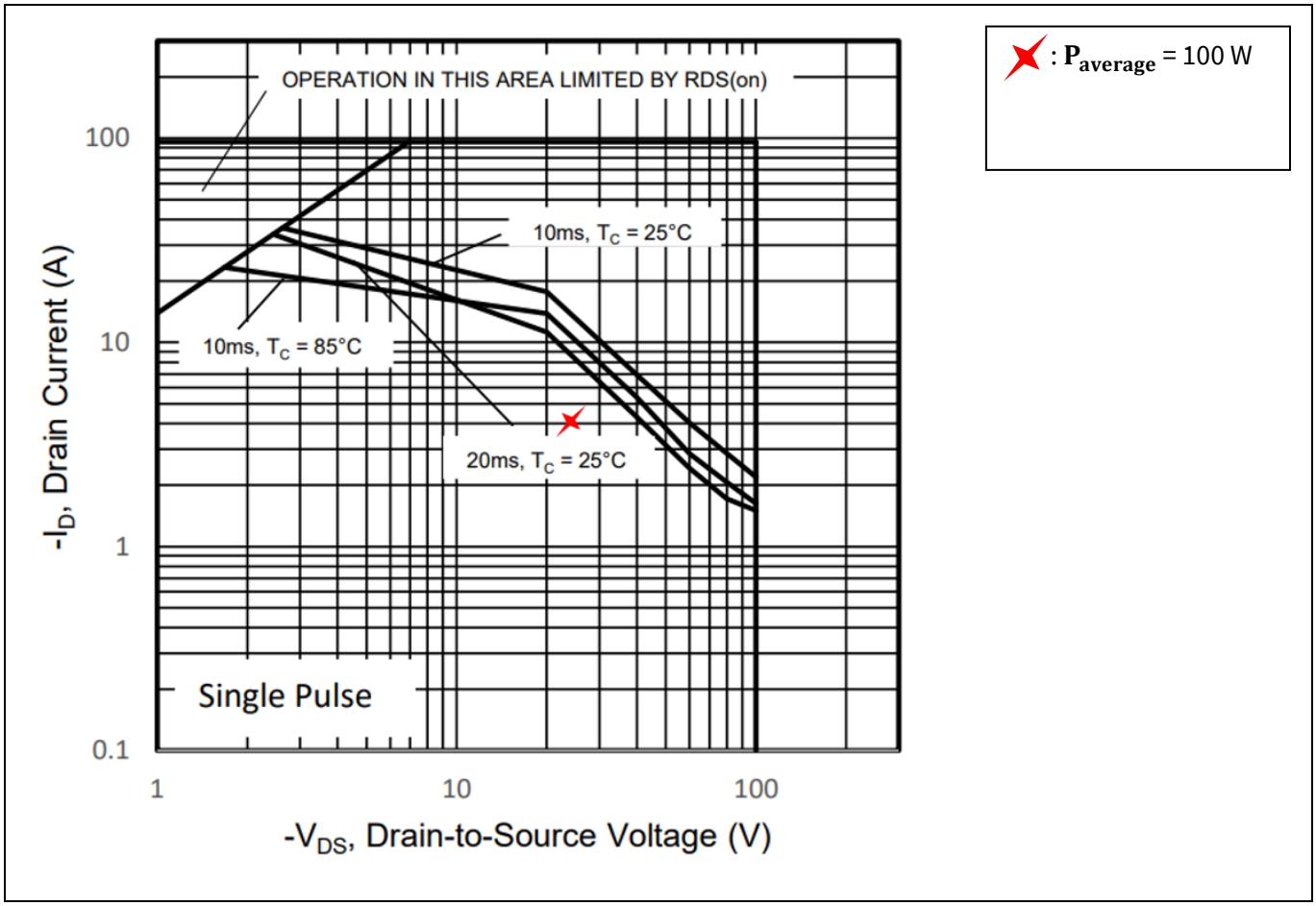

Figure 31 Simulated P_{max} of IRHNKC9A97130 when used as a current inrush limiter in a set up similar to IRHYS9A97034EVAL1

5.3 IRHNS9A97160 buck converter in Cadence OrCAD Capture and SIMetrix

The following figure shows a circuit and the key measured waveforms of a 20 kHz synchronous buck converter with a 9 V output and 0.2 Ω load represented in the simulators SIMetrix and Cadence OrCAD Capture to demonstrate consistent behavior of Level 3 PSpice Power FET models across different simulators. A duty cycle of 9 percent was implemented to step down an input voltage of 100 V to a 9 V output at the load.

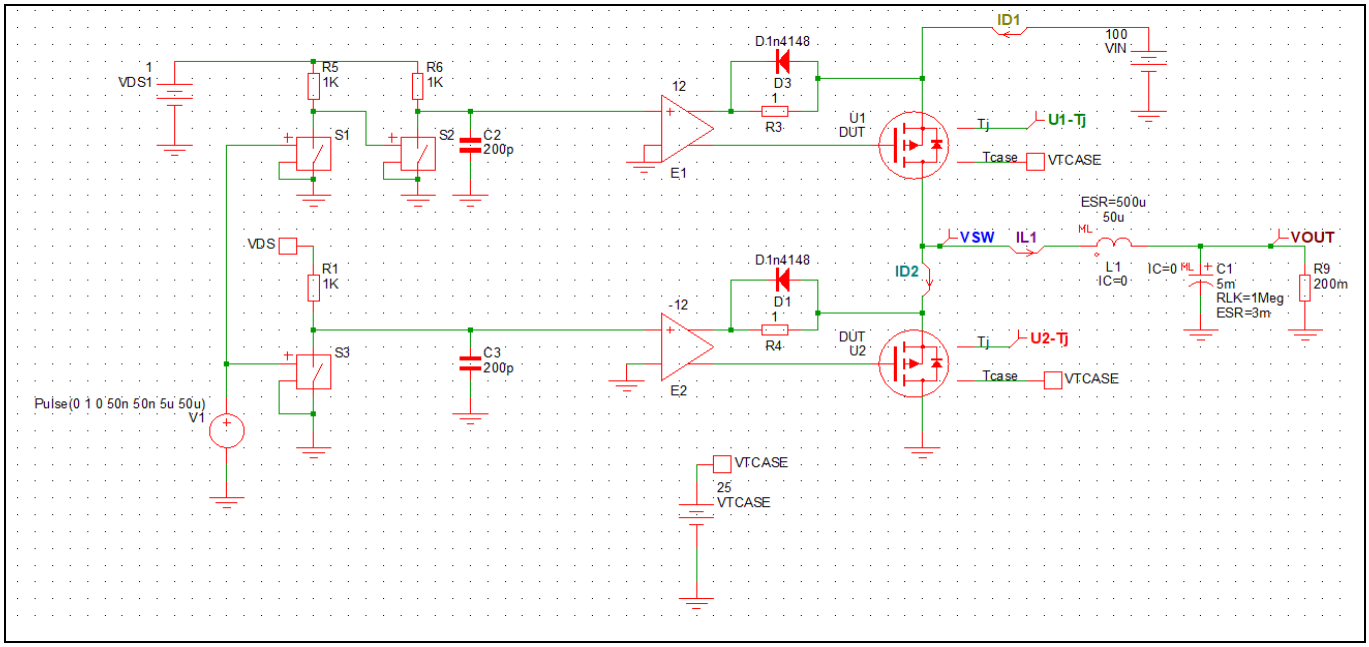

Figure 32 20 kHz synchronous buck converter demonstration circuit in SIMetrix

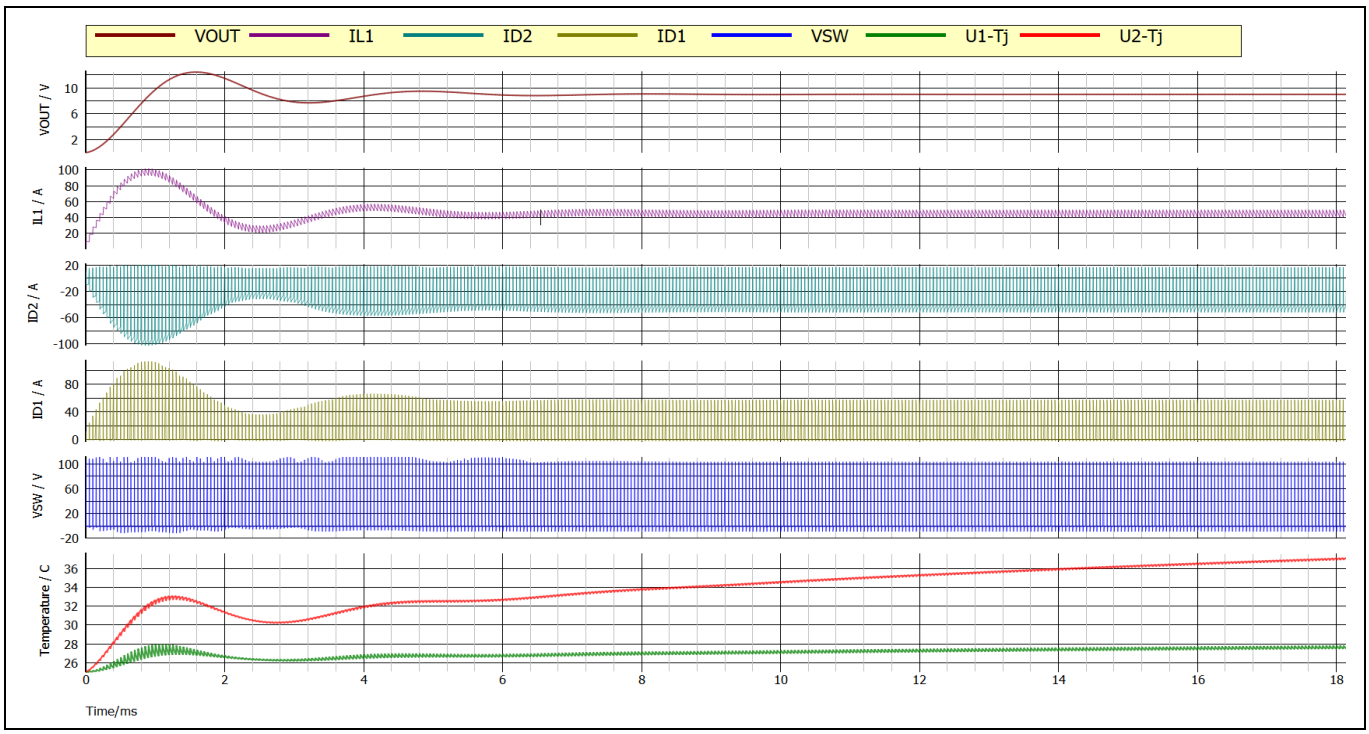

Figure 33 Circuit outputs for 20 kHz synchronous buck converter in SIMetrix

Figure 33 shows the buck converter in operation over 18 ms. Both MOSFETs experience a relatively large amount of heating at their junction's during the initial 2 ms of operation before the circuit achieves steady-state operation and the current through both MOSFETs stabilizes. Afterwards, the junction temperature of both MOSFETs continues to increase but flatten out as the thermal profile of the part stabilizes. The low-side MOSFET experiences significantly more junction heating than the high side MOSFET because it remains in the ohmic state over longer amounts of time due to a 9 percent duty cycle.

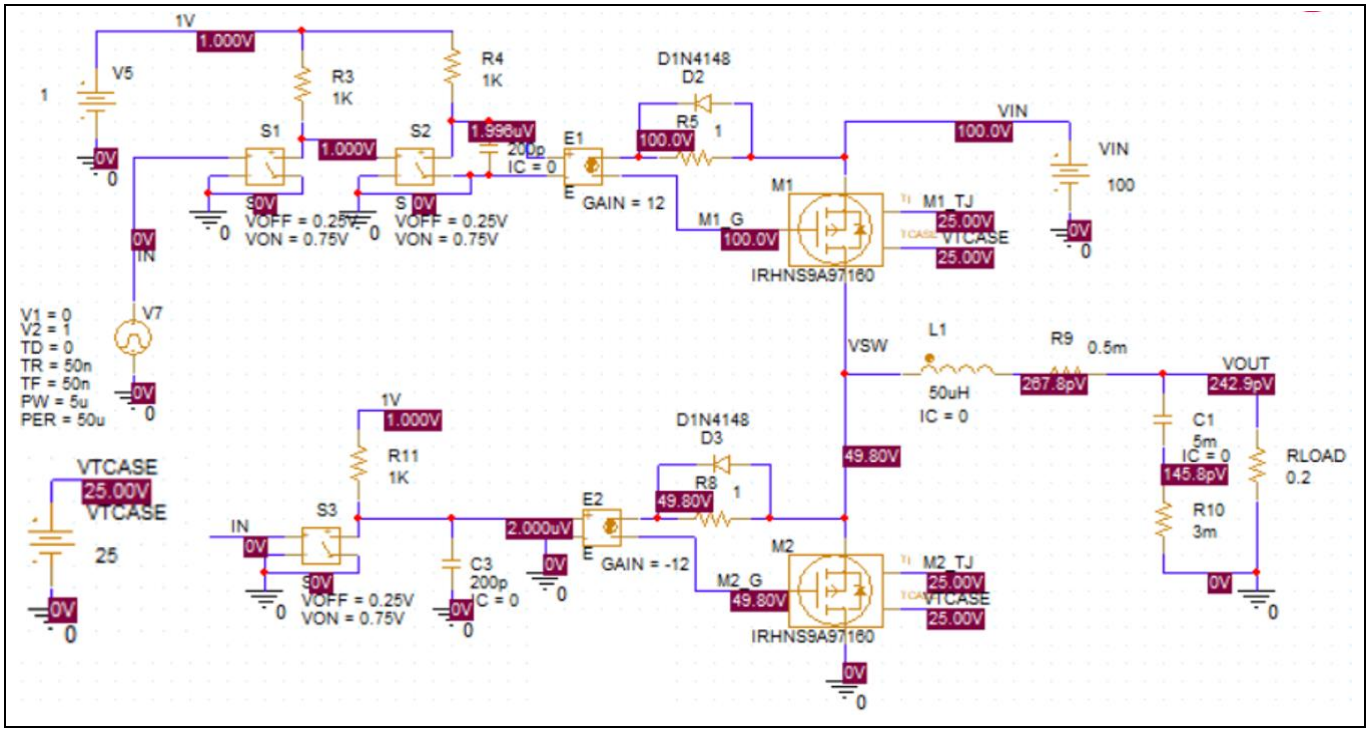

Figure 34 20 kHz buck converter demonstration circuit in Cadence OrCAD Capture

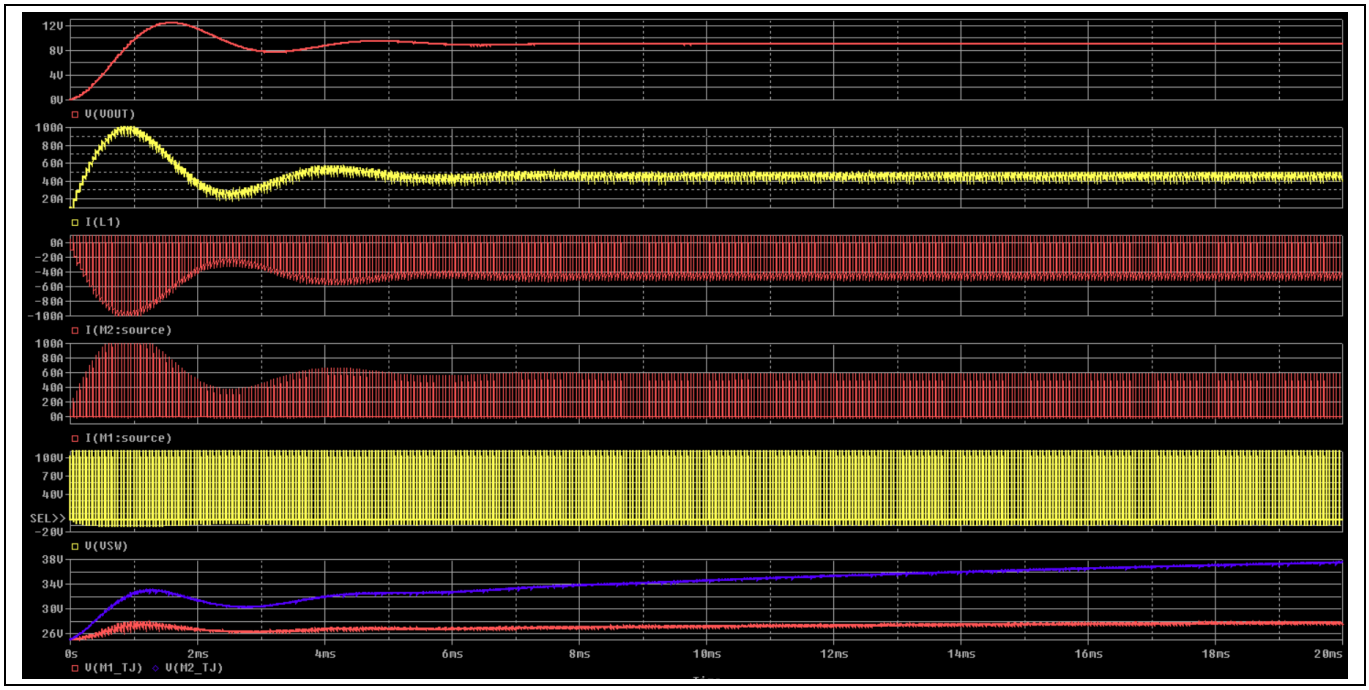

Figure 35 Circuit outputs for 20 kHz buck converter in Cadence OrCAD Capture

The identical waveforms depicted in Figure 33 and Figure 35 indicate that the library models of IRHNS9A97160 utilized in SIMetrix and Cadence OrCAD Capture show consistent behavior across different simulators.

6 Conclusion

The introduction of Level 3 power FET PSpice simulation models by IR HiRel allows designers to take full advantage of an electro-thermal model that provides an in-depth look into the real-time performance of several product lines (R8, R9, RG1, and RT) developed by IR HiRel for various applications. Each Level 3 power FET model is constructed from measurement data obtained for each part to ensure there is a strong correlation between the physical part and its corresponding simulation model. Two applications (a buck converter and in-rush current limiter) were investigated to show potential designers how these new models can emulate real circuit performance. Therefore, you may have greater insight into the behavior of their circuit before benchtop tests commence.

References

[1] Infineon Technologies AG: *Introduction to Infineon's Simulation Models Power MOSFETs V2.0; Application Note 2014-02*; Available online

[2] Infineon Technologies AG: *Transient thermal measurements and thermal equivalent circuit models V1.2; Application Note 2015-10*; Available online

Revision history

Document revision	Date	Description of changes
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V 1.1	2025-01-27	Revised some figures

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