Overall loop delay in CAN networks

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In automotive and industrial applications, different variants of the CAN protocol are established. In general, a transmitting CAN protocol handler reads back the receive data from the bus as reaction to its own transmitted data and compares it with the transmitted data. Due to several effects, there is the so-called loop delay between the transmitted data and the received data. The overall loop delay of the transmitting node is important especially in the arbitration phase. When looking only at the parameters related to the CAN transceiver alone, some parts of the loop delay may be forgotten. In reality, the physical layer comprises also the complete digital signaling path, starting from the CAN protocol handler (e.g. located in a host controller device), to the connected CAN transceiver for the transmit path and back to the protocol handler for the receiving path. In between are a lot of delays and this article likes to give some hints on how to consider all these delays in the CAN network. This is valid for Classical CAN, CAN FD and CAN XL protocol as well as for all kind of CAN Transceivers. But the focus will be on CAN FD Transceivers and CAN SIC Transceivers.

The basic concept of the CAN protocol

Each frame of the CAN protocol comprises two main phases, an arbitration phase and a data phase. The difference between Classical CAN protocol and the CAN FD protocol is that in Classical CAN, the protocol handler transmits all phases of the complete frame with the same bit rate, whereas in CAN FD, the protocol handler transmits with a lower bit rate in the arbitration phase (for example 500kBit/s) and a higher bit rate in the data phase (for example 5 Mbit/s). Independent from the protocol variant, the protocol handler reads back the received data and compares it to the transmitted one. As a consequence, the receive data belonging to the same bit position in the CAN frame as the transmit data must be available at the protocol handler input before the CAN protocol handler samples the data value. In the data phase of the CAN FD protocol the loop delay is not so important, because the transmitter delay compensation unit in the CAN FD controller compensates the loop delay of the transmitting node.

The overall loop delay of the CAN physical layer

The overall loop delay of the CAN physical layer comprises:

1. Propagation delay from the transmit data output of the CAN protocol handler to the transmit data input of the CAN transceiver
2. Propagation delay Microcontroller port to Transceiver TxD input pin.
3. Loop delay of the CAN Transceiver (CAN Transceiver, CAN FD transceiver or CAN SIC transceiver)
4. Propagation delay from the receive data output RxD of the Transceiver to RxD input port of the CAN controller.
5. Propagation delay microcontroller RxD input port to the CAN controller
6. Synchronization delay in the CAN protocol handler itself (the receive data is an asynchronous input signal to the protocol handler).

Figure 1 shows the complete physical layer loop delay path of a transmitting CAN node, assuming that the protocol handler and the transceiver are located in separate devices.

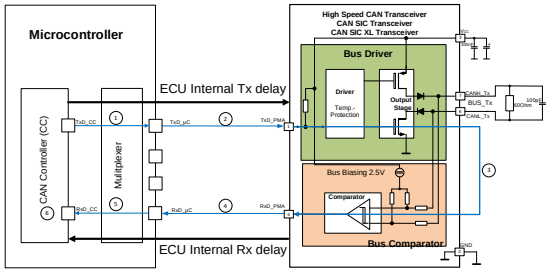

Figure1: Overall Loop delay of a transmitting node

1) Transmit path propagation delay from protocol handler to transceiver

This delay comprises the output driver delay of the host controller (where the CAN protocol layer is located), effects due to wiring and parasitics, such as capacitive loads, as well as the input stage of the transceiver device. In most cases, the output characteristics of the output driver can be configured in the host controller. The delays are given in the related section of a data sheet. Depending on the configuration of the host controller and the resulting capacitive load (incl. output driver capacitance, wiring/package capacitance and input stage capacitance), output driver delay may be adjusted in a range … (see example in data sheet)

2) Loop delay of a CAN Transceiver

The loop delay is the delay between the TxD input signal and the RxD output signal of a transmitting Transceiver

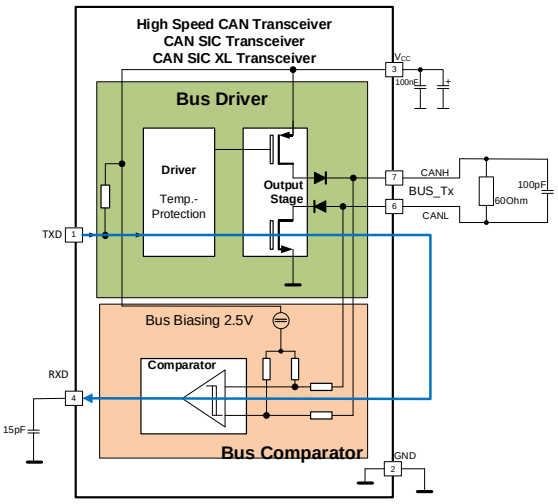

Figure 2: Transceiver Loop delay symmetry test circuitry

Figure 2 illustrates the test circuitry of the loop delay. Differences in the resistive or load conditions on the bus pins CANH and CANL as well as a different capacitive load on RxD Pin have an impact on the loop delay. Figure 3 shows the specification of the loop delay. The trigger level for the recessive to dominant edge is specified to 30% and for the dominant to recessive edge to 70% of the supply voltage of the transceiver device. *Figure* shows how the loop delay is specified. The symmetry of these both delays is very important for the transmitting node and there may be different values for a both edges. This part of the loop delay is specified for a 60Ohm load resistance on CANH to CANL and in parallel with 100pF capacitance to represent the capacitance of a bus wire.

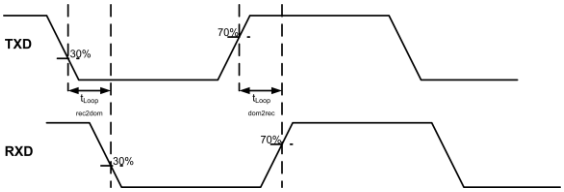

Figure3: Transceiver Loop delay specification

The loop delay for Transceiver is specified in the ISO 11898-2:2024.

CAN FD Transceiver:	255ns
CAN SIC Transceiver:	190ns
CAN SIC XL Transceiver:	190ns

These limits are valid for the indicated test setup condition, but in reality, these values depend on the implementation of the differential signals on the bus.

If there is ringing on the bus (due to signal reflections) the loop delay might be faster compared with the delay measured with the test setup condition, and in case of high capacitive load or plateau effects, the loop delay might be longer.

3) Receive path propagation delay from transceiver to protocol handler

This delay comprises the output driver delay of the transceiver device, effects

due to wiring and parasitics, such as capacitive loads, as well as the input stage of the host controller. The loop delay of the Transceiver is specified for a parasitic capacitance of 15pF on the RXD output pin.
This parasitic cap reflects the capacitance of the ECU layout traces and the input capacitance of the RXD port of the host controller.
A typical number for this parasitic capacitance of traces are 1pF/cm. The input capacitance of Aurix microcontroller RXD pin (TC2 and TC3) are 7pF.
This ends in a maximum distance between microcontroller and Transceiver of max 8 cm.
For higher capacitive load a higher delay has to be considered, but is not specified in transceiver datasheet.

4) Synchronization delay for the CAN controller

The received CAN signal is asynchronous to the internal clock of the CAN protocol handler. It gets synchronized, resulting in a delay of up to 2 clock periods of the protocol handler clock.

The synchronization delay of protocol handler clocked with a frequency of 40 MHz might be up to 50ns long and in case of a 80MHz clock frequency up to 25ns.

Overall loop delay

The overall loop delay is now the sum of all delays described above (please update).

A calculation example:

	Kind of delay	Delay CAN FD Transceiver	Delay CAN SIC Transceiver	Comment
1	CAN controller to TXD port	25ns	25ns	
2	Microcontroller TXD Port to Transceiver TXD Pin	15ns	15ns	C_{TxD}≤ 25pF
3	Transceiver loop delay	255ns	190ns	R_L=60Ω C_L=100pF
4	Transceiver RXD Pin to microcontroller RXD port	0ns	0ns	C_{RxD} ≤ 15pF
5	RXD port to CAN controller	25ns	25ns	
6	Synchronization delay	50ns	50ns	2 clock cycles @ 40MHz
	Overall loop delay	**370ns**	**305ns**	

Summary

The overall loop delay is more than the transceiver loop delay. For a proper setup of a CAN bus system, also the “digital” delays between a protocol handler and a transceiver device should be considered.

The calculation example in this article has been done without galvanic isolation elements.

The propagation delay of galvanic isolation elements has to be added in the propagation delay of 2) Microcontroller TXD port to Transceiver TXD Pin and 4) Transceiver RXD Pin to microcontroller RXD port.

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References

[1] ISO 11898-2, Road Vehicles-controller area network (CAN)- Part 2: High-speed physical media attachment (HS_PMA).

[2] CiA 601, CAN with flexible data rate (CAN FD) Part 1: Physical interface implementation

[3] The Physical Layer in the CAN FD world.
CAN conference paper Paris 2013
Author Magnus-Maria Hell

[4] The Physical Layer in the CAN FD world.
CAN FD Tech Day presentation.
Author: Magnus Maria Hell

[5] Application Note TLE9250G and TLE9251G