Operation and modeling analysis of a bidirectional CLLC converter

REF-DAB11KIZSICSYS: An example of the 11 kW bidirectional design

About this document

Scope and purpose

This application note provides an analysis of the design for an 11 kW bidirectional resonant CLLC (Capacitor-Inductor-Inductor-Capacitor) converter. This converter is used for bidirectional power conversion, with varying power capabilities in the forward and reverse directions of the power flow modes, based on its inductor and capacitor values. Furthermore, the document discusses the modeling of a CLLC converter that consists of an integrated constant current (CC) mode and a constant voltage (CV) mode. To increase the efficiency of this converter, the design incorporates Infineon's 1200 V SiC MOSFET (IMZ120R030M1H) switches. These switches are chosen for their superior performance compared to traditional silicon switches. Additionally, this document discusses synchronous rectification for controlling the secondary side of switches, which further enhances efficiency and reliability by operating under ZVS (Zero Voltage Switching) or ZCS (Zero Current Switching) condition. Finally, PLECS simulation results are presented for CC and CV modes, demonstrating the high efficiency of this design approach.

Overall, this document provides valuable insights into the design and analysis of bidirectional resonant CLLC converters for energy storage applications, showcasing the benefits of using advanced components and control techniques to achieve high efficiency.

Intended audience

The intended audiences for this document are design engineers, technicians, and developers of electronic systems.

Table of contents

1 Introduction

The application note discusses the working principles and gain properties of an isolated bidirectional DC-DC CLLC resonant converter for both powering (forward) and reverse (backward) modes. This converter topology is particularly suitable for applications such as rechargeable energy storage systems (ESS), DC electrification systems, and renewable energy systems (RES) within micro-grids.

This document also includes an analysis of an 11 kW bidirectional CLLC resonant converter operating at 73 kHz with silicon carbide (SiC) devices [1]. It discusses the design of resonance parameters and the incorporation of synchronous rectification (SR) for further improving the efficiency.

It also elaborates on the overall control block diagram of the system, which integrates constant current (CC), and constant voltage (CV) modes. PLECS simulation results are provided to demonstrate the performance and reliability of the design. Overall, this document provides comprehensive insights into the design and implementation of CLLC converters for various high-power applications within micro-grid systems.

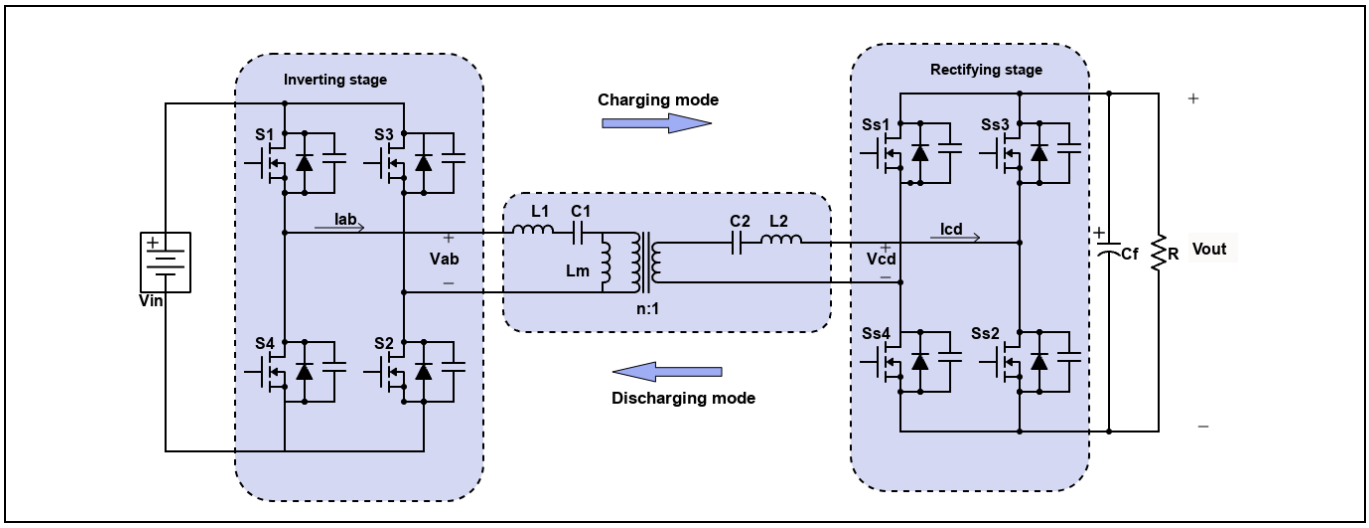


Figure 1 A bidirectional full-bridge CLLC resonant converter

2 Operating principles and gain analysis of a CLLC resonant converter

This section provides an analysis of the operating principles and gain of a CLLC resonant converter for both forward and reverse modes. The CLLC converter is made up of two individual LC (inductor-capacitor) resonant tanks that are connected to the primary and secondary sides of a high-frequency transformer (HFT). It can operate in both symmetrical and asymmetrical configurations with full-bridge primary inverting and secondary rectifying stages, as shown in Figure 1. The inverting stage generates a square waveform to excite the CLLC resonance tank, which can then generate a sinusoidal current waveform that can be scaled according to the transformer ratio of HFT as discussed in [2]. Later, it is rectified by a rectifying circuit. A filter capacitor is connected to reduce the ripple factor in the output waveform.

2.1 Operating principles of a CLLC converter

This section describes how a CLLC converter operates. The converter has three operating states for one half of the switching cycle. For the other half, the same states are repeated with different switches. Figure 5 shows the gate pulses and current waveforms of a CLLC converter.

- **State 1($t_a - t_b$):** This state is also known as the power transfer state. During this state, the primary side turns on switches S_1 and S_2 to deliver power to the secondary side, as shown in Figure 2. Then, the switch Ss_3 and Ss_4 rectify the power through the HFT. In this mode, the primary current, I_{ab}, flows in the negative direction, but the positive voltage, V_{ab}, forces it in the positive direction. The energy stored in the magnetizing inductance, L_m , increases linearly, which is why it does not participate in resonance. Power is transferred from the primary side to the secondary side when I_{ab} is greater than I_{Lm}. Once I_{ab} meets I_{Lm}, this mode ends. The secondary- side resonant current, I_{cd}, is the difference between I_{ab} and I_{Lm}.

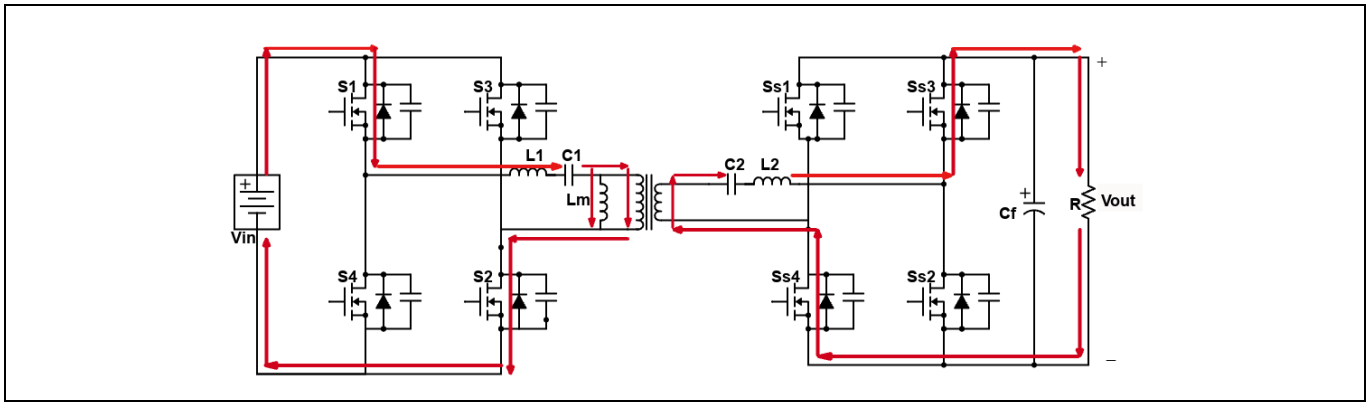


Figure 2 State-1 Power transfer state

- **State 2 ($t_b - t_c$):** This state is also known as the freewheeling state. In this state, the energy of the magnetizing inductance, L_m , gradually increases until the switches S_1 and S_2 are turned off, and the current on the secondary side of the transformer becomes zero, indicating that there is no output current ($I_{cd} = 0$), as shown Figure 3. This period only occurs when the switching frequency, f_s, is less than the resonant frequency f_r, which is further explained in Table 1.

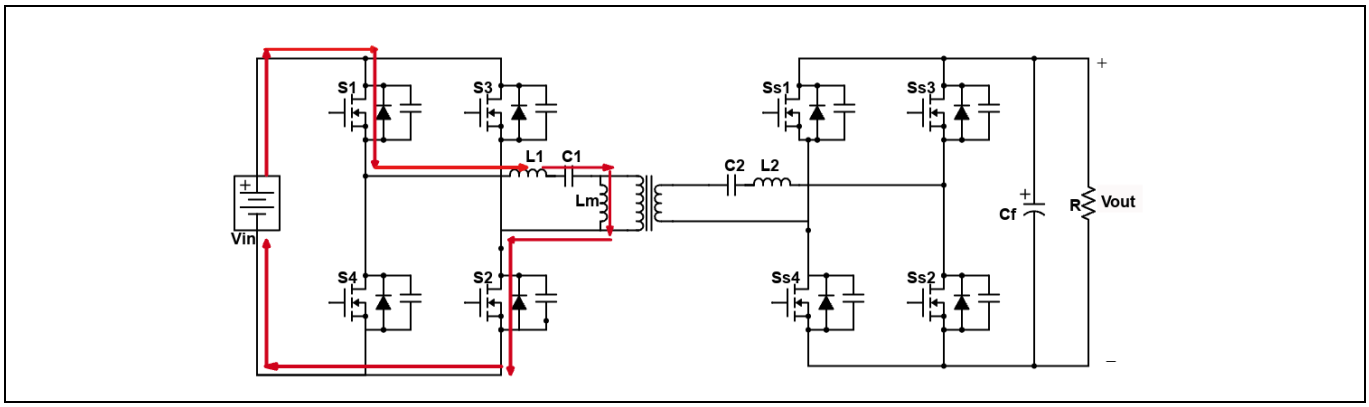


Figure 3 State-2 Freewheeling mode

- **State 3 $(t_c - t_d)$:** This duration is also known as the dead time duration. The internal capacitance of the primary switches is charged and discharged to turn them off and on, as shown in Figure 4. During this period, all the switches are in the OFF condition to prevent shoot-through currents. Switches S_1 and S_2 are charged to turn off, while switches S_3 and S_4 are discharged through their internal diodes. The primary current, I_{ab}, passes through the anti-parallel diodes of switches S_3 and S_4 .

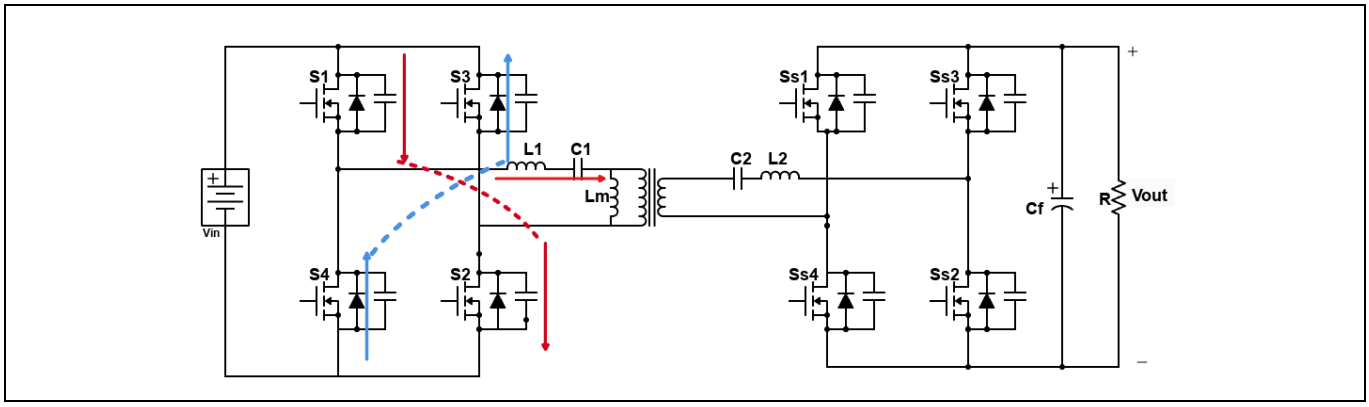


Figure 4 Mode-3 Dead time duration

Figure 5 represents the waveform of the switches' (S1 and S2) gate pulses, input current (I_{ab}), current flowing through magnetizing inductance (I_{Lm}), and output current (I_{cd}) for all the modes of operation with their time duration. It also represents all the states with their time intervals.

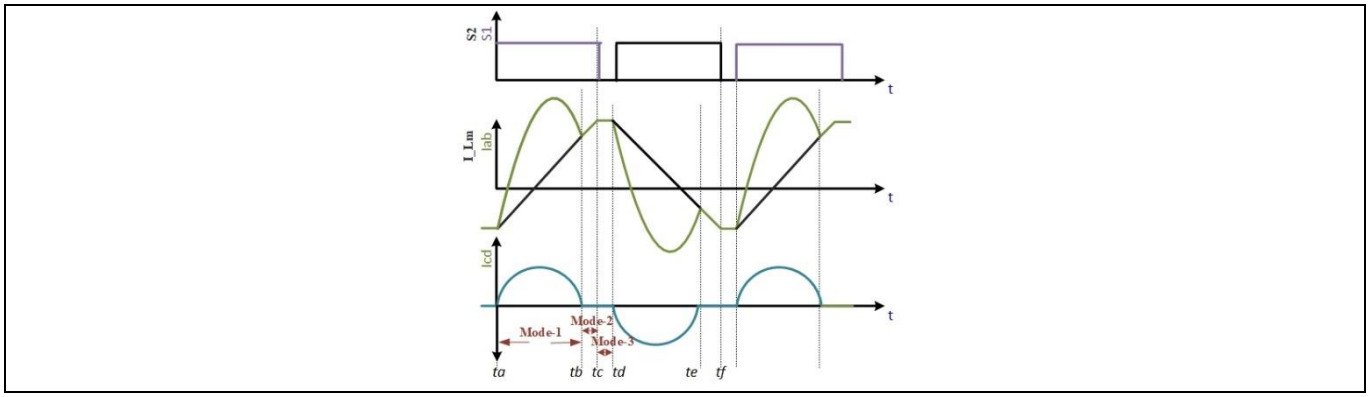
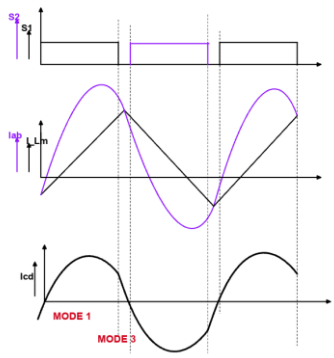
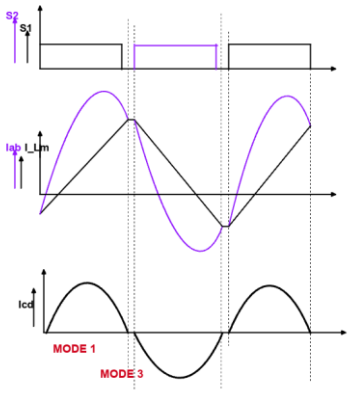
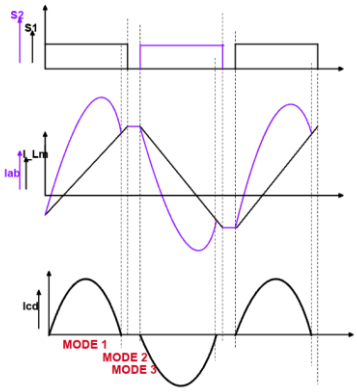


Figure 5 (i) Switches gate pulses, (ii) Input current and current flowing through magnetizing inductance, (iii) output current of CLLC resonant tank

Table 1 **Effects of the switching frequency**

$f_s > f_r; T_s < T_r$	$f_s = f_r; T_s = T_r$	$f_s < f_r; T_s > T_r$
Buck mode	**Resonant mode**	**Boost mode**
In this mode, one half of the switching cycle gets interrupted by the next half cycle. This is why it can only deliver partial power to the secondary side and the freewheeling mode gets eliminated. This increases the loss in the converter across the primary side of MOSFET and gives a hard commutation on the secondary side of MOSFET. Therefore, the CLLC converter operates for a step-down gain or in the buck mode.	In this mode, half of the switching cycle gets completed as a resonant cycle. This is why it can deliver power completely to the secondary side of the converter. Also, the freewheeling mode is eliminated here. This mode offers gain depending on the transformation ratio to the converter with high efficiency.	In this mode, half of the switching cycle gets completed within half the resonant cycle. After completing a resonant cycle, it follows the freewheeling mode until the switching cycle is completed. The primary side of the converter has more conduction losses because of the freewheeling mode. Therefore, the CLLC converter operates for a step-up gain or in the boost mode.
 The sinusoidal half waveform of the secondary-side current, I_{cd}, is interrupted by another half cycle at the end of mode 1.	 The secondary-side current, I_{cd}, is a smooth sinusoidal waveform with dead time duration.	

2.2 Voltage gain analysis of a CLLC converter based on the FHA method

First harmonic approximation (FHA) is a modelling technique used for analyzing the performance of resonant power converters. The assumption is that only the first harmonic signals contribute to the power transfer especially in the CLLC resonant converter.
Figure 6 represents the FHA for input and output voltage.

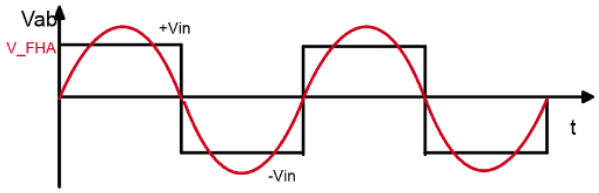


Figure 6 The sinusoidal approximation for an FHA analysis

$v_{ab}(t) = \frac{4}{\pi} V_{in} \sum_{m=1,3,5\ldots} \frac{1}{n} \sin(2m\pi f_s t);$

The fundamental component of v_{ab} is obtained by Fourier expansion (m = 1),

$v_s(t) = \frac{4}{\pi} V_{in} \sin(2\pi f_s t);$

Magnitude of $V_s = \frac{2\sqrt{2}}{\pi} V_{in}$

Similarly, the magnitude of the output voltage, $V_o = \frac{2\sqrt{2}}{\pi} V_{out}$

With the resistance power equation i.e., output equivalent resistance,

$R_{o\_eq} = \frac{(V_o)^2}{P_{out}} = \frac{(\frac{2\sqrt{2}}{\pi} V_{out})^2}{V_{out} * I_{out}} = \frac{8}{\pi^2} R;$

Output equivalent resistance referred to the primary side is $R_o = \frac{8n^2}{\pi^2} R$

This equivalent resistance is calculated for the forward mode. Similarly, equivalent resistance for the backward mode can also be calculated using FHA modelling.

$$R_o = \frac{8n^2}{\pi^2} R \; ; R'_o = \frac{8}{\pi^2 n^2} R$$

Equation 1 FHA modelling of AC resistance of circuit

Its resonant components L_1, L_2, L_m, C_1, and C_2 are independent of each other maintaining resonant frequency constant for both forward and backward modes i.e., $L_1 \neq n^2 L_2$ and $C_1 \neq \frac{C_2}{n^2}$ for the forward mode and vice-versa for the backward mode.

2.2.1 Voltage gain for forward (charging) mode

During the charging mode, the voltage gain analysis of an equivalent circuit of the CLLC converter is performed in the frequency domain, as shown in Figure 7.

These equations are represented in terms of quality factor (Q), transformation ratio (n), resonant inductor ratio (a), resonant capacitor ratio (b), inductance ratio (K), angular resonant frequency ω_r, and angular switching frequency ω_s.

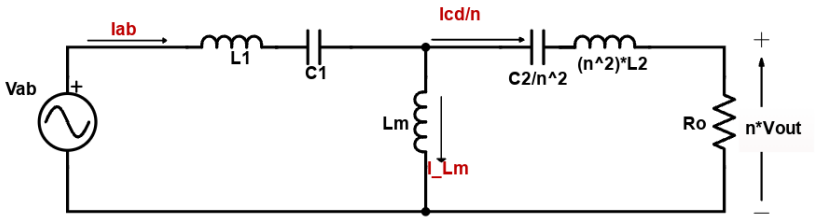


Figure 7 The equivalent circuit diagram for the charging mode referred to the primary side

$$Z_1 = sL_1 + \frac{1}{sC_1}; Z_2 = n^2\left(sL_2 + \frac{1}{sC_2}\right); Z_m = sL_m;$$

Input impedance, $Z_{IN} = \frac{V_{ab}}{I_{ab}} = Z_1 + ((Z_2 + R_o)||Z_m)$

By applying the voltage division rule:

$$\frac{nVout}{Vin} = \frac{Z_m||(Z_2+R_o)}{Z_1+Z_m||(Z_2+R_o)} * \frac{R_o}{Z_2+R_o};$$

$$\frac{nV_{out}}{Vin} = \frac{Z_m*R_o}{Z_1*Z_m+Z_1*Z_2+Z_1*R_o+Z_m*Z_2+Z_m*R_o};$$

$$\frac{nV_{out}}{V_{in}} = \frac{s^3\left(\frac{C_1C_2R_oL_m}{n^2}\right)}{s^4\left(L_1C_1L_2C_2+L_2C_2C_1L_m+\frac{L_1C_2C_1L_m}{n^2}\right)+s^3\left(\frac{L_1C_1C_2R_o}{n^2}+\frac{C_2C_1L_mR_o}{n^2}\right)+s^2\left(\frac{L_mC_2}{n^2}+L_2C_2+L_1C_1+C_1L_m\right)+s\left(\frac{C_2R_o}{n^2}\right)+1};$$

$$\frac{nV_{out}}{V_{in}} = \frac{s^3\left(\frac{k\sqrt{\frac{b}{a}}}{\omega_{r1}^2\omega_{r2}Q}\right)}{s^4\left(\frac{1+k+k/a}{\omega_{r1}^2\omega_{r2}^2}\right)+s^3\left(\frac{\sqrt{\frac{b}{a}}}{\omega_{r1}^2\omega_{r2}Q}(1+k)\right)+s^2\left(\frac{1+k}{\omega_{r1}^2}+\frac{1+k/a}{\omega_{r2}^2}\right)+s\left(\frac{\sqrt{\frac{b}{a}}}{\omega_{r2}Q}\right)+1};$$

$$a = \frac{n^2L_2}{L_1}; b = \frac{C_2}{n^2C_1}; Q = \frac{\sqrt{L_1/C_1}}{R_o}; k = \frac{L_m}{L_1}; \omega_{r1} = \frac{1}{\sqrt{L_1C_1}}; \omega_{r2} = \frac{1}{\sqrt{L_2C_2}}; s=j\omega_s$$

For $\omega_{r1} = \omega_{r2}$, $ab = 1$

$$\frac{nV_{out}}{V_{in}} = \frac{s^3\left(\frac{k}{\frac{a}{\omega_{r1}^3Q}}\right)}{s^4\left(\frac{1+k+k/a}{\omega_{r1}^4}\right)+s^3\left(\frac{b}{\omega_{r1}^3Q}(1+k)\right)+s^2\left(\frac{2+k+k/a}{\omega_{r1}^2}\right)+s\left(\frac{b}{\omega_{r1}Q}\right)+1}$$

Equation 2 Voltage gain equation for charging mode.

In Equation 2, it is observed that forward voltage gain transfer function depends mainly on the quality factor, Q, and inductance ratio, k. The effective quality factor relates to the characteristic impedance ($Z_s = \sqrt{L_1/C_1}$) with the effective load resistor (Ro) which is calculated using the FHA method considering the transformer-transfer ratio, n.

The gain versus switching frequency (f_s) curve is plotted keeping the quality factor (Q) fixed and varying the inductance ratio (k), and vice versa. The graph is presented in Figure 8.

- **Constant Q and varying k**: It can be observed that small k values give maximum gain nearer to the resonant frequency. In narrow frequency ranges, all gain values from maximum to minimum can be obtained. But small k values refer to small magnetizing inductance (L_m) that can bring some drawbacks regarding peak-to-peak current ripple. Also, during sudden load variations there is a chance that the CLLC converter operates in the capacitance region, which can increase losses and decrease efficiency. With high k values i.e., high magnetizing inductance (L_m), the converter can operate in a wider range of frequencies. It can also add some drawbacks such as bulkiness of the transformer and difficulties in achieving the required maximum gain. This the why the medium range of k value should be determined.
- **Constant k and varying Q**: For high values of Q, there is a shrink between two gain points, which can be fixed by changing the value of k. This also provides a narrow range of operating frequency. On the other hand, small values of Q provide a monotonic gain for the converter.

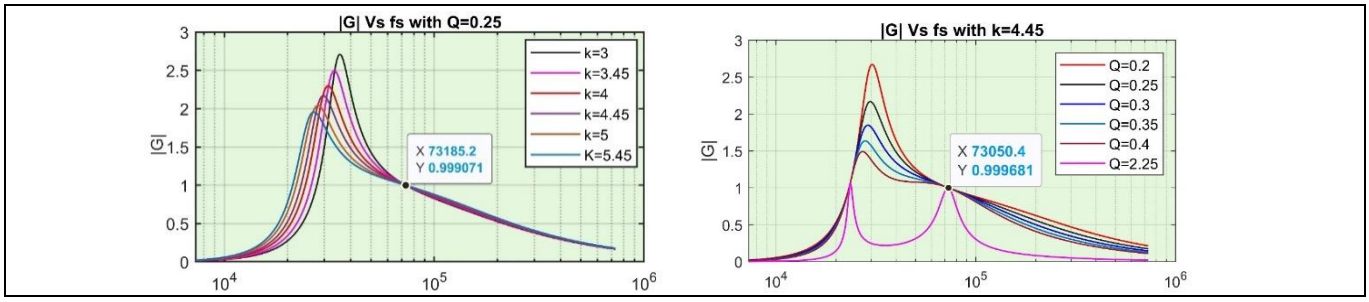


Figure 8 Voltage gain curves for different k and Q values

2.2.2 Voltage gain for reverse (discharging) mode

Voltage gain for the discharging mode [2] can be calculated in the same manner as for the charging mode. The equivalent circuit diagram for discharging mode is shown in Figure 9. Following the same procedures as in Section 2.2.1 , the equations come out to be:

$$a' = \frac{L_1}{n^2 L_2};\ b' = \frac{n^2 C_1}{C_2};\ Q' = \frac{\sqrt{L_2/C_2}}{R_o'};\ k' = \frac{L_m}{n^2 L_2};\ \omega_r = \frac{1}{\sqrt{L_2 C_2}};\ s=j\omega_s$$

$$\frac{V_{out}}{nV_{in}} = \frac{s^3\left(C_1 C_2 R_o' L_m\right)}{s^4\left(\frac{L_1 C_1 L_m C_2}{n^2}+L_1 C_1 L_2 C_2+L_2 C_2 C_1 L_m\right)+s^3\left(n^2 L_2 C_1 C_2 R_o'+C_2 C_1 L_m R_o'\right)+s^2\left(L_m C_1+\frac{L_m C_2}{n^2}+L_2 C_2+C_1 L_1\right)+s\left(n^2 C_1 R_o'\right)+1};$$

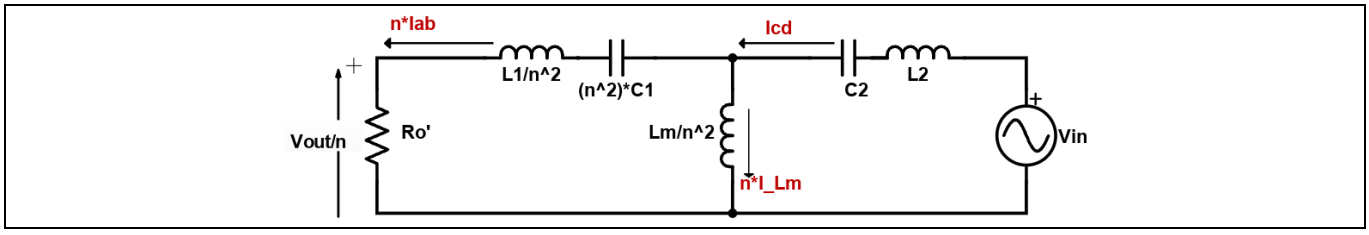


Figure 9 The equivalent circuit diagram for the discharging mode referred to the secondary side

$$\frac{V_{out}}{nV_{in}} = \frac{s^3\left(\frac{k'b'}{\omega_r^3 Q'}\right)}{s^4\left(\frac{1+k'+k'/a'}{\omega_r^4}\right)+s^3\left(\frac{b'}{\omega_r^3 Q'}(1+k')\right)+s^2\left(\frac{b'}{\omega_r^2}(2+k'+k'/a')\right)+s\left(\frac{b'}{\omega_r Q'}\right)+1}$$

2.3 Design specifications

The required design specifications for a full-bridge CLLC converter are listed in Table 2.

Table 2 Design specifications for a CLLC converter

S. No.	Specifications	Range	Nominal values
1	Bus voltage	700V – 800V	750 V
2	HV electronic load	550V – 800V	600 V
3	Natural resonant frequency	73 KHz	-
4	Output power	11 kW	-

The following steps describe how to design the resonant parameters for an 11 kW CLLC converter:

Step: 1 Calculating the turn ratio for the transformer

Transformer turn ratio for forward mode, $n_f = \frac{V_{in_{nominal}}}{V_{out_{nominal}}} = \frac{750}{600} = 1.25;$

Transformer turn ratio for reverse mode, $n_r = \frac{V_{in_{nominal}}}{V_{out_{nominal}}} = \frac{600}{750} = 0.8;$

Step: 2 Calculating the minimum and maximum voltage gain

For forward mode:

Minimum voltage gain, $M_{g_{min}} = \frac{n_f * V_{out_{min}}}{V_{in_{max}}} = \frac{1.25*550}{800} = 0.86;$

Maximum voltage gain, $M_{g_{max}} = \frac{n_f * V_{out_{max}}}{Vs_{in_{min}}} = \frac{1.25*800}{700} = 1.43 \cong 1.5;$

For reverse mode:

Minimum voltage gain, $M_{g_{min}} = \frac{n_r * V_{out_{min}}}{V_{in_{max}}} = \frac{0.8*700}{800} = 0.7;$

Maximum voltage gain, $M_{g_{max}} = \frac{n_r * V_{out_{max}}}{V_{in_{min}}} = \frac{0.8*800}{550} = 1.164;$

Step: 3 Choosing the k and Q factors

With the k value constant at 4.45, the Q factor can vary between 0.2 and 0.4, while the gain can vary from 0.86 to 1.5 as shown in Figure 10. This requires a minimum frequency of 40 kHz and a maximum frequency of 250 kHz.

Step: 4 Calculating the effective resistance, R_0

Effective resistance, $R_o = \frac{8n^2}{\pi^2} R_L = \frac{8*1.25^2}{\pi^2} \frac{V_o^2}{P} = \frac{8*1.25^2}{\pi^2} \frac{600^2}{11000} = 41.45 \text{ ohms};$

Step: 5 Calculating the resonant capacitor, C_1

Resonant capacitor, $C_1 = \frac{1}{2\pi Q f_r R_o} = \frac{1}{2*\pi*0.3984*73*10^3*41.45} = 132 \text{ nF};$

Step: 6 Calculating the resonant inductor, L_1

Resonant inductor, $L_1 = \frac{1}{(2\pi f_r)^2 C_1} = \frac{1}{(2*\pi*73*10^3)^2*132*10^{-9}} = 36 \text{ µH};$

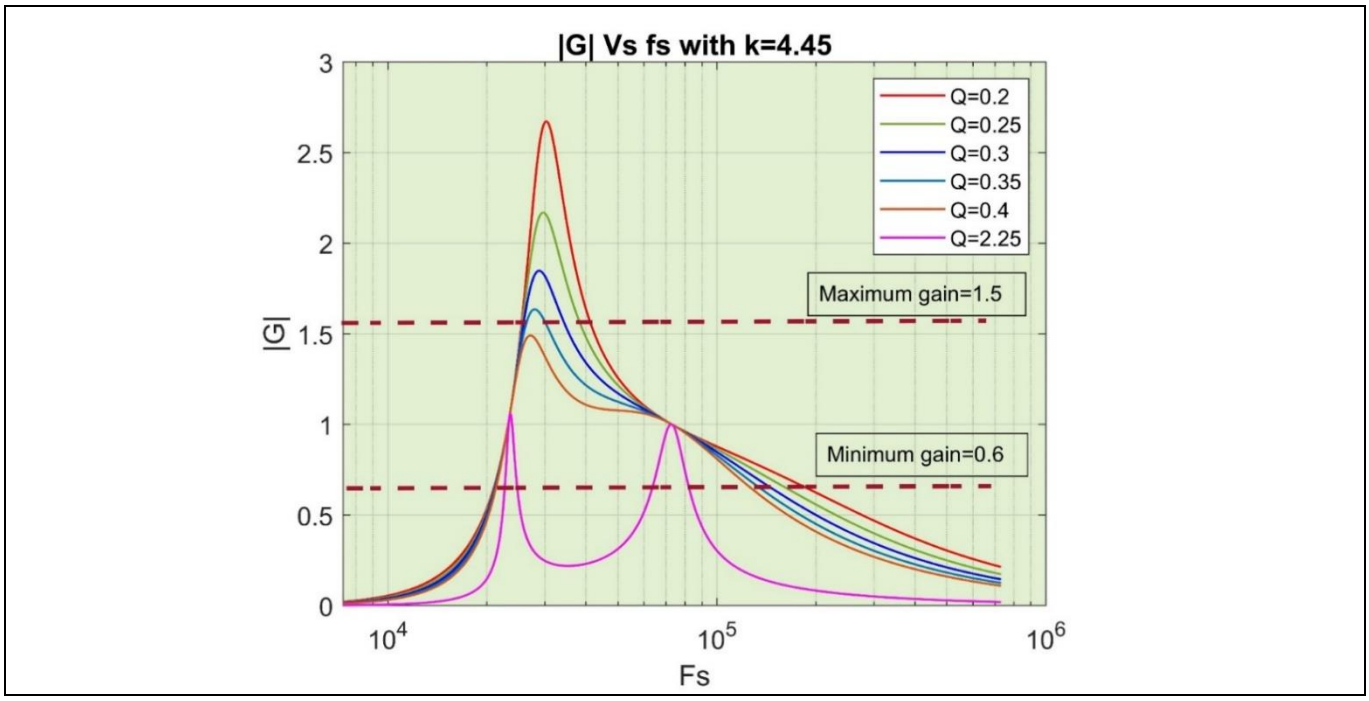


Figure 10 The gain versus frequency curve showing the minimum and maximum gain and frequency

Step: 7 Calculating magnetizing inductance, L_m

Magnetising inductance, $L_m = k * L_1 = 4.45 * 36 * 10^{-6} = 160.2\ \mu H$

Step: 8 Assuming a and b values

Resonant inductor ratio a = 0.95
Resonant capacitor ratio b = 1.052

Step: 9 Calculating the secondary-side resonant inductor (L_2) and capacitor (C_2)

$$L_2 = \frac{aL_1}{n^2} = \frac{0.95 * 36 * 10^{-6}}{1.25^2} = 22\mu H$$

$$C_2 = n^2 b C_1 = 1.25^2 * 1.052 * 132 * 10^{-9} = 216\ nF$$

Step: 10 Calculating the input current, I_{ab}

Input peak current, $I_{ab_p} = \frac{V_{abp}}{|Z_{in}|} = \frac{V_{in}}{|Z_{in}|}$

For resonant inductors and capacitors calculated above,

$$Z_{in} = \frac{3.176*10^{-29}s^5+3.192*10^{-23}s^4+7.285*10^{-18}s^3+1.234*10^{-12}s^2+1.387*10^{-7}s}{4.904*10^{-25}s^4+1.628*10^{-19}s^3+1.822*10^{-14}s^2}$$

From minimum and maximum frequency, the input impedance will be:

$Z_{in} at\ (40\ kHz) = 26.0956\angle 26.986\Omega$ and $Z_{in}(at\ 250\ kHz) = 123.568\angle 68.6833\ \Omega$

The input current at minimum and maximum frequency for input voltage $V_{in} = 800\ V$ will be:

$$I_{ab_p}(at\ 40kHz) = \frac{800}{26.0956} = 30.6565\ Amps \quad \& \quad I_{ab_p}(at\ 250kHz) = \frac{800}{123.568} = 6.4741\ Amps$$

Step: 11 Calculating the voltage stress across resonant capacitors and inductors at 40 kHz

$$V_{C1} = \frac{I_{ab_{rms}}}{2*\pi*f_s*C_1} = \frac{30.6565/\sqrt{2}}{2*3.14*40*10^3*132*10^{-9}} = 653\ V$$

$$V_{C2} = \frac{I_{cd_{rms}}}{2*\pi*f_s*C_2} = \frac{I_{ab_{rms}}/n}{2*\pi*f_s*C_2} = \frac{\frac{30.6565}{\sqrt{2}}/1.25}{2*3.14*40*10^3*216*10^{-9}} = 319.61\ V$$

$$V_{L1} = 2*\pi*f_s*L_1*I_{ab_{rms}} = 2*3.14*40*10^3*36*10^{-6}*\frac{30.6565}{\sqrt{2}} = 196.03323\ V$$

$$V_{L2} = 2*\pi*f_s*L_2*I_{cd_{rms}} = 2*3.14*40*10^3*22*10^{-6}*\frac{30.6565}{\sqrt{2}*1.25} = 95.83V$$

2.4 Dead time calculation

In Section 2.2, the fundamental component of v_{ab} calculated by FHA analysis is obtained by Fourier expansion (m = 1):

$$v_s(t) = \frac{4}{\pi}V_{in}\sin(2\pi f_s t)$$

Similarly, the voltage across the magnetizing inductance, v_m, is also a square waveform and its fundamental component can also be determined with the phase difference of φ:

$$v_m(t) = \frac{4}{\pi}\left(\frac{\omega_s^{\frac{3}{2}}L_m\sqrt{C_1}}{\sqrt{(\omega_s/\omega_r)^2+1}}\right)V_{in}\sin(2\pi f_s t-\varphi)$$

Magnetizing inductance current $i_m(t) = \frac{v_m(t)}{\omega_s L_m}$;

$$i_m(t) = \frac{4}{\pi}\left(\frac{\sqrt{\omega_s C_1}}{\sqrt{(\omega_s/\omega_r)^2+1}}\right)V_{in}\sin(2\pi f_s t-\varphi)$$

During the duration of the dead time [3], the resonant current is equal to the magnetizing inductance current as described in mode 3 operation. The energy stored in the magnetizing inductance and resonant inductor is the energy required for charging and discharging the parasitic capacitor of the MOSFETs. During the duration of the dead time, the magnetizing current (I_m) circulates through the internal capacitances (C_{DS}) and the body diode of the primary-side MOSFETs. In dead time, the capacitances of the switches S_1 and S_2 get charged through the internal diode of S_3 and S_4. The resonant capacitor value is much larger than 2^*C_{DS}. The effect of resonant capacitors during the energy conversion can be ignored. The equivalent capacitor, C_{eq}, can be considered as parasitic capacitances only. For a ZVS operation, the parasitic capacitor of the primary switches should be completely charged and discharged.

The secondary side of the resonant is not included while calculating the dead time because in this mode the secondary-side current is zero i.e., no energy is flowing in the secondary circuit.

$$\frac{1}{2}(L_m + L_1) * {I_{m_{peak}}}^2 > \frac{1}{2}(2 * C_{DS}) * {V_{ab}}^2;$$

The discharge time of the parasitic capacitances:

$$t_{dis} > \frac{C_{DS} * V_{in}}{I_{m_{peak}}};$$

For security analysis, the turn-on and turn-off delay of the practical switches (IMZ120R030M1H) should be considered. To improve its applicability, the time delay (t_d) to prevent it from the simultaneous conduction of two switches in the same leg is calculated from the datasheet.

$$t_d = t_{d_{on}} + t_{rise} - t_{d_{off}} - t_{fall};$$

Where $t_{d_{on}}$ is the turn-on delay, t_{rise} is the rise time, $t_{d_{off}}$ is the tur-off delay, and t_{fall} is the fall time.

Body diode characteristics of the SiC MOSFETs also play a role here. Turning on the body diode can be easily affected by stray inductance. For calculating the dead time, the turn-on time of the diode cannot be neglected. So, the overall dead time for a full-bridge circuit that has two SiC MOSFETs turned on and off can be calculated as:

$$t_{dead} > 1.75 * 2 * (t_c + t_d + t_{diode})$$

Where 1.75 is considered for the increase factor that includes the effects of the FHA modeling.

From these calculations, a 300 nanoseconds dead time is provided in between the switching period.

3 Control strategies for a CLLC resonant converter

This chapter describes the control design aspect of a CLLC resonant converter. The control aspects mainly depend on the input and output parameters. The input and output parameters are voltage, current, and power. In a CLLC converter, the popular control strategies are CC and CV. Figure 11 shows the control loop of the system including constant current and constant voltage loop **Error! Reference source not found.**. The reference v oltage and reference current are compared with the output voltage and current respectively, and the error signals are sent to the voltage controller and current controller. They send the smaller value of the controller's output to the voltage-controlled oscillator (VCO). The VCO will output a drive signal with a variable frequency to realize the stable operation of the system.

For controlling the secondary-side switches, a theoretical angular shift is provided to the VCO-generated frequency. Turning on the secondary side of the switches is known as synchronous rectification which is explained in Section 3.3.

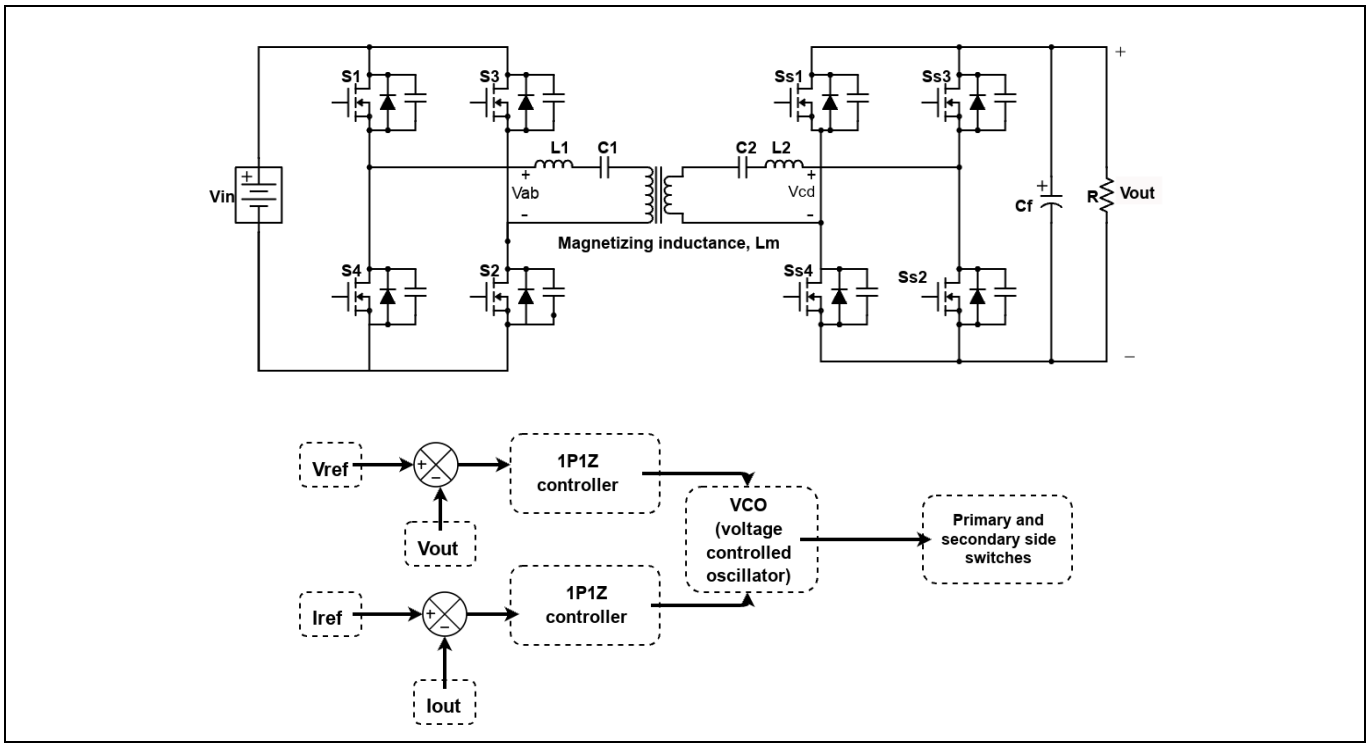


Figure 11 Control loop of the system

3.1 1P1Z controller design for the CV mode

Keeping all the calculated values from equation 2, the calculation comes out to be:

$$\frac{nV_{out}}{V_{in}} = \frac{s^3\left(\frac{21.29}{\omega_{r1}^3}\right)}{s^4\left(\frac{5.45}{\omega_{r1}^4}\right)+s^3\left(\frac{26.011}{\omega_{r1}^3}\right)+s^2\left(\frac{6.45}{\omega_{r1}^2}\right)+s\left(\frac{4.7818}{\omega_{r1}}\right)+1}$$

$$\frac{nV_{out}}{V_{in}} = \frac{-j{\omega_s}^3\left(\frac{21.29}{\omega_{r1}^3}\right)}{{\omega_s}^4\left(\frac{5.45}{\omega_{r1}^4}\right)-j{\omega_s}^3\left(\frac{26.011}{\omega_{r1}^3}\right)-{\omega_s}^2\left(\frac{6.45}{\omega_{r1}^2}\right)+j\omega_s\left(\frac{4.7818}{\omega_{r1}}\right)+1}$$

The location of the poles for the abovementioned transfer function IS (-2.76*10^4 ± i (1.58*10^5)) and (-2.89*10^5± i (3.01*10^5)) with a damping factor of 0.172 and 0.694 respectively.

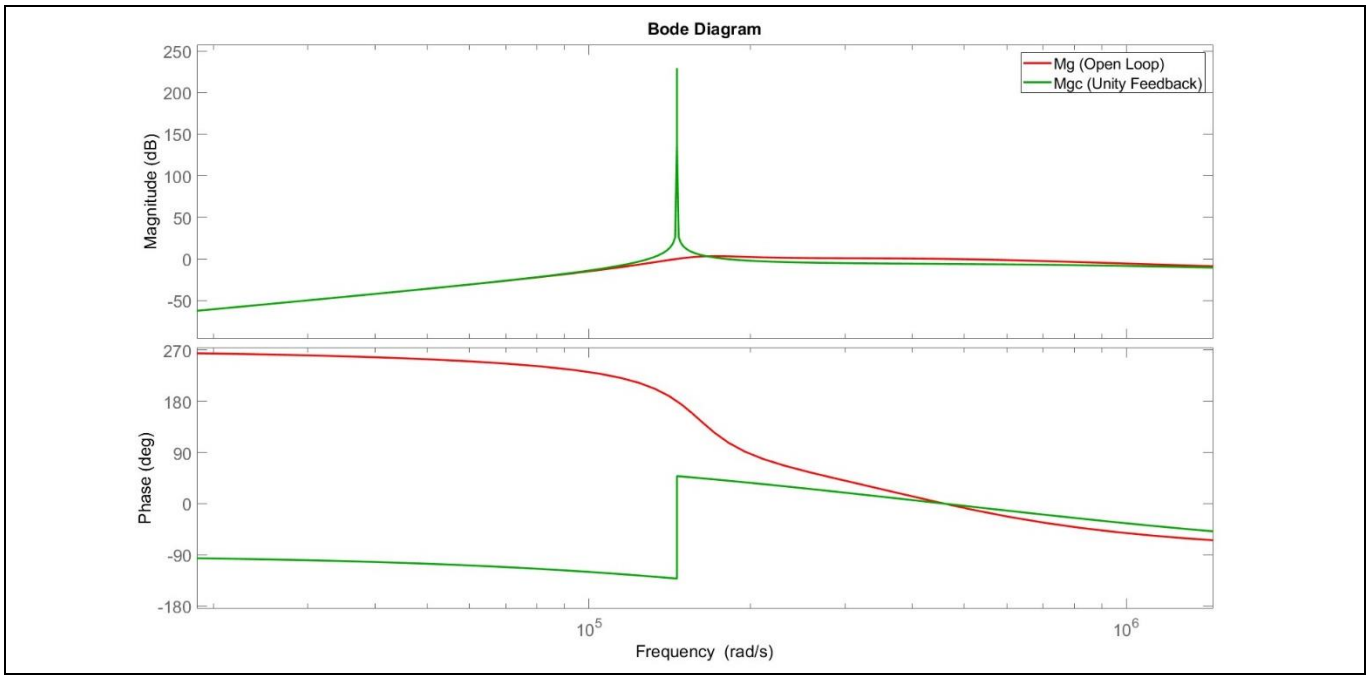


Figure 12 The Bode plot for an open loop and unity feedback closed loop transfer function

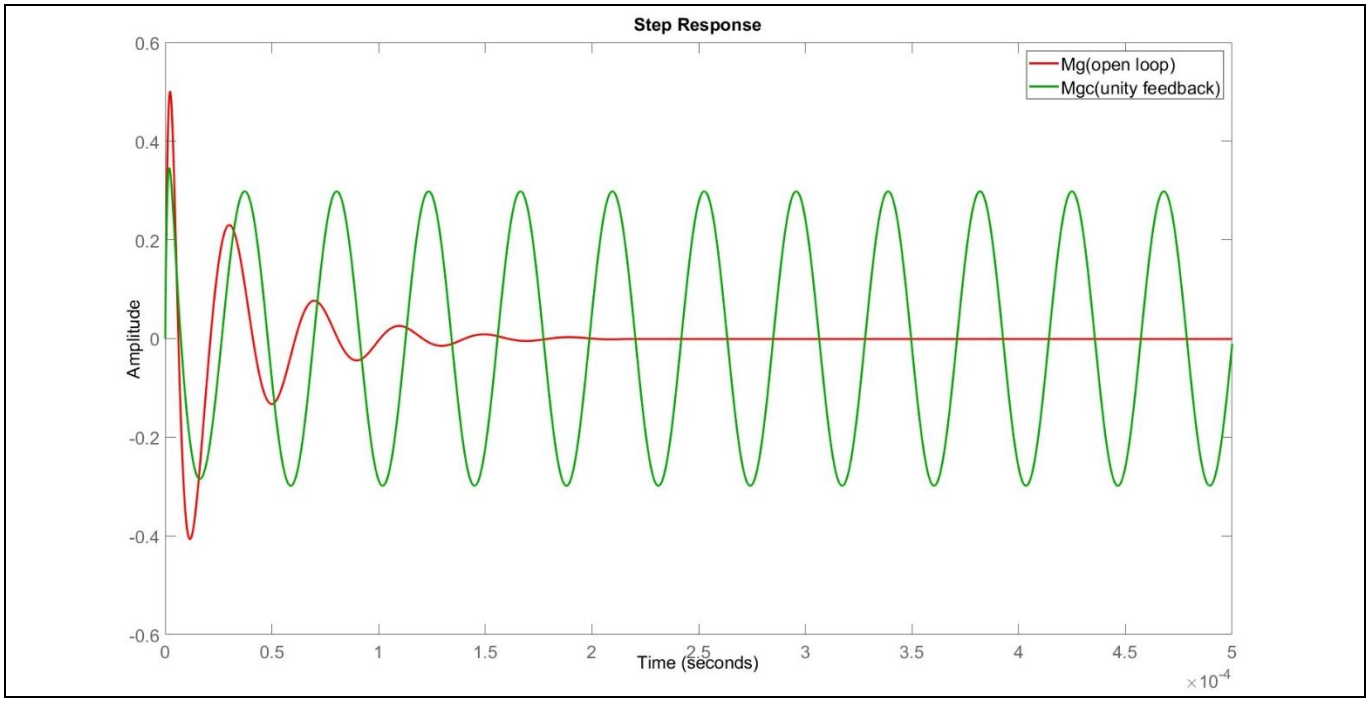


Figure 13 Step response for an open loop and unity feedback closed loop transfer function

The Bode plot of the open loop transfer function has gain margin at 0.00158 dB and phase margin at -0.006045°, as shown in Figure 12. The stable open loop step response indicates a well-behaved system. However, the closed loop transfer function with unity feedback and no controller exhibits instability, leading to sustained oscillations during the step response. Introducing a controller with 1 pole and 1 zero can be an effective

strategy to enhance the system's transient and steady-state response. This type of controller can help shape the closed-loop response to meet specific performance requirements and improve the overall stability of the system.

Controller transfer function, $G_C(s) = k\frac{s+z}{s+p}$

For simulation, the system stabilizes at k = 0.01, z = 200, and p = 0.01. Figure 15 depicts the Bode plot for an open loop transfer function ($^{nV_o}/_{V_{in}}$), controller transfer function ($G_c(s)$), and a closed loop transfer function. Figure 16 illustrates the step response of the closed-loop and open-loop transfer functions. To ensure stability and to achieve the desired performance, including phase margin and bandwidth, the gain crossover frequency is often set based on the desired control loop bandwidth, rather than be directly linked to the resonant frequency. This approach allows for a balanced design that can adequately reject disturbances while maintaining stability.

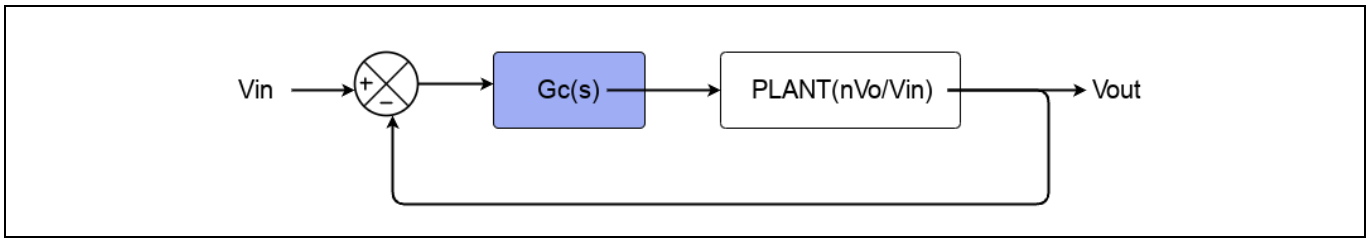


Figure 14 A compensated system

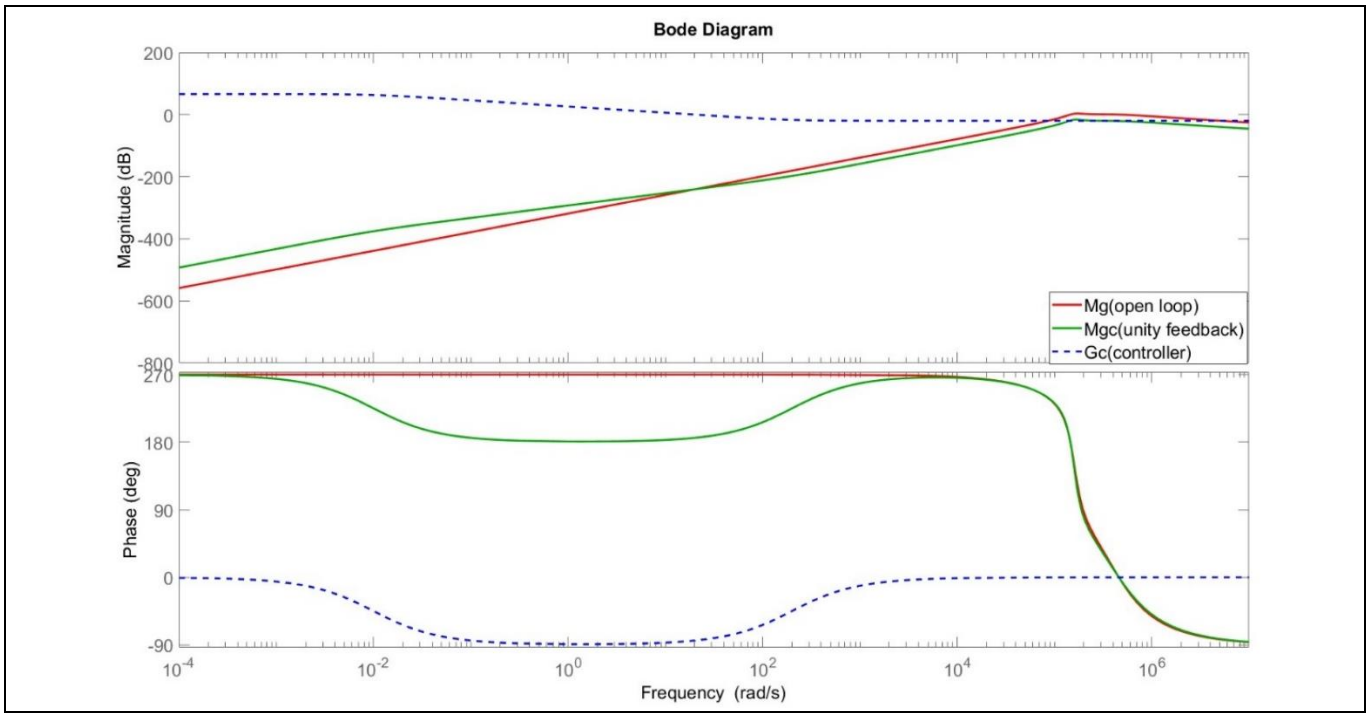


Figure 15 The Bode plot for an open loop, controller and a closed loop transfer function

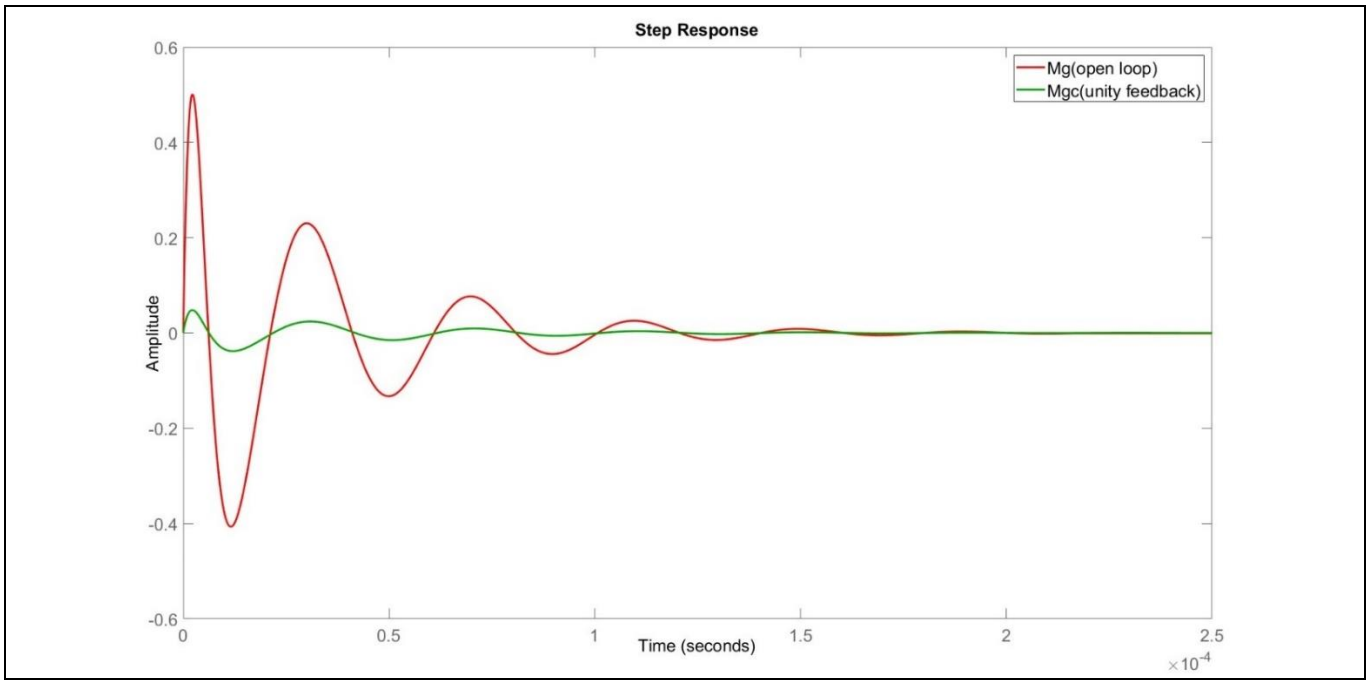


Figure 16 The step response for an open loop and closed loop transfer function

3.2 1P1Z controller design for CC mode

A PI-controller for CC mode in a CLLC converter involves setting the control parameters to regulate the output current to a desired value. Transfer function output current with respect to the input voltage is derived as follows:

$$\frac{I_{cd}}{nI_{ab}} = \frac{Z_m}{Z_m+Z_2+R_o} \,\&\, V_{ab} = (Z_1 + Z_m)I_{ab} - Z_m\frac{I_{cd}}{n}$$

From all above calculated values, the transfer function for $R_o = 73.7$ ohms is obtained.

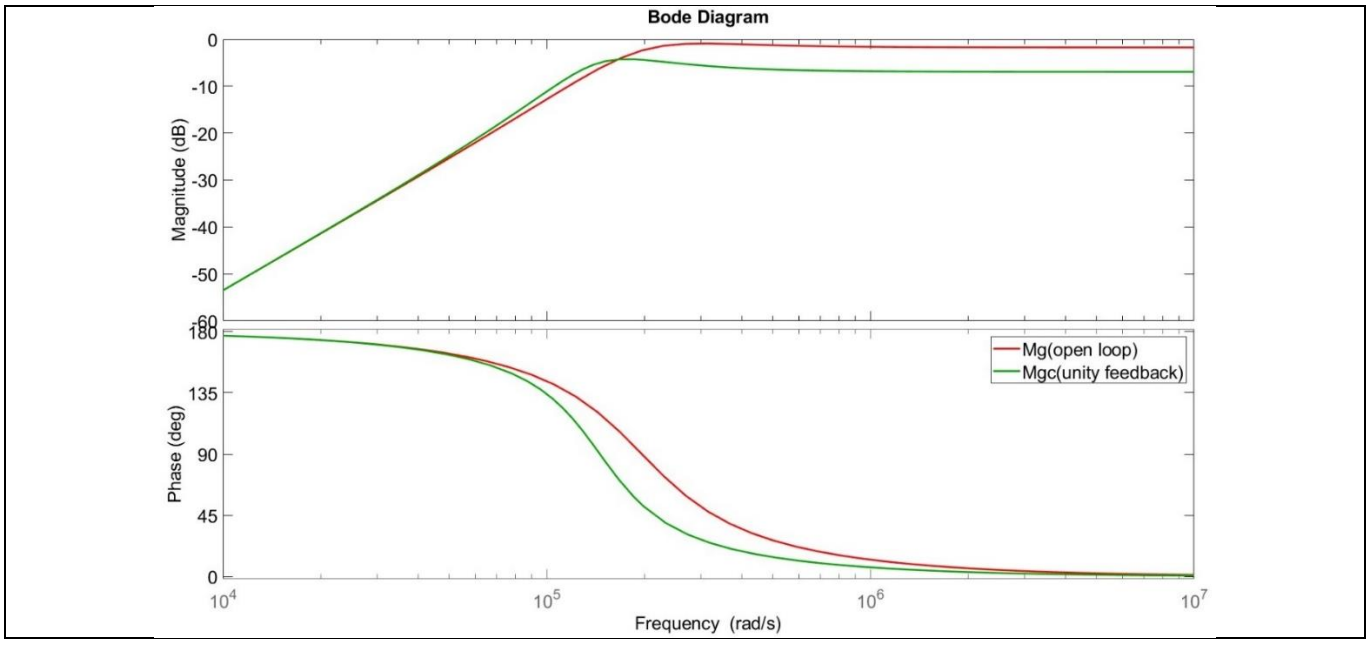


Figure 17 The Bode plot for an open loop and unity feedback closed loop transfer function

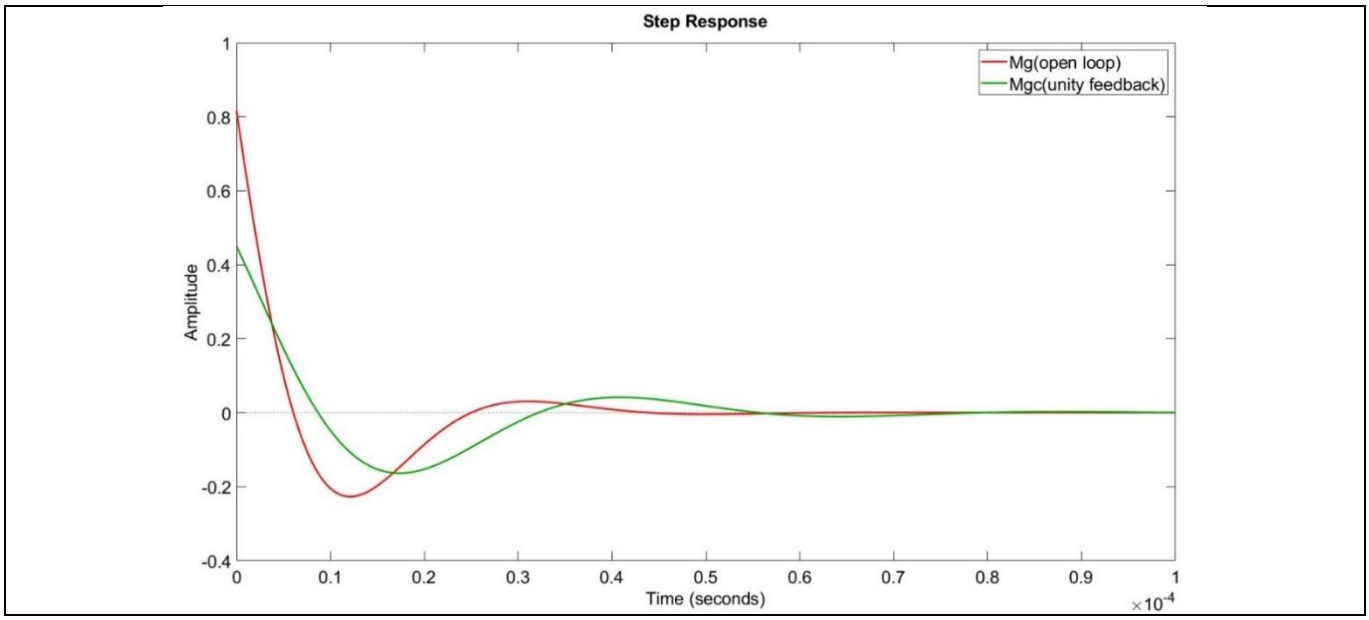


Figure 18 The step response for an open loop and unity feedback closed loop transfer function

The controller is designed in the same manner as discussed in Section 3.1.

Controller transfer function, $G_C(s) = k\frac{s+z}{s+p}$.

For simulation, the system stabilizes at k = 250, z = 400, and p = 1.

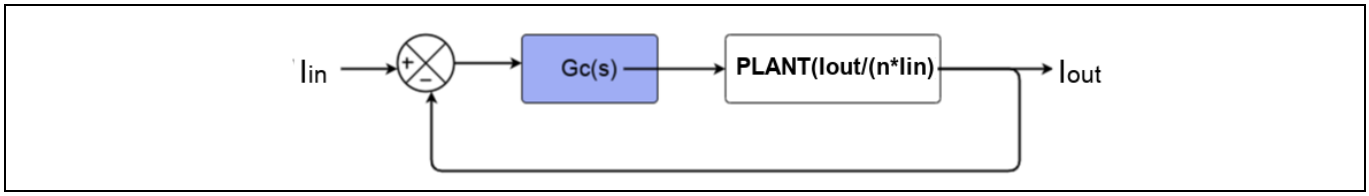


Figure 19 A compensated system

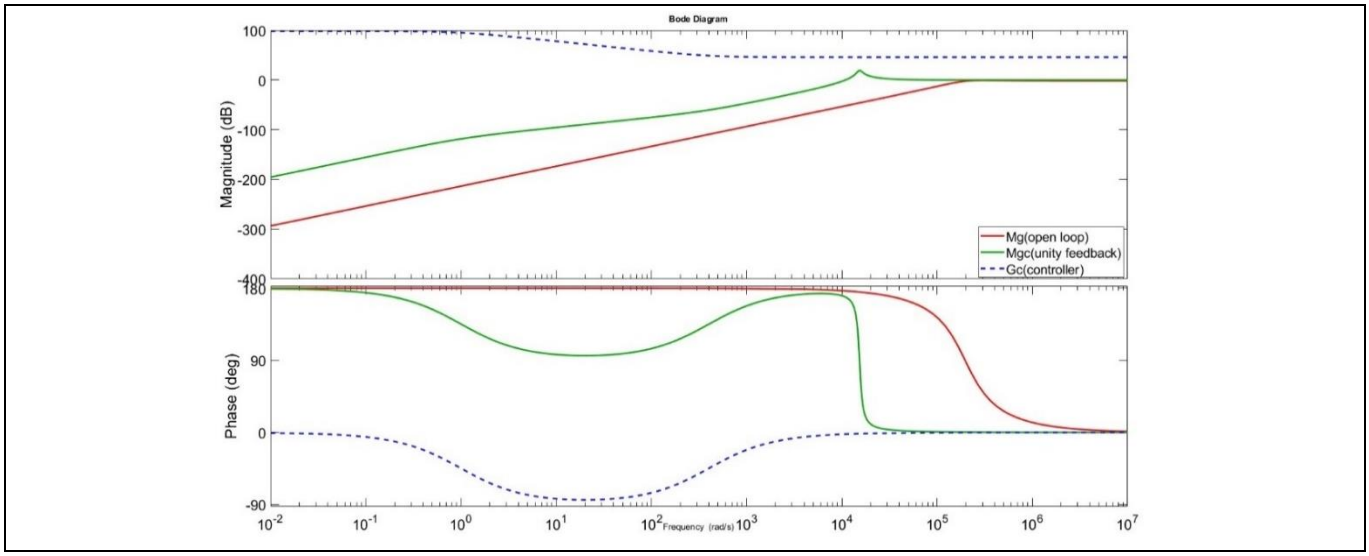


Figure 20 The Bode plot for an open loop and unity feedback with controller CL transfer function

3.3 Synchronous rectification (SR)

Using resonant tanks theoretical calculations

Characteristics of resonant tanks consist of two inductors and two capacitors that create a phase shift between the primary side gate pulses and switching frequency. This phase shift is defined as δ, which can be determined by resonant tank parameters and operating frequency. Without the help of sensors, δ can be estimated approximately. δ is dependent on the input impedance angle and angle between primary current and secondary current [4].

From Figure 6, input impedance angle $\angle Z_{ab} = \frac{V_{ab}}{I_{ab}}$ can be calculated.

$$Z_{ab} = Z_1 + ((Z_2 + R_o)||Z_m)$$

$$Z_{ab} = \frac{s^4\left(\frac{L_m C_1 C_2 L_1}{n^2}+L_2 C_1 C_2 L_1+L_m C_1 C_2 L_2\right)+s^3\left(\frac{L_1 C_1 C_2 R_o}{n^2}+\frac{L_m C_1 C_2 R_o}{n^2}\right)++s^2\left(L_1 C_1+L_2 C_2+L_m C_1+\frac{L_m C_2}{n^2}\right)+s\left(\frac{C_2 R_o}{n^2}\right)+1}{s^3\left(\frac{L_m C_1 C_2}{n^2}+L_2 C_1 C_2\right)+s^2\left(\frac{C_1 C_2 R_o}{n^2}\right)+sC_1}$$

$$Z_{ab} = \frac{s^4\left(\frac{1+k+\frac{k}{a}}{\omega_{r1}^4}\right)+s^3\left(\frac{b}{\omega_{r1}^3 Q}(1+k)\right)+s^2\left(\frac{2+k+\frac{k}{a}}{\omega_{r1}^2}\right)+s\left(\frac{b}{\omega_{r1} Q}\right)+1}{s^3\left(\frac{kb+1}{\omega_{r1}^3 Q R_o}\right)+s^2\left(\frac{b}{\omega_{r1}^2 Q^2 R_o}\right)+s\left(\frac{1}{\omega_{r1} Q R_o}\right)}$$

Keeping all the values, the calculated Z_{ab} will be:

$$Z_{ab} = \frac{s^4(2.948e{-}29)+s^3(3.322e{-}23)+s^2(6.83e{-}18)+s(1.284e{-}12)+1.32e{-}07}{s^3(4.508e{-}25)+s^2(1.695e{-}19)+s(1.742e{-}14)}$$

The Bode plot curve is shown in Figure 21 using the MATLAB code for the input impedance to check the behavior of the resonant tank with respective frequencies. Up to a frequency of 30 kHz, the capacitive region is present and for frequencies greater than 30 kHz, Figure 21 follows the inductive region.

When a circuit operates in the capacitive region, the current flowing through the resonant circuit can lead to the voltage, making it challenging to achieve zero voltage switching (ZVS). In such cases, the primary switches may start operating under hard-switching conditions, where the switching losses and reverse-recovery losses are high. This ultimately lowers the overall efficiency of the circuit.

The slow reverse-recovery characteristic of the body diodes in MOSFETs worsens the problem. During switching transitions, these slow-recovery diodes can allow high peak currents to flow through the primary MOSFETs. This overshoot current can lead to premature failure of the primary MOSFETs and contribute to increased electromagnetic interference (EMI) noises.

For the angle between the primary current and secondary current, the angle of transfer function $(\frac{I_{ab}}{I_{cd}})$ can be calculated as:

$$\frac{nI_{ab}}{I_{cd}} = \frac{Z_m+Z_2+R_o}{Z_m} = 1 + \left(\frac{\left(\frac{s}{\omega_{r1}}\right)^2+\frac{\left(\frac{s}{\omega_{r1}}\right)b}{Q}+1}{\frac{\left(\frac{s}{\omega_{r1}}\right)^2 k}{a}}\right)$$

$$\angle\frac{nI_{ab}}{I_{cd}} = \tan^{-1}\left(\frac{\frac{\omega_s b}{\omega_{r1} Q}}{1-\left(\frac{\omega_s}{\omega_{r1}}\right)^2}\right)$$

Thus, δ can be calculated as, $\delta = \angle Z_{ab} + \angle\frac{nI_{ab}}{I_{cd}}$

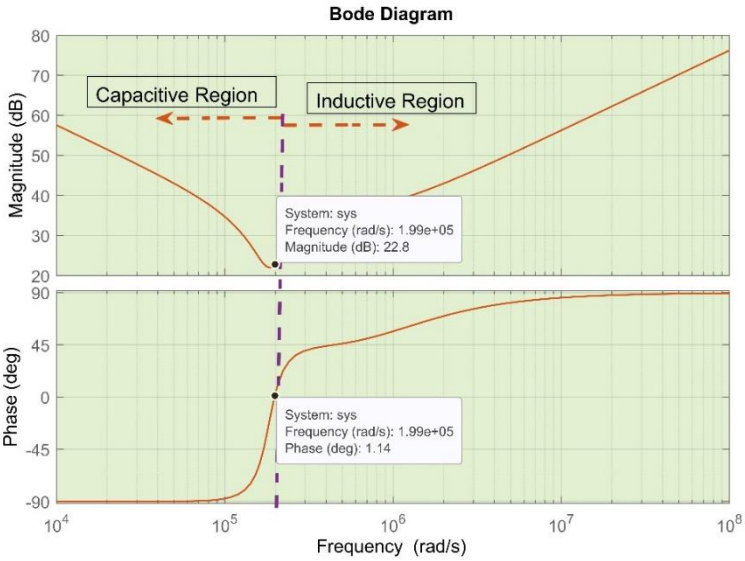


Figure 21 The capacitive and inductive regions of a resonant tank

Synchronous rectification is a technique that replaces the internal diode operations on the secondary side of a circuit with synchronous MOSFET operations. It reduces the switching and conduction losses in secondary switches. Controlling this phenomenon is non-trivial i.e., the turn-on and turn-off edges should be in sync with zero crossing of the secondary-side current (I_{cd}) which is dependent on the input voltage and load current. If they are not synchronous, a circulating current is introduced in the secondary side, leading to loss of efficiency and high drain-to-source stress.

Synchronous rectification involves replacing the traditional diode rectification in the secondary side of a transformer with synchronous MOSFETs. By doing so, the switching and conduction losses in the secondary switches can be reduced, leading to improved efficiency of the overall power conversion system. However, controlling synchronous rectification is important because the turn-on and turn-off of the MOSFETs must synchronize with zero crossing of the secondary-side current, I_{cd}. Achieving a synchronous operation ensures minimal overlap between the conduction paths of the synchronous rectifiers, thus reducing losses.

Failure to achieve a synchronous operation can lead to various issues, including the introduction of circulating currents on the secondary side that can significantly reduce efficiency and increase stress on the components, particularly the MOSFETs. These circulating currents can result in additional losses and contribute to decreased system reliability. Therefore, precise control of the synchronous rectification process, synchronized with zero crossing of the secondary side current, is essential for maximizing efficiency and minimizing stress on the components in power conversion systems.

Using current detection method

Synchronous rectification is a technique used in power electronics to improve efficiency by reducing losses in rectifier circuits. It involves using transistors to actively control the rectification process. A current transformer can be used to sense the current flowing through the load and provide feedback to the control system for the precise timing of the switching transistors. Sampling techniques are then used to measure the current waveform and adjust the timing of the synchronous rectification to maximize efficiency. This approach allows for more accurate control of the rectification process.

Theoretical calculations for synchronous rectification typically involve analyzing the power losses in the rectifier circuit and determining the optimal timing for the synchronous rectification switches. This can include calculating conduction losses, switching losses, and diode reverse recovery losses. Using sensors [5], such as high-frequency current transformers, allows for real-time monitoring of the current flowing through the load. This information is then fed back to the control system, which adjusts the timing of the synchronous rectification switches accordingly.

Using indirect sensing, such as measuring the voltage across resonant inductors, can offer advantages over traditional current transformers (CTs) in certain high-frequency applications. By integrating the voltage across the resonant inductor, the resonant current can be determined indirectly, which is essential for implementing synchronous rectification.

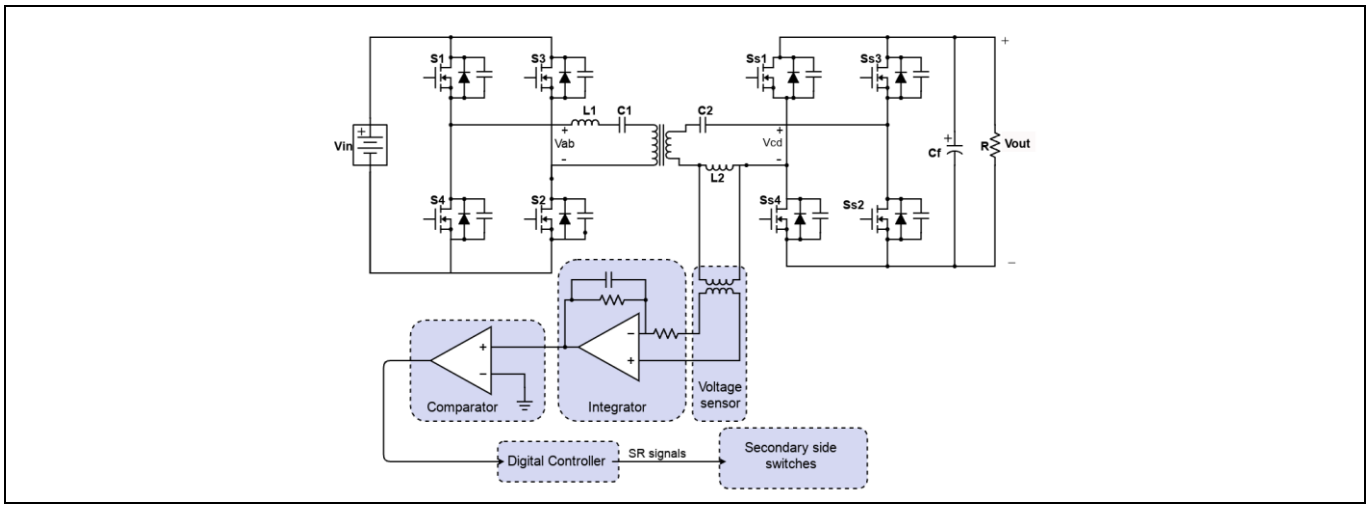


Figure 22 Synchronous rectification with sensors

Here is a breakdown of the proposed approach:

1. Voltage sensing: Measure the voltage across the resonant inductor using a sensing coil. This provides information about the resonant current passing through the inductor
2. Integration: Integrate the sensed voltage to obtain the average current across the resonant inductor. As the average current across the inductor is negligible, integrating the voltage provides a close approximation of the resonant current
3. Current direction restoration: Use a comparator to restore the current-direction information. This ensures that the synchronous rectification signals generated later are synchronized with the correct phase of the resonant current
4. Digital Control: Utilize a digital controller to generate synchronous rectification signals based on the restored current direction information. These signals are then provided to the secondary-side switches to enable synchronous rectification

This approach allows for accurate sensing and control of the resonant current without the drawbacks associated with connecting high-frequency current transformers in series. It can help mitigate issues such as increased cost, size, and losses in the circuit, making it a viable alternative for high-frequency synchronous rectification applications.

4 PLECS simulation model and results

A PLECS simulation was conducted using 1200 V SiC switches (IMZ120R030M1H) for the forward mode. The simulation design was intended to operate with an input voltage of 750 V and an output voltage of 600 V. In CC mode, the current flowing through the circuit was set to 18.33 A. The load connected to the circuit was a battery with a capacitance of 50 µFarad and an internal resistance of 51.1 ohms. The initial voltage of the load was set to 100 V. The closed loop PLECS simulation design is illustrated in Figure 23.

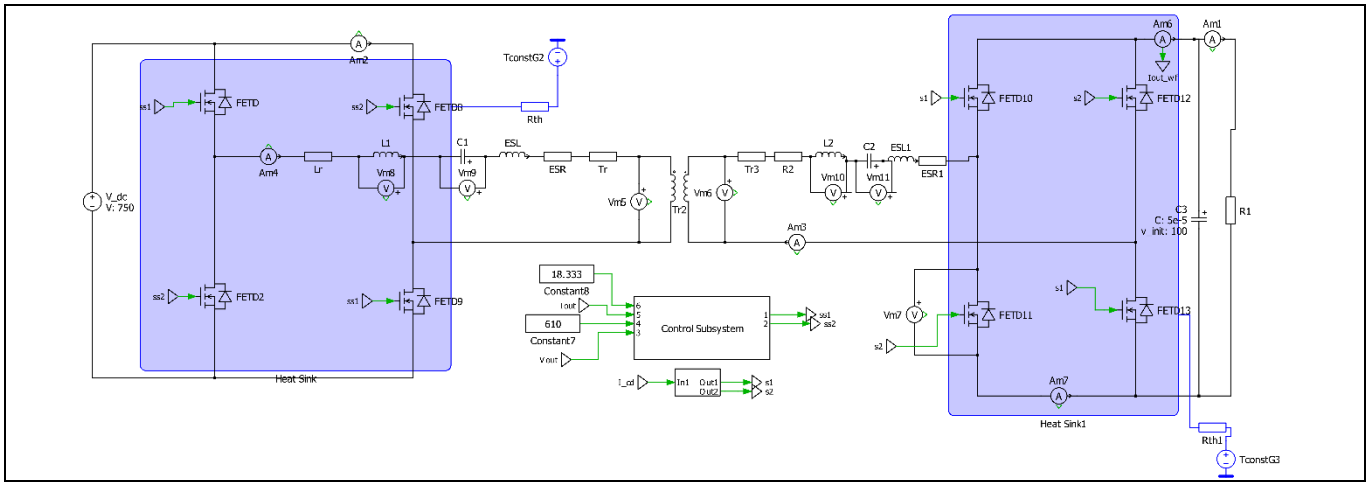


Figure 23 PLECS design of a CLLC resonant converter with controlling loop

Figure 24 and Figure 25 shows the waveform of the source voltage and current and the output voltage and current. These waveforms exhibit distinctive characteristics due to the resonant operation. The input current waveform is shaped by the resonant behavior of the converter's tank circuits. The energy stored in these resonant components can momentarily cause the current to reverse, resulting in a negative current flowing through the internal diodes of the MOSFETs. Figure 24 shows the output waveforms of the current and voltage with respect to the input current and voltage variation for CV mode. It can be seen that in the CV mode the settling time is approximately 0.5 seconds due to the 1-pole and 1-zero controller. During this mode, the input and output voltage variations shows transient and steady state stability.

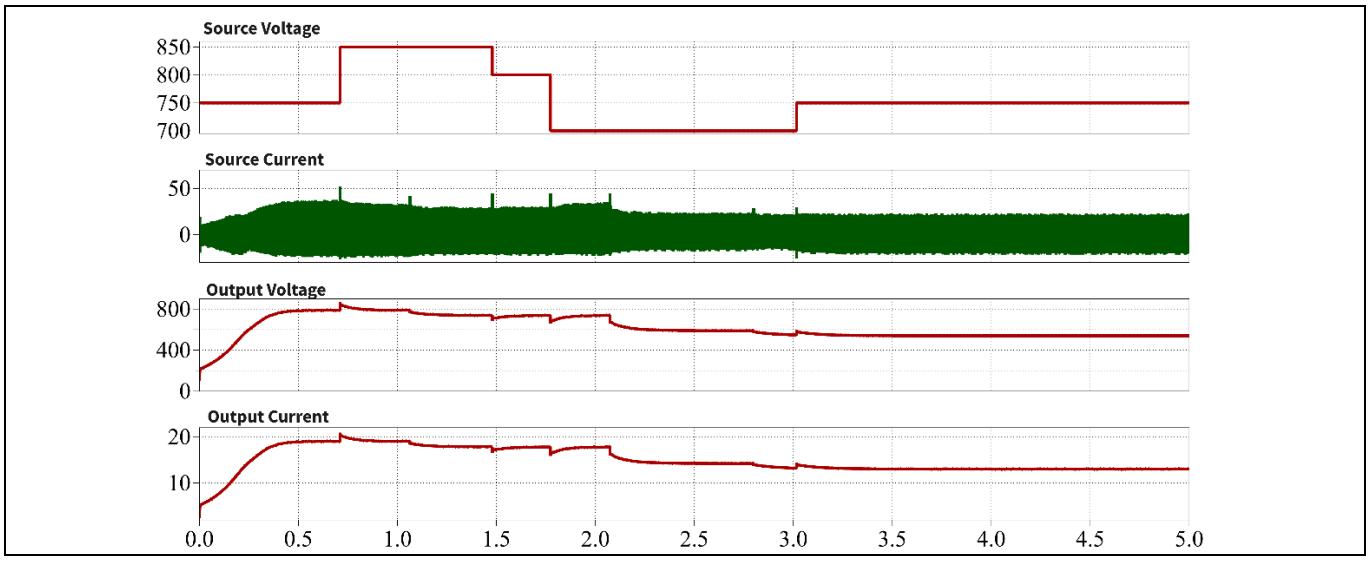


Figure 24 PLECS waveforms with variations in the input and output voltage during CV mode

Figure 25 displays the output waveforms of the current and voltage with respect to the input current and voltage for CC mode. It can be seen that in the CC mode the settling time is approximately 0.25 seconds due to the 1-pole and 1-zero controller. During this mode, the input voltage and output current variation shows transient and steady state stability.

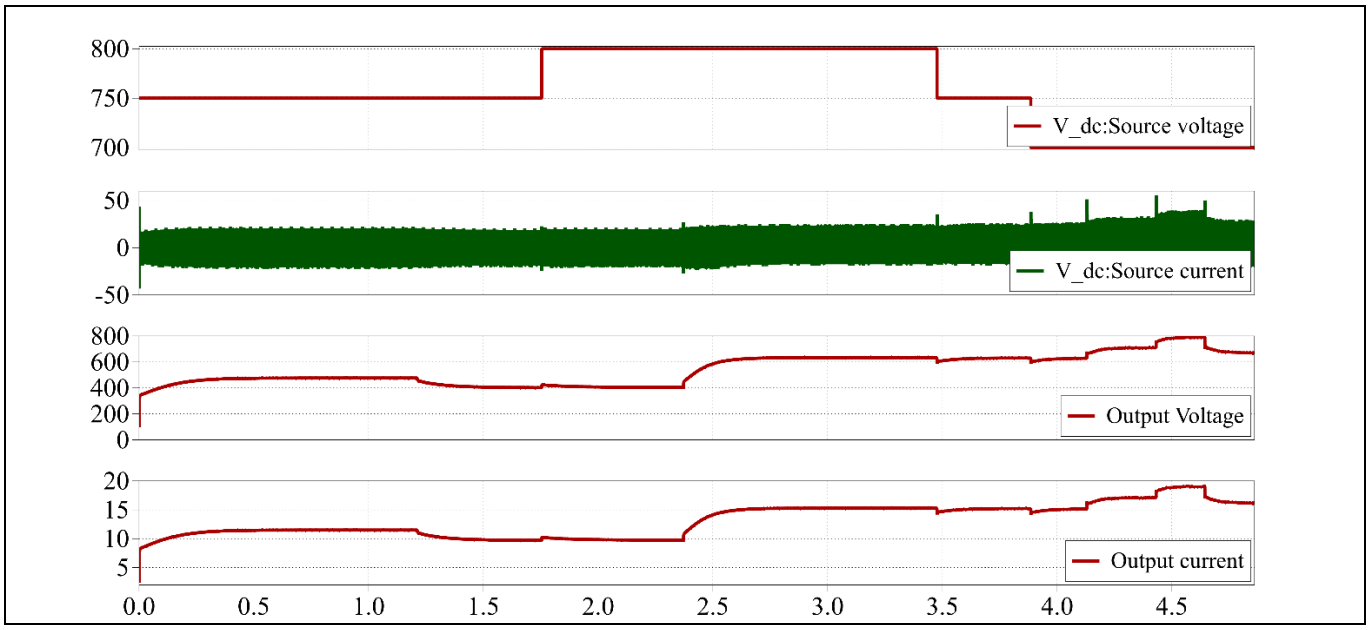


Figure 25 PLECS waveforms with variations in the input and output current during CC mode

For nominal input and output voltage (Vbus = 750 V and Vhv = 600 V) is performed to observe the other waveforms related to the CLLC converter.

With an input voltage of 750 V and a resonant frequency of 73 kHz, the CLLC converter, with a transformer turn ratio of 20:16, produces an output voltage of 600 V. As the reference voltage is 600 V, the CLLC converter operates in the resonance mode.

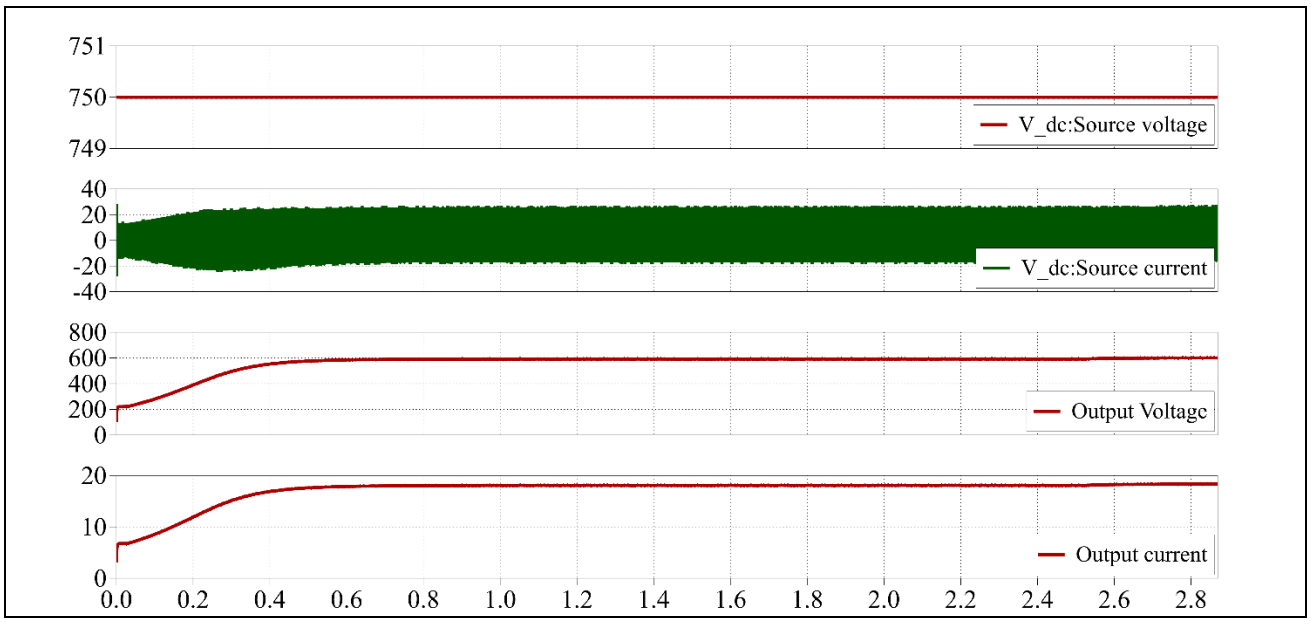


Figure 26 Waveforms for nominal input voltage and nominal output voltage at 11 kW

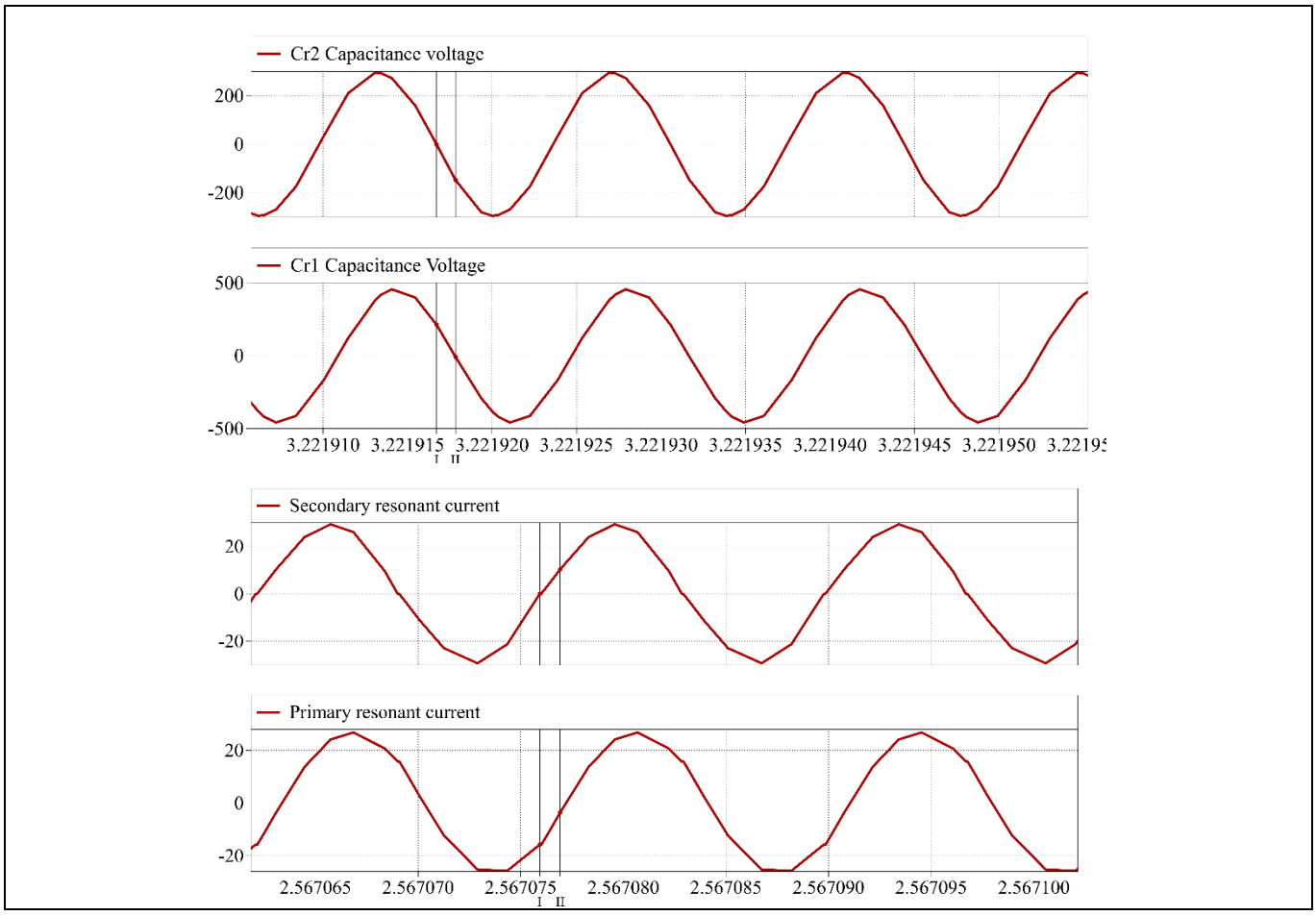


Figure 27 Resonant capacitor voltage and resonant input-output current (I_{ab}, I_{cd})

Figure 27 shows the resonant capacitor voltage and input-output current waveform to the resonant tank circuits. The angle difference between input resonant current and output resonant current can be seen more clearly in the expanded version of these waveforms, with the help of cursor I and cursor II, as explained in Section 3.3. The angle difference between the input current and the output current depends on the operating frequencies. It appears that, based on the output current of resonant tank circuits, the secondary side of MOSFETs should be turned on. Figure 248, shows that turning on the gate pulse for the secondary side of the MOSFETs concerns the output current. When I_{cd} is positive then Ss1 and Ss2 switches are turned on and when I_{cd} is negative the Ss3 and Ss4 switches are turned on.

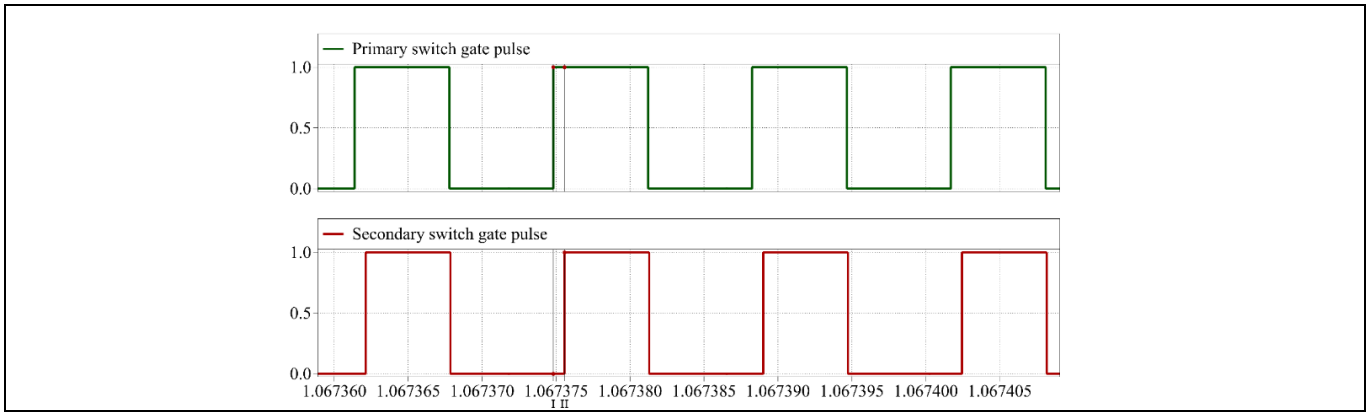


Figure 28 Switching gate pulse for primary and secondary-side switches

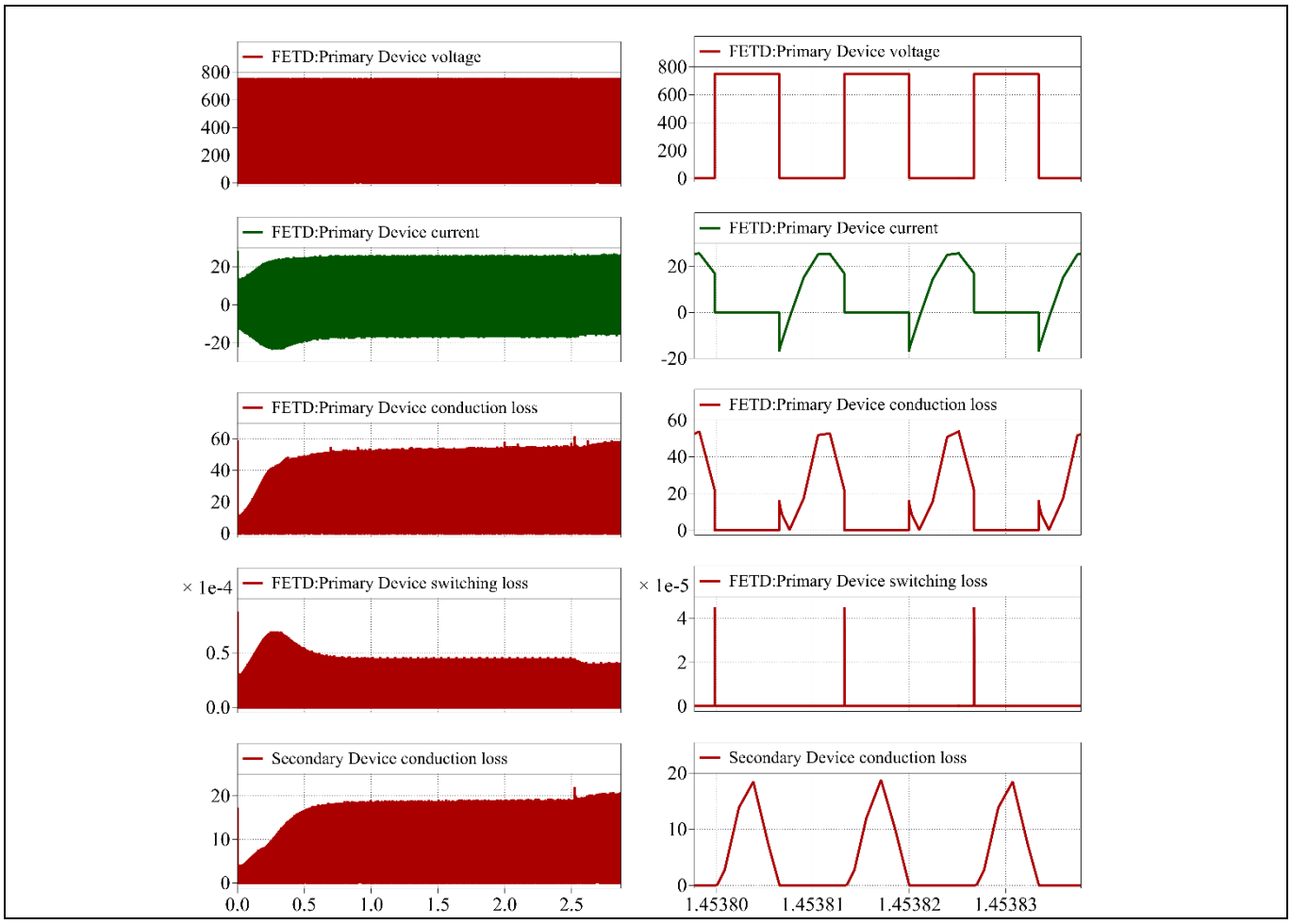


Figure 29 Voltage, current, conduction loss, and switching loss across the primary switch (S1) and conduction loss across the secondary switch (Ss1)

Figure 29 shows the parameters of the primary-side switches such as device voltage, device current, conduction loss, and switching loss across primary switch and conduction loss across the secondary switch. The average and RMS currents passing through the primary switch are 7.17 A and 13.32 A respectively while operating for 11 kW at nominal input and output voltage. The average and RMS power conduction losses across one primary side switch are 15 Watt and 25.7 Watt respectively. As the image shows, the switching losses are negligible. For all primary-side switches, the total conduction loss is 60 Watt and for secondary side switches, total conduction loss is 101.4 Watt. Whereas for the secondary-side switches, the average and RMS power conduction losses across one switch are 5.063 Watt and 8.53 Watt respectively, whereas the switching loss is negligible. For all the four secondary switches, the total conduction losses are 20.12 Watt and 34.12 Watt.

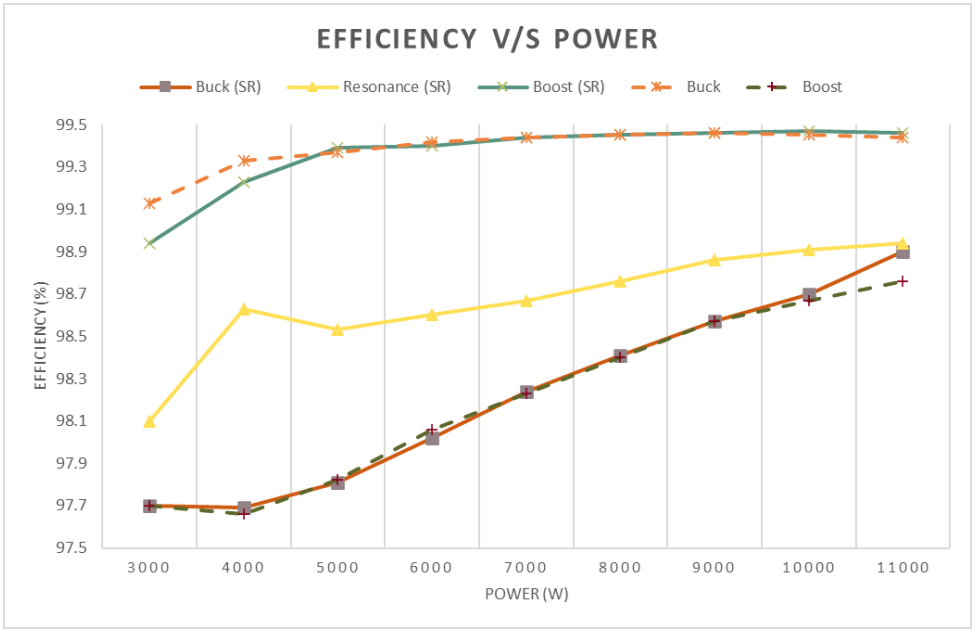


Figure 30 Efficiency v/s power curve with and without synchronous rectification

The efficiency throughout this operation can be calculated as:

$$\text{Efficiency},\eta = \frac{Pout}{Pin} = 1 - \frac{P_{loss}}{P_{in}} = 1 - \frac{101+34.12+internal\ losses}{11000} = 98.7\%$$

The efficiency, calculated at different power levels, with and without synchronous rectification is shown in Figure 30. Without synchronous rectification, at low load, the losses are higher, and the efficiency is lower than when operating with synchronous rectification.

Figure 30 shows the behavior of CLLC converter while working in buck, boost and at resonance with, and without synchronous rectification. In buck mode, the operating frequency is higher and draws more current for the same power. This can increase losses in the CLLC converter. As losses increase, efficiency gets affected.

5 Conclusion

The CLLC converter is a reliable and efficient solution for power conversion applications. Its resonant energy exchange between the inductor-capacitor tank circuits ensures efficient power transfer. While the soft-switching techniques minimize switching losses, leading to an overall increase in efficiency. Proper switch timing using synchronous rectification guarantees a smooth operation and reduces stress on the components. The converter's bidirectional power flow offers energy transfer in both forward and reverse directions, making it perfect for energy storage and bidirectional power flow applications.

Modeling CLLC converters requires capturing the behavior of the resonant tank circuits, semiconductor devices, and control strategies including constant current, constant power, and constant voltage controlling loop to achieve accurate predictions of performance under different operating conditions. The converter's high efficiency and reliability are attributed to its reduced switching losses, efficient energy transfer mechanisms, and soft-switching operation.

Conceptual validation of the model is crucial to ensure that the converter behaves as expected in real-world scenarios. This was done with the help of PLECS simulation using 1200 V IMZ120R030M1H practical SiC switches. Proper design, modeling, and validation are essential to optimize performance and guarantee successful implementation in practical systems.

In summary, the CLLC converter is a robust solution that offers high efficiency, bidirectional power flow, and reliable operation. Its effective energy transfer mechanisms reduced switching losses, and soft-switching operation make it the perfect solution for various power conversion applications.

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Revision history

Document revision	Date	Description of changes
Revision V1.0	2024-07-28	Initial version
Revision V1.0	2024-07-10	Migrated to the current template

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Edition 2024-07-10

Published by

Infineon Technologies AG

81726 Munich, Germany

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Document reference

AN-2024-06

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