500V CoolMOS^{TM} CE

Newest 500V Superjunction MOSFET for Consumer and Lighting Applications

The new CoolMOS^{TM} CE is the fourth technology platform of Infineon's market leading high voltage MOSFETs designed according to the revolutionary superjunction (SJ) principle in the 500V class. 500V CE provides all benefits of a fast switching SJ MOSFET while keeping ease of use and implementation. This article will show that the complete CE series of MOSFETs can achieve very low switching losses can make applications more efficient, more compact, lighter and thermally cooler while representing a cost appealing alternative compared to standard MOSFETs.

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Nowadays the 500V market is dominated by standard MOSFETs, particularly in the consumer market. It is visible that also this market range is going to be efficiency driven especially in light load operation. The way to achieve higher light load efficiency is to reduce driving losses and switching losses in load conditions. Due to the revolutionary area specific on-state resistance (R_{on}*A) of SJ MOSFETs this losses can be reduced by the reduced internal capacitances and therefore reduced output capacitance (C_{oss}) and gate charge (Q_g).

➢ Superjunction Principle

"All CoolMOS^{TM} series are based on the SJ principle. Where conventional or standard MOSFETs just command on one degree of freedom to master both on-state resistance and blocking voltage, the SJ principle allows two degrees of freedom for this task. Therefore conventional MOSFETs are bound by the limit of silicon, a barrier which marks the optimum doping profile for a given voltage class. This limit line (which is visible in Figure 1), has been theoretically derived by Chen and Hu in the late 80ies [1]. No commercial has an on-state resistance better than the limit line of silicon." [2]

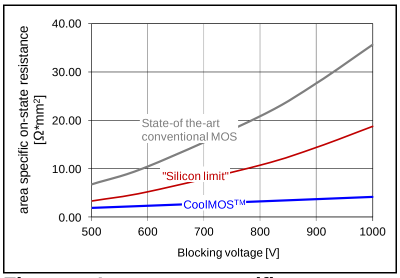

Figure 1: area specific on-state resistance versus breakdown voltage

Figure 1 describes the R_{on}*A (y-axis) over the rated blocking voltage or breakdown voltage ($V_{(BR)DSS}$). It is clearly visible that the CoolMOS^{TM} series has a nearly constant R_{on}*A over all $V_{(BR)DSS}$ classes which brings a reduction of about 70% R_{on}*A with a value of 1.95Ω*mm² of the 500V CE in comparison to a conventional or standard MOSFET. "The basic idea is simple, instead of having electrons flowing through a relatively high resistive (high voltage blocking) n-area, we allow them to flow in a very rich doped n-area, which gives naturally a very low on-state resistance. The crucial point for the SJ technology is to make the device block its full voltage, which requires a careful balancing of the additional n-charge by adjacently positioned deep p-columns, going all the way straight through the device close to the back side n+ contact." [2]

➢ Reduction of Internal Capacitances

The most important benefit of this small R_{on}*A of 1.95Ω/mm² is the reduction of internal capacitances. The following figure represents the internal capacitances of the IPA50R280CE against a comparable standard MOSFET with the same $R_{DS(on)}$.

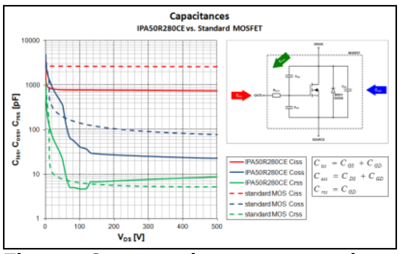

Figure 2: capacitance comparison 500V CE vs. standard MOSFET

In Figure 2 the capacitance value in pF on the y-axis and the drain source voltage (V_{DS}) from 0V - 500V is visible. The red line describes the input capacitance

(C_{iss}), the blue line the output capacitance (C_{oss}) and the green line the reverse capacitance (C_{rss}). Furthermore the solid line represents the 500V CE and the dashed line the comparable standard MOSFET. It is visible that the C_{iss} and the C_{oss} are much lower in comparison to the standard MOSFET and the C_{GD} is portioned to the C_{GS} in order to have a self-limiting behavior of the dv/dt of the MOSFET for example during hard commutation on a conducting body diode. "A fundamental characteristic of all superjunction MOSFETs is, that both the output and reverse capacitance show a strong non-linearity. The non-linearity in SJ capacitance characteristics comes from the fact that at a given voltage, typically in the range of 1/10th of the rated blocking voltage, p- and n-columns deplete to each other leading to a fast expansion of the space charge layer throughout the structure. This means that at a voltage beyond 50V for a 500V rated MOSFET both C_{oss} and C_{rss} reach minimum values of a few pF only, resulting in a dv/dt of more than 100V/ns and di/dt of several thousand A/µs if the load current is allowed to fully commute into the output capacitance during turn-off." [3] Furthermore it is visible that the capacitance value of the C_{oss} is decreasing by higher voltages, which means that the highest dv/dt is reached shortly before the bulk or bus voltage is reached. By the end the reduction of the capacitances brings a benefit also in the gate charge (Q_g) reduction.

➢ Gate Charge (Q_g)

One of the most important improvements is the gate charge (Q_g) reduction which heads to light load efficiency improvements given by the reduction of the driving losses. Furthermore it is possible to drive the MOSFET by using a gate driver with lower gate drive capability which leads to a reduction of the overall system costs.

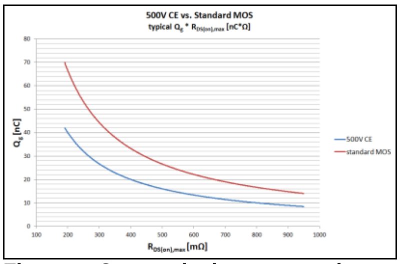

Figure 3: typical gate charge 190mΩ-950mΩ $R_{DS(on)}$

Figure 3 represents the Q_g in nC on the y-axis over the different maximum $R_{DS(on)}$ from 190mOhm to 950mOhm. The blue line illustrates the 500V CE and the red line the standard MOSFET. It is visible that there is a typical Q_g reduction of 40% in comparison to a standard MOSFET. This impact on the light load efficiency is going to be shown in the efficiency comparison in one of the following sections of this document.

➢ Applications

The new 500V CE finds its place in different applications according to the following figure of a typical AC/DC SMPS power architecture:

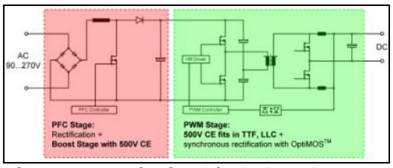

Figure 4: typical AC/DC SMPS power architecture

As shown 500V CE fits in PFC stage or more precisely in the boost stage of the PFC. Furthermore, also the DC/DC conversion stage is addressed where two different converters are mentioned. On the one hand side a hard switching topology where the TTF comes into place and the LLC converter which is a resonant topology. This concludes in the following target applications for the 500V CE:

- PC Silverboxes
- LCD/LED/PDP TVs
- Gaming Consoles
- Lighting applications

Efficiency comparison between 500V CE and standard MOSFET was conducted in CCM PFC, while hard commutation on conducting body diode was carried out in a half bridge configuration which is relevant for resonant topologies like a LLC resonant converter. Both comparisons are shown in this document.

➢ Efficiency

In order to give a clear statement of differences in the efficiency the CCM PFC is one of the most suitable applications to prove such a better efficiency statement given its simple construction and the applied fixed frequency. The following setup was therefore used:

- CCM PFC
- V_{in} = 90VAC
- V_{out} = 400VDC
- P_{out} = 0W to 400W
- Frequency = 100kHz
- $R_{G,ext}$ = 5Ω
- Ambient temperature = 25°C
- Heat sink preheated to 60°C
- Plug & Play scenario between IPP50R280CE and comparable standard MOSFET

As shown in the setup definition a worst case scenario was chosen with 90VAC input voltage in order to have higher currents flow through the PFC MOSFET. The switching frequency was set to 100kHz representing the average frequency currently used on the market (normally between 65kHz and 135kHz). Furthermore the heat sink is preheated to 60°C which is typically the temperature in a power supply.

Figure 5 represents the efficiency comparison of the mentioned parts in absolute values (upper diagram) and in relative values (lower diagram).

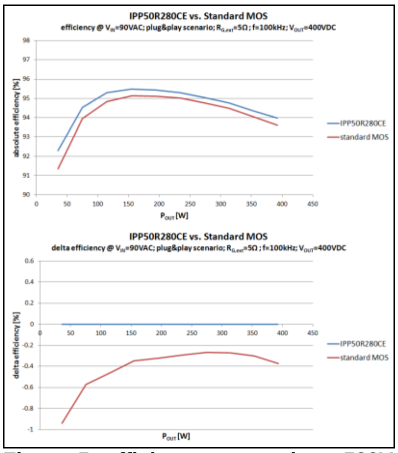

Figure 5: efficiency comparison 500V CE vs. standard MOSFET

On the x-axis the output power Pout is represented and on the y-axis the absolute efficiency and the efficiency delta of the two analyzed MOSFETs. This plug and play measurement shows the big advantage of the 500V CE in comparison to the standard MOSFET especially in light load operation. The highest efficiency on this system was measured at around 150W with an absolute value of around 95.5% bringing an average 0.3%-0.4% higher efficiency starting from 100W to 400W. The biggest advantage is observed at 40W which corresponds to 10% of load. In this load condition the 500V CE has about 0.9% higher efficiency than the comparable standard MOSFET mainly deriving from the 40% Q_g reduction. An increased switching speed could also bring negative aspects e.g. high di/dts could incite high voltage peaks in combination with parasitic inductances. Highest di/dts are reached during hard commutation on the conducting body diode when the Q_{rr} of the body diode has to be removed.

➢ Hard Commutation on Conducting Body Diode

The best way to analyze the behavior of the body diode of the MOSFET is in an half bridge configuration where the high side MOSFET is used as a switch to load the 145µH inductance which is located in parallel to the drain and source of the low side MOSFET. When the high side MOSFET is turned-off the current is running through the body diode of the low side MOSFET. After 2µs body diode conduction time the high side MOSFET is turned-on again and the Q_{rr} from the low side MOSFET has to be removed. In this case a high current is flowing from drain to source of the low side MOSFET with high di/dts which could provoke a voltage overshoot, which is marked as $V_{DS,max}$, due to the source inductance of the low side MOSFET. The setup according this behavior is represented in Figure 6.

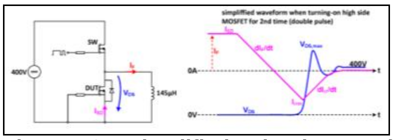

Figure 6: simplified circuitry and waveform for hard commutation

According to this setup the maximum V_{DS} peak is going to be analyzed in represented in Figure 7 which illustrates the V_{DS} peak on the y-axis over different currents (I_F) through the body diode. It is visible that the IPP50R500CE has a lower or same $V_{DS,max}$ peak over the whole current range than the much slower switching comparable standard MOSFET. This can only be achieved due to the self-limiting dv/dt behavior of this SJ MOSFET family. All mentioned technology parameters and these two measurements show that 500V CE brings benefits in hard switching topologies and resonant switching topologies.

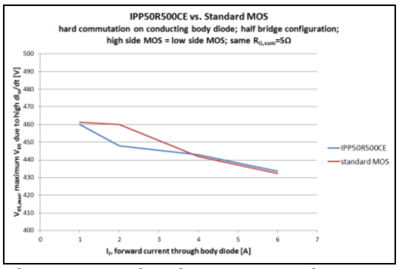

Figure 7: hard commutation on conducting body diode

➢ References

[1] X. B. Chen and C. Hu, "Optimum doping profile of power MOSFET's epitaxial Layer.", IEEE Trans. Electron Devices, vol. ED-29, pp. 985-987, 1982

[2] G. Deboy, L. Lin, R. Wu: "CoolMOS™ C6 Mastering the Art of Slowness", Application Note revision 1.0 2009-1221, pp. 5-6

[3] DR. H. Kaples: "Superjunction MOS devices – From device development towards system optimization", paper EPE 2009 – Barcelona, ISBN 9789075815009, pp. 3