Higher Efficiency & Power Density with Infineon

Infineon Offers in High Power Applications

- Infineon offers high performance solution in overall energy flow for Telecom/Server/Industrial and other high power applications

Analog&Digital controller

AC

PFC

HV DC/DC

SR

OR-ing

DC1

DC/DC Brick

DC2

PoL

DC3

Aux.Power

5V,12V

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1. High Voltage MOSFET

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Infineon is Leading AC/DC Application with CoolMOS™ Product Series

Year	Product	Description	Voltage
1998	S5	CoolMOS™ frist series	600V
2001	C3	Well-know as CoolMOS	600V
2004	CFD	First generation fast body diode CoolMOS	600V
2005	CP	Effieicency optimized	600V
2009	C6/E6	Successor of C3	600/650V
2011	CFD2	G2 fast body diode CoolMOS	650V
2012	P6	Optimization on efficiency and easy-of-use	600V
2013	650V C7	Rds(on)/package improved for high power density design	650V
2014	CE	For consumer electronica application	500/600/650/800V
2015	600V C7	Further improve efficiency based on C7 platform	600V
2016	800V P7	Optimized for flyback topology	800V
2017	600V CFD7, 600V P7, 700V P7		
2018	950V P7	For high Vin application	950V

20-year success in CoolMOS™ strengthens Infineon leading position of product performance and reliability in product process. Infineon delivers products to customers with good quality and high consistency.

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CoolMOS™ Portfolio High Power

Better efficiency
Lower price

CP
C6/E6
C3
CFD
Active parts 2017

C7
P6
CFD2
Active & Preferred parts 2017*

G7
C7
P7
CFD7
Active & Preferred parts 2017, 2018

C7/C7-Series
- Highest efficiency
- Fast switching

P7-Series
- Good price/ performance
- General purpose (PFC/LLC)

CFD7-Series
- Fast body diode (ZVS PS FB/ LLC)

Time

* Existing series to be preferred until relevant parts of the new CoolMOS™ 7 series are available

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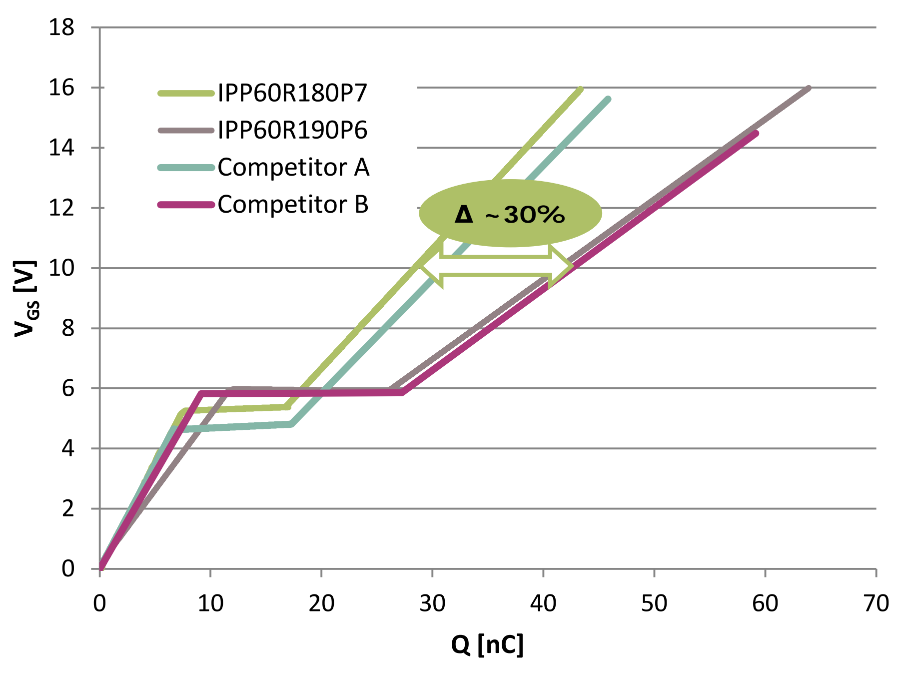
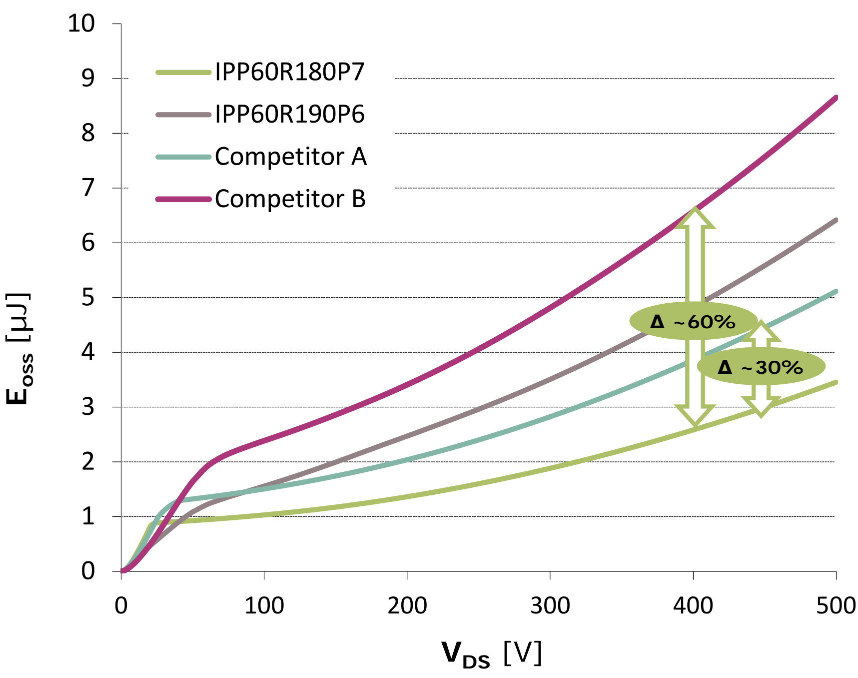
CoolMOS™ P7 offers significant reduction of driving and switching losses

Switching losses (Eoss)





600 V CoolMOS™ P7 offers

- ~ 30% reduced gate charge over competition at 10V
- between 30% and 60% lower Eoss than competition at 400 V

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CoolMOS™ P7 offers smaller Rds(on) change with Tj increasing

Rdson[mΩ] at 15.9A over Tj [°C]

CoolMOS™ P7 600 V offers lower $R_{DS(on)}$ increase with increasing junction temperature than competition and previous CoolMOS™ series.

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CoolMOS™ P7 integrated ESD protection reduces ESD related failures

ESD protection Mechanism

G
+
I_{GS}
V_{GS}
C_{GS}
–
S

During ESD event:

- V_{GS} is clamped by Zener Diode
- I_{GS} flows through Zener Diode
- Thus protect gate oxide

D
G
Zener diode
S

Customer benefits

- Better assembling yield thus less cost
- Less field failure rate
- Higher quality and better reputation

600 V CoolMOS™ P7 offers an **ESD robustness** of > 2kV (HBM Class 2)

- 100 mΩ – 600 mΩ due to integrated Zener diode
- < 100 mΩ ensured by chip size

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CoolMOS^{TM} P7 – the most well balanced high voltage MOSFET in key dimensions

CoolMOS™ P7
CoolMOS™ C7
Efficiency
Low Ringing
Commutation Ruggedness
ESD
Price Competitiveness
Portfolio

- Most rounded technology of all CoolMOS^{TM} families
- Perfect combination of:
  - high efficiency
  - excellent Ease-of-use
  - competitive price and
  - outstanding portfolio granularity

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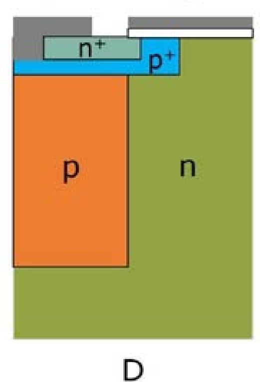
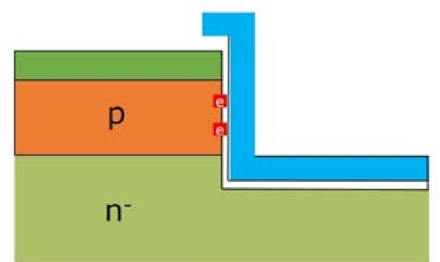
Si, SiC and GaN

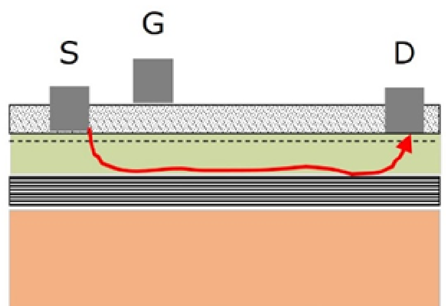
Si Superjunction



SiC MOSFET



GaN HV e-mode lateral HEMT



CoolMOS™	CoolSiC™	CoolGaN™
› Established Si-based SJ technology › Broadest portfolio down to 10 mOhm › Excellent E_{oss} values	› Low reverse recovery charge › Low temperature dependence of RDS(on) › Easy driving, compatible with TO packages	› Zero reverse recovery charge › Lowest Qoss and gate charge › More complex driving

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One specific feature of SiC MOSFETs is the flat temperature dependence of the $R_{DS(on)}$

normalized $R_{DS(on)}$ over T_J

IPW60R035CFD7_normalized
IPZA65R035M1_normalized
IGOT60R070D1_normalized

CoolMOS
CoolGaN
CoolSiC

+30%
+50%

At 100°C the $R_{DS(on)}$ of CoolSiC is 30% lower compared to CoolGaN and 50% lower than CoolMOS

$R_{DS(on)}$ normalized

2.50
2.00
1.50
1.00
0.50
0.00

-50 -25 0 25 50 75 100 125 150 175

T_J [°C]

This behaviour allows the use of higher $R_{DS(on)}$ values of SiCMOS compared to Si or GaN. Another aspect why higher $R_{DS(on)}$ values can be used with SiCMOS is the puls current limitation of GaN

→ both aspects are a strong comercial lever for SiCMOS and can partially compensate SiCMOS cost disadvantages

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Figure Of Merit (FOM) comparison
WBG shows significant benefits over Silicon

- facilitates dead time / resonant current settings and enables higher frequency
  → higher efficiency
- enables applications with repetitive hard commutation
  → e.g. CCM Totem Pole PFC
- minimum switching losses in hard switching topologies
  → e.g. classic boost PFC
- reducing driving losses
  → especially in light load conditions
- higher V_F than SJ MOSFETs
  → dead time has dramatic influence on system efficiency

DEVICE	$V_{(BR)DSS}$ [V]	$R_{DS(on),typ}$ [mΩ]	$R_{DS(on)} * Q_{oss}$ [mΩ * µC]	$R_{DS(on)} * Q_{rr}$ [mΩ * µC]	$R_{DS(on)} * E_{oss}$ [mΩ * µJ]	$R_{DS(on)} * Q_g$ [mΩ * nC]	V_F @ 15A [V]
CoolMOS™ C7	600	52	18.3	312	421	3536	0.85
CoolMOS™ CFD7	600	57	19	32.5	439	3819	1
CoolGaN™ Gen1	600	55	2.3	0	352	226	2.7 / 7.7
CoolSiC™ Gen1	650	50	3.2	3	525	2100	3.3

With these FOM's WBG devices enable hard switching half bridge configurations such as totempole PFC which cannot be served with SJ devices today and improve performance in resonant topologies

Source: René Mente – PMM ACDC AE CE, October 2018

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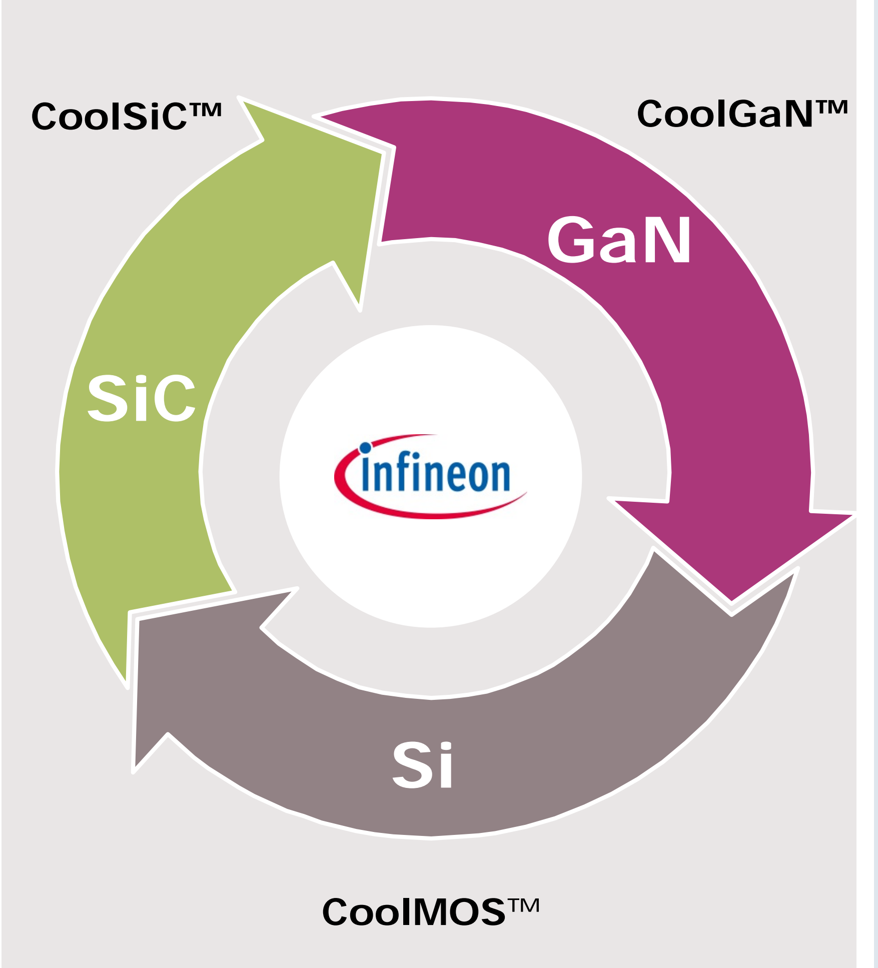
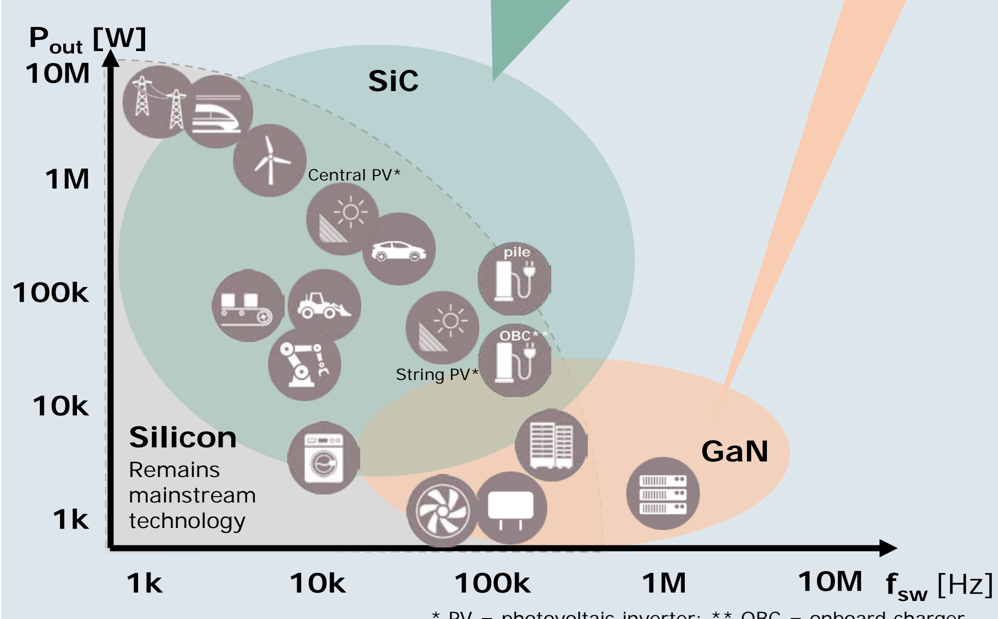
Infineon is the only company to master all power technologies…

…and is the trusted advisor for all of them



- GaN enable new horizons in power supply applications and audio fidelity
- Targeting 100V - 600V
- Medium power/ Highest switching frequency

- SiC complement silicon in many applications and enable new solutions
- Targeting 600V – 3.3 kV
- High power/ High switching frequency



* PV = photovoltaic inverter; ** OBC = onboard charger

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650V CoolSiC™ MOSFET

Target applications

Wave 1

R_{dson} max [mΩ] 18V	R_{dson} typ [mΩ] 18V	TO-247-4	TO-247-3
35	26	IPZA65R035M1	IPW65R035M1
65	48	IPZA65R065M1	IPW65R065M1
95	70	IPZA65R095M1	IPW65R095M1
145	107	IPZA65R145M1	IPW65R145M1

Rdson and product name are subject to change before the official product release

Availability according current plan:

- Early eng samples: now
- ISAR Samples: Q3 2019
- Target data sheets available
- General availability: Q1 2020 (or earlier)

Wave 2

Will be SMD package

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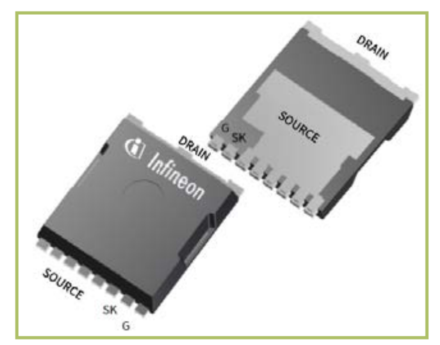
600V CoolGaN™ helps improve power density

- 600V GaN with 70mohm and 190mohm is available in the following package.

Package	DSO BSC PG-DSO-20-85	DSO TSC PG-DSO-20-87	TOLL PG-HSOF-8-3	DFN 8x8
Cooling				
Thermal performance	++	+++	+	0

DSO-20 BSC

DSO-20 TSC



TOLL

ThinPAK 8*8

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Power density feature
Best $R_{DS(on)}$/package

RDSON/Package - D²PAK_TOLL

Package	Footprint	Device	RDSON max in mΩ
D²PAK	Footprint 150mm²	Comp B	88
D²PAK	Footprint 150mm²	Comp A	63
D²PAK	Footprint 150mm²	C7 650V	45
D²PAK	Footprint 150mm²	C7 600V	40
TOLL	Footprint 115mm²	C7 GOLD 650V	33
TOLL	Footprint 115mm²	C7 GOLD 600V	28

CoolMOS™ C7 with the best $R_{DS(on)}$ in the world

CoolMOS™ G7 is even better

- Infineon already offers best $R_{DS(on)}$ in D²PAK
- Now improved again with C7 Gold and TOLL package with smaller footprint

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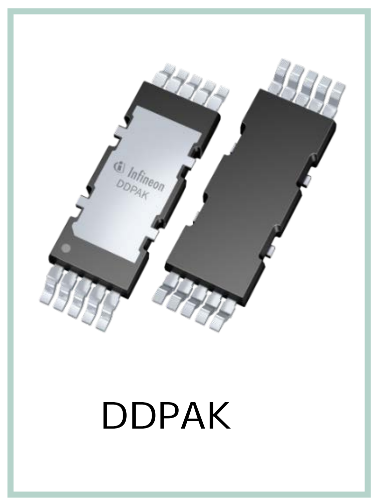
Package Innovation Contributes To High Power Density Design

TO-247-4pin

ThinPAK 8*8

TOLL



DDPAK

- With high efficiency conversion technology, Infineon also introduce innovative package to our customers, driving from through hole → SMD package to achieve high power density.
- Besides that, ...

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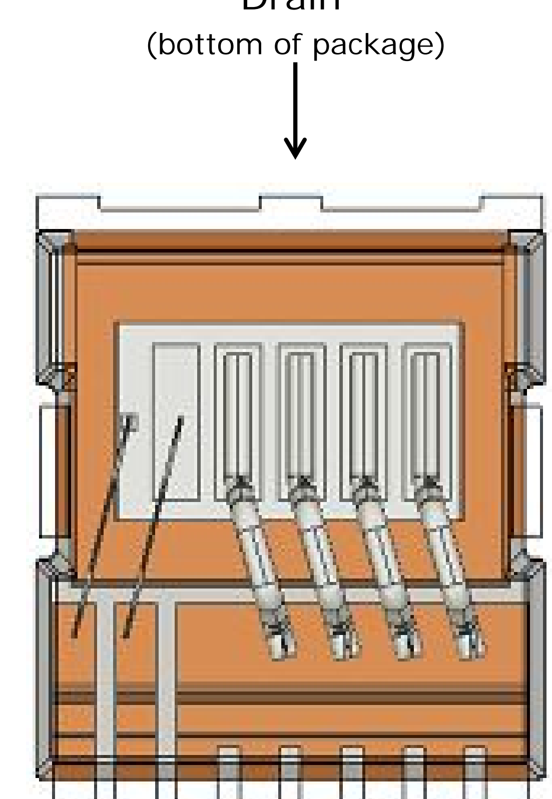
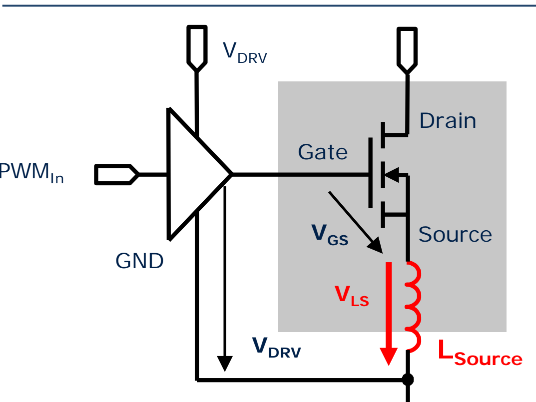
Kelvin Source Layout Helps Increase Efficiency

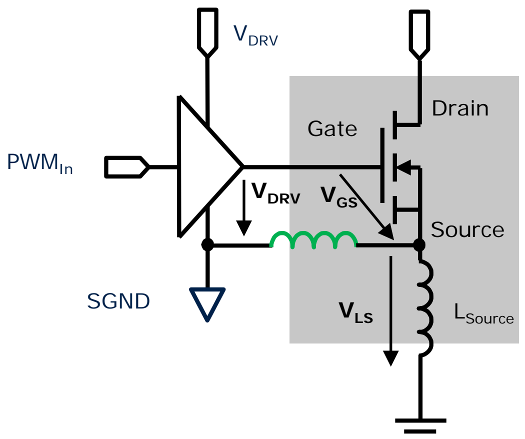


Traditional 3-pin Package



- Parasitic source inductance counter-acts drive voltage
- **Lower efficiency** due to slow down of transient

Innovative 4-pin configuration



- Separate pin “source-sense” delivers undisturbed signal to driver
- **Higher efficiency** at full load

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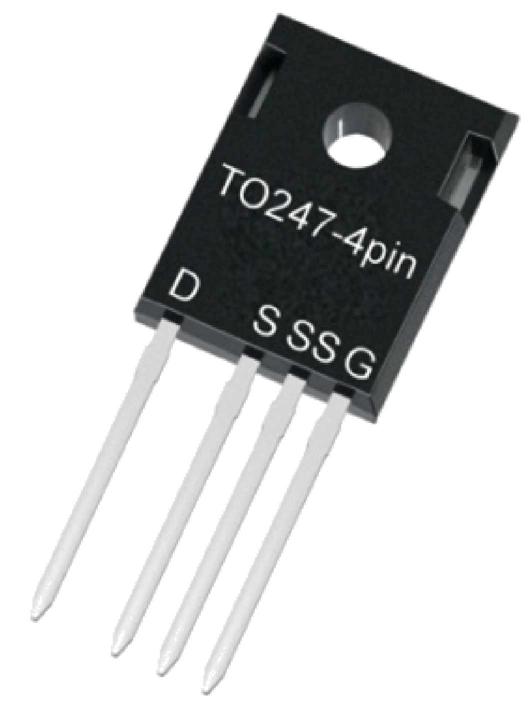
TO-247 4-PIN, an easy drop-in idea to increase efficiency



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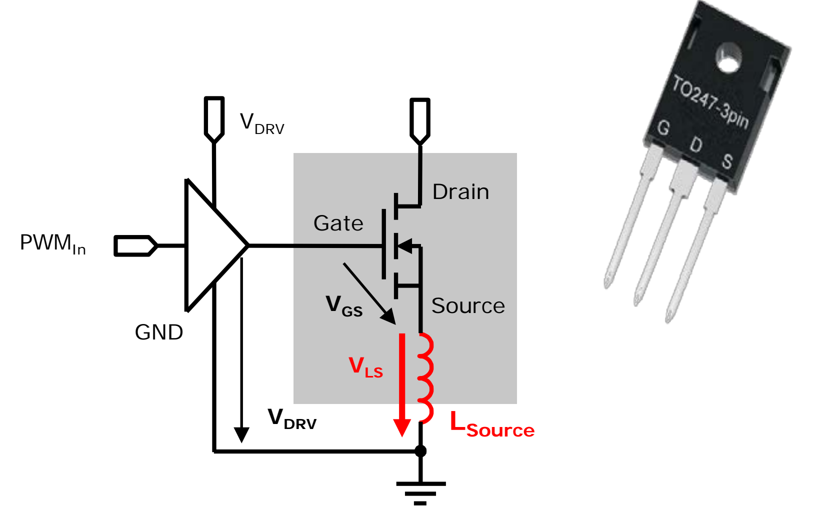
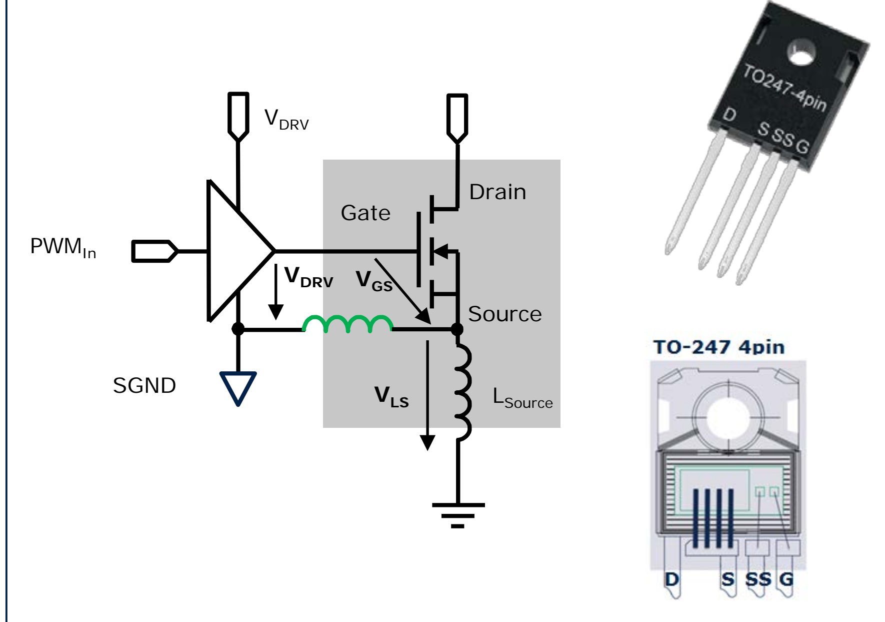
The TO247-4 package offers higher efficiency by means of a dedicated source-sense pin

Standard TO 247



- Parasitic source inductance counter-acts drive voltage
- Slow down of transient leads to lower efficiency

Novel TO 247-4 pin



- Separate pin "source-sense" (Kelvin source) delivering an undisturbed signal to the driver
- Up to 3x lower switching losses lead to
  - Higher efficiency
  - Cost reduction potential in application

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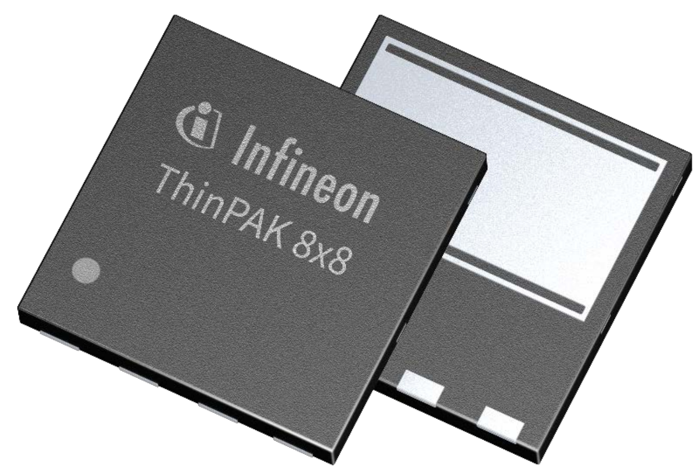
ThinPAK 8*8, high runner for low-to-mid power compact design



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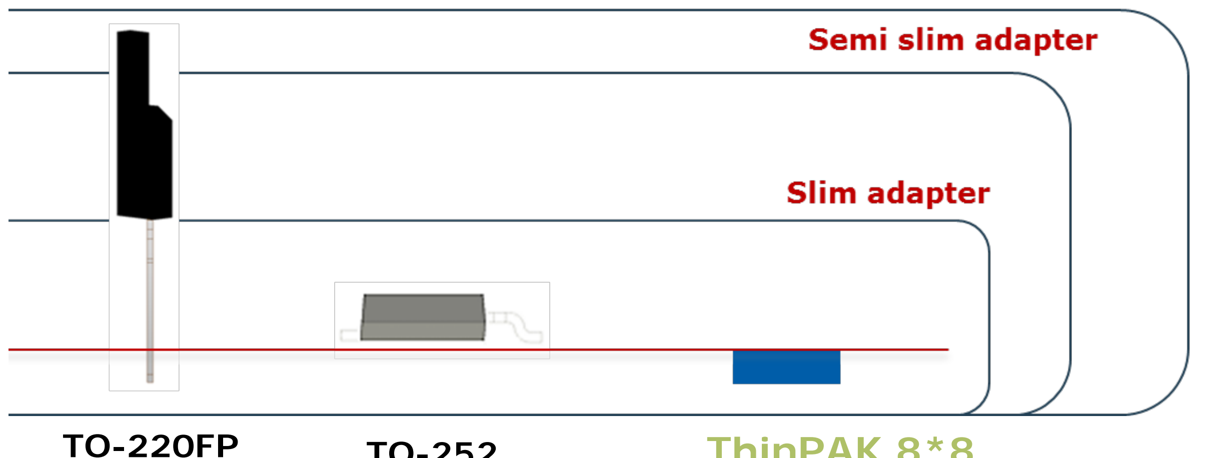
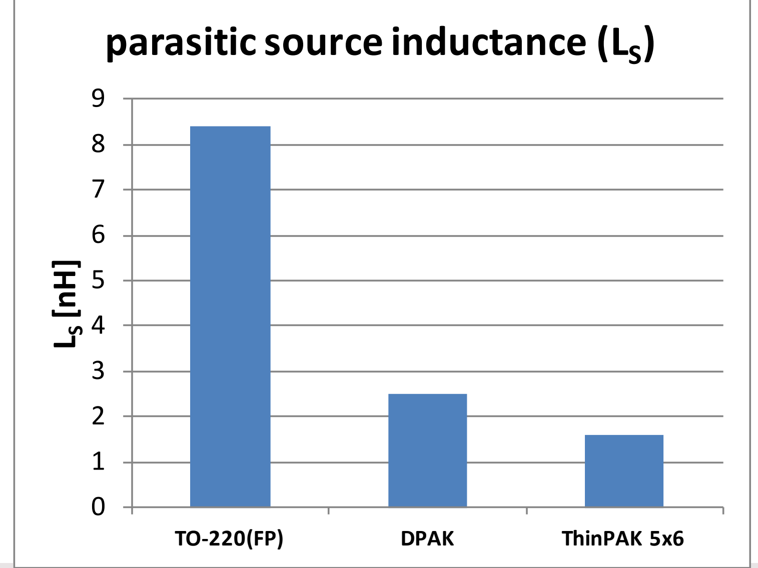
ThinPAK 8*8 – Slim Design





TO-220(FP)

DC	R (mohm)	L(nH)	AC (100MH)	R (mohm)	L(nH)
Gate	32	8.2	Gate	75	7.2
Drain	0.33	5.8	Drain	10.8	5.2
Source	3.7	8.4	Source	34.7	7.4

DPAK

DC	R (mohm)	L(nH)	AC (100MH)	R (mohm)	L(nH)
Gate	28.5	6.2	Gate	71	5.8
Drain	0.002	0.09	Drain	0.53	0.1
Source	2.5	4.7	Source	25	4.5

ThinPAK 5x6

DC	R (mohm)	L(nH)	AC (100MH)	R (mohm)	L(nH)
Gate	38	4.2	Gate	75	3.8
Drain	0.003	0.05	Drain	0.25	0.02
Source	4.5	1.6	Source	12	1.46

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TOLL, recommendation for mid-to-high power with high power density design

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TOLL a replacement for D²PAK - Space and inductance

10.0 mm
15 mm
4.4 mm

9.9 mm
11.7 mm
2.3 mm

Footprint: 150 mm² → Footprint: 115 mm²

30% footprint reduction	50% height reduction	→	60% space reduction

D²PAK		TOLL
5 nH inductance	→	1 nH inductance
RthJc 0.98°C/W	→	RthJc 0.8°C/W

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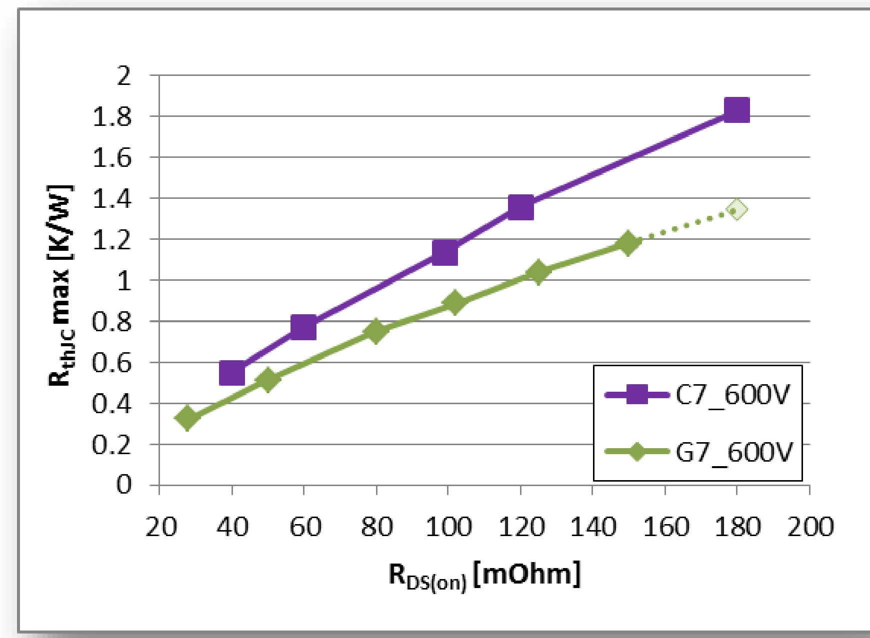
TOLL a replacement for D²PAK - Rth improvement

- Rth is determined by the heat transfer path through the package.
- The thinner the system the better the Rth.



D²PAK
Silicon
solder
lead frame
Cu/solder
PCB with thermal vias
Cu
TIM
Heat sink

TOLL
Silicon
solder
lead frame
Cu/solder
PCB with thermal vias
Cu
TIM
Heat sink

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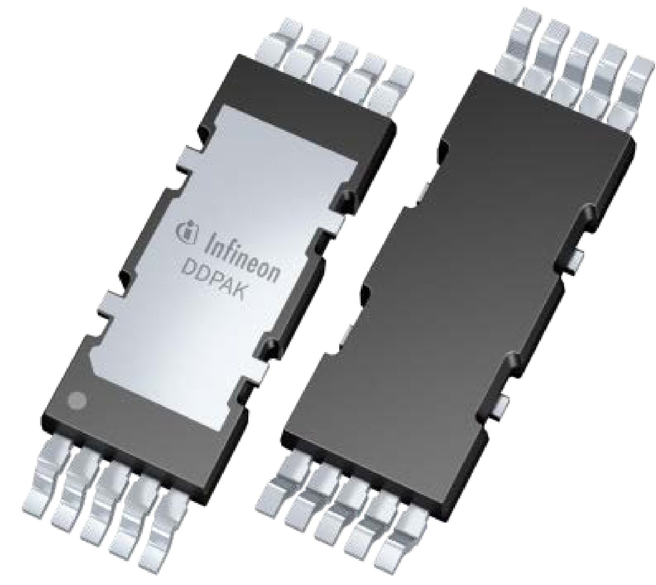
DDPAK, new introduction for compact mid-to-high power design with top-side cooling



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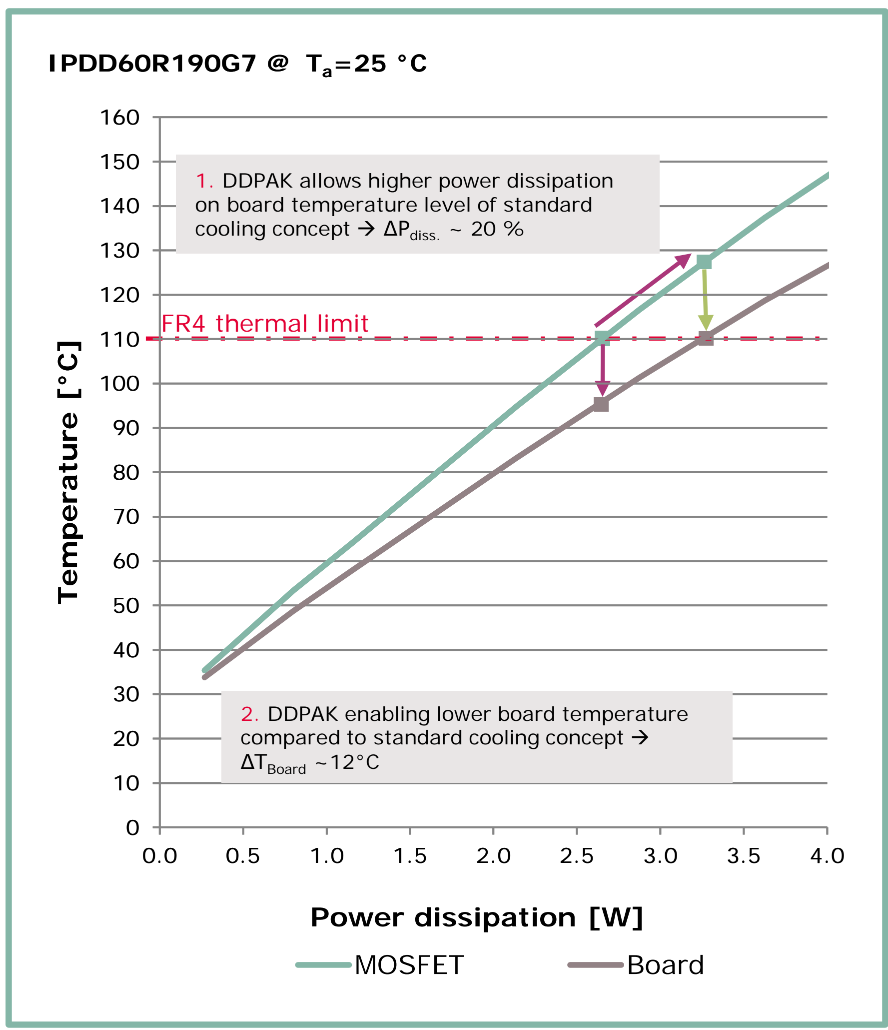
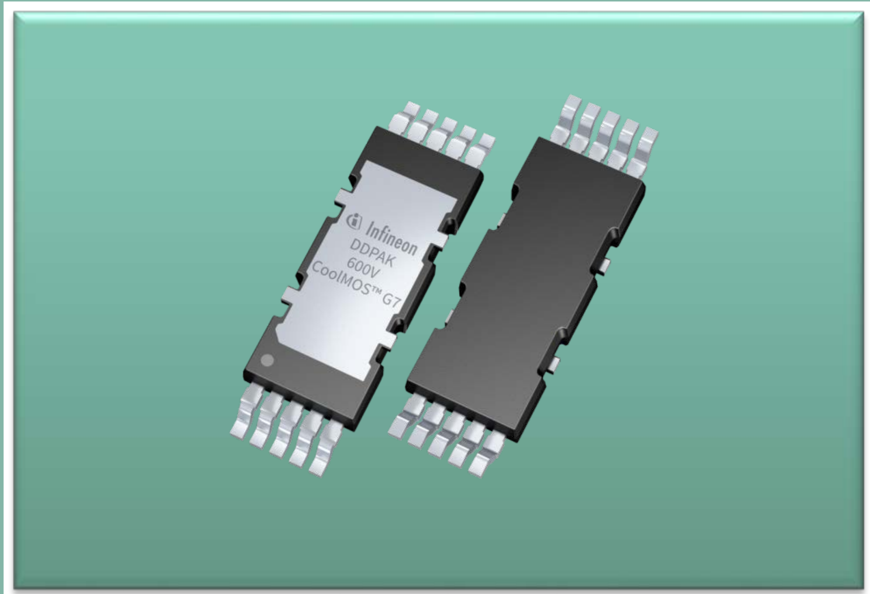
CoolMOS™ and CoolSiC™ in top-side cooled SMD packages enables delta between board and MOSFET temperature

Temperature measurement @ T_a = 25°C



Set up and benefit of top-side cooling concept



In today's common bottom-side cooling concepts the temperature of a PCB equals a MOSFET temperature

The top-side cooling concept of DDPAK allows thermal decoupling of PCB from the chip junction and enables

1. **~ 20% higher power dissipation at the same board temperature or**
2. **improved system lifetime based on reduced board temperature**

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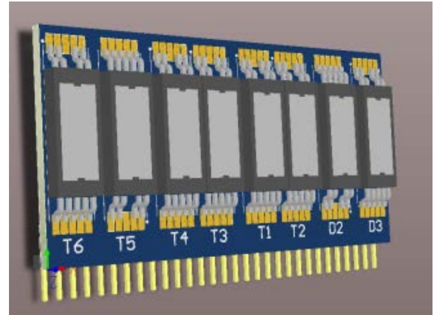
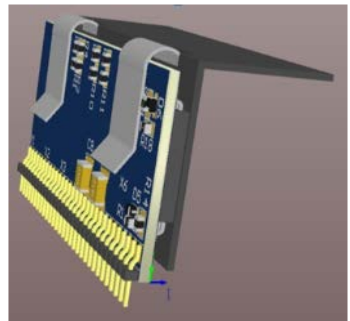
DDPAK offers different variants of mounting approaches

Heatsink with clip mounting





Modular daughter card approach for **server power supply**

- PFC stage: 4x PFC MOSFET, 2x PFC Diode
- LLC stage: 1x high side LLC MOSFET, 1x low side LLC MOSFET

Mounting steps:

1. DDPAK parts are soldered on daughter card using reflow
2. Top-side of the DDPAKs are covered with thermal foil
3. Heatsink is clipped on the top

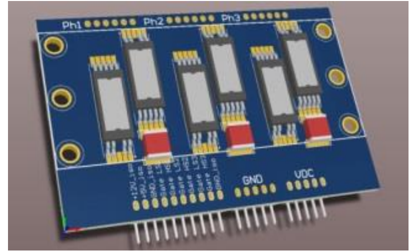
Attention:

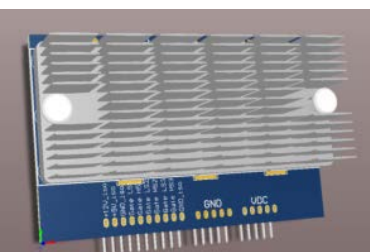
*Drain potential on the top-side is given!

*No wave soldering possible

*this solution is available in our 1600 W Server PSU board

Push pin





Mounting steps:

1. DDPAK parts are soldered on daughter card using reflow
2. Top-side of the DDPAKs are covered with thermal foil
3. Heatsink is fixed with two push pins giving enough contact pressure to realize a reasonable heat transfer

Attention:

*Drain potential on the top-side is given!

*No wave soldering possible

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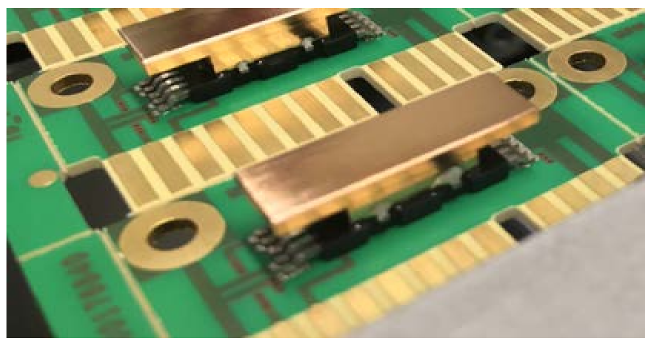
DDPAK offers different variants of mounting approaches

3 Heatsink on top of DDPAK package



The surface of the DDPAK top-side allows heatsinks to be soldered in an additional process step after soldering the package to the PCB.

Mounting steps:

1. DDPAK parts are soldered on daughter card using reflow
2. On the top of DDPAK is added Cu plate
3. The Cu plate is soldered in 2nd reflow step

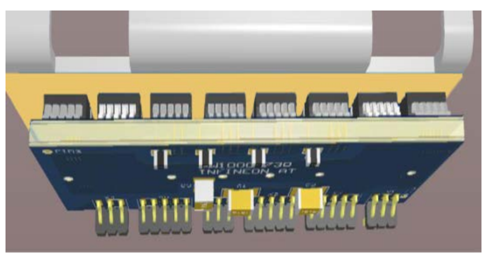
Attention:

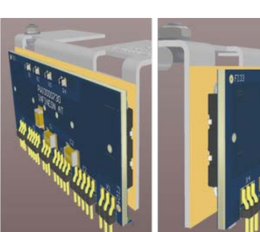
*Drain potential on the top-side is given!

*No wave soldering possible

*For special creepage & clearance requirements it has to be taken into account that the copper plate is not overtopping the connection pins of the package

4 Adhesives





Adhesives create a mechanical attachment of a component to a heat sink. Additionally the thermal transfer properties are guaranteed and the need for additional fasteners is obsolete

Furthermore, low modulus silicone design effectively absorbs mechanical stresses induced by the assembly process, shock and vibration while providing exceptional thermal performance and long-term reliability

Mounting steps:

1. DDPAK parts are soldered on daughter card using reflow
2. Top-side of the DDPAKs are covered with the adhesive
3. Heatsink is placed on the top of it

Attention:

*Drain potential on the top-side is given!

*No wave soldering possible

Daughter card approach enables modularity

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2. Low/Mid Voltage MOSFET

Analog&Digital controller

AC

PFC

HV DC/DC

SR

OR-ing

DC1

DC/DC Brick

DC2

PoL

DC3

Aux.Power

5V,12V

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OptiMOS™ silicon evolution

Size of portfolio

OptiMOS™ 2
- several TO-packages

OptiMOS™ 3
- several TO-packages + SuperSO8

OptiMOS™ 5
- all SMD- and TO-packages

OptiMOS™ 6
- all SMD- and TO-packages

~25% $R_{DS(on)}$ and FOM_g improvement/generation

Generation

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OptiMOS™ 6 in 40V Logic Level

Value proposition

- Low $R_{DS(on)}$ in small package
- Low gate charge
- Low output charge
- Logic level portfolio

R_{DS}(on) FOM

FOM Q_g @V_{GS} = 0 to 10V

$R_{DS(on)\ max.}$ @ 10V [mΩ]

-18%

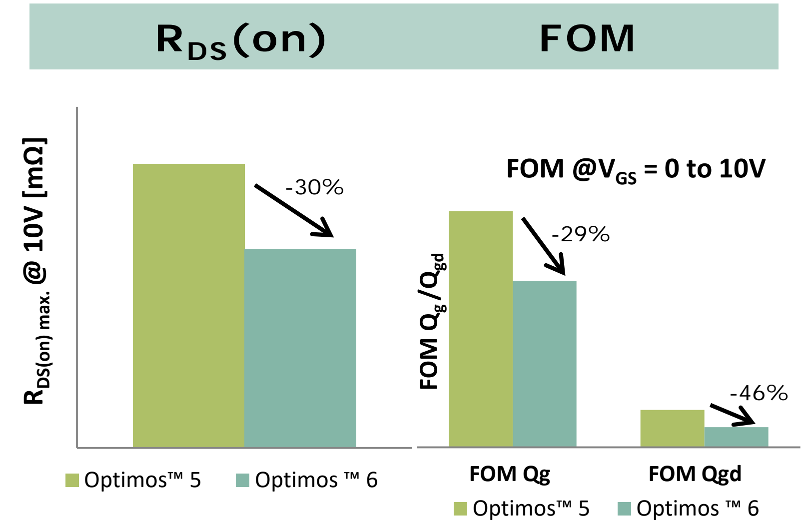
-47%

next best Comp. Optimos ™ 6

next best Comp. Optimos ™ 6

Target specifications

Part number	$R_{DS(on)}$max. @V_{GS} = 10V	Package	Release schedule
BSC007N04LS6	0.7mΩ	5*6	Released
BSC010N04LS6	1.0mΩ	5*6	Released
BSC022N04LS6	2.2mΩ	5*6	Released
BSC059N04LS6	5.9 mΩ	5*6	Released
BSZ021N04LS6	~2.1mΩ	3*3	Released
BSZ024N04LS6	~2.4mΩ	3*3	Released
BSZ063N04LS6	~6.3mΩ	3*3	Released



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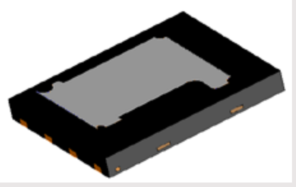
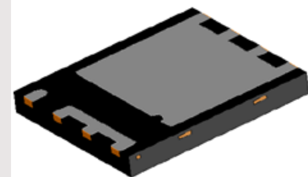
OptiMOS™ 5 SuperCool Overview

Target Applications

- Telecom DCDC/SR
- Server SR
- Drives/Motor control/Inverters
- Battery powered applications





Value Proposition(s)

- Increased power density leading to highest system efficiency
- Provides double-sided cooling possibility → Relief thermal requirements on PCB designs
- Achieve a next level of thermal performance esp. when forced airflow & heatsink are used
- Standard SuperSO8 footprint means drop-in replacements to standard designs

Target Specifications

Part Number	V_{DS} (V)	(*) $R_{DS(on)}$ max @V_{GS} = 10 V (mΩ)	(*) Rth_{JC_top} / Rth_{JC_bot} typ.	Package	Release Schedule
BSC010N04LSSC	40	1.0	1 k/w / 0.5 k/w	SuperSO8 + exposed clip	Q3 2019
BSC013N06NSSC	60	1.3	1 k/w / 0.5 k/w	SuperSO8 + exposed clip	Q3 2019
BSC016N06NSSC	60	1.6	1 k/w / 0.5 k/w	SuperSO8 + exposed clip	Q3 2019
BSC030N08NS5SC	80	3.0	1 k/w / 0.5 k/w	SuperSO8 + exposed clip	Q3 2019
BSC040N10NS5SC	100	4.0	1 k/w / 0.5 k/w	SuperSO8 + exposed clip	Q3 2019
BSC070N10NS5SC	100	7.0	1 k/w / 0.5 k/w	SuperSO8 + exposed clip	Q3 2019

**Target values only, subject to changes*

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Tj.max=175℃ Offers More Safe Operating Area

Product description

- OptiMOS™ 5 175°C in SuperSO8 is the new package family that achieves higher performance or longer life time with same performance compared to 150°C SuperSO8

Package	V_{DS} [V]	Part number	$R_{DS(on)}$ max @ V_{GS} = 10 V [mΩ]
SuperSO8	30 V	BSC011N03LST	1.1
	40 V	BSC010N04LST	1.0
		BSC014N04LST	1.4
		BSC019N04LST	1.9
	60 V	BSC014N06NST	1.4
		BSC016N06NST	1.6
		BSC019N06NS	1.9
		BSC028N06NST	2.8
		BSC097N06NST	9.7

- Products are in Mass Production

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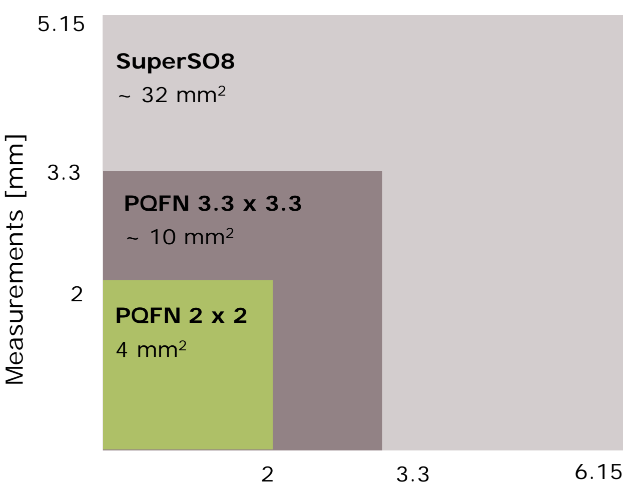
Compact Design with PQFN2*2 Package



- Infineon's latest generation of power MOSFETs in PQFN 2 x 2 package utilize **OptiMOS™ 5** logic level silicon to achieve benchmark performance in high speed switching and small form factor applications

Vds [V]	Part number	RDS(on) max. @VGS = 10 V [mΩ]	RDS(on) max. @VGS = 4.5 V [mΩ]	Qg (typ.) @VGS = 4.5 V [nC]	Release schedule
25	ISKE2N001LM5	<4.0	<5.0	~6.0	Q3 2019
30	ISK03N001LM5	<5.0	<6.0	~6.5	Q3 2019
40	ISK04N017LM5	<9.0	<12.0	~11.0	Q3 2020
60	IRL60HS118	17.0	23.5	5.3	MP
80	IRL80HS120	32.0	42.0	4.7	MP
100	IRL100HS121	42.0	59.0	3.7	MP

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3. Power of Load

AC

Analog&Digital controller

PFC

HV DC/DC

SR

OR-ing

DC1

DC/DC Brick

DC2

PoL

DC3

Aux.Power

5V,12V

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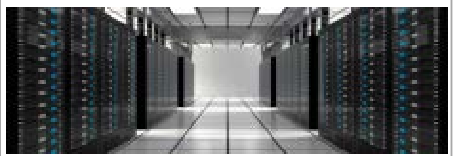
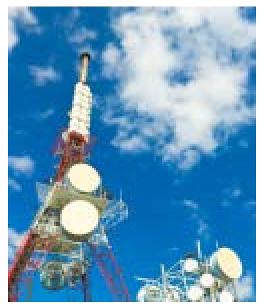
Enterprise Power Market Definition

Three Vehicals			
Server	**Communication**		**High-end Consumer**
	Datacom	Telecom	
			
• Server-Intel/IBM/ AMD/ARM • Workstation • Storage	• Comms Core • SOHO SAN • Edge Access	• Basestation (Macro + Distributed)	• HE Desktop • Notebook • Gaming • Graphic • Industrial PC

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Basic topology

Vin (5V ... 12V)

Power Stage

Vout (0.5V ... 2.5V)

IFX = Digital = Smart

gnd

IFX = Robust = Efficient

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EP Scope and Segmentation With Power MAP

Application Roadmap Scope

Segment	Gaming	Graphic Cards	Desktop	Server CPU, DDR, POL	AI Core	Datacom/ Networking/ Storage
Group	"Client" Intel / AMD / nVIDIA	"Client" Intel / AMD / nVIDIA	"Client" Intel / AMD / nVIDIA	"HPC" Intel / AMD / IBM-P / ARM	"HPC" Intel / AMD / IBM-P / ARM	ASICS / FPGAs / SSD
Future power levels	150W	400+W	200W	400+W	400+W	400+W
Current power levels		200+W	150W	200+W	200+W	200+W

Processor thermal design point (TDP): 100W, 150W, 200W, 250W, 300W, 400W

Legend: Future power levels; Current power levels

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EP Product Categories

Enterprise Power

Digital Controllers & IC's

Integrated Power Stages

uDrMOS 5x4

Integrated POL Voltage regulators

Bare Die

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4. CoolSET™ for Aux.Power

Analog&Digital controller

AC

PFC

HV DC/DC

SR

OR-ing

DC1

DC/DC Brick

DC2

PoL

DC3

Aux.Power

5V,12V

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Gen5 quasi CoolSET™ and standalone controller family

Max Pout 85~300 V_{AC} Ta=50°C	15 W	22 W	27 W	32 W	41-42 W	60 W
DSO-8						ICE5QSAG
DIP-7	ICE5QR4770AZ ICE5QR4780AZ	ICE5QR2270AZ ICE5QR2280AZ		ICE5QR1070AZ	ICE5QR0680AZ	
DSO-12	ICE5QR4770AG		ICE5QR1680AG		ICE5QR0680AG	

A – Auto-restart

ICE	5	Q/A/B/G	R	2	2	7	0	A	Z

5th Generation PWM controller

Frequency Switching Scheme
- Q : Quasi-Resonant
- A : fixed 100 KHz
- B : fixed 65 KHz
- G : fixed 125 KHz

Variant
- S : Controller only
- R : CoolSET™

Typ. $R_{DS(ON)}$ of the integrated MOSFET
Eg. 2.2 Ω

VDS of the integrated MOSFET
- 70 = 700 V
- 80 = 800 V

Package
- Z = DIP-7
- G = DSO-12/16

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Key differences between 2nd & 5th Gen QR

Features	2QR	5QR
Integrated MOSFET	650 V @ T_j=110°C 800 V @ T_j=25°C	700 V @ T_j=25°C 800 V @ T_j=25°C
Start-up cell	Yes	Cascode
Novel QR switching		✓
Selectable active burst Mode entry/exit		✓
Protection mode • Output OVP	Latch	Auto-restart
Protection coverage • Line over-voltage • Brown IN/Out • CS short to ground • VCC short to ground • OTP with hysteresis		✓
Pin out		Same package but different pin assignment

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Efficiency measurement @ 230 V_{AC}

Efficiency (%)

86.0%
85.0%
84.0%
83.0%
82.0%
81.0%
80.0%
79.0%
78.0%
77.0%
76.0%

Gen5 ~1% improvement

25% (3.92W)
50% (7.83W)
75% (11.75W)
100% (15.68W)

Load

ICE5QR4780AZ
ICE2QR4780Z

Note: Test was conducted using 15.4W demoboard based on ICE5QR4780AZ and ICE2QR4780Z under an open frame and room temperature condition.

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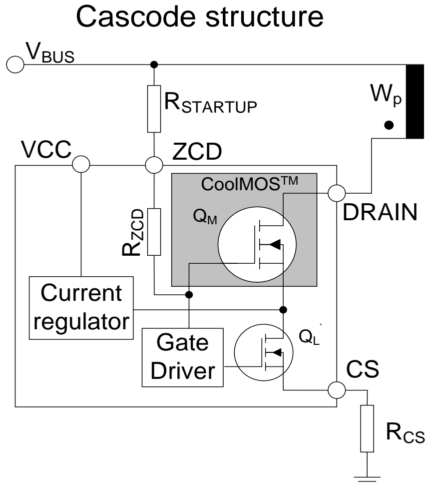
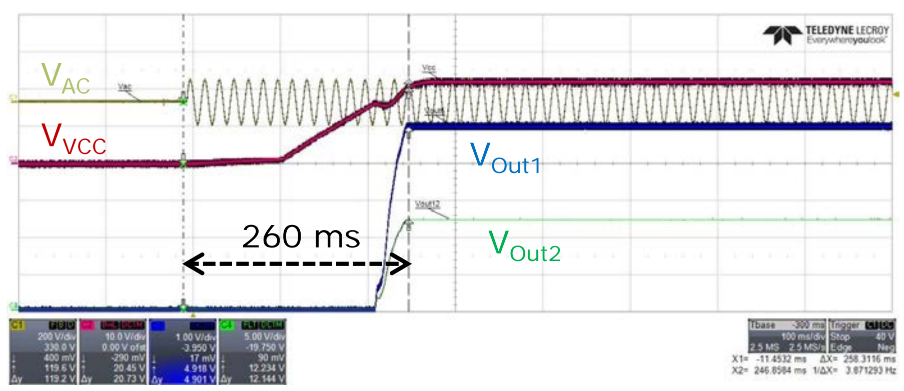
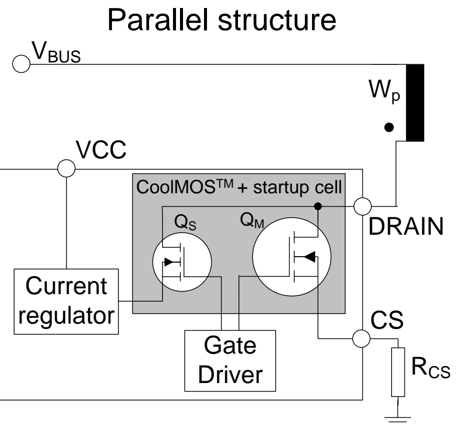
Fast & robust start-up with cascode configuration



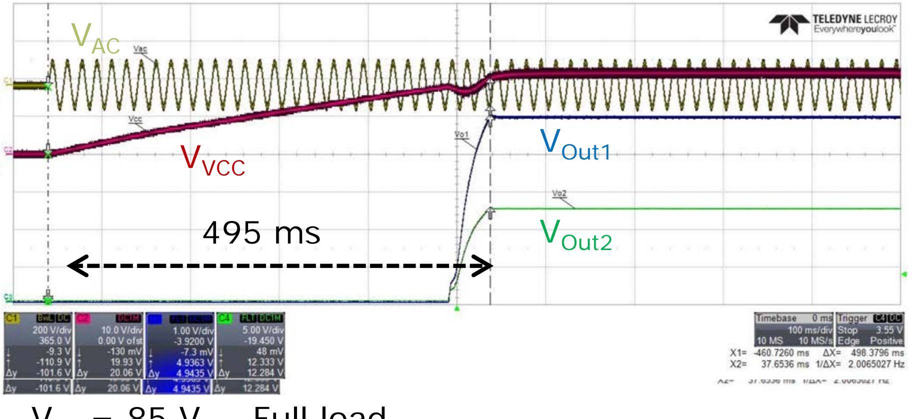
QR Gen5 CoolSET™ (ICE5QR4780AZ)



V_{IN} = 85 V_{AC}, Full load
$R_{STARTUP}$ = 45 MΩ, $t_{STARTUP}$ = 260 ms



QR Gen2 CoolSET™ (ICE2QR4780Z)



V_{IN} = 85 V_{AC}, Full load
$t_{STARTUP}$ = 495 ms

Result

- Gen2 → 495 msec
- Gen5 → 260 msec

Conclusion

- Gen5 start-up can be 1.9x faster than Gen2

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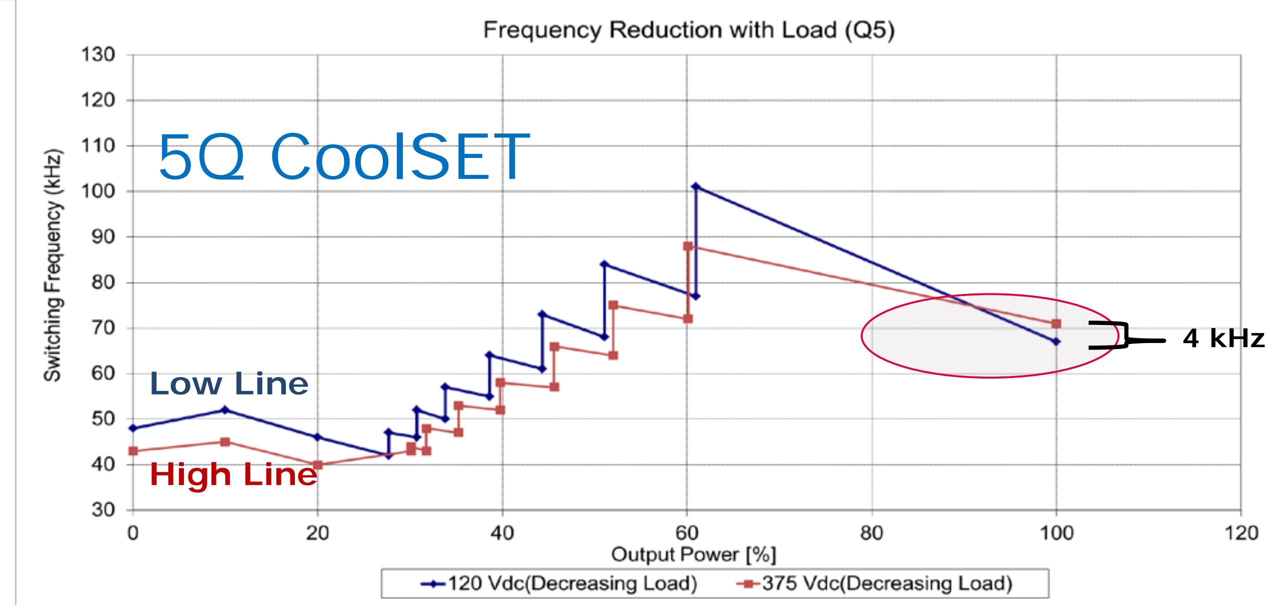
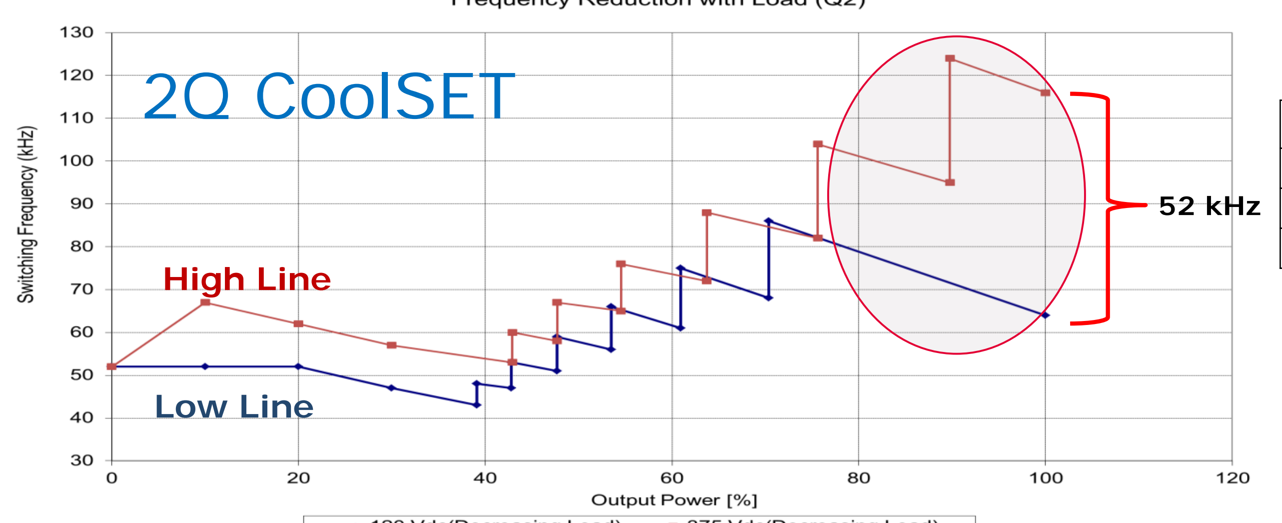
Gen5 & Gen2 QR switching frequency comparison





- With the introduction of Novel Quasi Resonant Switching scheme, 5Q is able to minimize the switching frequency spread between low and high line.
- For 5Q, the switching frequency between high line and low line full load is just 4 kHz (52 kHz for 2Q).

	Full load		
f_s	Low Line	High Line	HL - LL
5Q	67 kHz	71 kHz	4 kHz
2Q	64 kHz	116 kHz	52 kHz
5Q - 2Q	3 kHz	-45 kHz	

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Gen5 & Gen2 QR Conducted EMI Comparison 230 V_{AC} / Full Load

EN_V_QP
EN_V_AV
PK 5Q(230L FL)
PK 2Q(230L FL)
QP limit
AV limit
dBµV
f / MHz

Note:
Test was conducted on the same demo board and same power under open frame and room temperature condition. The measurement are peak measurement

Tested CoolSET :
QR Gen5 ICE5QR4780AZ (R)
QR Gen2 ICE2QR4780Z (P)

- Red curve : Gen5 QR ICE5QR4780AZ, Purple curve : Gen2 QR ICE2QR4780AZ
- Both curves can pass the limit with >6 dB margin. Gen5 QR is lower by 3 dB ~ 5dB in low and mid band frequency than Gen2 QR.

Conclusion: *Novel QR able to limit spread of switching frequency between high/low line input and thus, lower EMI signature*

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