

# ModusToolbox™ Programmer GUI user guide

#### Version

5.0.0

## About this document

#### Scope and purpose

ModusToolbox<sup>™</sup> Programmer is a stand-alone, cross-platform, flash programmer tool that provides a graphical user interface to Program, Erase, Verify, and Read the flash of the target device. It is delivered with the ModusToolbox<sup>™</sup> Programming tools package, and it supports HEX, SREC, ELF, and BIN programming file formats.

#### **Intended** audience

This document helps you learn how to use the ModusToolbox<sup>™</sup> Programmer GUI to perform various operations on devices.

#### **Reference documents**

Refer to the Infineon programming solutions website for more information as needed.

#### **Document conventions**

Convention	Explanation			
Bold Emphasizes heading levels, column headings, menus and sub-menus				
Italics	Denotes file names and paths.			
Courier New	Denotes APIs, functions, interrupt handlers, events, data types, error handlers, file/folder names, directories, command line inputs, code snippets			
File > New	Indicates that a cascading sub-menu opens when you select a menu item			

#### **Abbreviations and definitions**

The following define the abbreviations and terms used in this document:

Term	Description
CMSIS	Arm <sup>®</sup> Cortex <sup>®</sup> Microcontroller Software Interface Standard.
CMSIS-DAP	CMSIS Debug Access Port.
OpenOCD	The Open On-Chip Debugger is the debugger tool that provides on-chip programming support. This tool acts as a backend of the ModusToolbox™ Programmer application.
Data File	The data file for programming in the hex or binary format
DP	The Debug Port register of the Arm Cortex CPU. Used for programming and debugging, along with the corresponding SWD-address bit selections.
Flash kernel/loader	The firmware file loaded into the MCU's RAM. Sometimes referred to as RAM program, Flash kernel, Flash loader.
GDB	GNU Project Debugger – GNU.org.

# ModusToolbox™ Programmer GUI user guide



# About this document

Term	Description
JTAG	Joint Test Action Group. Specifies the use of a dedicated debug port while implementing a serial communication interface for low-overhead access without requiring direct external access to the system address and data buses.
МСИ	Microcontroller Unit.
PSoC™	A family of microcontroller integrated circuits. These chips include a CPU core and mixed-signal arrays of configurable integrated analog and digital peripherals.
Region	Logical areas within the target device the programmer operates on.
SWD	Serial Wire Debug interface.
QSPI	Quad Serial Peripheral Interface. A name used for SPI external memory interfaces



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#### Overview

# 1 Overview

ModusToolbox<sup>™</sup> Programmer supports the following features:

- Programming Infineon MCUs' internal and external memories
  - PSoC<sup>™</sup> 6 MCUs, including corresponding starter kits and evaluation boards
  - PSoC<sup>™</sup> 4 MCUs, including corresponding starter kits and evaluation boards
  - PMG1 and WLC1 MCUs, including corresponding evaluation boards
  - EZ-PD<sup>™</sup> CCG7S and CCG7D MCUs, CCG4, CCG3PA, CCG8
  - XMC7100/7200, CYT4BB/BF, CYT2Bx
- AIROC<sup>™</sup> Wi-Fi/Bluetooth<sup>®</sup> platforms (CYW4390x, CYW4343W, CYW20829, CYW208xx, CYW55513 and others), including corresponding starter kits and evaluation boards
- Connectivity devices via support of development boards
- Windows, Linux, and macOS
- Programming external memory devices using PSoC<sup>™</sup> 6 external memory interfaces (EBI / QSPI)
- Programming external memory of AIROC<sup>™</sup> Wi-Fi devices
- KitProg3 and MiniProg4 hardware
- SEGGER J-Link Base and J-Link Ultra hardware
- OpenOCD via machine interface (MI) to 3rd party debug hardware
- Cross-platform Bridge library I<sup>2</sup>C, SPI, UART communications
- KitProg3 firmware update



### Installing ModusToolbox™ Programmer

# 2 Installing ModusToolbox<sup>™</sup> Programmer

ModusToolbox<sup>™</sup> Programmer is delivered as part of the ModusToolbox<sup>™</sup> Programming tools package. A link is available to download/install from the IDC webpage here:

https://www.infineon.com/cms/en/design-support/tools/programming-testing/psoc-programming-solutions/

For installation details, see section 2 of the ModusToolbox™ Programming tools release notes.



# **3 Getting started**

### 3.1 Run ModusToolbox<sup>™</sup> Programmer

To run the ModusToolbox<sup>™</sup> Programmer GUI application, navigate to the ModusToolbox<sup>™</sup> Programming tools install location, open the *mtb-programmer* folder, and run the executable. See <u>Installing ModusToolbox<sup>™</sup></u> <u>Programmer</u>. The GUI opens and looks similar to this:

				_			
mtb-programmer					_		×
File View Options He	lp						
Open Probe/Kit: None	V Platform: V	ower (	Connect	) Erase	Program	Contraction Read	<b>Verify</b>
Settings							×
Program Settings File Reset Chip	C:/hex/lubm/CY8C6347BZI-BLD53_smif_internal_ba	nk.hex					
Probe Settings							
Info : [CyBridge] Sta Info : [CyBridge] The	art the API initialization e hardware initialization has complete	d in 57	2 ms				
Please attach USB probe devie	e to proceed				No	t Conne	cted

In this case, no kit or device is connected, and a message displays asking you to connect a device.



# 3.2 Load programming file

1. Connect the device to the host computer. Select the device name in the **Probe/Kit** drop-down, and ModusToolbox<sup>™</sup> Programmer will display information under **Probe Settings** (if the **Settings** section is viewable).

mtb-programmer						_		×
File View Options Hel	p 062-WiFi-BT-1616176C0322:	orm: PSoC 61/6 ¥	(1) Power	Connect	<b>D</b> Erase	Program	Read	<b>Verify</b>
Settings								×
Program Settings File Reset Chip Verify Regions External Memory Program Security Data								
Probe Settings Interface Voltage (V) Reset Type Sflash Restrictions	SWD 3.3 Soft Erase/Program Sflash prohibited							*
Info : [CyBridge] Sta Info : [CyBridge] Har Info : Connected - Ki Info : Selected Devic	rt API initialization dware initialization comple tProg3 CMSIS-DAP BULK-16161 e: CY8CKIT-062-WiFi-BT-1616	te 825 ms 76C03227400 FW 176C03227400	V Versio	on 2.21.10	005			
Press F1 for help				Powered: 3	255 mV	Not C	onnected	н.

#### 2. Click **Open**.

mtb-programmer				_		×
<u>File View Options H</u> elp						
Probe/Kit: CY8CKIT-062-WiFi-BT-1616176C0322:  Platform: PSoC 61/6	(U) Power	Connect	<b>D</b> Erase	Program	Read	<b>Verify</b>

On the Open Programming File dialog, navigate to the location of the HEX, SREC, ELF, or BIN file to load, select it, and click **Open**.

🔯 Open Programming File		×
$\leftarrow$ $\rightarrow$ $\checkmark$ $\uparrow$ $\blacksquare$ « Windows (C:) $\Rightarrow$ hex	> CY8CKIT-062-BLE ~ ひ	Search CY8CKIT-062-BLE
Organize   New folder		: • 1
<ul> <li>OneDrive</li> </ul>	^ Name	Date modified Type
This PC	ble_app.elf	7/22/2019 1:19 PM ELF File
3D Objects	BlinkyLED_mainapp_final.elf	4/12/2019 5:35 PM ELF File
	BlinkyLED_mainapp_final.hex	6/19/2019 2:02 PM HEX File
Documents		
Downloads		
Music		
E Pictures		
📕 Videos		
€ <sup>⊕</sup> Windows (C:)		
🥩 Network	× <	>
File name: BlinkyLED_mai	napp_final.hex v	Programming Files (*,hex *.srec ~ <u>Open</u> Cancel



# 3.3 Connect device

1. If the device is not powered, the status message "Not Powered" is displayed in the Status Bar. Click **Power** to power up the device.

mtb-programmer					_		×
<u>File View Options</u>	lelp						
Open Probe/Kit: CY8CKI	T-062-WiFi-BT-1616176C0322:  Platform: PSoC 61/6  Por	0 ower	Connect	D Erase	Program	Read	<b>Verify</b>
Settings							×
Program Settings File Reset Chip Verify Regions External Memory Program Security Dat	C:/hex/CY8CKIT-062-BLE/BlinkyLED_mainapp_final.hex						
Probe Settings Interface Voltage (V) Reset Type Sflash Restrictions	SWD 3.3 Soft Erase/Program Sflash prohibited						* *
og Info : [CyBridge] Si Info : [CyBridge] Hi Info : Connected - b Info : Selected Dev:	tart API initialization ardware initialization complete 804 ms (itProg3 CWSIS-DAP BULK-1616176C03227400 FW Ve ice: CY8CKIT-062-WiFi-BT-1616176C03227400	ersion	2.21.1	005			
Press F1 for help			Not Pow	ered	Not (	Connected	ł

2. Click **Connect**. ModusToolbox<sup>™</sup> Programmer communicates with the device and displays various messages in the **Log**. Then, a message in the Status Bar indicates that it is connected.

mtb-programmer				-		×	
<u>File View Options He</u>	lp						
Open Probe/Kit: CY8CKIT-	062-WiFi-BT-1616176C0322: - Platform: PSoC 61/6: - Po	ower Disconnect	Erase	C Program	Read	<b>Verify</b>	
Settings						×	
Program Settings							
File Reset Chip > Verify Regions External Memory Program Security Data	C:/hex/CY8CKIT-062-BLE/BlinkyLED_mainapp_final.hex						
Probe Settings							
Interface Voltage (V)	SWD 3.3					Ţ	
Reset Type Sflash Restrictions	Soft Erase/Program Sflash prohibited					7 7	
Log							
<pre>Info : #1 : psoc6_main_cm0 (psoc6) at 0x10000000, size 0x00000000, buswidth 4, chipwidth 4 Info : #1 : psoc6_work_cm0 (psoc6) at 0x140000000, size 0x00008000, buswidth 4, chipwidth 4 Info : #2 : psoc6_super_cm0 (psoc6) at 0x160000000, size 0x000000000, buswidth 4, chipwidth 4 Info : #3 : psoc6_super_cm0 (psoc6) at 0x10000000, size 0x000000000, buswidth 0, chipwidth 1 Info : #4 : psoc6_main_cm4 (virtual) at 0x10000000, size 0x000000000, buswidth 0, chipwidth 0 Info : #5 : psoc6_work_cm4 (virtual) at 0x10000000, size 0x000000000, buswidth 0, chipwidth 0 Info : #5 : psoc6_super_cm4 (virtual) at 0x10000000, size 0x000000000, buswidth 0, chipwidth 0 Info : #7 : psoc6_super_cm4 (virtual) at 0x10000000, size 0x000000000, buswidth 0, chipwidth 1 Info : cyp status: 0K Info : cyp get_mpn Info : ** Detected device PN: CY8C62478ZI-D54 SiliconID: E206 Revision: 22 FamilyID: 100 DIE: PSoC6ABLE2 v</pre>							
Connected to the target devic	e	Powered: 3	256 mV	CY8C624	47BZI-DS	54	



# 3.4 Program device

Click **Program**. ModusToolbox<sup>™</sup> Programmer downloads the program file onto the device and displays messages in the **Log**.

mtb-programmer	- 0	×				
<u>File View Options H</u>	elp					
Open Probe/Kit: CY8CKIT	r-062-WIFI-BT-1616176C0322: Y Platform: PSoC 61/6: Y Over Disconnect Frase Program Read	<b>Nerify</b>				
Settings		×				
Program Settings						
File Offset Reset Chip > Verify Regions External Memory Program Security Dat	C:/hex/CY8CKIT-062-BLE/BlinkyLED_mainapp_final.elf  tx0  a					
Probe Settings						
Interface	SWD					
Voltage (V)	3.3					
Reset Type	Soft					
Sflash Restrictions	Erase/Program USER/TOC/KEY allowed	19				
Log						
<pre>Info : [100%] [####################################</pre>						
Device programmed success	fully Powered: 3253 mV CY8C62478ZED5	4				

# 3.5 Save log file

Right-click in the **Log** section and select **Save As**.

Log		
Info : target halted due to debug-request, current mode: Thread		
Info : xPSR: 0x61000000 pc: 0x1600400c msp: 00000000		
Info : ** Programming Started **		
Info : auto erase enabled		
Info : Flash write discontinued at 0x100019a0, next section at 0x1	10002000	
Info : Padding image section 3 at 0x100019a0 with 96 bytes (bank	Copy	hment)
Info : [100%] [####################################		
Info : [100%] [####################################	Select All	
Info : Padding image section 7 at 0x10004a10 with 496 bytes (ban	Jereet / III	gnment)
Info : [100%] [####################################	Save As	
Info : [100%] [####################################	Clear	
Info : wrote 17920 bytes from file D:/hex/BlinkyLED_mainapp_fina_	Cical	24s (20.034 KiB/s)
Info : ** Programming Finished **		-
Info : cyp status: OK		
Info : cyp_get_mpn		
Info : ** Detected device PN: CY8C6247BZI-D54 SiliconID: E206 Revi	ision: 22 Fam:	ilyID: 100 DIE: PSoC6ABLE2 📒
Info : true		-
Device programmed successfully	Powere	ct: 3257 mV CY8C6247BZI-D54

Note:

You can also select the **Select All** command to select the text, then copy and paste the text to the file you selected.



# 4 GUI description

ModusToolbox<sup>™</sup> Programmer contains menus and toolbar commands to perform actions. This chapter describes the various GUI elements.

mtb-programmer	· · · · · · · · · · · · · · · · · · ·		×
File View Options H	<u>l</u> elp		
Open Probe/Kit: CYBCKI	IT-062-WIFI-BT-1616176C0322:  Platform: PSoC 61/6:  Power Disconnect Frase Program	m Read	<b>S</b> Verify
Settings			×
Program Settings File Offset Reset Chip > Verify Regions External Memory Program Security Da	C:/hex/CY8CKIT-062-BLE/BlinkyLED_mainapp_final.elf 0x0		
Probe Settings			
Interface Voltage (V) Reset Type Sflash Restrictions	SWD 3.3 Soft Erase/Program USER/TOC/KEY allowed		* * *
Log Info : flash 'psoc6 Info : #0 : psoc6 m Info : #1 : psoc6_w Info : #2 : psoc6_s Info : #3 : psoc6_e Info : #4 : psoc6_w Info : #5 : psoc6_w Info : #6 : psoc6_s Info : #7 : psoc6_s Info : cyp status: Info : cyp status: Info : cyp_get_mpn Info : ** Detected of Psoc6ABLE2	_efuse' found at 0x90700000 ain_cm0 (psoc6) at 0x10000000, size 0x00100000, buswidth 4, chipwidth 4 ork_cm0 (psoc6) at 0x14000000, size 0x00008000, buswidth 4, chipwidth 4 uper_cm0 (psoc6) at 0x16000000, size 0x00008000, buswidth 4, chipwidth 4 fuse_cm0 (psoc6_efuse) at 0x90700000, size 0x00000000, buswidth 1, chipwi ain_cm4 (virtual) at 0x10000000, size 0x00000000, buswidth 0, chipwidth 0 ork_cm4 (virtual) at 0x14000000, size 0x00000000, buswidth 0, chipwidth 0 uper_cm4 (virtual) at 0x16000000, size 0x00000000, buswidth 0, chipwidth fuse_cm4 (virtual) at 0x90700000, size 0x00000000, buswidth 0, chipwidth fuse_cm4 (virtual) at 0x90700000, size 0x00000000, buswidth 1, chipwidth fuse_cm4 (virtual) at 0x90700000, size 0x00000000, buswidth 1, chipwidth fuse_cm4 (virtual) at 0x90700000, size 0x00000400, buswidth 1, chipwidth fuse_cm4 (virtual) at 0x90700000, size 0x00000000, buswidth 1, chipwidth OK	dth 1 0 1	~
Connected to the target dev	rice Powered: 3255 mV CY8C	62478ZI-D54	4

### 4.1 Menus

# 4.1.1 File

The **File** menu contains the following commands:

- **Open (Ctrl+O)** Opens the programming file.
- **Connect/Disconnect (Alt+Q)** Connects and disconnects the selected device.
- **Program (Alt+G)** Programs the selected device with the selected file.
- Erase (Alt+E) Erases the selected device.
- Read (Alt+R) Reads flash of the selected device into a HEX or SREC file.
- Verify (Alt+Y) Verifies that the selected device is programmed correctly.
- Recent Files Lists up to five recently loaded programming files.
- Exit (Alt+F4) Closes the ModusToolbox<sup>™</sup> Programmer application.



#### 4.1.2 View

The **View** menu contains the **Settings** check box. Select it to view the **Settings** section of the window; unselect it to hide the **Settings** section. See <u>Settings</u>.

## 4.1.3 Options

The **Options** menu contains the following commands:

# 4.1.3.1 Programmer Options (Alt+T)

Opens the **Programmer Options** dialog to set the **Upgrade Firmware** mode and other options.

Programmer Options - mtb-programmer X					
Name	Value				
Upgrade Firmware	Show Pop-Up $\sim$				
OpenOCD Telnet Port	4445				
	OK Cancel				

- Upgrade Firmware mode:
  - Automatically The firmware is updated automatically when the tool opens.
  - **Show Pop-up** A dialog displays asking if you want to upgrade the firmware.
  - **Ignore** The firmware is not updated and no prompt displays.
- **OpenOCD Telnet Port**: This option specifies the port number of the OpenOCD telnet connection.

# 4.1.3.2 Upgrade Firmware (Alt+U)

When this command is enabled, select it to upgrade the programmer firmware on the device.

### 4.1.4 Verify Regions

The Verify Regions menu is available only if Verify Regions option is selected in Program Settings.

- Add Region Adds a custom flash region to the Verify Regions list.
- **Reload Regions** Resets the **Verify Regions** list to the default state corresponding to the flash map of the target.
- Undo (Ctrl+Z) Undo the last change in the Verify Regions list.
- Redo (Ctrl+Y) Redo the last change in the Verify Regions list.
- **Verify –** Initiates the Verify device operation.

# 4.1.5 Help

The Help menu contains the following commands:

- View Help (F1) Opens this document.
- About mtb-programmer Opens the About box.



# 4.2 Toolbar

The toolbar contains the **Open, Connect, Erase, Program, Read,** and **Verify** commands, which are also located on the <u>File menu</u>. This area also contains the following:

# 4.2.1 Probe/kit and platforms

If you have more than one device connected to your computer, use these pull-down menus to select the specific probe and target platform to use.





### 4.2.2 Power

Use the **Power** Use the power on and off the selected device.

# 4.2.3 Connect

Use the **Connect** Use the **Connect** button to connect to and disconnect from the selected device.



# 4.2.4 Settings

The **Settings** section of the tool allows you to update the program and probe/target settings as follows:

## 4.2.4.1 **Program Settings**

- File Use this to select the programming file to perform actions on or with.
- **Offset** This is an optional offset parameter; it can be an integer or hexadecimal value. The relocation offset is added to the base address for each section in the image when the image is programmed. This option is visible only if a binary or elf file is selected for programming operations.
- **Reset Chip** Use this to reset the chip after the Program operation completes. This option resets the target chip and runs the programmed firmware on it.
- Verify Regions Use this option to define flash regions used during device verification. This allows to verify user defined flash regions of the PSoC<sup>™</sup> MCU. This option does not change behavior of the Program operation. See <u>Verify Custom Flash Regions of PSoC<sup>™</sup> 6 MCU</u> for details.
- **External Memory** Enables/disables the programming of external memory in the target device. For PSoC<sup>™</sup> 6x MCUs, this option enables programming of the QSPI regions. This is also used for programming external memory of AIROC<sup>™</sup> Wi-Fi devices.
- **Program Security Data** Allows programming security regions if the target device supports this capability. For example, for PSoC<sup>™</sup> 61 PSoC<sup>™</sup> 62, and PSoC<sup>™</sup> 63 MCUs, this option enables programming the eFuse region.
- **Target AP** Allows you to select the target access port (DAP) that will be used for programming. Possible values include: CM0, CM4, and SYS\_AP. This option is available only for PSoC<sup>™</sup> 64 MCUs.
- Flash Size Limit Limits the size of application flash available for programming operations. This option is available only for PSoC<sup>™</sup> 64 MCUs.
- **Programming Mode** Use this option to define programming mode for PMG1 devices. The mode options include:
  - Reset: This programming mode enables acquisition of the target device in the Test mode.
  - PowerCycle: In this mode, the programmer cycles power to acquire the device.
- **Flashloader** Use this option to select the patched QSPI CMSIS flashloader file (in FLM format). This flashloader is used for external flash programming.

Note: To be able to program custom external flash you should also provide the appropriate QSPI configuration file (qspi\_config.cfg), generated by the ModusToolbox™ QSPI Configurator tool. This file should be located in the same directory as the patched flashloader file.

- **Debug Certificate** Use this option to specify the location of the debug certificate binary file. The debug certificate is used for programming AIROC<sup>™</sup> CYW20829 targets in Secure lifecycle mode.
- **ECC Config** Use this option to enable or disable the ECC error reporting. This option is only applicable for read flash operations of some MCUs.



# 4.2.4.2 Probe Settings

The Probe settings allow you to configure the programming and target device before you connect to it. These settings are available when ModusToolbox™ Programmer is not connected to the device.

- **Interface** To select the hardware (debug) interface for communication with the target device. The possible values include: SWD and JTAG if supported by the device.
- **JTAG Chain** To select the interested target device in the JTAG chain. This option is only available for probes supporting JTAG interface. See <u>Program PSoC<sup>™</sup> 6 MCU in JTAG Chain</u> for details.
- **Voltage (V)** –To select the power supply voltage of the target device in Volts. This option is available only if the selected probe has the power control capability.
- **Clock (KHz)** To select the frequency of the hardware interface in KHz. This option is available only if the selected probe supports configurable frequencies.
- **Reset Type** Specifies the type of the Reset Chip operation. The possible values include: Soft and XRES:
  - Soft is a software reset type that sends the system reset request to the ARM core.
  - XRES is a hardware reset type that toggles the XRES hardware line.
- Sflash Restrictions Specifies the Sflash programming behavior. This option is available only for PSoC<sup>™</sup> 61/62/63, XMC7100/7200, FX3G2, CYT4Bx and CYT2Bx MCUs. The possible values include:
  - Erase/Program of Sflash is prohibited.
  - Erase and Program of USER/TOC/KEY is allowed.
  - Erase of USER/TOC/KEY and Program of USER/TOC/KEY/NAR is allowed.
  - Erase and Program of entire Sflash is allowed.



# 5 **Programming Operations**

This chapter covers the various programming operations you can perform using the ModusToolbox<sup>™</sup> Programmer tool.

## 5.1 Erase Device

- 1. Connect to the device (see <u>Connect Device</u>).
- 2. Click the **Erase** button.

ModusToolbox<sup>™</sup> Programmer erases the device and displays various messages in the **Log**. Then, a message in the Status Bar indicates that the device was erased successfully or that an error occurred.

🔲 mtb-programmer			- c	x í
<u>File View Options H</u>	lp			
Open Probe/Kit: CY8CKIT	-062-WIFI-BT-1616176C0322; Y Platform: PSoC 61/6; Y Over Discon	nect Erase	Program	Read Verify
Program Settings				~
File Offset Reset Chip > Verify Regions External Memory Program Security Data	C:/hex/CY8CKIT-062-BLE/BlinkyLED_mainapp_final.elf 0x0			
Probe Settings				
Interface	SWD			
Voltage (V)	3.3			~
Reset Type	Soft			~
Sflash Restrictions	Erase/Program USER/TOC/KEY allowed			~
Log				
Warn : Some SFlash r Info : erased sector Info : ** Erasing ba Info : [100%] [##### Info : erased sector Info : ** Erasing ba Info : [100%] [##### Info : erased sector Info : cyp status: 0 Info : cyp status: 0 Info : ** Erased OK Info : cyp_get_mpn Info : ** Detected d PSoC6ABLE2	<pre>bws were skipped during erase, see 'sflash_restrictions s 0 through 63 on flash bank 2 in 0.278954s hk 1 ** ##################################</pre>	' command FamilyID:	100 DIE:	~
Device erased successfully	Power	ed: 3256 mV	CY8C6247	7BZI-D54 .:



### 5.2 **Program Device**

- 1. Connect the device to the host computer and select it in the **Probe/Kit** drop-down.
- 2. Select the programming file as described in <u>Load Programming File</u> section.
- 3. Connect to the device (see <u>Connect Device</u>).

#### 4. Click the **Program** button.

ModusToolbox<sup>™</sup> Programmer programs the device and displays various messages in the **Log**. Then, a message in the Status Bar indicates that device was programmed successfully or that an error occurred.

mtb-programmer			- 0	×
File View Options H	lelp		-	
Open Probe/Kit: CY8CKI	T-062-WiFI-BT-1616176C0322: - Platform: PSoC 61/6: - Ower	Disconnect Era	se Program Read	<b>Nerify</b>
Settings				×
Program Settings				
File Offset Reset Chip > Verify Regions External Memory Program Security Dat	C:/hex/CY8CKIT-062-BLE/BlinkyLED_mainapp_final.elf 0x0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1			
Probe Settings				
Interface	SWD			
Voltage (V)	3.3			
Reset Type	Soft			~
Sflash Restrictions	Erase/Program USER/TOC/KEY allowed			*
Log				
<pre>Info : Padding image Info : [100%] [##### Info : [100%] [##### Info : Padding image Info : [100%] [##### Info : [100%] [##### Info : wrote 17920 I (23.542 KiB/s) Info : ** Programmin Info : cyp status: 0 Info : cyp_get_mpn Info : ** Detected of PSoC6ABLE2</pre>	<pre>&gt; section 3 at 0x100019a0 with 96 bytes (bank write ####################################</pre>	end alignmen e end alignmen inapp_final.e : 22 FamilyID	t) nt) 1f in 0.743345s : 100 DIE:	~
Device programmed success	sfully	Powered: 3255 m	V CY8C6247BZI-C	54



## 5.3 Program Device and Reset Chip

- 1. Connect the device to the host computer and select it in the **Probe/Kit** drop-down.
- 2. Select the programming file as described in the <u>Load Programming File</u> section.
- 3. Connect to the device (see <u>Connect Device</u>).
- 4. Select the **Reset Chip** check box under **Program Settings**.
- 5. Click the **Program** button.

ModusToolbox<sup>™</sup> Programmer programs the device and displays various messages in the **Log**. Then, a message in the Status Bar indicates that the device was programmed successfully or that an error occurred.

mtb-programmer		$\times$
<u>File View Options H</u>	lelp	
Open Probe/Kit: CY8CKI	T-062-WiFi-BT-1616176C0322: v Platform: PSoC 61/6: v O Power Disconnect Program Read	<b>Verify</b>
Settings		×
Program Settings File Offset Reset Chip	C:/hex/CY8CKIT-062-BLE/BlinkyLED_mainapp_final.elf	
External Memory Program Security Dat	ta	
Probe Settings		
Interface	SWD	
Voltage (V)	3.3	Ψ.
Reset Type	Soft	~
Sflash Restrictions	Erase/Program USER/TOC/KEY allowed	~
Loa		
Info : [100%] [##### Info : Padding image Info : [100%] [##### Info : [100%] [##### Info : wrote 17920 H (23.889 KiB/s) Info : ** Programmin Info : cyp status: ( Info : cyp status: ( Info : cyp get_mpn Info : ** Detected of PSoC6ABLE2 Info : reset run Info : SWD DPIDR 0xd	H####################################	~
Device programmed success	fully Powered: 3255 mV CY8C62478ZI-C	54

The target device is reset and running.



## 5.4 Program Binary File with Offset

- 1. Connect the device to the host computer and select it in the **Probe/Kit** drop-down.
- 2. Select the binary programming file as described in the <u>Load Programming File</u> section.
- 3. Connect to the device (see <u>Connect Device</u>).
- 4. Enter the desired address in the **Offset** field under **Program Settings**.
- 5. Click the **Program** button.

ModusToolbox<sup>™</sup> Programmer programs the device and displays various messages in the **Log**. Then, a message in the Status Bar indicates that the device was programmed successfully or that an error occurred.

🔲 mtb-programmer		- 0	$\times$
File View Options H	<u>H</u> elp		
Open Probe/Kit: CY8CK	IT-062-WIFI-BT-1616176C0322;  Platform: PSoC 61/6;  Power Disconnect Erase	Program F	Read Verify
Settings			×
Program Settings			
File	C:/bex/sample.bin		
Offset	0x10000000		
<ul> <li>Verify Regions</li> <li>External Memory</li> <li>Program Security Da</li> </ul>	uta		
Probe Settings			
Interface	SWD		
Voltage (V)	3.3		~
Reset Type	Soft		~
Sflash Restrictions	Erase/Program USER/TOC/KEY allowed		Ψ.
og Info : psoco.cpu.cm Info : xPSR: 0x6100 Info : ** Programmi Info : auto erase e Info : [100%] [####	4 naited due to debug-request, current mode: inread 0000 pc: 0x1600400c msp: 00000000 ng Started ** nabled ####################################		^
<pre>Info : [100%] [#### Info : wrote 131072 Info : ** Programmi Info : cyp status: Info : cyp_get_mpn Info : ** Detected PSoC6ABLE2 Info : reset run Info : SWD DPIDR 0x</pre>	<pre>####################################</pre>	LOO DIE:	v
Device programmed succes	sfully Powered: 3255 mV	CY8C6247	BZI-D54



## 5.5 Program External Memory

- 1. Attach and select a device that supports external memory (for example, CY8CKIT-062-WiFi-BT with QSPI support).
- 2. Select the External Memory option under Program Settings.

mtb-programmer					_		×
<u>File View Options H</u> e	p						
Probe/Kit: CY8CKIT-	062-WiFi-BT-1616176C0322;  Platform: PSoC 61/6	0 Power	Connect	D Erase	Program	Read	Verify
Settings							×
Program Settings File Reset Chip Verify Regions External Memory Program Security Data	C:/hex/psoc6/CY8CKIT-062-WIFI-BT/mtb-example-psoc6-h	nello-worl	d.hex				
Probe Settings Interface Voltage (V) Reset Type	SWD 3.3 Soft						•
Sflash Restrictions	Erase/Program USER/TOC/KEY allowed						-

- 3. Select the programming file as described in the <u>Load Programming File</u> section. The programming file should contain external memory region(s) and correct QSPI configuration data.
- 4. Select Erase/Program USER/TOC/KEY allowed option under Probe Settings > Sflash Restrictions.
- 5. Connect to the device (see <u>Connect Device</u>).
- 6. Click the **Program** button.



ModusToolbox<sup>™</sup> Programmer programs the device and displays various messages in the **Log**. Then, a message in the Status Bar indicates that the device was programmed successfully or that an error occurred.

mtb-programmer				-		×
Probe/Kit: CY8CKI	Pow Platform: PSoC 61/6: Pow Pow	Ver Disconnect	<b>D</b> Erase	Program	ead	<b>Nerify</b>
Settings						×
Program Settings File Reset Chip > Verify Regions External Memory Program Security Dat	C:/hex/psoc6/CY8CKIT-062-WIFI-BT/mtb-example-psoc6-hello-	world.hex				
Probe Settings						
Interface Voltage (V) Reset Type Sflash Restrictions	SWD 3.3 Soft Erase/Program USER/TOC/KEY allowed					*
Log Info : [100%] [##### Info : [100%] [##### Info : [100%] [##### Info : [100%] [#####	<pre>(####################################</pre>					^
<pre>Info : [100%] [##### Info : wrote 1682329 world.hex in 179.8319 Info : ** Programmin Info : cyp status: ( Info : cyp_get_mpn Info : ** Detected of PSoC6ABLE2 Info : reset run Info : SWD DPIDR 0x0</pre>	<pre>####################################</pre>	-BT/mtb-exam ion: 22 Fami	ple-pso lyID: 1	Doc6-hell	.0 -	~
Device programmed success	fully	Powered: 3	252 mV	CY8C6	247BZJ-D	54



# 5.6 Program PSoC<sup>™</sup> 6 MCU in JTAG Chain

1. Connect the host computer to a MiniProg4 or J-Link probe attached to several MCU targets in the JTAG chain.

The following hardware configuration is used in this example:



The sample JTAG chain configuration contains six serially connected PSoC<sup>™</sup> 6 MCU targets.

- 2. Select the MiniProg4 probe in the **Probe/Kit** drop-down and ModusToolbox<sup>™</sup> Programmer will display information under **Probe Settings**. Ensure the JTAG chain is powered.
- 3. Select the JTAG interface in the Interface drop-down.

mtb-programmer	
<u>File View Options H</u> elp	
Probe/Kit: MP4BULK-091 Open	ID 10C800287400   Platform: PSoC 61/62/63   Power Connect  Power Vorumet  Power Vorumet  Power Vorumet  Program Read Verify
Settings	
Program Settings	
File	C:/PROGTOOLS/garbage_hex_generator/cyopenocd_regression-icw-4.2-elfconverter/bin/file/20819_20820/20819A1_flash_empty.hex
Reset Chip	
Verify Regions	
External Memory	
Program Security Data	
Probe Settings	
Interface	JTAG
V JTAG Chain	
[0] PSoC 61/62/63	0
[1] PSoC 61/62/63	0
[2] PSoC 61/62/63	0
[3] PSoC 61/62/63	0
[4] PSoC 61/62/63	0
[5] PSoC 61/62/63	۲
Voltage (V)	2.5
Reset Type	Soft
Sflash Restrictions	Erase/Program USER/TOC/KEY allowed



 ModusToolbox<sup>™</sup> Programmer queries the JTAG chain and displays detected devices under the JTAG Chain option in Probe Settings. The list of devices in the chain contains target names for supported devices and ID codes for those which are not supported.

mtb-programmer	
<u>File View Options H</u> elp	
Open Probe/Kit: MP4BULK-091	ID 10C800287400   Platform: PSoC 61/62/63   Power Connect  Frase Program Read Verify
Settings	
Program Settings	
File	$C:/PROGTOOLS/garbage\_hex\_generator/cyopenocd\_regression-icw-4.2-elfconverter/bin/file/20819\_20820/20819A1\_flash\_empty.hex$
Reset Chip	$\square$
Verify Regions	
External Memory	
Program Security Data	
Probe Settings	
Interface	JTAG
✓ JTAG Chain	•
[0] PSoC 61/62/63	0
[1] PSoC 61/62/63	0
[2] PSoC 61/62/63	0
[3] PSoC 61/62/63	0
[4] PSUC 61/62/63	
[5] PSoC 61/62/63	
Voltage (V)	2.5
Reset Type	Soft
Sflash Restrictions	Erase/Program USER/TOC/KEY allowed

- 5. Select the desired target device in the list by clicking the radio button next to the target name.
- 6. Select the programming file as described in the <u>Load Programming File</u> section.
- 7. Click **Connect**. ModusToolbox<sup>™</sup> Programmer communicates with the device and displays various messages in the **Log**. Then, a message in the Status Bar indicates that it is connected.





8. Click the **Program** button.

ModusToolbox<sup>™</sup> Programmer programs the device and displays various messages in the **Log**. Then, a message in the Status Bar indicates that the device was programmed successfully or that an error occurred.

🔲 mtb-programmer			- 0	×
<u>File View Options H</u> elp				
Open Probe/Kit: MP4 BULK-091	D10C800287400    Platform: PSoC 61/62/63			
Settings				×
Program Settings				
File	C:/OpenOCD_TEST_DATA/bin/file/CY8C6347BZI-BLD53/CY8C6347BZI-BLD53_main.hex			
Reset Chip				
> Verify Regions				
External Memory				
Program Security Data				
Probe Settings				_
Interface	JTAG			Ψ.
✓ JTAG Chain				
[0] PSoC 61/62/63				
[1] PSoC 61/62/63				
[2] PSoC 61/62/63				
[3] PSoC 61/62/63				
[4] PSoC 61/62/63				
[5] PSoC 61/62/63	•			
Voltage (V)	2.5			v
Reset Type	Soft			Ψ.
Sflash Restrictions	Erase/Program USER/TOC/KEY allowed			Ψ.
L				
log Info : ** Program image Info : psoc6.cpu.cm0 ha Info : sv58: 0x21000000 Info : ** psoc6.cpu.cm4 ha Info : psoc6.cpu.cm4 ha Info : sv58: 0x61000000 Info : auto erase enabl Info : [100%] [######## Info : [100%] [######## Info : wrote 10448576 by Info : cyp status: 0K Info : cyp get_mpn Info : reset run	C:/UpenOLD_IESI_DATA/bin/file/CY8C634782I-BLD53/CY8C634782I-BLD53_main.hex offse lted due to debug-request, current mode: Thread pc: 0x20000131, issuing SYSRESETREQ lted due to debug-request, current mode: Thread pc: 0x10000130 msp: 0x08024000 : Ran after reset and before halt lted due to debug-request, current mode: Thread pc: 0x16004080c msp: 00000000 tarted ** ed ############################# [ Erasing ] ####################################			~
Device programmed successfully		Powered: 2508 mV	CY8C6247BZI-D5	4



### 5.7 Verify Device

- 1. Connect the device to the host computer and select it in the **Probe/Kit** drop-down.
- 2. Select the programming file as described in the <u>Load Programming File</u> section.
- 3. Connect to the device (see <u>Connect Device</u>).
- 4. Click the **Verify** button.

ModusToolbox<sup>™</sup> Programmer performs the Verify device operation and displays various messages in the **Log**. Then, a message in the Status Bar indicates that the device was verified successfully or that an error occurred.

The View Options H	-	-		×
Open Probe/Kit: CY8CKI	T-062-WiFI-BT-1616176C0322: VIETOrm: PSoC 61/6: Disconnect Erase I	<b>Program</b>	Sead	<b>N</b> Verify
Settings				×
Program Settings				
File Reset Chip > Verify Regions External Memory Program Security Da	C:/hex/CY8CKIT-062-BLE/BlinkyLED_mainapp_final.hex			
Probe Settings Interface Voltage (V) Reset Type Sflash Restrictions	SWD 3.3 Soft Erase/Program USER/TOC/KEY allowed			*
Log Into : ** Probing D Info : flash 'psoc6 Info : ** Probing b	ank ט ** ' found at 0x10000000 ank 1 **			^
<pre>Info : flash 'psoc6 Info : ** Probing bu Info : flash 'psoc6 Info : flash 'psoc6 Info : flash 'psoc6 Info : flash 'psoc6 Info : verified 1111 Info : cyp status: Info : ** Verified Info : cyp_get_mpn Info : ** Detected of PSoC6ABLE2</pre>	' found at 0x14000000 ank 2 ** ' found at 0x16000000 ank 3 ** _efuse' found at 0x90700000 _image C:/hex/CY8CKIT-062-BLE/BlinkyLED_mainapp_final.hex offset:0 * 5136 bytes in 4.157334s (261.947 KiB/s) OK OK ** device PN: CY8C6247BZI-D54 SiliconID: E206 Revision: 22 FamilyID: 10	* 0 DIE:		~
Device verified successfully	Powered: 3253 mV	CY8C62	478Z	



# 5.8 Verify Device with External Memory

- 1. Connect the device that supports external memory (for example, CY8CKIT-062-WiFi-BT with QSPI support) to the host computer and select it in the **Probe/Kit** drop-down.
- 2. Select the programming file as described in the <u>Load Programming File</u> section. The programming file should have external memory region(s).
- 3. Select the External Memory option under Program Settings.

		_
<u>File View Options H</u>	lelp	
Open Probe/Kit: CY8CKIT	r-062-WiFi-BT-1616176C03227400 ▼ Platform: PSoC 61/62/6: ▼ 0	) /erify
Settings		×
Program Settings		
File	D:/hex/lubm/CY8C6347BZI-BLD53_smif_internal_bank.hex	
Reset Chip		
Verify Regions	_	
External Memory		
Program Security Data		
Probe Settings		
Interface	SWD	
Voltage (V)	3.3	•
Reset Type	Soft	•
Sflash Restrictions	Erase/Program Sflash prohibited	•
Reset Type Sflash Restrictions	Soft Erase/Program Sflash prohibited	•

- 4. Connect to the device (see <u>Connect Device</u>).
- 5. Click the **Verify** button.



ModusToolbox<sup>™</sup> Programmer verifies the device and displays various messages in the **Log**. Then, a message in the Status Bar indicates that the device was verified successfully or that an error occurred.

mtb-programmer					-		×
File View Options H	lelp						
Open Probe/Kit: CY8CK	T-062-WiFi-BT-1616176C0322; Y Platform: PSoC 61/6; Y	(1) Power	0 Disconnect	<b>D</b> Erase	Program	Sead	<b>S</b> Verify
Settings							×
Program Settings							
File Reset Chip > Verify Regions External Memory Program Security Da	C:/hex/psoc6/CY8CKIT-062-WIFI-BT/mtb-example-psoc6-h	ello-worl	ld.hex				
Probe Settings							
Interface Voltage (V) Reset Type	SWD 3.3 Soft						*
Log							
Info : flash 'psoc6 Info : ** Probing b Info : flash 'psoc6 Info : ** Probing b Info : flash 'psoc6 Info : ** Probing b Info : flash 'cmsis Info : ** Verifying ** Info : verified 181 Info : cyp status: Info : ** Verified Info : ** Verified	' found at 0x14000000 ank 2 ** ' found at 0x16000000 ank 3 ** _efuse' found at 0x90700000 ank 8 ** _flash' found at 0x18000000 image C:/hex/psoc6/CY8CKIT-062-WIFI-BT/mtb-e 4236 bytes in 8.199423s (216.078 KiB/s) OK **	example	e-psoc6-he.	llo-wor	old.hex	offset	.0
Info : ** Detected PSoC6ABLE2	device PN: CY8C6247BZI-D54 SiliconID: E206 Re	evisior	n: <mark>22 Fami</mark>	lyID: 1	00 DIE:		~
Device verified successfully			Powered: 3	253 mV	CY8C6	2478ZI-D	54



# 5.9 Verify Custom Flash Regions of PSoC<sup>™</sup> 6 MCU

- 1. Connect the device to the host computer and select it in the **Probe/Kit** drop-down.
- 2. Select the programming file as described in the <u>Load Programming File</u> section.
- 3. Connect to the device (see <u>Connect Device</u>).
- 4. Expand **Verify Regions** option in **Program Settings** to see the list of flash regions available for verification. By default, only supported by target device regions are displayed:
  - application
  - AUXflash
  - Sflash
  - eFuse
  - QSPI

Settings		x
Program Settings		
File	D:/hex/BlinkyLED_mainapp	_final.hex
Reset Chip		
Verify Regions		
From	То	
0x10000000	0x100fffff	
0x14000000	0x14 application	
0x16000000	0x16007fff	
0x90700000	0x907003ff	

5. Right-click on **Verify Regions**, or any region entry, to open the context menu.

Pro	ogram Settings		
	File	D:/hex/BlinkyLED_maina	pp_final
	Reset Chip		
4	Verify Regions	Add Region	-1
	From	<u>R</u> eload Regions	
	0x10000000	<u>U</u> ndo	
	0x14000000	Redo	
	0x16000000	Verify	
	0x90700000	-0.50/00311	_

6. To add a custom flash region, select **Add Region**. Select the added list entry, and enter the correct values for start and end addresses of the region.

Progr	am Settings		
F	ile	D:/hex/BlinkyLED_mainapp_final.hex	
R	eset Chip		
⊿ V	erify Regions		
	From	То	
	0x10000000	0x100fffff	
	0x14000000	0x14007fff	
	0x16000000	0x16007fff	
-	0x90700000	0x907003ff	
	0x10001000	3 0x10µ00000	



7. To remove any region in the list, right-click the desired region entry and select **Remove Region**.

Program Settings	
File	D:/hex/lubm/CY8C6347BZI-BLD53_smif_internal_bank.hex
Reset Chip	
Verify Regions	
From	То
0x10000000	0x100fffff
0x14000000	0x14007fff
0x16000000	0*15007fff
0x90700000	Add Region
External Memory	R <u>e</u> move Region
Program Security Data	Undo
Probe Settings	Redo
Interface	S Verify
Voltage (V)	3
Reset Type	s <sup>Cu</sup>
Sflash Restrictions	E Copy
	Paste
Log	Delete
Info : flash 'psoc6'	
Info : flash 'psoco'	Select All

- 8. To revert any previous change, select **Undo**.
- 9. When finished with the list of regions, start device verification by clicking the **Verify** button on the toolbar.

mtb-progr	mmer					_		×
<u>F</u> ile <u>V</u> iew <u>(</u>	ptions Ve	ify <u>R</u> egions <u>H</u> elp						
Open Probe/	Kit: CY8CKIT	062-WiFI-BT-1616176C0322; * Platform: PSoC 61/6; *	Power	<b>O</b> isconnect	Erase	Program	Sead	<b>S</b> Verify
Settings								×
Program Setting	s							
File		C:/hex/lubm/CY8C6347BZI-BLD53_smif_internal_bank.he	x					
Reset Chip		$\checkmark$						
<ul> <li>Verify Reg</li> </ul>	ons							
From 0x100	00000	To 0x100fffff						

You can also select Verify on the context menu.

Pro	gram Settings				
	File	D:/hex/BlinkyLED_	mainap	op_final.hex	
	Reset Chip			Add Region	
4	Verify Regions			Add Region	
	From	То		Keload Regions	
	0x10000000	0x100000ff		<u>U</u> ndo	
	0x14000000	0x14007fff		<u>R</u> edo	
	0x10010000	0x10020000		<u>V</u> erify	

ModusToolbox<sup>™</sup> Programmer verifies only for the regions specified in the **Verify Regions** list. Then, a message in the Status Bar indicates that the device was verified successfully or that an error occurred.

10. To reset the **Verify Regions** list to its default state select **Reload Regions** from the context menu. This action will remove all custom regions and load default regions corresponding to the flash map of the PSoC<sup>™</sup> 6 MCU.

Program Settings			
File	D:/hex/lubm/CY8C6347E	ZI-BLD53_smif_internal_bank.hex	
Reset Chip			
▲ Verify Regions	Add Region		
From	<u>R</u> eload Regions		
0x1000000	<u>U</u> ndo		
0x14000000	Redo		
0x16000000	Verify		
0x90700000	veniy		
External Memory			



#### 5.10 Read Device

- 1. Connect the device to the host computer and select it in the **Probe/Kit** drop-down.
- 2. Select the programming file as described in the <u>Load Programming File</u> section.
- 3. Connect to the device (see <u>Connect Device</u>).
- 4. Click the **Read** button.



5. On the **Read Device to File** dialog, navigate to the location of the HEX or SREC file to be saved, enter the file name, select the file type in the **Save as type** drop-down, and click **Save**.



Note:

Under Ubuntu Linux, specify the full file name with an extension (e.g. kp3-dev.srec); otherwise, the file will be saved in HEX format.



ModusToolbox<sup>™</sup> Programmer performs the Read device operation and displays various messages in the **Log**. Then, a message in the Status Bar indicates that the device was read successfully or that an error occurred.

File View Options	X
Open Probe/Kit: CY8C	IT-062-WIFI-BT-1616176C0322;  Platform: PSoC 61/6;  Power Disconnect Program Read Ver
Settings	
Program Settings File Reset Chip > Verify Regions External Memory Program Security D:	C:/hex/lubm/CY8C6347BZI-BLD53_smif_internal_bank.hex
Probe Settings Interface Voltage (V) Reset Type Sflash Restrictions	SWD 3.3 Soft Erase/Program USER/TOC/KEY allowed
pq	
pank 1 at offset 0xi Info : ** Reading H Info : wrote 32768 bank 2 at offset 0xi Info : ** Reading H Info : ** Reading H bank 3 at offset 0xi Info : TARGET: pso Info : set SMIF_BAH Info : region 1 ad	<pre>W0000000 in 0.266674s (119.997 KiB/s) wank 2, filename C:/Users/Svynchuk/AppData/Local/Temp/dump_2_369098752.bin ** bytes to file C:/Users/Svynchuk/AppData/Local/Temp/dump_2_369098752.bin from flash W0000000 in 0.267883s (119.455 KiB/s) wank 3, filename C:/Users/Svynchuk/AppData/Local/Temp/dump_3_2423259136.bin ** wytes to file C:/Users/Svynchuk/AppData/Local/Temp/dump_3_2423259136.bin from flash W0000000 in 0.272995s (3.663 KiB/s) %6.cpu WKS {1 {addr 0x18000000 size 0x01000000 psize 0x200 esize 0x40000}} </pre>



## 5.11 Program eFuse Region of PSoC<sup>™</sup> 6/TRAVEO<sup>™</sup> T2G/XMC7xxx MCU

- 1. Connect the device to the host computer and select it in the Probe/Kit drop-down.
- 2. Select the programming file as described in the <u>Load Programming File</u> section. The programming file should contain valid eFuse data region (at address 0x90700000).
- 3. Select the **Program Security Data** check box under Program Settings.



- 4. Connect to the device (see <u>Connect Device</u>).
- 5. Click the **Program** button.



ModusToolbox<sup>™</sup> Programmer programs the device and displays various messages in the **Log**. Then, a message in the Status Bar indicates that the device was programmed successfully or that an error occurred.

If some eFuse bits have been already programmed before, a warning message "The efuse bit at address xx has been already blown" appears in **Log**.



# 5.12 Program PSoC<sup>™</sup> 4 MCU With Protected Flash

Flash protection allows you to protect any PSoC<sup>™</sup> 4 flash rows from being written. Applying protection to the user data with ModusToolbox<sup>™</sup> Programmer is nothing more than programming a data file containing appropriate flash protection region (at the address 0x90400000).

Programming data into protected flash region will fail with "Programming Failed" error.

mtb-programmer						-		×
Probe/Kit: CY8	<u>H</u> eip KIT-041-41XX-0D1D078303105400 7 Pk	atform: PSoC 4 😁	O Power	Disconnect	<b>D</b> Erase	Program	Read	<b>Verify</b>
Settings								×
Program Settings File Reset Chip > Verify Regions	C:/hex/psoc4/41005/BreathingLED_sr	mall3.hex						
Probe Settings								
Interface Reset Type	SWD							*
Info : Flash write Info : Padding im Warn : Only mass of Info : [100%] [## Harn : Only mass of Error: [ 64%] [## failure - "Row Pro Error: error write Error: cyp status Info : Program de Error: C:/Program Error: ** Programm Error: in procedu	discontinued at 0x000000c0, n ge section 0 at 0x000000c0 wit rase available, erase skipped! ####################################	ext section at ( th 64 bytes (bank (psoc4 mass_err [ Programming ] (psoc4 mass_err [ Programming ] s a protected roo 0000 at offset 00 rogrammer 4.0/./s	0x00006 k write ase <ba ] ase <ba ]Error: w" x00006 scripts</ba </ba 	5f00 e end align ank_id>) ank_id>) : Flash ali 500 5/cyp_base	nment) gorithm _defau]	n reporta	ed 8:	l
Error: at file "C cyp_base_default.t Info : cyp_get_mp	/Program Files (x86)/Cypress/C 1", line 38	ypress Programme	er 4.0/	<pre>/./scripts,</pre>	/			~
Error: Program device fa	ed			Powered: 3	367 mV	Con	nected	

Use the **Erase** button to un-protect user flash rows from writing.



# 5.13 Program Chip-Protected PSoC<sup>™</sup> 4 MCU

The chip-level protection mechanism restricts access of the programmer application to silicon resources. In this mode, access to flash, SRAM, and most of the registers in the PSoC<sup>™</sup> 4 are disabled. Chip protection can be activated by programming a HEX file with a special protection region at address 0x90600000.

If you try to connect ModusToolbox<sup>™</sup> Programmer to a chip-protected PSoC<sup>™</sup> 4/PMG1/WLC1 device, a warning message indicates that device is in protected mode. The only available operation is **Erase** device in this case.

mtb-programmer					<u></u>		×
<u>File View Options H</u> elp							
Probe/Kit: CY8CKIT-041-41XX-0D1D07B303105400 Y Platform: PSoC 4 O Open Disconnect Program Read Ver						<b>Verify</b>	
Settings							×
Program Settings File Reset Chip Verify Regions	C:/hex/psoc4/4100S/CE216873 ADC with Breathing L	ED_lock.hex					
Probe Settings							
Interface Reset Type	SWD Soft						v
Error: Failed to n Info : flash 'psoc Info : SWD DPIDR @ Error: Failed to n Info : flash 'psoc Info : SWD DPIDR @ Error: Failed to n Info : flash 'psoc Info : SWD DPIDR @ Error: Failed to n Info : flash 'psoc Info : #0 : psoc4. Info : #1 : psoc4. Info : #3 : psoc4. Info : cyp status: Marn : * PSoC 4 de	ead memory at 0x40110000 4' found at 0x00000000 x0bc11477 ead memory at 0x40110000 4' found at 0x0ffff200 x0bc11477 ead memory at 0x40110000 4_flash_prot' found at 0x90400000 x0bc11477 ead memory at 0x40110000 4_flash_prot' found at 0x90600000 mflash (psoc4) at 0x00000000, size 0x0000 flashp (psoc4_flash_prot) at 0x90400000, s OK **********************************	0000, bus 0000, bus size 0x000 ize 0x000	width 0, ch width 0, ch 000000, bus 00001, busw **	ripwidth Lipwidth Width 0 Lidth 1,	0 0, chipwi chipwi	idth 0 dth 1	,
Warn : ***********************************	se Device to clear protection. All data w	111 De 10 *********	st: **				~
Connected to the target de	avice		Powered: 3	3371 mV	Cor	nected	

Use the **Erase** button to clear chip protection and move target to the open state.



### 5.14 Program Secure AIROC<sup>™</sup> CYW20829 MCU

You can program the flash of an AIROC<sup>™</sup> CYW20829 device in Secure lifecycle mode only by providing a valid debug certificate file.

- 1. Connect the device to the host computer and select it in the Probe/Kit drop-down.
- 2. Select the programming file as described in the <u>Load Programming File</u> section.
- 3. Click on the **Debug Certificate** option under **Program Settings** and select the certificate file in the dialog.

#### The path will display under Settings.

	mtb-programmer –	• 😣
<u>File View Options</u>	Help	
Open Probe/Kit: N	1P4 BULK-1921055303147400 V Platform: CYW20829 V Onnect Erase Program Read	Verify
Settings		D
Program Settings		*
File Reset Chip Verify Regions	/home/cyptest/osvn/20829/CYW20829A0LKML_secure_no_cm33_app.hex	
Flashloader	Default	-
Debug Certificate	/home/cyptest/osvn/20829/debug_cert_oem.bin	-
Probe Settings		
Interface	SWD	*
Clock (KHz)	2000	*
Voltage (V)	33	*

- 4. Connect to the device (see <u>Connect Device</u>).
- 5. Click the **Program** button.

# 5.15 Program QSPI memory with patched flashloader

This feature is supported by AIROC<sup>™</sup> CYW20829 devices, as well as XMC7100/7200 and CYT4Bx MCUs. It allows you to specify the patched flashloader file in FLM format along with the appropriate QSPI configuration. Patched flashloaders contain data about how your external memory is configured.

- 1. Connect the device to the host computer and select it in the Probe/Kit drop-down.
- 2. Select the programming file as described in the Load Programming File section.
- 3. Select the External Memory option under Program Settings (if supported).
- 4. Click on the Flashloader option under **Program Settings** and select the patched flashloader (FLM) file in the dialog.

#### The path will display under Settings.

	mtb-porgrammer					-	0 😣
<u>File View Options</u>	Help						
Open Probe/Kit: M	1P4 BULK-1921055303147400 * Platform: CYW20829 *	Power	Connect	Erase	<b>C</b> Program	Read	<b>O</b> Verify
Settings							6
Program Settings							-
File	/home/cyptest/osvn/20829/uppercase/CYW20829A0LKML	_secure_r	no_cm33_ap	p.HEX			
Reset Chip Verify Regions							
Flashloader	/home/cyptest/osvn/20829/FLM/CYW208xx_SMIF.flm						•
Debug Certificate	/home/cyptest/osvn/20829/debug_cert_oem.bin						
Probe Settings							
Interface	SWD						Ŧ
Clock (KHz)	2000						Ŧ
10 M 10 M 10 M							

5. Connect to the device (see <u>Connect Device</u>).



#### 6. Click the **Program** button.

Note:

To be able to program custom QSPI memory, you should also provide the appropriate QSPI configuration file (qspi\_config.cfg) generated by the ModusToolbox<sup>™</sup> QSPI Configurator tool. This file should be placed in the same directory as the patched flashloader file; it is located and read by ModusToolbox<sup>™</sup> Programmer automatically. Refer to the <u>QSPI Configurator user guide</u> for more information about patching flashloaders.



#### Troubleshooting

# 6 Troubleshooting

#### 6.1 Limitations

- ModusToolbox<sup>™</sup> Programmer does not support RAM programming, you can program only the flash memory of a target device, except for devices that support only RAM such as CYW9M2BASE-43012BT and CYW955513EVK-01 kits.
- Programming devices in DAPLink mode is not supported. You have to switch your device into CMSIS-DAP BULK mode by pressing the mode selection button.

## 6.2 How to Recover AIROC<sup>™</sup> Bluetooth<sup>®</sup> Devices on Failure

If the program operation for an AIROC<sup>™</sup> Bluetooth<sup>®</sup> device fails, it is possible the memory on the board has been corrupted by a previously loaded application, or the application used a custom baud rate that the download process does not detect.

To recover from this, it may be necessary to reset the board to factory defaults, as follows:

- 1. Press and hold the **Recovery** button (SW1).
- 2. Press the **Reset** button (SW2).
- 3. Release the **Reset** button (SW2).
- 4. Release the **Recovery** button (SW1).



**Upgrading firmware** 

# 7 Upgrading firmware

The ModusToolbox<sup>™</sup> Programmer application allows you to upgrade KitProg2, KitProg3, and MiniProg4 device firmware.

# 7.1 Upgrade KitProg2 firmware

The following upgrade process is based on the CY8CKIT-062-WIFI-BT hardware.

- 1. Run the ModusToolbox<sup>™</sup> Programmer application.
- 2. Go to **Options > Programmer Options** and select the Show Pop-Up value for the **Upgrade Firmware** option.

Programmer Options - m	ntb-programmer X
Name	Value
Upgrade Firmware	Show Pop-Up $\sim$
OpenOCD Telnet Port	4445
	OK Cancel

- 3. Click **OK** to apply the changes.
- 4. Connect the device with the KitProg2 firmware to the host PC. Ensure that the KitProg2 device is in Native KP2 mode.
- 5. If **LED2** is off, press the **SW3** (Mode Select) button and hold it for about 1 second. When **LED2** is on, the device is ready for upgrading the firmware.



A warning dialog displays with the "Firmware is Out of Date" message.





#### Upgrading firmware

6. Click the **Upgrade Firmware** button to start the upgrade process.

After the upgrade process completes, the message "Firmware of 'KitProg2-xx' upgraded successfully" displays in the **Log** view. The KitProg2-xx device disappears from the **Probe/Kit** drop-down. The **Probe/Kit** drop-down is populated with the names of the supported KitProg3 Kits.

mtb-programmer				
File	View Opti	ons Help		
	Probe/Kit:	None	$\sim$	Platform:
Open		None		
Cotting		CY8CKIT-062-BLE-061B12C800287400		
setting	5	CY8CKIT-062-WiFi-BT-061B12C800287400		
Program Settings CYW943012P6EVB-01-061B12C800287400				
Fil	e	C:/hex/lubm/CY8C6347BZI-BLD53_	sm	nif_internal

# 7.2 Upgrade KitProg3 on kit or MiniProg4 firmware

Follow this process to upgrade KitProg3 on a kit or MiniProg4 firmware:

- 1. Run the ModusToolbox<sup>™</sup> Programmer application.
- 2. As needed, go to **Options > Programmer Options** and select the Show Pop-Up value for the **Upgrade Firmware** option.
- 3. Connect the KitProg3/MiniProg4 device to the host PC. A warning dialog with the "Firmware is Out of Date" message displays.



4. Click the **Upgrade Firmware** button to start the upgrade process.

After the upgrade process completes, the message "Firmware of 'KitProg3-xx' upgraded successfully" or "Firmware of 'MiniProg4 xx' upgraded successfully" displays in the **Log** view.

# **Revision history**

# **Revision history**

Version	Date	Description
**	2023-07-18	New document.
		Updates for Production milestone:
* ^	2019 10 20	Various screen captures
A	2018-10-30	Description of the Platforms pull-down menu
		Description of the Clock option in Probe Settings
		Updated to version 2.1.
*B	2019-07-19	Added Verify Regions menu.
Ь	2019-07-19	Added JTAG Chain instructions.
		Added Verify Custom Flash Regions section.
		List of changes:
		User Guide clean-up in whole document
*C	2019-10-11	Updated section "Features"
•		Updated section "Limitations"
		Updated section "Settings"
		<ul> <li>Added section "How to Recover AIROC<sup>™</sup> Bluetooth<sup>®</sup> Devices on Failure"</li> </ul>
		List of changes:
	2020-05-04	Updated to version 3.0
*D		Updated screenshots across the document
		Made modifications with new features of CYP 3.0
		<ul> <li>Added section "Program eFuse Region of PSoC™ 6 MCU"</li> </ul>
		Corrected mistakes.
		List of changes:
		Updated to version 4.0.
+-		Updated all sections with new screenshots
^E	2021-03-18	<ul> <li>Updated sections "Getting Started", "Settings", "Program PSoC™ 6 MCU in JTAG Chain"</li> </ul>
		<ul> <li>Added section "Program Chip Protected PSoC<sup>™</sup> 4 MCU"</li> </ul>
		Corrected mistakes
		List of changes:
*F	2022-03-15	Updated to version 4.0.1
·	2022 03 13	Updated section "Introduction"
		Updated section "Installing CYP"
		List of changes:
*G	2022-10-28	Updated to version 4.1.0
•		Minor updates across the document
		List of changes:
	2023-02-14	Updated to version 4.2.0
<b></b>		Updated section 4.2.4.1
*H		Added sections 5.14 and 5.15
		Minor updates across the document





# **Revision history**

Version	Date	Description
*	2023-09-12	<ul> <li>List of changes:</li> <li>Updated to version 5.0.0</li> <li>Changed title of the tool and user guide to ModusToolbox<sup>™</sup> Programmer.</li> <li>Tool is now part of Programming tools package; installation instructions now included in the release notes.</li> </ul>

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Edition 2023-09-13

**Published by** 

Infineon Technologies AG

81726 Munich, Germany

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Document reference 002-25230 Rev.\*I

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