

# Keil µVision for ModusToolbox™ user guide

ModusToolbox<sup>™</sup> tools package version 3.1.0

### About this document

#### Scope and purpose

ModusToolbox<sup>™</sup> software is a set of tools and libraries that support device configuration and application development. These tools enable you to integrate our devices into your existing development methodology. This document provides information and instructions for using Keil µVision with ModusToolbox<sup>™</sup> software.

#### **Document conventions**

Convention	Explanation			
Bold	Emphasizes heading levels, column headings, menus and sub-menus.			
Italics	Denotes file names and paths.			
Courier New	Denotes APIs, functions, interrupt handlers, events, data types, error handlers, file/folder names, directories, command line inputs, code snippets.			
File > New	Indicates that a cascading sub-menu opens when you select a menu item.			

#### **Reference documents**

Refer to the following documents for more information as needed:

- <u>ModusToolbox<sup>™</sup> tools package installation guide</u> –Provides information and instructions about installing the tools package on Windows, Linux, and macOS.
- <u>ModusToolbox<sup>™</sup> tools package user guide</u> –Provides information about all the tools included with ModusToolbox<sup>™</sup> tools package.
- <u>Dashboard user guide</u> Provides specific information about the Dashboard tool.
- <u>Project Creator user guide</u> Provides specific information about the Project Creator tool.
- <u>Device Configurator guide</u> Provides specific information about the Device Configurator.



### Table of contents

### **Table of contents**

Abou	\bout this document1				
Table	e of contents	2			
1	Download/install software				
1.1	ModusToolbox™ tools package	3			
1.2	Keil μVision (Windows only)	3			
1.3	Python	3			
1.4	J-Link	3			
2	Getting Started	4			
2.1	Create new application	4			
2.2	Export existing application	6			
2.3	Open application in Keil $\mu$ Vision	7			
3	Configure and build the application				
3.1	PSoC <sup>™</sup> 64 application configuration	9			
4	Programming/Debugging	13			
4.1	To use KitProg3/MiniProg4, CMSIS-DAP, and ULink2 debuggers	14			
4.2	To use J-Link debugger with PSoC™ MCUs				
4.3	To use J-Link debugger with XMC7000 devices				
4.4	Program external memory	22			
4.5	Erase external memory	23			
5	Multi-core debugging	24			
5.1	Supported debugger probes	24			
5.2	Opening µVision multi-core projects	24			
5.3	Debugger configuration	24			
5.4	Launching multi-core debug session				
6	Patched flashloaders for AIROC™ CYW208xx devices	30			
Revis	sion history	31			



Download/install software

### **1** Download/install software

### **1.1** ModusToolbox<sup>™</sup> tools package

Refer to the instructions in the <u>ModusToolbox<sup>™</sup> tools package installation guide</u> for how to download and install the ModusToolbox<sup>™</sup> tools package.

### **1.2** Keil μVision (Windows only)

Keil µVision version 5.30 or later

#### 1.3 Python

Python 3.8 is installed in the tools\_3.x directory, and the make build system has been configured to use it. You don't need to do anything if you use the modus-shell/Cygwin.bat file to run command line tools.

However, if you plan to use your own version of Cygwin or some other type of bash, you will need to ensure your system is configured correctly to use Python 3.8. Use the CY PYTHON PATH as appropriate.

#### 1.4 J-Link

For J-Link debugging, download and install J-Link software:

https://www.segger.com/downloads/J-Link/J-Link Windows.exe



### 2 Getting Started

This section covers the ways to get started using IAR Embedded Workbench with ModusToolbox™ software.

- <u>Create new application</u>
- Exporting existing application
- Open application Keil µVision

#### 2.1 Create new application

Creating an application includes several steps, as follows:

### 2.1.1 Step 1: Open Project Creator tool

The ModusToolbox<sup>™</sup> Project Creator tool is used to create applications based on code examples and template applications. You can open the Project Creator tool from the Windows **Start** menu, or by launching the executable. By default, the tool is installed in the following directory:

<user\_home>/ModusToolbox/tools\_<version>/project-creator

The tool is provided in GUI form and as a command line interface. For more details, refer to the <u>Project Creator</u> <u>user guide</u>.

Note: You can also launch the Project Creator tool from the ModusToolbox<sup>™</sup> Dashboard. Refer to the <u>Dashboard user guide</u> for details.

### 2.1.2 Step 2: Choose Board Support Package (BSP)

When the Project Creator tool opens, expand one of the BSP categories under **Kit Name** and select an appropriate kit; see the description for it on the right. The following image is an example; the precise list of boards available in this version will reflect the platforms available for development. You can also create a new BSP or browse for one on disk.

Choose Board Support Package (BSP) -	Project Creator 2.10			- 🗆 X
<u>S</u> ettings <u>H</u> elp				
Source Template				
Enter filter text	<u>I</u>	Create from MPN Browse for BSP	⊨₽	CY8CKIT-06252-43012
Kit Name           > PSoC™ 4 BSPs           Y PSoC™ 6 BSPs           CY8CEVAL-06252           CY8CEVAL-06252-LAI-43439M2           CY8CEVAL-06252-LAI-4373M2           CY8CEVAL-06252-MUR-43439M2           CY8CEVAL-06252-MUR-43439M2           CY8CEVAL-06252-MUR-43439M2           CY8CEVAL-06252-MUR-4373M2           CY8CEVAL-06252-MUR-4373M2           CY8CEVAL-06252-MUR-4373M2           CY8CKIT-06254-MUR-4373M2           CY8CKIT-06254-43012           CY8CKIT-06254-WIF-BT           CY8CKIT-0648052-4343W           CY8CKIT-0648052-4343W           CY8CKIT-0648052-4343W	MCU/SOC/SIP CY8C624ABZI-S2D44 CY8C624ABZI-S2D44 CY8C624ABZI-S2D44 CY8C624ABZI-S2D44 CY8C624ABZI-S2D44 CY8C624ABZI-S2D44 CY8C624ABZI-S2D44 CY8C624ABZI-S2D44 CY8C6244ABZI-S2D44 CY8C644ABZI-S2D44 CY8C644ABZI-S2D44 CY8C624ABZI-S2D44	Connectivity <none> Sterling-LWB+ (CYW43439KUBG) Sterling-LWB5+ (CYW4373EUBGT) LBEE5K11YN (CYW43439KUBG) LBEE5PK2BC (CYW4373IUBGT) <none> LBEE59K1DX (CYW43012C0WKWBG) <none> LBEE5KL1DX (CYW4343WKUBG) LBEE5KL1DX (CYW4343WKUBG)</none></none></none>	~	The CY8CKIT-062S2-43012 PSoC <sup>™</sup> 6S2 Wi-Fi BT Pioneer Kit is a low-cost hardware platform that enables design and debug of PSoC <sup>™</sup> 6 MCUs. It comes with a Murata 1LV Module (CYW43012 Wi-Fi + Bluetooth Combo Chip), industry- leading CAPSENSE <sup>™</sup> for touch buttons and slider, on-board debugger/programmer with KitProg3, microSD card interface, 512-Mb Quad- SPI NOR flash, PDM-PCM microphone interface. Kit Features: • Support of up to 2MB Flash and 1MB SRAM • Dedicated SDHC to interface with WICED wireless devices. • Delivers dual-cores, with a 150-MHz Arm ® Cortex ®-M4 as the primary application processor and a 100-MHz
BSP: CY8CKIT-06252-43012				^
Press "Next" to select application.				~
				<u>N</u> ext > <u>C</u> lose

For this example, select the CY8CKIT-062S2-43012 kit.



### 2.1.3 Step 3: Select application

Click **Next >** to open the Select Application page.

Select Application - Pr	oject Creator 2.10 -	۵		×
<u>S</u> ettings <u>H</u> elp				
Application(s) Root Path:	C:/Users/Test/mtw3.1/uvision		Brows	e
Target IDE:	<none></none>	~		
Enter filter text	🖉 Browse for Application 🔻 🎇 🗄 🗈 🖪			
Template Application > Bluetooth® > Community Code Ex. > Connectivity > Getting Started > Graphics > Machine Learning > Manufacturing > Peripherals > Sensing > Wi-Fi	New Application Name New BSP Name			
Select one or more temp	ate applications to proceed with the new project creation process.			
	< <u>B</u> ack <u>C</u> reate		<u>C</u> los	e ]

This page displays example applications, which demonstrate different features available on the selected BSP. In this case, the CY8CKIT-062S2-43012 provides the PSoC<sup>™</sup> 62 MCU and the AIROC<sup>™</sup> CYW43012 Wi-Fi & Bluetooth<sup>®</sup> combo chip. You can create examples for PSoC<sup>™</sup> 6 MCU resources such as CAPSENSE<sup>™</sup> and QSPI, as well as numerous examples for other capabilities.

Click **Browse...** next to **Application(s) Root Path** to create or specify a folder where the application will be created.

Pull down the Target IDE menu, and select ARM MDK (uVision).

Application(s) Root Path:	C:/Users/Test/mtw3.1/uvision	Browse
Target IDE:	<none> ~</none>	
Enter filter text	<none> Eclipse IDE for ModusToolbox™</none>	
	Microsoft Visual Studio Code IAR Embedded Workbench	
Bluetooth®	ARM MDK (uVision)	

Under the **Template Application** column, expand **Getting Started** and select **Hello World** from the list. This example exercise uses the PSoC<sup>™</sup> 6 MCU to blink an LED.

Template Application	New Application Name	New BSP Name
✓ Getting Started		
Dual-CPU Empty PSoC6 App		
Empty App		
Hello World	Hello_World	APP_CY8CKIT-062S2-43012
Security App		
Switching Power Modes		

The actual application names available might vary.

Type a name for your application and/or BSP, or leave the default names. Do not use spaces. Also, do not use common illegal characters, such as:

\* . " ` /  $\setminus$  [ ] : ; | = ,



### 2.1.4 Step 4: Create application

Click **Create** to start creating the application. The tool displays various messages.

Select Application - Pr	🖀 Select Application - Project Creator 2.10 — 🗆 🗙					×				
<u>S</u> ettings <u>H</u> elp										
Application(s) Root Path:	C:/Users/Test/m	ntw3.1/uvision							Brow	se
Target IDE:	<none></none>								1	
Enter filter text			Browse for Application 💎	94	- -	Ŧ				
Template Application		New Application Name	New BSP Name			^				
<ul> <li>Connectivity</li> <li>Getting Started</li> <li>Dual-CPU Employed</li> <li>Empty App</li> </ul>	pty PSoC6 App									
Hello World		Hello_World	APP_CY8CKIT-062S2-43012							
Security App Switching Pov Graphics	ver Modes									
> Machine Learning										
> Manufacturing > Peripherals										
> Sensing										
> Wi-Fi						~				
warning: redirecting to ht warning: redirecting to ht warning: redirecting to ht warning: redirecting to ht warning: redirecting to ht	ttps://gitlab.intra ttps://gitlab.intra ttps://gitlab.intra ttps://gitlab.intra	a.infineon.com/repo-staging/ a.infineon.com/repo-staging/ a.infineon.com/repo-staging/ a.infineon.com/repo-staging/	TARGET_CY8CKIT-062S2-43012.git/ retarget-io.git/ core-lib.git/ 'cat1cm0p.git/							< >
							< <u>B</u> ack	<u>C</u> reate	<u>C</u> lo	se

When the process completes, a message states that the application was created. Click **Close** to exit the Project Creator tool.

0 error(s), 0 warning(s)	^
Summary:	
Successfully created and exported "Hello_World" application.	¥
	< <u>B</u> ack <u>Create</u> <u>Close</u>

### 2.2 Export existing application

If you have a ModusToolbox<sup>™</sup> application that was created for another IDE or for the command line, you can export that application to be used in µVision. Open a terminal window in the application directory, and run the command make uvision TOOLCHAIN=ARM.

Note:	<i>For applications that were created using core-make-3.0 or older, you must use the make uvision5 command instead.</i>
Note:	This sets the TOOLCHAIN to ARM in the Keil µVision configuration files but <b>not</b> in the ModusToolbox™ application's Makefile. Therefore, builds inside Keil µVision will use the ARM toolchain while builds from the ModusToolbox™ environment will continue to use the toolchain that was previously specified in the Makefile. You can edit the Makefile's TOOLCHAIN variable if you also want ModusToolbox™ builds to use the ARM toolchain.
Note:	Check the output log for instructions and information about various flags.



### 2.3 Open application in Keil µVision

Creating or exporting the application generates the following file in the application directory:

mtb-example-psoc6-hello-world.cprj

The cprj file extension should have the association enabled to open it in Keil µVision.

1. Double-click the *mtb-example-psoc6-hello-world.cprj* file. This launches the Keil µVision IDE. The first time you do this, the following dialog displays:



- 2. Click Yes to install the device pack. You only need to do this once.
- 3. Follow the steps in the Pack Installer to properly install the device pack.

Pack Unzip: Cypress PSoC6_DFP 1.0.0	<	
License Agreement		
Please read the following license agreement carefully.		
To continue with SETUP, you must accept the terms of the License Agreement. To accept the agreement, click the check box below.		
CYPRESS END USER LICENSE AGREEMENT PLEASE READ THIS END USER LICENSE AGREEMENT ("Agreement") CAREFULLY BEFORE DOWNLOADING, INSTALLING, COPYING, OR USING THIS SOFTWARE AND ACCOMPANYING DOCUMENTATION. BY DOWNLOADING, INSTALLING, COPYING OR USING THE SOFTWARE, YOU ARE AGREEING TO BE BOUND BY THIS AGREEMENT. IF YOU DO NOT AGREE TO ALL OF THE TERMS OF THIS AGREEMENT, PROMPTLY RETURN AND DO NOT AGREE TO ALL OF THE TERMS OF THIS AGREEMENT, PROMPTLY RETURN AND DO NOT USE THE SOFTWARE. IF YOU HAVE PURCHASED THIS LICENSE TO THE		µVision ×
SOFTWARE, YOUR RIGHT TO RETURN THE SOFTWARE EXPIRES 30 DAYS AFTER YOUR	_	Software Packs folder has been modified. Reload Packs?
<< Back Next >> Cancel		Yes No

*Note:* In some cases, you may see the following error message:

SSL caching disabled in Windows Internet settings. Switched to offline mode.

See this link for how to solve this problem: <u>https://developer.arm.com/documentation/ka002253/latest</u>

- 4. When complete, close the Pack Installer and close the Keil  $\mu$ Vision IDE.
- 5. Then double-click the .cprj file again and the application will be created for you in the IDE.



# 3 Configure and build the application

1. Right-click on the *mtb-example-psoc6-hello-world* directory in the μVision Project view, and select **Options** for Target '<a physical select '> ...



- 2. On the dialog, select the C/C++ (AC6) tab.
  - Check that the Language C version was automatically set to c99.
  - Select "AC5-like warnings" in the Warnings drop-down list.
  - Select "-Os balanced" in the **Optimization** drop-down list.
  - To reduce memory usage, select the One ELF Section per Function check box.

🔣 Options for Target 'mtb-example-psoc6-hello-world'				
Device   Target   Output   Listing   User C/C++ (AC6)   Asm   Linker   Debug   Utilities				
Preprocessor Symbols				
Define:				
Undefine:				
Language / Code Generation Execute-only Code Warnings: AC5-like Warnings  Language C: C99				
Optimization: Os balanced  Tum W No Warnings Language C++: c++98				
Link-Time Optimization				
Split Load and Store Multiple MISRA Compatible pendent use RTTI				
One ELF Section per Function Read-Write Position Independent No Auto Includes				
Include Paths\mtb-example-psoc6-hello-world;.\libs Misc Controls				
Compiler control string				
OK Cancel Defaults Help				



3. Select the **Debug** tab, and select KitProg3 CMSIS-DAP as an active debug adapter:

📱 Options for Target 'mtb-example-psoc6-hello-world' 🛛 🗙					
Device   Target   Output   Listing   User   C/C++ (AC6)	Asm Linker Debug Utilities				
C Use Simulator with restrictions Settings	Use: CMSIS-DAP Debugger     Settings				
Limit Speed to Real-Time	CMSIS-DAP Debugger				
Load Application at Startup     Initialization File:	Load J-LINK / J-TRACE Cortex Models Cortex-M Debugger Initializatic ST-Link Debugger NULink Debugger				
Restore Debug Session Settings Restore Debug Session Settings Reakpoints Value Toolbox Watch Windows & Performance Analyzer Memory Display System Viewer	Restore Stellaris ICDI SiLabs UDA Debugger Wathera Blaster Cortex Debugger Waten Winnows Memory Display System Viewer				
CPU DLL: Parameter:	Driver DLL: Parameter:				
SARMCM3.DLL -REMAP -MPU	SARMCM3.DLL -MPU				
Dialog DLL: Parameter:	Dialog DLL: Parameter:				
DCM.DLL pCM4	TCM.DLL pCM4				
Wam if outdated Executable is loaded Manage Component	Wam if outdated Executable is loaded				
ОК	Cancel Defaults Help				

4. Click **OK** to close the Options dialog.

#### 5. Select **Project > Build target**.

Note:

For applications using the PSoC™ 64 MCU, skip this step. Instead, perform the steps outlined in the following section.

Build Output
compiling cy retarget io.c
linking
.\libs\TARGET CY8CPROTO-062-4343W\COMPONENT CM4\TOOLCHAIN ARM\cy8c6xxa cm4 dual.sct(144): warning: L6329W: Pattern *(.cy ramfunc) only matches removed unused sections.
.\libs\TARGET_CY8CFROTO-062-4343W\COMFONENT_CM4\TOOLCHAIN_ARM\cy8c6xxa_cm4_dual.sct(170): warning: L6314W: No section matches pattern *(.cy_app_signature).
.\libs\TARGET_CY8CPROTO-062-4343W\COMPONENT_CM4\TOOLCHAIN_ARM\cy8c6xxa_cm4_dual.sct(180): warning: L6314W: No section matches pattern *(.cy_em_eeprom).
.\libs\TARGET_CY8CPROTO-062-4343W\COMPONENT_CM4\TOOLCHAIN_ARM\cy8c6xxa_cm4_dual.sct(189): warning: L6314W: No section matches pattern *(.cy_sflash_user_data).
.\libs\TARGET_CY8CPROTO-062-4343W\COMPONENT_CM4\TOOLCHAIN_ARM\cy8c6xxa_cm4_dual.sct(198): warning: L6314W: No section matches pattern *(.cy_sflash_nar).
.\libs\TARGET_CY8CPROTO-062-4343W\COMPONENT_CM4\TOOLCHAIN_ARM\cy8c6xxa_cm4_dual.sct(207): warning: L6314W: No section matches pattern *(.cy_sflash_public_key).
.\libs\TARGET_CY8CPROTO-062-4343W\COMPONENT_CM4\TOOLCHAIN_ARM\cy8c6xxa_cm4_dual.sct(216): warning: L6314W: No section matches pattern *(.cy_toc_part2).
.\libs\TARGET_CY8CFROIO-062-4343W\COMPONENT_CM4\TOOLCHAIN_ARM\cy8c6xxa_cm4_dual.sct(225): warning: L6314W: No section matches pattern *(.cy_rtoc_part2).
.\libs\TARGET_CY8CPROTO-062-4343W\COMPONENT_CM4\TOOLCHAIN_ARM\cy8c6xxa_cm4_dual.sct(235): warning: L6314W: No section matches pattern *(.cy_xip).
.\libs\TARGET_CY8CFROIO-062-4343W\COMPONENT_CM4\TOOLCHAIN_ARM\cy8c6xxa_cm4_dual.sct(245): warning: L6314W: No section matches pattern *(.cy_efuse).
.\libs\TARGET_CY8CPROTO-062-4343W\COMPONENT_CM4\TOOLCHAIN_ARM\cy8c6xxa_cm4_dual.sct(253): warning: L6314W: No section matches pattern *(.cymeta).
Program Size: Code=19998 RO-data=8386 RW-data=440 ZI-data=1037896
Finished: 0 information, 11 warning and 0 error messages.
".\mtb-example-psoc6-hello-world_build\mtb-example-psoc6-hello-world.axf" - 0 Error(s), 11 Warning(s).
Build Time Elapsed: 00:01:31
CMSIS-DAP Debugger CAPI NUM SCRLI OVRI R /W

To suppress the linker warnings about unused sections defined in the linker scripts, add "6314,6329" to the **Disable Warnings** setting in the Project Linker Options.

### **3.1 PSoC<sup>™</sup> 64 application configuration**

Before building an application for a PSoC<sup>™</sup> 64 secure MCU in Keil µVision, you must perform the following configuration steps:

1. Build the application using the ModusToolbox<sup>™</sup> make build command. You can do this by using a Terminal or by exporting the application to Eclipse or VS Code.



2. Copy the post-build command from the log. For example:

C:/Infineon/Tools/ModusToolbox/tools\_3.1/python/python.exe C:/UG/CY8CPROTO-064S1-SB\_Secure\_Blinky\_LED\_FreeRTOS\_UG/bsps/TARGET\_APP\_CY8CPROTO-064S1-SB/psoc64\_postbuild.py -core CM4 --secure-boot-stage single --policy policy\_single\_CM0\_CM4 --target cyb06xx7 -toolchain-path C:/Infineon/Tools/ModusToolbox/tools\_3.1/gcc --toolchain GCC\_ARM --build-dir C:/UG/CY8CPROTO-064S1-SB\_Secure\_Blinky\_LED\_FreeRTOS\_UG/build/APP\_CY8CPROTO-064S1-SB/Debug --app-name\_mtb-example-psoc6-secure-blinkyled-freertos --cm0-app-path ../mtb\_shared/cat1cm0p/release-v1.0.0/COMPONENT\_CAT1A/COMPONENT\_CM0P\_SECURE --cm0-app-name psoc6\_01\_cm0p\_secure

- 3. Paste the command into an appropriate editor, and make the following edits:
  - Change --toolchain-path to the ARM toolchain; for example, C:/Keil\_v5/ARM/ARMCLANG
  - Change -- toolchain to ARM
  - Change --build-dir to Keil µVision build directory

Example of command after edit:

```
C:/Infineon/Tools/ModusToolbox/tools_3.1/python/python.exe C:/UG/CY8CPROTO-064S1-
SB_Secure_Blinky_LED_FreeRTOS_UG/bsps/TARGET_APP_CY8CPROTO-064S1-SB/psoc64_postbuild.py
--core CM4 --secure-boot-stage single --policy policy_single_CM0_CM4 --target cyb06xx7
--toolchain-path C:/Keil_v5/ARM/ARMCLANG --toolchain ARM --build-dir C:/UG/CY8CPROTO-
064S1-SB_Secure_Blinky_LED_FreeRTOS_UG/mtb-example-psoc6-secure-blinkyled-
freertos_Objects --app-name mtb-example-psoc6-secure-blinkyled-freertos --cm0-app-path
../mtb_shared/cat1cm0p/release-v1.0.0/COMPONENT_CAT1A/COMPONENT_CM0P_SECURE --cm0-app-
name psoc6_01_cm0p_secure
```

- 4. Copy the edited command.
- 5. In μVision, select **Project > Options for Target 'Target 1'...** to open the Options dialog.
- 6. Select the **User** tab and enable the **Run #1** check box under **After Build/Rebuild**. Then, paste the edited command.

🔣 Options for Target 'Target 1'				)	×
Device   Target   Output   Listing	Jser C/C++ (AC6) Asm Linker Debug Utilities				_
Command Items	User Command		Stop on Exi	S	
Before Compile C/C++ File					
		2	Not Specified	$\Box$	
🗌 🗌 Run #2		2	Not Specified	$\Box$	
⊟ Before Build/Rebuild					
Run #1		2	Not Specified	$\Box$	
Run #2		2	Not Specified		
After Build/Rebuild				_	
Run #1	C:/Infineon/Tools/ModusToolbox/tools_3.1/pyt	Z	Not Specified		
Run #2		$\geq$	Not Specified		
					4
Run 'After-Build' Conditionally					
Beep When Complete	Start Debugging				
	OK Cancel Defaults		H	Help	



7. Select the **Output** tab and enable the **Create HEX File** check box.

🕎 Options for Target 'Target 1'	×
Device Target Output Listing User C/C++ (AC6) Asm Linker Debug Utilities	
Select Folder for Objects Name of Executable: mtb-example-psoc6-secure-blinkyle	
• Create Executable: .\mtb-example-psoc6-secure-blinkyled-freertos_Objects\mtb-example-psoc6-secure	
☑ Debug Information	
Create HEX File	
I Browse Information	
C Create Library: .\mtb-example-psoc6-secure-blinkyled-freertos_Objects\mtb-example-psoc6-secure-blinkyled-freert	
OK Cancel Defaults Help	

8. On the same **Output** tab, add an ".elf" extension in the **Name of Executable** field.

W Options for Target 'Target 1'	Х
Device   Target Output   Listing   User   C/C++ (AC6)   Asm   Linker   Debug   Utilities	
Select Folder for Objects	
Create Executable: .\mtb-example-psoc6-secure-blinkyled-freertos_Objects\mtb-example-psoc6-secure	
☐ Debug Information ☐ Create Batch File	
✓ Create HEX File	
I Browse Information	
C Create Library: .\mtb-example-psoc6-secure-blinkyled-freertos_Objects\mtb-example-psoc6-secure-blinkyled-freert	
OK Cancel Defaults Help	

9. Create an empty *project.ini* file in the project root folder.



10. On the Options dialog, select the **Utilities** tab and select the *project.ini* file using the [...] button. Then, click **Edit** to open the file and click **OK** to close the options dialog.

vice Target Ou	utput Listing User C/C++ (AC6	) Asm Linker	Debug Utilities
Configure Flash M	lenu Command		
• Use Target D	viver for Flash Programming		✓ Use Debug Driver
	Use Debug Driver	Settings	✓ Update Target before Debugging
Init File: N	project.ini		[Edit]
Arguments: [			
Configure Image F	Run Independent		
Configure Image F Output File:	Run Independent	Add Output Fi	le to Group:
Configure Image Files Root	Run Independent	Add Output Fi	le to Group:  └── Generate Listing

11. Type LOAD \$L@L.hex in the project.ini file and save the file.

12. Select **Project > Build Target** to build the application and execute post-build commands.

After performing these steps, you should be able to run debug, erase, and program for PSoC<sup>™</sup> 64 secure MCUs.



## 4 Programming/Debugging

- 1. Connect the PSoC<sup>™</sup> 6 kit to the host PC.
- 2. As needed, run the fw-loader tool to make sure the board firmware is upgraded to KitProg3. See <u>KitProg3</u> <u>User Guide</u> for details. The tool is located in this directory by default:

<user\_home>/ModusToolbox/tools\_3.1/fw-loader/bin/

#### 3. Select Debug > Start/Stop Debug Session.







You can view the system and peripheral registers in the SVD view.

### 4.1 To use KitProg3/MiniProg4, CMSIS-DAP, and ULink2 debuggers

1. Select the **Device** tab in the Options for Target dialog and check that M4 core is selected:

W Options for Target 'mtb-example-psoc6-gpi	io-interrupt'	×
Device Target Output Listing User C/C++ Software Packs Vendor: Cypress Device: CY8C6247BZI-D54:Cortex-M4 Toolset: ARM Search:	ACC6) Asm Linker Debug Utilities	
CY8C6247BZI-D54     CY8C6247BZI-D54:Cortex-M0p     CY8C6247FDI-D54:Cortex-M4     CY8C6247FDI-D32     CY8C6247FDI-D32     CY8C6247FDI-D52     CY8C6247FII-D52     CY8C6247FII-D52     CY8C6247FII-D52     CY8C6247FII-D54     CY8C6248AZI-S2D14     ✓	PSoC 62 (Performance Line): Dual-core Cortex-M4/M0+ MCU series with programmable digital and analog peripherals, advanced graphics, CapSense, crypto and secure boot security.	
ОК	Cancel Defaults Help	



#### 2. Select the **Debug** tab.

Note:

To use the ULink2 probe for multi-core debugging, select the **CMSIS-DAP Debugger** instead of ULink for each core of the project (CM4 and CM0P).

3. Click the **Settings** button.

🕼 Options for Target 'mtb-example-psoc6-gpio-interrupt'				
Device     Target     Output     Listing     User     C/C++ (AC6)     A       C     Use     Simulator     with restrictions     Settings	sm Linker Debug Utilities			
✓ Load Application at Startup     ✓ Run to main() Initialization File:	✓ Load Application at Startup     ✓ Run to main() Initialization File:			
Restore Debug Session Settings Preakpoints Watch Windows & Performance Analyzer Memory Display CPU DLL: Parameter:	Restore Debug Session Settings   Restore Debug Session Settings    Restore Debug Session Settings    Restore Debug Session Settings    Restore Debug Session Settings    Restore Debug Session Settings    Restore Debug Session Settings    Restore Debug Session Settings    Restore Debug Session Settings    Restore Debug Session Settings    Restore Debug Session Settings    Restore Debug Session Settings    Restore Debug Session Settings    Restore Debug Session Settings     Restore Debug Session Settings    Restore Debug Session Settings     Restore Debug Session Settings      Restore Debug Session Settings         Restore Debug Session Settings			
SARMCM3.DLL -REMAP -MPU Dialog DLL: Parameter: DCM.DLL PCM4 Wam if outdated Executable is loaded	SARMCM3.DLL         -MPU           Dialog DLL:         Parameter:           TCM.DLL         -pCM4           Wam if outdated Even table is loaded			
Manage Component Vie	ewer Description Files			
OK Car	ncel Defaults Help			

- 4. On the Target Driver Setup dialog on the **Debug** tab, select the following:
  - set **Port** to "SW"
  - set Max Clock to "1 MHz"
  - set **Connect** to "Normal"
  - set **Reset**:
    - For PSoC<sup>™</sup> 6, to "VECTRESET"
    - For PSoC<sup>™</sup> 4, PMG1, and AIROC<sup>™</sup> CYW208xx, to "SYSRESETREQ"
  - enable **Reset after Connect** option

CMSIS-DAP - JTAG/SW Adapter Cypress MiniProg4 (CMSIS-D, Serial No: 051619880223741	SW De	IDCODE	Device Name ARM CoreSight SW	I-DP	Move Up
Max Clock: 1MHz	© Au C Ma Add	tomatic Detection inual Configuration Delete U	ID CODE: Device Name: pdate		AP: <b>0x02</b>
Connect & Reset Options     Connect: Normal     Normal     Reset atter Connect	t: VECTRI	ESET 🔽	Cache Options Cache Code Cache Memory	Download Optio	ns Download o Flash



5. Select the **Flash Download** tab and select "Reset and Run" option after download, if needed:

CMSIS-DAP Cortex-M Target Drive Debug Trace Rash Download Download Function Composed Function C Erase Full Chip C Erase Sectors C Do not Erase	Pack	RAM for J Start:	Algorithm	×
Programming Algorithm Description CY8C6xxx_SFLASH_TOC2 CY8C6xxx_SFLASH_PKEY CY8C6xxx_SFLASH_USER CY8C6xxx_WFLASH CY8C6xxx_WFLASH	Device Size 1k 3k 2k 32k	Device Type On-chip Flash On-chip Flash On-chip Flash On-chip Flash	Address Range 16007C00H - 16007FFFH 16005A00H - 160065FFH 16000800H - 16000FFFH 14000000H - 1007FFFH	
	Add	Start:	Size:	
	OK	Cance	el Hel	p

6. Select the **Pack** tab and check if "Cypress.PSoC6\_DFP" is enabled:

CMSIS-DAP Cortex-M Target Driver Setup		Х
Debug   Trace   Flash Download   Pack		
Debug Description		$\neg$
Pack: Cypress.PSoC6_DFP.1.0.0		
🔽 Enable 🔲 Enable Flash Sequences		
Log Sequences: D:\CyP\tmp\new\KeilProject\CY8CKIT-062-WIFI-BT\EM\mtb-example-psoc6-gpio-inter		
Configuration:	E dit	1
OK Cancel	Help	



### 4.2 To use J-Link debugger with PSoC<sup>™</sup> MCUs

- 1. Make sure you have J-Link software version 6.62 or newer.
- 2. Select the **Debug** tab in the Options for Target dialog, select J-LINK / J-TRACE Cortex as debug adapter, and click "Settings":

8				
Options for Target 'mtb-example-psoc6-gpio-interru	pť X			
Device   Target   Output   Listing   User   C/C++ (AC6)   A	sm Linker Debug Utilities			
C Use Simulator <u>with restrictions</u> <u>Settings</u> Limit Speed to Real-Time	Use: J-LINK / J-TRACE Cortex Settings			
✓ Load Application at Startup ✓ Run to main() Initialization File:	✓ Load Application at Startup Initialization File:			
Edit	Edit			
Restore Debug Session Settings	Restore Debug Session Settings			
🔽 Breakpoints 🔽 Toolbox	I Breakpoints I Toolbox			
✓ Watch Windows & Performance Analyzer	✓ Watch Windows			
Memory Display Vistem Viewer	Memory Display Vistem Viewer			
CPU DLL: Parameter:	Driver DLL: Parameter:			
SARMCM3.DLL -REMAP -MPU	SARMCM3.DLL -MPU			
Dialog DLL: Parameter:	Dialog DLL: Parameter:			
DCM.DLL -pCM4	TCM.DLL -pCM4			
Warn if outdated Executable is loaded				
Manage Component Viewer Description Files				
ОК Са	ncel Defaults Help			

3. If you see the following message, click **OK** in the Device selection message box:

Cortex JLink/JTrace Target Driver Setu	р	$\times$
Debug Trace Flash Download		
J-Link / J-Trace Adapter	JTAG Device Chain	
SN:  Device:	TDO	Move Up
HW : dll :	ТОІ	Down
J-Link V6.62 J-Link V6.62 Device	Selection ?	×
The selected device "CY8C624	7BZI-D54:CORTEX-M4" is unknown to this version of the J-Link	software.
Please make sure that at least the Proper device selection is required for flash download or unlimited for flash download or u	he core J-Link shall connect to, is selected. ired to use the J-Link internal flash loaders J flash breakpoints.	
For some devices which requir	e a special handling, selection of the correct device is important	
		D.K. Dad



### 4. Select the appropriate target in Wizard:

elected Device: C	Y8C6xx7_CM4			Little End	dian 🔻 Core 🕯	#0
Manufacturer	Device	Core	NumCores	Flash Size	RAM Size	
Cypress	CY8C6xx6_CM4	Cortex-M4	1	512 KB + 32 K	32 KB	
Cypress	CY8C6xx6_CM4_sect256KB	Cortex-M4	1	512 KB + 32 K	32 KB	
Cypress	CY8C6xx7_CM0p	Cortex-M0	1	1 MB + 32 KB	32 KB	
Cypress	CY8C6xx7_CM0p_sect256KB	Cortex-M0	1	1 MB + 32 KB	32 KB	
Cypress	CY8C6xx7_CM0p_sect256KB_tm	Cortex-M0	1	1 MB + 32 KB	32 KB	
Cypress	CY8C6xx7_CM0p_tm	Cortex-M0	1	1 MB + 32 KB	32 KB	
Cypress	CY8C6xx7_CM4	Cortex-M4	1	1 MB + 32 KB	32 KB	
Cypress	CY8C6xx7_CM4_sect256KB	Cortex-M4	1	1 MB + 32 KB	32 KB	
Cypress	CY8C6xxA_CM0p	Cortex-M0	1	2 MB + 32 KB	32 KB	
Cypress	CY8C6xxA_CM0p_sect256KB	Cortex-M0	1	2 MB + 32 KB	32 KB	
Cypress	CY8C6xxA_CM0p_sect256KB_t	Cortex-M0	1	2 MB + 32 KB	32 KB	
Cypress	CY8C6xxA_CM0p_tm	Cortex-M0	1	2 MB + 32 KB	32 KB	
Cypress	CY8C6xxA_CM4	Cortex-M4	1	2 MB + 32 KB	32 KB	
Cypress	CY8C6xxA_CM4_sect256KB	Cortex-M4	1	2 MB + 32 KB	32 KB	
Cypress	CYBL10xxx	Cortex-M0	1	128 KB	16 KB	
< li>	CV0140 050	C · 10	4	and KB	22.10	>

#### 5. Go to **Debug** tab in **Target Driver Setup** dialog and select:

- set Port to "SW"
- set Max Clock to "1 MHz"
- set Connect to "Normal"
- set Reset to "Normal"
- enable Reset after Connect option

J-Link / J-Trace Adapter	SW Device	e		
SN: 50107842 -	SWD	IDCODE	Device Name	Move
Device: J-Link		O 0X6BA024//	ARM CoreSignt SW-DP	Up
HW : V10.10 dll : V6.62d				Down
Port: Max Clock:	C Autom	natic Detection	ID CODE:	
SW 👻 1 MHz 👻	C Manu	al Configuration	Device Name:	
Auto Clk	Add	I succession		
AULU CIK				
Connect & Reset Ontions				ad Ontions
Connect & Reset Options Connect Normal  Reset: Reset after Connect	Normal	Cach	e Options Downlo ache Code ache Memory	ad Options ify Code Download wnload to <u>F</u> lash
Connect & Reset Options Connect Normal Reset: Reset after Connect	Normal	Cach	e Options Downlo ache Code ache Memory	ad Options ffy Code Download wnload to <u>F</u> lash Misc
Connect & Reset Options Connect Nomal Reset: Reset after Connect Interface USB C TCP/IP	Normal Settings	Delece Up Cach	e Options Downlo ache Code ache Memory Dow	ad Options fry Code Download wnload to Eash Misc JLink Info
Connect & Reset Options Connect Normal  Reset: Reset after Connect Interface USB C TCP/IP Scan	Normal Settings sss . 0 . 0 .	Pott (Au . 1 : □ 0	e Options Downlo ache Code ache Memory Downlo	Misc



6. Select the **Flash Download** tab in **Target Driver Setup** dialog and select "Reset and Run" option after download if needed:

Cortex JLink/JTrace Target Driver	Setup			×
Debug Trace Flash Download				
Download Function C Erase Full Chip C Erase Sectors C Do not Erase	<ul> <li>✓ Program</li> <li>✓ Verify</li> <li>✓ Reset and F</li> </ul>	RAM for J Start:	Vgorithm 2x08026400 Size: 0x8000	
Description CY8C6xx_SFLASH_TOC2 CY8C6xx_SFLASH_PKEY CY8C6xx_SFLASH_USER CY8C6xx_WFLASH CY8C6xx7_sect256KB	Device Size 1k 3k 2k 32k 1M	Device Type On-chip Flash On-chip Flash On-chip Flash On-chip Flash On-chip Flash	Address Range 16007C00H - 16007FFFH 16005A00H - 160065FFH 16000800H - 16000FFFH 14000000H - 14007FFFH 10000000H - 100FFFFFH	
	Add	Start:	Size:	
			OK Cancel Appl	y _

### 4.3 To use J-Link debugger with XMC7000 devices

### 4.3.1 **Program set-up instructions**

1. Select the **Debug** tab in the Options for Target dialog, select "J-LINK / J-TRACE Cortex" as the debug adapter, and click **Settings**.

🔣 Options for Target 'Target 1'	×
Device   Target   Output   Listing   User   C/C++ (AC6)   A	sm Linker Debug Utilities
Use Simulator with restrictions     Settings     Limit Speed to Real-Time	Use: J-LINK / J-TRACE Cortex      Settings
Load Application at Startup     Initialization File:     Load Application at Startup     Initialization File:     Load Application at Startup     Load Application at Startup     Initialization File:     Load Application File:     Initialization File:     Load Application File:     Initialization Fi	Image: Vertication at Startup     Image: Vertication Telle:       Image: Vertication File:     Image: Vertication Telle:       Image: Vertication Telle:     Image: Vertication Telle:
Restore Debug Session Settings         Image: Seakpoints       Image: Toolbox         Image: Seakpoints       Image: Seakpoints         Image: Seakpoints       Image: Seakpoints <t< td=""><td>Restore Debug Session Settings         I Breakpoints       I Toolbox         I Watch Windows       I Tracepoints         I Memory Display       I System Viewer</td></t<>	Restore Debug Session Settings         I Breakpoints       I Toolbox         I Watch Windows       I Tracepoints         I Memory Display       I System Viewer
CPU DLL: Parameter: SARMCM3 DLL -REMAP -MPU	Driver DLL: Parameter:
Dialog DLL: Parameter: DCM.DLL pCM7	Dialog DLL: Parameter: TCM.DLL pCM7
Wam if outdated Executable is loaded Manage Component Vi	Warn if outdated Executable is loaded
OK Ca	ncel Defaults Help



2. On the **Debug** tab in the Cortex J-Link/JTrace Target Driver Setup dialog, select "Connect under Reset" on the **Reset** pull-down menu, and then click **OK**.

Cortex JLink/JTrace Target Driver Setup	×
Debug Trace Flash Download	
J-Link / J-Trace Adapter SW D	evice
SN: 504403253 -	IDCODE Device Name Move
Device: J-Link Ultra SV	/D 💿 0x6BA02477 ARM Core Sight SW-DP
HW : V4.00 dll : V7.70	Down
FW : J-Link Ultra V4 compiled Sep :	
Port: Max Clock: © A	utomatic Detection ID CUDE:
Auto Clk	Id Delete Update IH len:
Connect & Reset Options Connect: Normal  Reset: Normal Reset after Connect Normal Core Reset Pin Interface Connect under the connect under the connec	Cache Options ✓ Cache Code ✓ Cache Memory der Reset
IP-Add Halt before Scan State: ready	Bootloader er Kemel ripherals
	OK Cancel Apply

3. Select the **Utilities** tab in the Options for Target dialog and deselect the **Update target before Debugging** check box.

V Options for Target 'Target 1'	×
Device Target Output Listing User C/C++ (AC6) Asm Linker Debug Utilities	
Configure Flash Menu Command	
Use Debug Driver Settings	
Init File:	
C Use External Tool for Flash Programming	
Command:	
Arguments:	
🗖 Run Independent	
- Configure Image File Processing (FCARM):	
Output File: Add Output File to Group:	
Source	
Image Files Root Folder:	
OK Cancel Defaults Help	,



### 4.3.2 Debug set-up instructions

1. Select the **Debug** tab in the Options for Target dialog, select "J-LINK / J-TRACE Cortex" as the debug adapter, and click **Settings**.

🔣 Options for Target 'Target 1'	×
Device   Target   Output   Listing   User   C/C++ (AC6)   A	sm Linker Debug Utilities
C Use Simulator with restrictions Settings Limit Speed to Real-Time	Ise: J-LINK / J-TRACE Cortex
Load Application at Startup     Initialization File:	Load Application at Startup     Run to main() Initialization File:     Load Application Edit
Restore Debug Session Settings         Image: Breakpoints         Image: Breakpoints	Restore Debug Session Settings         Image: Session Settings
Dialog DLL:     Parameter:       DCM.DLL     pCM7       Warn if outdated Executable is loaded	Dialog DLL: Parameter: TCM.DLL pCM7 Warn if outdated Executable is loaded ever Description Files
OK Car	ncel Defaults Help

2. On the **Debug** tab in the **Target Driver Setup** dialog:

- **Reset** pull-down: select "Normal," "Core" or "Reset Pin"
- **Download Options**: enable "Verify Code Download" and "Download to Flash"

	SW Devic	ce		
SN: 504403253 💌		IDCODE	Device Name	Move
Device: J-Link Ultra	SWD	⊙ 0x6BA02477	ARM CoreSight SW-DP	Up
HW : V4.00 dll : V7.70				Down
FW : J-Link Ultra V4 compiled Sep :		1		
Port: Max Clock:	C Auto	matic Detection	ID CODE:	
SW V 2 MHz V	C Man	ual Configuration	Device Name:	
Auto Clk	Add	Delete I In	date IR len:	
			,	
			,	
Connect & Reset Options		Cach	e Options — Download Op	otions
Connect & Reset Options Connect: Normal   Reset: Mc	mal	Cach	e Options Download Op ache Code Verify Cod	otions de Download
Connect & Reset Options Connect: Normal  Reset: Normal Reset after Connect	rmal	Cach	e Options ────────────────────────────────────	otions de Download d to <u>Fl</u> ash
Connect & Reset Options Connect: Normal ▼ Reset: Normal Reset after Connect Con Reset after Connect Re	mal mal re set Pin	Cach	e Options ache ⊆ode ache Memory	otions de Download d to <u>Fl</u> ash
Connect & Reset Options Connect: Normal ▼ Reset: Normal Reset after Connect Re Interface TCP/IP Connect	mal mal re iset Pin nnect under	Cach	e Options Download Op ache ⊆ode ache Memory ↓ Verify Cor V Download	otions de Download d to <u>Fl</u> ash Misc
Connect & Reset Options Connect: Normal ▼ Reset: Normal ■ Reset after Connect Connect Interface TCP/IP ● USB © TCP/IP	mal mal re set Pin nnect under It after Bootl It before Boot	Reset oader otloader	e Options Download Op ache Code ache Memory Verify Cov Download to: 0) Autodetect	de Download d to <u>F</u> lash /lisc JLink Info
Connect & Reset Options Connect: Normal ▼ Reset: Normal ■ Reset after Connect C Re Interface TCP/IP © USB © TCP/IP Scan 127 AD	mal mal re set Pin nnect under lt after Bootk lt before Boo retis JI Halt after P	Reset oader otloader Kemel : 0	e Options Download Op ache Code ache Memory Verify Cov Download to: 0) Autodetect	de Download de Download d to Flash Misc JLink Info



### 4.4 Program external memory

1. Download internal flash as described above.

Notice "No Algorithm found for: 18000000H - 1800FFFFH" warning.

2. Select the **Flash Download** tab in **Target Driver Setup** dialog and remove all programming algorithms for On-chip Flash and add programming algorithm for External Flash SPI:

CMSIS-DAP Cortex-M Target Driver Setup	×
Debug Trace Flash Download Pack	
Download Function       C       Frase Full Chip       ✓       Program         Image: C       Erase Sectors       ✓       Verify       Start:       0x08026400       Size:       0x00008000         Image: C       Do not Erase       ✓       Reset and Run       C       Start:       0x08026400       Size:       0x00008000	
Programming Algorithm	
Description         Device Size         Device Tune         Address Bance           CY8C6xx_SFLASH_TOC2         1k         On-chip Flash         16007C00H - 16007FFH           CY8C6xx_SFLASH_PKEY         3k         On-chip Flash         16005A00H - 160065FFH           CY8C6xx_SFLASH_USER         2k         On-chip Flash         16000800H - 16000FFFH           CY8C6xx_WFLASH         32k         On-chip Flash         14000000H - 14007FFFH           CY8C6xx7_sect256KB         1M         On-chip Flash         10000000H - 100FFFFFH	
Start: 0x16007C00 Size: 0x00000400	
Add Remove	
OK Cancel Help	
CMSIS-DAP Cortex-M Target Driver Setup           Debug         Trace         Flash Download         Pack	×
Download Function       C Erase Full Chip       ✓ Program         Image: C Erase Sectors       ✓ Verify       Start:       0x08026400       Size:       0x00008000         Image: C Erase Sectors       ✓ Reset and Run       Fase       Image: C Erase Sectors       Image	
Programming Algorithm	
Description         Device Size         Device Type         Address Range           CY8C6xx_SMIF         128M         Ext. Flash SPI         18000000H - 1FFFFFFH	
Start: 0x18000000 Size: 0x08000000	
Add Remove	

3. Download flash.

Notice warnings:

- No Algorithm found for: 1000000H 1000182FH
- No Algorithm found for: 10002000H 10007E5BH
- No Algorithm found for: 16007C00H 16007DFFH



### 4.5 Erase external memory

1. Select the **Flash Download** tab in **Target Driver Setup** dialog and remove all programming algorithms for On-chip Flash and add programming algorithm for External Flash SPI:

CMSIS-DAP Cortex-M Target Driver Setup	×
Debug Trace Flash Download Pack	
Download Function         C Erase Full Chip         ▼ Program           ● Erase Sectors         ▼ Verify           C Do not Erase         ▼ Reset and Run	
Programming Algorithm	
Description         Description         Address Bance           CY8C6xx_SFLASH_TOC2         1k         On-chip Flash         16007C00H - 16007FFFH           CY8C6xx_SFLASH_PKEY         3k         On-chip Flash         16005A00H - 16006FFFH           CY8C6xx_SFLASH_USER         2k         On-chip Flash         160005A00H - 16000FFFH           CY8C6xx_WFLASH         32k         On-chip Flash         1600000H - 16007FFFH           CY8C6xx7_sect256KB         1M         On-chip Flash         1000000H - 100FFFFH	
Start: 0x16007C00 Size: 0x00000400	
Add Remove	
OK Cancel Help	
CMSIS-DAP Cortex-M Target Driver Setup	×
Debug Trace Flash Download Pack	
Download Function         RAM for Algorithm           C Erase Full Chip         ✓ Program           ⓒ Erase Sectors         ✓ Verfy           C Do not Erase         ✓ Reset and Run	
Programming Algorithm	
Description         Device Size         Device Troe         Address Range           CY8C6xx_SMIF         128M         Ext. Rash SPI         18000000H - 1FFFFFFH	
Start: 0x18000000 Size: 0x08000000	
Add Remove	
OK Cancel Help	

2. Click **Flash > Erase** in menu bar.



### 5 Multi-core debugging

This section explains how to set up multi-core debugging in the  $\mu$ Vision IDE.

#### 5.1 Supported debugger probes

- KitProg3 onboard programmer
- MiniProg4
- ULINK2
- J-Link

### 5.2 Opening µVision multi-core projects

After you create a ModusToolbox<sup>™</sup> multi-core application for use with µVision, do the following:

1. Navigate to ModusToolbox<sup>™</sup> project directory for one of the cores and double-click project description file (either \*.cprj or \*.cpdsc depending on μVision version).

The first time you do this, a dialog may pop-up offering to install missing CMSIS-Pack. Click **Yes** and the pack will be installed.

2. Repeat the same process for the CM4/CM7 project(s). This will create and open µVision projects.

### 5.3 Debugger configuration

Next, configure projects to launch multi-core debugging.

### 5.3.1 Configure CM0+ project

1. Go to **Project > Options for Target <target\_name>**, switch to the **Debug** tab, select the applicable debug probe (CMSIS-DAP or J-Link) as shown:



- If using ULINK2, select the **CMSIS-DAP Debugger** option as the debug probe, because the ULINK2 driver does not support multi-core debugging.
- 2. Click the **Settings** button to configure the target driver.
  - If you select the J-Link probe, a pop-up window might display reporting that the device is unknown to J-Link software.



• If so, click **O.K.** and select the device manually in the opened Target device settings dialog. For XMC7200 devices, there will be three aliases, each dedicated to a separate core.





3. Switch to the **Flash Download** tab, select the **Erase Sectors** radio button, and select the **Program**, **Verify**, and **Reset and Run** check boxes.

CMSIS-DAP Cortex-M Target Drive	er Setup			×
Debug Trace Flash Download	Pack			
Download Function Carase Full Chip Frase Sectors C Do not Erase	<ul> <li>✓ Program</li> <li>✓ Verify</li> <li>✓ Reset and I</li> </ul>	RAM for A	Algorithm 2x08002400 Size: [0x00008000	
Programming Algorithm	,			
Description	Device Size	Device Type	Address Range	
CY8C6xxA_SFLASH_TOC2	1k	On-chip Flash	16007C00H - 16007FFFH	
CY8C6xxA_SFLASH_PKEY	3k	On-chip Flash	16005A00H - 160065FFH	
CY8C6xxA_SFLASH_USER	2k	On-chip Flash	16000800H - 16000FFFH	
CY8C6xxA_WFLASH	32k	On-chip Flash	14000000H - 14007FFFH	
CY8C6xxA_sect256KB	2M	On-chip Flash	1000000H - 101FFFFFH	
1		Start:	Size:	
	Add	Remove		
	0	( Cance	el He	lp 🔤

- 4. Click **OK** to close the Target Driver Setup dialog.
- 5. Next, configure the project so that it also programs other image(s) from the CM4/CM7 project(s). Do this using the \*.ini file.
  - a. Create a new empty file named *load\_cmx.ini* and save it inside the CM0+ project directory.
  - b. Add a LOAD command with a path to the CM4/CM7 images. For example:

LOAD "../\proj cm4/\proj cm4 Objects/\proj cm4.axf"

- c. Add as many LOAD commands for all the CM4/CM7 projects as you have.
- 6. Go to **Project > Options for Target <target\_name>**, select the **Utilities** tab, and specify the created *load\_cmx.ini* file in the **InitFile** edit field.



7. Switch to the **Debug** tab, and click the **Settings** button.

The configuration settings are different for CMSIS-DAP/ULINK2 and J-Link. Refer to the following sections for the applicable options:

- CMSIS-DAP/ULINK2 Target Driver Setup Use the following options:
  - Port: SW
  - Max Clock: 1 MHz
  - Connect: Normal
  - **Reset**: SYSRESETREQ



CMSIS-DAP Cortex-M Target Driver Set	tup				×
Debug Trace   Flash Download   Pack	k				
CMSIS-DAP - JTAG/SW Adapter	SW De	vice			
Any 👻		IDCODE	Device Name		Move
Serial No: 181201A50024940	SWDIO	⊙ 0x6BA02477	ARM CoreSight SW	-DP	Up
Firmware Version: 2.0.0					Down
SWJ Port: SW 🗸	© Au	tomatic Detection			
Max Clock: 1MHz 👤	Add	I Delete U	odate	AP: D	(01
Debug Connect & Reset Options			Cache Options	Download Option	ns
Connect: Nomal	OP after R	setreq 💌	<ul> <li>Cache Code</li> <li>Cache Memory</li> </ul>	Download to	Download Flash
		ОК С	ancel		Help

- J-Link Target Driver Setup Use the following options:
  - Port: SW
  - Max clock: 1 MHz
  - Connect: Normal
  - **Reset**: Normal

ortex JLink/JTrace Target Driver Setup				
Debug Trace   Flash Download				
J-Link / J-Trace Adapter	SW Devi	ce		
SN: 50107842		IDCODE	Device Name	Move
Device: J-Link	SWD	⊙ 0x6BA02477	ARM CoreSight SW-DP	Up
HW: V10.10 dll: V7.70e				Down
FW : J-Link V10 compiled Jul 22 20		1		
Port: Max Clock:	C Auto	matic Detection	ID CODE:	
SW 💌 1 MHz 💌	C Man	ual Configuration	Device Name:	
Auto Clk	Add	Delete Up	date IB len:	
Connect & <u>Reset Options</u> Connect Normal  Reset: I Reset after Connect	Normal	⊂ach ▼ C ▼ C	e Options Downloa ache Code ache Memory Downloa	ad Options y Code Download inload to <u>F</u> lash
Interface     TCP/IP     VSB C TCP/IP     Vetwork     IP-Addree	Settings	Port (Au	to: 0) Autodetect	Misc JLink Info
Scan 127 State: ready	. 0 . 0	. 1 : 0	Ping	JLink Cmd

That completes configuring the CM0+ project. The next step is to configure CM4/CM7 project(s).

### 5.3.2 Configure CM4/CM7 project

1. Go to **Project > Options for Target <target\_name>**, switch to the **Utilities** tab and deslect the Update Target before Debugging check box.

Device   Target   Output   Listing   User   C/C++ (AC6)   Asm   Linker	Debug Utilities
Configure Flash Menu Command	
O Use Target Driver for Flash Programming	Vse Debug Driver
Use Debug Driver Settings	Update Target before Debugging
Init File:\pror_cm7_0.ini	Edit
C Use Esternal Teal for Back Programming	
O use External roomor hash Programming	
Command:	

- 2. Switch to the **Debug** tab, select the applicable debug probe (CMSIS-DAP or J-Link).
  - If using ULINK2, select the **CMSIS-DAP Debugger** option as the debug probe, because the ULINK2 driver does not support multi-core debugging.
- 3. Click the **Settings** button to configure the target driver.



4. On the Target Driver Setup dialog, switch to the **Flash Download** tab, select the **Do not Erase** radio button, and deselect the **Program**, **Verify**, and **Reset and Run** check boxes.



5. Switch to the **Debug** tab.

The configuration settings are different for CMSIS-DAP/ULINK2 and J-Link. Refer to the following for the appropriate options:

- CMSIS-DAP/ULINK2 Target Driver Setup Use the following options:
  - Port: SW
  - Max Clock: 1 MHz
  - **Connect**: Normal
  - Reset: VECTRESET
  - Reset after Connect check box: deselected

CMSIS-DAP Cortex-M Target Driver Setup	×
Debug Trace   Flash Download   Pack	
CMSIS-DAP - JTAG/SW Adapter         SW Device           Arry         IDCODE         Device Name           Serial No: [181201A5002494]         SWDIO         O 0x68A02477         ARM CoreSight SW-DP	Move Up Down
Image: Swight	2
Debug     Connect # Reset Options     Download Options       Connect: Normal     Reset: VECTRESET     Image: Connect Connec	wnload Iash
OK Cancel	Help

- J-Link Target Driver Setup Use the following options:
  - Port: SW
  - Max Clock: 1 MHz
  - **Connect**: Normal
  - Reset: Core
  - Reset after Connect check box: deselected



Cortex JLink/JTrace Target Driver Setup				×
Debug Trace   Flash Download				
J-Link / J-Trace Adapter	SW Devi	ce		
SN: 50107842 -		IDCODE	Device Name	Move
Device: J-Link	SWD	⊙ 0x6BA02477	ARM CoreSight SW-DP	Up
HW: V10.10 dll: V7.70e				Down
FW : J-Link V10 compiled Jul 22 20				
Port: Max Clock:	€ Auto	matic Detection	ID CODE:	
SW 💌 1 MHz 💌	C Man	ual Configuration	Device Name:	
Auto Clk	Add	Delete Upo	late IR len:	_
Connect & Reset Options Connect: Normal  Reset: Core		Cache	e Options Downloa ache <u>C</u> ode <u>V</u> erify	d Options Code Download
<u>R</u> eset after Connect		l <b>v</b> u	ache <u>M</u> emory	lioad to <u>F</u> lash
Interface C USB C TCP/IP Scan State: ready Iteration	ings . 0	Port (Au	to: 0) Autodetect Ping	Misc JLink Info JLink Cmd
			OK Cano	el <u>Apply</u>

- 6. Click **OK** to close the Target Driver Setup dialog.
- 7. Save the project(s).

#### 5.4 Launching multi-core debug session

To launch a multi-core debug session, all your µVision projects must be opened in separate IDE instances.

- Open a μVision IDE session with the project for the CM0+ core and start debugging by pressing Debug > Start/Stop Debug Session. This will program all images, reset the target, and halt at the beginning of the CM0+ project main ().
- 2. Repeat the same process for the CM4/CM7 core(s). This will attach the running CM4/CM7 core that will be spinning in the boot code until the CM0+ project starts it.

*Note: Ensure both projects are built before launching a debug session.* 



For dual-core MCUs, the projects will appear similar to these images:



The left side of the screen shows a  $\mu$ Vision IDE instance attached to the CM0+ core. The right side shows the CM4 core has not started yet. Once the Cy\_SysEnableCM4() function on the CM0+ core has been executed, the CM4 will start executing its application. You can step through the code by switching back and forth between the two  $\mu$ Vision IDE instances.



#### Patched flashloaders for AIROC<sup>™</sup> CYW208xx devices

### 6 Patched flashloaders for AIROC<sup>™</sup> CYW208xx devices

To enable support for different QSPI settings, the ModusToolbox<sup>™</sup> QSPI Configurator patches flashloaders and stores files for them in the application directory. When exporting such applications to Keil µVision, these patched flashloader files must be copied into the appropriate directory.

- 1. Copy the CYW208xx\_SMIF.FLM file.located in the <app-dir>\libs\<Kit-Name>\COMPONENT\_BSP\_DESIGN\_MODUS\GeneratedSource directory.
- 2. Paste the flashloader file to the C:\Program Files\IAR Systems\Embedded Workbench 9.0\arm\config\flashloader\Infineon\CYW208XX directory.
- 3. Also, to use the SEGGER J-Link debugger, paste the *CYW208xx\_SMIF.FLM* file to the *C:\Program Files\SEGGER\J-Link\Devices\Cypress\cat1b* directory.



### **Revision history**

# **Revision history**

Revision	Date	Description
**	2023-05-15	New document.
*A	2023-06-02	Removed obsolete instructions for customizing linker scripts.

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