Frequently Asked Questions

Product Name: System Basis Chips (SBCs) **Date:** August 2018
Application: Automotive ECUs **Datasheet:** TLE926x(-3)BQX
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Mid-Range+ SBC

Question 1: Chapter 3	What's the difference between **n.c.** pins and **N.U.** pins?
Answer:	**n.c.** pins means "not connected pins". They are high impedance pins and internally not bonded to the chip. These pins can be left floating. It is recommended to connect to GND to improve thermal behavior. **N.U.** pins means not used pin. These pins are electrically connected to the silicon chip, therefore they should be left open on the PCB. In case N.U. pins are connected on the board an open bridge has to be foreseen to avoid external disturbances.
Question 2: Chapter 3.3	How shall I connect the unused pins?

Answer:	Please refer to the following recommendations:
	• WK1/2/3: connect to GND and disable WK inputs via SPI
	• HSx: leave open
	• LIN, CAN: leave all pins open
	• RO, FOx: leave open
	• INT: leave open
	• TEST:
	  ○ To activate SBC Development Mode, connect to GND during power-up operation. The connection can be removed after power-up
	  ○ For normal operations, leave open
	• VCAN: connect to VCC1
	• VCC2: leave open and keep disabled
	VCC3: Do not enable the VCC3 via SPI if not used because this will lead to an increased current consumption.
	• VCC3SH: Connect to VS or leave open
	• VCC3B, VCC3REF: leave open

Question 3: Chapter 4.1.4	What does this mean: "VCC2 is short-to-battery protected"?
Answer:	Regulators with a maximum output voltage rating less than the battery voltage (e.g. 5V) will be damaged in case of a short to the battery. The VCC2 output pin of Mid-Range SBC can withstand a voltage up to 28V, and temporarily up to 40V for load dump. Therefore this SBC will not be damaged even if the output pin is shorted to the battery (or to GND over long cable).
Question 4: Chapter 4.4	What is the current consumption adder during cyclic sense in SBC Stop or Sleep Mode?
Answer:	The current consumption adder for cyclic sense (CS) with one high-side switch in SBC Stop Mode can be calculated using following equation: IStop,CS = 20µA + (550µA *ton-time/Tperiod). The same applies for SBC Sleep Mode. A typ. 75µA / max 125µA (Tj= 85°C) adder applies for every additionally activated HSx switch.

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Question 5: **Chapter 4.4**	How can we calculate the High-Side Switch (HSS) current consumptions for every additional activated HSx switch in SBC Stop or Sleep Mode?
Answer:	When one of the four HSS is already turned on during SBC Stop Mode, the additional current consumption is typ. 575µA / max 700µA (Tj = 85°C). A typ. 75µA / max 125µA (Tj = 85°C) adder applies for every additionally activated HSx switch in SBC Stop Mode. The current consumption for cyclic sense is reduced by the duty cycle of the configured period and on-time.
Question 6: **Chapter 4.4**	Is “the VCC2 low power mode current consumption in SBC stop mode” the same to the VCC2 current consumption in SBC sleep mode?
Answer:	The VCC2 current is almost the same for SBC Stop and for SBC Sleep Mode. Please refer to (P_4.4.19) and (P_4.4.20). Note: You do not have to enable VCC2 for SBC Stop or SBC Sleep Mode for the CAN wake capable mode.
Question 7: **Chapter 4.4**	What is the contribution of the watchdog operation to the SBC current consumption during SBC stop mode?
Answer:	Additional 20µA typ. is required at 25°C. For more details, please refer to the datasheet, (P_4.4.30) and (P_4.4.31).
Question 8: **Chapter 4.4**	What is the HSS current consumption value for 1 * HSx in SBC Stop Mode without cyclic sense?
Answer:	The difference on the HS current consumptions with and without cyclic sense is that the current consumption in cyclic sense is reduced by the duty cycle (ton/Tperiod). See also the footnotes of the datasheet parameters (P_4.4.23), (P_4.4.27), (P_4.4.33) and (P_4.4.34).
Question 9: **Chapter 5.1**	Is the transition from SBC Init Mode to SBC Normal Mode automatic, or do we have to send a SPI command?
Answer:	The transition from SBC Init Mode to SBC Normal Mode is triggered by **ANY** SPI command, sent by the microcontroller. A recommendation is to use the first watchdog trigger command, which is sent with the watchdog timing chosen. In this case no additional SPI command must be sent for entering the SBC Normal Mode.
Question 10: **Chapter 5.1.1**	What is the watchdog mode after power-up? Window watchdog or time-out/standard watchdog?
Answer:	The default watchdog mode is time-out watchdog.
Question 11: **Chapter 5.1.1.2**	Do you have some recommendation for the sequence of initial settings?
Answer:	After the Power-On Reset (POR), the SBC is in SBC Init Mode. Then following actions are recommended: • Watchdog trigger and watchdog (WD) settings • Configure VCC3 for load sharing, if used • Clear the POR bit for proper diagnosis • All other initializations of the SBC peripherals (CAN, LIN, HSx, WKx, etc.) The actual sequence and timing of the commands depend on the application and other boundary conditions (e.g. microcontroller, drivers, functional safety requirements, etc.).

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Question 12: **Chapter 5.1.4**	SBC Stop Mode is used for our application in low-power mode of the ECU. There is a concern to accidentally enter SBC Sleep Mode (VCC1 OFF) by single point failure. Is there any suggestion to reduce this risk?
Answer:	One suggestion is to set a wake-flag as “1” and leave it intentionally (just after SBC initialization) because SBC Sleep Mode access is prevented when wake-flags are still set. One possibility would be following configuration after power-up: • Create an internal wake-event (TIMER_WU) from an unused timer (Timer 1 or Timer 2) using cyclic wake • Keep this bit set (do not clear in the register). Only then, set other wake sources before entering SBC Stop Mode. • In case other wake sources are set and the register needs to be cleared, the procedure should be repeated. As explained in Chapter 5.1.4, to enter SBC Sleep Mode successfully, all wake source signalization flags from WK_STAT_1 and WK_STAT_2 need to be cleared. A failure to do so results in an immediate wake-up from SBC Sleep Mode (going via SBC Restart to Normal Mode).
Question 13: **Chapter 8**	What is the current capability and the current limitation of VCC3?
Answer:	Current capability of VCC3: • VCC3 is designed to drive PNP transistors with a base current from VCC3B of up to 80mA. Depending on the current amplification of the respective PNP the collector current could be a multiple. For power dissipation and thermal protection reasons, also PNPs can be driven in parallel. • The maximum power dissipation of the PNP determines the current capability and needs to be managed to avoid a thermal damage. With e.g. 400mA and VS = 16V the power dissipation is 4.4W in a 5V configuration, which can only be managed for short periods because the heat cannot be dissipated from the PCB itself. Assuming an Rth of 40K/W and an ambient temperature of 85°C, the junction temperature of the PNP would increase to ~300°C, which is too high for the PNP on a steady state level. In addition the overall SBC power dissipation also needs to be considered Current limitation of VCC3: • In stand-alone configuration, the current limitation for the PNP is determined by the shunt resistor between VS and VCC3SH. • In load-sharing configuration, the current limitation is only indirect by the current limitation of VCC1.
Question 14: **Chapter 8**	Is it possible to set VCC1=3.3V, VCC2=5V and VCC3=5V?
Answer:	Yes, it is possible to configure VCC3 to a different voltage, even higher than VCC1. An external resistor divider must be used, see below.

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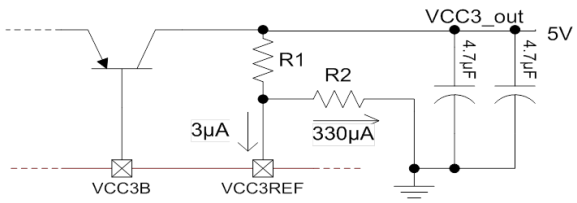
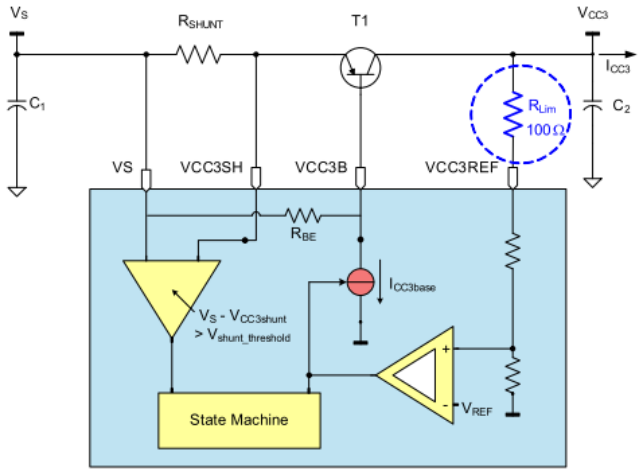
	 Input current on Vcc3_ref. Typical value form BE@ambient results $R1 = \frac{VCC3_{out} - VCC3_{ref}}{I_{R2} + I_{VCC3\_ref}} = \frac{5 - 3.3}{330E^{-6} + 3E^{-6}} = 5.11k\Omega$ The resulting 330uA is an optimum choice between circuit robustness and current consumption (see also next page) $R2 = \frac{VCC3_{ref}}{I_{R2}} = \frac{3.3}{330 \cdot E^{-6}} = 10K\Omega$
Question 15: **Chapter 8.2.1**	1. What is the function of R_{Lim}? 2. Does it affect Vcc3 output accuracy a lot?
Answer:	1. RLim is a simple solution to improve robustness of the VCC3 regulator and to protect the VCC3REF pin for short circuit events in case of off-board usage. 2. Assuming a VCC3REF input current of 10uA (P_8.6.2), a 100Ωhm resistor adds only 1mV offset. 
Question 16: **Chapter 8.2.2**	1. When we use VCC3 independently, it is possible to turn on and off VCC3? 2. Is it possible to turn ON and OFF VCC3 once configured for load sharing?
Answer:	1. In stand-alone configuration VCC3 can be turned on and off as needed (VCC3_ON). Once configured as stand-alone, the load sharing cannot be chosen anymore unless the SBC is powered down. 2. When load sharing is chosen (VCC3_LS_= 1), VCC3 can't be turned off by using the VCC3_ON register, because VCC3_ON register setting will be ignored. VCC3 status is always synchronized with VCC1 during load sharing. By default VCC3 is disabled in SBC Stop Mode and for VS < VS_UV. If needed, VCC3 can also stay activated in Stop Mode by setting the bit VCC3_LS_ STP_ON (with a slightly increased quiescent current) and below VS_UV by setting the bit VCC3_VS_ UV_OFF. *Note: Setting the bit VCC3_ON before setting the bit VCC3_LS prevents the load sharing configuration to be activated*

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Question 17: Chapter 8.3	Would you provide the information on the acceptable ESR values for the VCC3 output capacitor, as reference?
Answer:	It is recommended to use a ceramic capacitor with 10mΩ – 150mΩ. Below table is the recommendation for the external devices of VCC3.

Table 12 Bill of Materials for the V_{CC3} Function with and without load sharing configuration

Device	Vendor	Reference / Value
C2	Murata	10 µF/10 V GCM31CR71AA106K
RSHUNT	-	1 Ω (with LS) / 470 mΩ (without LS)
T1	ON Semiconductor	MJD253

Question 18: Chapter 8.4	Would you provide the information on the load sharing ratio in case of the Mid-Range SBC when the load sharing is used?
Answer:	The load sharing ratio can be selected via the shunt resistor (between VS and VCC3SH) by using the equation from the datasheet. A shunt resistor of 1Ω would result in a load sharing ratio of 1:1 (VCC3:VCC1).
Question 19: Chapter 8.4	1. How is the load-sharing function working? 2. How can I calculate the appropriate RSHUNT value?
Answer:	1. VCC1 circuit works as the main feedback loop to control the voltage (voltage controlled voltage source). The shunt resistor determines the load sharing ratio between VCC1 and VCC3. In other words, the VCC3 circuit work as the additional current supply (current controlled current source) and it is similar to a current mirror function. 2. Based on above (i), following calculation approach and method is proposed to determine the proper RSHUNT value: (i) Take the total current needed and determine the Icc1 value (e.g. based on your power dissipation estimation) (ii) Calculate the Icc3 value based on Step 1. (iii) RSHUNT is calculated by using following equation: $$R_{SHUNT} = \frac{I_{CC\ 1} \cdot 110\ \Omega\ /105\ - 15\ mV}{I_{CC\ 3}}$$
Question 20: Chapter 8.6	Would you provide the information on the output voltage accuracy when operating in load sharing?
Answer:	It is ±2% from the nominal value (5V or 3.3V) in SBC Normal Mode and ±4% in SBC Stop Mode (P_8.6.13).
Question 21: Chapter 8.6.6	Why does the datasheet state “up to 400mA with 470mΩ shunt resistor”? Regarding the 400mA, does it come from Vshunt_threshold 180mV min?
Answer:	Yes, it is based on the min shunt threshold voltage of 180mV. When using a 470mΩ shunt then the VCC3 current is ~382mA. It is also a practical achievable max. value. In theory the VCC3 current is limited by the max. base current and the power dissipation within the SBC and the PNP.
Question 22: Chapter 10.1	What is the internal link between the CAN transceiver and VCC2?
Answer:	The CAN transceiver and VCC2 are independent. CAN is supplied by the dedicated VCAN supply input pin, but any 5V supply could be used (e.g. for the 5V variant from VCC1, VCC2, VCC3 or an external voltage regulator).

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Question 23: **Chapter 10.1**	Can we disable VCC2 in SBC Stop Mode while keeping the CAN transceiver in wake capable mode?
Answer:	An internal supply derived from VS is active during CAN wake capable to supply the wake receiver. Therefore, VCC2 does not need to be active during SBC Stop or Sleep, i.e. it can be switched off during CAN wake capable mode.
Question 24: **Chapter 10.2.4**	How can the microcontroller detect a wake-up on CAN in SBC Stop Mode?
Answer:	There are two signalizations how a CAN wake-up is detected: 1. The INT pin is pulled low for t_{INT}. 2. RXDCAN is pulled low until the CAN mode is changed via SPI. The microcontroller can use either signal as wake-up detection. Please refer to the datasheet Chapter 10.2.4 “CAN wake Capable Mode” for the details. The same applies for a wake-up on LIN but with a signalization on RXDLIN
Question 25: **Chapter 11.1**	Which pin is the power supply for the integrated LIN module?
Answer:	It is supplied via VSHS pin. Please refer to the block diagram in Chapter 11.1.
Question 26: **Chapter 11.3**	What is the LIN dominant voltage level?
Answer:	TLE926x specifications are based on LIN2.2A standard. Therefore it is NOT described as voltage level but it is described as the duty cycle.

Duty Cycle D2 (for worst case at 20 kbit/s) LIN 2.2 Normal Slope	D2	–	–	0.581		[3)] $TH_{Rec}(min.) = 0.422 \times V_{SHS}$; $TH_{Dom}(min.) = 0.284 \times V_{SHS}$; $V_{SHS} = 7.6 \ldots 18$ V; $t_{bit} = 50$ µs; $D2 = t_{bus\_rec(max)}/2\ t_{bit}$; LIN 2.2 Param 28	P_11.3.32
Duty Cycle D4 (for worst case at 10.4 kbit/s) SAE J2602 Low Slope	D4	–	–	0.590		[3)] THRec(min.) = 0.389 × V_{SHS}; THDom(min.) = 0.251 × V_{SHS}; $V_{SHS} = 7.6 \ldots 18$ V; $t_{bit} = 96$ µs; $D4 = t_{bus\_rec(max)}/2\ t_{bit}$; LIN 2.2 Param 30	P_11.3.34

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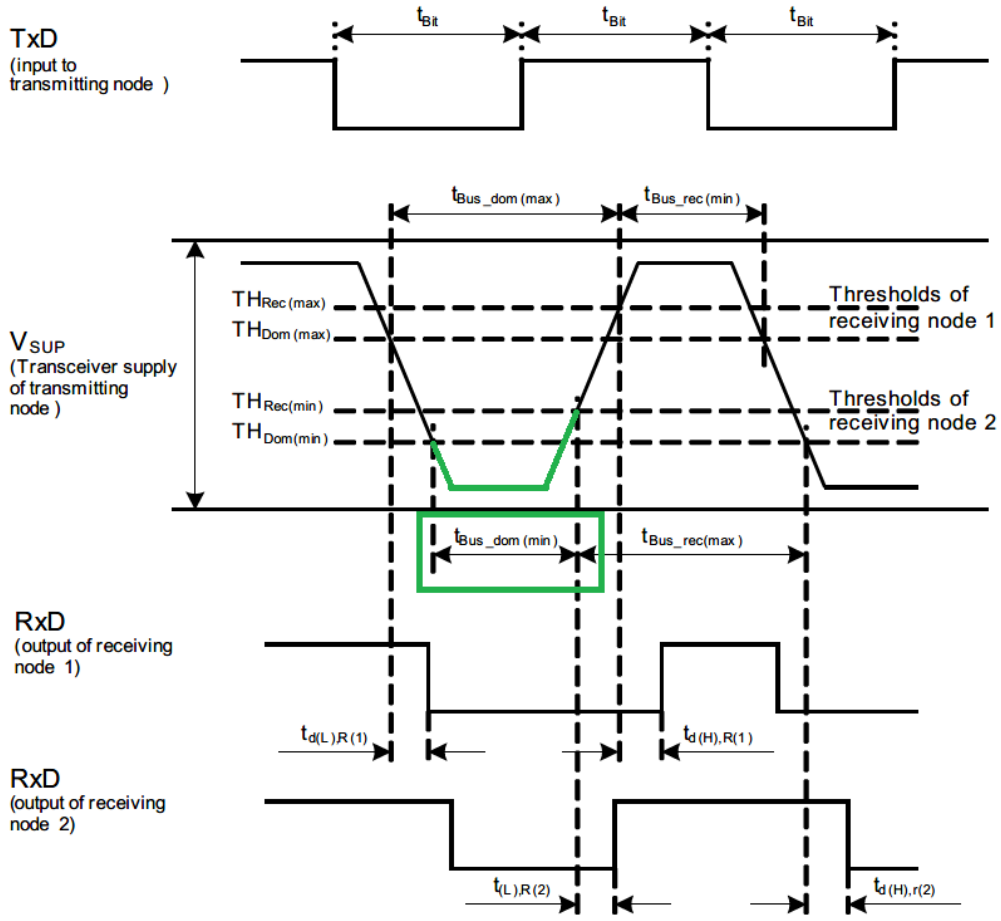

Question 27: **Chapter 12.3**	1. What max. voltage can be applied to the WKx pins and how large is the current flowing into the pin? 2. Must the current be limited if a pin voltage of >40V is applied?
Answer:	1. The maximum voltage on WKx pins can be 40V (P_4.1.6). As long as the voltage doesn't exceed VS+0.3V, the current is as specified (P_12.3.4). 2. In general, voltages of >40V are not allowed because of the break through voltage of the ESD diode. ESD diodes can withstand a high (>1mA) current only for a very short period. In case the pin is connected to outside the control unit, the protection of ESD / ISO pulses is necessary. An external capacitor of 10nF and a 10k series resistor are suitable to limit the pulse current into the pin. *Note: The 500µA maximum rating of (P_4.1.13 and (P_4.1.14) apply for the case when the HV measurement function between WK1 and WK2 is enabled (Chapter 12.2.2) and the current between the two pins must be limited*.
Question 28: **Chapter 14.1**	1. Is there an internal pull-up resistor on FO3 /TEST pin? 2. Do we need to add an external pull-up for the productive application?
Answer:	1. Yes, there is an internal pull-up resistor (R_{TEST}) implemented in the FO3/TEST pin, which is activated only during the power-up phase of the SBC. It is used to detect, whether the SBC Development Mode shall be activated or not. The SBC Software Development Mode is entered, if the FO3/TEST pin is set and kept LOW during SBC Init Mode. The voltage level monitoring is started as soon as VS > $V_{POR,r}$. The SBC Development Mode is configured and maintained, if the SBC Init Mode is left by sending any SPI command while FO3/TEST is LOW. The Software Development Mode is NOT configured, if the FO3/TEST level is HIGH for longer than t_{TEST} during the monitoring period. 2. After the power-up phase the internal pull-up resistor is disabled and the pin provides an

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	open drain output. The external pull-up may be required depending on the used functionality. *Note: FO2 and FO3/TEST can also be reconfigured after power-up as a low-side, high-side or wake-input functionality. The configuration is performed in the register GPIO_CTRL.*
Question 29: **Chapter 15.6**	Do VCC1, VCC2 and VCC3 have an under-voltage detection feature?
Answer:	• VCC1: a pre-warning detection (P_15.6.1), a configurable under-voltage reset (P_15.6.1), a short circuit detection (Chapter 15.7), and an over voltage detection (P_15.6.2) are implemented • VCC2: an under-voltage detection is implemented (P_15.8). An SPI bit will be set but no reset is generated • VCC3: an under-voltage detection is implemented (P_15.7) depending on the configured voltage. An SPI bit will be set but no reset is generated Please refer to the datasheet Section 15.6 – 15.8 for further information
Question 230: **Chapter 15.9.1**	What happens to VCC1, if VCC2 enters thermal shutdown and is turned off?
Answer:	There are independent temperature's sensors on each voltage regulator and also for the other power stages. Therefore VCC1 will continue to operate independently from the VCC2 condition as long as the temperature is below the thermal shutdown threshold for VCC1..
Question 31: **Chapter 15.10**	Would you provide the information on the VS min voltage to release reset (RO is L to H) surely during VS ramp-up?
Answer:	It is 5.45V based on following calculation. (Vrt1,f) + (Vrt, hys) + (Vcc1, d2) = 4.75Vmax + 0.2Vmax + 0.5Vmax = 5.45Vmax
Question 32: **Chapter 15.10.18**	How long is the reset pulse width for the WD time-out?
Answer:	The reset delay time (t_{RD1}) is typ. 2ms typ. In case of a watchdog trigger reset the RO pin is pulled low for this time. For other events, e.g. under voltage reset, the RO is pulled down for at least the 2ms but as long as VCC1 is below the reset threshold.
Question 33: **Chapter 16**	Are the SPI registers exactly the same among TLE926x(-3)BQX(V33) family? What happen in case of programming a register associated to a non-available function?
Answer:	All members of the MR-SBC family are fully software compatible between each other. The LIN2 (in the TLE9262, TLE9261 and TLE9260 variants), the LIN1 (in the TLE9261 and TLE9260 variants) and VCC3 (in TLE9260 variant) are disabled via internal hardwiring. The respective control bits behave like other reserved bits, i.e. they read as '0' and are also tied to '0'. No control or configuration is possible. No SPI_FAIL bit is set.
Question 34: **Chapter 16.2**	A reserved bit in configuration register has to be written as 0, will it trigger a raise of SPI_FAIL flag if programmed as 1?
Answer:	Nothing will happen, when trying to write a '1' to a reserved bit because there is no real digital registers for reserved bits, The read back value is always '0' for reserved bits. The SPI_FAIL flag is not set.. *Note: For the details of the invalid SPI Commands leading to SPI_FAIL, please refer to the datasheet Chapter 16.2.*
Question 35: **Chapter 16.7**	Are there any internal pull-ups or pull-downs at SPI pins?

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Answer:

- CSN pin: there is a pull-up resistor (40kΩ typ.)
- SDI and CLK pin: each pin has a pull down resistor (40kΩ typ.).
- SDO pin: there is no pull-up or pull-down resistor. It is a push-pull output stage.

Please refer to (P_16.7.6) and (P_16.7.7).

Question 36:
Chapter 16.7.23

What is the transition time for SBC mode changes triggered via SPI?

Answer:

The mode transition time is max. 6µs. Please refer to (P_16.7.23).

Question 37:
Chapter 3

Which pins have which internal structures?

Please see below table for each pin:

Pin	Symbol	Function
1	GND	**Ground**
2	n.c.	**not connected;** internally not bonded.
3	VCC3REF	**VCC3REF;** Collector connection for external PNP, reference input
4	VCC3B	**VCC3B;** Base connection for external PNP
5	VCC3SH	**VCC3SH;** Emitter connection for external PNP, shunt connection
6	n.c.	**not connected;** internally not bonded.
7	n.c.	**not connected;** internally not bonded.
8	HS1	**High Side Output 1;** typ. 7Ω
9	HS2	**High Side Output 2;** typ. 7Ω
10	HS3	**High Side Output 3;** typ. 7Ω
11	HS4	**High Side Output 4;** typ. 7Ω
12	n.c	**not connected;** internally not bonded.
13	VSHS	**Supply Voltage HS, LIN and GPIO1/2 in HS configuration; Supply voltage for High-Side Switches and LIN modules and respective UV-/OV supervision; Connected to battery voltage with reverse protection diode and filter against EMC**; connect to VS if separate supply is not needed
14	VS	**Supply Voltage; Supply voltage for chip internal supply and voltage regulators; Connected to Battery Voltage with external reverse protection Diode and Filter against EMC**
15	VS	**Supply Voltage; Supply voltage for chip internal supply and voltage regulators; Connected to Battery Voltage with external reverse protection Diode and Filter against EMC**
16	n.c.	**not connected;** internally not bonded.
17	VCC1	**Voltage Regulator Output 1**
18	VCC2	**Voltage Regulator Output 2**
19	n.c.	**not connected;** internally not bonded.
20	GND	**GND**
21	FO1	**Fail Output 1**
22	WK1	**Wake Input 1;** Alternative function: HV-measurement function input pin (only in combination with WK2, see Chapter 12.2.2)
23	WK2	**Wake Input 2;** Alternative function: HV-measurement function output pin (only in combination with WK1, see Chapter 12.2.2)
24	WK3	**Wake Input 3**
25	TXDLIN2	**Transmit LIN2**
26	RXDLIN2	**Receive LIN2**
27	CLK	**SPI Clock Input**
28	SDI	**SPI Data Input; into SBC (=MOSI)**
29	SDO	**SPI Data Output;** out of SBC (=MISO)

Pin	Symbol	Function
30	CSN	**SPI Chip Select Not Input**
31	INT	**Interrupt Output**; used as wake-up flag for microcontroller in SBC Stop or Normal Mode and for indicating failures. Active low. During start-up used to set the SBC configuration. External pull-up sets config 1/3, no external pull-up sets config 2/4.
32	RO	**Reset Output**
33	TXDLIN1	**Transmit LIN1**
34	RXDLIN1	**Receive LIN1**
35	TXDCAN	**Transmit CAN**; alternate function: calibration of high-precision oscillator
36	RXDCAN	**Receive CAN**
37	VCAN	**Supply Input; for internal HS-CAN cell**
38	GND	**GND**
39	CANL	**CAN Low Bus Pin**
40	CANH	**CAN High Bus Pin**
41	n.c.	**not connected;** internally not bonded.
42	LIN1	**LIN1 Bus;** Bus line for the LIN interface, according to ISO. 9141 and LIN specification 2.2 as well as SAE J2602-2.
43	GND	**Ground**
44	LIN2	**LIN2 Bus;** Bus line for the LIN interface, according to ISO. 9141 and LIN specification 2.2 as well as SAE J2602-2.
45	n.c.	**not connected;** internally not bonded.
46	n.c.	**not connected;** internally not bonded.
47	FO2	**Fail Output 2** - Side indicator; Side indicators 1.25Hz 50% duty cycle output; Open drain. Active LOW. **Alternative Function: GPIO1**; configurable pin as WK, or LS, or HS supplied by VSHS (default is FO2, see also Chapter 14.1.1)
48	FO3/TEST	**Fail Output 3** - Pulsed Light Output; Break/rear light 100Hz 20% duty cycle output; Open drain. Active LOW **TEST**; Connect to GND to activate SBC Development Mode; Integrated pull-up resistor. Connect to VS with pull-up resistor or leave open for normal operation. **Alternative Function: GPIO2**; configurable pin as WK, or LS, or HS supplied by VSHS (default is FO3, see also Chapter 14.1.1)
Cooling Tab	GND	Cooling Tab - Exposed Die Pad; For cooling purposes only, do not use as an electrical ground.[1]

1) The exposed die pad at the bottom of the package allows better power dissipation of heat from the SBC via the PCB. The exposed die pad is not connected to any active part of the IC an can be left floating or it can be connected to GND (recommended) for the best EMC performance.