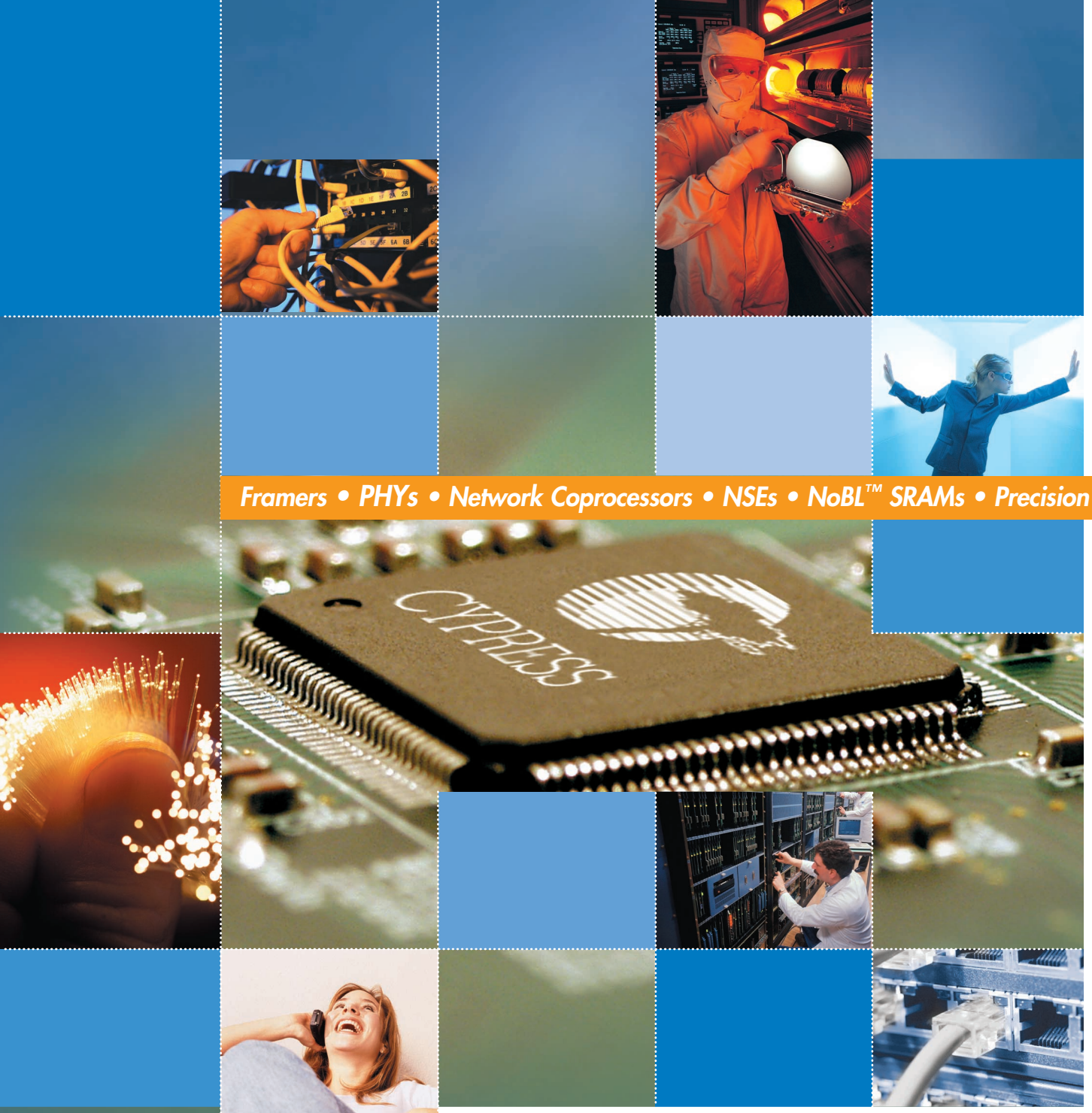


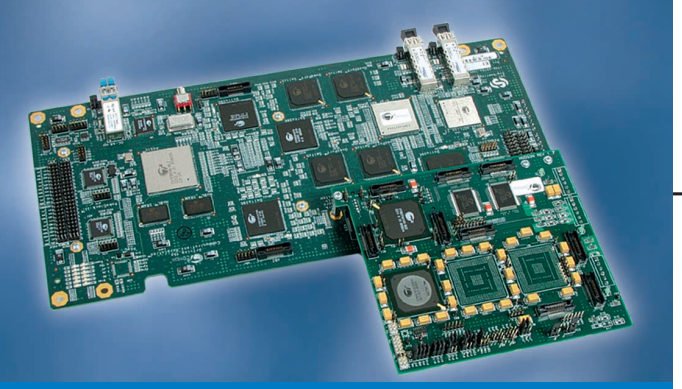
Wirespeed Communication Solutions

Framers • PHYs • Network Coprocessors • NSEs • NoBL™ SRAMs • Precision Clocks • QuadPort™ DSEs • Specialty Memories

PERSONAL ACCESS ENTERPRISE METRO CORE

CYPRESS

Connecting From Last Mile to First Mile.™



Data Over SONET/SDH

Communications systems continue to revolutionize the way we conduct our lives, both personally and professionally. With the continued growth of the Internet, specialized silicon-based solutions are necessary to provide reliable, state-of-the-art network infrastructure equipment.

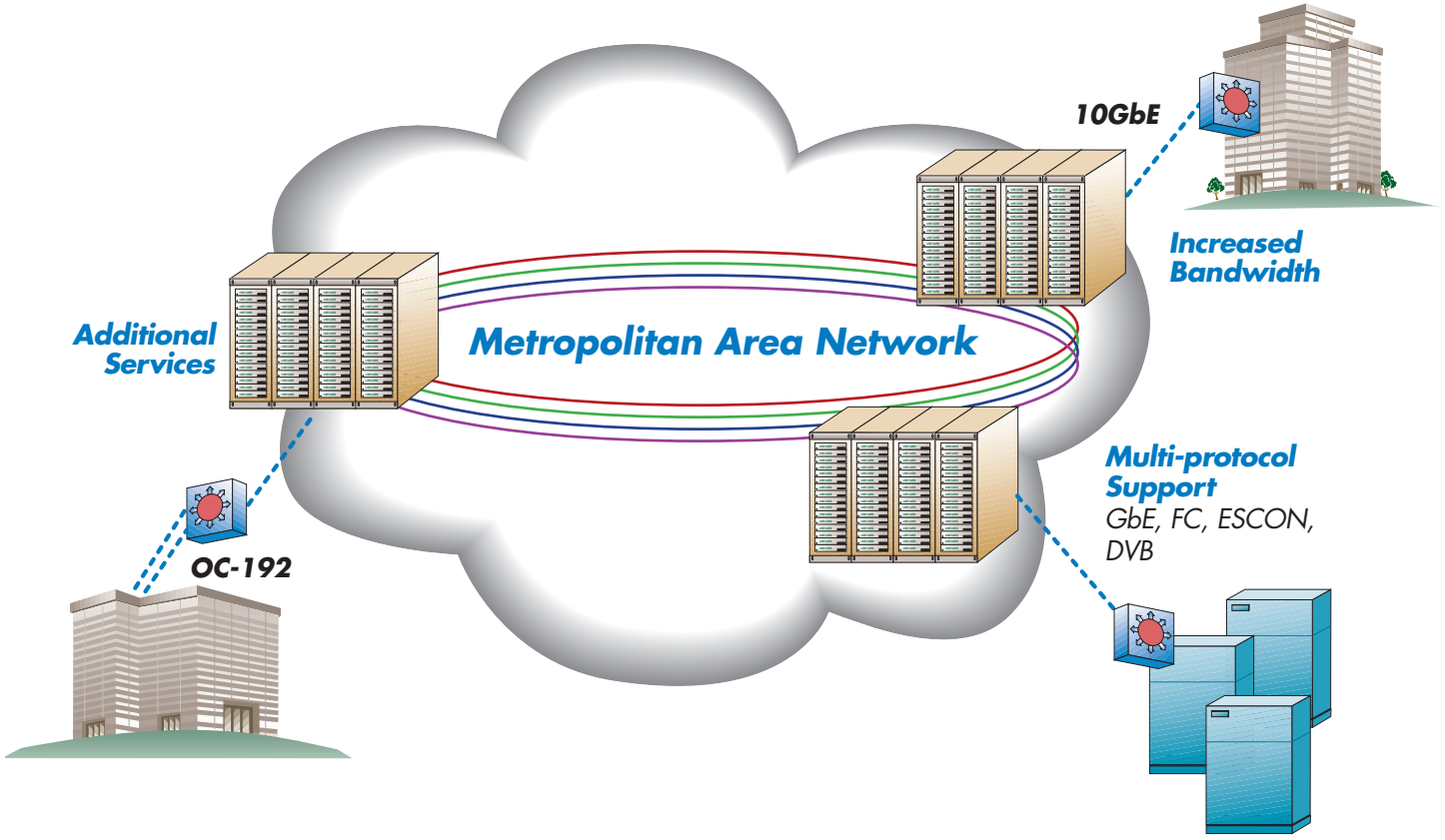
To address the increasing complexity and bandwidth requirements of these communications systems, Cypress offers a comprehensive portfolio of high-performance solutions.

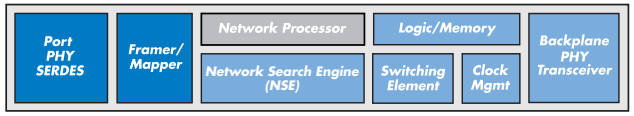
Cypress's broad product portfolio offers wirespeed solutions across the entire linecard. Port PHYs and framers optimize high-speed transmissions over SONET/SDH; Network Search Engines (NSEs) and coprocessors enable high-performance packet processing; and flexible PHY and backplane management solutions continue to drive high-performance serial backplanes.

Cypress solutions are instrumental in enabling datapath connections from last mile to first mile.

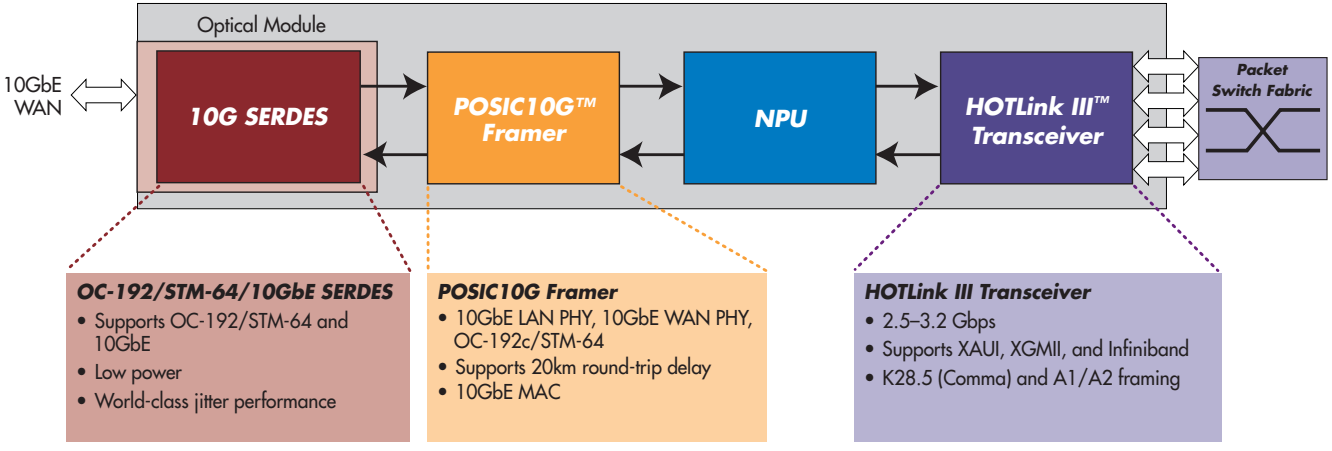
Enabling the Next-Generation Metropolitan Area Network

The demand for bandwidth, types of new services, and number of new network users all continue to grow. There is growth in new data and telecom services such as remote storage, video conferencing, video training, and voice over IP. Coupled with consistent growth in bandwidth and users, these services place increasing demands on carriers and ISPs attempting to build a robust Metropolitan Area Network. The need to transport multiple services over existing SONET infrastructure requires the type of flexibility and efficiency only Cypress's multi-protocol based solutions can offer. Cypress enables system vendors to meet their market demands by providing complete 10 Gbps solutions. Along with state-of-the-art physical layer devices, Cypress offers world-class transport solutions.





Increased Bandwidth: OC-192/STM-64/10GbE Linecard

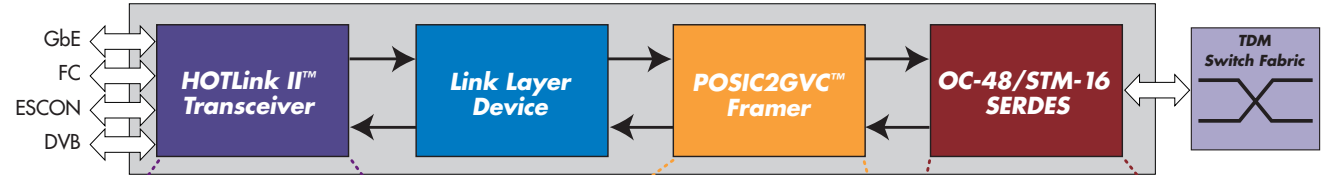


OC-192/STM-64/10GbE SERDES
- Supports OC-192/STM-64 and 10GbE
- Low power
- World-class jitter performance

POSIC10G Framer
- 10GbE LAN PHY, 10GbE WAN PHY, OC-192c/STM-64
- Supports 20km round-trip delay
- 10GbE MAC

HOTLink III Transceiver
- 2.5–3.2 Gbps
- Supports XAUI, XGMII, and Infiniband
- K28.5 (Comma) and A1/A2 framing

Multi-protocol Support: Multi-protocol OC-48/STM-16 Linecard



HOTLink II Transceiver
- 200Mbps–1.5 Gbps data rate
- Independent channels support multiple protocols
- Programmable version with 100K logic gates available

POSIC2GVC Framer
- Virtual concatenation (VC) allows efficient transport of multiple protocols over SONET
- GFP & HDLC allow flexible mapping of data
- 16 VC channels programmable in increments of STS-1

OC-48/STM-16 SERDES
- Smallest, lowest-power 16-bit OC-48/STM-16 SERDES
- Seamless interface to POSIC2GVC and POSIC2G™ framers
- Full Telcordia/ITU-T jitter compliance

POSIC™ Framer Family

Version	Part #	Standards	Features
10GVC	CY7C9546	Quad OC-48,OC-192 STM-64,10GbE	VC, POS/GFP
10G	CY7C9547	OC-192c/STM-64, 10GbE	POS
10GLAN	CY7C9548	10GbE	LAN PHY
2GVC	CY7C9536	OC-48/STM-16, Quad OC-12, 16xOC-3	VC, POS/GFP/ ATM
2G	CY7C9537	OC-48/STM-16 Quad OC-12, 16xOC-3	POS/GFP/ATM

WAN SERDES Family

Data Rate (Gbps)	Part #	Standards	Parallel Interface
9.9–10.7	CYS100G01xxDX	OC-192/STM-64	16-bit LVDS SFI4.1, XSBI
2.5	CYS25G0102DX	OC-48/STM-16	16-bit, HSTL LVPECL
2.5	CYS25G0101DX	OC-48/STM-16	16-bit, HSTL LVPECL
2.5	CYS25G01K100	OC-48/STM-16	Prog. I/Os

HOTLink® LAN/SAN PHY Family

Data Rate (Gbps)	Part #	Standards	# of Channels
9.9–10.7	CYP100G01xxDX	10GbE, 10xFC	1
1.0–3.4	CYP34G04xxDX	XAUI, 1-2xFC, GbE, Infiniband	4
2.5–3.2	CYP32G04xxDX	XAUI, Infiniband	4
0.2–1.5	CYP15GxxxxDX	ESCON, GbE, 1xFC	1, 2, 4
0.2–1.5	CY15G04K100	ESCON, GbE, 1xFC	4

Solving the Search Problem

Wirespeed Packet Processing

As Internet usage, line rates and traffic complexity increase, transmission bottlenecks are emerging, particularly in the packet processing section of the networking linecard. From the core to the edge, simple packet processing no longer provides a universal solution. Increasingly, designers require deep-packet processing solutions capable of resolving challenging, policy-oriented Class of Service (CoS) and Quality of Service (QoS) issues. They are moving away from simple, software-based solutions in favor of intelligent search architectures customized to address the requirements of specific applications. In short, a packet processing revolution is underway. Cypress is driving that revolution.

Leading the way are new generations of network search engines (NSEs) and network coprocessors compatible with industry leading NPUs and ASICs. Cypress is committed to developing high-performance, large-entry search solutions that enable packet forwarding, policy resolution, and netflow tracking. Cypress's portfolio of deterministic, deep-packet and algorithmic solutions meet the needs of next-generation system designers and set the standard for packet processing innovation.

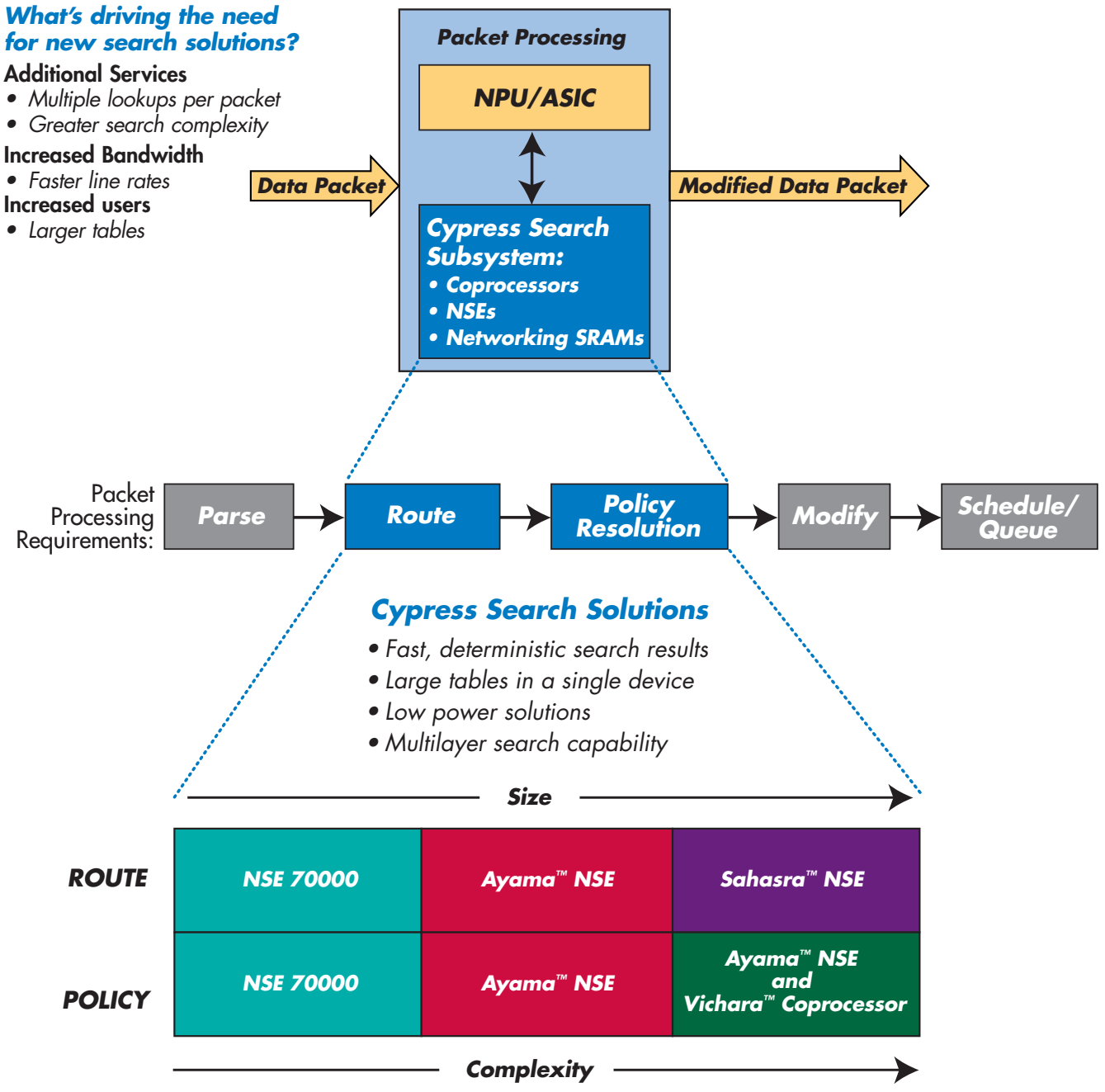
Cypress Search Families

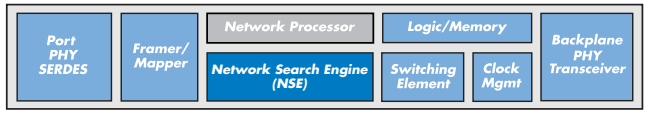
Cypress's NSE family names are based on the ancient language of Sanskrit.

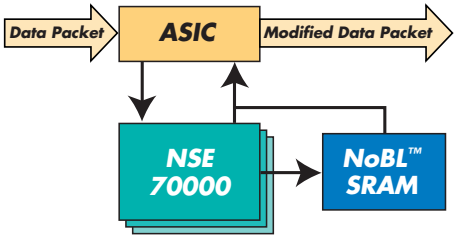
Ayama™ NSE—"Extension". The Ayama family extends the performance, density, power management, and table management of Cypress's market leading NSE 70000 family.

Sahasra™ NSE—"Thousands" or "Infinite". Sahasra provides the largest number of entries, nearly an infinite number, to support very large forwarding tables.

Vichara™ Network Coprocessor—"Continued Thought". Vichara provides additional intelligence to perform complex, deep-packet searches.

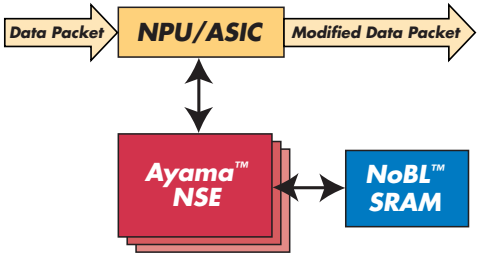






NSE 70000 Family

- *Broad line of densities (32K, 64K, 128K, 256K IPv4 entries)*
- *Performance up to 100 million searches per second (MSPS)*
- *Full-bit ternary masking*
- *Footprint-compatible with the Ayama 10000 NSEs*
- *Cascade up to 31 devices*



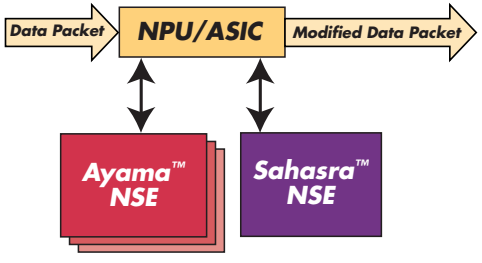
Ayama Family

Ayama 10000

- *Densities of 128K, 256K and 512K IPv4 entries*
- *Highest performance at 266 MSPS*
- *Lowest power with unique Mini-Key™ power management feature*
- *Configurable table widths within a single device (x36/72/144/288/576)*
- *Parity to detect errors in the NSE core and across the data bus*

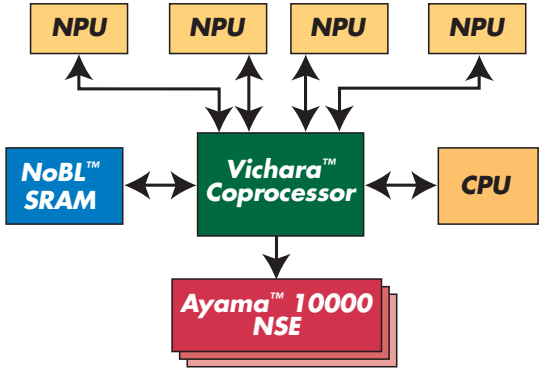
Ayama 20000

- *Glueless interface to IBM, Intel, AMCC, and all processors with LA-1 and XSC interfaces*
- *Interface up to 4 NPUs to a single Ayama 20000 device*
- *Parity error detection, Soft Priority™, and Mini-Key features*



Sahasra Forwarding NSE

- *Supports searches with density >1 million entries*
- *Deterministic results*
- *Unique high-performance, low power search solution*
- *Larger tables through cascading*
- *Lowest power per route*
- *Advanced software suite*



Vichara Coprocessor

- *Manages multiple searches for the NPU eliminating bus bottlenecks*
- *Interface up to 4 NPUs to a single Vichara 81000*
- *Search key extraction and support for conditional branching operations*
- *Aging, policing, and flow statistics*
- *Glueless interface to IBM, Intel, AMCC, and all processors with LA-1 and XSC interfaces*

NSE 70000 Family

Part #	IPv4 Entries	Density	Performance
CYNSE70032	32K	1 Mbit	83 MSPS
CYNSE70064	64K	2 Mbits	83 MSPS
CYNSE70128	128K	4 Mbits	100 MSPS
CYNSE70256	256K	9 Mbits	83 MSPS

Ayama™ 10000 Family

Part #	IPv4 Entries	Density	Performance
CYNSE10128	128K	4 Mbits	266 MSPS
CYNSE10256	256K	9 Mbits	266 MSPS
CYNSE10512	512K	18 Mbits	266 MSPS

Ayama™ 20000 Family

Part #	IPv4 Entries	Density	Performance
CYNSE20128	128K	4 Mbits	266 MSPS
CYNSE20256	256K	9 Mbits	266 MSPS
CYNSE20512	512K	18 Mbits	266 MSPS

Sahasra™ 50000

Part #	IPv4 Entries	Performance
CYNSE50000	> 1M	> 200 MSPS

Vichara™ 81000

Part #	NPU Interface	Features
CYNCP81000	4 LA-1; 4 XSC	Recursive Search, Conditional Branch Operations, Aging, Policing, and Flow Statistics

Cypress Backplane Solutions—The Ultimate in Flexibility

Backplanes Made Easy

Backplane designers can count on two things: increasing port speed and increasing port density. Both of these require more data throughput and higher performance in the backplane. More and more backplane designs are taking advantage of low-noise, scalable serial links to enable high-performance backplanes. As a pioneer in serial backplanes, Cypress has continued to be an innovation leader.

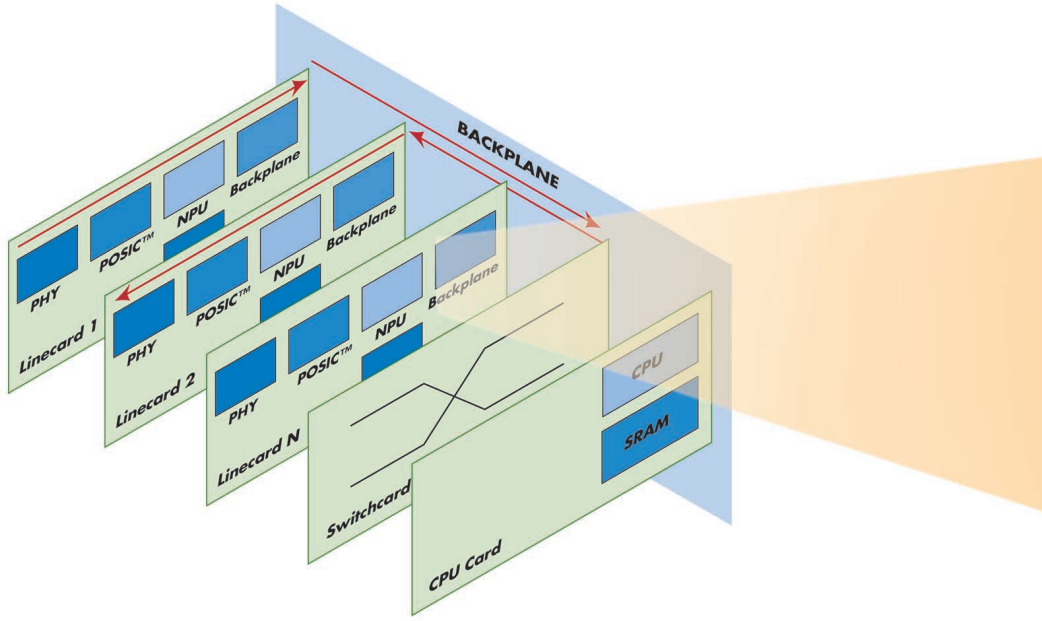
Today, Cypress's flexible physical layer and backplane management solutions mean designing serial backplanes has never been easier. Each Cypress family offers unparalled flexibility. Whether it is over 3 Gbps of frequency agility in the HOTLink® family, programmable skew timing in the RoboClock® family, high-performance programmable logic in the Delta 39K™ CPLDs, or data buffering flexibility in the QuadPort Datapath Switching Element (QuadPort™ DSE) device, Cypress has the backplane solution.

HOTLink® Backplane Family

Data Rate (Gbps)	Part #	Features	# of Channels
1.0–3.4	CYP34G04xxDX	<100mW/channel B1 Monitoring	4
2.5–3.2	CYP32G04xxDX	8b/10B Encoding A1/A1 Framing	4
0.2–1.5	CYP15GxxxxDX	8b/10B Encoding Channel Bonding	1, 2, 4
0.2–1.5	CYP15G04K100	Programmable	4

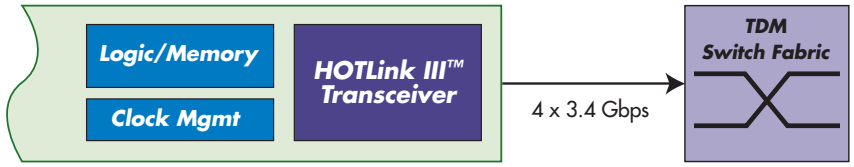
What do next generation backplanes require?

- *Increased bandwidth*
- *Scalability*
- *Frequency agility*
- *Innovative managment*



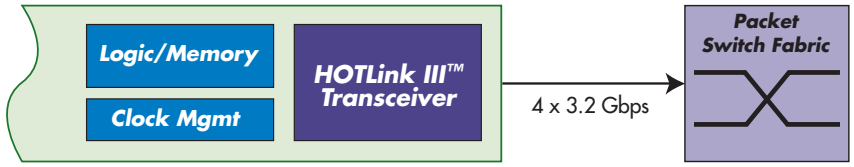
1.0–3.4 Gbps SONET Backplane

- *Ultra-low power (<100 mW per channel)*
- *A1/A2 framing, B1 monitoring*
- *Programmable pre-emphasis*
- *Programmable output levels*



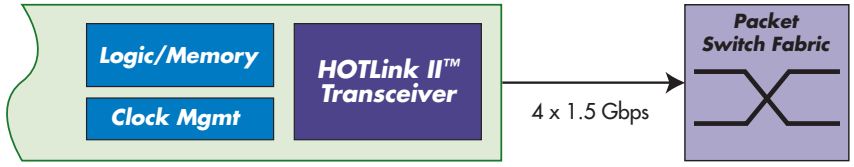
2.5–3.2 Gbps Backplane

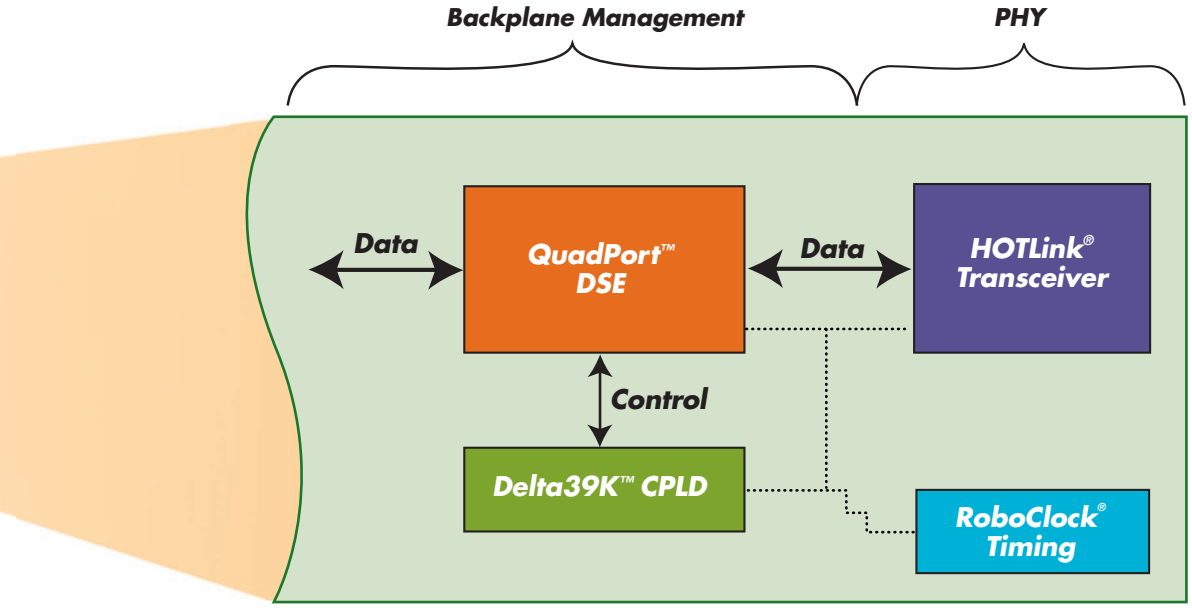
- *Frequency Agile*
- *XAUI compatible*
- *8B/10B bypassable encoding*
- *K28.5, and A1/A2 framing*



200 Mbps–1.5 Gbps Backplane

- *Multichannel bonding*
- *Frequency independent channels*
- *100K gates of logic*
- *8B/10B bypassable encoding*





Memory Solutions

Cypress supports a full portfolio of memory solutions, offering a broad selection of performance, features, and design flexibility.

QuadPort™ DSE
- *Allows innovative system design*
- *Densities up to 5 Mbits*
- *4 ports up to 167MHz*

Dual-Port RAMs
- *Densities up to 9 Mbits*
- *Speeds up to 167MHz*
- *Supports burst counters*

FIFOs
- *Densities up to 5 Mbits*
- *Speeds up to 200MHz*
- *Bus matching for flexibility*

Flexible Timing

Broadest portfolio of high-performance clock distribution products.

RoboClock® Timing
- *Programmable output skew per bank*
- *Programmable divide/multiply per bank*
- *18 outputs up to 200MHz*

ComLink™ Buffers
- *Differential to LVPECL/LVDS buffers*
- *Up to 650MHz single-ended outputs*
- *Up to 350MHz differential outputs*

Zero Delay, Non-ZDB Buffers
- *Split 2.5V/3.3V outputs*
- *Up to 21 outputs at 200MHz*
- *Motorola alternate solutions*

Programmable Logic

Cypress has the highest-density CPLDs, up to 200K gates of logic.

Delta39K™ CPLDs
- *Up to 200K gates*
- *Most integrated memory*
- *Highest number of I/Os*
- *Self-boot support*
- *Deterministic timing*

Quantum38K™ CPLDs
- *Easy migration to Delta39K*
- *Up to 100K gates*
- *Pin-compatible footprints*

Ultra37000™ CPLDs
- *Speeds up to 200MHz*
- *In-System Reprogrammable™ (ISR™)*

QuadPort™ DSE Family

Part #	Density	Config.	Freq.	Packages
CY7C0452	5 Mbits	128K x 40	167	676 BGA (27 x 27)
CY7C0451	2 Mbits	64K x 40	167	676 BGA (27 x 27)
CY7C0431	2 Mbits	128K x 20	167	676 BGA (27 x 27)
CY7C0430	1 Mbit	64K x 18	133	272 BGA (27 x 27)
CY7C04312	1/2 Mbit	32K x 18	133	272 BGA (27 x 27)
CY7C04314	1/4 Mbit	16K x 18	133	272 BGA (27 x 27)

Dual-Port Family

Part #	Density	Config.	Freq.	Packages
CY7C0853	9 Mbits	256K x 36	150	172 BGA (15 x 15)
CY7C0852	4 Mbits	128K x 36	167	172 BGA (15 x 15) 176 TQFP (24 x 24)
CY7C0851	2 Mbits	64K x 36	167	172 TQFP (15 x 15) 176 TQFP (24 x 24)
CY7C0832	4 Mbits	256K x 18	167	120 TQFP (14 x 14)
CY7C0831	2 Mbits	128K x 18	167	120 TQFP (14 x 14)

FIFO Family

Part #	Density	Config.	Freq.	Packages
CY7C4808	5 Mbits	64K x 80	200	288 BGA (19 x 19)
CY7C4806	1 Mbit	16K x 80	200	288 BGA (19 x 19)
CY7C43684	1 Mbit	16K x 36 x2	133	128 TQFP (14 x 20)
CY7C43683	1/2 Mbit	16K x 36	133	128 TQFP (14 x 20)

Delta39K™ Family

Device	Typ. Gates	Macro	RAM (Kb)	f_{MAX2} (MHz)
39K200	92K–288K	3072	480	181
39K165	77K–241K	2560	400	181
39K100	46K–144K	1536	240	222
39K50	23K–72K	768	120	233
39K30	16K–48K	512	80	233

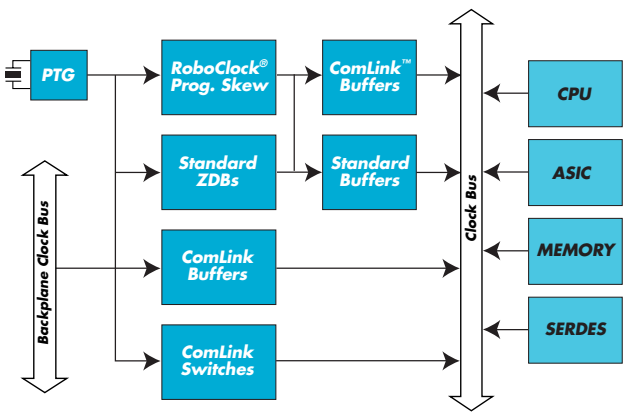
Quantum38K™ Family

Device	Typ. Gates	Macro	RAM (Kb)	f_{MAX2} (MHz)
38K100	46K–144K	1536	48	125
38K50	23K–72K	768	24	125
38K30	16K–48K	512	16	125

Timing Solutions

Cypress offers the largest portfolio of clock distribution solutions including Zero Delay Buffers (ZDBs); high-performance, non-zero-delay buffers; and RoboClock® programmable skew buffers. RoboClock skew buffers provide the flexibility and reliability needed in complex communications systems through programmability and redundancy. In addition, the ComLink™ family includes multiplexed, differential line drivers that provide redundant links for serial backplanes, three-state buffers, and clock distribution.

Typical Backplane Timing Distribution



ComLink™ Family

Part #	Outputs	Freq.	Output	Voltage
CY2CC910	10	650MHz	LVCMOS	1.8V
CY2DP814/8	4/8	350MHz	LVPECL	3.3V
CY2DL814/8	4/8	350MHz	LVDS	3.3V
CY2LL8422/23	4	350MHz	LVDS	3.3V
CY23020-1	20	200MHz	LVCMOS	2.5V, 3.3V

RoboClock® Family

Part #	Outputs	Freq.	Output	Voltage
CY7B9945V	10	200MHz	LVCMOS	3.3V
CY7B994V	18	200MHz	LVCMOS	3.3V
CY7B995	8	200MHz	LVCMOS	2.5
CY7B9950	8	200MHz	LVCMOS	2.5

SRAM Solutions

NoBL™ (No Bus Latency™) synchronous SRAMs optimize the most demanding high-speed applications requiring maximum bandwidth by eliminating latency when transitioning between read and write operations.

72-Mbit NoBL SRAM

Part #	Config.	Power	I/Os	Frequencies
CY7C1470V33	2M x 36	3.3V	3.3V, 2.5V	250, 200, 167
CY7C1470V25	2M x 36	2.5V	2.5V	250, 200, 167
CY7C1472V33	4M x 18	3.3V	3.3V, 2.5V	250, 200, 167
CY7C1472V25	4M x 18	2.5V	2.5V	250, 200, 167
CY7C1474V25	1M x 72	2.5V	2.5V	250, 200, 167

36-Mbit NoBL SRAM

Part #	Config.	Power	I/Os	Frequencies
CY7C1460	1M x 36	3.3V	3.3V, 2.5V	250, 200, 167
CY7C1460V25	1M x 36	2.5V	2.5V	250, 200, 167
CY7C1462	2M x 18	3.3V	3.3V, 2.5V	250, 200, 167
CY7C1462V25	2M x 18	2.5V	2.5V	250, 200, 167
CY7C1464V25	512K x 72	2.5V	2.5V	250, 200, 167

18-Mbit NoBL SRAM

Part #	Config.	Power	I/Os	Frequencies
CY7C1370B/C	512K x 36	3.3V	3.3V, 2.5V	250, 200, 167
CY7C1370B/CV25	512K x 36	2.5V	2.5V	250, 200, 167
CY7C1372B/C	1M x 18	3.3V	3.3V, 2.5V	250, 200, 167
CY7C1372B/CV25	1M x 18	2.5V	2.5V	250, 200, 167

9-Mbit NoBL SRAM

Part #	Config.	Power	I/Os	Frequencies
CCY7C1354A/B	256K x 36	3.3V	3.3V, 2.5V	250, 200, 167, 133
CY7C1354/BV25	256K x 36	2.5V	2.5V	250, 200, 167, 133
CY7C1356A/B	512K x 18	3.3V	3.3V, 2.5V	250, 200, 167, 133
CY7C1356/BV25	512K x 18	2.5V	2.5V	250, 200, 167, 133

4-Mbit NoBL SRAM

Part #	Config.	Power	I/Os	Frequencies
CY7C1350B/C	128K x 36	3.3V	3.3V	143, 133, 100
CY7C1352B/C	256K x 18	3.3V	3.3V	143, 133, 100

Connecting From Last Mile to First Mile.™

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Connecting From Last Mile To First Mile.™

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