

SONET OC-48 Transceiver

Features

- SONET OC-48 operation
- Bellcore and ITU jitter compliance
- 2.488-GBaud serial signaling rate
- Multiple selectable loopback/loop-through modes
- Single 155.52-MHz reference clock
- Transmit FIFO for flexible data interface clocking
- 16-bit parallel-to-serial conversion in transmit path
- Serial-to-16-bit parallel conversion in receive path
- Synchronous parallel interface
 - LVPECL-compliant
 - HSTL-compliant
- Internal transmit and receive phase-locked loops (PLLs)
- Differential CML serial input
 - 50-mV input sensitivity
 - 100Ω Internal termination and DC-restoration
- Differential CML serial output
 - Source matched for 50Ω transmission lines (100Ω differential transmission lines)
- Direct interface to standard fiber-optic modules
- Less than 1.0W typical power
- 120-pin 14 mm × 14 mm TQFP
- Standby power-saving mode for inactive loops
- 0.25μ BiCMOS technology

Functional Description

The CYS25G0101DX SONET OC-48 Transceiver is a communications building block for high-speed SONET data communications. It provides complete parallel-to-serial and serial-to-parallel conversion, clock generation, and clock and

data recovery operations in a single chip, optimized for full SONET compliance.

Transmit Path

New data is accepted at the 16-bit parallel transmit interface at a rate of 155.52 MHz. This data is passed to a small integrated FIFO to allow flexible transfer of data between the SONET processor and the transmit serializer. As each 16-bit word is read from the transmit FIFO, it is serialized and sent out the high-speed differential line driver at a rate of 2.488 Gbits/second.

Receive Path

As serial data is received at the differential line receiver, it is passed to a clock and data recovery (CDR) PLL, which extracts a precision low-jitter clock from the transitions in the data stream. This bit-rate clock is then used to sample the data stream and receive the data. Every 16-bit-times, a new word is presented at the receive parallel interface along with a clock.

Parallel Interface

The parallel I/O interface supports high-speed bus communications using HSTL signaling levels to minimize both power consumption and board landscape. The HSTL outputs are capable of driving unterminated transmission lines of less than 70 mm, and terminated 50Ω transmission lines of more than twice that length.

The CYS25G0101DX Transceiver's parallel HSTL I/O can also be configured to operate at LVPECL signaling levels. This can all be done externally by changing V_{DDQ} , V_{REF} , and creating a simple circuit at the termination of the transceiver's parallel output interface.

Clocking

The source clock for the transmit data path is selectable from either the recovered clock or an external BITS (Building Integrated Timing Source) reference clock. The low jitter of the

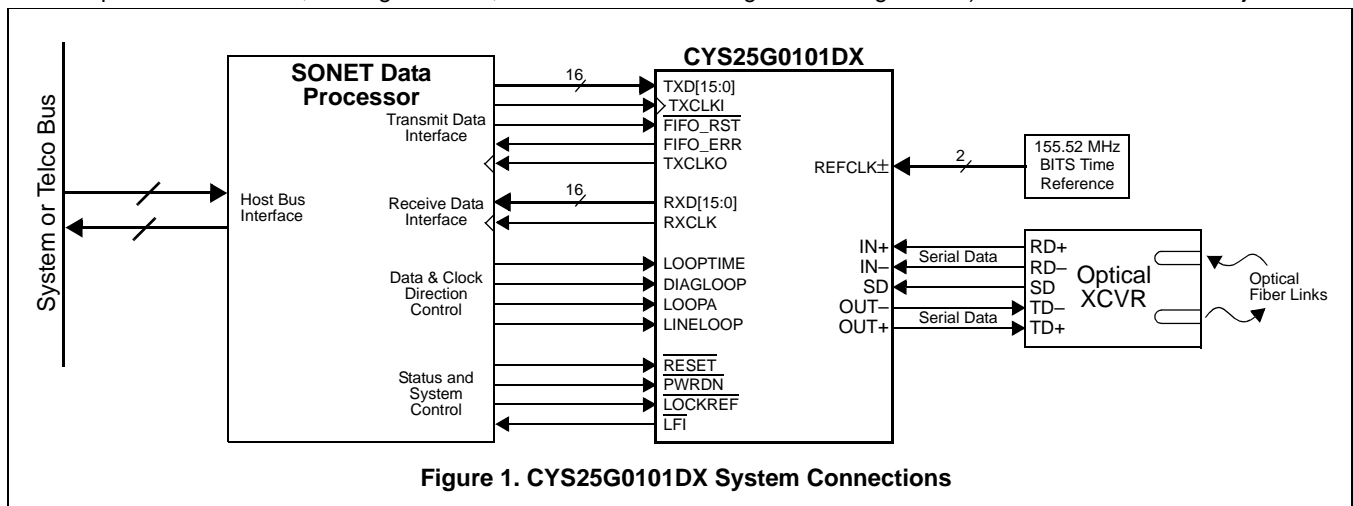


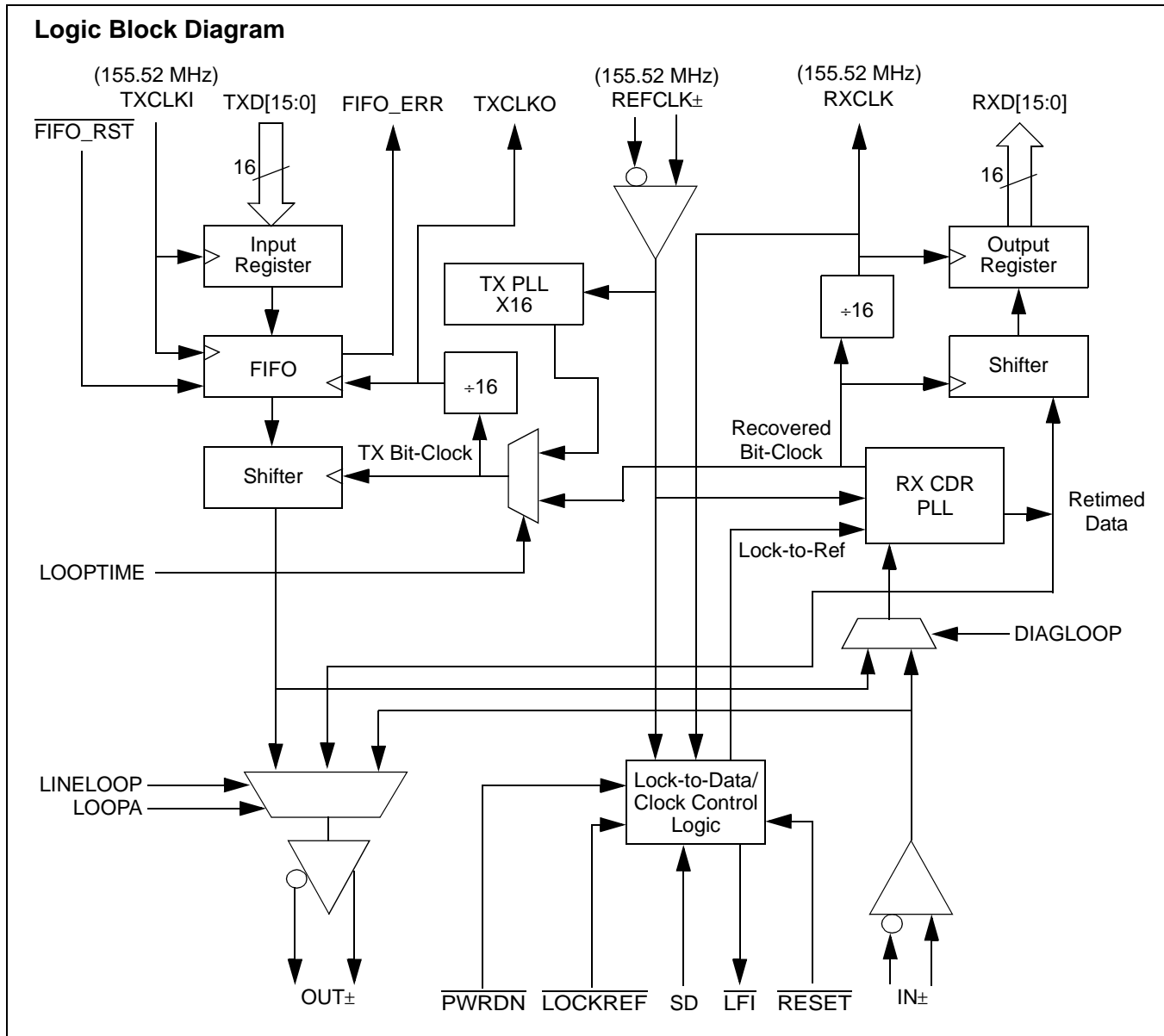
Figure 1. CYS25G0101DX System Connections

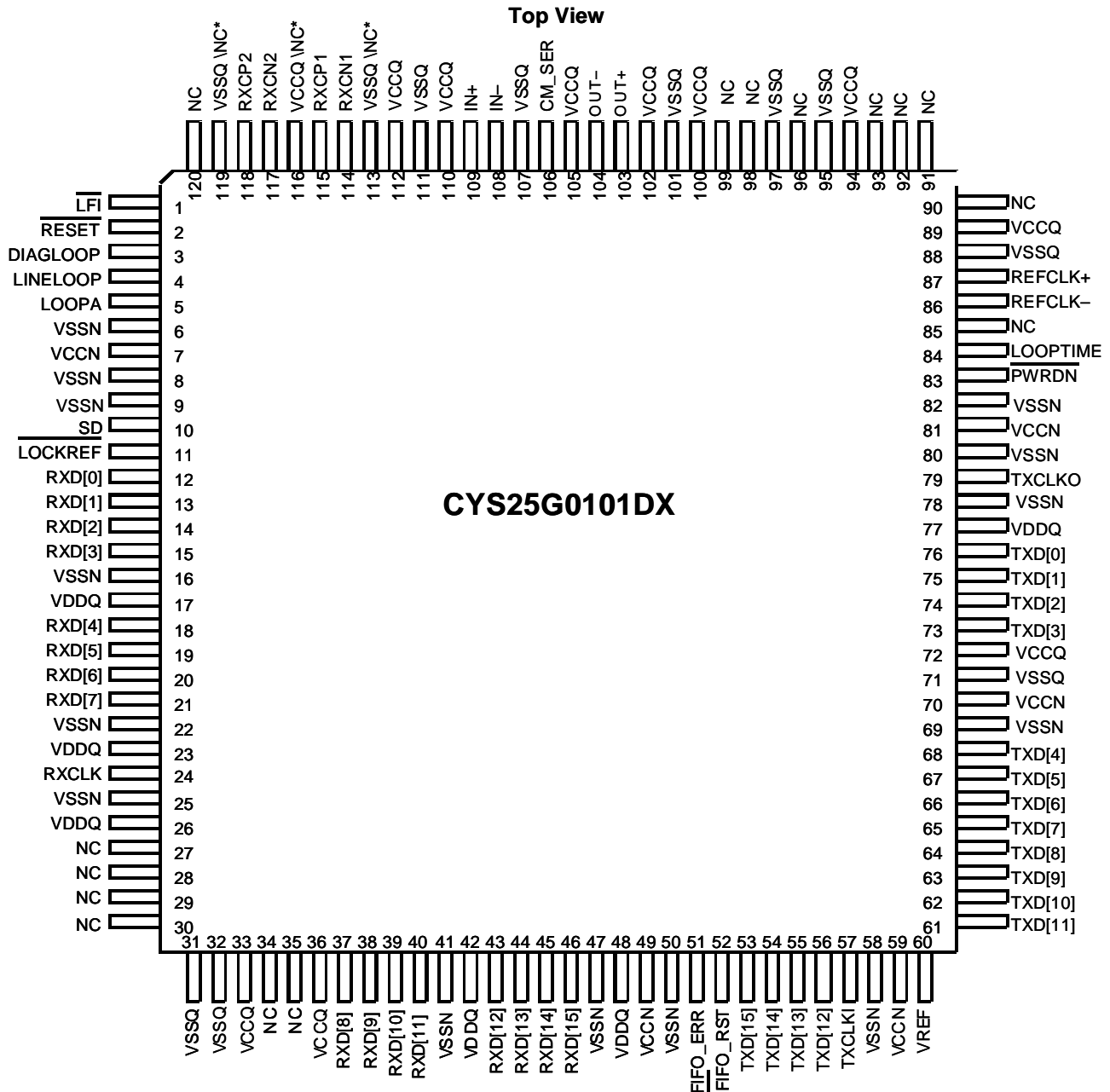
CDR PLL allows loop-timed operation of the transmit data path while still meeting all Bellcore and ITU jitter requirements.

Multiple loopback and loop-through modes are available for both diagnostic and normal operation. For systems containing

redundant SONET rings that are maintained in standby, the CYS25G0101DX may also be dynamically powered down to conserve system power.

Logic Block Diagram



Pin Configuration^[1, 2]
120-pin Thin Quad Flatpack Pin Configuration

Notes:

1. No connect (NC) pins must be left unconnected or floating. Connecting any of these pins to the positive or negative power supply may cause improper operation or failure of the device.
2. Pins 113 and 119 can be either no connect or VSSQ. Use VSSQ for compatibility with next generation of OC-48 SERDES devices. Pin 116 can be either no connect or VCCQ. Use VCCQ for compatibility with next generation of OC-48 SERDES devices.

Pin Descriptions
CYS25G0101DX OC-48 SONET Transceiver

| Pin Name | I/O Characteristics | Signal Description |
|--|---------------------------------|--|
| Transmit Path Signals | | |
| TXD[15:0] | HSTL inputs, sampled by TXCLKI↑ | Parallel Transmit Data Inputs. A 16-bit word, sampled by TXCLKI↑. TXD[15] is the most significant bit (the first bit transmitted). |
| TXCLKI | HSTL Clock input | Parallel Transmit Data Input Clock. The TXCLKI is used to transfer the data into the input register of the serializer. The TXCLKI samples the data, TXD [15:0], on the rising edge of the clock cycle. |
| TXCLKO | HSTL Clock output | Transmit Clock Output. Divide by 16 of the selected transmit bit-rate clock. It can be used to coordinate byte-wide transfers between upstream logic and the CYS25G0101DX. |
| V _{REF} | Input Analog Reference | Reference Voltage for HSTL Parallel Input Bus. V _{DDQ} /2. ^[3] |
| Receive Path Signals | | |
| RXD[15:0] | HSTL output, synchronous | Parallel Receive Data Output. These outputs change following RXCLK↓. RXD[15] is the most significant bit of the output word, and is received first on the serial interface. |
| RXCLK | HSTL Clock output | Receive Clock Output. Divide by 16 of the bit-rate clock extracted from the received serial stream. RXD [15:0] is clocked out on the falling edge of the RXCLK. |
| CM_SER | Analog | Common Mode Termination. Capacitor shunt to V _{SS} for common mode noise. |
| RXCN1 | Analog | Receive Loop Filter Capacitor (Negative) |
| RXCN2 | Analog | Receive Loop Filter Capacitor (Negative) |
| RXCP1 | Analog | Receive Loop Filter Capacitor (Positive) |
| RXCP2 | Analog | Receive Loop Filter Capacitor (Positive) |
| Device Control and Status Signals | | |
| REFCLK± | Differential LVPECL input | Reference Clock. This clock input is used as the timing reference for the transmit and receive PLLs. A derivative of this input clock may also be used to clock the transmit parallel interface. The reference clock is internally biased allowing for an AC-coupled clock signal. |
| LFI | LVTTTL output | Line Fault Indicator. When LOW, this signal indicates that the selected receive data stream has been detected as invalid by either a LOW input on SD, or by the receive VCO being operated outside its specified limits. |
| RESET | LVTTTL input | Reset for all logic functions except the transmit FIFO. |
| LOCKREF | LVTTTL input | Receive PLL Lock to Reference. When LOW, the receive PLL locks to REFCLK instead of the received serial data stream. |
| SD | LVTTTL input | Signal Detect. When LOW, the receive PLL locks to REFCLK instead of the received serial data stream. The SD is to be connected to an external optical module to indicate a loss of received optical power. |
| FIFO_ERR | LVTTTL output | Transmit FIFO Error. When HIGH the transmit FIFO has either under or overflowed. When this occurs, the FIFO's internal clearing mechanism will clear the FIFO within 9 clock cycles. In addition, FIFO_RST must be activated at device power-up to ensure that the in and out pointers of the FIFO are set to maximum separation. |
| FIFO_RST | LVTTTL input | Transmit FIFO Reset. When LOW, the in and out pointers of the transmit FIFO are set to maximum separation. FIFO_RST must be activated at device power-up to ensure that the in and out pointers of the FIFO are set to maximum separation. When the FIFO is being reset, the output data is a 1010... pattern. |
| PWRDN | LVTTTL input | Device Power Down. When LOW, the logic and drivers are all disabled and placed into a standby condition where only minimal power is dissipated. |
| Loop Control Signals | | |
| DIAGLOOP | LVTTTL input | Diagnostic Loopback Control. When HIGH, transmit data is routed through the receive clock and data recovery and presented at the RXD[15:0] outputs. When LOW, received serial data is routed through the receive clock and data recovery and presented at the RXD[15:0] outputs. |

Note:

- V_{REF} equals to (V_{CC} - 1.33)V if interfacing to a parallel LVPECL interface.

CYS25G0101DX OC-48 SONET Transceiver (continued)

| Pin Name | I/O Characteristics | Signal Description |
|-------------------|-------------------------|---|
| LINELOOP | LVTTTL input | Line Loopback Control. When HIGH, received serial data is looped back from receive to transmit after being reclocked by a recovered clock. When LINELOOP is LOW, the data passed to the OUT± line driver is controlled by LOOPA. When both LINELOOP and LOOPA are LOW, the data passed to the OUT± line driver is generated in the transmit shifter. |
| LOOPA | LVTTTL input | Analog Line Loopback. When LINELOOP is LOW and LOOPA is HIGH, received serial data is looped back from receive input buffer to transmit output buffer, but is not routed through the clock and data recovery PLL. When LOOPA is LOW, the data passed to the OUT± line driver is controlled by LINELOOP. |
| LOOPTIME | LVTTTL input | Loop Time Mode. When HIGH, the extracted receive bit-clock replaces transmit bit-clock. When LOW, the REFCLK input is multiplied by 16 to generate the transmit bit clock. |
| Serial I/O | | |
| OUT± | Differential CML output | Differential Serial Data Output. This differential CML output (+3.3V referenced) is capable of driving terminated 50Ω transmission lines or commercial fiber-optic transmitter modules. |
| IN± | Differential CML input | Differential Serial Data Input. This differential input accept the serial data stream for deserialization and clock extraction. |
| Power | | |
| V _{CCN} | Power | +3.3V supply (for digital and low-speed I/O functions) |
| V _{SSN} | Ground | Signal and power ground (for digital and low-speed I/O functions) |
| V _{CCQ} | Power | +3.3V quiet power (for analog functions) |
| V _{SSQ} | Ground | Quiet ground (for analog functions) |
| V _{DDQ} | Power | +1.5V supply for HSTL outputs ^[4] |

CYS25G0101DX Operation

The CYS25G0101DX is a highly configurable device designed to support reliable transfer of large quantities of data using high-speed serial links. It performs necessary clock and data recovery, clock generation, serial-to-parallel conversion, and parallel-to-serial conversion. CYS25G0101DX also provides various loopback functions.

CYS25G0101DX Transmit Data Path
Operating Modes

The transmit path of the CYS25G0101DX supports 16-bit-wide data paths.

Phase-Align Buffer

Data from the input register is passed to a phase-align buffer (FIFO). This buffer is used to absorb clock phase differences between the transmit input clock and the internal character clock.

Initialization of the phase-align buffer takes place when the FIFO_RST input is asserted LOW. When FIFO_RST is returned HIGH, the present input clock phase relative to TXCLKO is set. Once set, the input clock is allowed to skew in time up to half a character period in either direction relative to REFCLK (i.e., ±180°). This time shift allows the delay path of the character clock (relative to REFCLK) to change due to operating voltage and temperature while not effecting the desired operation. FIFO_RST is an asynchronous input. FIFO_ERR is the transmit FIFO Error indicator. When HIGH,

Note:

4. V_{DDQ} equals V_{CC} if interfacing to a parallel LVPECL interface.

the transmit FIFO has either under or overflowed. The FIFO can be externally reset to clear the error indication or if no action is taken, the internal clearing mechanism will clear the FIFO in nine clock cycles. When the FIFO is being reset, the output data is 1010.

Transmit PLL Clock Multiplier

The Transmit PLL Clock Multiplier accepts a 155.52-MHz external clock at the REFCLK input, and multiplies that clock by 16 to generate a bit-rate clock for use by the transmit shifter. The operating serial signaling rate and allowable range of REFCLK frequencies is listed in Table 7. The REFCLK phase noise limits to meet SONET compliancy are illustrated in Figure 5. The REFCLK± input is a standard LVPECL input.

Serializer

The parallel data from the phase-align buffer is passed to the Serializer which converts the parallel data to serial data using the bit-rate clock generated by the Transmit PLL clock multiplier. TXD[15] is the most significant bit of the output word, and is transmitted first on the serial interface.

Serial Output Driver

The serial interface Output Driver makes use of high-performance differential Current Mode Logic (CML) to provide a source-matched driver for the transmission lines. This driver receives its data from the Transmit Shifters or the receive loopback data. The outputs have signal swings equivalent to that of standard LVPECL drivers, and are capable of driving AC-coupled optical modules or transmission lines.

CYS25G0101DX Receive Data Path

Serial Line Receivers

A differential line receiver, IN_{\pm} , is available for accepting the input serial data stream. The serial line receiver inputs can accommodate high wire interconnect and filtering losses or transmission line attenuation ($V_{SE} \geq 25$ mV, or 50 mV peak-to-peak differential), and can be AC-coupled to +3.3V or +5V powered fiber-optic interface modules. The common-mode tolerance of these line receivers accommodates a wide range of signal termination voltages.

Lock to Data Control

Line Receiver routed to the clock and data recovery PLL is monitored for

- status of signal detect (SD) pin
- status of $\overline{LOCKREF}$ pin.

This status is presented on the Line Fault Indicator (\overline{LFI}) output, which changes asynchronously in the cases in which SD or $\overline{LOCKREF}$ go from HIGH to LOW. Otherwise, it changes synchronously to the REFCLK.

Clock/Data Recovery

The extraction of a bit-rate clock and recovery of data bits from received serial stream is performed by a Clock/Data Recovery (CDR) block. The clock extraction function is performed by high-performance embedded phase-locked loop (PLL) that tracks the frequency of the incoming bit stream and aligns the phase of the internal bit-rate clock to the transitions in the selected serial data stream.

CDR accepts a character-rate (bit-rate * 16) reference clock on the REFCLK input. This REFCLK input is used to ensure that the VCO (within the CDR) is operating at the correct frequency (rather than some harmonic of the bit-rate), to improve PLL acquisition time, and to limit unlocked frequency excursions of the CDR VCO when no data is present at the serial inputs.

Regardless of the type of signal present, the CDR will attempt to recover a data stream from it. If the frequency of the recovered data stream is outside the limits set by the range controls, the CDR PLL will track REFCLK instead of the data stream. When the frequency of the selected data stream returns to a valid frequency, the CDR PLL is allowed to track the received data stream. The frequency of REFCLK is required to be within ± 100 ppm of the frequency of the clock that drives the REFCLK signal of the remote transmitter to ensure a lock to the incoming data stream.

For systems using multiple or redundant connections, the \overline{LFI} output can be used to select an alternate data stream. When an LFI indication is detected, external logic can toggle selection of the input device. When such a port switch takes place, it is necessary for the PLL to reacquire lock to the new serial stream.

External Filter

The CDR circuit uses external capacitors for the PLL filter. A 0.1- μ F capacitor needs be connected between RXCN1 and RXCP1. Similarly a 0.1- μ F capacitor needs to be connected between RXCN2 and RXCP2. The recommended packages and dielectric material for these capacitors are 0805 X7R or 0603 X7R.

Deserializer

The CDR circuit extracts bits from the serial data stream and

clocks these bits into the Deserializer at the bit-clock rate. The Deserializer converts serial data into parallel data. RXD[15] is the most significant bit of the output word and is received first on the serial interface.

Loopback/Timing Modes

CYS25G0101DX supports various loopback modes, as described below.

Facility Loopback (Line Loopback with Retiming)

When the LINELOOP signal is set HIGH, the Facility Loopback mode is activated and the high-speed serial receive data (IN_{\pm}) is presented to the high-speed transmit output (OUT_{\pm}) after retiming. In Facility Loopback mode, the high-speed receive data (IN_{\pm}) is also converted to parallel data and presented to the low-speed receive data output pins (RXD[15:0]). The receive recovered clock is also divided down and presented to the low-speed clock output (RXCLK).

Equipment Loopback (Diagnostic Loopback with Retiming)

When the DIAGLOOP signal is set HIGH, transmit data is looped back to the RX PLL, replacing IN_{\pm} . Data is looped back from the parallel TX inputs to the parallel RX outputs. The data is looped back at the internal serial interface and goes through transmit shifter and the receive CDR. SD is ignored in this mode.

Line Loopback Mode (Non-retimed Data)

When the LOOPA signal is set HIGH, the RX serial data is directly buffered out to the transmit serial data. The data at the serial output is not retimed.

Loop Timing Mode

When the LOOPTIME signal is set HIGH, the TX PLL is bypassed and receive bit-rate clock is used for transmit side shifter.

Reset Modes

ALL logic circuits in the device can be reset using \overline{RESET} and $\overline{FIFO_RST}$ signals. When \overline{RESET} is set LOW, all logic circuits except FIFO are internally reset. When $\overline{FIFO_RST}$ is set LOW, the FIFO logic is reset.

Power-down Mode

CYS25G0101DX provides a global power-down signal \overline{PWRDN} . When LOW, this signal powers down the entire device to a minimal power dissipation state. \overline{RESET} and $\overline{FIFO_RST}$ signals should be asserted LOW along with \overline{PWRDN} signal to ensure low power dissipation.

LVPECL Compliance

The CYS25G0101DX HSTL parallel I/O can be configured to LVPECL compliance with slight termination modifications. On the transmit side of the transceiver, the TXD[15:0] and TXCLKI can be made LVPECL compliant by setting V_{REF} (reference voltage of a LVPECL signal) to $V_{CC} - 1.33V$. To emulate an LVPECL signal on the receiver side, VDDQ needs to be set to 3.3V and the transmission lines need to be terminated with the Thévenin equivalent of Z_0 at LVPECL ref. The signal is then attenuated using a series resistor at the driver end of the line to reduce the 3.3V swing level to an LVPECL swing level (see Figure 10). This circuit needs to be used on all 16 RXD[15:0] pins, TXCLKO, and RXCLK. The voltage divider has been calculated assuming the system is built with 50 Ω transmission lines.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

| | |
|---|--|
| Storage Temperature | -65°C to +150°C |
| Ambient Temperature with Power Applied..... | -55°C to +125°C |
| V _{CC} Supply Voltage to Ground Potential | -0.5V to +4.2V |
| V _{DDQ} Supply Voltage to Ground Potential | -0.5V to +4.2V |
| DC Voltage Applied to HSTL Outputs in High-Z State | -0.5V to V _{DDQ} + 0.5V |
| DC Voltage Applied to Other Outputs in High-Z State | -0.5V to V _{CC} + 0.5V |
| Output Current into LVTTTL Outputs (LOW)..... | 30 mA |
| DC Input Voltage..... | -0.5V to V _{CC} + 0.5V |
| Static Discharge Voltage | > 1100V (per MIL-STD-883, Method 3015) |
| Latch-up Current..... | > 200 mA |

Table 1. DC Specifications—LVTTTL

| Parameter | Description | Test Conditions | Min. | Max. | Unit |
|-----------------------|------------------------------|---|------|-----------------------|------|
| LVTTTL Outputs | | | | | |
| V _{OHT} | Output HIGH Voltage | V _{CC} = Min., I _{OH} = -10.0 mA | 2.4 | | V |
| V _{OLT} | Output LOW Voltage | V _{CC} = Min., I _{OL} = 10.0 mA | | 0.4 | V |
| I _{OS} | Output Short Circuit Current | V _{OUT} = 0V | -20 | -90 | mA |
| LVTTTL Inputs | | | | | |
| V _{IHT} | Input HIGH Voltage | Low = 2.1V, High = V _{CC} + 0.5V | 2.1 | V _{CC} - 0.3 | V |
| V _{ILT} | Input LOW Voltage | Low = -3.0V, High = 0.8 | -0.3 | 0.8 | V |
| I _{IHT} | Input HIGH Current | V _{CC} = Max., V _{IN} = V _{CC} | | 50 | μA |
| I _{ILT} | Input LOW Current | V _{CC} = Max., V _{IN} = 0V | | -50 | μA |
| Capacitance | | | | | |
| C _{IN} | Input Capacitance | V _{CC} = Max., @ f = 1 MHz | | 5 | pF |

Table 2. DC Specifications—Power

| Parameter | Description | Test Conditions | Typ. | Max. | Unit |
|------------------|-----------------------------|-----------------|------|------|------|
| Power | | | | | |
| I _{CC1} | Active Power Supply Current | | 300 | 347 | mA |
| I _{SB} | Standby Current | | | 5 | mA |

Table 3. DC Specifications—Differential LVPECL Compatible Inputs (REFCLK) ^[5]

| Parameter | Description | Test Conditions | Min. | Max. | Unit |
|---------------------|----------------------------|--|-----------------------|------------------------|------|
| V _{INSGLE} | Input Single-ended Swing | | 200 | 600 | mV |
| V _{DIFFE} | Input Differential Voltage | | 400 | 1200 | mV |
| V _{IEHH} | Highest Input HIGH Voltage | | V _{CC} - 1.2 | V _{CC} - 0.3 | V |
| V _{IELL} | Lowest Input LOW Voltage | | V _{CC} - 2.0 | V _{CC} - 1.45 | V |
| I _{IEH} | Input HIGH Current | V _{IN} = V _{IEHH} Max. | | 750 | μA |
| I _{IEL} | Input LOW Current | V _{IN} = V _{IELL} Min. | -200 | | μA |
| Capacitance | | | | | |
| C _{INE} | Input Capacitance | | | 4 | pF |

Note:

5. See Figure 2 for differential waveform definition.

Power-up Requirements

Power supply sequencing is not required if you are configuring VDDQ=3.3volts and all power supplies pins are connected to the same 3.3 volt power supply.

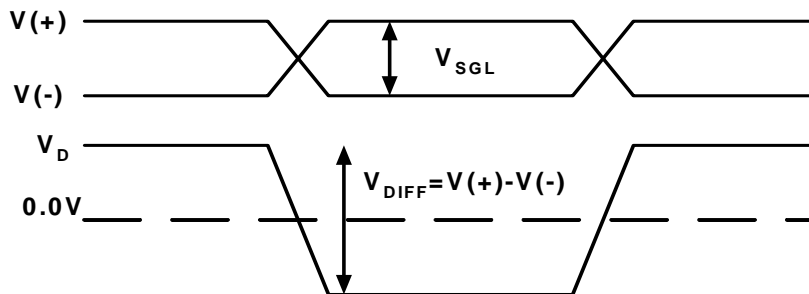
Power supply sequencing is required if you are configuring VDDQ=1.5volts. Power must be applied in the following sequence: VCC (3.3) followed by VDDQ (1.5). Power supply ramping may occur simultaneously as long as the VCC/VDDQ relationship is maintained.

Operating Range

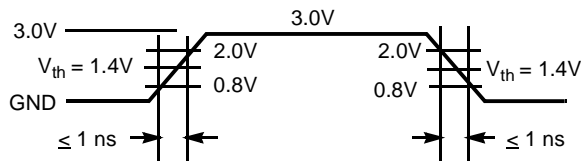
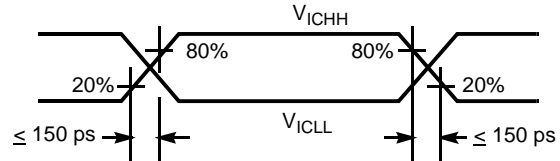
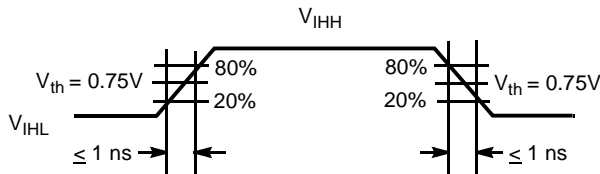
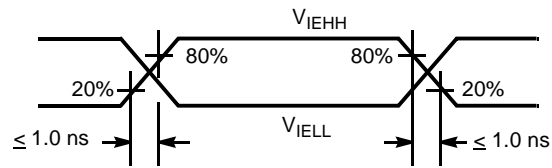
| Range | Ambient Temperature | V _{DDQ} | V _{CC} |
|------------|---------------------|-----------------------------|-----------------|
| Commercial | 0°C to +70°C | 1.4V to 1.6V ^[4] | 3.3V ± 10% |
| Industrial | -40°C to +85°C | 1.4V to 1.6V ^[4] | 3.3V ± 10% |

Table 4. DC Specifications—Differential CML^[5]

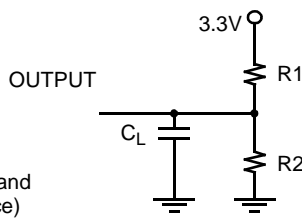
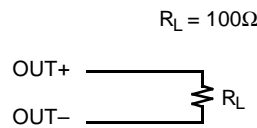
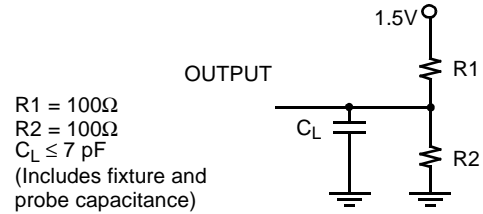
| Parameter | Description | Test Conditions | Min. | Max. | Unit |
|---|--|------------------------|-----------------------|------------------------|------|
| Transmitter CML-compatible Outputs | | | | | |
| V _{OHC} | Output HIGH Voltage (V _{CC} Referenced) | 100Ω differential load | V _{CC} - 0.5 | V _{CC} - 0.15 | V |
| V _{OLC} | Output LOW Voltage (V _{CC} Referenced) | 100Ω differential load | V _{CC} - 1.2 | V _{CC} - 0.7 | V |
| V _{DIFFOC} | Output Differential Swing | 100Ω differential load | 560 | 1600 | mV |
| V _{SGLCO} | Output Single-ended Voltage | 100Ω differential load | 280 | 800 | mV |
| Receiver CML-compatible Inputs | | | | | |
| V _{INSGLC} | Input Single-ended Swing | | 25 | 1000 | mV |
| V _{DIFFC} | Input Differential Voltage | | 50 | 2000 | mV |
| V _{ICHH} | Highest Input HIGH Voltage | | | V _{CC} | V |
| V _{ICLL} | Lowest Input LOW Voltage | | 1.2 | | V |


Figure 2. Differential Waveform Definition
Table 5. DC Specifications—HSTL

| Parameter | Description | Test Conditions | Min. | Max. | Unit |
|---------------------|------------------------------|---|-------------------------|------------------------|------|
| HSTL Outputs | | | | | |
| V _{OHH} | Output HIGH Voltage | V _{CC} = min., I _{OH} = -4.0 mA | V _{DDQ} - 0.4 | | V |
| V _{OLH} | Output LOW Voltage | V _{CC} = min., I _{OL} = 4.0 mA | | 0.4 | V |
| I _{OSH} | Output Short Circuit Current | V _{OUT} = 0V | | 100 | mA |
| HSTL Inputs | | | | | |
| V _{IHH} | Input HIGH Voltage | | V _{REF} + 0.13 | V _{DDQ} + 0.3 | V |
| V _{ILH} | Input LOW Voltage | | -0.3 | V _{REF} - 0.1 | V |
| I _{IHH} | Input HIGH Current | V _{DDQ} = max., V _{IN} = V _{DDQ} | | 50 | μA |
| I _{ILH} | Input LOW Current | V _{DDQ} = max., V _{IN} = 0V | | -40 | μA |
| Capacitance | | | | | |
| C _{INH} | Input Capacitance | V _{DDQ} = max., @ f = 1 MHz | | 5 | pF |

AC Waveforms

(a) LVTTTL Input Test Waveform

(b) CML Input Test Waveform

(c) HSTL Input Test Waveform

(d) LVPECL Input Test Waveform
AC Test Loads

$R1 = 330\Omega$
 $R2 = 510\Omega$
 $C_L \leq 10 \text{ pF}$
 (Includes fixture and probe capacitance)


(a) TTL AC Test Load

(b) CML AC Test Load

(c) HSTL AC Test Load
AC Specifications
Table 6. AC Specifications—Parallel Interface

| Parameter | Description | Min. | Max. | Unit |
|---------------|---|-------|-------|------|
| t_{TS} | TXCLKI Frequency (must be frequency coherent to REFCLK) | 154.5 | 156.5 | MHz |
| t_{TXCLKI} | TXCLKI Period | 6.38 | 6.47 | ns |
| $t_{TXCLKID}$ | TXCLKI Duty Cycle | 40 | 60 | % |
| $t_{TXCLKIR}$ | TXCLKi Rise Time | 0.3 | 1.5 | ns |
| $t_{TXCLKIF}$ | TXCLKi Fall Time | 0.3 | 1.5 | ns |
| t_{TXDS} | Write Data Set-up to \uparrow of TXCLKI | 1.5 | | ns |
| t_{TXDH} | Write Data Hold from \uparrow of TXCLKI | 0.5 | | ns |
| t_{TOS} | TXCLKO Frequency | 154.5 | 156.5 | MHz |
| t_{TXCLKO} | TXCLKO Period | 6.38 | 6.47 | ns |
| $t_{TXCLKOD}$ | TXCLKO Duty Cycle | 43 | 57 | % |
| $t_{TXCLKOR}$ | TXCLKO Rise Time | 0.3 | 1.5 | ns |
| $t_{TXCLKOF}$ | TXCLKO Fall Time | 0.3 | 1.5 | ns |
| t_{RS} | RXCLK Frequency | 154.5 | 156.5 | MHz |
| t_{RXCLK} | RXCLK Period | 6.38 | 6.47 | ns |
| t_{RXCLKD} | RXCLK Duty Cycle | 43 | 57 | % |
| t_{RXCLKR} | RXCLK Rise Time ^[6] | 0.3 | 1.5 | ns |
| t_{RXCLKF} | RXCLK Fall Time ^[6] | 0.3 | 1.5 | ns |
| t_{RXDS} | Recovered Data Set-up with reference to \uparrow of RXCLK | 2.2 | | ns |
| t_{RXDH} | Recovered Data Hold with reference to \uparrow of RXCLK | 2.2 | | ns |
| t_{RXPd} | Valid Propagation Delay | -1.0 | 1.0 | ns |

Table 7. AC Specifications—REFCLK^[7]

| Parameter | Description | Min. | Max. | Unit |
|-------------------|--|-------|-------|------|
| t _{REF} | REFCLK Input Frequency | 154.5 | 156.5 | MHz |
| t _{REFP} | REFCLK Period | 6.38 | 6.47 | ns |
| t _{REFD} | REFCLK Duty Cycle | 35 | 65 | % |
| t _{REFT} | REFCLK Frequency Tolerance — (relative to received serial data) ^[8] | -100 | +100 | ppm |
| t _{REFR} | REFCLK Rise Time | 0.3 | 1.5 | ns |
| t _{REFF} | REFCLK Fall Time | 0.3 | 1.5 | ns |

Table 8. AC Specifications—CML Serial Outputs

| Parameter | Description | Min. | Typical | Max. | Unit |
|-------------------|---|------|---------|------|------|
| t _{RISE} | CML Output Rise Time (20–80%, 100Ω balanced load) | 60 | | 170 | ps |
| t _{FALL} | CML Output Fall Time (80–20%, 100Ω balanced load) | 60 | | 170 | ps |

Table 9. Jitter Specifications

| Parameter | Description | Min. | Typical ^[10] | Max. ^[10] | Unit |
|-----------------------|---|------|-------------------------|----------------------|------|
| t _{TJ-TXPLL} | Total Output Jitter for TX PLL (p-p) ^[9] | | 0.03 | 0.04 | UI |
| | Total Output Jitter for TX PLL (rms) ^[9, 11] | | 0.007 | 0.008 | UI |
| t _{TJ-RXPLL} | Total Output Jitter for RX CDR PLL (p-p) ^[9] | | 0.035 | 0.05 | UI |
| | Total Output Jitter for RX CDR PLL (rms) ^[9, 11] | | 0.008 | 0.01 | UI |

Notes:

6. RXCLK rise time and fall times are measured at the 20 to 80 percentile region of the rising and falling edge of the clock signal.
7. The 155.52 MHz Reference Clock Phase Noise Limits for the CYS25G0101DX are illustrated in *Figure 5*.
8. ±20 ppm is required to meet the SONET output frequency specification.
9. The RMS and P-to-P jitter values are measured using a 12-KHz to 20-MHz SONET filter.
10. Typical values are measured at room temperature and the Max. values are measured at 0° C.
11. This device passes the Bellcore specification from -10° C to 85° C.

Jitter Waveforms

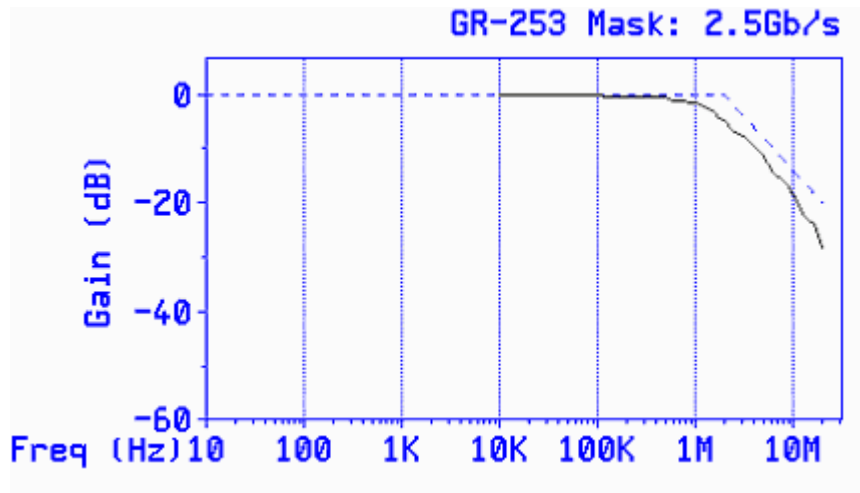


Figure 3. Jitter Transfer Waveform of CYS25G0101DX^[12]

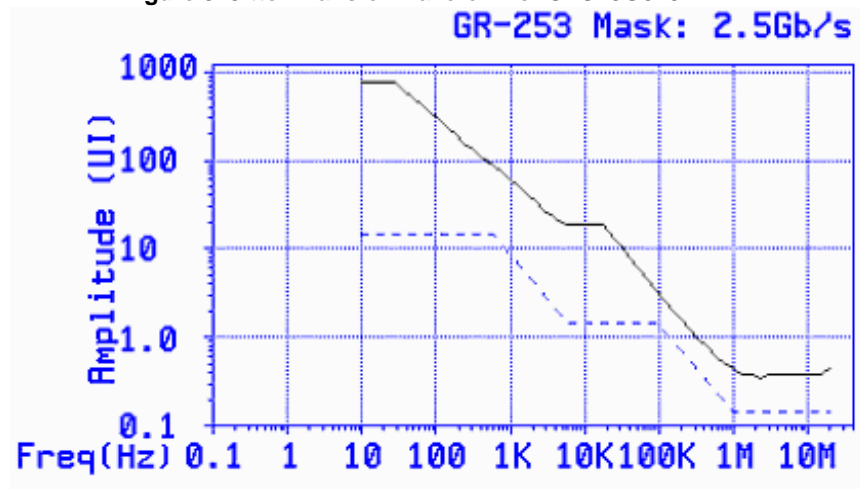


Figure 4. Jitter Tolerance Waveform of CYS25G0101DX^[12]

Note:

12. The bench jitter measurements were performed using an Agilent Omni-bert SONET jitter tester.

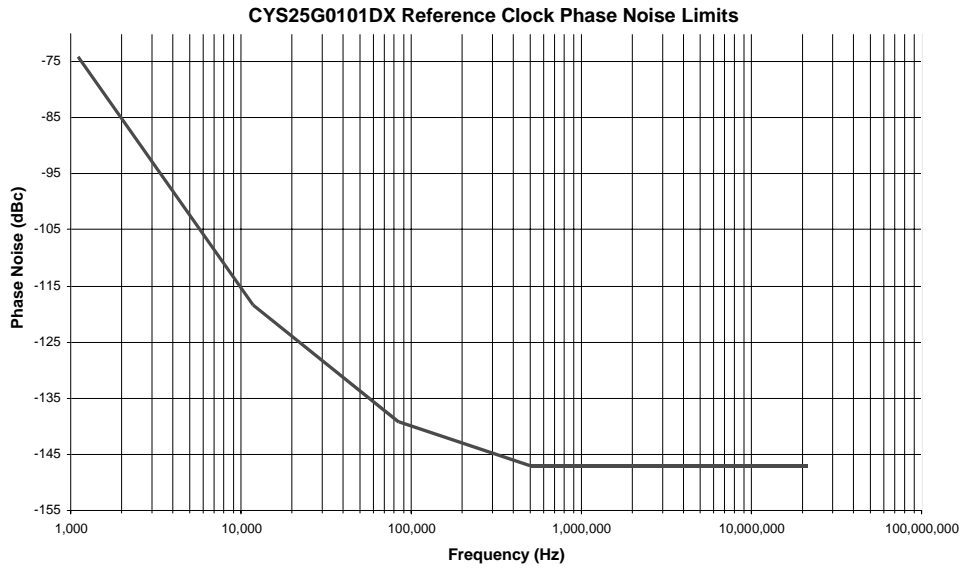
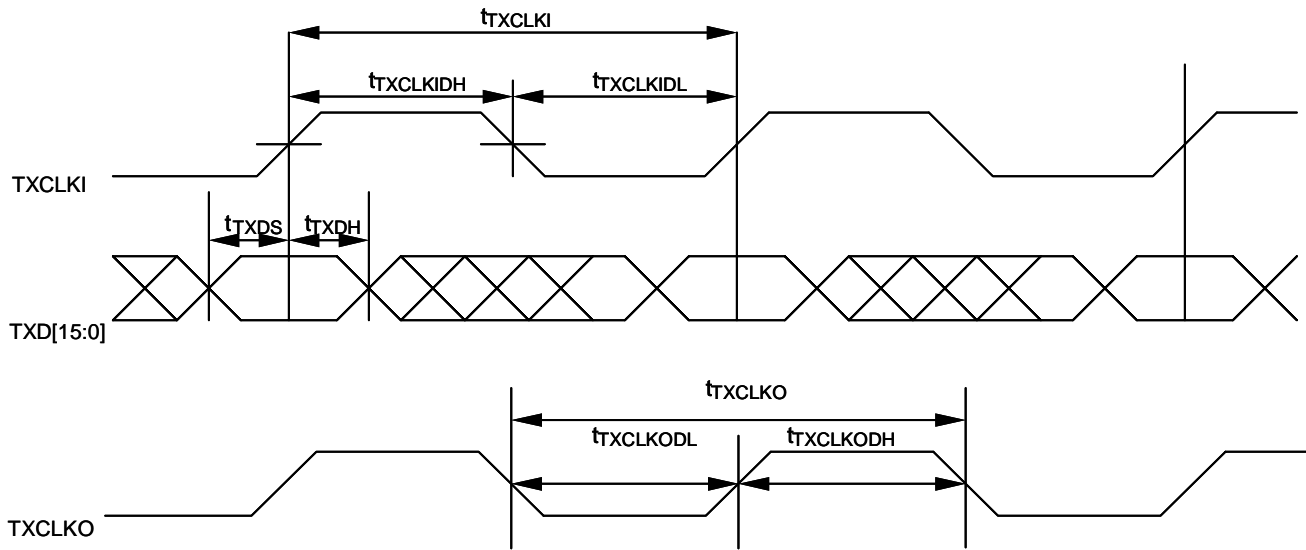


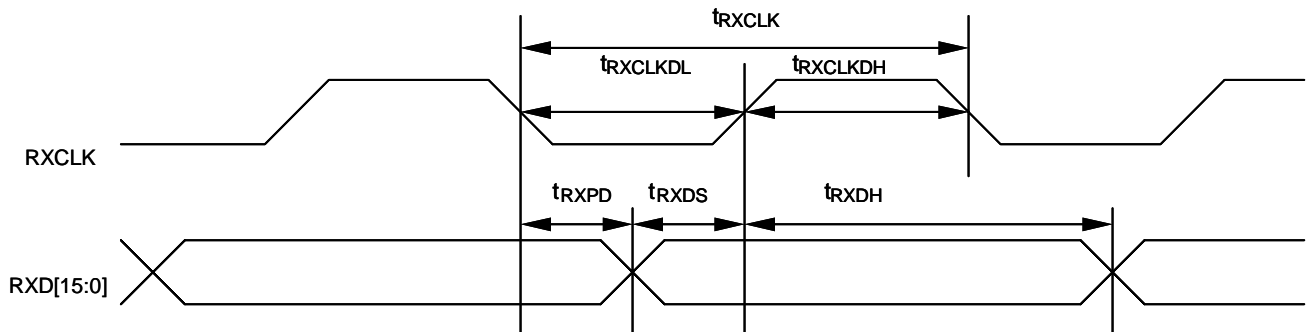
Figure 5. CYS25G0101DX Reference Clock Phase Noise Limits

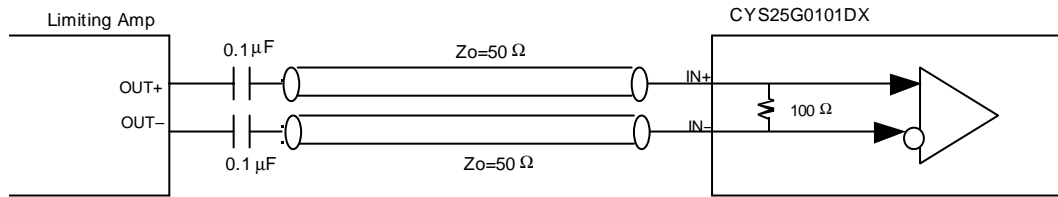
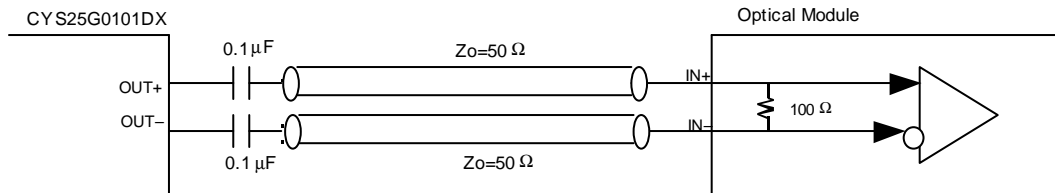
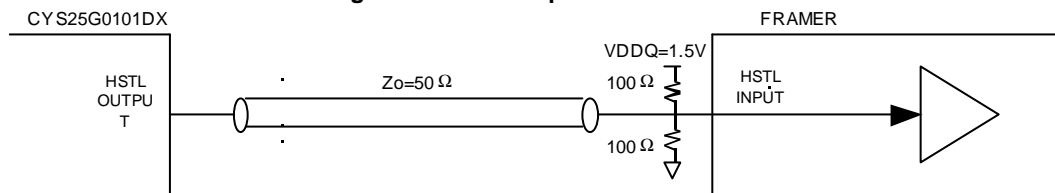
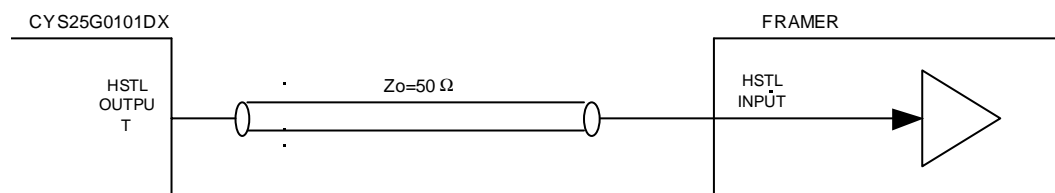
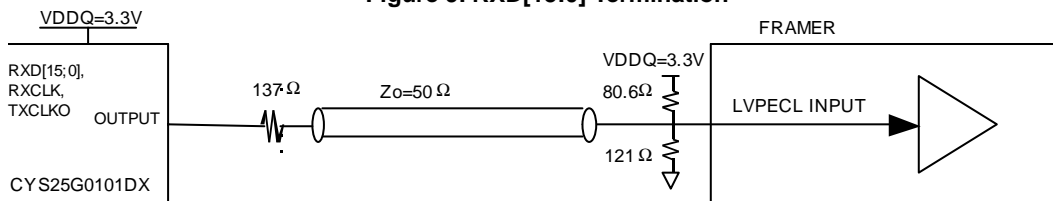
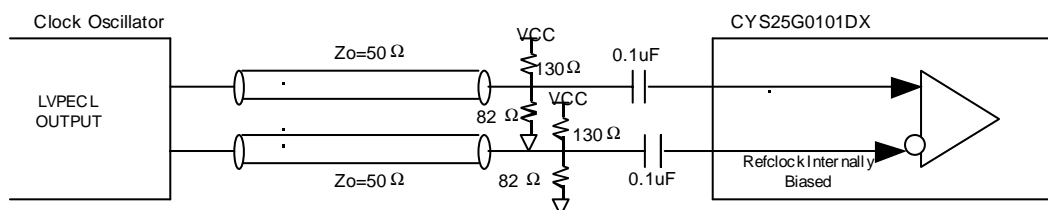
Switching Waveforms

Transmit Interface Timing

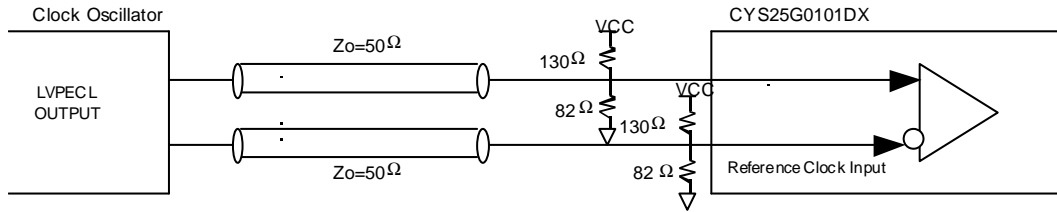


Receive Interface Timing

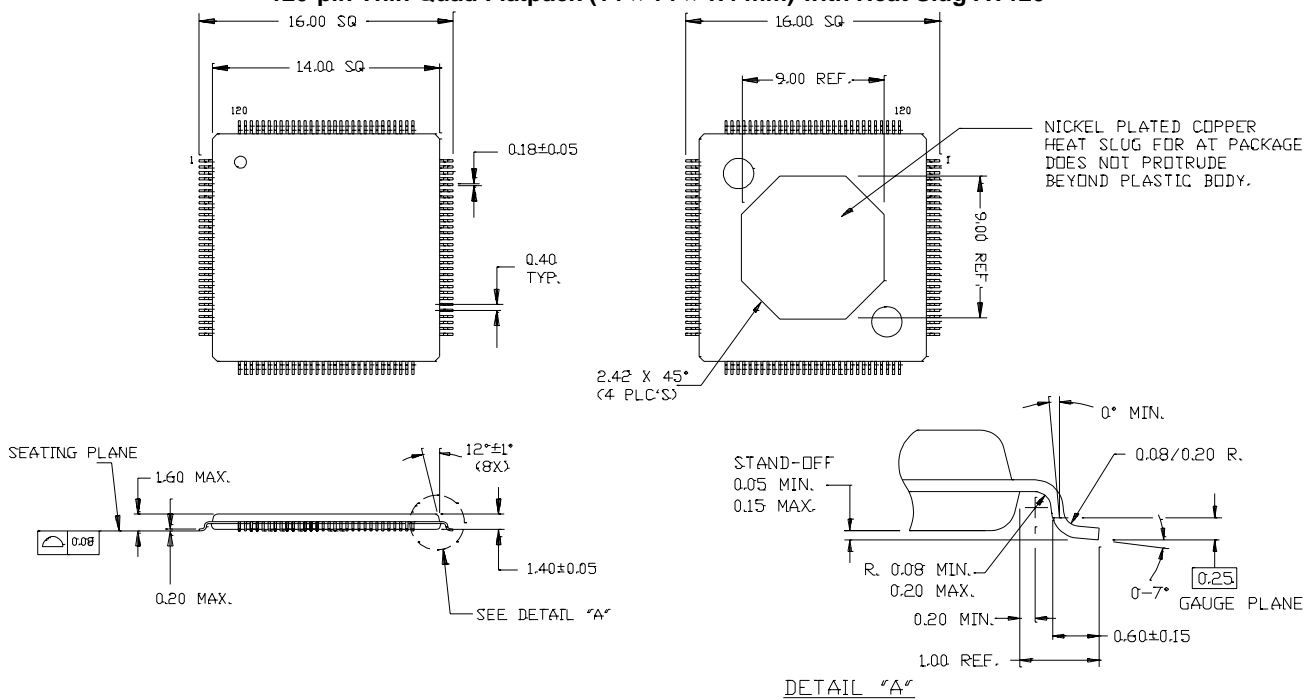


Typical I/O Terminations

Figure 6. Serial Input Termination

Figure 7. Serial Output Termination^[13]

Figure 8. TXCLKO/ RXCLK Termination

Figure 9. RXD[15:0] Termination

Figure 10. LVPECL-compliant Output Termination

Figure 11. AC-Coupled Clock Oscillator Termination
Note:

13. Serial output of CYS25G0101DX is source matched to 50Ω transmission lines (100Ω differential transmission lines).


Figure 12. Clock Oscillator Termination
Ordering Information

| Speed | Ordering Code | Package Name | Package Type | Operating Range |
|----------|------------------|--------------|--------------|-----------------|
| Standard | CYS25G0101DX-ATC | AT120 | 120-pin TQFP | Commercial |
| Standard | CYS25G0101DX-ATI | AT120 | 120-pin TQFP | Industrial |

Package Diagram
120-pin Thin Quad Flatpack (14 × 14 × 1.4 mm) with Heat Slug AT120


DIMENSIONS IN MILLIMETERS

51-85116-**

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Document History Page

| Document Title: CYS25G0101DX SONET OC-48 Transceiver | | | | |
|--|---------|------------|-----------------|--|
| Document Number: 38-02009 | | | | |
| REV. | ECN NO. | Issue Date | Orig. of Change | Description of Change |
| ** | 105847 | 03/22/01 | SZV | Change from Spec number: 38-00894 to 38-02009. |
| *A | 108024 | 06/20/01 | AMV | Changed Marketing part number. |
| *B | 111834 | 12/18/01 | CGX | Updated power specification in features and DC specs section. Changed pinout to be compatible with CYS25G0102DX in pin diagram and descriptions. Verbiage added or changed for clarity in pin descriptions section. Changed input sensitivity in Receive Data Path section, page 6. RXCLK rise time corrected to 0.3 nSec min. CML and LVPECL input waveforms updated in test load and waveform section. Diagrams replaced for clarity Figures 1-10. Added two Refclock diagrams Figures 9 and 10. |
| *C | 112712 | 02/06/02 | TME | Updated temperature range, static discharge voltage, and max total RMS jitter. |
| *D | 113791 | 04/24/02 | CGX | Updated the single ended swing and differential swing voltage for Receiver CML compatible inputs. Created a separate table showing peak to peak and RMS jitter for both TX PLL and RX PLL. |
| *E | 115940 | 05/22/02 | TME | Added Industrial temperature spec to pages 8, 11, and 15. |
| *F | 117906 | 09/06/02 | CGX | Added differential waveform definition. Added BGA pinout and package information. Changed LVTTTL V_{IHT} min. from 2.0 to 2.1 volts. |
| *G | 119267 | 10/17/02 | CGX | Added phase noise limits data. Removed BGA pinout and package information. Removed references to CYS25G0102DX. |
| *H | 121019 | 11/06/02 | CGX | Removed "Preliminary" from data-sheet |
| *I | 122319 | 12/30/02 | RBI | Add power up requirements to Maximum Ratings information |
| *J | 124438 | 02/13/03 | WAI | Revised power up requirements |