The Selection of MOSFETs for DC-DC-Converters

by Jens Ejury, V2.0

- Application Schematic
- Device Considerations
  - Pulse Drain Current
  - Avalanche
  - Summary
- Customer Policies
- Conclusions

Application Schematic

Figure 1 shows the power parts in a DC-DC-Converter. The MOSFET Q_1 is the Control-FET (High Side FET), Q_2 is the Synchronous FET (Low Side FET). Both FETs are subject to many calculations in order to choose the most suitable combination for the application. Basically both FETs have to withstand the input voltage. The MOSFETs also have to have a capability to handle additional voltage spikes caused by parasitic inductances. The maximum current seen by both FETs is the output current plus 50 % of the ripple current. Since both FETs are switched dynamically their power dissipation results partly out of the static losses contributed by the on-resistance and the current and partly out of the switching losses. Especially for the hard switched Control-FET switching losses play an important role.

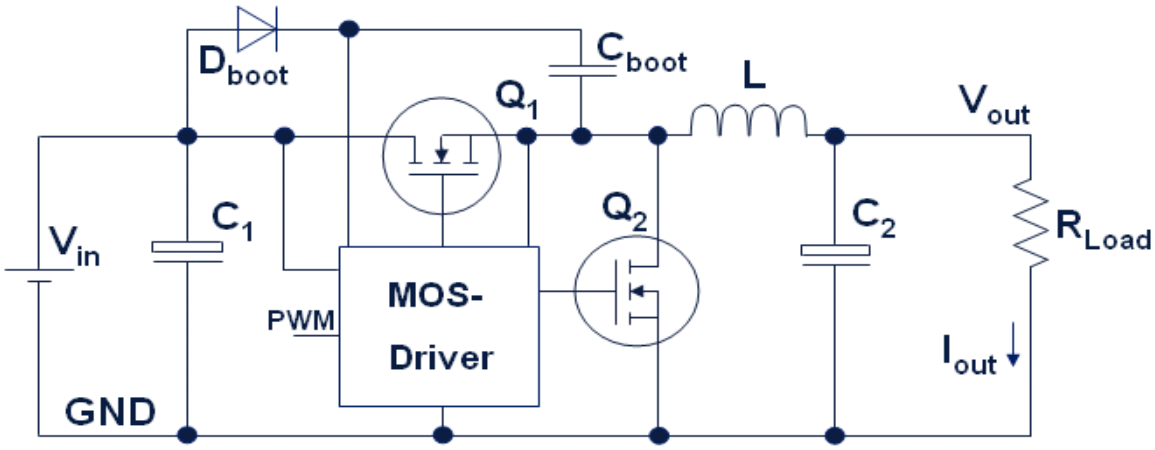


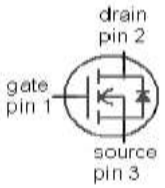
Figure 1

Device Considerations

Every semiconductor is aging, certain parameters change within a specified range. The Infineon specification (datasheet) gives values that are valid during the whole life of the

semiconductor. Only a design based on these values where the MOSFET never exceeds the maximum operation conditions, like given in the datasheet, will fulfill the reliability requirements.

Furthermore, in the datasheet several values are given that allow to exceed the values for static operation mode in a certain range. By means of the Infineon 3.8 mΩ OptiMOS®2 N-Channel MOSFET IPD04N03LA in a D-PAK package this topic shall be considered. Figure 2 shows the table of the first page with the absolute maximum ratings.



Type	Package	Ordering Code	Marking
IPD04N03LA	P-TO252-3-11	Q67042-S4177	04N03LA

Maximum ratings, at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	T_C=25 °C[1)]	50	A
		T_C=100 °C	50	
Pulsed drain current	$I_{D,pulse}$	T_C=25 °C[2)]	350	
Avalanche energy, single pulse	E_{AS}	I_D=50 A, R_{GS}=25 Ω	890	mJ
Reverse diode dv/dt	dv/dt	I_D=50 A, V_{DS}=20 V, di/dt=200 A/µs, $T_{j,max}$=175 °C	6	kV/µs
Gate source voltage[3)]	V_{GS}		±20	V
Power dissipation	P_{tot}	T_C=25 °C	115	W
Operating and storage temperature	T_j, T_{stg}		-55 ... 175	°C
IEC climatic category; DIN IEC 68-1			55/175/56	

Figure 2

Pulse Drain Current

Like shown the nominal drain current rating is 50 A. However, it is possible to have current pulses of up to 350 A like stated in this table too. The note 2) refers to a schematic belonging to the datasheet (Figure 3). This diagram (Safe Operating Area) gives information about the static operation conditions of the MOSFET as well as about the conditions under which the static values can be exceeded without violating the specification. The device is able to handle V_{DS} and $I_{D,pulse}$ over a time of 1 µs assuming that the initial conditions have been like given in the specification (T_C=25˚C). That represents a total power dissipation of 25 V x 350 A, which is equal to 8.75 kW.

Compared to the permitted static P_{tot} value of 115 W this is 76-fold more. Again it should be mentioned that this is an allowed operation mode which is not violating the specification as long as the boundary conditions (T_j, T_a, t) are not exceeded.

The most critical value for the aging of the MOSFET is the junction temperature. This value is also given on the first page and may not be exceeded under any circumstances. With respect to the previous explanations the junction temperature doesn't exceed the given maximum rating of 175 ˚C. This can be explained by the relatively low dissipated energy of only 8.75 mJ (8.75 kW, 1 µs) in a very short period of time. The reason for the ability of the MOSFET to absorb this amount of energy without suffering can be found in the thermal capacitance of the device itself.

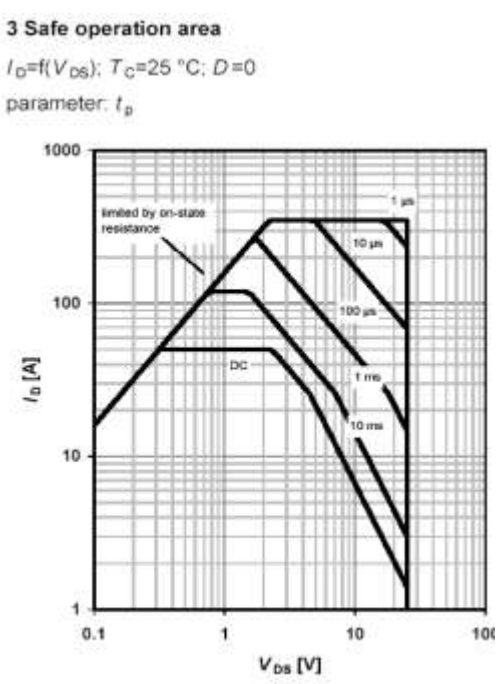


Figure 3

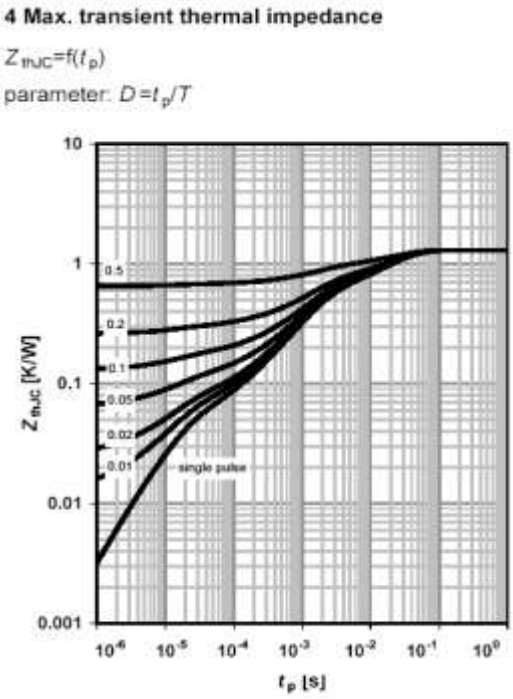


Figure 4

Figure 4 shows the thermal impedance of the MOSFET. In order to maintain the junction temperature below T_{jmax} a thermal impedance Z_{thJC} of less than 17 mK/W is required (equation 1).

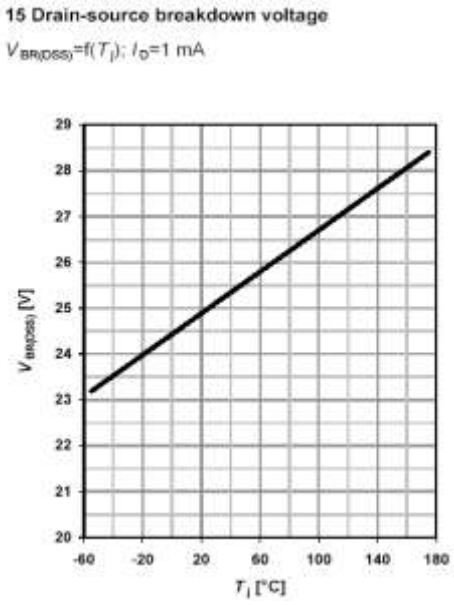
$$Z_{thJC} = \frac{T_{j\max} - T_a}{P_{tot}(1\mu s)} = \frac{(175-25)°C}{8.75kW} = 17.14\frac{mK}{W} \qquad \textbf{(1)}$$

A look into the diagram for the maximum transient thermal impedance shows a value of about 3.2 mK/W for a pulse duration of 1 µs. Compared to the required thermal

impedance this value is less than a fifth. Also here it can be seen that the specification given in the datasheet provides already a safety margin to guarantee the operation.

Avalanche

Another important parameter given on the first page of the datasheet is the single pulse avalanche energy. For the IPD04N03LA this energy is 890 mJ for an avalanche current equal to the nominal drain current of 50 A. This amount of energy is over 100 times compared to the previously described over current events. The reason for that during an avalanche event the MOSFET is blocked completely. The drain-source voltage has exceeded the blocking capability of the MOSFET. This leads to a huge power spike which can be withstand only for a short time. In that short time the thermal impedance is mainly defined by the die itself and is very small permitting this higher energy compared to the previous investigation for linear operation.



Under datasheet conditions the applied voltage is $V_{(BR)DSS}$ plus a safety margin according to manufacturing tolerances given by the MOSFET manufacturer. The customer should not expect the device to have a safety margin for the breakdown voltage. Nevertheless the breakdown voltage characteristic can be taken into account when designing the circuit. Figure 5 gives the behavior of the breakdown voltage over the junction temperature. This behavior is inherent all MOSFETs. Having a higher junction temperature is not favored for a low on-resistance of the MOSFET. On the other hand the breakdown voltage increases as sure as the on-resistance does. This is additional headroom for appearing spikes caused by e.g. parasitic inductances.

Figure 5

The MOSFET is operating within the $V_{(BR)DSS}$ specification when the drain-source voltage is $V_{(BR)DSS}$ or less. If the MOSFET is operating at maximum junction temperature the related $V_{(BR)DSS}$ can be taken out of figure 5. In the case of the IPD04N03LA it would be a voltage of 28.4 V. This value is 13.6 % above the 25 ˚C value and can be taken into account during the design process of the circuit.

Summary

Figure 6 shows the resulting consequences for the device choice considering the temperature dependencies.

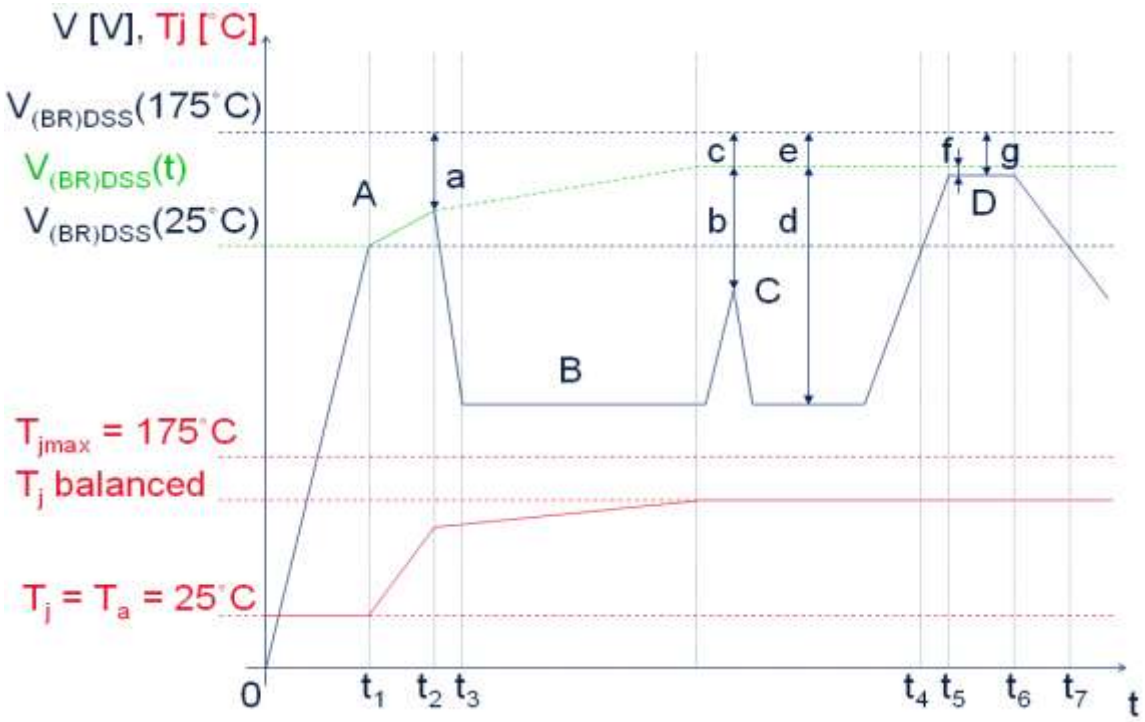


Figure 6

The case "A" represents a single pulse avalanche event after the circuit was activated. It can be seen how the breakdown voltage of the MOSFET increases during the avalanche event resulting out of the dissipated avalanche energy. At the end of the avalanche event the breakdown voltage is still far below (a) the expected value for T_{jmax}.
During the phase "B" the junction temperature rises until is has become a steady state. The safety margin for this event is now given by "d" without consideration of avalanche cases. Including avalanche the safety margin is represented by "e".
Analogous an appearing voltage spike "C" can be considered to have a headroom of "b" without avalanching or "c" with avalanching.
The steady operation of the MOSFET can be even beyond $V_{(BR)DSS}$(25 ˚C) like shown in case "D". Since the $V_{(BR)DSS}$ of the MOSFET has reached a higher level (green limit line) the MOSFET doesn't work in avalanche. The safety margin here is given by "f". If the power dissipation increases further the breakdown voltage rises up to the level of $V_{(BR)DSS}$(175 ˚C). The margin here is given as "g".

Customer Policies

Usually a design engineer is the bridge between the circuit requirements and the purchasing department. For a given on-resistance the MOSFET with the lowest breakdown voltage possible is the best choice since its chip size is smaller and the costs are expected to be lower too. What is now the lowest breakdown voltage possible? Beside all the technical explanations for waveforms some vendors have a very strict policy to say that the highest occurring voltage in the circuit (time independently) may never exceed a certain percentage (e.g. 80 %) of the $V_{(BR)DSS}$ of the MOSFET. The circuit designer usually takes the datasheet value for 25 ˚C and checks if the breakdown voltage is within the permitted range. That means in return that the MOSFET (which is operating under real conditions for example at T_j = 120˚C) provides a much higher safety margin than required. For the device example IPD04N03LA that would be an additional safety margin of 8.8 %. Furthermore the avalanche capability is often considered to be not present. By doing so the breakdown voltage for the chosen MOSFET is far beyond the requirements.
In order to avoid misunderstandings it should be mentioned here that conservative designs generally are the right way. An 80 % limit for the breakdown voltage can be considered to be as very conservative. If on top of that the MOSFET inherent safety margin, caused by the device operating temperature and avalanche capability, is there in addition, then the target has been exceeded by far. Consequently the circuit performance drops and the device expenses will increase.

Conclusions

The datasheet parameters Infineon as a MOSFET manufacturer gives in its specifications are already conservative in terms of device reliability. All the parameters are given under certain conditions. They are valid until the MOSFET has reached the so called end of life. Since Infineon provides its products also for automotive applications the ruggedness has to be inherent and the parameters in the datasheet have to have a very high confidence level. If a customer decides to use only a certain percentage of the device capability then it should be considered to take the 100 % value from the real operating conditions including avalanche capabilities and not from the 25 ˚C value. The application then provides still the calculated safety margin for the device but as a customer you will get a performance benefit e.g. by choosing a lower breakdown voltage.