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Synchronous Rectified Buck MOSFET Driver IC

Drivers

PX3517

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Table of contents

Revision History 3
Table of Contents 4
1 Introduction 5
2 Theory of Operation 6
3 Current Capability and Internal Bootstrap 9
4 Power Dissipation 10
5 Inputs to the Internal Control Circuits 11
6 Thermal Protection 12
7 Layout Considerations 14
8 Performances 17

Table of Figures

Figure 1 Simplified block diagram 7
Figure 2 Application Circuit 14
Figure 3 Picture of a 5 phases board 15
Figure 4 Top view 16
Figure 5 Bottom view 16
Figure 6 Efficiency results 17
Figure 7 Turn off 18
Figure 8 Turn on 19

1 Introduction

The PX3517 is a dual, high speed driver designed to drive a wide range of high side and low side n-channel power MOSFETs in synchronous rectified buck converters. When combined with the Primarion family of Digital Multi-phase Controller ICs or Digital Point of Load Controller ICs and Infineon n-channel MOSFET products, the PX3517 forms a complete core-voltage regulator solution for advanced micro and graphics processors as well as point-of-load applications.

The pins VCC and PVCC can be tied together and supplied by a voltage ranging between 4.5V and 8V. They can be separated for better noise decoupling of the logic section (VCC) from the power section (PVCC). They can also be supplied with different voltages, but in this case the appropriate power up sequence has to be implemented. PVCC provides the capability of driving the high side MOSFET gate and low side MOSFET gate with a variable gate driving voltage to tailor efficiency based on customer conditions. The device embeds the bootstrap diode for the high side MOSFET floating driver.

Adaptive shoot-through protection is integrated into the IC. This prevents both upper and lower MOSFETs from conducting simultaneously and minimizes dead time.

The device offers the possibility to be synchronized up to 1.2 MHz with an external PWM signal which implements also a tri-state functionality setting the both MOSFETs in OFF state. The PWM pins have a built in resistor divider which have the function so set the voltage of the PWM inside the tri-state window to avoid any fault condition in case the pin is left floating. The value of the divider is selected compromising two criteria: from one side the resistor divider is creating a consumption that might affect the low load efficiency or stand by requirements, for this reason the network should be planned with high resistances; on the other side the reaction time of the PWM can be in some cases influenced by these resistances and the parasitic capacitance related to the pin /trace from controller to driver. In this case a low value resistance is desirable.

The high sink/source currents capability, for both high side and low side sections of the driver, allows the device to switch very low $R_{DS(on)}$ MOSFETs (generally showing an high input capacitance value), permitting the design of a high output current (up to 50A) single phase buck converter. The high side driver, through the high sink/source current capability (ISRC_UG, ISNK_UG), has the capability to switch relatively high capacitance MOSFET in few ns time making the device suitable also for balanced duty ratio application (for example 5V down to 3.3V). The low side driver sink impedance (RSNK_LG) is designed to be very low in order to ensure the OFF state of the low side MOSFET during the turning on of the high side MOSFET; in fact during this transition high dv/dt on the drain of the low side MOSFET can be coupled through the CRSS to the gate of the low side MOSFET resulting in an induced turn on. In case low $R_{DS(on)}$ MOSFETs are used in the low side section, then the capability to turn on the low side MOSFET quickly is also extremely important to reduce the dead time; this is the reason for the high current capability of the source section of the low side driver (ISRC_LG).

The low thermal resistance junction to solder point (θJS) (bottom exposed pad) secures a good thermal path to the PCB. This good connection to the PCB is very important to decrease the self heating of the driver due to the MOSFET gate charge related losses that might be significant in case of multiple low side MOSFETs used.

A thermal warning function with an adjustable threshold, set by an external resistance, is featured to protect the system from thermal issues. Once the junction temperature of the PX3517 encounters the thermal warning threshold the driver outputs a logic signal through the open drain THW# pin.

2 Theory of Operation

The PX3517 functionality is enabled by the VCC pin. When the VCC pin voltage overcomes the VCC rising voltage threshold (VUVLO_R), the driver begins to operate depending on the PWM status. Before the VCC pin voltage reaches the VCC rising threshold both MOSFETs are kept in the OFF state. For VCC is recommended to have a slope for the rising edge higher than 5V/100ms around the rising UVLO threshold. The PX3517 functionality is driven by PWM signal transitions. When the PWM signal performs a transition from low state to high state (PWM voltage higher than 2.5V typ) the low side MOSFET is turned off, after the turn off propagation delay time. Next the high side MOSFET is turned on, after the turn on propagation delay time. Once the on time has expired, the PWM signal provides a transition from high state to low state (PWM voltage lower than 0.8V typ). This will drive the high side MOSFET from the ON state to the OFF state, after the turn off propagation delay time. The PX3517 is also capable of driving two external MOSFETs into the OFF state. When the PWM signal level enters the shut down window or tri-state (typically between 1.2V and 2V), after the shut down hold off time has expired, both MOSFETs are switched off. This feature is useful when the IC controller wants to reduce the number of active phases in order to decrease power consumption. In principle the tri-state can also be used to improve performance during transitions between heavy and light loads.

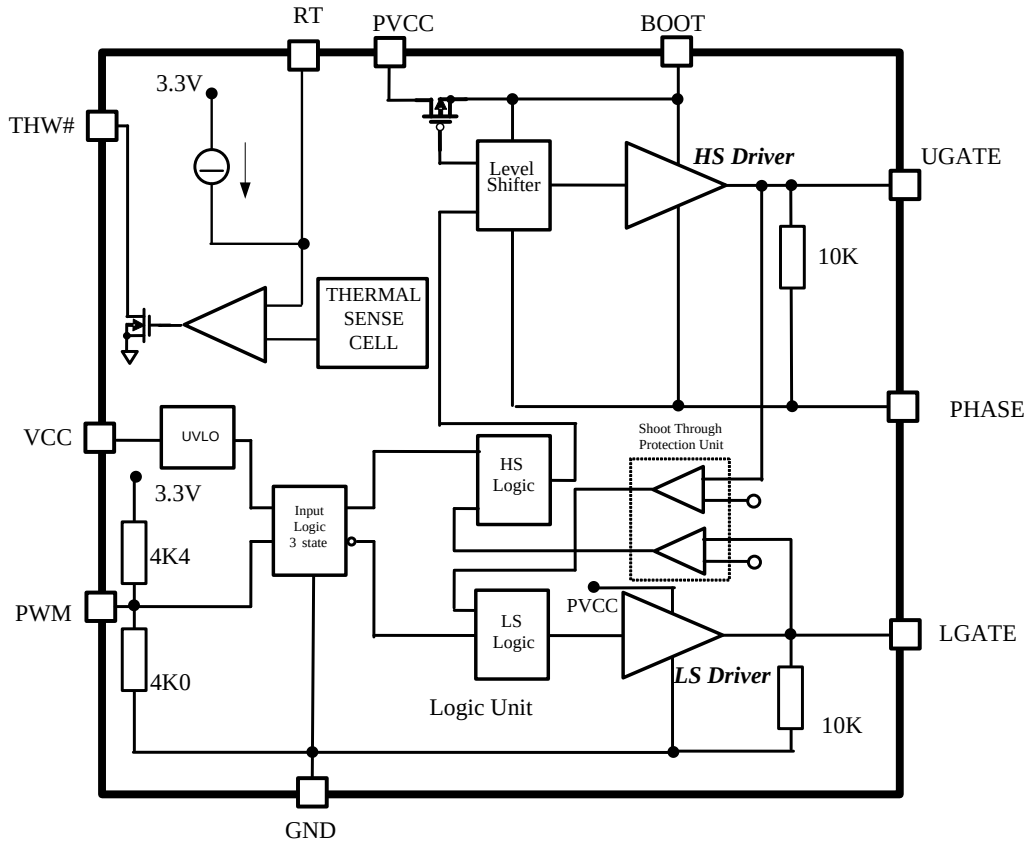


Figure 1 Simplified block diagram

The PX3517 implements an embedded resistor network, which forces the PWM pin voltage of the device into the middle of the shut down window if the PWM input is left floating by the controller IC.

An adaptive anti-shoot-through control scheme is implemented in order to avoid cross conduction between the high side MOSFET and the low side MOSFET. This adaptive scheme allows the use of a variety of different power MOSFETs for different kinds of power conversion. Nevertheless, the dead time is kept as short as possible in order to maximize the efficiency of the overall solution.

The adaptive cross conduction protection is based on the gate-to-source voltage level of the MOSFETs during turn off. When the PWM signal goes low, the high side MOSFET will begin to turn off. Once the VGS of the high side MOSFET is discharged below 1V, the low side MOSFET will begin to turn on.

When the PWM signal goes high, the low side MOSFET will begin to turn off. Once the VGS of the low side MOSFET is discharged below 1V, the high side MOSFET will begin to turn on.

There is an additional control mechanism on the PHASE pin that forces the turn on of the low side MOSFET if the PHASE pin is not actively held high. This ensures that the converter will sink current efficiently, and that the bootstrap capacitor will be refreshed appropriately during each switching cycle.

During start up it is possible for the 12V conversion input to rise before the 5V input. In this case, the high side MOSFET can have an induced turn on through the CGD/CGS partition. In order to avoid this undesirable effect the PX3517 embeds a resistance of 10kΩ between UGATE pin and PHASE pin. The value of these resistances is selected keeping in mind two different trends: in order to keep the impact of the consumption related to the resistances low for low load efficiency, the value should be as high as possible. In order to make the protection effective the value should be as low as possible. A range of 10K seems to be a reasonable mix between these two opposite trends.

The gate driver of the PX3517 has 2 voltage inputs, VCC and PVCC. VCC is the logic supply for the driver. PVCC is used to drive the high and low side MOSFETs. Ceramic capacitors should be placed very close to these input voltage pins to decouple the sensitive control circuitry from a noisy environment.

Since two different pins are provided for supplying the power to the driver, the correct power up sequence has to be considered. In order to avoid false turn on of the gates (spurious high side turn on, for instance) it is strongly suggested to ensure that the voltage at the VCC pin reaches the UVLO threshold earlier than the PVCC pin. In this way the logic section will ensure the correct functionality of the power section.

Due to the presence of an internal regulator that is generating the 3.3V it is also strongly recommended to avoid applying voltage to the PWM pin at the start up before applying voltage to the PVCC and VCC pins.

Considering all the above suggestions the suggested power up sequence in case PVCC and VCC are not tied together, is:

VCC

PVCC

PWM

The MOSFETs selected for this application are optimized for 5V gate drive, giving the end user optimized efficiency at both high load and light load. Nevertheless the driving voltage (PVCC) can be increased, (independently from VCC), up to 8V in order to have a customized efficiency curve depending on application conditions. The reference for the power circuitry including the driver output stage and the reference for the gate driver control circuit is CGND.

Referring to the block diagram in **Error! Reference source not found.** on page 7, VCC is internally connected to the UVLO circuit. For VCC voltages less than the 3.6V (typ.) required for proper circuit operation, the UVLO circuit will perform a system shut-down. PVCC supplies both the floating high side MOSFET driver and the low side MOSFET driver circuits. An active boot circuit for the high side MOSFET

gate drive is also included. A second UVLO circuit, sensing the BOOT voltage level is implemented to prevent false UGATE turn on during insufficient power supply level conditions (BOOT Cap charging/discharging sequence). During such an undervoltage condition both UGATE and LGATE are driven low actively. Further, a passive pull-down (10kΩ is placed on each gate).

The PX3517 features adjustable thermal warning protection. The thermal warning trip point ranges from 70°C to 130°C and is selected according to a resistance between the RT pin and GND pin. An embedded thermal sense element senses the driver temperature and compares it to the trip point. Once the two temperatures match, a logical signal is issued by the THW# pin. In this case the driver system does not shut down. The thermal warning has a hysteresis of 10°C. Once the temperature reaches the threshold determined by the external resistance, the THW# will be de-asserted if the temperature drops below the threshold by 10°C.

3 Current Capability and Internal Bootstrap

The PX3517 implements high current capability and low ohmic pull down resistances for the driving stages. The high current capability ensures fast switching transition for the MOSFETs. This reduces the switching losses (2A of driving source/sink current for the upper MOSFET) even with high gate charge high side MOSFETs. The low ohmic pull down resistance (lower drive sink impedance 0.35Ω) prevents the induced turn on phenomenon of the low side MOSFET during the fast turn on of the high side MOSFET.

The high side MOSFET is powered through the bootstrap circuitry. The PX3517 provides an embedded bootstrap diode, so to complete the power network only a capacitance between the PHASE pin and the BOOT pin is needed. In many cases the PX3517 is optimized for the best switching behavior, so an external resistance is not needed. The bootstrap capacitance is chosen depending on the high side MOSFET gate charge. The following formula gives a good estimation of the voltage drop across the bootstrap capacitance due to the charging of the high side MOSFET.

$$C_{BOOT} > {QG_{HS}}/{\Delta V_{BOOT}}$$

DVBOOT is the desired variation of the bootstrap voltage. This should generally be as low as possible in order to avoid high side MOSFET $R_{DS(on)}$ drop. Generally, a value between 0.1V and 0.01V is acceptable.

The low side MOSFET driver is powered through the PVCC pin. The same considerations and formula for the bootstrap capacitance can be applied to the capacitance used to filter the PVCC pin.

The flexibility to adjust the driving voltage from 4.5V to 8V gives designers the capability to shape the efficiency curve in any way that is desired.

4 Power Dissipation

The power dissipation of the driver is mainly given by the gate charge of the external power MOSFETs. The following formulas held:

$$P\_DISS = P\_VCC * f\_SW * (Q\_(GS\_HS) + Q\_(GS\_LS))$$

fsw is the switching frequency and QGHS and QGLS are respectively the gate charge of the high side MOSFET and the gate charge of the low side MOSFET at the PVCC driving voltage.

For instances considering a buck converter application with one high side MOSFET (BSC050NE2LS) one low side MOSFET a driving voltage of 5V and a switching frequency of 500KHz the power dissipation results:

$$P\_DISS = 5[V] * 500[KHz] * (5[nC] + 29[nC]) = 85mW$$

A small contribution can be given also from the driver itself. At 300KHz switching frequency the power dissipation due to the driver is in the range of 10mW. This power dissipation is given by the IPVCC_300kHz multiplied by the driving voltage (5V).

The very low thermal resistance package junction to solder point used for the PX3517 allows the device to avoid any usage of external resistances to decrease the power dissipation inside the driver even with high driving voltage. The thermal resistance needed for the determining the increased of temperature due to the power dissipation is not related to the package only, but it is necessary to consider also the PCB board. In this case the thermal resistance junction to ambient (θJA) depends strongly on PCB characteristics: how many layers, thickness of the copper used etc etc. A standard PCB layout which addresses power conversion application has generally two or more layers with at least 1 Oz copper and a big area dedicated to the GND connection; if all the characteristics expressed before are satisfied, most likely the θJA will be already in the range of 20 K/W. Assuming such a rough estimation real it can be seen, the increase of the temperature due to the self power dissipation is negligible.

$$\Delta T = \theta\_JA * P\_DISS$$

$$\Delta T 20\left[\frac{K}{W}\right] * 0.085[W] = 1.7\ [K]$$

5 Inputs to the Internal Control Circuits

The PWM is the control input to the IC from an external PWM controller IC and is compatible with 3.3V.

The PWM input has tri-state functionality. When the voltage remains in the specified PWM shutdown window for at least the PWM shutdown holdoff time t_tsshd, operation is suspended by keeping both MOSFET gate outputs low. If left open, the pin is internally fixed to VPWM_O = +1.6V level.

During the power-up sequence, the initial state of the PWM signal is ignored, until the first rising edge.

Since all the thresholds are derived from an internal linear regulator they will not depend on the VCC input.

PWM logic level	**Driver output**
Low	LGATE= High, UGATE = Low
High	LGATE = Low, UGATE = High
Open (left floating, or High impedance)	LGATE = Low, UGATE = Low

Table 1 PWM Pin Functionality

6 Thermal Protection

The THW# pin offers the possibility to check when the temperature of the driver overcomes the threshold fixed by the RT pin resistor. Once the temperature of the driver matches the trip point this open drain output (pulled up to 3.3V by, for instance, an external resistance in the range of 10kΩ) is pulled to zero (active low) with a typical resistance of 37Ω. When the temperature of the device goes below the thermal warning minus the hysteresis (10°C typ), the pin THW# is released and pulled up by the external resistance. If the thermal warning is not used, then leave the pin floating. The thermal warning protection does not switch off the driver.

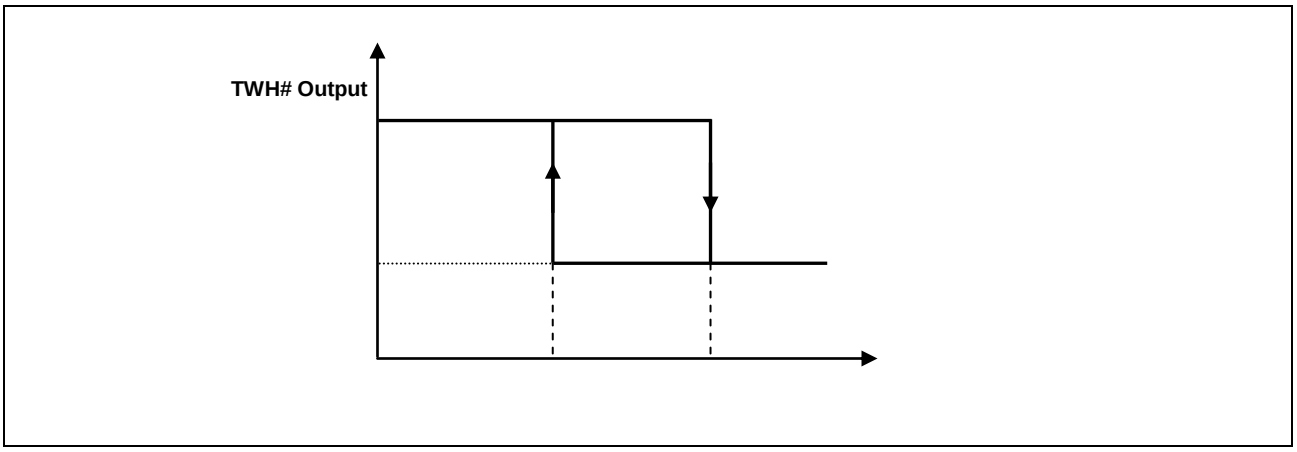


Figure 1 Thermal warning

The RT pin provides the option to program the trip point of the thermal warning as follows:

$$r\_RT\ (\Omega) = 248 * (T - 70) + 82{,}000\Omega$$

T is the desired warning temperature. If the threshold is fixed to T=100°C then the □T is 30°C and external resistance is equivalent to 89.5k□, as shown in the following table.

Desired warning temperature [°C]	Resistance connected to the RT pin [□]
70	82000
80	84400
90	87000
100	89500
110	92000
120	94400
130	96880

The adjustability of the thermal warning should compensate the fact that the sensing point on the driver can be slightly different from the hot spot of the application. In this case a gap between the temperature of the hot spot and the temperature of the driver can be measured and then the thermal warning can be designed with an offset to compensate for the difference.

Another important detail for a correct use of the thermal sense as protection is the thermal dependency of the resistance used in the RT pin; in order to achieve higher accuracy a resistance with a very low thermal coefficient (0.1%-1%) should be used. This detail is very important due to the fact the resistance, due to the small area in the layout dedicated to the driver, might be effected by the same temperature increases the driver is effected.

In order to have better temperature matching it is strongly recommended to connect the GND exposed pad of the driver as near as possible to the hot spot; depending on the application condition and the MOSFETs package used this might be easy or complicated. For instances, considering a reasonable power losses distribution between high side MOSFET and low side MOSFET and CanPAK™ package (like BSF035NE2LQ; BSB012NE2LXI, the placement of the driver on the bottom side of the board with shared GND pad with the source pin of the low side MOSFET seems to meet the requirements for the best thermal coupling. In this case is very important to have a direct connection with thermal vias or filled vias. In the case of SuperSO8 package (BSC050NE2LS; BSC010NE2LSI) the placement of the driver might be more difficult and the thermal coupling might be less effective due to the not direct connection between the >GND pad of the driver and the die of the MOSFET. It is important to note that generally the protection of the low side MOSFET is easier due to the sharing of the source pin with the GND pad of the driver; the protection of the high side MOSFET is more complex due to the absence of shared power connection between high side MOSFET and driver.

7 Layout Considerations

The PX3517 has a good protection system against unwanted overshoot and undershoot; even the static maximum input voltage is 16V the PHASE pin can range between dynamically from -8V to 25V (10ns) allowing the designer a further margin in terms of spikes at that pin.

The parasitic inductances of the PCB and of the power devices' packaging (both upper and lower MOSFETs) can cause serious ringing, exceeding absolute maximum rating of the devices. Careful layout can help minimize such unwanted stress. The following advice is meant to lead to an optimized layout:

1. Keep decoupling loops (PVCC-GND and BOOT-PHASE) as short as possible. (orange and yellow squares).
2. Minimize trace inductance, especially on low impedance lines. All power traces (UGATE, PHASE, LGATE, GND, PVCC) should be short and wide, as much as possible. (red lines)
3. The PHASE node should also be short and wide. Minimize the distance between the PHASE node and both the high side MOSFET source and the low side MOSFET drain to avoid efficiency losses. (red line)
4. Minimize the current loop of the output and input power trains. Short the source connection of the lower MOSFET to ground as close to the transistor pin as feasible. Input capacitors (especially ceramic decoupling) should be placed as close to the drain of upper and source of lower MOSFETs as possible.

To optimize heat spreading, copper should be placed directly underneath the IC whether it has an exposed pad or not. The copper area can be extended beyond the bottom area of the IC and/or connected to buried copper plane(s) with thermal vias. This combination of vias for vertical heat escape, extended copper plane, and buried planes for heat spreading allows the IC to achieve its full thermal potential.

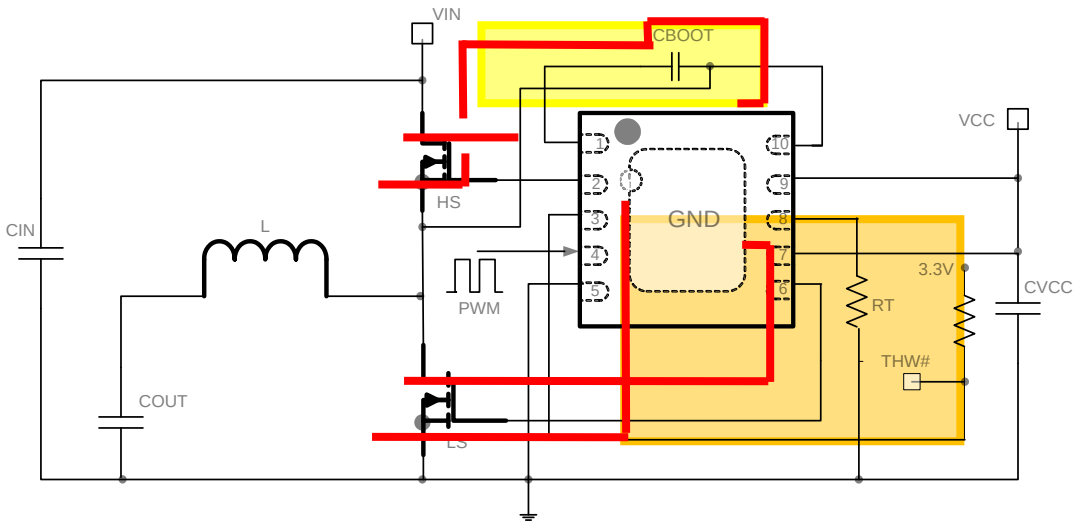
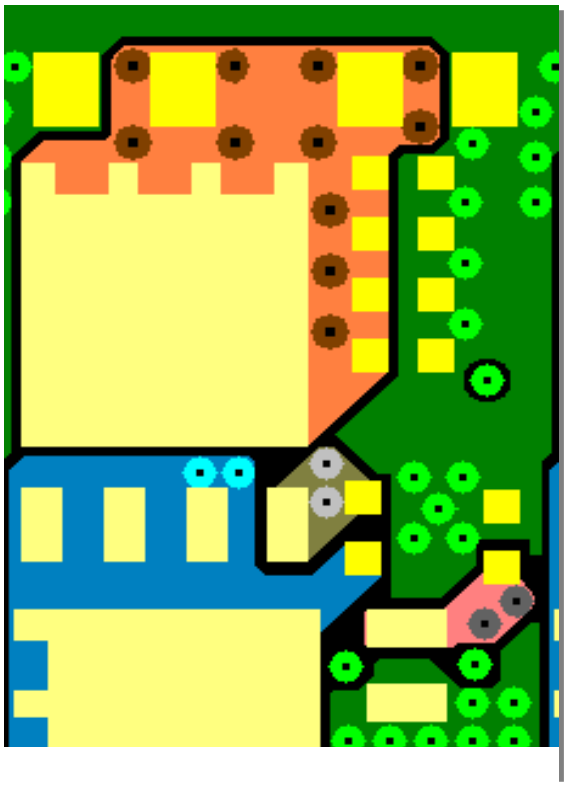


Figure 2 Application Circuit

In the pictures 1 and 2 a partial layout example with SuperSO8 high side MOSFET and low side MOSFET is shown; the relevant expected above mentioned are visible in the two pictures: in particular the phase connection of the driver is as near as possible to the source of the high side MOSFET and in order to improve reliability and parasitic inductance of the connection itself the vias are doubled. Same observation for the gate connections (high side and low side MOSFET), which have double vias.

The two decoupling capacitances for VCC and PVCC, together with the BOOT capacitance, are placed on the bottom side where also the driver is. In order to have a very good thermal coupling and a very small parasitic inductance with the low side MOSFET, 5 vias are used to connect the exposed pad of the driver to the GND which ultimately is the source of the low side MOSFET.

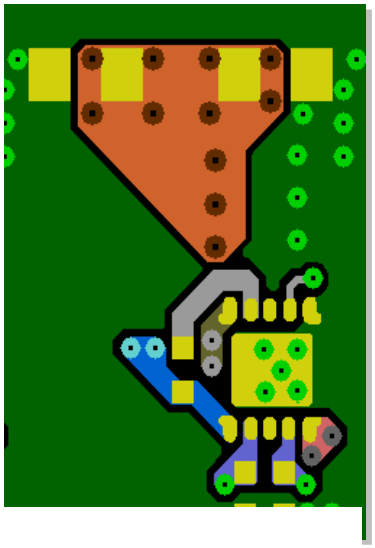
Figure 3 Picture of a 5 phases board



Colors Legend

Orange	→ Input voltage
Green	→ Ground
Blue	→ Phase Node
Brown	→ Gate connection for high side MOSFET
Pink	→ Gate connection for low side MOSFET

Figure 4 Top view



Colors Legend

Orange	→ Input voltage
Green	→ Ground
Blue	→ Phase Node
Brown	→ Gate connection for high side MOSFET
Pink	→ Gate connection for low side MOSFET
Grey	→ Boot connection

Figure 5 Bottom view

8 Performances

The performance of a buck converter are strongly depending on many factors, layout board composition (how many layers, thickness of the layers) and MOSFET technology. Each one of this factor can play a fundamental role in determining the final performance of the converter. It is enough to not optimize one of this factor to degrade the efficiency of several percent.

In this paragraph a collection of results is presented to show the capabilities of the PX3517 in terms of efficiency, dead time and rise time fall time.

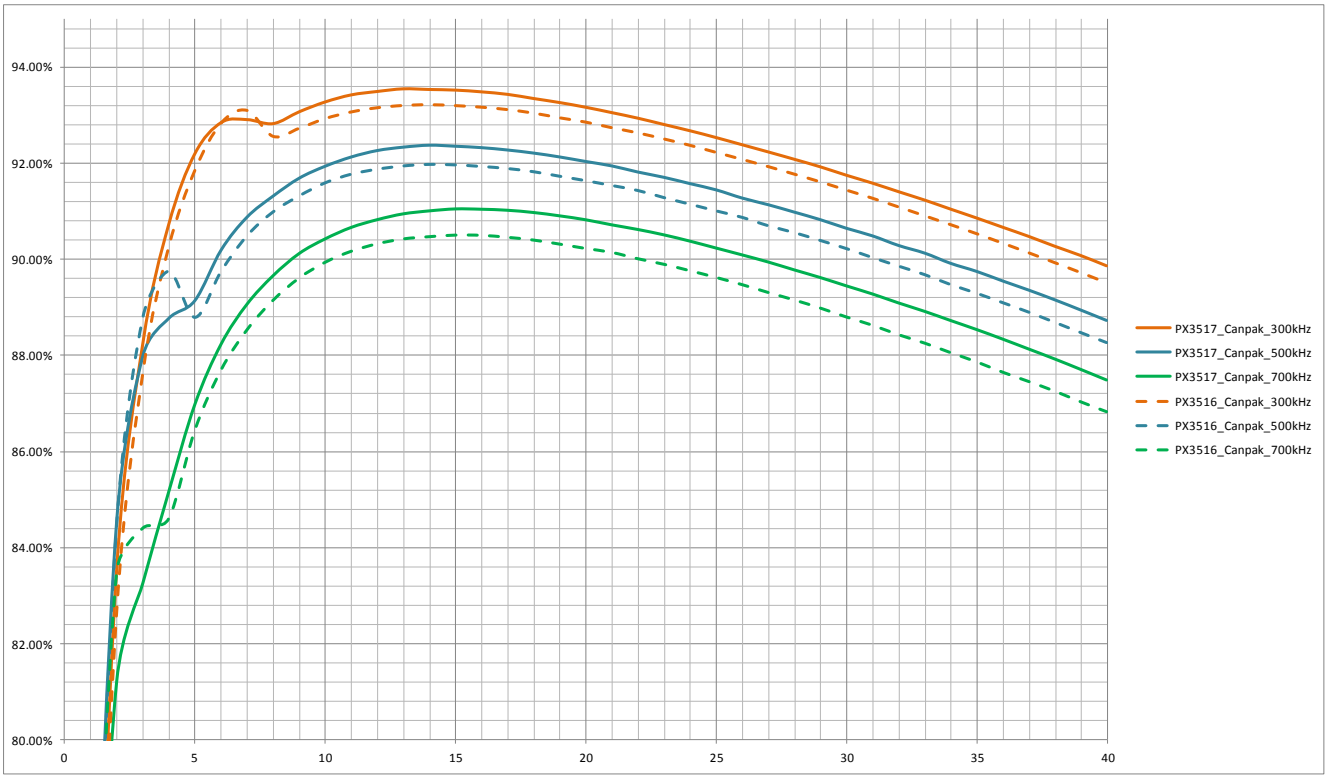


Figure 6 Efficiency results

Efficiency in different conditions are shown in picture 3 for different switching frequency. Depending on the conditions the peak efficiency can be up to 94% and full load up to 90%

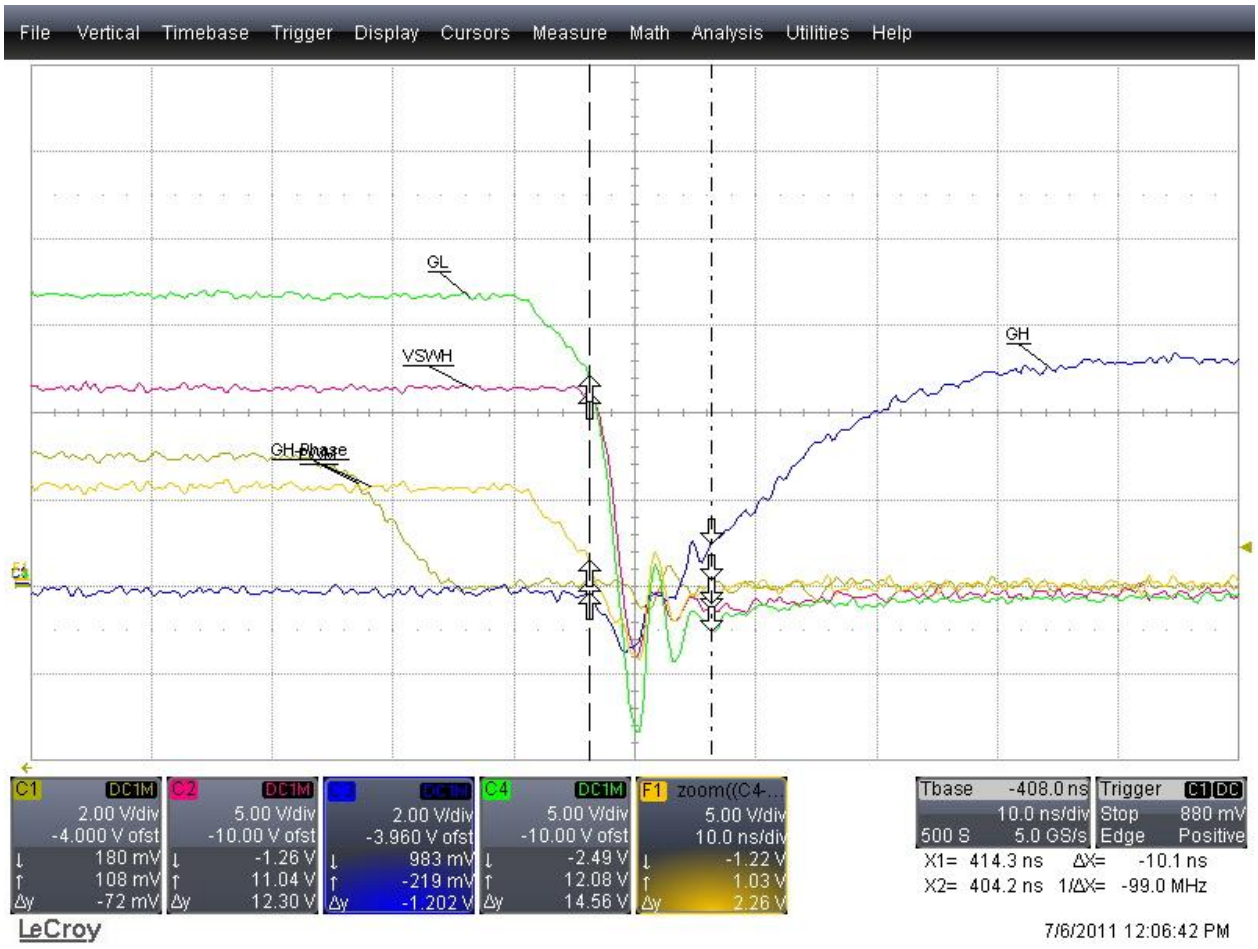


Figure 7 Turn off

As it is shown in the picture 4 the transition time from high side on to high side off and low side on is very small. The falling edge of the VSW pin is in the range of 4 ns meanwhile the time required to switch of completely the high side gate is in the range of 6ns.

Identify the dead time between high side MOSFET off and low side MOSFET on from the VSW/PHASE node might be difficult due to the noise; the reference is given by the low side MOSFET gate signal, when it overcomes the 1V value. In this case the dead time can be evaluated in around 6ns.

The transition from low side MOSFET on to high side MOSFET on is shown in picture 12. In this case the rising edge of the VSW/PHASE node is in the range of 4ns. The duration of the dead time is more in the range of 10ns considering when the low side gate crosses the 1V threshold. During the rising edge of the high side MOSFET a spike can be seen on the low side MOSFET gate. This spike is generally understood as sign of induced turn on (low side is turned on by the CGD/CGS coupling during the fast dv/dt of the VSW/PHASE node). Most of the time the spike on the gate is nothing else than a spike due to the parasitic

inductance of the package or trace connection. In other words the spike is not translated immediately in a spike on the VGS of the low side MOSFET.

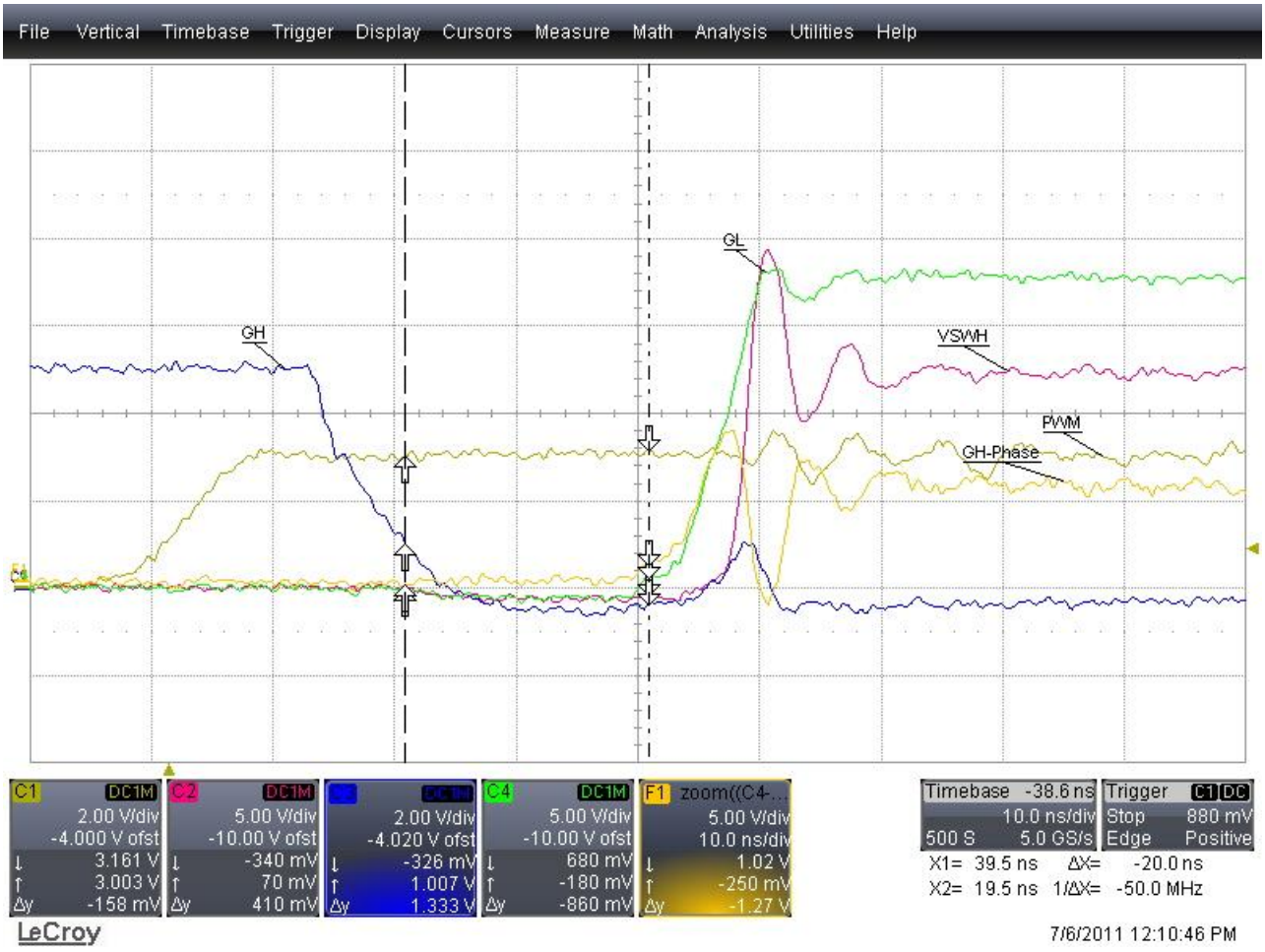


Figure 8 Turn on