OptiMOS™ device selection for synchronous rectification

Application Note

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About this document

Scope and purpose

This application note discusses secondary-side synchronous rectification (SR) in different switched-mode power supply (SMPS) topologies and how to select suitable MOSFETs to be used for this purpose. In order to do this, the following factors are considered: conduction loss, body diode recovery loss, output capacitance loss and, gate driving loss. Different loss contributions according to whether the system operates in hard- or soft-switching at the secondary side and under different load conditions are also discussed.

A selection chart is introduced to provide a method for determining the best MOSFET and number of parallel devices required for a specific voltage, frequency and current. A set of selection charts is provided for a range of MOSFET voltages.

This application note replaces the original releases mentioned in references **[1]** and **[2]**, by replacing discontinued parts with current devices based on Infineon's improved technologies.

Intended audience

This document addresses the SMPS applications market, and is aimed at designers wishing to provide a highly efficient system solution as well as reduce system costs. It is intended for design engineers, applications engineers, and students.

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1 Introduction

The trend toward higher efficiency and power density requires the replacement of diodes with SR in switching power supply output stages. This overcomes the power losses produced by the forward voltage drop in traditional Schottky diode secondary-side rectifier implementations by replacing them with MOSFETs. **Figure 1** illustrates the basic principle of SR, in which a basic diode-based output rectifier for a forward converter or similar topology is shown in the upper circuit with the diodes replaced by MOSFETs in the lower circuit. In SR, the MOSFETs must be oriented such that the body diodes are in the same direction as the diodes being replaced. It should be kept in mind that the SR MOSFETs *do not block forward current* when they are switched off. Instead, the forward current passes through the body diode in this state. When the MOSFETs are switched on, the body diodes are bypassed to eliminate diode forward voltage power losses V_f x i_f, to be replaced with a much lower $R_{DS(on)}$ x i_f^2.

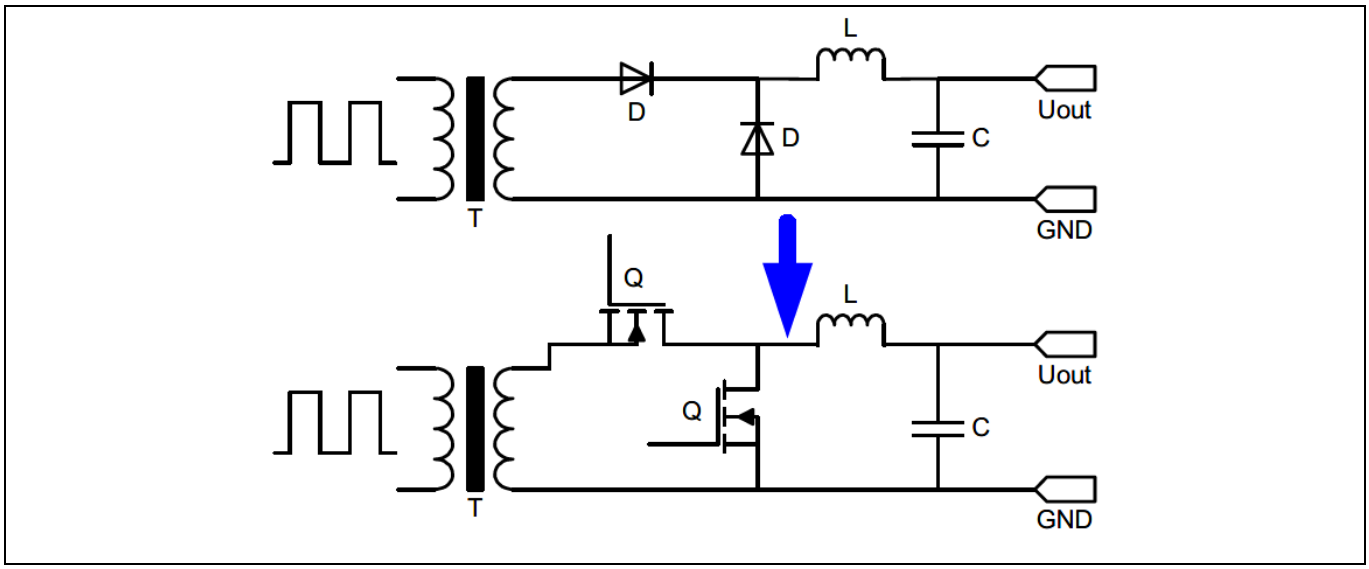


Figure 1 Diode vs. SR example in a forward converter

Since there are also losses relating to switching to consider, replacing rectifier diodes with MOSFETs leads to new challenges in optimizing system efficiency and controlling voltage overshoots. This application note provides guidance in MOSFET selection by using optimization charts containing the latest generations of Infineon's OptiMOS™ family of trench MOSFETs for 25 V, 30 V, 40 V, 60 V, 75 V, 80 V, 100 V, 120 V and 150 V BV_{DSS} ratings.

2 Basics of synchronous rectification

SR requires precise timing of the switch-on and switch-off of the MOSFETs, which must be synchronized with the switching of the primary-side MOSFET(s). Failure to do this can result in SR MOSFETs being on at the wrong time, allowing conduction of very high reverse currents likely to cause component failure. Different control schemes are used to provide the SR gate drive pulses, and these can be classified as follows:

1. Combined primary and secondary control
   In this implementation, one controller provides the gate drive for both primary and secondary switches. This may be a microcontroller or ASIC.

2. Independent secondary control
   In this implementation a secondary-side controller is used, which is not connected to the primary controller. The secondary controller senses the voltage and/or current signals on the secondary side to determine when to switch the SR MOSFET(s) on and off.

Furthermore, SR circuits containing more than one MOSFET must include dead times between the switch-on or -off of one MOSFET and the switch-on of the other to prevent shoot-through currents.

In order to select the best available MOSFET to design into a system for SR, the power loss mechanism needs to be well understood. First of all, the losses need to be distinguished between load-dependent conduction losses and frequency-dependent switching losses.

Conduction losses are determined by the $R_{DS(on)}$ of the MOSFET and the forward voltage of the internal body diode, V_{SD}. As the output current increases at higher loads, the conduction losses ($R_{DS(on)}$ losses) are also increasing. During the conduction phase of each SR MOSFET, the secondary current first passes from source to drain through its body diode for a short period of time until the MOSFET is switched on to divert the current through its channel. Toward the end of the conduction period the MOSFET switches off so that once again the current may be diverted through the body diode for a short time. The body diode conduction times are typically in the 50 to 100 ns range.

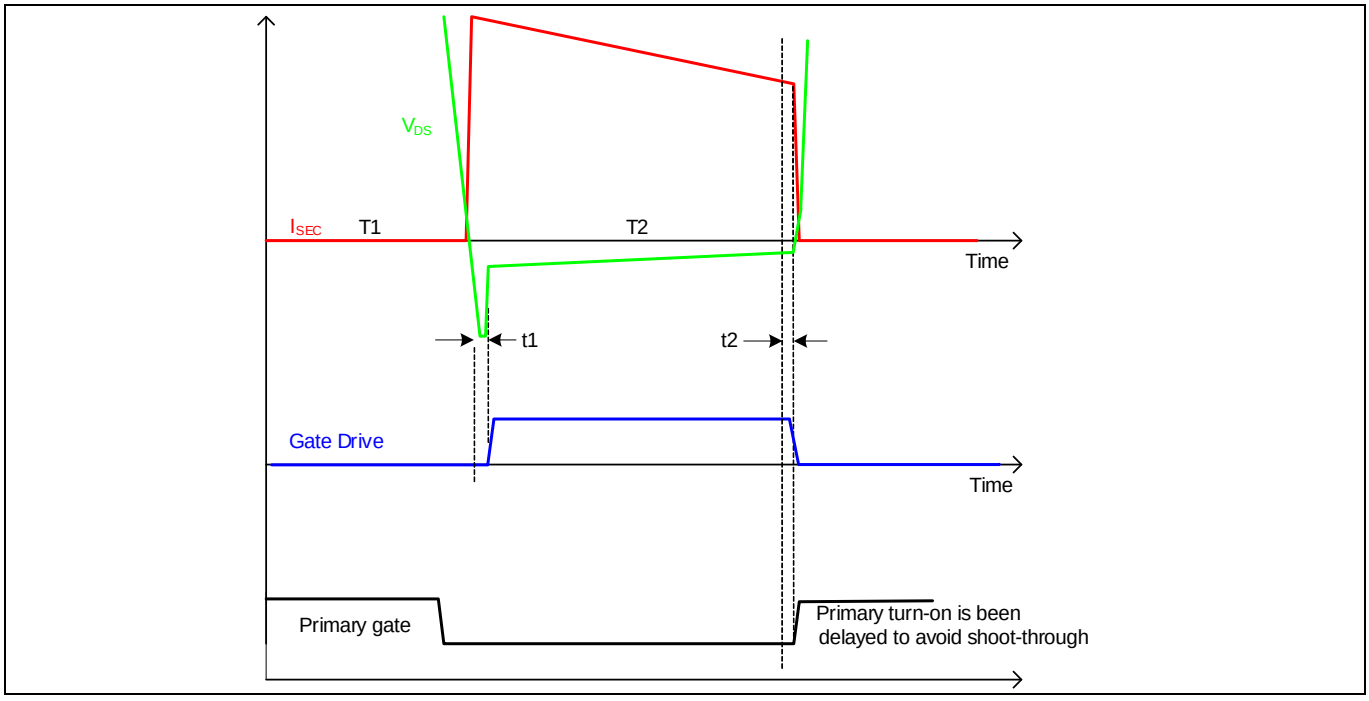


Figure 2 SR operating waveforms

Depending on the switching frequency (f_{SW}) and the output load (I_{OUT}) of the power converter, switching losses can have a large impact on the total MOSFET losses. For switch-on, the gate-to-source voltage V_{GS} is driven to around 10 V by supplying the gate charge Q_G. To switch the MOSFET off, the gate charge is removed, reducing V_{GS} to zero. The average current required for the gate drive is equal to Q_G x f_{SW}. Q_G is dependent on the MOSFET technology and die area, which means that devices with lower $R_{DS(on)}$ have higher values of Q_G in a given technology.

Another important portion of the total switching losses is related to the output capacitance C_{oss} and the reverse recovery charge Q_{rr} of the MOSFET. During turn-off, Q_{rr} must be applied before the body diode can block conduction, and the output capacitance is charged up to the secondary-side transformer voltage (V_T). This process results in a reverse current transient, which causes ringing oscillations due to the interaction of the circuit inductance from the PCB traces and MOSFET packages and C_{oss}. This oscillation gets damped by the series resistance in the circuit. Switch-off losses are proportional to MOSFET Q_{oss}, which is also related to die area. It is therefore necessary to select a device where a suitable trade-off can be made between conduction and switching losses to minimize the total SR losses.

For a first approximation, Q_{rr} can be neglected for OptiMOS™ products, as it makes a minor contribution to the total power losses. In this case Q_{rr} is considered as only the MOSFET body diode reverse recovery charge, whereas the Q_{rr} quoted in part datasheets is measured according to JEDEC standards and therefore includes not only the body diode Q_{rr} but also a part of the output charge of the MOSFET. In the application the Q_{rr} value may be lower than the datasheet value. This is because datasheet values are measured by applying a defined MOSFET drain current with the body diode conducting for a long period, up to 500 µs, where di/dt is fixed to a defined value.

In a real application, currents of about no more than a third of the maximum rated drain current are typically seen, and the body diode conduction time is in the range of 20 to 100 ns. However, di/dt can reach values of 800 A/µs.

3 MOSFET power loss analysis

3.1 Analyzing the turn-off behavior of the SR MOSFET

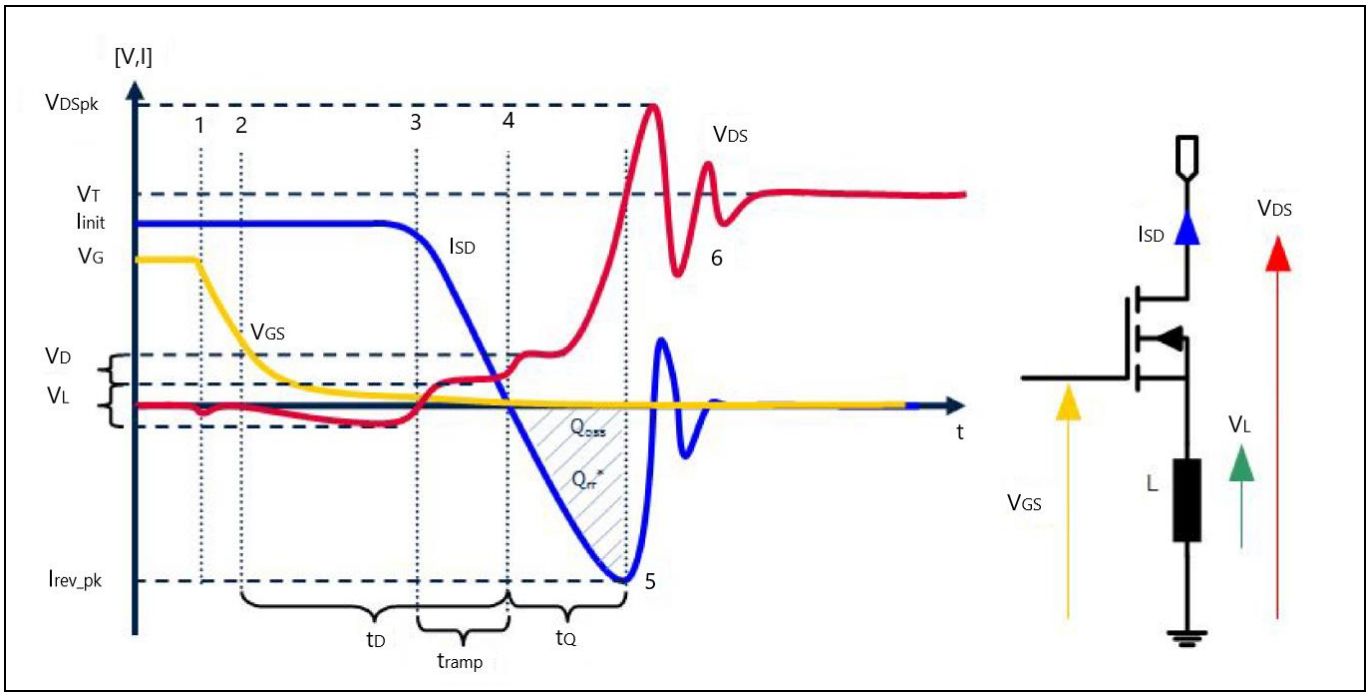


Figure 3 Turn-off behavior of the SR MOSFET with fragmentation in different switching points

The starting point for the analysis is the on-state of the switch. The gate voltage is at high level, the drain-source voltage is close to zero and a current is flowing from source to drain. At point 1 indicated in **Figure 3** the gate is turned off. This can also be seen in the V_{DS} waveform (indicated in red) in the form of a small negative voltage dip coming from the discharge of the gate input capacitance. This discharge produces a peak with a high di/dt in the source current of the MOSFET I_{SD} (indicated in blue) due to the inductive law:

$$V_L = -L \cdot \frac{di}{dt} \quad (1)$$

Inductance in the source creates a voltage drop in the V_{DS} waveform. At point 2 the MOSFET channel ceases conduction but nevertheless current continues to flow due to the output inductor. The current must commutate to the body diode of the MOSFET, resulting in a negative voltage drop V_D over the device; this period is indicated as t_D. After switching the primary side at point 3, the current has to ramp down. If the switching of the primary-side MOSFETs is fast, current commutation is limited by the secondary-side loop inductances, resulting in a constant di/dt. In this phase, indicated as t_{ramp}, a voltage drop caused by the source inductance of the MOSFET can be seen in the drain-source waveform, now transitioning into the positive direction due to negative di/dt. When the current crosses the zero line at point 4, current is no longer flowing through the body diode, and therefore the forward voltage drop across the diode becomes zero. This results in a further positive voltage drop at the V_{DS} waveform with the value of the forward voltage drop of the body diode V_D. After the zero crossing the current continues with the same di/dt but now in a negative direction, removing the reverse recovery charge Q_{rr}* of the body diode and charging the output capacitance C_{oss} of the MOSFET. In this case the Q_{rr}* is considered as the MOSFET body diode reverse recovery charge only, whereas the Q_{rr} specified in device datasheets is measured according to JEDEC standards and also includes part of the output charge of the MOSFET Q_{oss} besides the body diode Q_{rr}* (this will be further discussed). While the C_{oss} is being

charged, the voltage over the MOSFET begins to rise toward the transformer secondary winding voltage. At point 5, the maximum reverse current I_{rev_peak} is reached; this means that C_{oss} is now charged up to the transformer voltage. Ideally the system would now be stable; however, there is still energy in the system defined by:

$$E_{ind} = \frac{1}{2} L_{stray} \cdot I_{rev_{pk}}^2 \tag{2}$$

This inductive energy is now producing an LC oscillation circuit and forcing the stored energy in the stray inductances L_{stray} to be transferred to the output capacitance of the MOSFET and therefore producing the turn-off overvoltage spike. The LC circuit is comprised of the inductance of the transformer, the layout, the package and the MOSFET C_{oss}, as seen below:

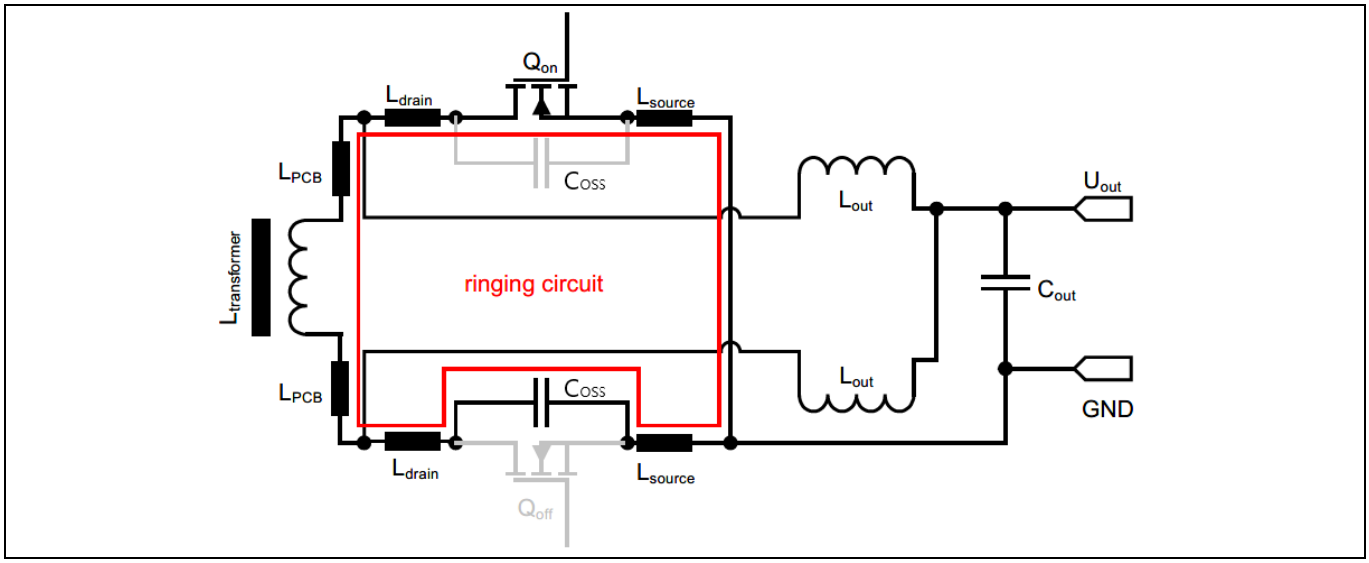


Figure 4 LC turn-off oscillation circuit elements in a current-doubler SR circuit

This circuit has an oscillation frequency of:

$$f_0 = \frac{1}{2\pi\sqrt{L_{stray}\, C_{oss}}} \tag{3}$$

Where:

$$L_{stray} = L_{source} + L_{drain} + L_{PCB} + L_{transformer} \tag{4}$$

These oscillations are damped by the parasitic resistances in the loop. The shape of the waveform described is only valid if the current commutation on the secondary side is inductively limited. This means the di/dt is not limited by the switching speed of the primary-side MOSFETs but by the stray inductances on the secondary side of the power supply.

3.2 Development of a power loss model

For the design of a high-efficiency power supply using SR, it is necessary to know exactly where the power losses in the SR MOSFET are generated. In the following, all important sources of power losses are identified based on ideal MOSFET switching behavior.

Conduction losses are defined by the $R_{DS(on)}$ of the MOSFET. The calculation can be done with the following formula:

$$P_{cond} = I_{RMS}^2 \cdot R_{DS(on)} \quad (5)$$

Here the I_{RMS} is the trapezoidal current through the MOSFET, not the output current of the converter. To ensure synchronization between the two SR MOSFETs necessary to avoid a current shoot-through, sufficient dead time must be inserted. The corresponding MOSFET therefore has to be switched off before the primary side is turned on. This causes the current to commutate from the MOSFET channel to the MOSFET body diode, which can be seen in a negative drain-source voltage drop. The time period is the body diode on time t_D. The calculation of the diode power loss can be done by using following parameters: forward voltage drop of the body diode V_D, the source-to-drain body diode current I_{SD}, the body diode on-time t_D and the converter switching frequency f_{SW}:

$$P_{diode} = V_D \cdot I_{SD} \cdot t_D \cdot f_{SW} \quad (6)$$

Gate drive losses of the SR MOSFET are defined by the gate charge Q_G, the gate driving voltage V_G and the switching frequency f_{SW}:

$$P_{gate} = Q_G \cdot V_G \cdot f_{SW} \quad (7)$$

These losses are generated due to the gate charge of the MOSFET but are dissipated in the gate resistor and the gate driver.

The output charge Q_{oss} and the reverse recovery charge Q_{rr} also produce losses while turning off the SR MOSFET. A formula can be derived to evaluate this from a simplified model of the turn-off behavior.

By using the following approximations: a triangular shape of the current waveform and a constant output capacitance of the MOSFET, a calculation of the turn-off energy is derived. The triangular shape of the current waveform can be assumed if the current commutation is inductively limited, which is the case for most applications.

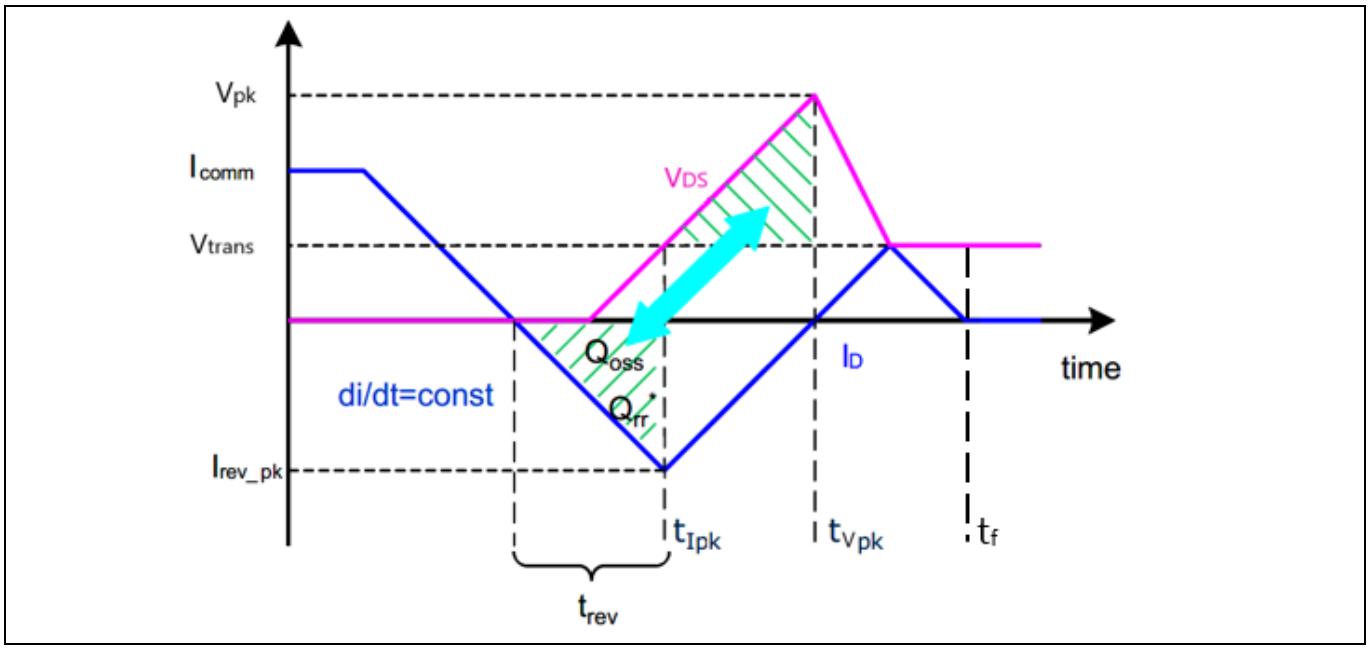


Figure 5 Simplified model of the SR MOSFET turn-off

To calculate the equivalent constant capacitance $C_{oss(AV)}$ of the MOSFET at a certain drain-source voltage *v*, the nonlinear output capacitance $C_{oss}(v)$ is required:

$$Q_{oss}(v) = \int_0^v C_{oss}(v')\,dv' = v \cdot C_{oss(AV)}(v) \tag{8}$$

Where $C_{oss(AV)}$ assumes the meaning of *total* capacitance:

$$C_{oss(AV)}(v) = \frac{Q_{oss}(v)}{v} = \frac{1}{v} \cdot \int_0^v C_{oss}(v')\,dv' \tag{9}$$

Therefore at point t_{Ipeak}, where the drain-source voltage equals the transformer voltage V_T (shown as V_{trans} in **Figure 5**):

$$Q_{oss}(V_T) = V_T \cdot C_{oss(AV)}(V_T) \tag{10}$$

For calculating the turn-off switching losses, first the peak reverse-recovery current I_{rev_pk} is calculated:

$$I_{rev_{pk}} = \frac{di}{dt} \cdot t_{rev} \Longrightarrow t_{rev} = \frac{I_{rev_{pk}}}{di/dt} \tag{11}$$

The di/dt can be estimated by using the transformer voltage and the inductances in the current commutation loop:

$$\frac{di}{dt} = -\frac{V_T}{L_{stray}} \tag{12}$$

The switching charge is given by:

$$Q_{sw} = Q_{oss} + Q_{rr}^{*} \tag{13}$$

and can be evaluated as follows (Q_{SW} in this case represents the *total recovered charge*, and should not be confused with the gate switching charge also referred to as Q_{SW}):

$$Q_{sw} = \frac{I_{rev_{pk}} \cdot t_{rev}}{2} = \frac{I_{rev_{pk}}^2}{2\left|di/dt\right|} \Rightarrow I_{rev_{pk}}^2 = 2Q_{sw}\left|\frac{di}{dt}\right| \tag{14}$$

From this derivation the inductive switching energy is calculated:

$$E_{ind} = \frac{1}{2} L_{stray}\, I_{rev_{pk}}^2 = L_{stray}\left|\frac{di}{dt}\right| Q_{sw} \tag{15}$$

Equation (15) highlights that the total energy stored in the loop inductance is proportional to the *total* recovered charge and to the rate of change of the current during the commutation. Care must be taken when trying to extrapolate the results for different values of di/dt, since Q_{sw} also shows a strong dependence on the rate of change of the current (via Q_{rr}^{*}).

By using **Equation (12)**, expression can be further rearranged, giving:

$$E_{ind} = V_T\, Q_{sw} \tag{16}$$

which represent, in turn, the work done by the generator (considering the secondary transformer winding as an ideal voltage source of value V_T) to deplete the charge from the drift region (Q_{rr}^{*}) and charge the output capacitance of the MOSFET up to V_T.

It should be noted that, despite **Equation (16)** holds under the assumption of triangular current shown in **Figure 5**, it is valid in general (i.e. regardless of the waveforms for current and voltage) that the work done by the generator is:

$$W_g = V_T\, Q_{sw} \tag{17}$$

In other words, this means that the while – for the sake of clarity – the analysis has been carried out for an idealized case, the results are of general validity.
Looking at the point t_{Ipk}, not only magnetic energy is stored in the loop inductance (distributed in multiple stray inductances as per **Equation (4)**) but also electrical energy is being accumulated in the C_{oss}. Taking a snapshot at this point of time: the total energy stored in the reactive elements can be expressed as:

$$E_{TOT}(t_{Ipk}) = \frac{1}{2} L_{stray}\, I^2_{rev_{pk}} + E_{oss}(V_T) \tag{18}$$

Where E_{oss} is the energy stored in the output capacitance of the MOSFET:

$$E_{oss}(V_T) = \int_0^{V_T} C_{oss}(v)\, v\, dv = \int_0^{Q_{oss}(V_T)} v\, dq \tag{19}$$

From this point onward, a resonant transient will occur, with oscillations in both drain-source voltage and drain current. Indeed, the magnetic energy in **Equation (16)** transfers to the output capacitance of the MOSFET shown in **Figure 5**, and there it produces an overvoltage spike. Oscillations are dampened throughout the transient by means of all the resistances in the path (**Figure 3**).

When the resonant transients end, the resonant current is zero and no energy is stored in L_{stray}. C_{oss} stores electric energy in amount of $E_{oss}(V_T)$. Let's take another snapshot at this point of time t_f: the total energy stored in the reactive elements can be expressed as:

$$E_{TOT}(t_f) = E_{oss}(V_T) \tag{20}$$

According to the energy conservation principle, energy balance can be expressed as follows:

$$E_{TOT}(t_{Ipk}) = E_{TOT}(t_f) + E_{diss} \tag{21}$$

Which results in an energy dissipation, in terms of conduction losses happening during the resonant transient, which can be quantified as follows:

$$E_{diss} = \frac{1}{2} L_{stray}\, I^2_{rev_{pk}} = V_T\, Q_{sw} = W_g \tag{22}$$

It appears that the total work done by the generator is energy which is lost every time the synchronous rectifier MOSFET is turned-off. This actually does not hold true. Indeed, we have to remember that at the end of the turn-off transient, energy is still stored in the output capacitance of the MOSFET. Assuming CCM operation, the energy $E_{oss}(V_T)$ will be recovered, transferred to the load inductor in the next turn-on transition of the SR. In order to get the switching-cycle averaged switching losses, the turn-on transition have to be considered as well; hence $E_{oss}(V_T)$ must be substracted from E_{diss}:

$$P_{sw} = [V_T \cdot (Q_{oss} + Q^*_{rr}) - E_{oss}(V_T)]\, f_{sw} \tag{23}$$

Therefore, by separating the output charge from the reverse-recovery charge:

$$P_{sw} = [V_T\, Q_{oss} - E_{oss}(V_T)]\, f_{sw} + V_T Q^*_{rr} f_{sw} \tag{24}$$

Otherwise expressed as:

$$P_{sw} = \left[V_T\, Q_{oss} - \int_0^{Q_{oss}(V_T)} v\, dq\right] f_{sw} + V_T Q^*_{rr} f_{sw} \tag{25}$$

Then, with the aim of **Figure 6 (b)**, it is easy to recognize that the term between brackets represents the purple area underlying the output charge characteristic $Q_{oss}(V_{DS})$:

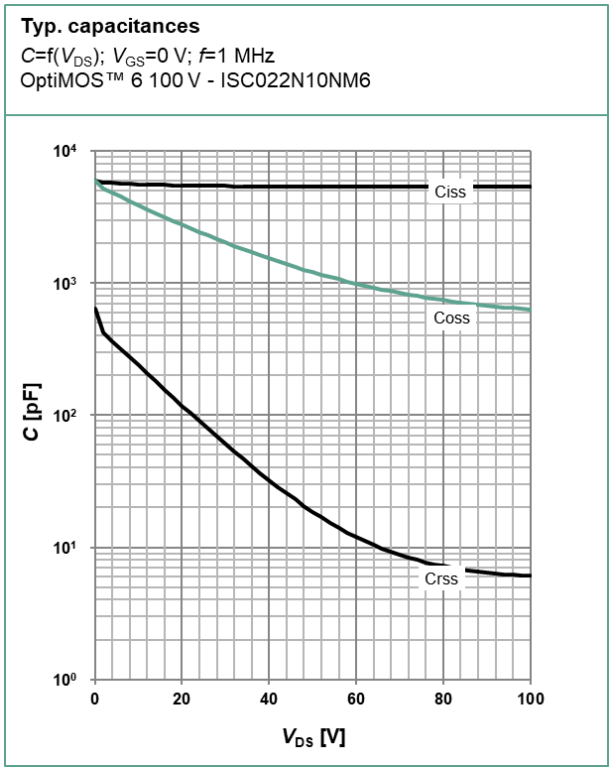
$$P_{sw} = \left[\int_0^{V_T} Q_{oss}(v)\, dv\right] f_{sw} + V_T Q_{rr}^* f_{sw} \tag{26}$$

Assuming Q_{rr}* negligible:

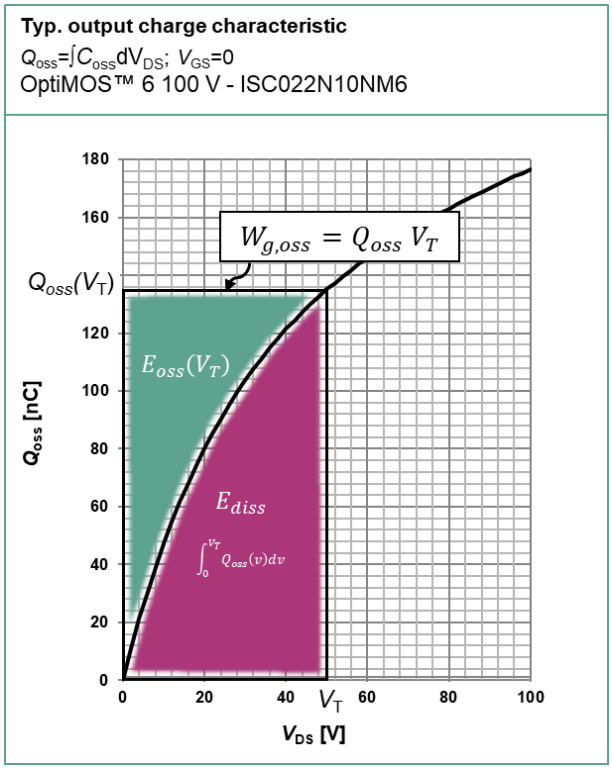
$$P_{sw} \approx f_{sw} \int_0^{V_T} Q_{oss}(v)\, dv = f_{sw} \int_0^{V_T} \int_0^{u} C_{oss}(v) dv\, du \tag{27}$$

Equation (27) provides a simple way to estimate the trun-off switching losses for a certain SR MOSFET provided that Q_{rr}* is negligible. It also highlight that these losses can be estimated through knowledge of the output capacitance curve $C_{oss}(V_{DS})$ alone, by integrating it two times. Finally, again with the aim of **Figure 6 (b)**, one may think about approximating the integral as:

$$P_{sw} \approx \frac{1}{2} f_{sw}\, Q_{oss}(V_T)\, V_T \tag{28}$$



(a) Typ. capacitances profiles for OptiMOS™ 6 100 V ISC022N10NM6



(b) Output charge characteristic obtained by integration of C_{oss} curve

Figure 6 Energy considerations based on the analysis of the output charge characteristic, assuming V_T = 50 V

Since the the output charge characteristic profile strongly depends on the technology generation and the voltage class, **Equation (28)** represents just a crude approximation. Still, can be useful for a first round of iteration in the process of selection of the SR MOSFET, especially if V_T mathches half of breakdown voltage so that Q_{oss} is already specified in the product datasheet. If it is not the case, **Equations (8)** to **(10)** apply.

Please also note that the accuracy of this calculation depends on the switching behavior of the MOSFET. It is necessary to ensure that no second-order effects such as dynamic turn-on or avalanche are occurring. Furthermore, it should be noted that the above equations are valid for hard-switching. However, in resonant topologies, ZCS may be achieved and therefore Q_{rr}* would be zero.

In this case the MOSFET can be optimized for lower $R_{DS(on)}$, as some part of the switching energy can possibly be recovered.

3.3 Reverse recovery charge of the body diode

The MOSFET body diode plays an important role when an optimization regarding efficiency is being carried out. As it is typically flooded with current every switching cycle before the MOSFET gets turned off, a reverse recovery charge Q_{rr}* is built up. As previously mentioned, the real Q_{rr}* is not adequately represented by the Q_{rr} value quoted in datasheets.

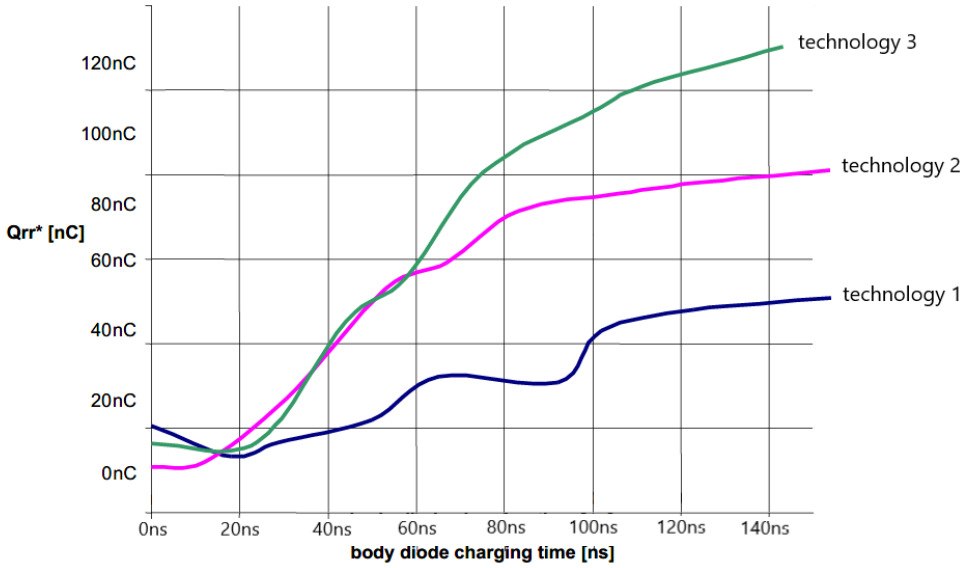


Figure 7 Q_{rr}* dependency of body diode charging time

As shown in the diagram above, the MOSFET gate timing has a strong influence on the effective Q_{rr}*. The longer the body diode is conducting current before turn-off, the higher the reverse recovery charge will be. This will decrease efficiency and lead to a higher turn-off voltage spike. Consider technology 3 as an example. Going from a perfect timing of just 20 ns up to 140 ns, an additional power loss of about 0.5 W at transformer voltage = 40 V and switching frequency = 125 kHz can influence efficiency dramatically, especially at light load.

Depending on MOSFET technology and the flooding time of the body diode, the Q_{rr} is often of secondary importance where the output capacitance is typically dominant.

4 Selecting the optimum SR MOSFET

For optimization of the SR MOSFET to obtain best system efficiency, a well-balanced ratio between switching losses and conduction losses needs to be reached. Considering first a light-load condition, the $R_{DS(on)}$ conduction losses play only a minor role. In this case the switching losses, which are more or less constant over the whole load range, are dominant. However, in case of high output current the conduction losses contribute most to the total power losses, as illustrated in the following example considering a 60 V OptiMOS™ 3 device with a maximum $R_{DS(on)}$ of 3.6 mΩ:

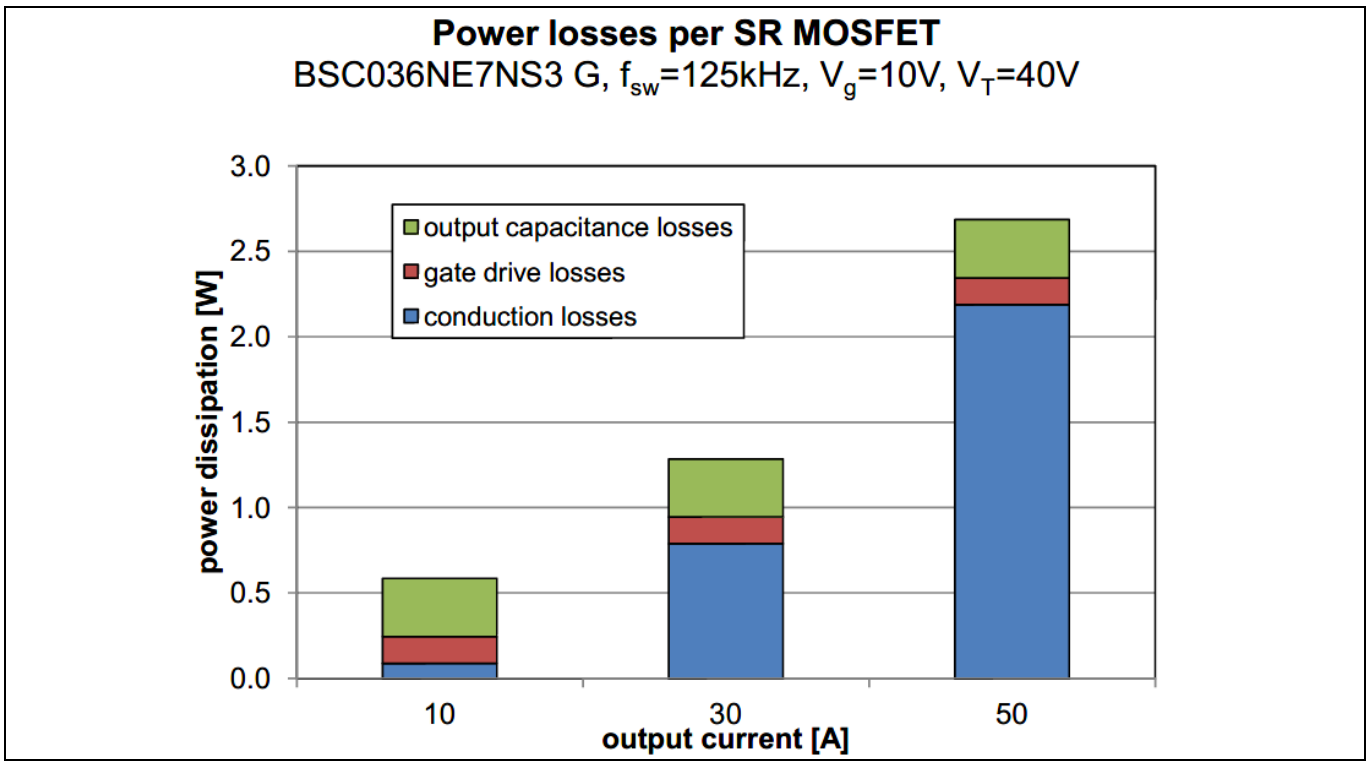


Figure 8 Power loss breakdown vs. output current

As expected, the switching losses and gate drive losses do not vary with load, but the conduction losses increase with load proportional to the square of the current. To choose the best-fitting MOSFET, special attention has to be given to the $R_{DS(on)}$ class. To illustrate this, **Figure 9** compares the losses of three different die size devices from the 60 V OptiMOS™ 3 family at an average current of 15 A switching at 175 kHz. The optimum point is seen where the total losses, indicated by the green curve, reach a minimum point. Increasing $R_{DS(on)}$ beyond the optimum point increases total power losses at a more or less constant rate. However, reducing the $R_{DS(on)}$ below 0.5 mΩ leads to dramatically increased losses because of rapidly increasing output capacitance. Furthermore, in **Figure 9**, it can be seen that the $R_{DS(on)}$ range for minimum total power losses ranges from 1.3 mΩ to 1.5 mΩ with some room either side of these values that would give acceptable results. That being the case, both the **BSC016N06NS** and **BSC028N06NS** would be suitable. And, actually, since losses are still below 1 W over a broader range (0.55 to 3.9 mΩ), selecting the **BSC039N06NS** could also be acceptable. However, the BSC039N06NS would perform better in applications with lower current and/or higher switching frequency.

Keep in mind that graphs such as **Figure 8** are plotted under a specific set of conditions. Indeed, as can be seen in **Figure 10** the situation changes greatly when varying the switching frequency or the current flowing through each MOSFET. If we take the example where the MOSFET current (I_{MOSFET}) is decreased to 5 A and f_{SW} remains at 175 kHz, switching losses now represent a greater share of the overall losses so it is advantageous to opt for the BSC039N06NS. On the other hand, when the switching frequency is reduced to 100 kHz and I_{MOSFET} stays at 15 A, a part that exhibits lower conduction losses such as the BSC016N06NS performs much better.

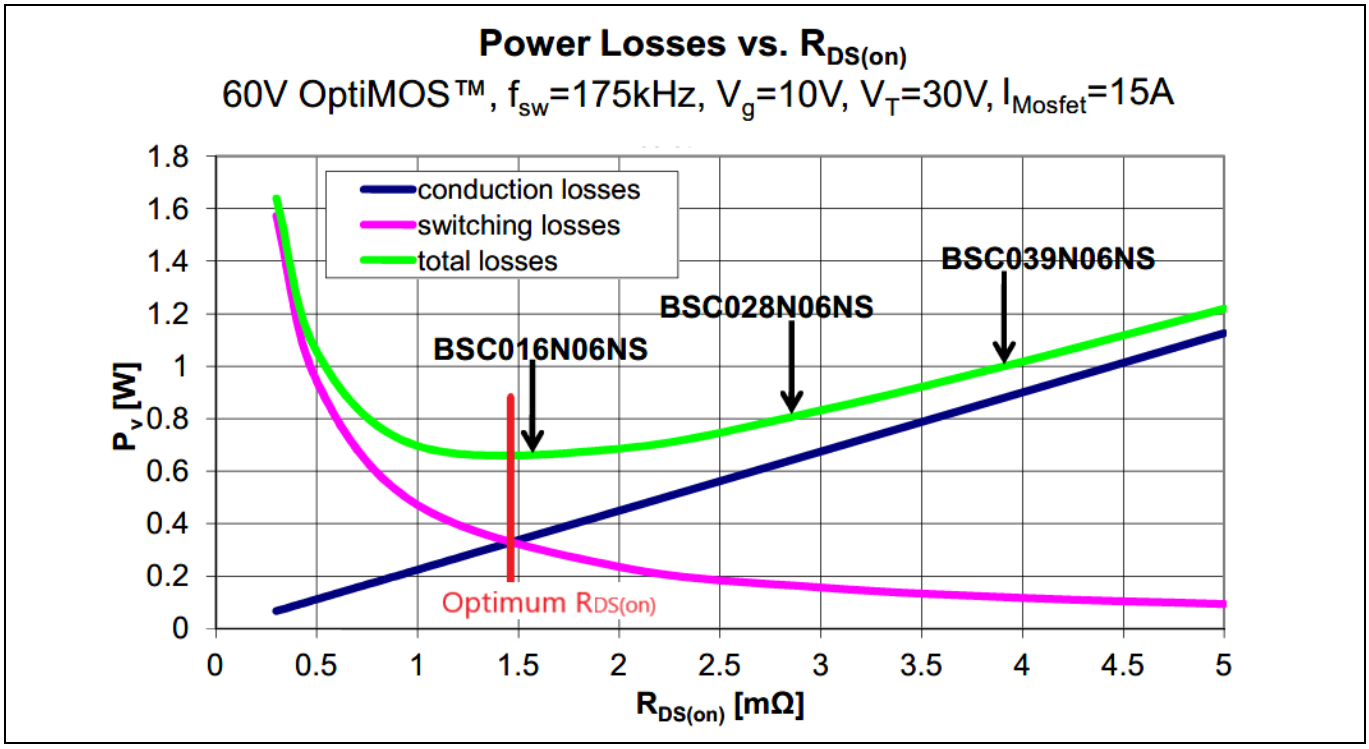


Figure 9 Power losses vs. $R_{DS(on)}$

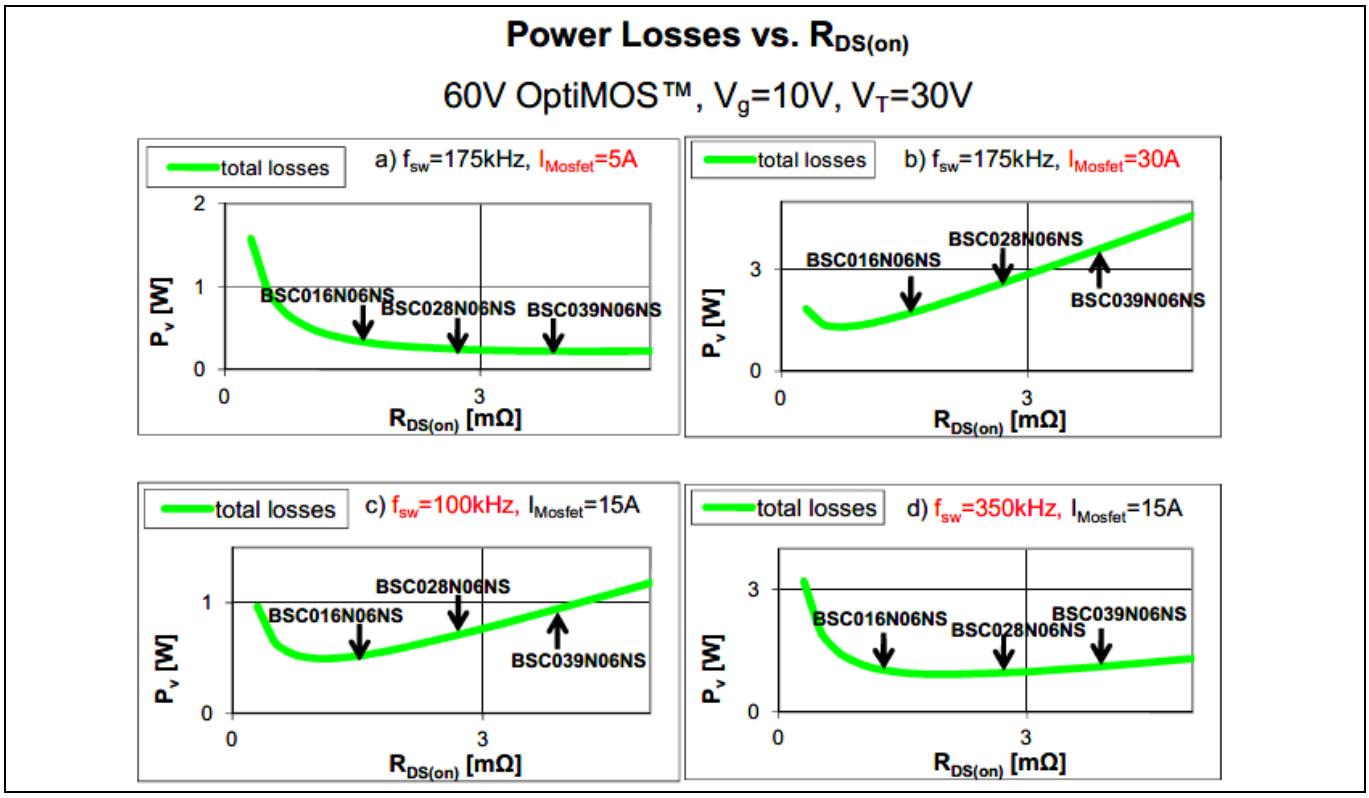


Figure 10 Power losses vs. $R_{DS(on)}$ at different f_{SW} and I_{MOSFET}

A further important issue for optimizing SR as well as selecting the best device technology is the correct choice of the MOSFET package. An efficiency boost can be achieved simply by replacing the TO-220 package with a

SuperSO8 (5x6 QFN) due to its reduced package contribution to the total $R_{DS(on)}$. Reducing the package $R_{DS(on)}$ while keeping the output capacitance the same leads to a reduced $FOMQ_{OSS}$, which is a performance indicator of a given MOSFET technology ($FOMQ_{OSS} = R_{DS(on)} \times Q_{OSS}$). Lower $FOMQ_{OSS}$ results in reduced switching losses and therefore increases the efficiency.

5 Optimization for different load conditions

To achieve a balanced efficiency over the complete load range, a suitable choice of the MOSFET current to be used with the four-quadrant SR device optimization chart has to be made. Full-load optimization will give good efficiency results at high output current; however, this approach will decrease efficiency at light loads and increase the number of parallel MOSFETs to an unacceptable value. A trade-off needs to be found in order to achieve a relative constant efficiency value over the entire load range.

To illustrate this problem, efficiency curves with different optimization approaches can be seen in **Figure 11**. These efficiency charts show the calculated efficiency of a SR stage with an output voltage (V_{OUT}) of 12 V, a transformer voltage of 24 V, a gate driving voltage of 10 V and a switching frequency of 200 kHz. Taking the **BSC010N04LS** in the 40 V optimization chart and executing the design process for 20 A MOSFET current gives a single MOSFET as the optimum choice. The efficiency curve shows a high efficiency at low currents but lower efficiency at high currents. To improve this a 40 A optimization is shown, which yields the optimum number of parallel MOSFETs as 2. In this case, the efficiency at low currents decreases but reaches a maximum at higher loads. Typically, a balanced efficiency can be achieved by optimizing the MOSFET for 20 to 30 percent of the maximum output power. For systems with focus on light-load efficiency, currents as low as 10 to 20 percent of the maximum current can be used, while for high-load designs optimization of up to 60 percent may be appropriate. Optimization for 100 percent output load should be avoided, since low-load efficiency will be degraded and the number of parallel MOSFETs is increased.

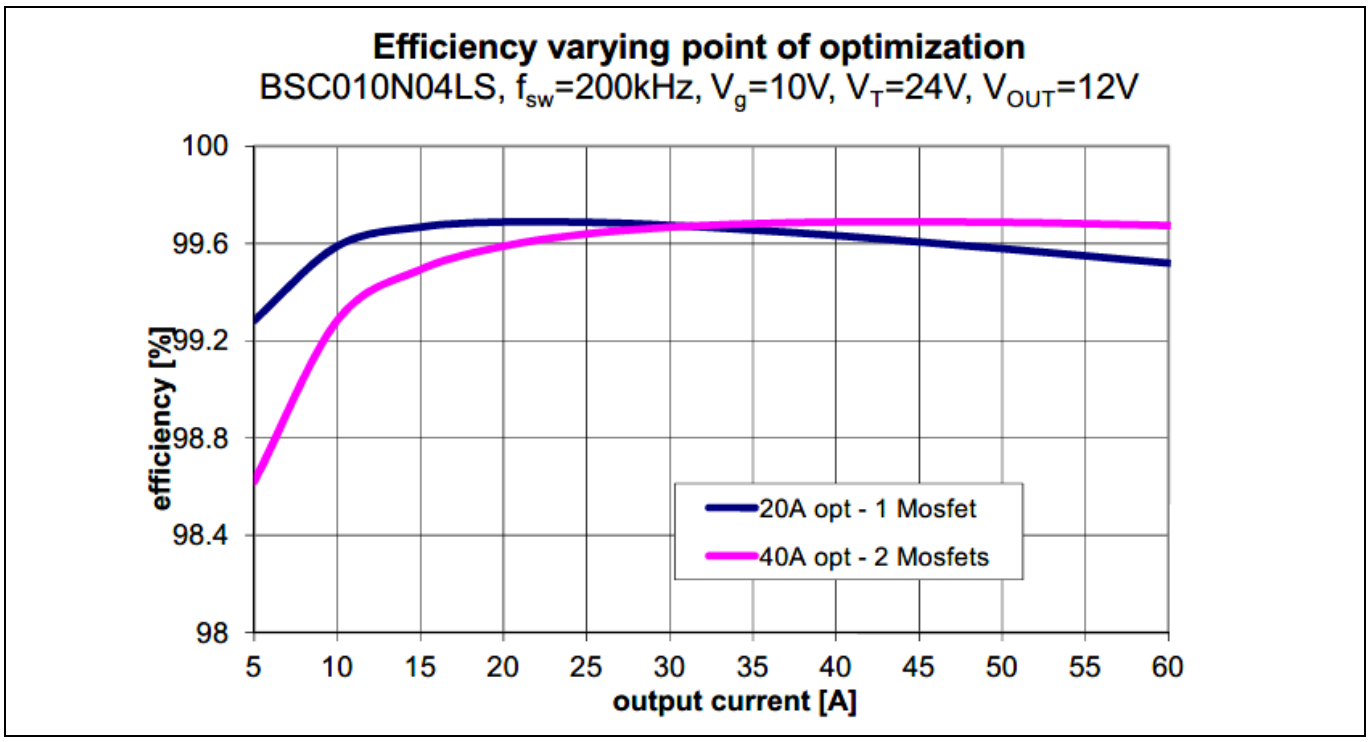


Figure 11 Efficiency varying point of optimization

6 MOSFET selection using a four-quadrant SR device optimization chart

For easier selection of the MOSFET in the SR application, a four-quadrant SR device optimization chart was developed several years ago by Infineon.[1] With this chart it is easy to find the best-fitting part without performing any calculations since the curves have already been calculated according to the MOSFET device parameters and using a set of rules developed to model operation in SR applications.

The selection chart is generated from an Excel spreadsheet by entering sets of MOSFET data for devices of a specific BV_{DSS}. The values entered for each device are: $R_{DS(on)}$, Q_G (at V_{DS} = 10 V) and a list of values of Q_{OSS} calculated at different V_{DS} points. The frequency curves in quadrant (2) and the current lines in quadrant (3) are calculated independently of the MOSFET parameters based on a general application model. Using this spreadsheet it is quite straightforward to generate a chart for any MOSFET. It should be noted however that the Q_{OSS} data used is not included in device datasheets.

By using three application parameters – secondary-side transformer voltage, switching frequency and RMS MOSFET current – with the chart, the optimum $R_{DS(on)}$ is determined. A worked example is shown below:

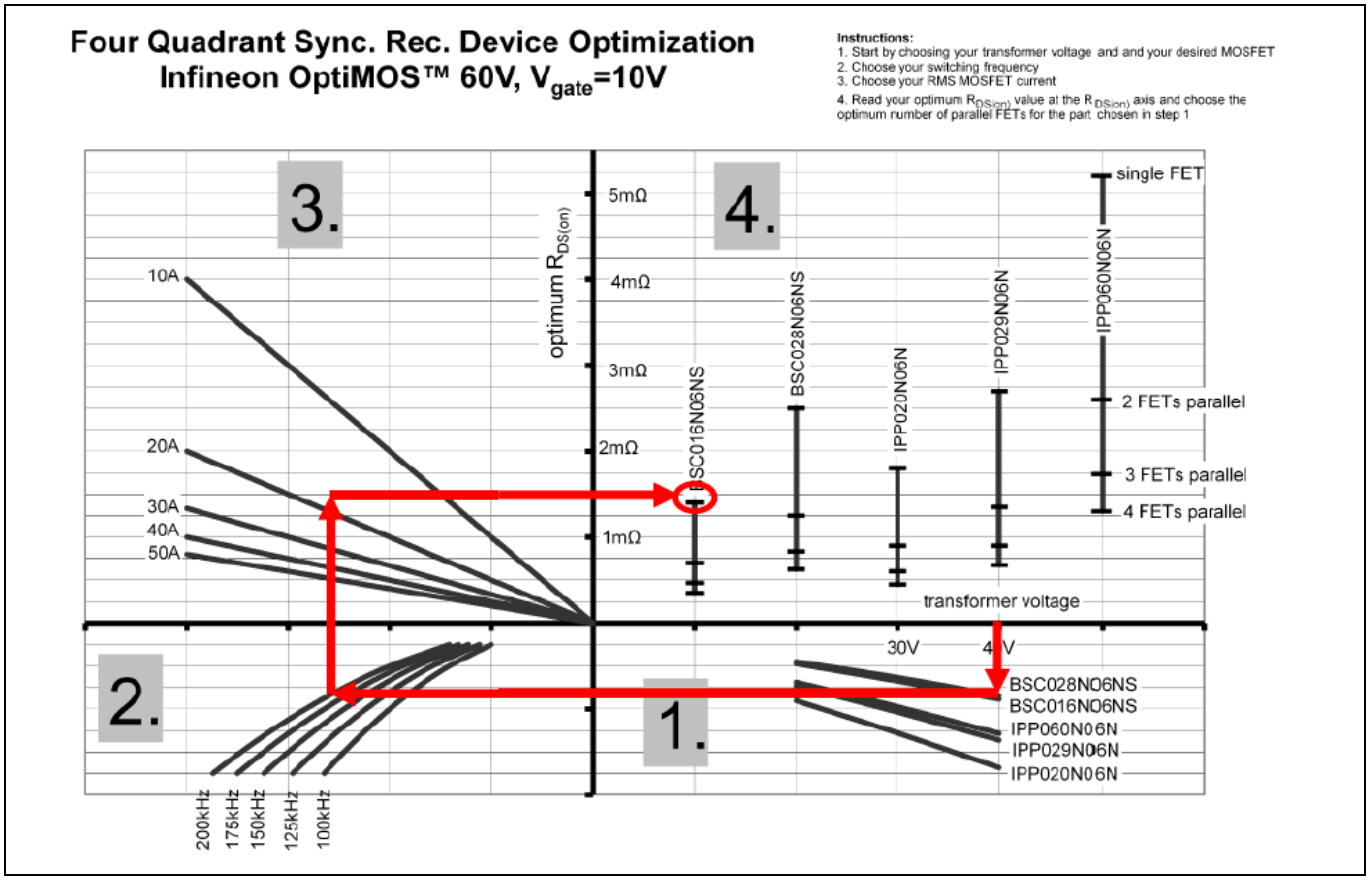


Figure 12 Four-quadrant SR device optimization chart

The starting point for the optimization chart is the secondary-side transformer voltage located on the x-axis on the right-hand side of the diagram. By drawing a vertical line downward from the voltage point, a specific MOSFET can be chosen by intersecting with the curves given for different devices in quadrant (1). These curves

[1] Refer to the original application notes on this topic listed in the References section written by the original developers of this method.

provided here are calculated from the device Q_{OSS}. It should be noted that the x-axis represents voltage only in area (1) but not in quadrant (2).

By completing the following steps, the diagram will indicate whether this device can meet the design requirements:
A horizontal line is drawn from the intersection point in quadrant (1) to intersect with the frequency lines provided in quadrant (2). From the desired frequency an upward vertical line is drawn to intersect with the current lines displayed in quadrant (3). As previously discussed, a good starting point for the current level is 20 to 30 percent of full-load current. Another horizontal line is then added from the current line intersection point in quadrant (3) to quadrant (4), where it crosses the vertical lines representing the MOSFETs featured in the chart, which are recommended for this purpose. As this line crosses the y-axis, the optimum $R_{DS(on)}$ value can be read. The vertical MOSFET lines displayed in quadrant (4) are divided into sections to indicate the number of parallel devices required to meet the system requirements, where the highest point represents a single MOSFET.

The process may then be repeated if needed with different values of transformer voltage, switching frequency and RMS current to explore different MOSFET options. The result that gives the lowest optimum $R_{DS(on)}$ produces minimum power losses and therefore provides the highest system efficiency. This process is a quick method to determine, from the selection of devices given in the chart, which is best suited to the required operating conditions.

It should be noted that this MOSFET selection method is designed for applications with optimum switching behavior. If any second-order effects like dynamic turn-on or avalanche are occurring this chart may be inaccurate. Furthermore, best results are achieved for hard-switched converter topologies. Any resonant soft-switching topology might lead to a mismatch as some part of the switching energy can potentially be recovered. In this case the optimum $R_{DS(on)}$ class would be lower than that given by the calculation. Note that a quasi-resonant topology on the primary side (e.g. phase-shift zero-voltage switching full-bridge) can also exhibit hard-switching behavior on the secondary-side SRs and can therefore be optimized using these design charts.

All results derived from the optimization charts are based on ideal MOSFET behavior. According to experience, results can differ in real applications compared to ideal calculations. Therefore, these results should be considered as an indication for best possible device selection and as a prevention for under/oversizing of the MOSFETs. If the result of the chart is between two different numbers of parallel MOSFETs, the lower number will be low-load optimized, while the higher number will give better performance at high power levels. Furthermore, any snubber networks that may be connected between the drain and source of the SR MOSFETs would affect switching performance. The design charts do not to take this into account.

Optimization over the whole load range cannot be done in a single calculation. A specific load point (current level) has to be taken to determine optimum $R_{DS(on)}$ and select the MOSFET(s). For expanding the optimization range, multiple extrapolations using the four-quadrant diagram for different load currents need to be carried out to cover different operating points.

7 MOSFET selection charts for synchronous rectification by voltage class

7.1 25 V OptiMOS™ devices

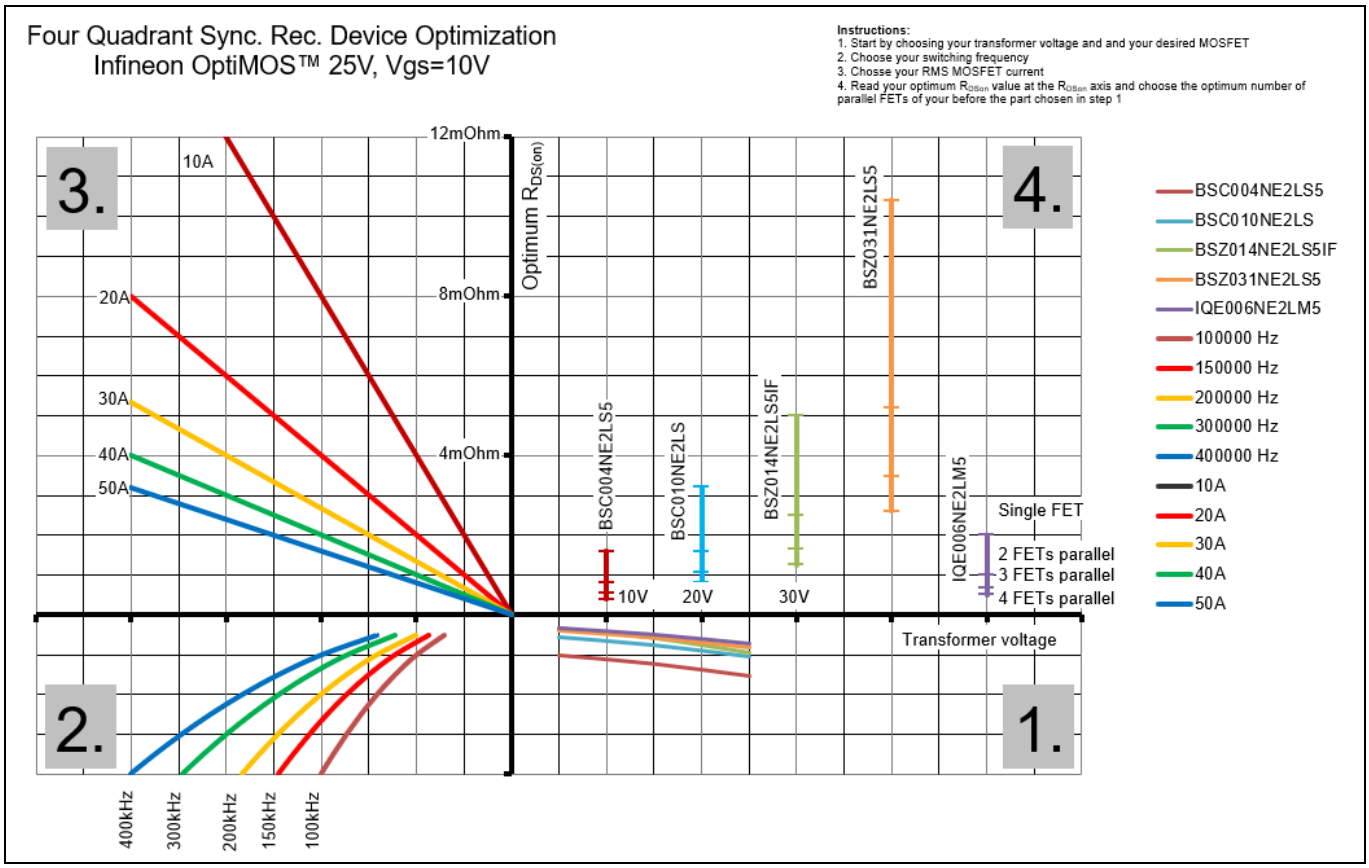


Figure 13 25 V OptiMOS™ SR MOSFET selection chart

Table 1 25 V OptiMOS™ SR MOSFET list

Part number	Package	$R_{DS(on)}$ typical (mΩ) at 10 V	BV_{DSS}
BSC004NE2LS5	SuperSO8 5 x 6	0.40	25
BSC010NE2LS	SuperSO8 5 x 6	0.80	25
BSZ014NE2LS5IF	PQFN 3.3 x 3.3	1.25	25
BSZ031NE2LS5	PQFN 3.3 x 3.3	2.60	25
IQE006NE2LM5	PQFN 3.3 x 3.3 source down	0.50	25

7.2 30 V OptiMOS™ devices

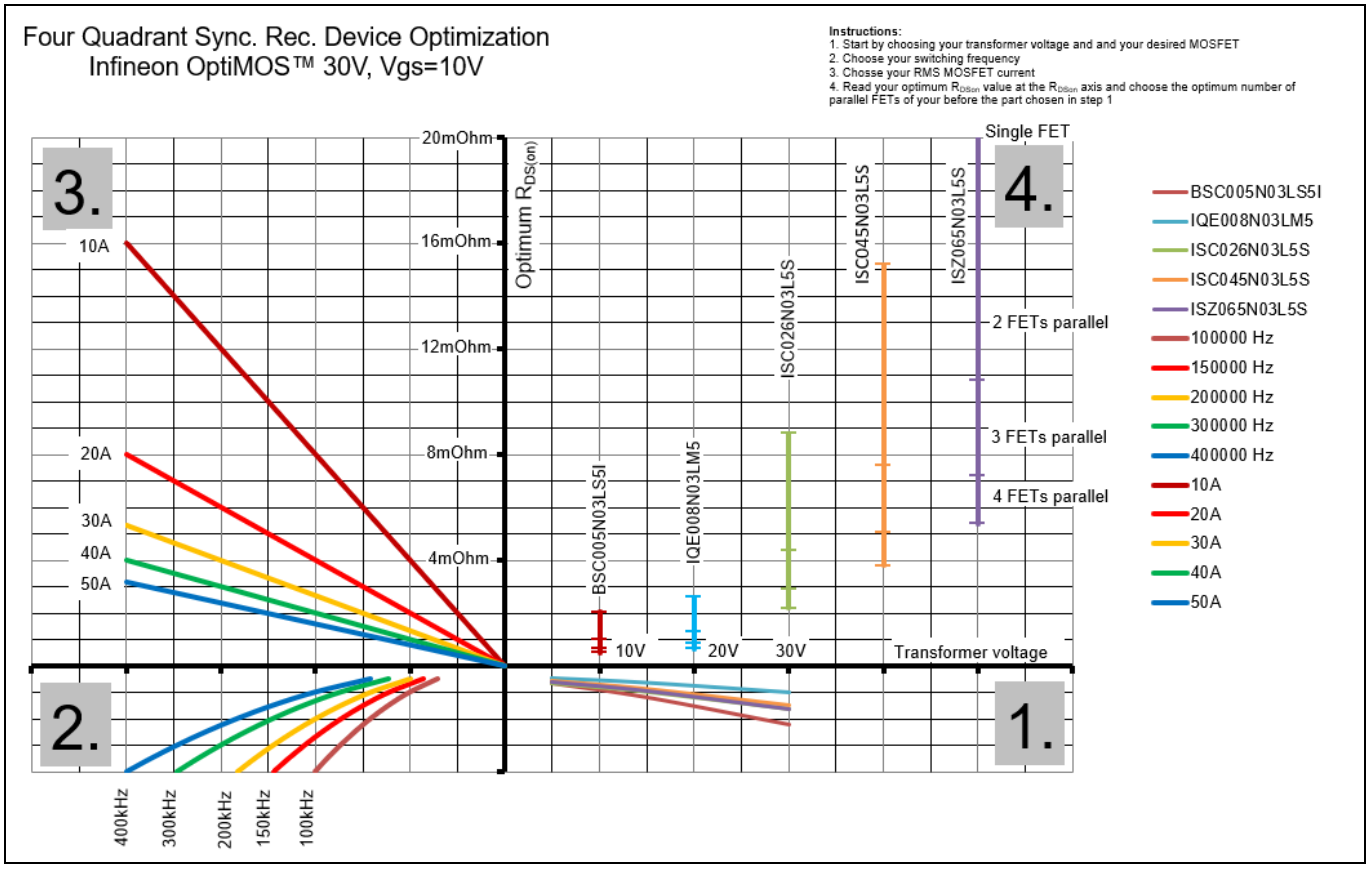


Figure 14 30 V OptiMOS™ SR MOSFET selection chart

Table 2 30 V OptiMOS™ SR MOSFET list

Part number	Package	$R_{DS(on)}$ typical (mΩ) at 10 V	BV_{DSS}
BSC005N03LS5I	SuperSO8 5 x 6	0.51	30
IQE008N03LM5	PQFN 3.3 x 3.3 source down	0.65	30
ISC026N03L5S	SuperSO8 5 x 6	2.20	30
ISC045N03L5S	SuperSO8 5 x 6	3.80	30
ISZ065N03L5S	PQFN 3.3 x 3.3	5.40	30

7.3 40 V OptiMOS™ devices

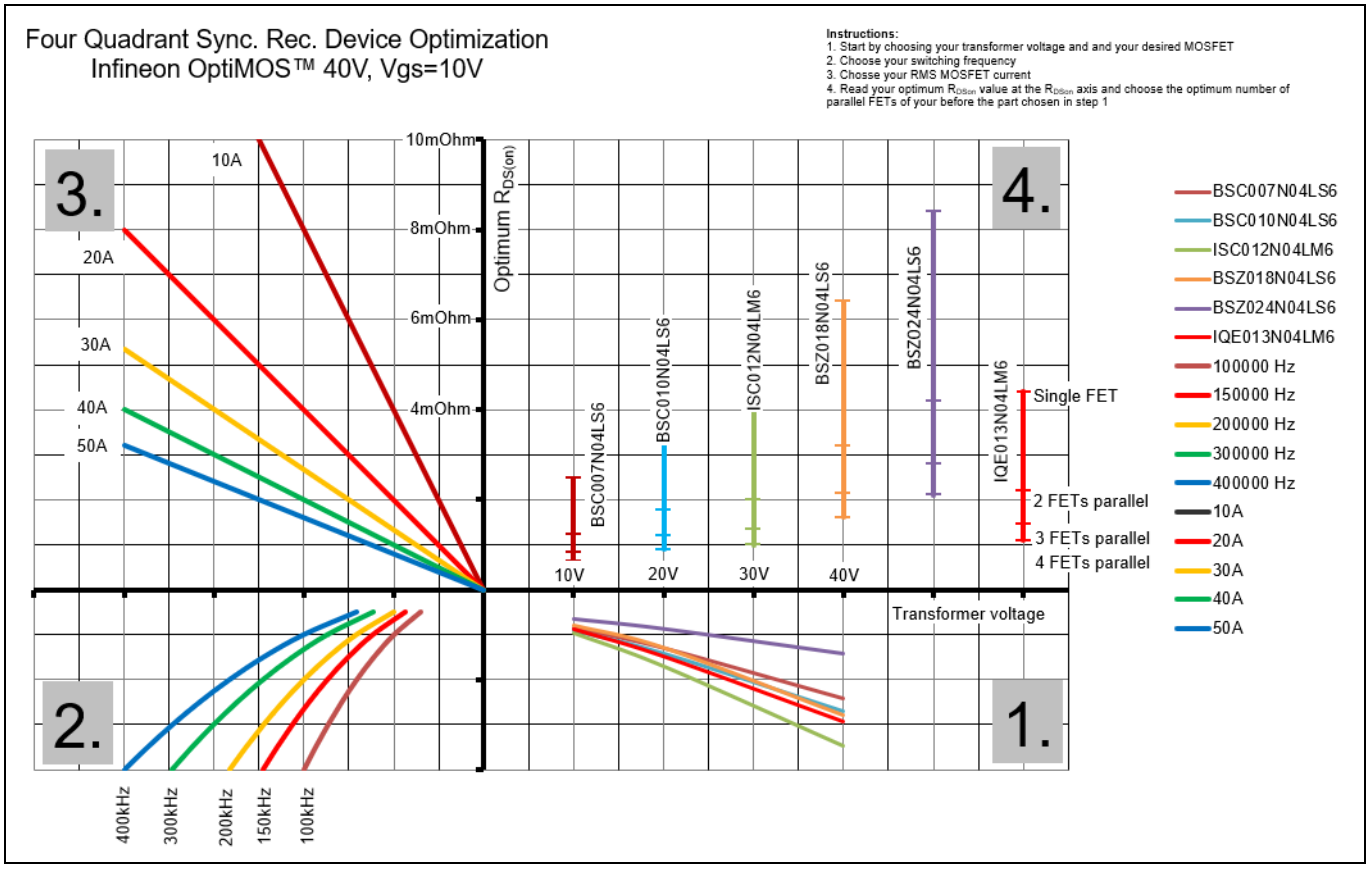


Figure 15 40 V OptiMOS™ SR MOSFET selection chart

Table 3 40 V OptiMOS™ SR MOSFET list

Part number	Package	$R_{DS(on)}$ typical (mΩ) at 10 V	BV_{DSS}
BSC007N04LS6	SuperSO8 5 x 6	0.62	40
BSC010N04LS6	SuperSO8 5 x 6	0.89	40
ISC012N04LM6	SuperSO8 5 x 6	1.00	40
BSZ018N04LS6	PQFN 3.3 x 3.3	1.60	40
BSZ024N04LS6	PQFN 3.3 x 3.3	2.10	40
IQE013N04LM6	PQFN 3.3 x 3.3 source down	1.10	40

7.4 60 V OptiMOS™ devices

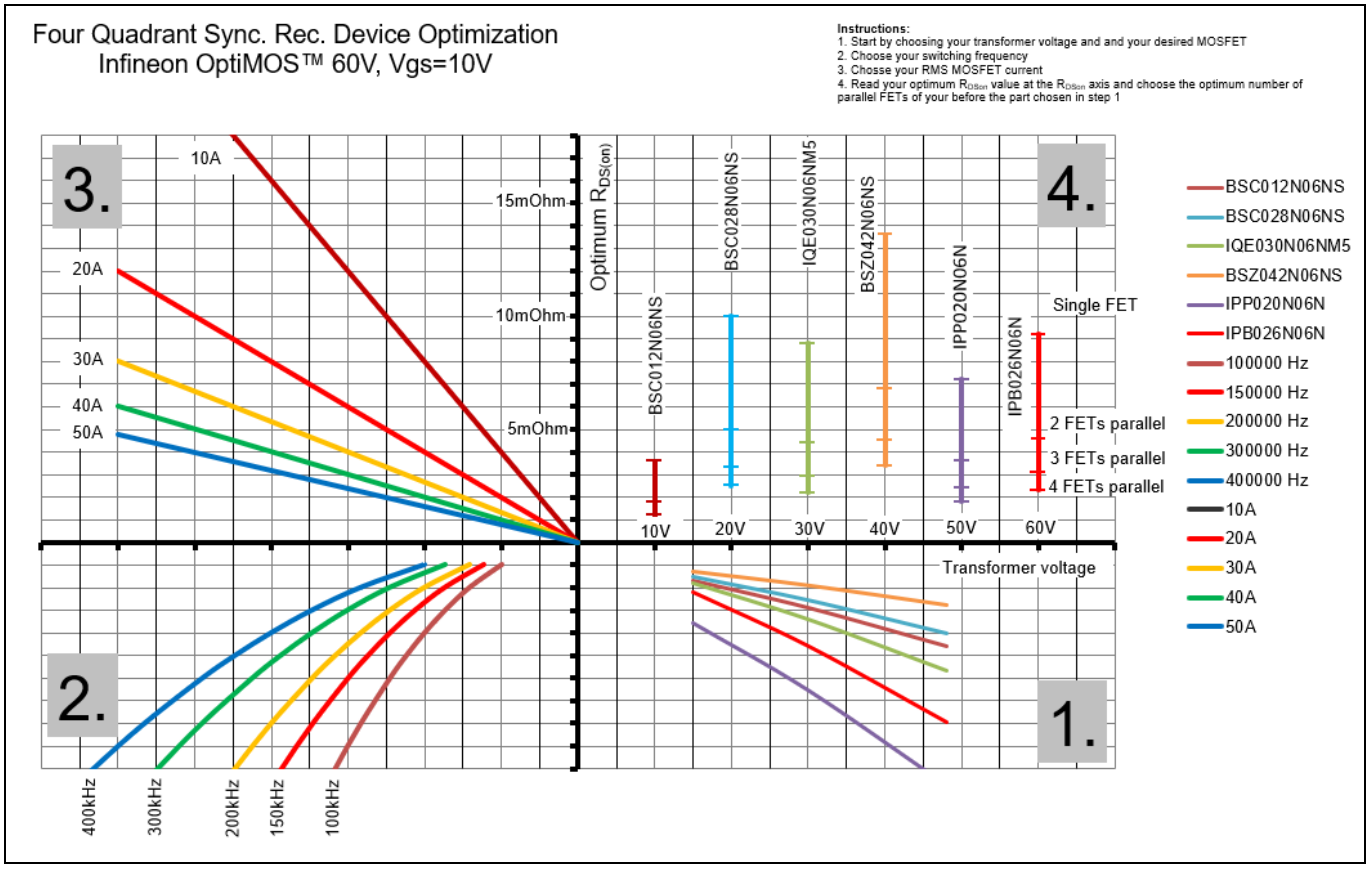


Figure 16 60 V OptiMOS™ 3 SR MOSFET selection chart

Table 4 60 V OptiMOS™ SR MOSFET list

Part number	Package	$R_{DS(on)}$ typical (mΩ) at 10 V	BV_{DSS}
BSC012N06NS	SuperSO8 5 x 6	0.90	60
BSC028N06NS	SuperSO8 5 x 6	2.50	60
IQE030N06NM5	PQFN 3.3 x 3.3 source down	2.20	60
BSZ042N06NS	PQFN 3.3 x 3.3	3.40	60
IPP020N06N	TO-220	1.80	60
IPB026N06N	D2PAK	2.30	60

7.5 80 V OptiMOS™ devices

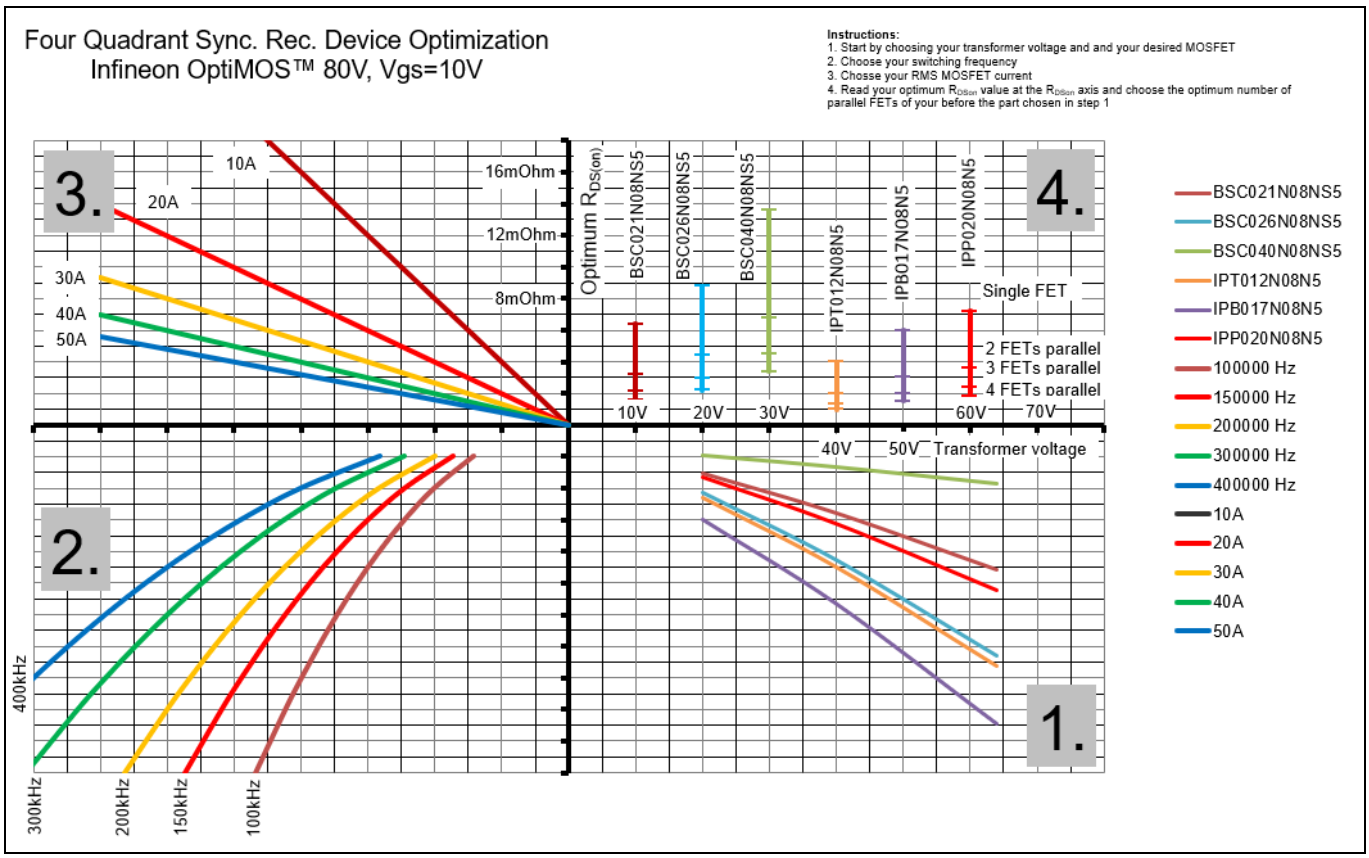


Figure 17 80 V OptiMOS™ 3 SR MOSFET selection chart

Table 5 80 V OptiMOS™ SR MOSFET list

Part number	Package	$R_{DS(on)}$ typical (mΩ) at 10 V	BV_{DSS}
BSC021N08NS5	SuperSO8 5 x 6	1.60	80
BSC026N08NS5	SuperSO8 5 x 6	2.20	80
BSC040N08NS5	SuperSO8 5 x 6	3.40	80
IPT012N08N5	TOLL	1.00	80
IPB017N08N5	D2PAK	1.50	80
IPP020N08N5	TO-220	1.80	80

7.6 100 V OptiMOS™ devices

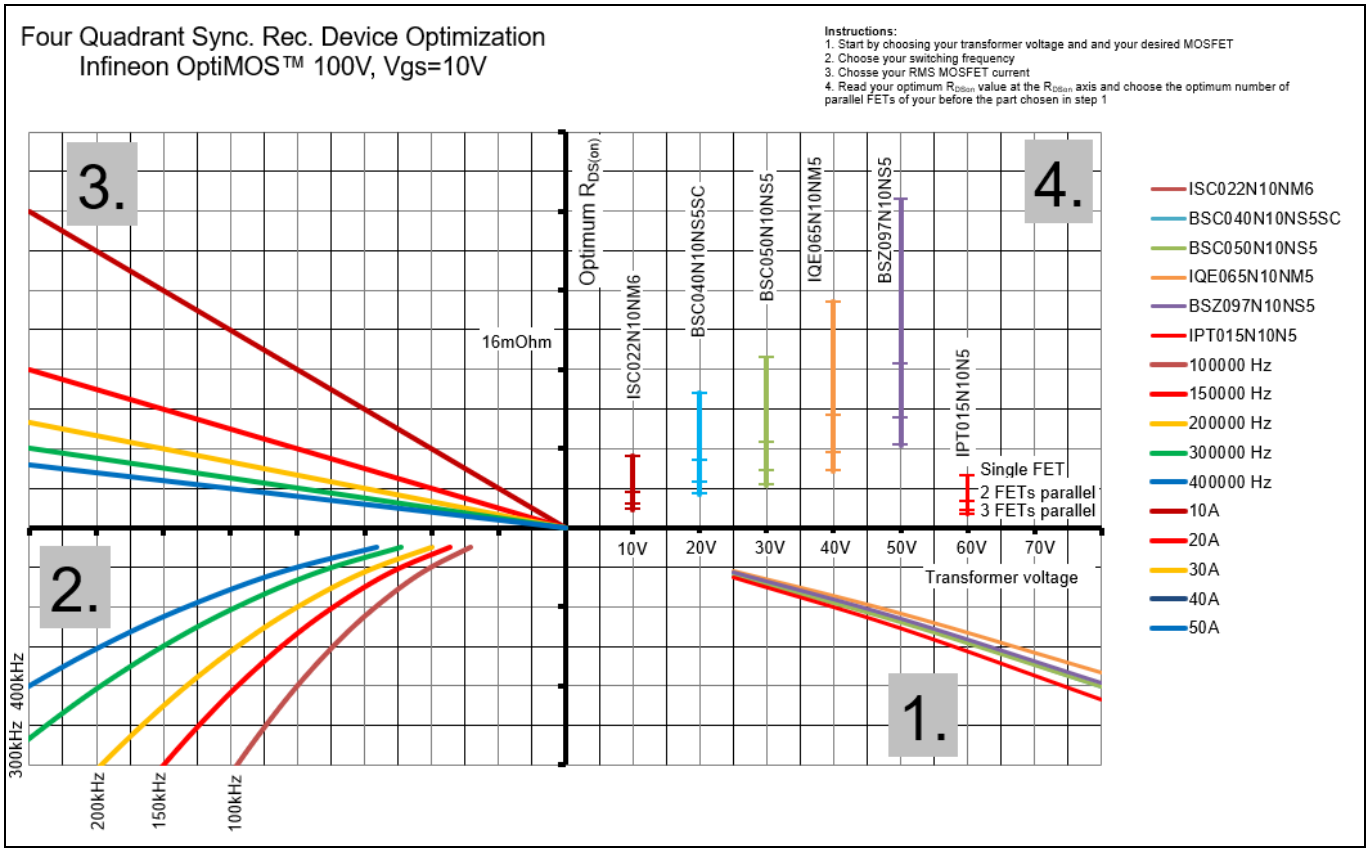


Figure 18 100 V OptiMOS™ 3 SR MOSFET selection chart

Table 6 100 V OptiMOS™ SR MOSFET list

Part number	Package	$R_{DS(on)}$ typical (mΩ) at 10 V	BV_{DSS}
ISC022N10NM6	SuperSO8 5 x 6	1.80	100
BSC040N10NS5SC	SuperSO8 5 x 6 DSC	3.40	100
BSC050N10NS5	SuperSO8 5 x 6	4.30	100
IQE065N10NM5	PQFN 3.3 x 3.3 source down	5.70	100
BSZ097N10NS5	PQFN 3.3 x 3.3	8.30	100
IPT015N10N5	TOLL	1.30	100

7.7 120 V OptiMOS™ devices

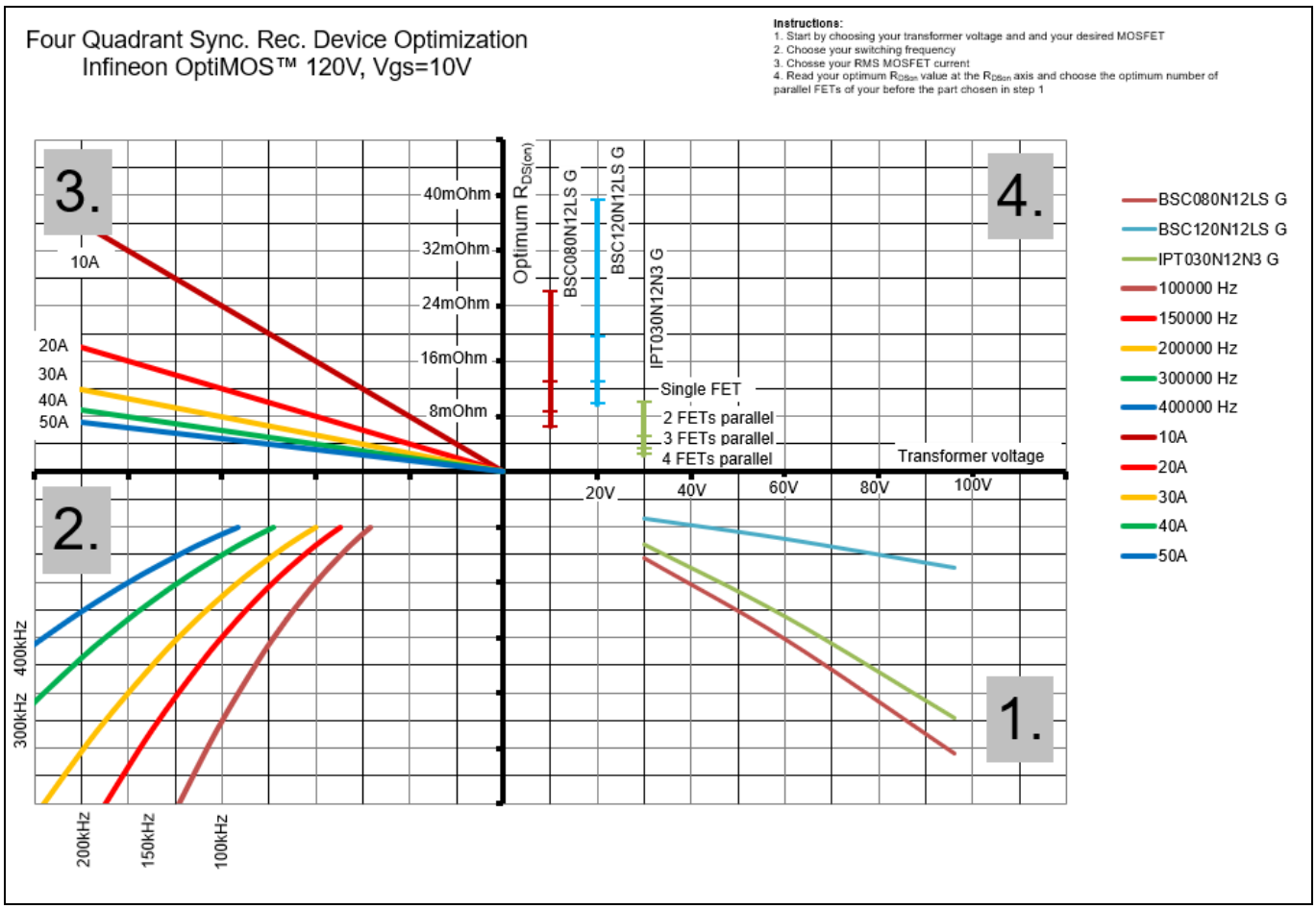


Figure 19 120 V OptiMOS™ 3 SR MOSFET selection chart

Table 7 120 V OptiMOS™ SR MOSFET list

Part number	Package	$R_{DS(on)}$ typical (mΩ) at 10 V	BV_{DSS}
BSC080N12LS G	SuperSO8 5 x 6	6.5	120
BSC120N12LS G	SuperSO8 5 x 6	9.8	120
IPT030N12N3 G	TOLL	2.50	120

7.8 150 V OptiMOS™ devices

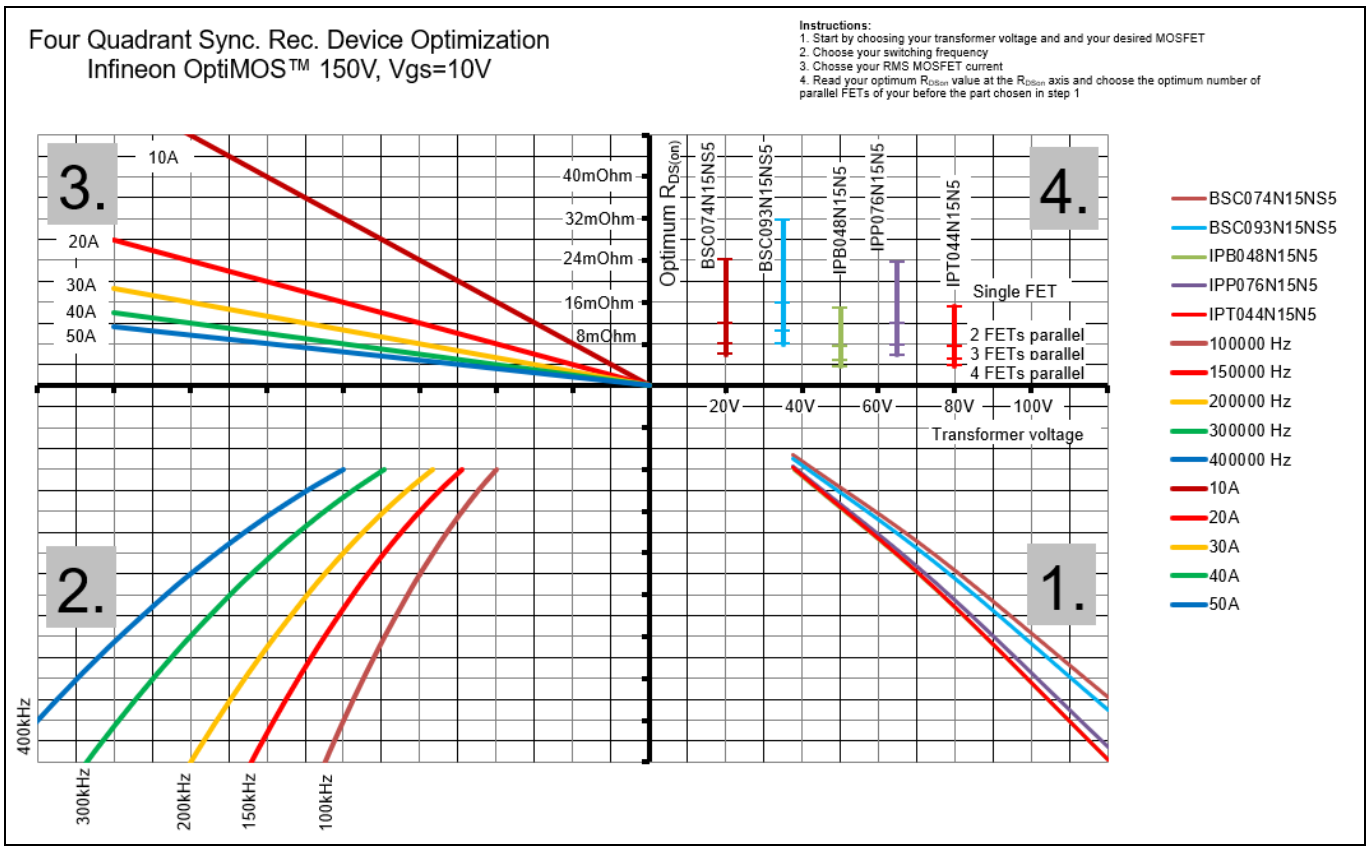


Figure 20 150 V OptiMOS™ 3 SR MOSFET selection chart

Table 8 150 V OptiMOS™ SR MOSFET list

Part number	Package	$R_{DS(on)}$ typical (mΩ) at 10 V	BV_{DSS}
BSC074N15NS5	SuperSO8 5 x 6	6.0	150
BSC093N15NS5	SuperSO8 5 x 6	7.9	150
IPB048N15N5	D2PAK	3.70	150
IPP076N15N5	TO-220	5.9	150
IPT044N15N5	TOLL	3.80	150

8 Conclusion

This application note presents a method to analyze power losses in the SR stage of switched-mode power converters. An analytical yet simple model for calculating the switching losses was developed. With these results developers of SMPS using SR have the chance to optimize topology and MOSFET selection. A calculation to provide a reasonable estimate of the SR power losses can be done, which helps to speed up the design process and improve efficiency.

The SR MOSFET design charts presented here are a useful time-saving tool that help avoid the need for repetitive calculations and simulations and enable the designer to select a suitable device.

References

[1] Infineon Technologies AG: *Optimum MOSFET selection for synchronous rectification;* Application Note; 2012-05-04

[2] Infineon Technologies AG: *Improving efficiency of synchronous rectification by analysis of the MOSFET power loss mechanism*; Application Note; 2012-03-01

[3] Infineon Technologies AG: *Simple design techniques for optimizing efficiency and overvoltage spike of synchronous rectification in DC to DC converters*; Application Note; 2012-03-01

[4] Salato, Maurizio/Lokhandwala, Adnaan/Soldano, Marco: *Design of secondary side rectification using IR1167 SmartRectifier™ control IC*; Application Note

[5] Bocciola, Cesare/Giacomini, Davide: *Design of secondary side rectification using AUIRS1167 SmartRectifier™ control IC*; Application Note

Revision history

Document revision	Date	Description of changes
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V 1.1	2023-02-15	Updated section 3.2

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