Application of OptiMOS™ Linear FET as protection switch in battery-powered motor drive applications

About this document

Scope and purpose

This application note explains the advantages of OptiMOS™ Linear FET over standard MOSFET for inrush current limiting and short-circuit protection in battery-powered applications. The test conditions for each scenario are explained, and the test setups and experimental results are shown. To effectively use the OptiMOS™ Linear FET in a single or parallel combination, guidance has been provided for the external R_G-C_{GD} selection in the gate drive circuit for both turn-on (during inrush current conditions at start-up) and turn-off (during short-circuit protection) transitions.

Intended audience

Power electronics engineers and component engineers; applicable to all battery-powered applications that use parts where short-circuit protection and inrush current conditions at start-up influence the MOSFET selection criteria.

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1 Introduction

The development of modern power MOSFETs has focused on ultrafast switching and ultralow-ohmic devices, leading to continuously decreasing $R_{DS(on)}$, gate charge and output capacitances. But the requirements of protection MOSFETs in battery-powered motor drive applications such as e-bikes, power and gardening tools, etc. differ significantly from those in normal switching MOSFETs. These applications require protection MOSFETs to operate primarily in linear mode (high voltage and current applied at the same time). Therefore, these applications require MOSFETs which have low $R_{DS(on)}$, high current-carrying capability (continuous and pulsed I_D ratings), avalanche ruggedness (E_{AS}), linear mode capability (wider safe operating area/SOA) and better thermal performance (Z_{TH}/R_{TH}). Typically, there is a tradeoff between the low-ohmic device technologies and wider SOA capability due to increased transconductance of the MOSFET, as discussed in **[1]**. OptiMOS™ Linear FET was introduced as a revolutionary approach to avoid the linear mode vs. $R_{DS(on)}$ tradeoff by offering the wider SOA of planar MOSFETs and low $R_{DS(on)}$ of trench MOSFETs.

Figure 1 shows a typical linear mode operating scenario. During the inrush current scenario, the MOSFET is initially in the off-state, where it is blocking the entire battery voltage. Then it moves into linear mode operation, where the MOSFET sees high voltage and high current being applied simultaneously, and then it finally goes into the on-state, where it is conducting steady-state current and a low drain-to-source voltage drop ($V_{DS} = R_{DS(on)} * I_D$) across it. During the short-circuit scenario, the MOSFET starts in the on-state with a low V_{DS} while carrying the short-circuit current. After this it transitions into linear mode during the turn-off transient, and then finally into the off-state, where the current is zero and it is blocking all the battery voltage.

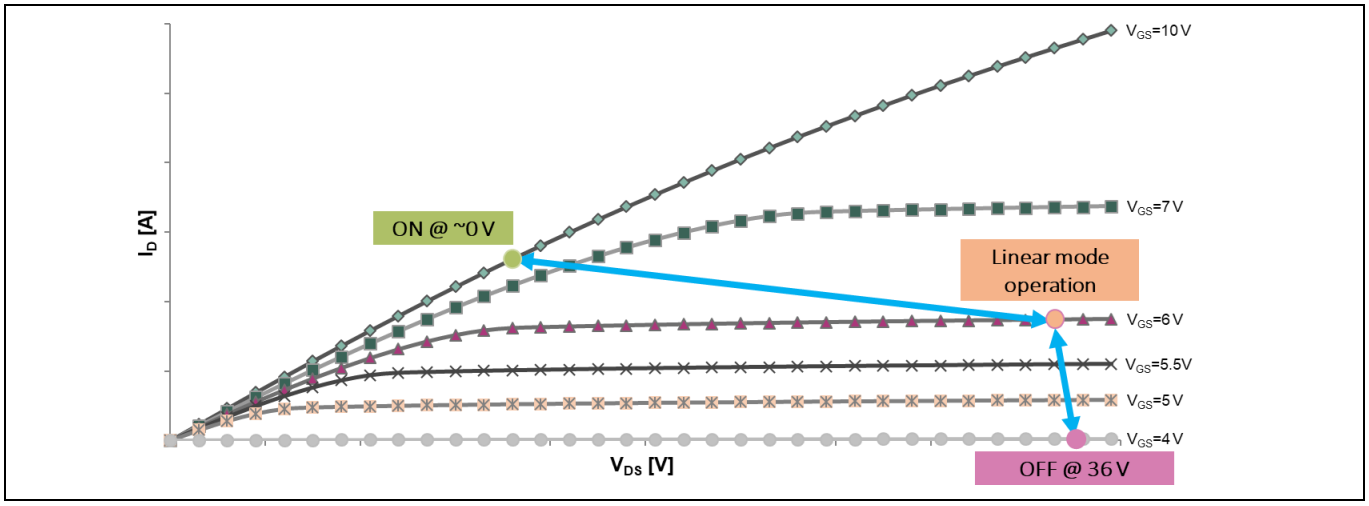

Figure 1 Output characteristic of the MOSFET during one switching period

In protection mode circuits, the MOSFET operates in linear mode for a considerable amount of time (typically a few hundred microseconds up to several milliseconds), which makes OptiMOS™ Linear FET a desirable option. OptiMOS™ Linear FET offers a faster switching response compared to a standard MOSFET. It also provides lower transconductance, which helps with equal current sharing when two or more Linear FETs are operating in parallel. This helps limit the peak currents and improves the lifetime of bulk capacitors and battery packs.

In this application note we will discuss the differences between an OptiMOS™ Linear FET (**IPT008N06NM5LF**) and the equivalent standard MOSFET (**IPT007N06N**), which is optimized for low $R_{DS(on)}$, fast switching applications. The turn-on and turn-off behaviors when an inrush current and short-circuit scenario are introduced into the system, respectively, have been shown. The SOA calculations and comparisons for each condition were performed to exhibit the advantages of Linear FET over standard MOSFET. Finally, R_G-C_{GD}

selection guidance for the gate drive circuit is provided to ensure the device does not avalanche and also stays within the SOA limits.

This selection guidance can be used for the following devices:

Table 1 Linear FET portfolio

Voltage (V)	Part number
60	IPT008N06NM5LF
80	IPT013N08NM5LF
100	IPB017N10N5LF
	IPB020N10N5LF
	IPB033N10N5LF
150	IPB048N15N5LF
	IPB083N15N5LF
200	IPB110N20N3LF

2 Protection in battery-powered applications

2.1 Inrush current limiting

Figure 2 shows a typical battery-powered motor drive system with the bulk capacitors at the input. When the system is first powered on, the input capacitors draw large amounts of inrush current and this can easily exceed the nominal load current. The peak of the inrush current depends on the amount of input capacitance installed, and can be several hundred amperes. A controlled charging of these capacitors is desirable to reduce the peak inrush currents. High inrush currents can adversely affect the overall lifetime of the battery and the input bulk capacitors. To help limit this current, Linear FET can be used as a protection switch, as it enables a controlled inrush current profile and has larger SOA limits for linear mode robustness.

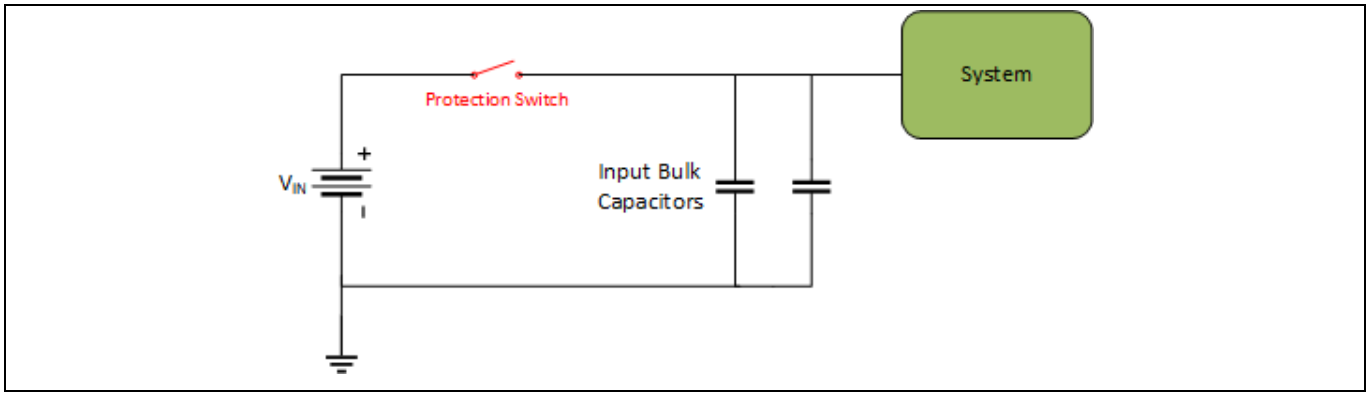

Figure 2 Linear FET as a protection switch for inrush current limiting

2.2 Short-circuit protection

Generally, in battery-powered motor drive systems, short-circuit events happen due to several reasons, with the most common being the inverter FETs failing or the motor winding getting shorted. When a short-circuit occurs in the system, the battery terminals will also be shorted, which can result in very large currents being drawn out of it. These large currents can damage the battery and other components in the system. During such events, it is important to disconnect the battery from the system as quickly as possible, before it causes any system damage, fire hazards or serious injuries. This can be achieved by using a Linear FET as a protection switch between the battery and the inverter (as shown in **Figure 3**).

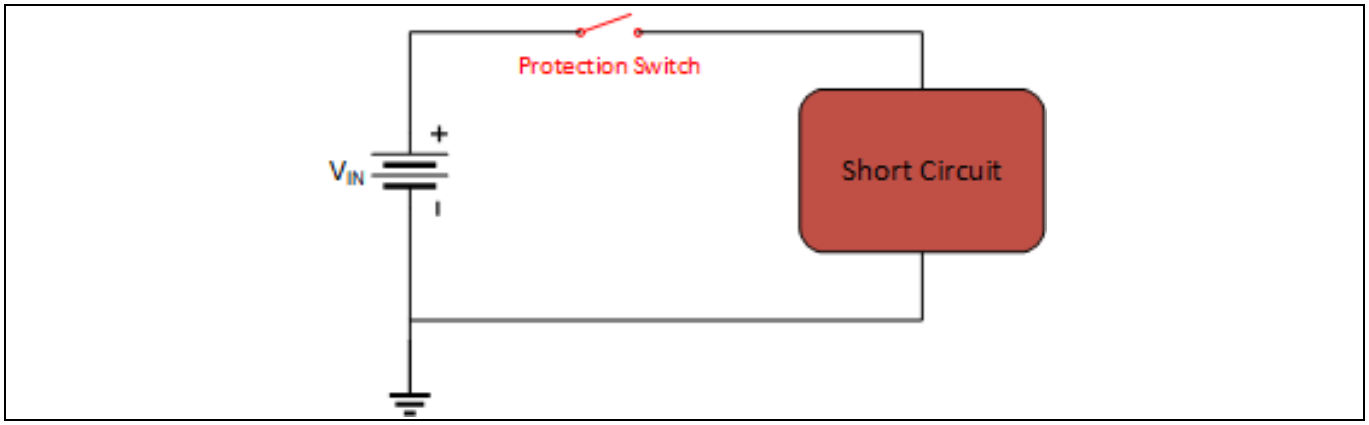

Figure 3 Linear FET as a protection switch during short-circuit

3 Importance of the safe operating area

The safe operating area (SOA) of a MOSFET defines the maximum allowable current and voltage range where a power MOSFET can be safely operated. **Figure 4** shows a typical SOA diagram for a MOSFET. The boundary of the SOA consists of five limits, and within these limit-lines the green shaded area shows where the MOSFET can be safely operated. The limit lines defining the SOA diagram are the $R_{DS(on)}$ limit, the package limit, the maximum power limit, the thermal stability limit, and the breakdown voltage limit. During linear mode operation, the most critical constraints are the maximum power limit and the thermal stability limit.

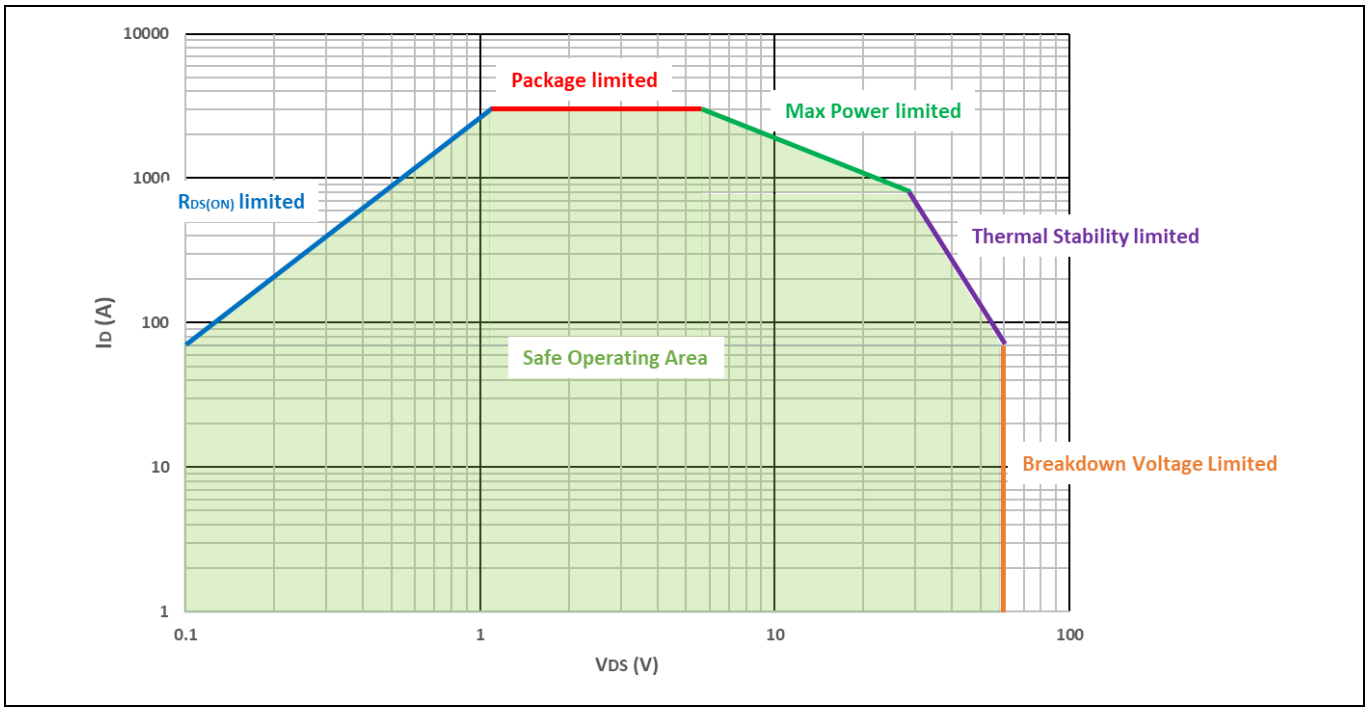

Figure 4 SOA of a MOSFET

When the MOSFET is conducting, the current (I_D) is flowing through it, and the voltage drop across the MOSFET ($V_{DS(on)}$) can be expressed as the product of I_D and $R_{DS(on)}$. In this case the MOSFET is operating in the $R_{DS(on)}$-limited part of the SOA. The $R_{DS(on)}$ helps to limit the maximum short-circuit current that can flow in the circuit. During switching transients, the MOSFET sees both high current and high voltage across it. This corresponds to the "maximum power limit" and "thermal stability limit" sections in the SOA. These operating regions will be the main focus of this application note, to demonstrate the benefits of Linear FET, since they correspond to linear mode operation of the MOSFET. OptiMOS™ Linear FET is a unique product in the Infineon portfolio, providing high linear mode robustness as well as low conduction losses. This makes it a good choice for inrush current limiting, because it has a controlled current profile compared to standard MOSFET. It is also a good choice for short-circuit protection because of larger SOA at higher V_{DS}, as explained in **sections 5** and **6** in this application note.

4 Experimental setup

In this section, the experimental setup and schematic diagram for the inrush current and short-circuit scenarios are described. The objective was to find the same gate drive circuit optimization for the Linear FET that could be used for both the scenarios, and compare the performance with the corresponding standard MOSFET. All the tests were conducted on the same PCB by replacing the MOSFETs to eliminate differences caused by board-to-board variations.

4.1 Inrush current limiting

To emulate the inrush current scenario, an application board (as shown in **Figure 5**) was developed. On this board, the input capacitors of the typical system are emulated by the capacitor load, which is connected to the power supply using a protection MOSFET (shown in **Figure 2**). The board had provision for multiple capacitors to analyze and compare the inrush current limiting performance of the Linear FET to the standard MOSFET at different inrush current levels. This board can also accommodate two MOSFETs in parallel to investigate current sharing during inrush transients. For a single MOSFET, the capacitive load was varied from 1 × 470 µF to 3 × 470 µF, whereas for the two MOSFETs in parallel, the capacitive load was varied from 1 × 470 µF to 5 × 470 µF.

Figure 5 shows the schematic for the inrush current limiting test setup. In this setup, 10 mΩ current shunts were used for measuring the individual MOSFET switching currents. For a single MOSFET, only Q_1 was populated and the current was measured using Current Shunt 1. For two MOSFETs in parallel, both Q_1 and Q_2 were populated and the currents were measured using the respective current shunts. The gate drive circuit was tuned to obtain a controlled inrush current with Linear FET. For the gate resistors, a 50 kΩ resistor was selected for R_{Gon} and a 5 kΩ resistor was selected for R_{Goff} for both Q_1 and Q_2. An external C_{GD} of 1 nF was used for both the parallel MOSFETs. The R_G-C_{GD} selection is discussed in detail in **section 7**.

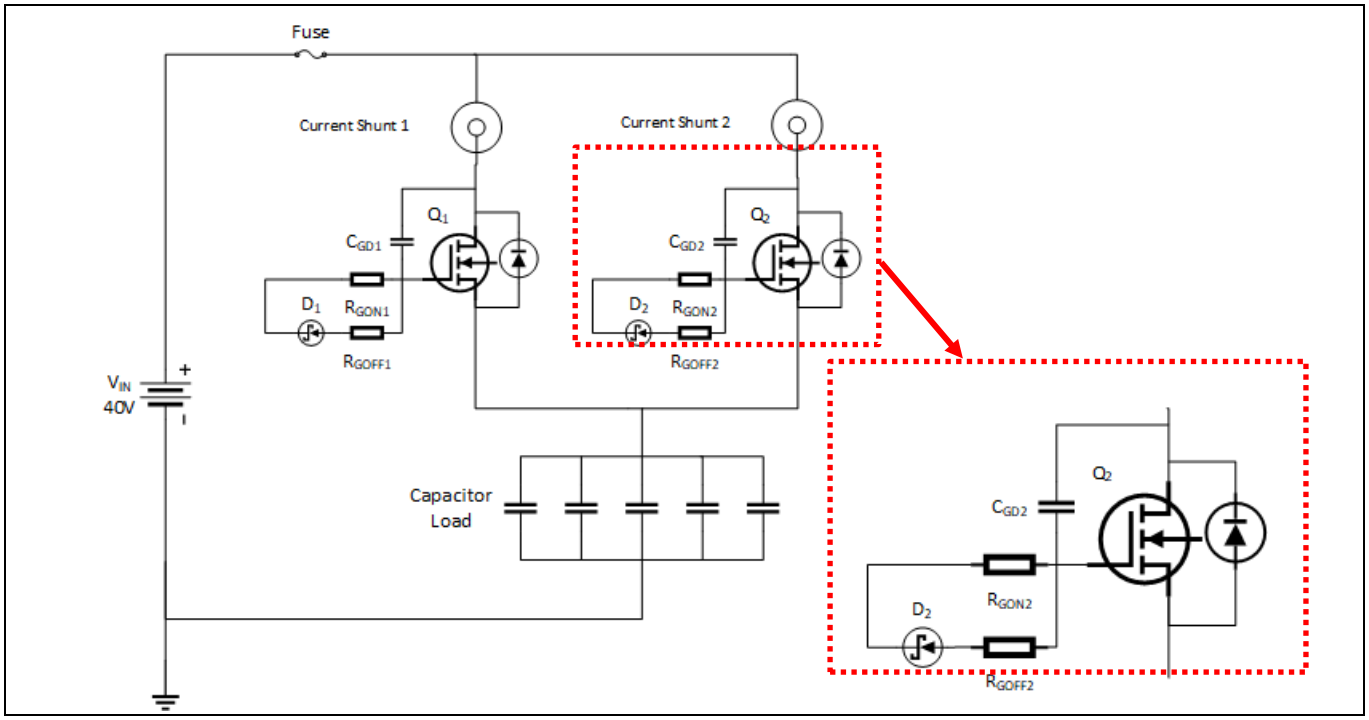

Figure 5 Schematic diagram for inrush current limiting setup

SOA analysis and waveform comparisons were performed to understand and compare the linear mode and current sharing capabilities of both the Linear FET and the corresponding standard MOSFETs, and is discussed in detail in **sections 5.1** and **6.1**.

4.2 Short-circuit protection

To emulate the short-circuit scenario, a 36 V battery was connected through an external resistor bank, R_{EXT} (0 to 1 Ω) to the input of the same application board used for inrush current limiting tests. This resistor bank was used to vary the short-circuit current levels and understand the performance at each current level. On the output side, the board has provision for connecting a contactor, which acts like the short in the system. The contactor resistance is 50 mΩ. For single MOSFET comparison, the short-circuit current was varied from 110 to 230 A. For two MOSFETs in parallel, the short-circuit current was varied from 240 to 460 A to have similar short-circuit current in each MOSFET as the single MOSFET test.

Figure 6 shows the schematic for short-circuit protection setup. In this setup, 10 mΩ current shunts were used for measuring the individual MOSFET switching currents. For a single MOSFET, only Q_1 was populated and the current was measured using Current Shunt 1. For two MOSFETs in parallel, both Q_1 and Q_2 were populated and the currents were measured using the respective current shunts. The gate drive circuit was tuned to obtain a controlled inrush current with Linear FET. For the gate resistors, a 50 kΩ resistor was selected for R_{GON} and a 5 kΩ resistor was selected for R_{GOFF} for both Q_1 and Q_2. An external C_{GD} of 1 nF was used for both the parallel MOSFETs. The R_G-C_{GD} selection is discussed in detail in **section 7**.

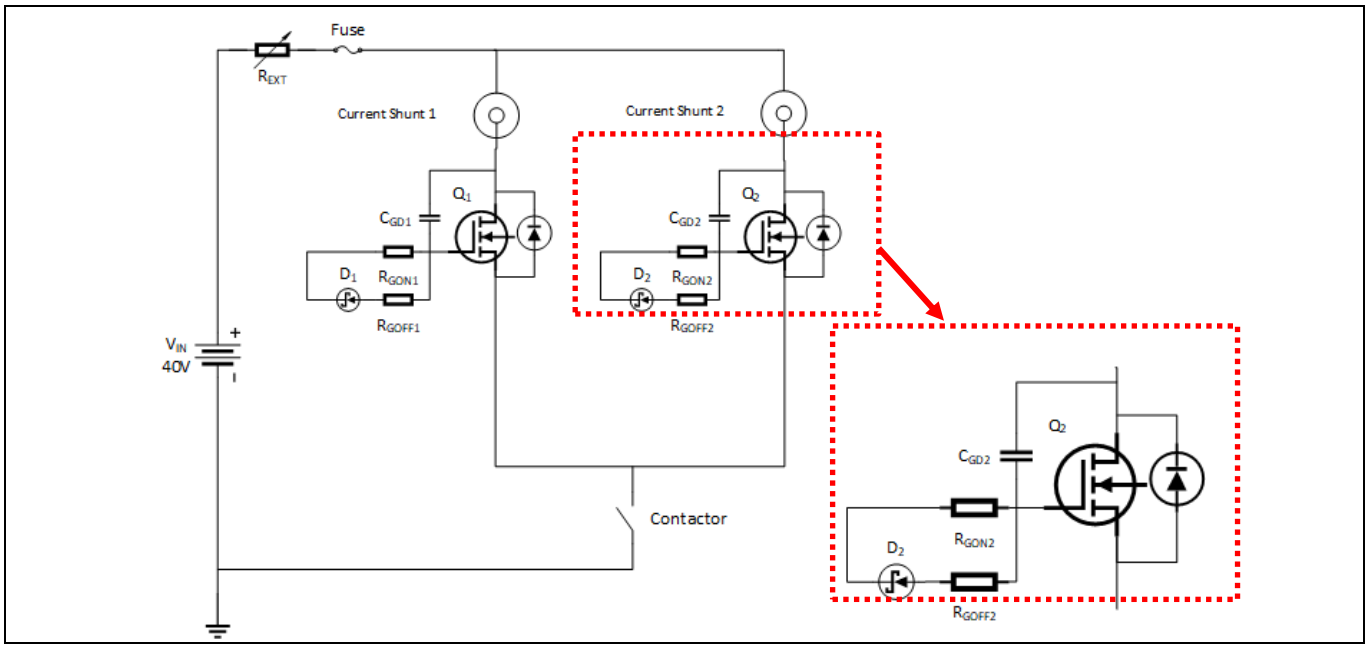

Figure 6 Schematic diagram for short-circuit protection setup

SOA analysis and waveform comparisons were performed to understand and compare the linear mode and current sharing capabilities of both the Linear FET and the corresponding standard MOSFETs and is discussed in detail in **sections 5.2** and **6.2**.

4.3 SOA calculations

To perform the SOA calculations, the following parameters are required. These parameters can be obtained using the switching waveforms. For example, peak power dissipation (P_{max}) and total energy dissipation (E_{tot}) can be calculated from the scope functions by multiplying V_{DS} and I_D and integrating the power curve over time, respectively.

Table 2 SOA calculation parameters

Parameter	Notation
Peak Power Dissipation	P_{max}
Total Energy Dissipation	E_{tot}
Pulse Width	t_{pul}
I_D at Peak Power Dissipation	$I_{D\,max}$
V_{DS} at Peak Power Dissipation	$V_{DS\,max}$

The peak power point (P_{max}) can be identified and the corresponding values of I_D at P_{max} (I_{Dmax}) and V_{DS} at P_{max} (V_{DSmax}) can be found on the oscilloscope. This value of I_{Dmax} and V_{DSmax} can be used for generating an equivalent square pulse for SOA and can be plotted on the SOA diagram. The pulse length (t_{pul}) for the switching scenario needs to be calculated as well. It can be calculated by dividing the total dissipated energy (E_{tot}) by P_{max}. This t_{pul} will provide the boundary for SOA. If the peak power point (V_{DSmax}, I_{Dmax}) lies inside this boundary line, then the device is operating safely.

5 Single standard MOSFET vs. Linear FET

In this section, the single MOSFET performances for standard MOSFET and Linear FET are compared for both inrush current and short-circuit scenarios.

5.1 Inrush current limiting

For inrush current limiting tests, the MOSFET performances from 1 × 470 µF to 3 × 470 µF capacitor load for both standard MOSFET and Linear FET are compared. The calculation for 1 × 470 µF and 3 × 470 µF are shown below. The SOA analysis for each condition is shown in **Table 3** to understand the SOA capability of each MOSFET.

$P_{max} = 1.7\ kW$

$E_{tot} = 0.265\ J$

$t_{pul} = 156\ \mu s$

$I_{Dmax} = 61.2\ A$

$V_{DSmax} = 27.8\ V$

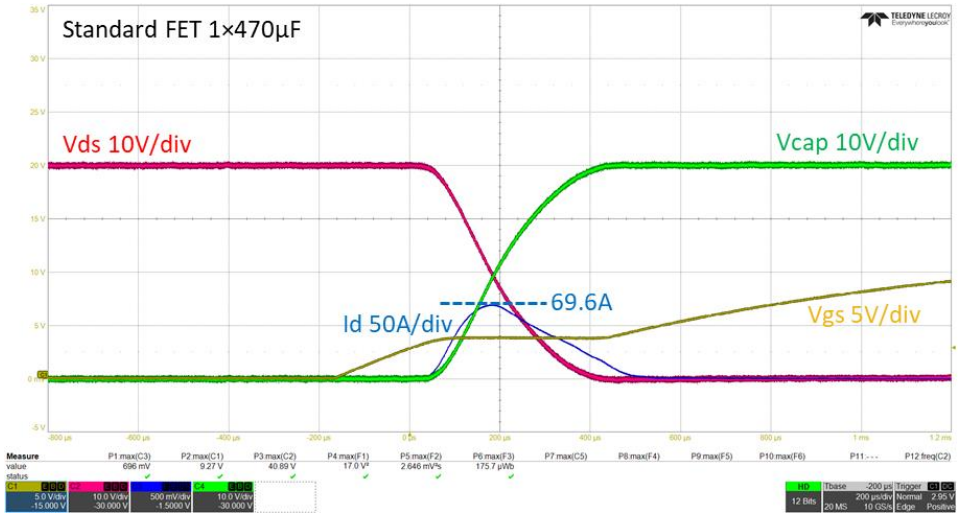

Figure 7 Inrush current for single standard MOSFET with 1 × 470 µF load

$P_{max} = 4.15\ kW$

$E_{tot} = 0.735\ J$

$t_{pul} = 177\ \mu s$

$I_{Dmax} = 152.5\ A$

$V_{DSmax} = 27.2\ V$

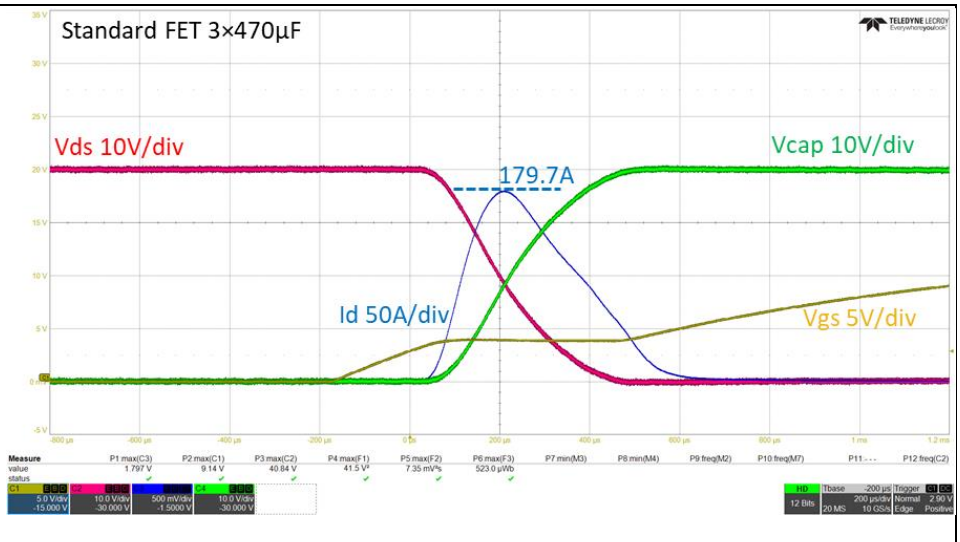

Figure 8 Inrush current for single standard MOSFET with 3 × 470 µF load

Plotting these pulse lines on the SOA of the standard MOSFET will give the corresponding SOA boundaries for each condition, as shown in **Figure 9**. **Figure 9** shows that when the capacitor load is 1 × 470 µF (blue line) the MOSFET is operating just inside the SOA boundary (blue point). When the load is increased to 3 × 470 µF (red line), the MOSFET is well outside the SOA boundary (red point).

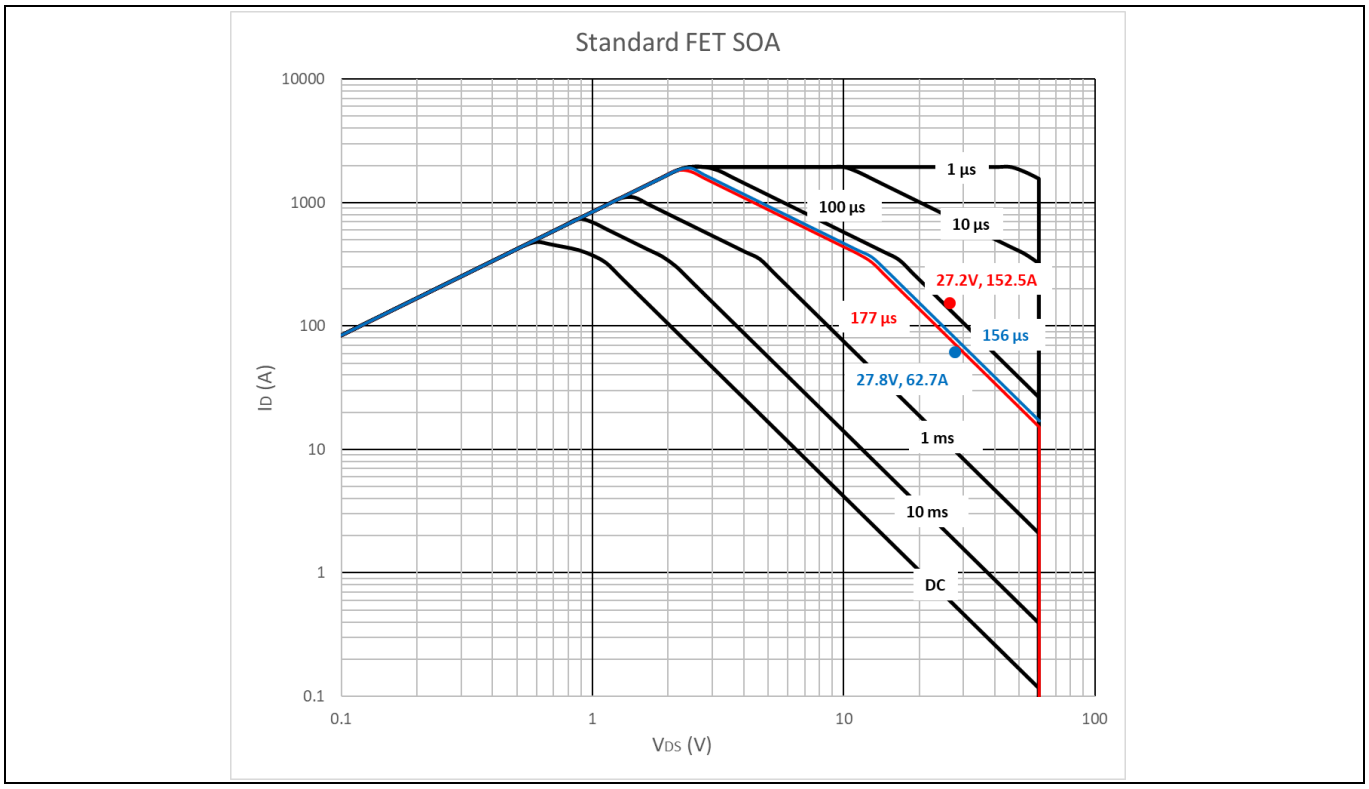

Figure 9 SOA analysis for single standard MOSFET for inrush current scenario

Performing the calculations for Linear FET for the same capacitor load conditions gives the following pulse widths.

$$P_{max} = 1.66\ kW$$

$$E_{tot} = 0.260\ J$$

$$t_{pul} = 157\ \mu s$$

$$I_{Dmax} = 53.9\ A$$

$$V_{DSmax} = 30.8\ V$$

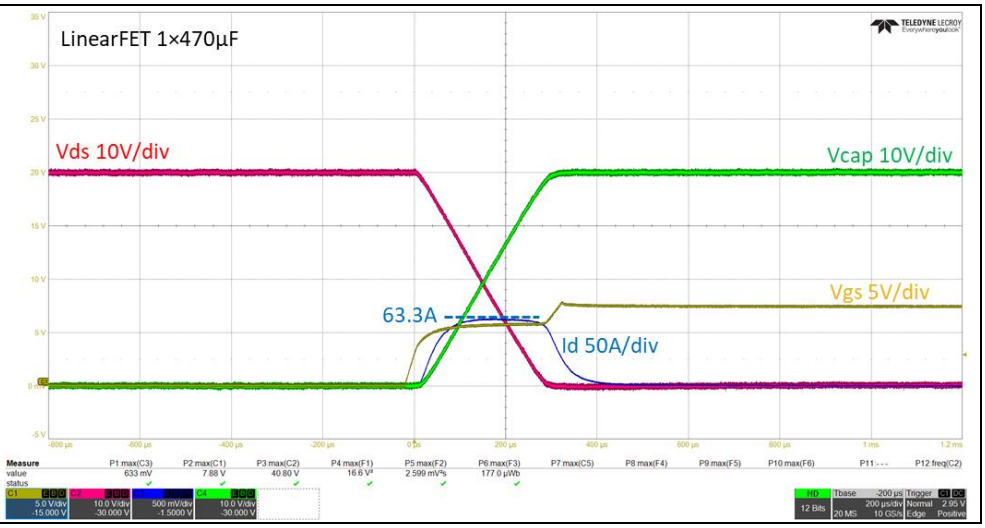

Figure 10 Inrush current for single standard MOSFET with 1 × 470 µF load

$P_{max} = 3.37\ kW$

$E_{tot} = 0.775\ J$

$t_{pul} = 230\ \mu s$

$I_{Dmax} = 107.9\ A$

$V_{DSmax} = 31.2\ V$

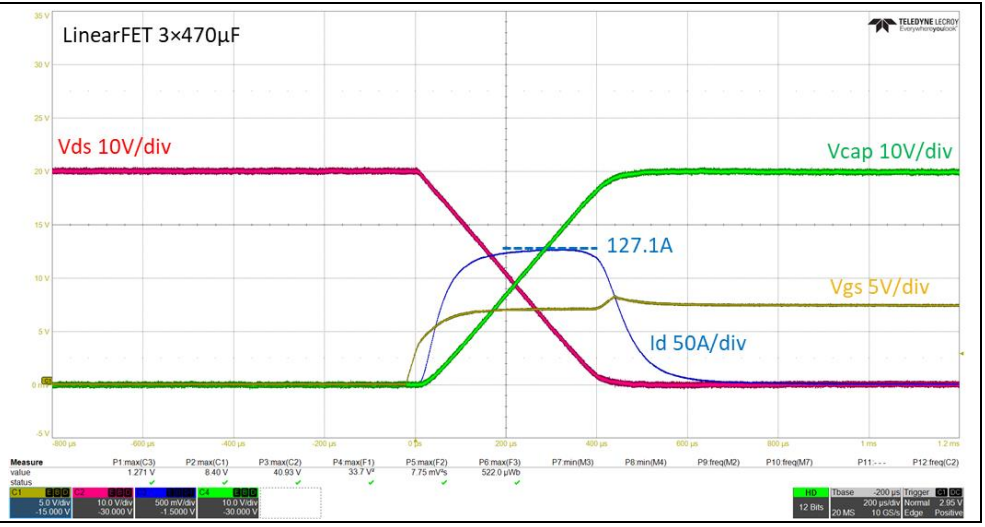

Figure 11 Inrush current for single standard MOSFET with 3 × 470 µF load

Plotting these pulse lines on the SOA of the Linear FET will give the corresponding SOA boundary for each condition, which is shown in **Figure 12**. **Figure 12** shows that when the capacitor load is 1 × 470 µF (blue line) the MOSFET is operating well inside the SOA boundary (blue point). When the load is increased to 3 × 470 µF (red line), the MOSFET is operating on the SOA boundary (red point).

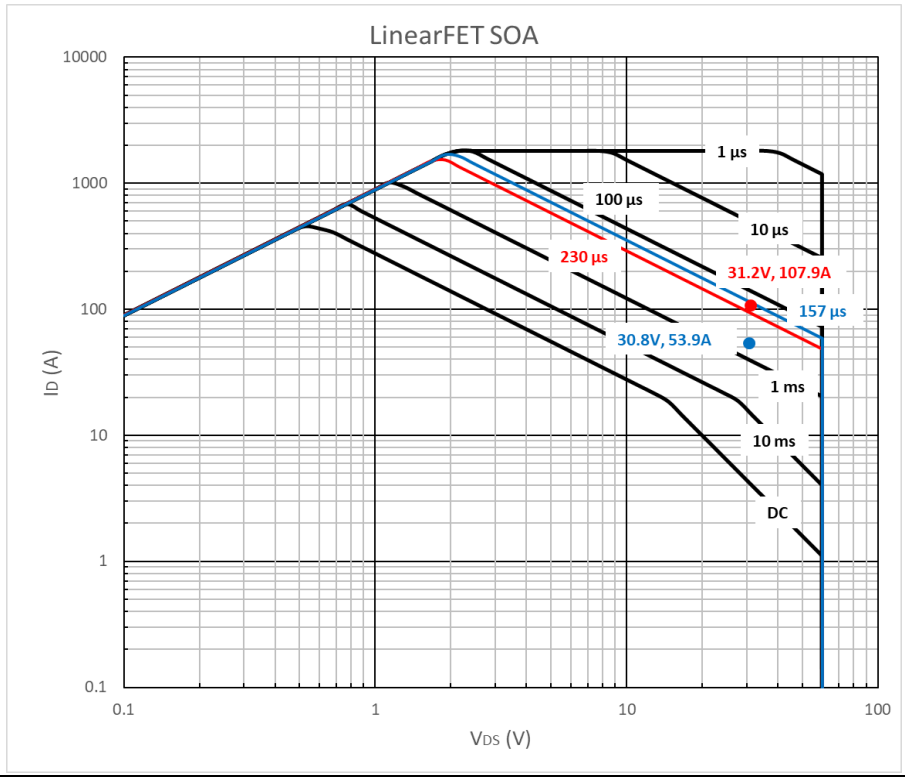

Figure 12 SOA analysis for a single Linear FET for inrush current scenario

The waveforms show that Linear FET has much better inrush current limiting capability. At 3 × 470 µF capacitive load, Linear FET has 53 A (~30 percent) lower current peak than the standard MOSFET. **Figure 9** and **Figure 12** also show that Linear FET has better SOA performance and can support ~3 times larger capacitor load during inrush.

Table 3 shows the SOA parameter values and the operating points for both standard MOSFET and Linear FET at all the test conditions.

Table 3 SOA analysis for single MOSFET during inrush current scenario

Part	Load	P_{max} (kW)	E_{tot} (J)	t_{pul} (µs)	I_{Dmax} (A)	V_{DSmax} (V)	SOA operating point
Standard MOSFET	1 × 470 µF	1.7	0.265	156	61.2	27.8	Inside
	2 × 470 µF	2.93	0.488	167	108.5	27	Outside
	3 × 470 µF	4.15	0.735	177	152.5	27.2	Outside
Linear FET	1 × 470 µF	1.66	0.26	156	53.9	30.8	Inside
	2 × 470 µF	2.64	0.515	195	85.6	30.4	Inside
	3 × 470 µF	3.37	0.775	230	107.8	31.2	Boundary

From the above table, it is clear that at all load levels, Linear FET has better SOA performance compared to standard MOSFET. This makes Linear FET a better choice for inrush current limiting as compared to standard MOSFET.

5.2 Short-circuit protection

For short-circuit protection tests, the MOSFET performances were compared during the turn-off transient at various short-circuit current levels from 110 to 230 A. The SOA calculations for 110 and 230 A conditions to determine the SOA operating point are shown. The SOA analysis for each condition is shown in **Table 4** to understand the protection capability of each MOSFET.

$P_{max} = 1.22\ kW$

$E_{tot} = 0.0705\ J$

$t_{pul} = 58\ \mu s$

$I_{Dmax} = 51.2\ A$

$V_{DSmax} = 23.8\ V$

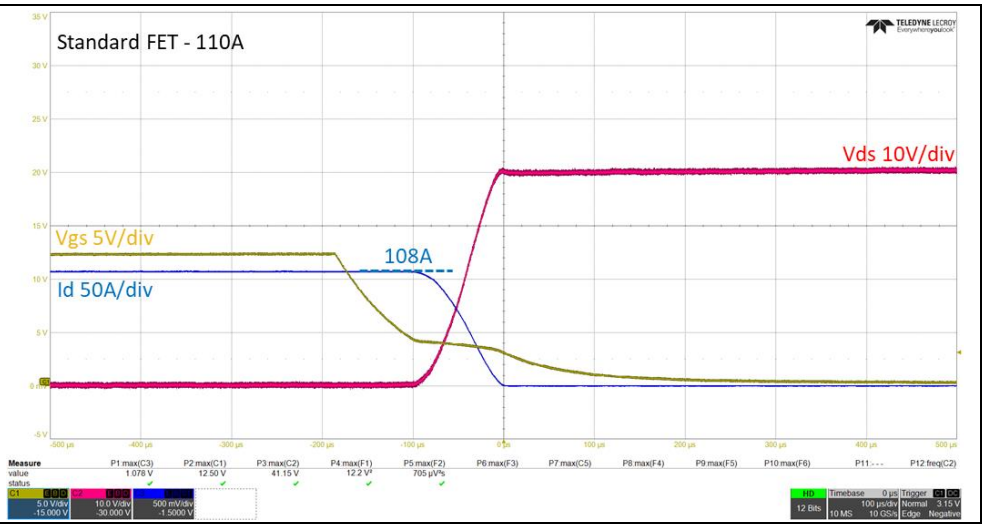

Figure 13 Short-circuit protection with single standard MOSFET at 110 A

$P_{max} = 2.91\ kW$

$E_{tot} = 0.152\ J$

$t_{pul} = 52\ \mu s$

$I_{Dmax} = 119.9\ A$

$V_{DSmax} = 24.3\ V$

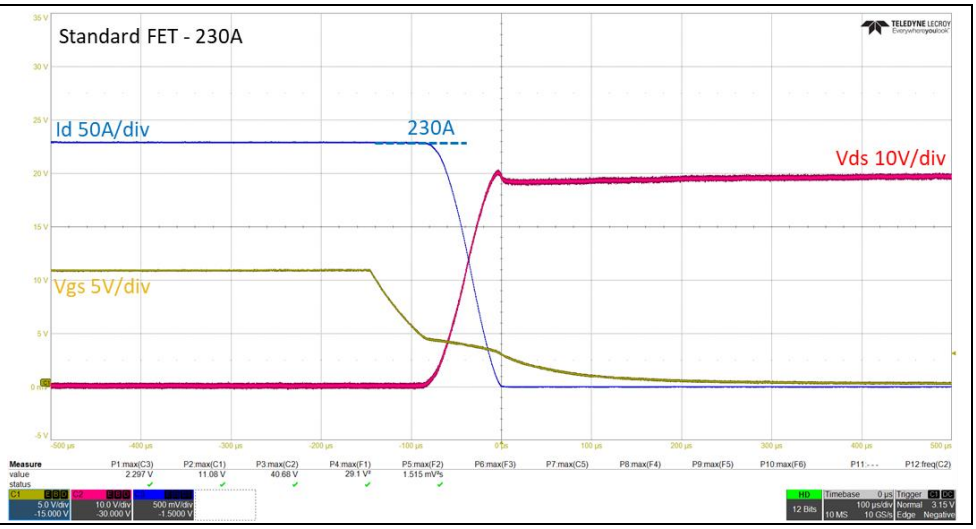

Figure 14 Short-circuit protection with single standard MOSFET at 230 A

Plotting these pulse lines on the SOA of the standard MOSFET will give the corresponding SOA boundary for each condition, which is shown in **Figure 15**.

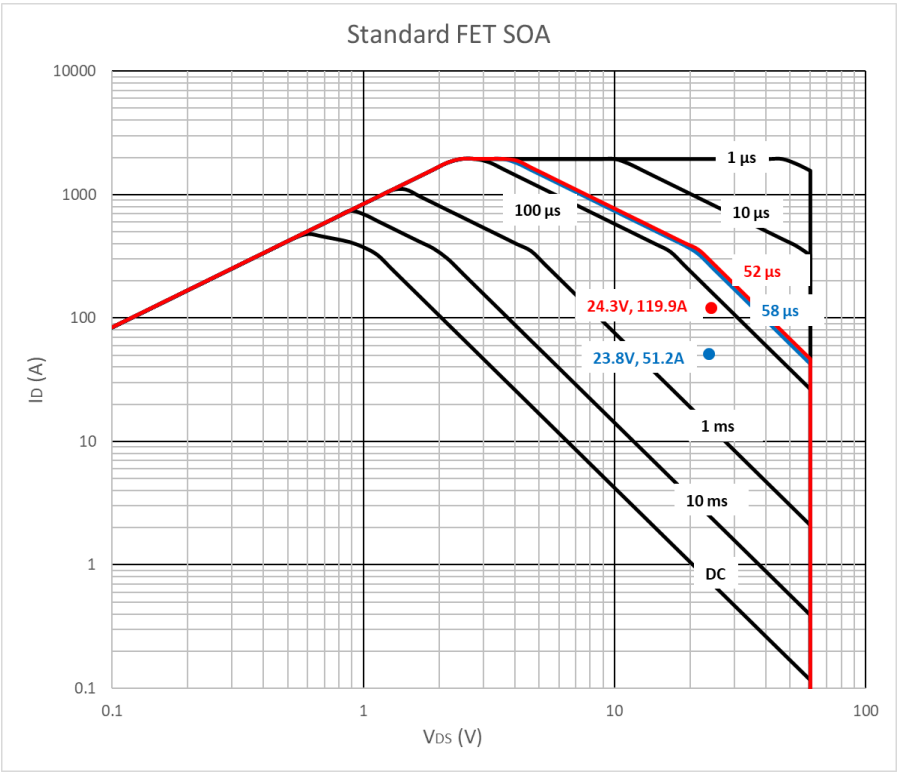

Figure 15 SOA analysis for single standard MOSFET during short-circuit scenario

Figure 15 shows that for both 110 A short-circuit current (blue line) and 230 A short-circuit current (red line), the MOSFET is operating inside the SOA.

Performing the calculations for Linear FET for the same conditions gives the following pulse widths.

$P_{max} = 1.41\ kW$

$E_{tot} = 0.0216\ J$

$t_{pul} = 15\ \mu s$

$I_{Dmax} = 62.7\ A$

$V_{DSmax} = 22.5\ V$

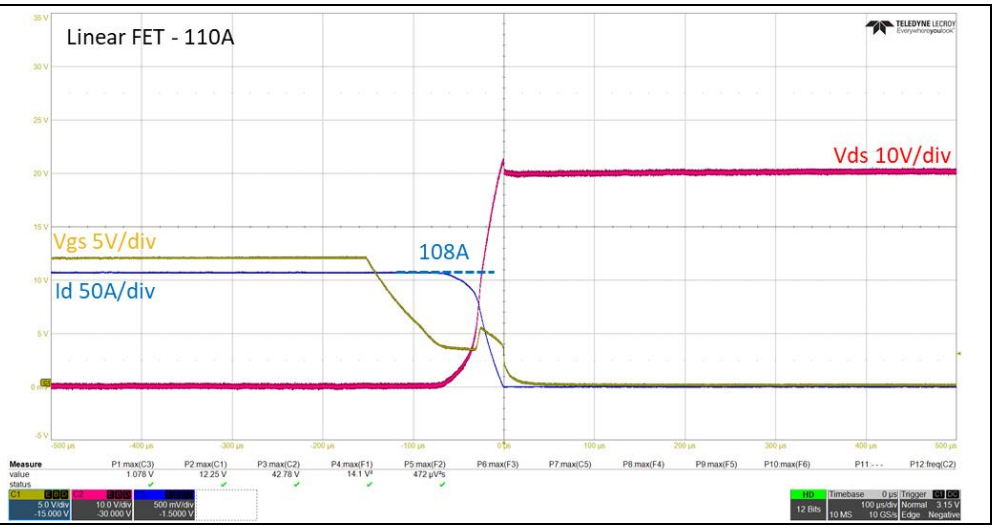

Figure 16 SCP with single Linear FET at 110 A

$P_{max} = 3.9\ kW$

$E_{tot} = 0.0405\ J$

$t_{pul} = 10\ \mu s$

$I_{Dmax} = 141.1\ A$

$V_{DSmax} = 27.6\ V$

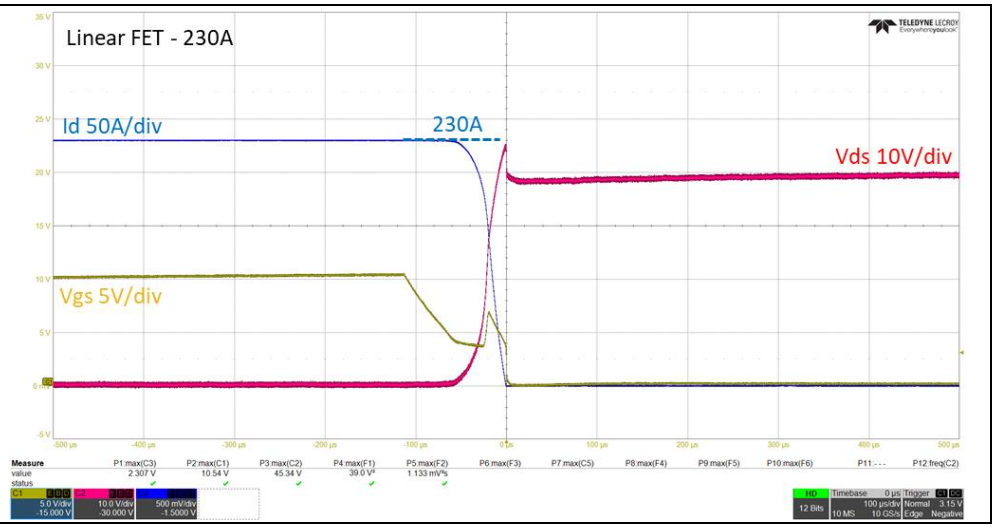

Figure 17 SCP with single Linear FET at 230 A

Plotting these pulse lines on the SOA of the Linear FET will give the corresponding SOA boundary for each condition, shown in **Figure 18**. It can be seen that for both 110 A short-circuit current (blue line) and 230 A short-circuit current (red line), the MOSFET is operating inside the SOA.

Table 4 shows the SOA parameter values and the operating points for both standard MOSFET and Linear FET at all the test conditions during short-circuit scenarios.

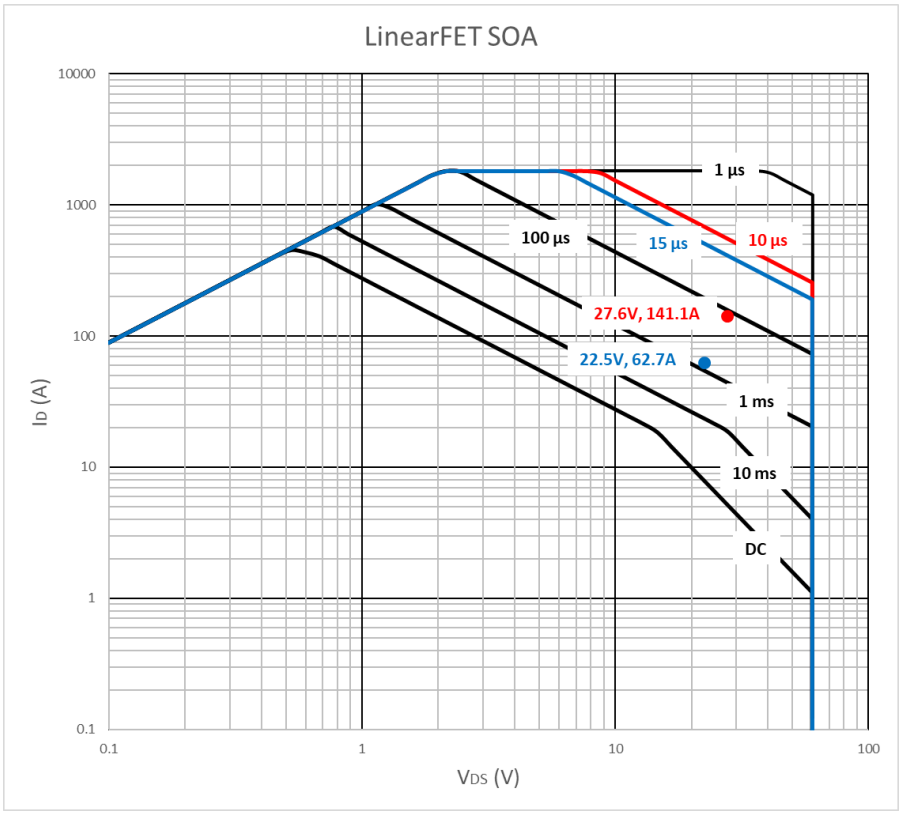

Figure 18 SOA analysis for single Linear FET during a short-circuit scenario

Table 4 SOA analysis for single MOSFET during a short-circuit scenario

Part	Current (A)	P_{max} (kW)	E_{tot} (J)	t_{pul} (µs)	I_{Dmax} (A)	V_{DSmax} (V)	SOA operating point
Standard MOSFET	110	1.22	0.0705	58	51.2	23.8	Inside
	150	1.71	0.0959	56	73.5	23.3	Inside
	180	2.15	0.116	54	92.8	23.2	Inside
	230	2.91	0.152	52	119.9	24.3	Inside
Linear FET	110	1.41	0.0216	15	62.7	22.5	Inside
	150	2.09	0.0268	13	89.5	23.4	Inside
	180	2.72	0.0314	12	108.2	25.1	Inside
	230	3.9	0.0405	10	141.1	27.6	Inside

Table 4 shows that Linear FET turns off much faster than standard MOSFET. It spends 80 percent less time in linear mode compared to standard MOSFET at all current levels without avalanching. This makes Linear FET a better choice for battery protection in the event of a short-circuit as compared to standard MOSFET.

6 Parallel standard MOSFET vs. Linear FET

In this section, the parallel MOSFET performances for standard MOSFET and Linear FET are compared for both inrush current and short-circuit scenarios. The current sharing between the parallel FETs during the turn-on and turn-off switching periods is also monitored to understand if the system can be scaled to higher load levels.

6.1 Inrush current limiting

For inrush current limiting tests, the MOSFET performances from 1 × 470 µF to 5 × 470 µF capacitor load for both standard MOSFET and Linear FET are compared. The calculations for 1 × 470 µF and 5 × 470 µF are shown below. The SOA analysis for Q_1 and Q_2 for each condition is shown in **Table 5** to understand the SOA capability of each MOSFET and current sharing between parallel FETs.

$$P_{\max Q1} = 1.23\ kW$$
$$E_{totQ1} = 0.188\ J$$
$$t_{pulQ1} = 153\ \mu s$$
$$I_{D\max Q1} = 45.7\ A$$
$$V_{DS\max Q1} = 26.9\ V$$

$$P_{\max Q2} = 0.52\ kW$$
$$E_{totQ2} = 0.076\ J$$
$$t_{pulQ2} = 146\ \mu s$$
$$I_{D\max Q2} = 19.1\ A$$
$$V_{DS\max Q2} = 27.2\ V$$

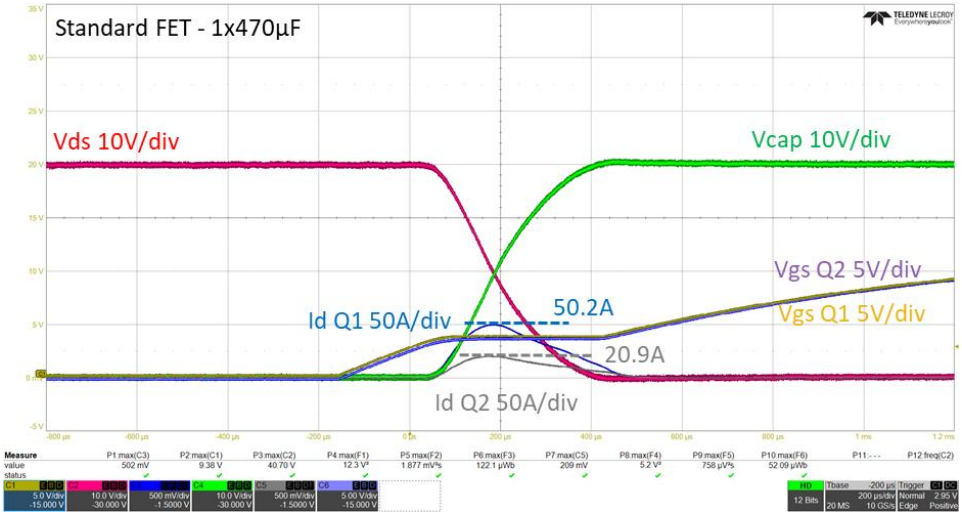

Figure 19 Inrush current for parallel standard MOSFETs with 1 x 470 µF load

$$P_{\max Q1} = 3.83\ kW$$
$$E_{totQ1} = 0.686\ J$$
$$t_{pulQ1} = 179\ \mu s$$
$$I_{D\max Q1} = 148.6\ A$$
$$V_{DS\max Q1} = 25.8\ V$$

$$P_{\max Q2} = 2.89\ kW$$
$$E_{totQ2} = 0.519\ J$$
$$t_{pulQ2} = 180\ \mu s$$
$$I_{D\max Q2} = 112.1\ A$$
$$V_{DS\max Q2} = 25.8\ V$$

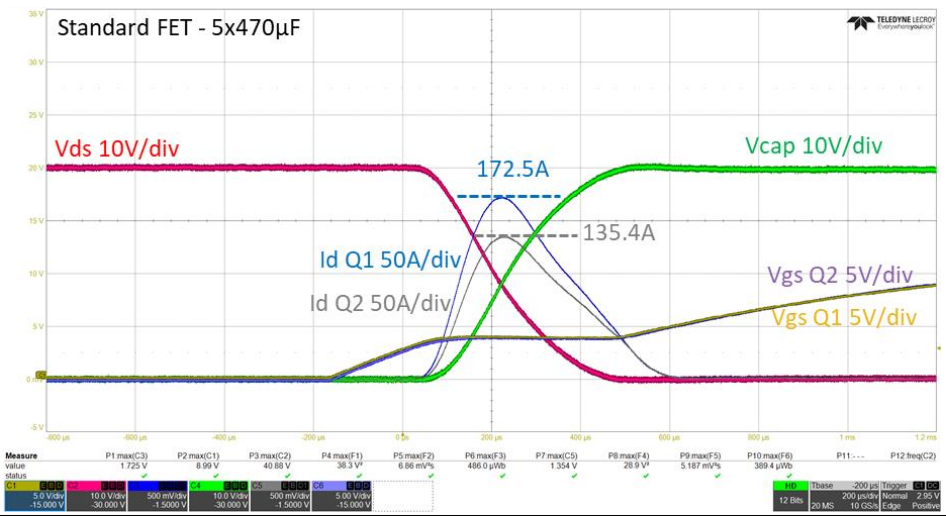

Figure 20 Inrush current for parallel standard MOSFETs with 5 x 470 µF load

Plotting the highest pulse widths from each condition, which will give the worst-case SOA, and peak power points for both Q_1 and Q_2 on the standard MOSFET SOA will give the SOA performance for MOSFET parallelization. This is shown in **Figure 21**.

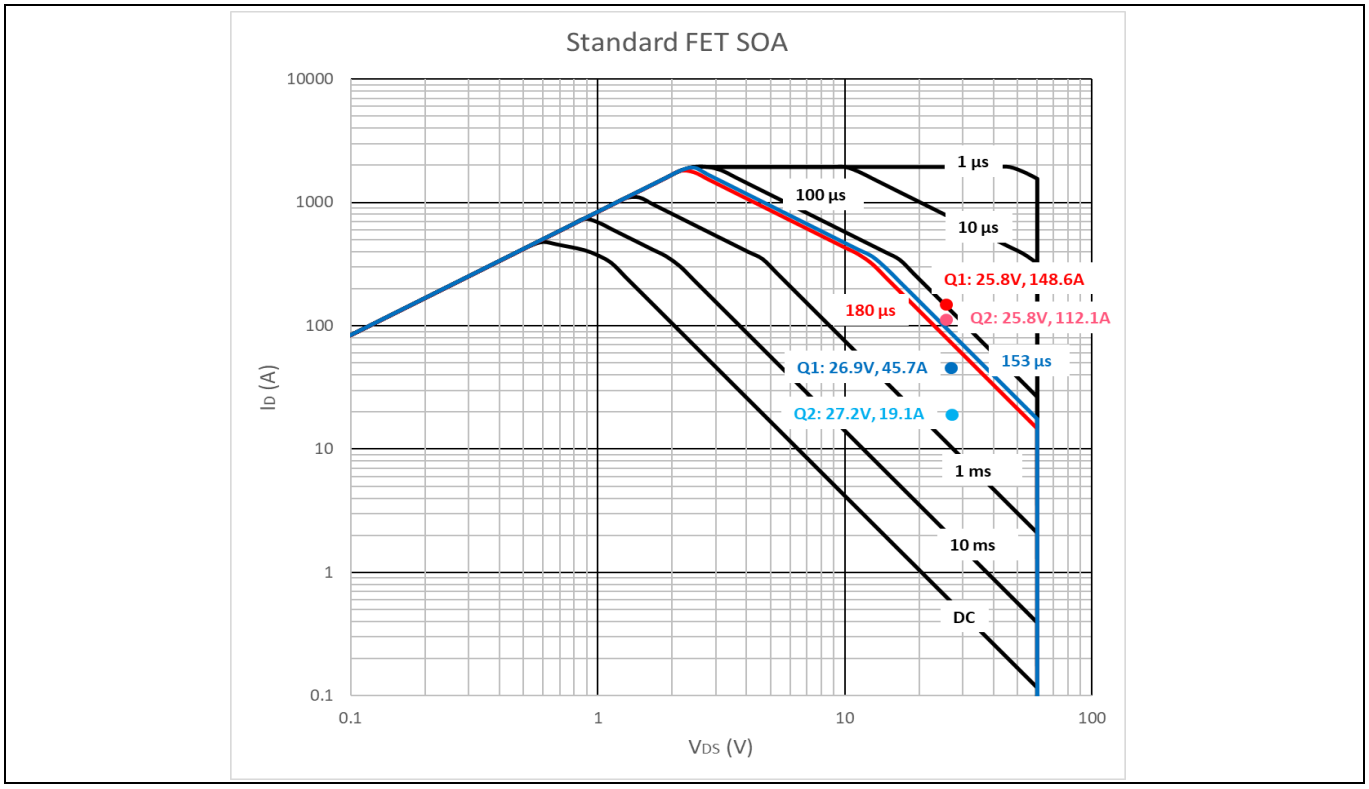

Figure 21 SOA analysis for parallel standard MOSFETs during inrush current scenario

Figure 21 shows that when the capacitor load is 1 × 470 µF (blue line) the FETs are operating inside the SOA boundary (Q_1: blue point, Q_2: light-blue point). When the load is increased to 5 × 470 µF (red line), both FETs are well outside the SOA boundary (Q_1: red point, Q_2: light-red point).

Performing the calculations for parallel Linear FET for the same conditions gives the following pulse widths and operating points.

$$P_{\max Q1} = 0.93\ kW$$
$$E_{totQ1} = 0.127\ J$$
$$t_{pulQ1} = 137\ \mu s$$
$$I_{D\max Q1} = 30.8\ A$$
$$V_{DS\max Q1} = 30.2\ V$$

$$P_{\max Q2} = 0.93\ kW$$
$$E_{totQ2} = 0.133\ J$$
$$t_{pulQ2} = 143\ \mu s$$
$$I_{D\max Q2} = 30.9\ A$$
$$V_{DS\max Q2} = 30.1\ V$$

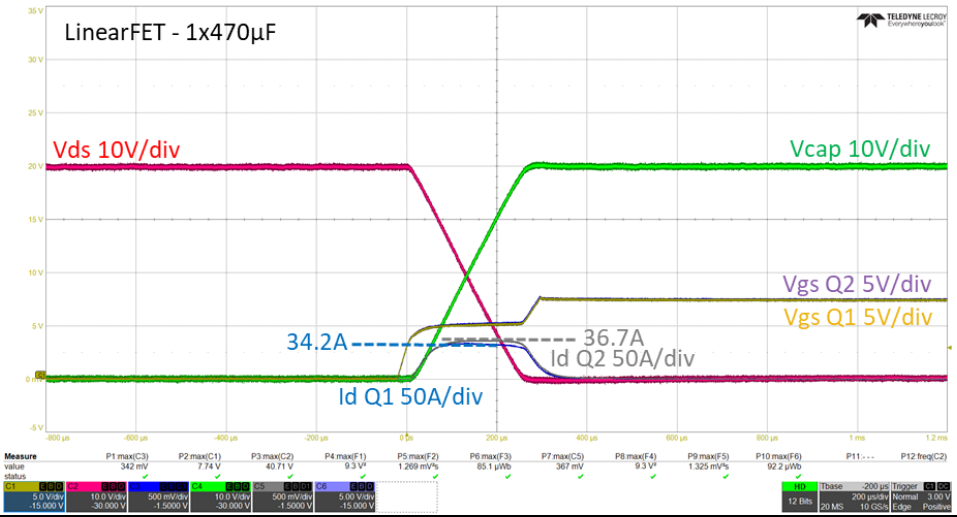

Figure 22 Inrush current for parallel Linear FETs with 1 x 470 µF load

$P_{\max Q1} = 3.04\ kW$
$E_{totQ1} = 0.606\ J$
$t_{pulQ1} = 199\ \mu s$
$I_{D\max Q1} = 103.3\ A$
$V_{DS\max Q1} = 29.4\ V$

$P_{\max Q2} = 3.04\ kW$
$E_{totQ2} = 0.602 J$
$t_{pulQ2} = 198\ \mu s$
$I_{D\max Q2} = 103.5\ A$
$V_{DS\max Q2} = 29.4\ V$

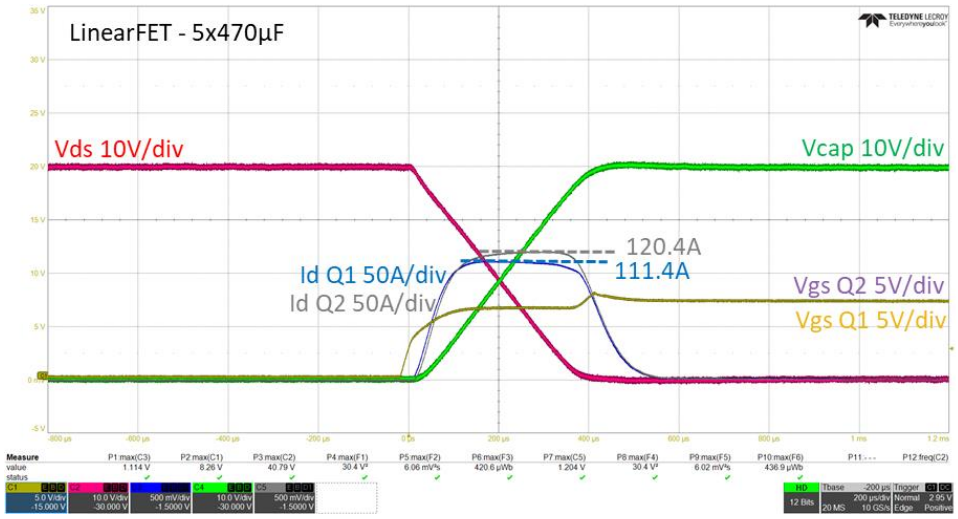

Figure 23 Inrush current for parallel Linear FETs with 5 x 470 µF load

Plotting the highest pulse widths from each condition, which will give the worst-case SOA, and peak power points for both Q_1 and Q_2 on the Linear FET SOA will give the SOA performance for MOSFET parallelization. This is shown in **Figure 24**. Since both the FETs have very similar peak power points, they can't be distinguished on the SOA.

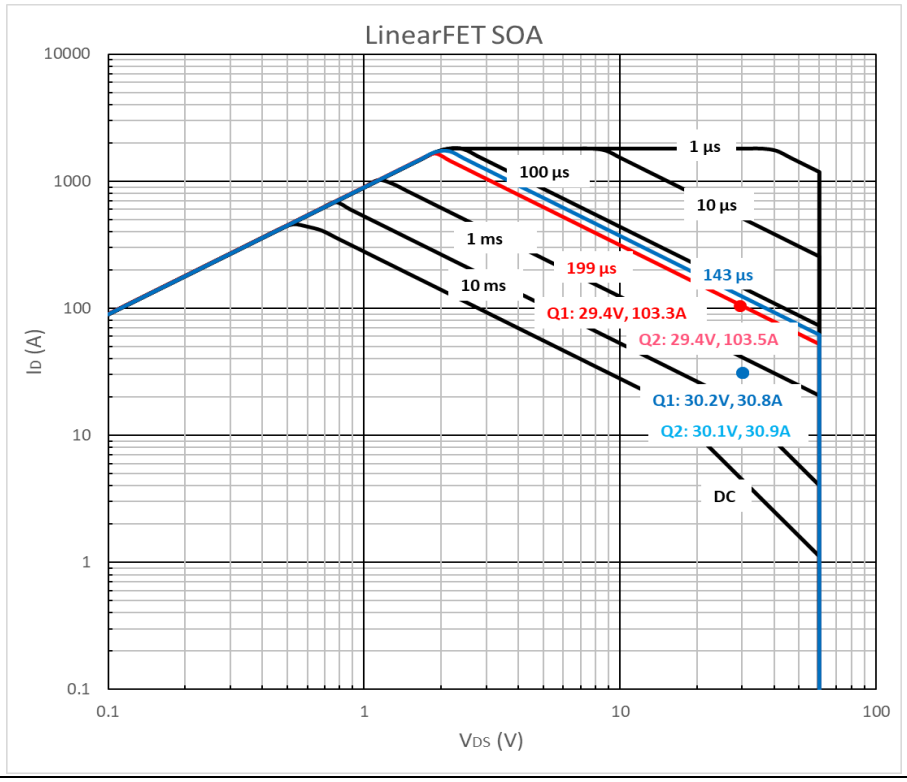

Figure 24 SOA analysis for parallel Linear FETs during inrush current scenario

Figure 24 shows that when the capacitor load is 1 × 470 µF (blue line) the FETs are operating inside the SOA boundary (Q_1: blue point, Q_2: light-blue point). When the load is increased to 5 × 470 µF (red line), both FETs are well on the SOA boundary (Q_1: red point, Q_2: light-red point).

Table 5 shows the SOA parameter values and the operating points for both standard MOSFET and Linear FET at all the test conditions.

Table 5 SOA analysis for parallel FETs during inrush current scenario

Part	Load	MOSFET	I_{PEAK} (A)	P_{max} (kW)	E_{tot} (J)	t_{pul} (µs)	I_{Dmax} (A)	V_{DSmax} (V)	SOA operating point
Standard MOSFET	1 × 470 µF	Q_1	50.2	1.23	0.188	153	45.7	26.9	Inside
		Q_2	20.9	0.52	0.076	146	19.1	27.2	Inside
	2 × 470 µF	Q_1	100.6	2.42	0.381	157	88.9	27.2	Outside
		Q_2	36.5	0.82	0.127	155	29.9	27.4	Inside
	3 × 470 µF	Q_1	119.2	2.78	0.467	168	102.9	27	Outside
		Q_2	78	1.73	0.288	166	63.4	27.3	Inside
	4 × 470 µF	Q_1	146.2	3.33	0.583	175	128.8	25.9	Outside
		Q_2	108.6	2.36	0.412	175	91.2	25.9	Outside
	5 × 470 µF	Q_1	172.5	3.83	0.686	179	148.6	25.8	Outside
		Q_2	135.4	2.89	0.519	180	112.1	25.8	Outside
Linear FET	1 × 470 µF	Q_1	34.2	0.93	0.127	137	30.8	30.2	Inside
		Q_2	36.7	0.93	0.133	143	30.9	30.1	Inside
	2 × 470 µF	Q_1	60.5	1.60	0.245	153	55.6	28.8	Inside
		Q_2	65	1.64	0.255	156	56.9	28.8	Inside
	3 × 470 µF	Q_1	82.9	2.20	0.366	166	73.9	29.8	Inside
		Q_2	86	2.18	0.351	161	73.2	29.8	Inside
	4 × 470 µF	Q_1	97.5	2.62	0.481	184	89.8	29.2	Inside
		Q_2	105.5	2.70	0.49	181	92.7	29.1	Inside
	5 × 470 µF	Q_1	111.4	3.04	0.606	199	103.3	29.4	Boundary
		Q_2	120.4	3.04	0.602	198	103.5	29.4	Boundary
	6 × 470 µF	Q_1	121.7	3.30	0.724	219	110.6	29.8	Outside
		Q_2	133	3.43	0.745	217	115	29.8	Outside

Table 5 shows that parallelization of Linear FET has better SOA performance for both Q_1 and Q_2 as compared to standard MOSFET. Comparing this to Table 3, it can be concluded that adding multiple Linear FETs in parallel helps scale the maximum capacitive load capability because of equal current sharing. Meanwhile, having multiple parallel standard MOSFETs does not scale, as one MOSFET is operating outside the SOA due to highly unequal current sharing. This makes Linear FET a better choice for high inrush current scenarios, as it can be scaled up by adding multiple FETs in parallel, which is not possible for standard MOSFET.

6.2 Short-circuit protection

For short-circuit protection tests, the MOSFET performances were compared during the turn-off transient at various short-circuit current levels from 240 to 460 A. The SOA calculations for 240 and 460 A conditions to determine the SOA operating point are shown. The SOA analysis for Q_1 and Q_2 for each condition is shown in Table 6 to understand the SOA capability of each MOSFET and current sharing between two parallel MOSFETs.

$P_{\max Q1} = 1.53\ kW$
$E_{totQ1} = 0.0792\ J$
$t_{pulQ1} = 52\ \mu s$
$I_{D\max Q1} = 68.5\ A$
$V_{DS\max Q1} = 22.3\ V$

$P_{\max Q2} = 1.35\ kW$
$E_{totQ2} = 0.0705\ J$
$t_{pulQ2} = 52\ \mu s$
$I_{D\max Q2} = 52.1\ A$
$V_{DS\max Q2} = 25.9\ V$

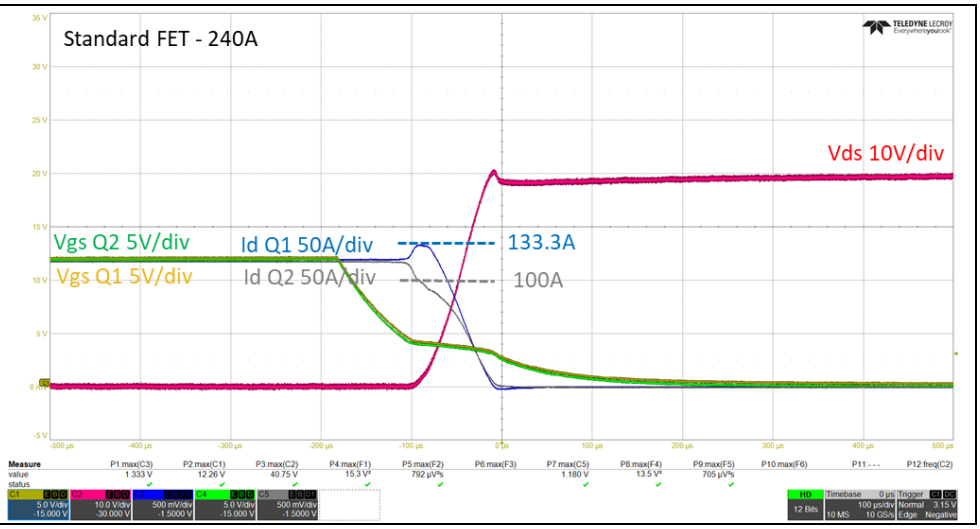

Figure 25 Short-circuit protection with parallel standard MOSFETs at 240 A

$P_{\max Q1} = 3.57\ kW$
$E_{totQ1} = 0.17\ J$
$t_{pulQ1} = 48\ \mu s$
$I_{D\max Q1} = 139.3\ A$
$V_{DS\max Q1} = 25.6\ V$

$P_{\max Q2} = 3.33\ kW$
$E_{totQ2} = 0.159\ J$
$t_{pulQ2} = 48\ \mu s$
$I_{D\max Q2} = 117.1\ A$
$V_{DS\max Q2} = 28.4\ V$

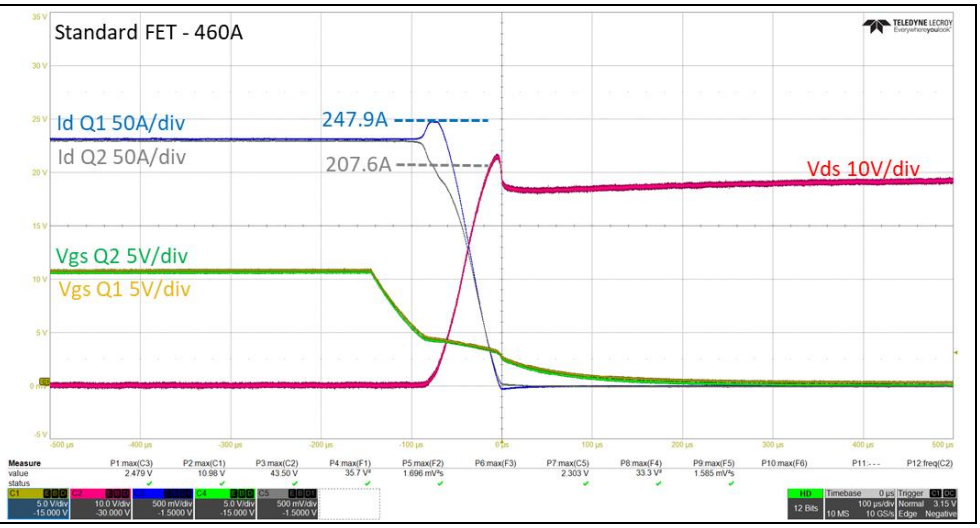

Figure 26 Short-circuit protection with parallel standard MOSFETs at 460 A

Figure 25 and **Figure 26** show that there is significant difference between the currents in Q_1 and Q_2 when they are turning off.

By plotting the pulse widths and peak power points for both Q_1 and Q_2 from each condition on the standard MOSFET SOA, we can evaluate the MOSFET performance during parallelization. This is shown in **Figure 27**.

Figure 27 shows that for both short-circuit current levels 240 A (blue line) and 460 A (red line) the FETs are operating inside the SOA boundary (Q_1: blue point, Q_2: light-blue point for 240 A and Q_1: red point, Q_2: light-red point for 460 A).

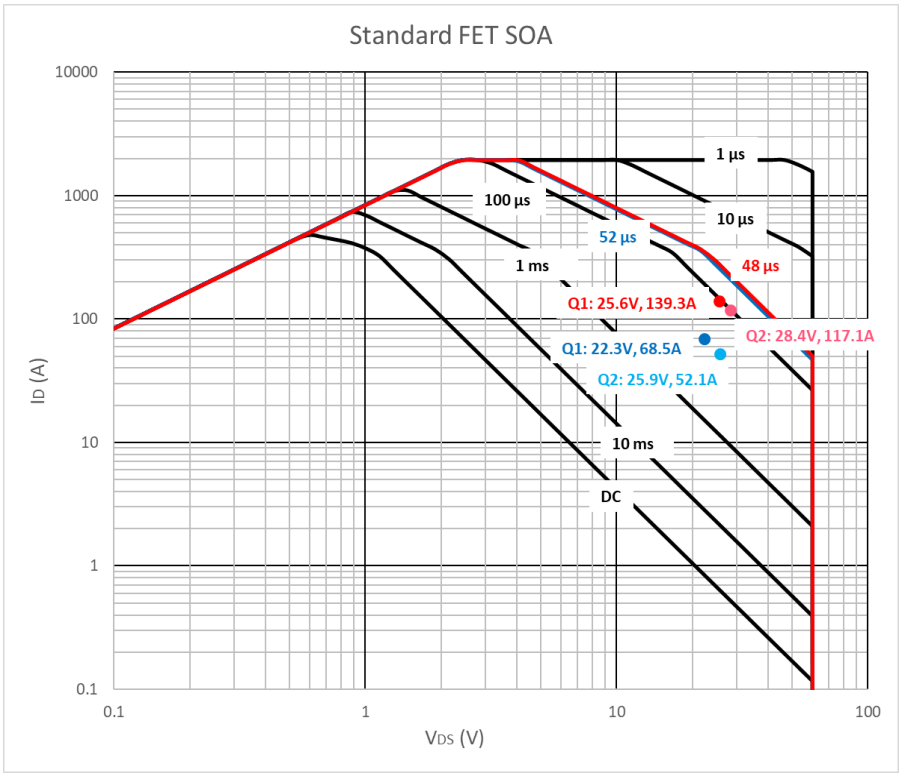

Figure 27 SOA analysis for parallel standard MOSFETs during short-circuit scenario

Performing the calculations for two Linear FETs in parallel for the same short-circuit conditions gives the following pulse widths and operating points.

$$P_{\max Q1} = 1.73\ kW$$
$$E_{totQ1} = 0.0282\ J$$
$$t_{pulQ1} = 16\ \mu s$$
$$I_{D\max Q1} = 76.6\ A$$
$$V_{DS\max Q1} = 22.6\ V$$

$$P_{\max Q2} = 1.85\ kW$$
$$E_{totQ2} = 0.0325\ J$$
$$t_{pulQ2} = 18\ \mu s$$
$$I_{D\max Q2} = 81.2\ A$$
$$V_{DS\max Q2} = 22.8\ V$$

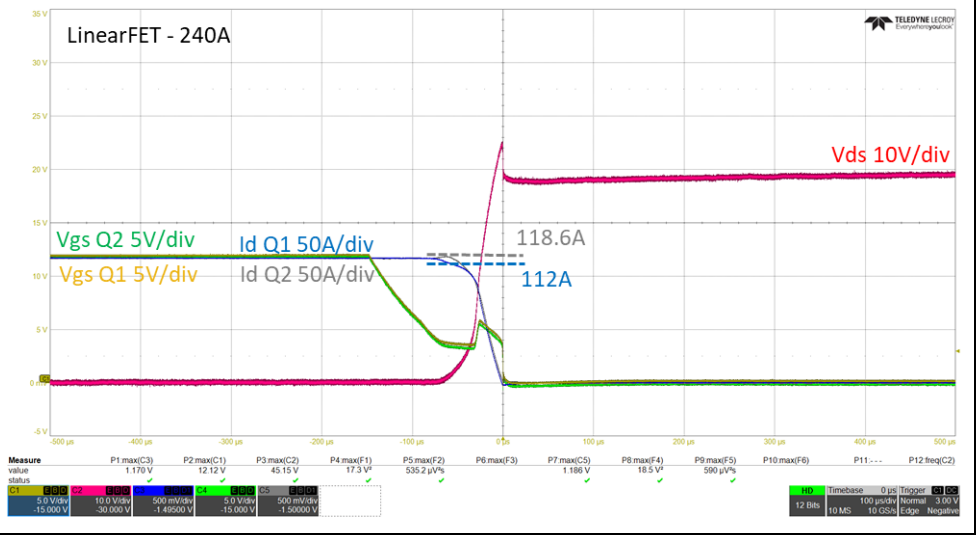

Figure 28 Short-circuit protection with parallel Linear FETs at 240 A

$P_{\max Q1} = 4.75kW$
$E_{totQ1} = 0.0657\ J$
$t_{pulQ1} = 14\ \mu s$
$I_{D\max Q1} = 144.5\ A$
$V_{DS\max Q1} = 32.9\ V$

$P_{\max Q2} = 5.00\ kW$
$E_{totQ2} = 0.0718\ J$
$t_{pulQ2} = 14\ \mu s$
$I_{D\max Q2} = 152.6\ A$
$V_{DS\max Q2} = 32.8\ V$

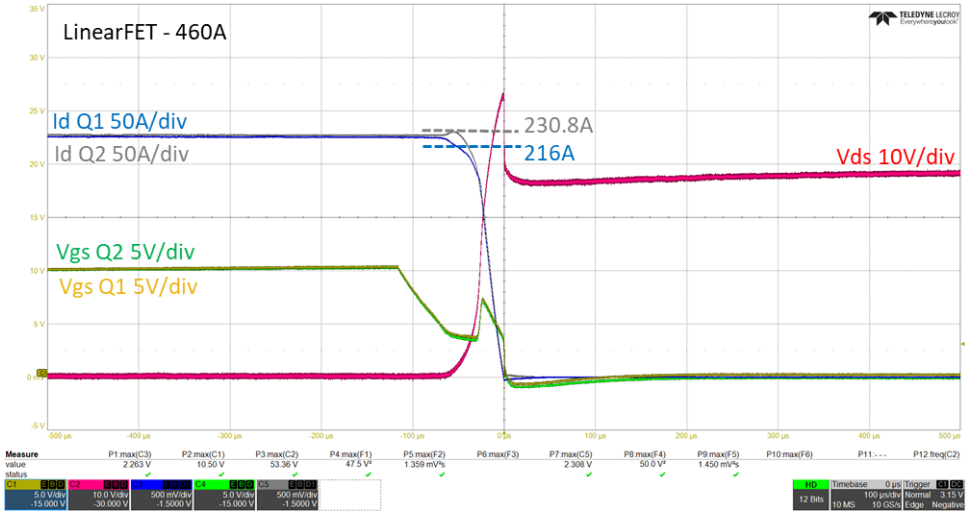

Figure 29 Short-circuit protection with parallel Linear FETs at 460 A

Figure 28 and **Figure 29** show that the currents in Q_1 and Q_2 when they are turning off are very similar for Linear FETs.

By plotting the pulse widths and peak power points for both Q_1 and Q_2 from each condition on the Linear FET SOA we can evaluate the Linear FET performance during parallelization. This is shown in **Figure 30**.

Figure 30 shows that for both short-circuit current levels 240 A (blue line) and 460 A (red line) the FETs are operating inside the SOA boundary (Q_1: blue point, Q_2: light-blue point for 240 A and Q_1: red point, Q_2: light-red point for 460 A).

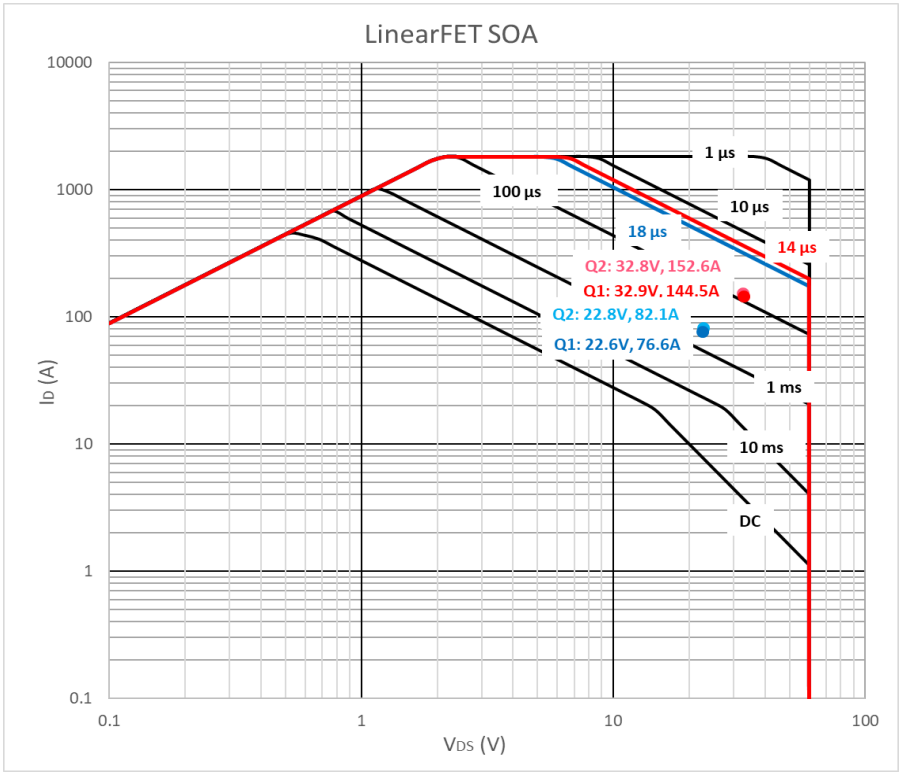

Figure 30 SOA analysis for parallel Linear FETs during a short-circuit scenario

Table 6 shows the SOA parameter values and the operating points for both standard MOSFET and Linear FET at all the test conditions.

Table 6 SOA analysis for parallel FETs during a short-circuit scenario

Part	Current (A)	MOSFET	I_{PEAK} (A)	P_{max} (kW)	E_{tot} (J)	t_{pul} (µs)	I_{Dmax} (A)	V_{DSmax} (V)	SOA operating point
Standard MOSFET	240	Q_1	133.3	1.53	0.0792	52	68.5	22.3	Inside
		Q_2	100	1.35	0.0705	52	52.1	25.9	Inside
	280	Q_1	154.8	1.85	0.0948	51	85	21.8	Inside
		Q_2	120.3	1.66	0.0848	51	66.3	25	Inside
	340	Q_1	185.9	2.38	0.118	50	102.8	23.2	Inside
		Q_2	150.2	2.17	0.107	49	88.7	24.5	Inside
	400	Q_1	214.6	2.91	0.143	49	127.1	22.9	Inside
		Q_2	177.6	2.69	0.133	49	107.3	25.1	Inside
	460	Q_1	247.9	3.57	0.17	48	139.3	25.6	Inside
		Q_2	207.6	3.33	0.159	48	117.1	28.4	Inside
Linear FET	240	Q_1	112	1.73	0.0282	16	76.6	22.6	Inside
		Q_2	118.6	1.85	0.0325	18	81.2	22.8	Inside
	280	Q_1	132.8	2.19	0.0353	16	80.1	27.3	Inside
		Q_2	141.3	2.37	00397	17	86.7	27.3	Inside
	340	Q_1	170.7	2.93	0.0391	13	105.2	27.8	Inside
		Q_2	161.2	3.14	0.0435	14	112.5	27.9	Inside
	400	Q_1	191.3	3.70	0.0491	13	123.2	30	Inside
		Q_2	201.3	3.93	0.0542	14	130.6	30.1	Inside
	460	Q_1	216	4.75	0.0657	14	144.5	32.9	Inside
		Q_2	230.8	5.00	0.0718	14	152.6	32.8	Inside

Table 6 shows that parallelization of Linear FET has better SOA performance for both Q_1 and Q_2 as compared to standard MOSFET. Linear FETs also turn off much faster than standard MOSFETs and spend 70 percent less time in linear mode compared to standard MOSFETs at all current levels without avalanching. The similar current sharing exhibited by Linear FET is further compared below to understand why Linear FET is better than standard MOSFET.

Figure 31 compares the current sharing between Linear FET and standard MOSFET during an inrush current scenario with 5 × 470 µF capacitor load. **Figure 32** compares the current sharing between Linear FET and standard MOSFET during a short-circuit scenario at 460 A total short-circuit current.

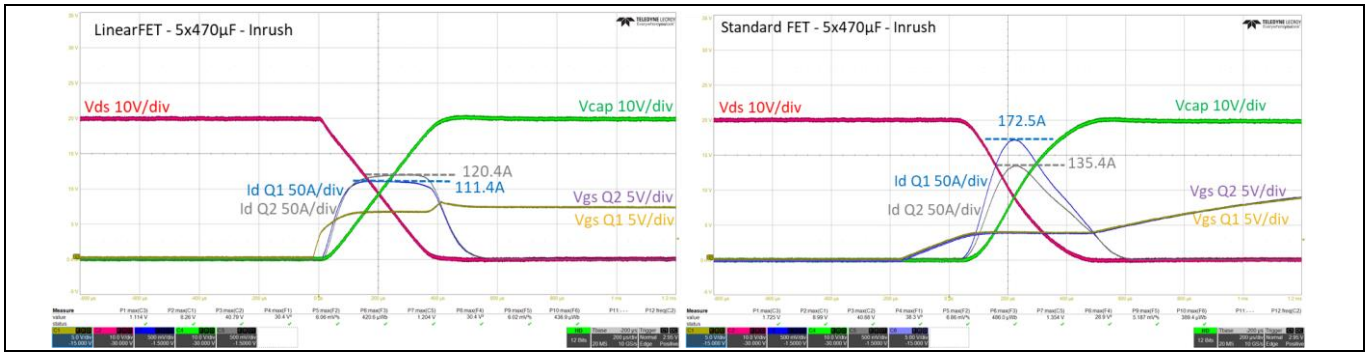

Figure 31 Current-sharing comparison for Linear FET and standard MOSFET during inrush

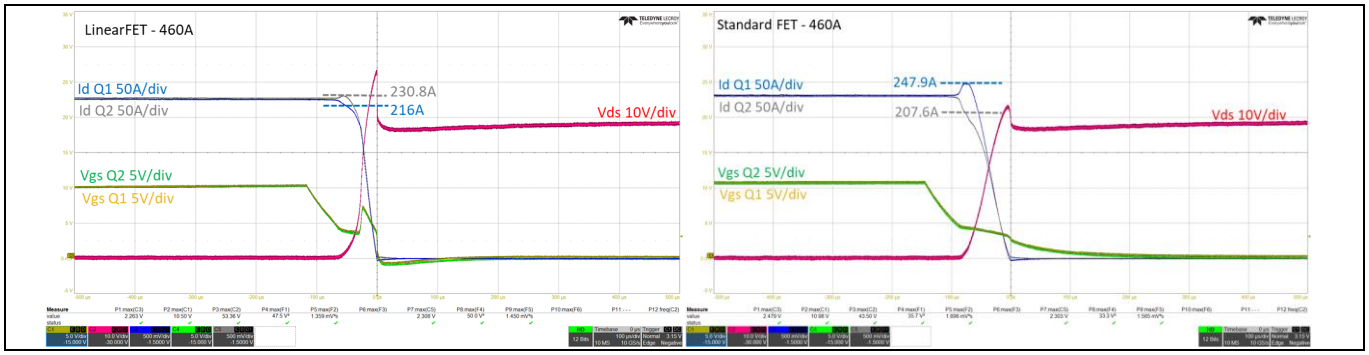

Figure 32 Current-sharing comparison for Linear FET and standard MOSFET during short-circuit

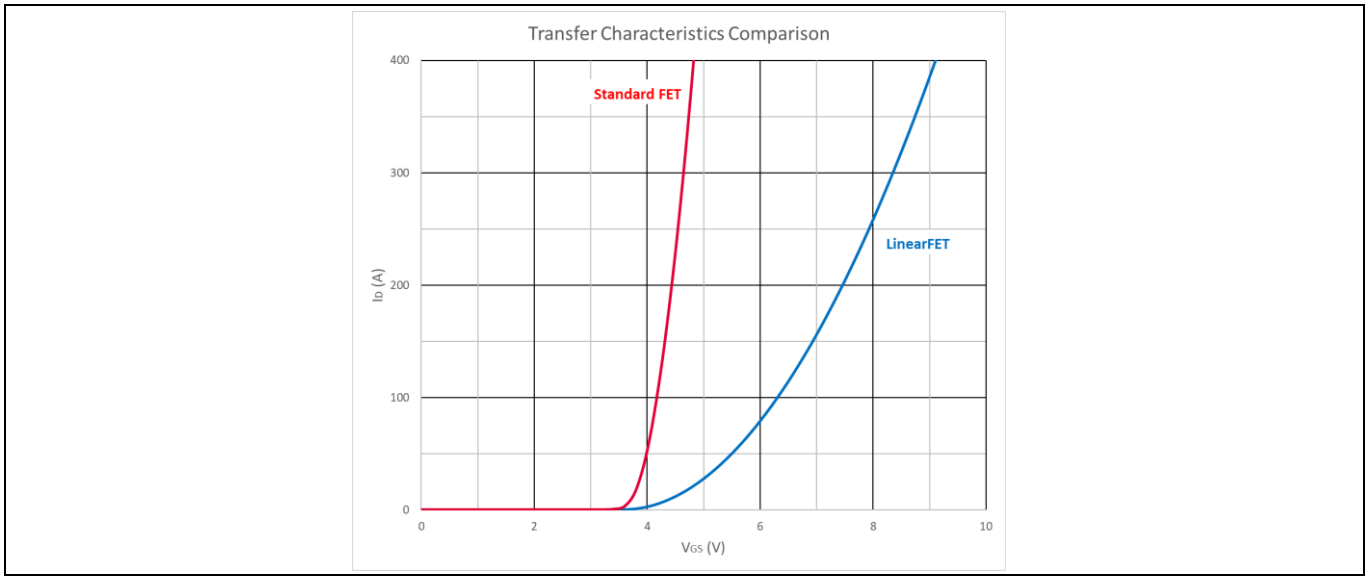

Figure 33 Transfer characteristics comparison

The slope of the curve in **Figure 33** is the transconductance (g_{fs}) of the MOSFET. Higher g_{fs} can cause significant differences in current sharing between parallel FETs, since there would be a significant change in drain current I_D for a small difference in V_{GS}. It can be seen that for standard MOSFET the g_{fs} is very high, which would result in unequal current sharing between parallel FETs if there is slight difference in V_{GS}. Whereas, since Linear FET has much smaller g_{fs}, it helps in equal current sharing between parallel FETs.

Thus, it can be concluded that Linear FET has better performance for both inrush current limiting and short-circuit protection than standard MOSFET. It can also be parallelized more easily, which will help scale the system for higher current-carrying capabilities. This makes Linear FET a much better choice as a 7th MOSFET for battery protection.

7 Gate driver/R_G-C_{GD} selection guidance

To optimize the external R_{Gon}, C_{GD} and R_{Goff} values for turn-on and turn-off, respectively, detailed calculations are required (see **Figure 34**). All of the information needed here is either available from the circuit design, e.g., total capacitive load to be charged, etc., or mentioned in the product datasheet, such as the maximum current capability in linear mode, available in the transfer characteristics and/or SOA diagram in the datasheet. Calculations are split into three sections. Section I focuses on the total gate current requirements based on the capacitive load to be charged under controlled current. Section II focuses on external R_{Gon}, C_{GD} and R_{Goff} optimization to achieve the controlled load current turn on and turn off. This ensures the maximum product specifications mentioned in the datasheet are not violated. Section III describes the external R_{Gon}, C_{GD} and R_{Goff} boundary conditions. All three sections are described with illustration of the optimization for IPT008N06NM5LF, which is a 60 V Linear FET in a TOLL package with 0.8 mΩ $R_{DS(on)}$ 10 V max.

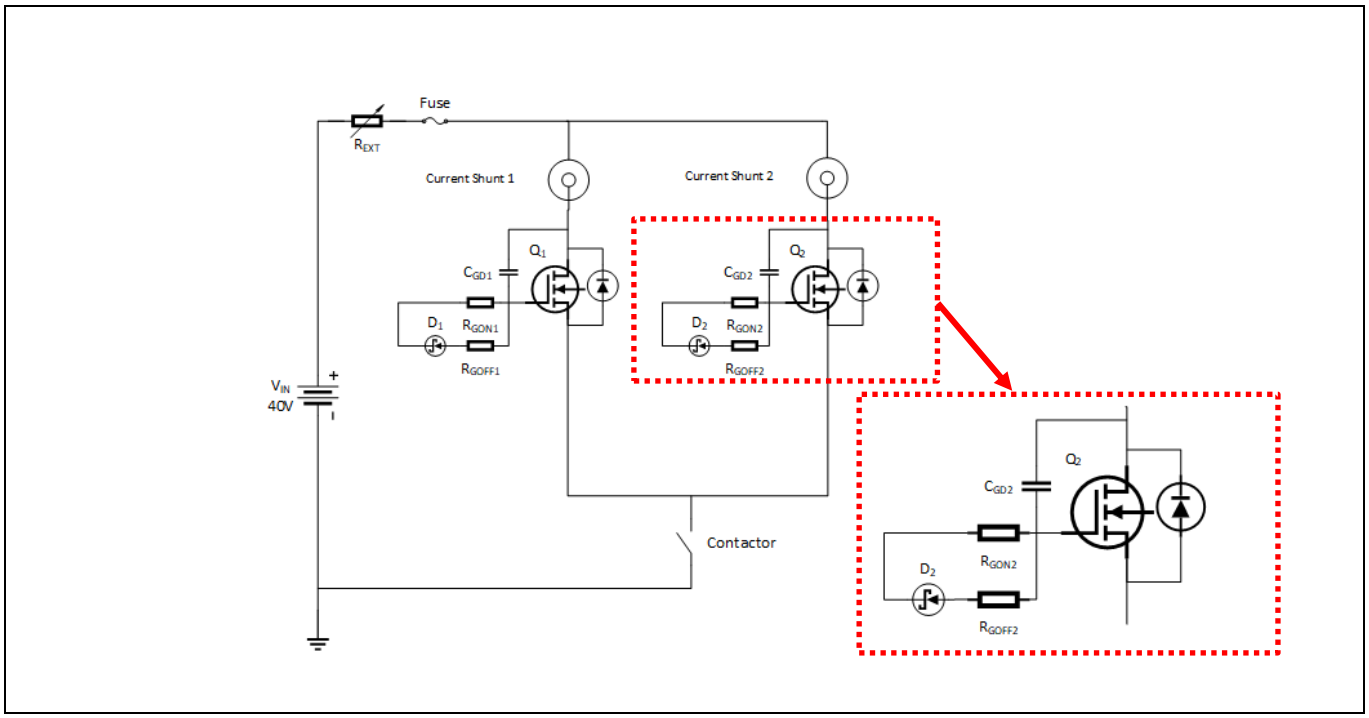

Figure 34 External R_{Gon}, R_{Goff} and CGD along with the antiparallel Schottky diode in the R_{Goff} loop

Section I: In this section we calculate the maximum gate drive current required in order to charge the capacitive load when Linear FET is used as the 7th MOSFET for inrush protection or as a discharge MOSFET in the BMS socket.

A. Calculate maximum drain current, **I_D** (in Amperes) for the product from the transfer characteristics (Diagram 7 in the DS) at gate plateau voltage (V_{GS} plateau). V_{GS} plateau voltage is provided in **Table 7** $V_{PLATEAU}$. For IPT008 this value is 8.7 V. Hence the maximum drain current I_D at this gate voltage at 150°C is 259 A as per the DS transfer curve.

B. Total capacitance values or load, **C_{LOAD}** in Farads. In this example we are assuming three 470 µF capacitors in parallel, which is 1.41 mF total capacitance to be charged.

C. Maximum battery voltage. In this example we are using a lithium-ion battery with 4.2 V maximum per cell. With 10 cells in series, maximum battery voltage, **V_{IN}** is 42 V.

D. Based on the formula for a parallel plate capacitor Q = C*V, where Q is the charge on the capacitor in Coulombs, C is the capacitance value in Farads and V is the voltage in Volts, total charge can be calculated. In our example **Q_{LOAD}** is 59.2 mC.

E. Time required to charge this load capacitance knowing the total drain current available, $T = Q/I_D$ from (I.A and D), we get $\mathbf{T_{TOTAL}}$ 229 µs.

F. For the MOSFET IPT008, total switching charge is $\mathbf{Q_{SW}} = Q_{GS} + Q_{GD}$ = 161 nC from **Table 7**. In theory switching charge is $Q_{GD} + Q_{GS2}$; however, in this case since Q_{GS} is small – only 6 nC – we approximated it to be $Q_{GD} + Q_{GS}$. For most Linear FET products, it is sufficient to use Q_{GS} instead of Q_{GS2}.

G. Based on I = Q/T where I is the current in Amperes, Q is the charge in Coulombs and T is time in seconds, we get maximum gate drive current, $\mathbf{I_{ON\ MAX}}$ (from E and F) of 704 µA.

Section II: This section will focus on the selection of external R_{Gon}, C_{GD} and R_{Goff} for both turn-on and turn-off. To control the load current during turn-on and to ensure safe turn-off during discharge or short on the inverter side, a combination of external R_G and C_{GD} optimization is required. During turn-on, we focus on the load capacity to be charged and optimize the R_{Gon} to achieve controlled drain current charging. During turn-off focus is on the maximum dV_{DS}/dT and peak V_{DS} voltage such that the MOSFET will not go into avalanche, while ensuring faster turn-off to minimize power dissipation in linear mode.

A. Maximum V_{DS} peak is kept below 80 percent of rated breakdown voltage. For the example given, as we are using a 60 V N-channel MOSFET, $\mathbf{V_{DSmax}}$ is ~48 V.

B. Maximum ($\mathbf{dV_{DS}/dT_{max}}$) is 0.7 V/µs. This value is assumed based on the gate charge, internal gate resistance, charge ratio (Q_{GD}/Q_{GS}) and capacitance ratio (C_{ISS}/C_{RSS} at 0 V_{DS}). The objective in this case is to keep the dV_{DS}/dT sufficiently low, so that the accidental induced turn-on due to $C*dV_{DS}/dT$ during MOSFET turn-off is avoided.

C. Maximum gate drive voltage, $\mathbf{V_{DRIVE}}$ is 15 V. Most of the OptiMOS™ technologies have +/- 20 V_{GS} absolute maximum ratings.

D. Gate plateau voltage, $\mathbf{V_{PLATEAU}}$ of 8.7 V as already mentioned in section I.A.

E. MOSFET internal gate resistance is required. In the current examples, as per the DS, $\mathbf{R_{GINT}}$ is 70 Ω.

F. Internal resistance of the gate driver, based on the choice of gate driver used. In our case we used IR4427S with a gate driver resistance of ~8.7 Ω. In many gate drivers, sink and source resistances are different. For simplicity, please use the minimum gate drive resistance, $\mathbf{R_{GATEDRIVER}}$, which in most cases is for the sink path.

G. MOSFET input capacitance or $\mathbf{C_{ISS}}$ at gate drive voltage (Step 3). For IPT008 this value is 0.8 nF at a gate drive voltage of 15 V.

H. Maximum gate drive current for turn-off, $\mathbf{I_{OFF\ MAX}}$ can be calculated from Step I.F, II.A and II.B

$$I_{OFF\ MAX} = \frac{(Q_{GS} + Q_{GD}) * \left(\frac{dV_{DS}}{dT}\right) max}{V_{DSMAX}}$$

In the current example based on the above equation, $I_{OFF\ MAX}$ is 2.35 mA.

I. To calculate the turn-on gate drive current, time-constant of the gate loop, $\boldsymbol{\tau_{gate\ loop}}$ is calculated with the following equation (Steps I.G II.C, II.D and II.G)

$$\tau_{gate\ loop} = \frac{(V_{DRIVE} - V_{PLATEAU}) * 1.3 * C_{ISS}}{I_{ON\ MAX}}$$

In this example $\tau_{gate\ loop}$ is 9.31 µs. A factor of 1.3*C_{ISS} is used to account for the datasheet typical to a maximum of 30 percent.

J. The maximum number of time-constants required to fully charge a capacitor is 5. From II.I we get time to charge, **T_{CHARGE}** of 46.53 µs.

Section III: In section II we calculated the turn-off time and also the time-constant for the turn-on time. In this section we will define the boundary conditions for the selection of R_{Gon}, C_{GD} and R_{Goff} values.

A. Maximum external on-resistance, **$R_{Gon\ MAX}$** can be calculated as follows:

$$R_{Gon\ MAX} = \frac{T_{CHARGE}}{C_{ISS}}$$

T_{CHARGE} is derived in the previous section II.J and C_{ISS} is noted in II.G. In the current example the value of $R_{Gon\ MAX}$ is 58.16 kΩ.

B. **$R_{Goff\ EQUIVALENT}$** will be calculated next. As shown and discussed previously at the start of this section, R_{Goff} has a Schottky diode in series. When the gate drive voltage is pulled to 0 V during MOSFET turn-off, the two resistors R_{Gon} and R_{Goff} are in parallel, as the Schottky diode is forward-biased. Hence, we calculate the equivalent R_{Goff} value, $R_{Goff\ EQUIVALENT}$.

$$R_{Goff\ EQUIVALENT} = \frac{V_{PLATEAU}}{I_{OFF\ MAX}} - R_G - R_{GATEDRIVER}$$

Values of $V_{PLATEAU}$, $I_{OFF\ MAX}$, R_G and $R_{GATEDRIVER}$ have already been discussed in sections I.A, II.H, II.E and II.F. For this current example the calculated value of $R_{Goff\ EQUIVALENT}$ is 3.63 kΩ.

C. Minimum external off-resistance, **$R_{Goff\ MIN}$**, is calculated as follows. $R_{Gon\ MAX}$ and $R_{Goff\ EQUIVALENT}$ were already calculated in sections III.A and B.

$$R_{Goff\ MIN} = \frac{R_{Gon\ MAX} * R_{Goff\ EQUIVALENT}}{R_{Gon\ MAX} - R_{Goff\ EQUIVALENT}}$$

For the current example, $R_{Goff\ MIN}$ is 3.8 kΩ.

D. To simplify the design and considering that the external C_{GD} will be contributing to the C_{GD}/C_{GS} ratio (important for the $C*dV_{DS}/dT$ immunity), external C_{GD} is chosen equal to the input capacitance C_{ISS} of the MOSFET. For the current calculations, **$C_{GD\ MIN}$** is 0.8 nF as discussed in section II.G.

E. We can now calculate the minimum switch-on time, **T_{ON}** as $R_{Gon\ MAX}$ multiplied by $C_{GD\ TOTAL}$. $R_{Gon\ MAX}$ was already discussed in III.A. $C_{GD\ TOTAL}$ will be a parallel combination of C_{GD} internal and C_{GD} external. Typically, C_{GD} internal is much smaller than C_{GD} external, hence we only considered C_{GD} external, calculated in section III.D. For the current example this value is 46.53 µs.

F. Minimum turn-off time, **T_{OFF}**, is calculated using the formula $R_{Goff\ EQUIVALENT}$ multiplied by C_{GD} external. $R_{Goff\ EQUIVALENT}$ is calculated in section III.B and C_{GD} is discussed in section III.D. For the current example this results in $T_{OFF\ MIN}$ of 2.9 µs.

We have used these calculations to verify the performance of various 60 to 200 V Linear FETs in both inrush and BMS (charge/discharge MOSFET) sockets. The results of those have already been shown in previous sections with 60 V TOLL FETs. The external R_{GON}, R_{GOFF} and C_{GD} are required for each of the MOSFETs when multiple MOSFETs are connected in parallel. The turn-on time and turn-off time are explicitly mentioned as minimum T_{ON} and T_{OFF} in sections III.E and F. If exact component values for R_{GON} and R_{GOFF} are not available, it is suggested that the designer use the closest component values (±10 percent of recommended values). For C_{GD}, the designer should choose greater than or equal to the C_{ISS} value of the MOSFET. These components (R_{GON}, R_{GOFF} and C_{GD}) should be chosen to satisfy the T_{ON} and T_{OFF} times shown in III.E and F. A simple Excel file can be created for

sections I to III to calculate the required component values as shown in **Table 7** for the example covered in this section.

Table 7 R_G-C_{GD} selection guidance

Section	Point	Parameters	Value	Units
I	A	I_D	259	A
	B	C_{LOAD}	1.41	mF
	C	V_{IN}	42	V
	D	Q_{LOAD}	59.2	mC
	E	T_{TOTAL}	229	µs
	F	Q_{SW}	161	nC
	G	$I_{ON\ MAX}$	704	µA
II	A	$V_{DS\ MAX}$	48	V
	B	dV_{DS}/dT max.	0.7	V/µs
	C	V_{DRIVE}	15	V
	D	$V_{PLATEAU}$	8.7	V
	E	R_{GINT}	70	Ω
	F	$R_{GATEDRIVER}$	8.7	Ω
	G	C_{ISS}	0.8	nF
	H	$I_{OFF\ MAX}$	2.35	mA
	I	$\tau_{gate\ loop}$	9.31	µs
	J	T_{CHARGE}	46.53	µs
III	A	$R_{GON\ MAX}$	58.16	kΩ
	B	$R_{GOFF\ EQUIVALENT}$	3.63	kΩ
	C	$R_{GOFF\ MIN}$	3.8	kΩ
	D	$C_{GD\ MIN}$	0.8	nF
	E	T_{ON}	46.53	µs
	F	T_{OFF}	2.9	µs

8 Conclusion

In this application note we have discussed the advantages of OptiMOS™ Linear FET versus a standard MOSFET used as an inrush and short-circuit protection switch and/or a charge/discharge MOSFET in a battery management system. The experimental results for both turn on and turn off have been shown, with varying load conditions for a single MOSFET and two MOSFETs in parallel. Corresponding power and energy calculations based on waveforms have been demonstrated, along with mapping these onto the SOA diagram. This approach ensures MOSFET operation within the SOA limits specified on the datasheet. Choosing the right R_{Gon}, R_{Goff} and C_{GD} values for the controlled turn on and turn off is critical, and has been fully described with the corresponding calculations with boundary conditions.

9 References

[1] Infineon Technologies AG: Linear Mode Operation and Safe Operating Diagram of Power-MOSFETs, Application Note (V 1.1); 2017-05; **available online**.

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