# Design guidelines for OptiMOS™ 5 in high-power low-voltage motor drives

## How to design using OptiMOS™ 5 MOSFETs in motor drive applications

## About this document

### Scope and purpose

This document explains the differences between OptiMOS™ 3 and OptiMOS™ 5 technology, and how to successfully interchange them. Datasheet parameters are a focus of this document, as well as how to handle paralleled MOSFETs to ensure better current sharing between them. The gate driver circuit is also covered in this document, which explains how to modify it to accommodate the differences between these two technologies.

### Intended audience

This document is intended for design engineers who are using the OptiMOS™ 5 in a new design or replacing the OptiMOS™ 3 with the OptiMOS™ 5 generation of existing designs in motor drive applications such as light electric vehicles (LEVs), material handling equipment such as forklifts, and similar applications.

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# 1 Introduction

In today's fast-growing motor drive market, it is important to become familiar with the new technology in order to optimize the cost and performance of products such as motor inverters. In particular, Infineon's OptiMOS™ family of MOSFETs are a suitable choice for low-voltage motor drives. In this document we will cover high-power low-voltage motor drive (HP LVMD) applications that commonly use MOSFETs in the voltage range of 60 V to 250 V.

Specifically, we will consider Infineon's previous generation of OptiMOS™ 3 MOSFETs and compare them with the OptiMOS™ 5 generation. A common mistake is to assume that two MOSFETs will behave the same way when interchanging them, even if they are from the same manufacturer. Therefore, it is important to understand some key differences between these two generations.

## 1.1 Key differences between OptiMOS™ 3 and OptiMOS™ 5 generations

The OptiMOS™ 5 is currently available in voltage classes up to 150 V, and OptiMOS™ 3 up to 200 V.

Table 1 shows key parameters for HP LVMDs, and in this example, we will take a look at the 150 V MOSFET in both technologies. The OptiMOS™ 3 best-in-class product is 7.2 mΩ and for OptiMOS™ 5 it is 4.4 mΩ, but here we will compare the closest $R_{DS(on)}$ value available in OptiMOS™ 5, which is 7.3 mΩ.

**Table 1 Overview of the datasheet – typical values**

| Parameter | OptiMOS™ 3 | OptiMOS™ 5 |
|---|---|---|
| | IPB072N15N3 G | IPB073N15N5 |
| Test condition | At $I_D$ = 100 A | At $I_D$ = 57 A |
| Drain current $I_D$ | 100 A | 114 A |
| Drain-source on-state resistance $R_{DS(on),max}$ | 7.2 mΩ | 7.3 mΩ |
| Internal gate resistance $R_g$ | 2.3 Ω | 1.1 Ω |
| Transconductance $g_{fs}$ | 130 S | 91 S |
| Input capacitance $C_{iss}$ | 5470 pF | 3600 pF |
| Output capacitance $C_{oss}$ | 638 pF | 900 pF |
| Reverse transfer capacitance $C_{rss}$ | 10 pF | 21 pF |
| Output charge $Q_{oss}$ | 179 nC | 136 nC |
| Gate-to-source charge $Q_{gs}$ | 30 nC | 21 nC |
| Gate-to-drain charge $Q_{gd}$ | 11 nC | 10 nC |
| Switching charge $Q_{sw}$ | 25 nC | 17 nC |
| Gate charge total $Q_g$ | 70 nC | 49 nC |
| Gate threshold voltage $V_{GS(th)}$ | 3 V (min. 2 V, max. 4 V) | 3.8 V (min. 3.0 V, max. 4.6 V) |
| Diode reverse recovery time $t_{rr}$ | 146 ns | 69 ns |
| Diode reverse recovery charge $Q_{rr}$ | 478 nC | 96 nC |
| Thermal resistance, junction-case $R_{th,J-C}$ | 0.5 K/W | 0.7 K/W |

As shown in this table, none of the parameters have the same values. The following sections describe how they affect the performance in an application.

# 2 Test conditions

When comparing two MOSFETs it is important to pay attention to test conditions, as they might be different. In this case the test condition for OptiMOS™ 3 is 100 A and for OptiMOS™ 5 it is 57 A. This is purely a test condition and is no indication of the device performance. If this value is different, some datasheet parameters may not be comparable, such as $Q_{rr}$, due to fact that this parameter value changes with the test condition.

| | | | | | | |
|---|---|---|---|---|---|---|
| Reverse recovery time | $t_{rr}$ | $V_R$=75 V, $I_F$=$I_S$, $di_F/dt$ =100 A/µs | - | 146 | - | ns |
| Reverse recovery charge | $Q_{rr}$ | | - | 478 | - | nC |
| $Q_{rr@100A} \neq Q_{rr@57A}$ | | | | | | |

**Figure 1 Datasheet test conditions**

More details about $Q_{rr}$ are given in section 10.

# 3 Continuous drain current $I_D$ rating

The $I_D$ current rating states how much current a MOSFET can carry under defined test conditions. The $I_D$ of the MOSFET can be based on different boundary conditions and as a result the $I_D$ rating will be different for the same product.

Infineon's previous method for $I_D$ rating included an assumption that the PCB temperature is at a constant 85°C. As a result, Infineon products were perceived as lower-current-rated products, since the datasheets of some other manufacturers assumed 25°C. For this reason, Infineon took another approach and made an assumption that the PCB temperature equals the case temperature, i.e. it varies from 25°C to 175°C. This is a much more realistic scenario, and at the same time it allows a better comparison with competitor parts.

For more details please refer to the Infineon application note "**A new approach to data sheet maximum drain current ID rating of low voltage MOSFETs".**

# 4 Drain-source on-state resistance $R_{DS(on)}$

The drain-source on-state resistance, $R_{DS(on)}$, is always evaluated at 25°C but not necessarily at the same current. Fortunately, $I_D$ test current influence on the $R_{DS(on)}$ value is minimal. More importantly, the temperature coefficient can be different. This means that for two products with different temperature coefficients the resultant $R_{DS(on)}$ will be different at higher temperatures. In this example with IPB072N15N3, IPB073N15N5 the temperature coefficient difference is minimal. The formula that gives the relationship between $R_{DS(on)}$ and a temperature coefficient α is:

$$R_{n-channel} = R_{25}\left(1+\frac{\alpha}{100}\right)^{T-25}$$

- $R_{25}$ – $R_{DS(on)}$ value at 25°C
- T – silicondie new temperature

**Figure 2** shows the values of $R_{DS(on)}$ at temperatures of -50°C to 175°C.

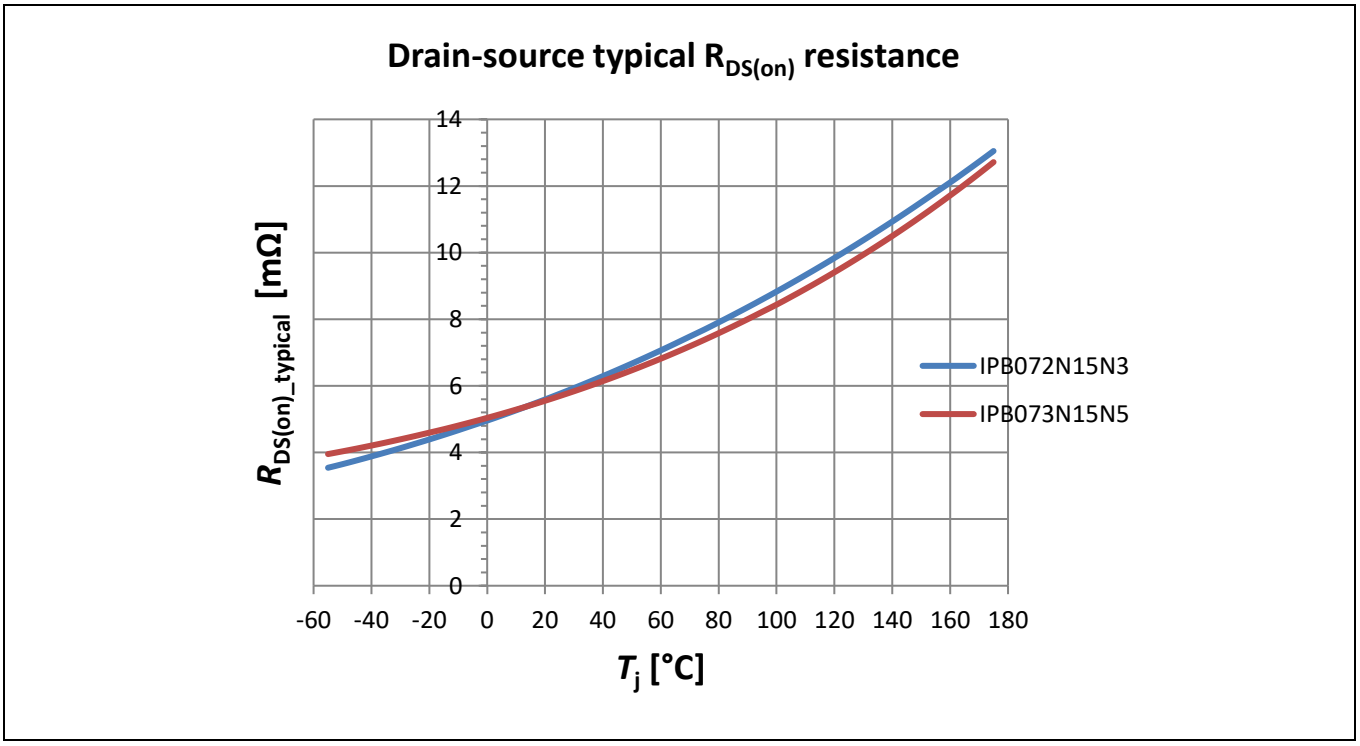



**Figure 2 Drain-source $R_{DS(on)}$ resistance – temperature dependency**

# 5 Internal gate resistance $R_g$ and gate drive circuit

Depending on the technology and internal structure of the MOSFET, the internal gate resistance $R_g$ can be different for MOSFETs with the same $R_{DS(on)}$. In our example IPB072N15N3 has a value of 2.3 Ω and IPB073N15N5 a value of 1.1 Ω.

In some cases where a slower slew rate is required, it is common practice to connect an external $C_{gs}$ capacitor, but in this case the designer needs to make sure this additional capacitor doesn't cause any oscillations.

As illustrated in **Figure 3**, an added external capacitor $C_{gs\_ext}$ builds a resonant circuit with internal and external parasitic components.

The $R_g$ in this loop acts as a damping resistor, and if the value is too low, the circuit may become unstable and start oscillating.

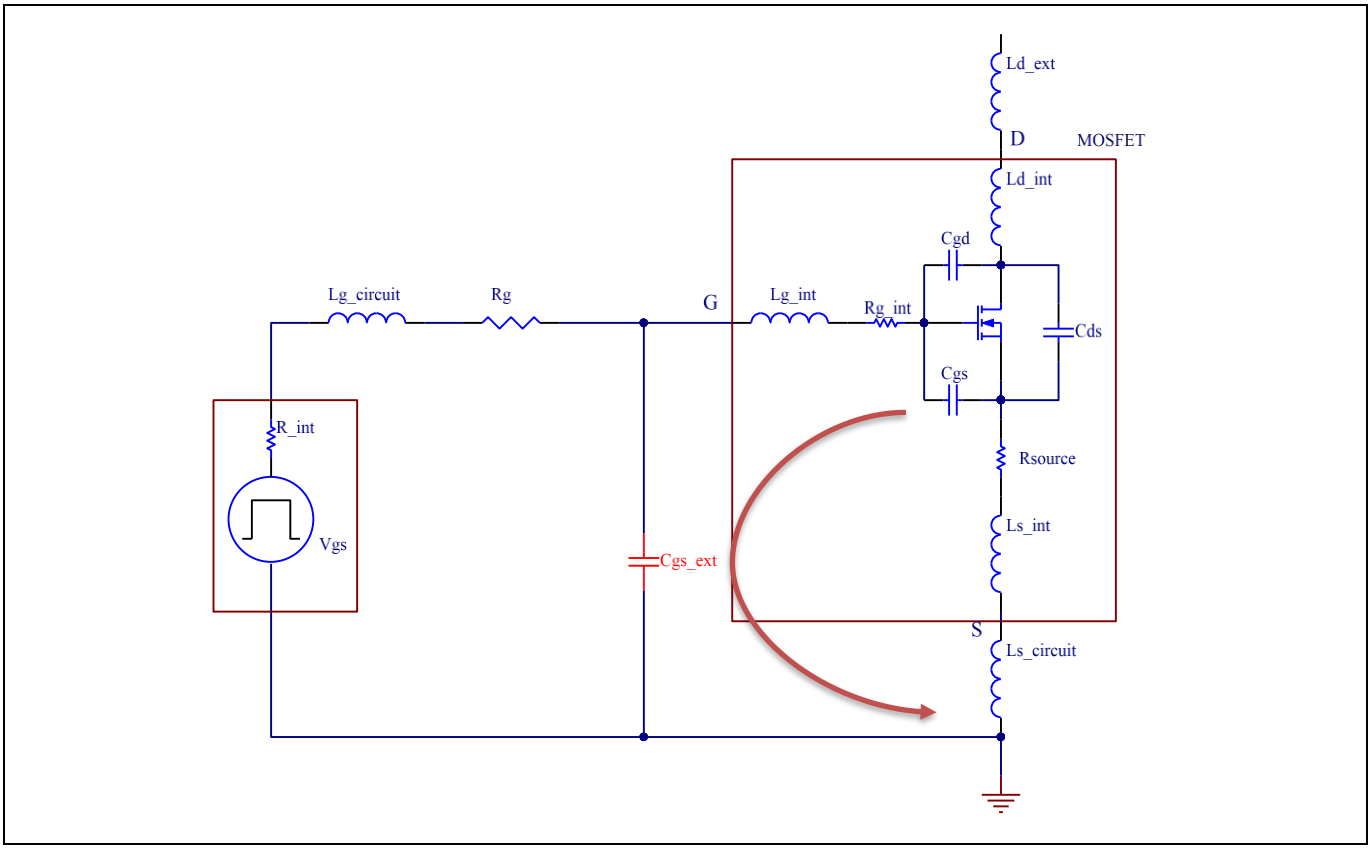



**Figure 3 Parasitic elements of a MOSFET (red box) and the external circuit**

**Figure 4** shows drain-source and gate-source oscillations when $C_{gs\_ext}$ is connected at the gate source of a MOSFET, and **Figure 5** shows a solution to this problem by simply introducing an external resistor less than 10 Ω between the gate and the external capacitor.

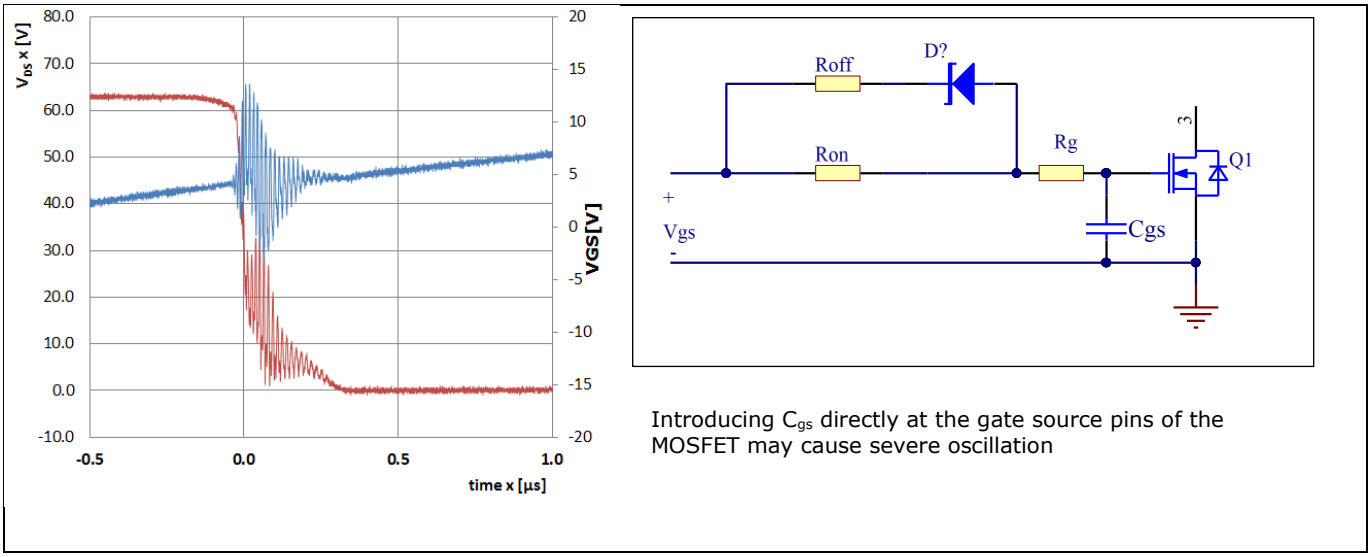



**Figure 4** $V_{DS}$ (red) and $V_{GS}$ (blue) waveforms with $C_{gs}$ connected directly at gate source

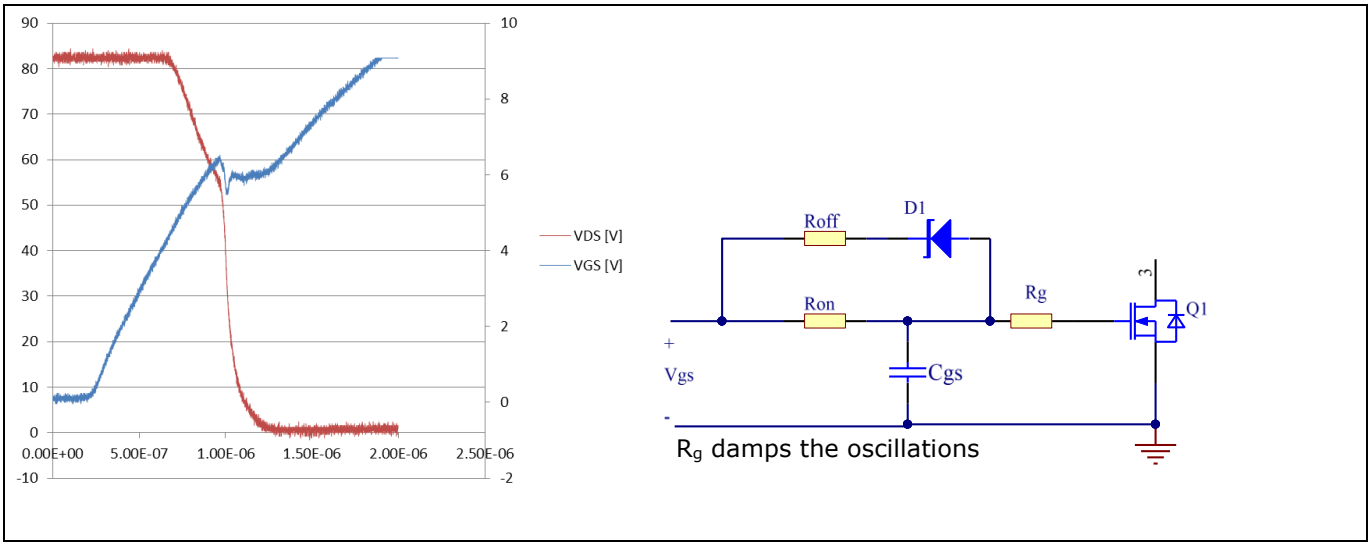



**Figure 5** $V_{DS}$ (red) and $V_{GS}$ (blue) waveforms with external $R_g$ between gate and capacitor

So far, we've looked at the case of 150 V technology. Let's take a quick look at 80 V technology and observe the differences between OptiMOS™ 3 and OptiMOS™ 5.

In a simple half-bridge topology, shown in **Figure 6**, in which the load current is created by turning on the high-side MOSFET, we can observe some differences in output voltage and $I_D$ – drain current of Q2.

In **Figure 7** we aim to obtain the same di/dt value of $I_D$ and in this example we are using $R_g$ = 40 Ω for OptiMOS™ 3 IPB019N08N3 and for OptiMOS™ 5 IPB019N08N5 we need to increase the gate resistor value to $R_g$ = 64 Ω. In addition, OptiMOS™ 5 shows a lower $V_{DS}$ overshoot, which prevents the avalanche condition and a higher dv/dt, which reduces switching loss. The main contributors are lower $Q_{rr}$ and $I_{rrm}$ values (refer to section 10 for more information about $Q_{rr}$ and $I_{rrm}$).

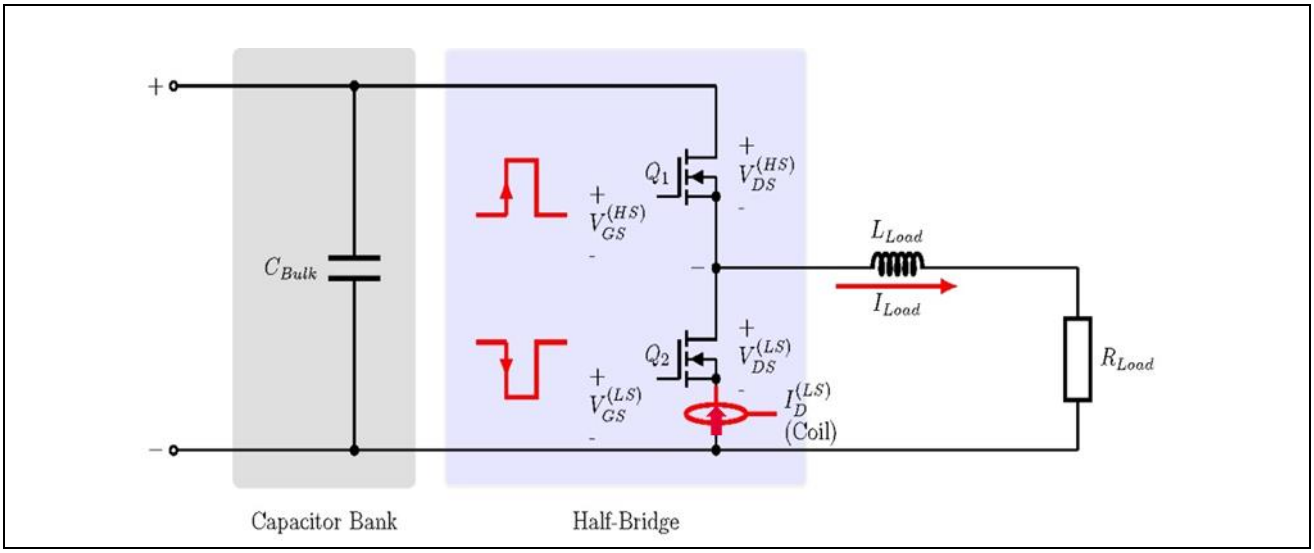



**Figure 6 Simplified half-bridge test circuit**

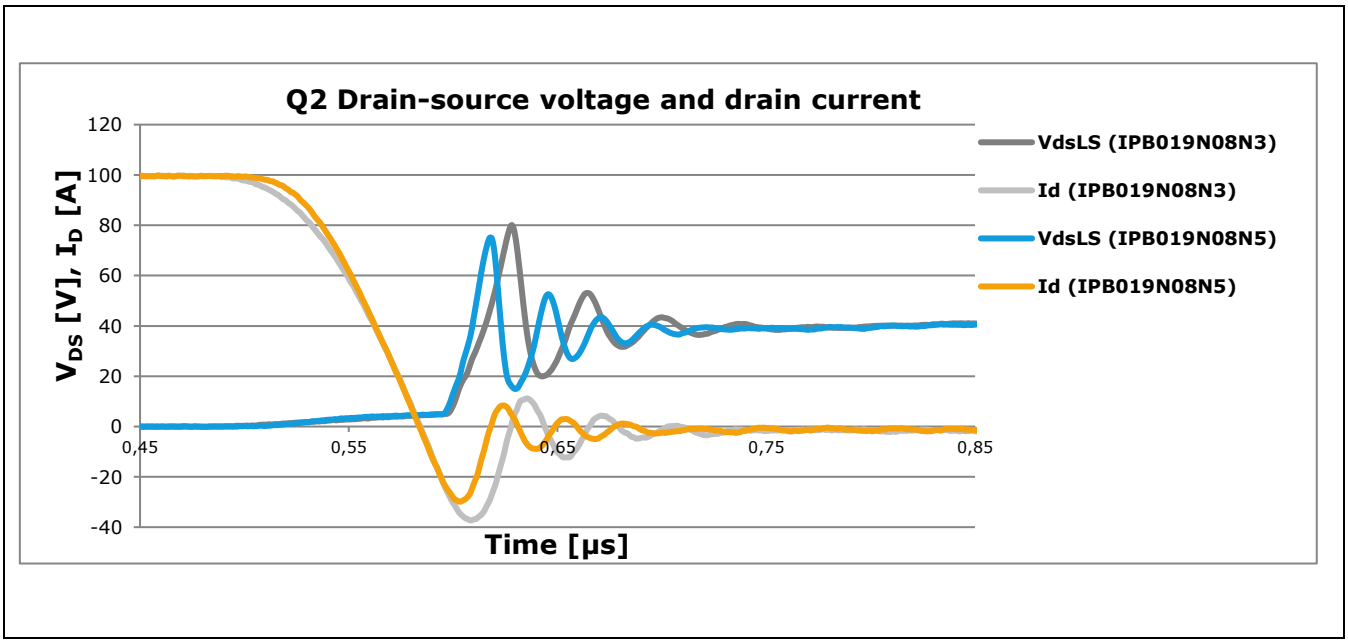



**Figure 7 $V_{DS}$ of Q2 – output phase voltage and $I_D$ of Q2 – MOSFET current**

# 6 Transconductance $g_{fs}$

The transconductance is a parameter that indicates the change of $I_D$ current due to change of $V_{GS}$ voltage. It can be expressed with the formula:

$$gfs = \frac{\Delta Id}{\Delta Vgs}$$

When comparing 150 V classes of OptiMOS™ 3 with OptiMOS™ 5, we see that IPB073N15N5 has a value of 91 S and IPB072N15N3 a value of 130S. However, it should be noted that IPB073N15N5 was tested with $I_D$ = 57 A and IPB072N15N3 with $I_D$ = 100 A. In order to make a fair comparison we have to use datasheet graphs to obtain the value of $g_{fs}$ of IPB073N15N5 at $I_D$ =100 A. This value is 118 A. **Figure 8** shows both $g_{fs}$ curves.

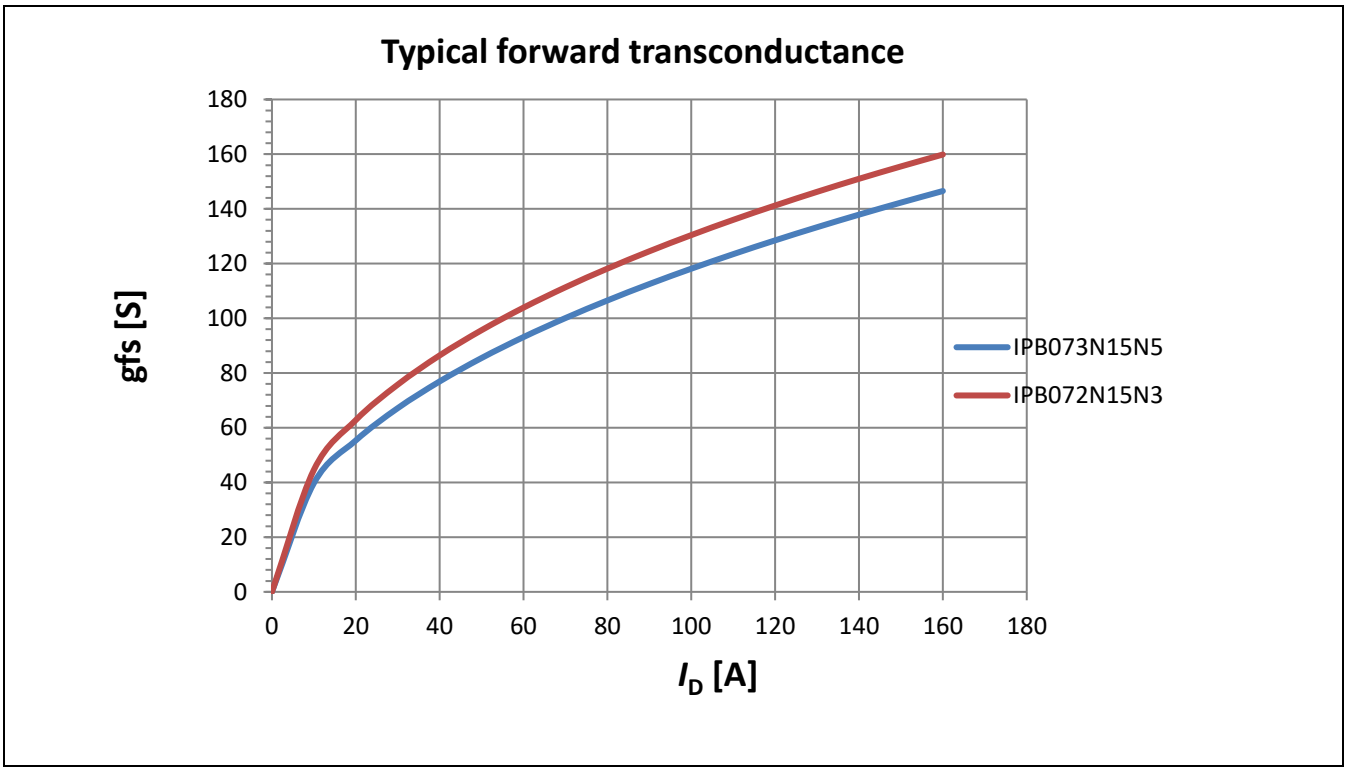



**Figure 8 Typical forward transconductance**

The practical implication of $g_{fs}$ would contribute to current sharing among paralleled MOSFETs.

In this sense a higher $g_{fs}$ value demands a smaller $V_{th}$ spread in order to have the same current sharing as a MOSFET with lower $g_{fs}$.

Fortunately the effect of this parameter on current sharing is not very strong. In **Figure 9** the extreme values are assumed to show current imbalance due to different $g_{fs}$.

This graph was obtained by simulating four paralleled 80 V MOSFETs, IPB019N08N5, in which one MOSFET had a minimum $V_{GS(th)}$ and the remaining three MOSFETs had a maximum $V_{GS(th)}$ value. With this configuration the $g_{fs}$ was varied from 120 S to 250S. We can conclude that the effect of $V_{GS(th)}$ mis-match has a much larger influence on current sharing than mis-match in $g_{fs}$.

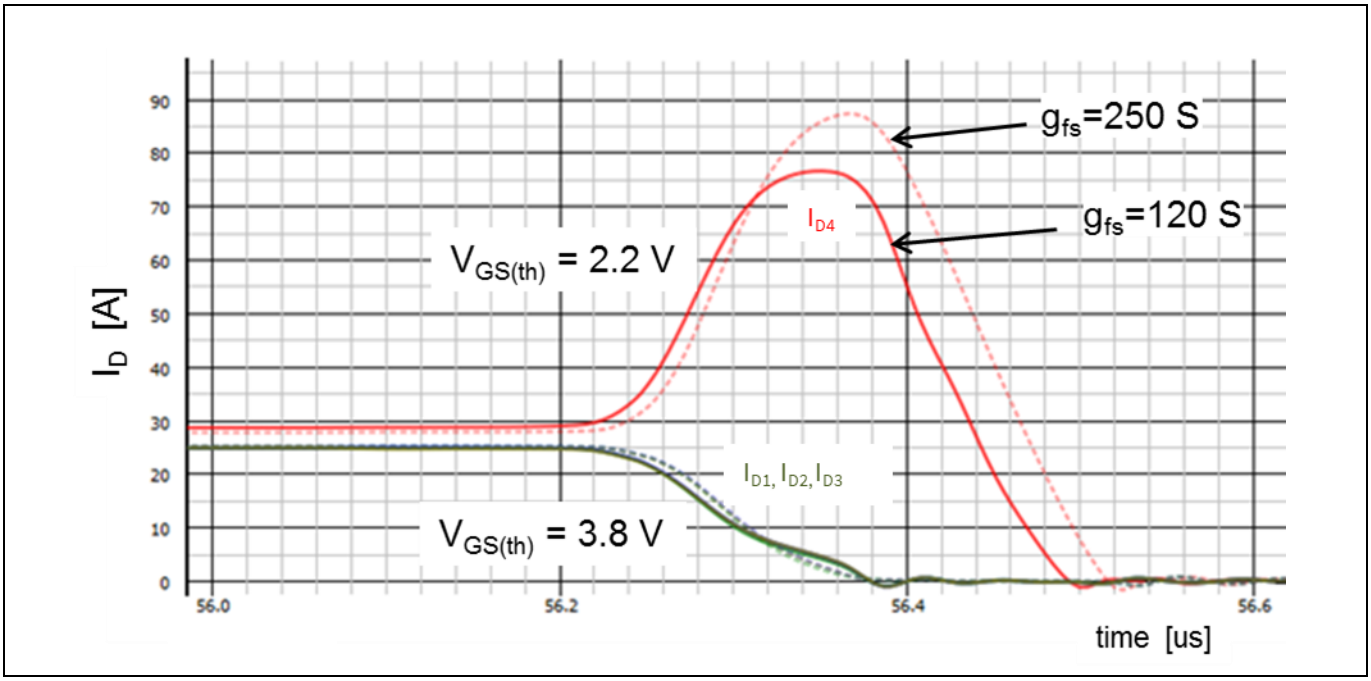



**Figure 9 Influence of $V_{GS(th)}$ and $g_{fs}$ on current sharing**

# 7 Input capacitance $C_{iss}$, reverse recovery capacitance $C_{rss}$ and output capacitance $C_{oss}$

The input capacitance $C_{iss} = C_{gs} + C_{gd}$ contributes to gate driver losses, as it needs to be charged and discharged at high switching rates. The gate source capacitance $C_{gs}$ affects the rate of change of drain current di/dt. With a lower $C_{gs}$ the MOSFET will have a higher di/dt than a MOSFET with higher $C_{gs}$ due to faster charging of $C_{gs}$, assuming all other parameters are the same. A higher value of gate resistor can be used to reduce di/dt.

In fact we should use $Q_{gs}$ since this parameter is a true reflection of how much charge should be provided to create a change in $I_D$ current.

In our example IPB072N15N3 with $C_{iss}$ = 5470 pF ($Q_{gs}$ = 30 nC) and IPB073N15N5 with $C_{iss}$ = 3600 pF ($Q_{gs}$ = 21 nC) indicates that OptiMOS™ 5 will have a transition of $I_D$ with less gate charge.

The reverse transfer capacitance $C_{rss}$, also called Miller capacitance, is another parasitic capacitance of a MOSFET during which drain-source voltage $V_{DS}$ is transitioning. In **Figure 10** we can see that OptiMOS™ 5 has more linear capacitances, which are reflected in switching waveforms of $V_{DS}$, shown in **Figure 11**.

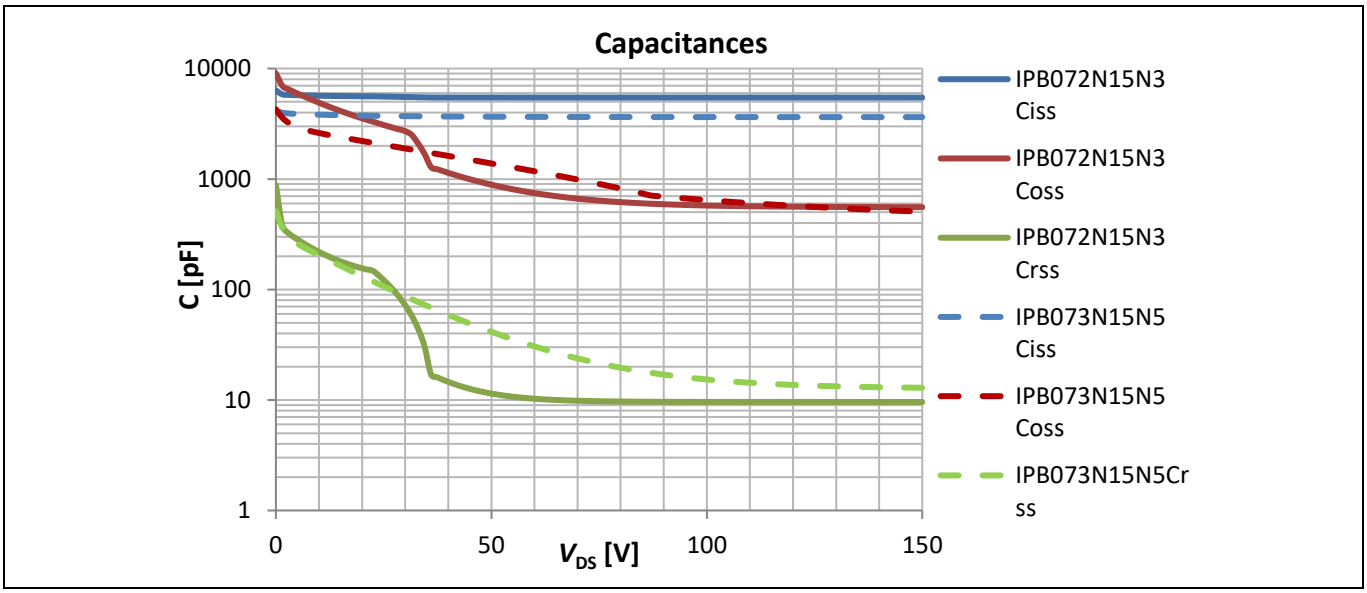



**Figure 10 Capacitances of 150 V OptiMOS™ 3, OptiMOS™ 5**

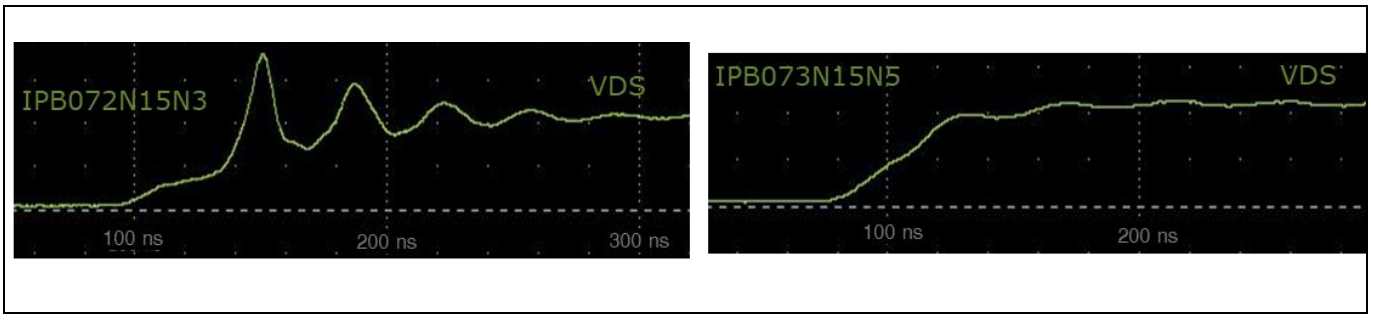



**Figure 11 Effect of parasitic capacitance on drain-source voltage**

A smoother transition of $V_{DS}$ translates directly into lower overshoots and less EMI.

### Input capacitance Ciss, reverse recovery capacitance Crss and output capacitance Coss

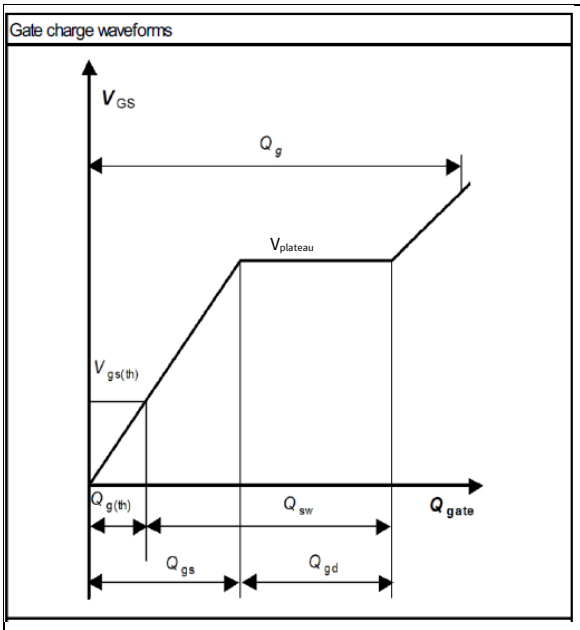
**The output capacitance $C_{oss}$ = $C_{gd}$ + $C_{ds}$** provided in the datasheet is a capacitor value at a single point in **Figure 10** at specified test voltage (in this case, 75 V). The linearity of the $C_{oss}$ curve also has an effect on the $V_{DS}$ waveform shown in **Figure 10**.

**The output charge $Q_{oss}$** is simply integration of $C_{oss}$ over a specified $V_{DD}$ voltage (in this case 0 V to 75 V). This value has to be charge or discharged for each turn-on and turn-off of a MOSFET. From the datasheet OptiMOS™ 3 has a value of 179 nC and OptiMOS™ 5 a value of 136 nC, which tells us that switching losses in the OptiMOS™ 5 generation will be lower.

The $Q_{oss}$ charge is contained in the $Q_{rr}$ area shown in **Figure 17**, but it is often referred to only as $Q_{rr}$.

# 8 Gate charges: $Q_{g(th)}$,$Q_{gs}$, $Q_{gd}$, $Q_{sw}$, $Q_g$

Referring to **Figure 12**, we can identify all charges which are stated in the datasheet.




**$Q_{g(th)}$** – the charge applied to the MOSFET by the gate driver to reach the onset of $I_D$ current change

**$Q_{gs}$** – the charge required to complete the $I_D$ current transition, and will affect the rate of change of $I_D$, i.e. di/dt

**$Q_{gd}$** – the charge required to complete the $V_{DS}$ voltage transition, and will affect the rate of change of $V_{DS}$, i.e. dv/dt

**$Q_{sw} = (Q_{gs} + Q_{gd} - Q_{th})$** – the charge required to complete the transition of $I_D$ and $V_{DS}$

**$Q_g$** – a total charge required to fully turn-on the MOSFET

**Figure 12 Gate charge waveform**

In our example the OptiMOS™ 5 has a smaller $Q_{gd}$ than OptiMOS™ 3 and requires lower gate drive current.

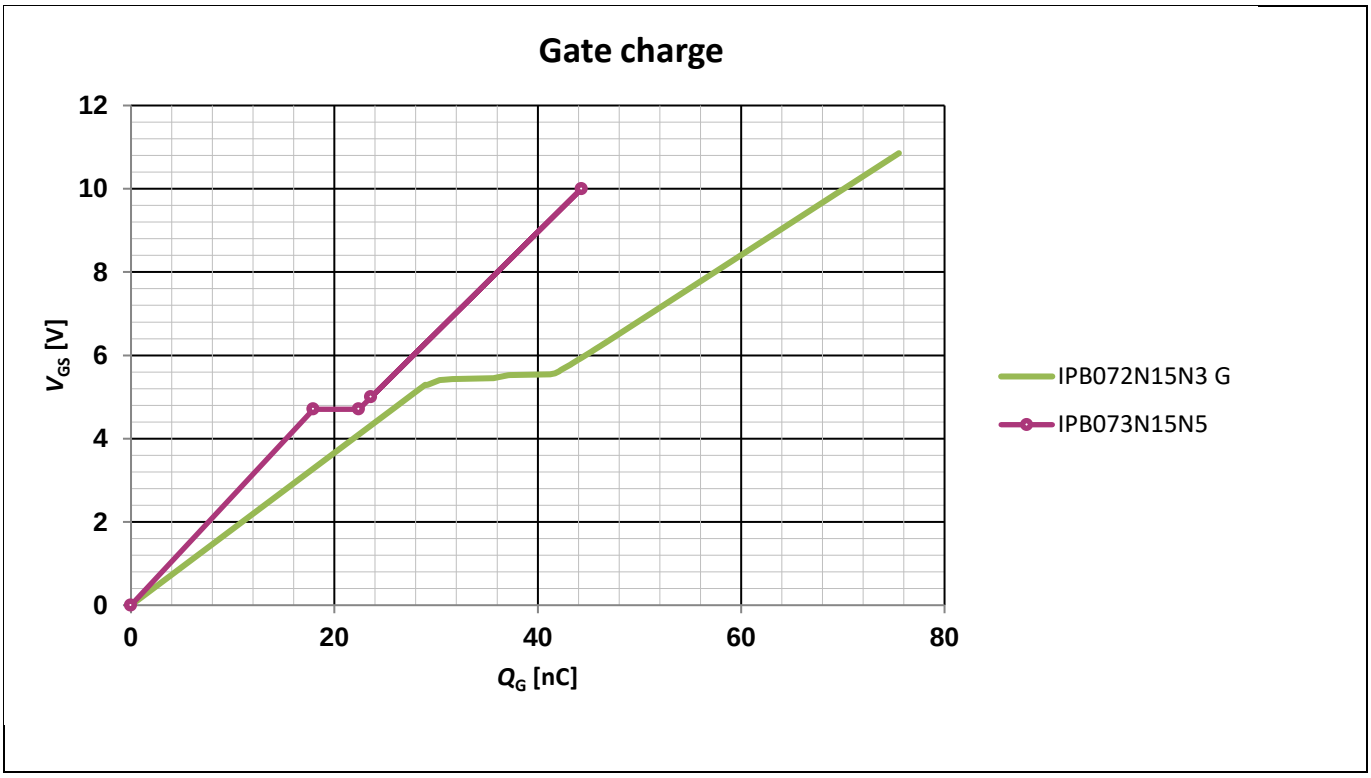



**Figure 13 Gate charge for OptiMOS™ 3 and OptiMOS™ 5**

# 9 Gate threshold voltage $V_{GS(th)}$

This voltage defines the onset of $I_D$ current change. In applications in which gate ringing can occur, a MOSFET with lower $V_{GS(th)}$ can turn-on unintentionally. With a higher temperature the $V_{GS(th)}$ level is dropping, as shown in **Figure 14**.

The minimum $V_{GS(th)}$ voltage of 150 V in the OptiMOS™ 5 is increased by 1 V (from 2 V to 3 V), which improves the gate source immunity to noise.

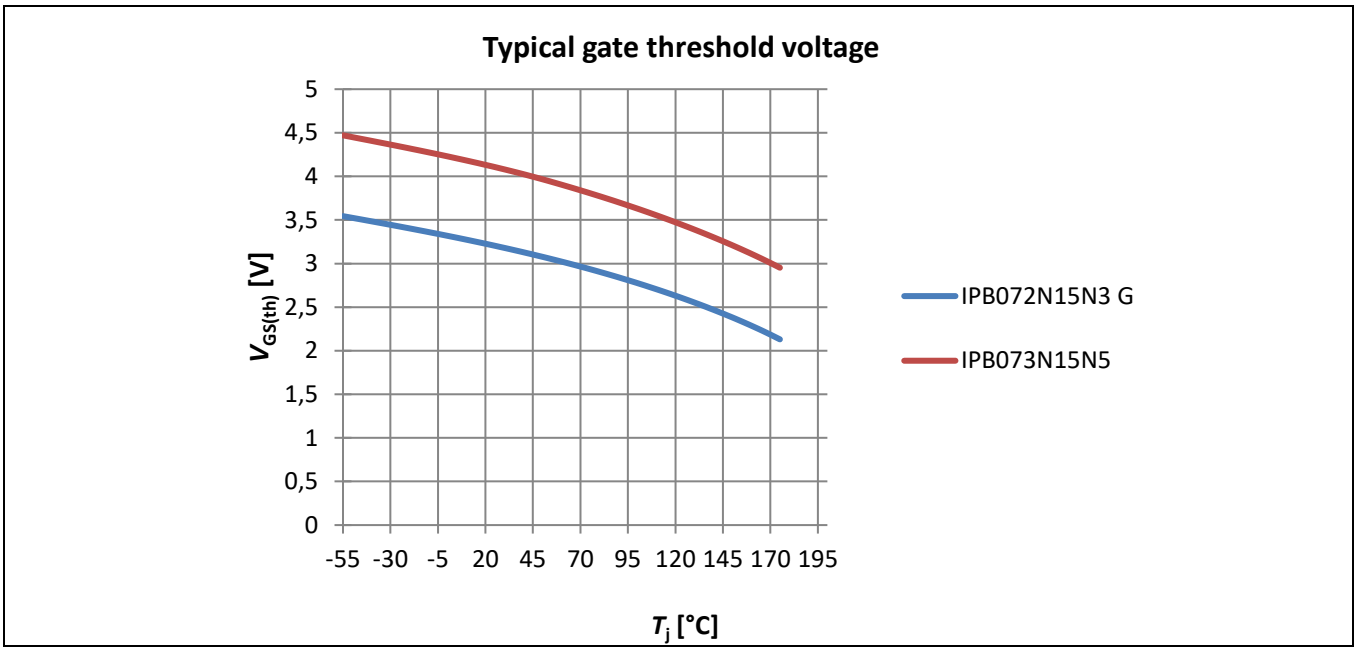



**Figure 14 Typical gate threshold voltage**

***Attention:*** ***In applications such as high-power motor drives in which many MOSFETs are paralleled, the $V_{GS(th)}$ difference between the MOSFETs should be as small as possible. This value depends on MOSFET technology as well as production accuracy.***

Infineon MOSFETs are showing extremely narrow $\Delta V_{GS(th)}$ production trends, which makes them a perfect choice for high-current applications where paralleling is required. In addition, even narrower $\Delta V_{GS(th)}$ can be obtained by using non-merged lot MOSFETs, which ensures that MOSFETs come from a single production lot.

In order to demonstrate the effect of $V_{GS(th)}$ imbalance, six MOSFETs are paralleled in half-bridge configuration. The MOSFET with the lowest $V_{GS(th)}$ (MOSFET no. 5 in **Figure 15**) will take the most current and heat up more than other MOSFETs. Due to the fact that $V_{GS(th)}$ has a negative temperature coefficient (decreasing $V_{GS(th)}$ with higher $T_j$), a MOSFET with the lowest $V_{GS(th)}$ could experience thermal runaway.

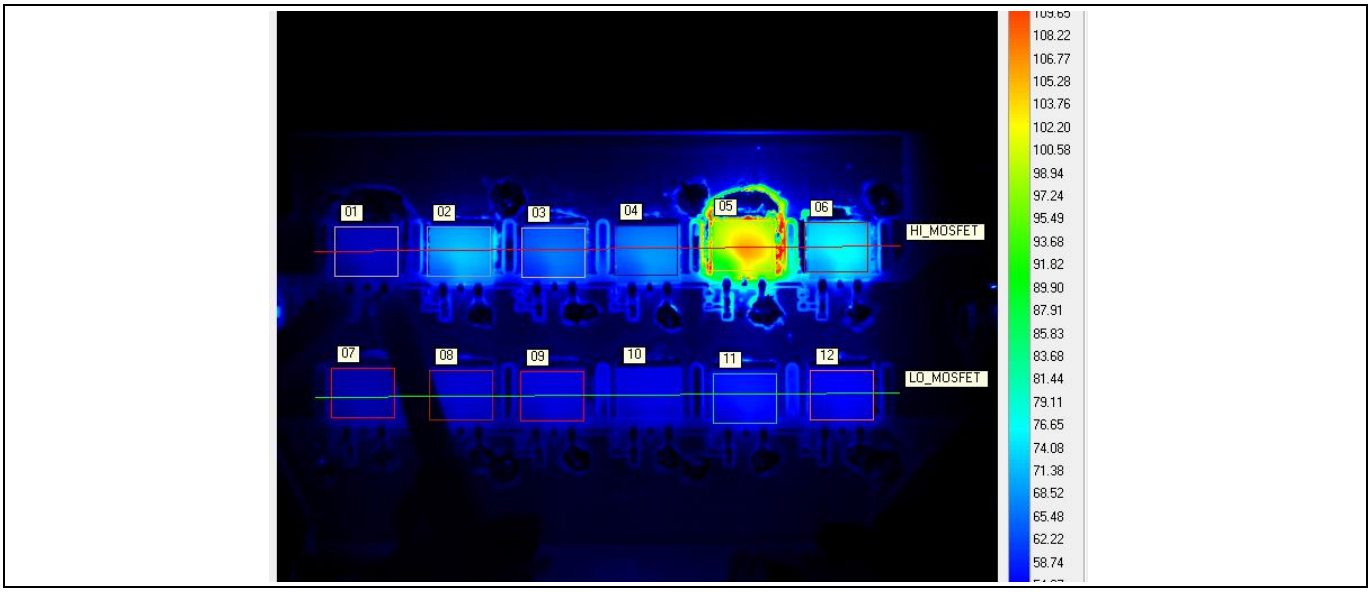



**Figure 15 MOSFET no. 5 has the lowest $V_{GS(th)}$ and the highest temperature**

# 10 Reverse diode recovery charge $Q_{rr}$, and reverse recovery time $t_{rr}$

These two parameters are specified in the datasheet, and unfortunately are valid only for this condition. If any of the following conditions change, the value of $Q_{rr}$ will change as well:

1. $V_R$
2. $I_F$
3. $di_F/dt$

Since IPB072N15N3 and IPB073N15N5 are evaluated at different diode current $I_F$, it is not possible to compare $Q_{rr}$ and $t_{rr}$ values.

However, Infineon's extended bench test reveals that under the same condition the OptiMOS™ 5 IPB073N15N5 has about 60 percent lower $Q_{rr}$ than OptiMOS™ 3 IPB072N15N3.

In hard-switching applications such as motor drives, the $Q_{rr}$ value directly affects the switching losses, switching waveforms and $V_{DS}$ overshoot.

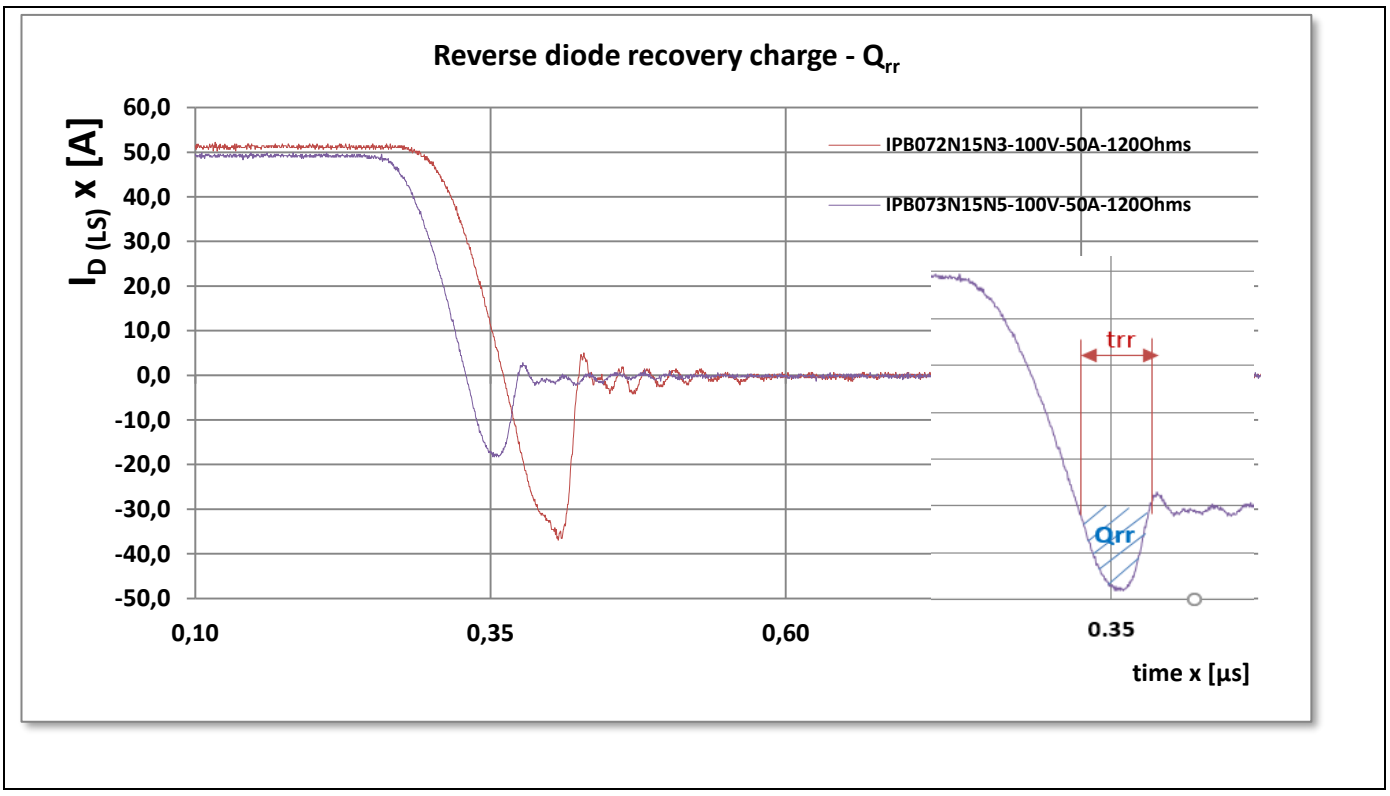



**Figure 16 Reverese recovery charge for OptiMOS™ 3 and OptiMOS™ 5 at 100 V/50 A**

# 11 Thermal resistance, junction-case $R_{th\_J\text{-}C}$

This parameter can be used to calculate the temperature of the silicon die when the power loss is known using the formula:

$$\Delta T = P_{loss} * Rth$$

In general, the thermal resistance of junction to case $R_{th\_J\text{-}C}$ is much lower than the thermal resistance from case to heatsink. While the typical $R_{th\_J\text{-}C}$ is in the range of typical 0.2 K/W, the thermal resistance between case and the PCB is much higher $R_{th\_C\text{-}HS}$ and ranges from 1 to 5 K/W depending on the PCB type and number of thermal vias used (all values are based on best-in-class $R_{DS(on)}$ in $D^2PAK$ package).

From Table 1 IPB072N15N has $R_{th\_J\text{-}C,max}$ = 0.5 K/W and the IPB073N15N5 has $R_{th\_J\text{-}C,max}$ = 0.7 K/W.

We can conclude that the $R_{th\_J\text{-}C}$ is more critical for better thermally conductive PCBs such as IMS PCBs, because it is a bigger percentage of the total thermal resistance from silicon die to heatsink $R_{th\_j\text{-}hs}$.

Besides the $R_{th\_J\text{-}C}$, the $Z_{th\_J\text{-}C}$ can be also very important in transient conditions for power pulses of less than 100 ms. In our example the maximal thermal impedance of IPB072N15N3 for 1 ms at a single pulse is 0.1 K/W and for IPB073N15N5 it is 0.2 K/W. This means that IPB073N15N5 can handle half of the pulse power for 1 ms. In motor drive applications short high peak currents are possible, so the designer needs to ensure that the $T_j$ is not exceeded during transient conditions.

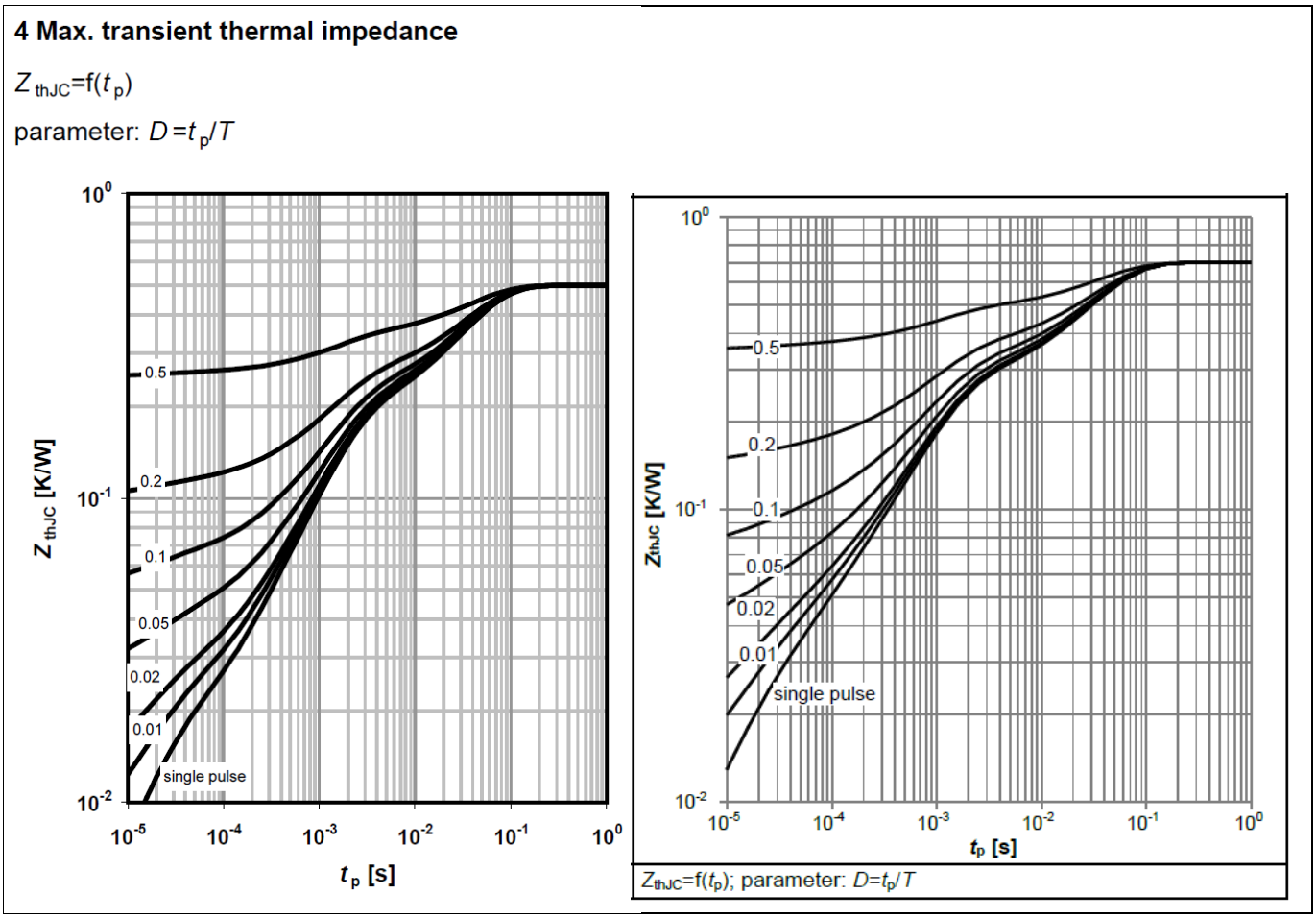



**Figure 17 Max. transient impedance for IPB072N15N3 (left) and IPB073N15N5 (right)**

# 12 Conclusion

During circuit design with OptiMOS™ 5 or in the process of interchanging MOSFETs on an existing design, an engineer should carefully examine both datasheets to get an overall picture and understanding of both MOSFETs. An example of OptiMOS™ 3 and OptiMOS™ 5 150 V generations was shown in this document, identifying which parameters influence specific behavior of a MOSFET. The same approach can be used for other voltage classes, some of which are shown in this document on OptiMOS™ 5 80 V.

In some cases, it will be difficult to quantify the effect of different MOSFET parameters on their behavior.

One good option is to establish a simulation platform with SPICE simulation models, which can reveal the differences in which tuning of the gate driving circuit can be easily done.

If during simulation or a bench test the ringing and oscillations are observed, some of the following methods can be utilized:

- Slow down MOSFET by implementing higher gate resistor value $R_g$
- Slow down MOSFET by implementing $C_{gs}$ – typical values 1 nF to 5 nF
- Introduce a damping gate resistor in the gate drive circuit if external $C_{gs}$ is used – typical value 10 Ω
- Drain-source RC snubber – for example 1 nF/2 Ω

If the $R_{DS(on)}$ value is the same, due to higher $R_{th}$ and $Z_{th}$, the OptiMOS™ 5 will result in higher MOSFET temperatures than OptiMOS™ 3 if they dissipate the same power, but this power dissipation can be reduced by:

- Lower $R_{DS(on)}$
- Lower switching losses – faster di/dt and dv/dt, lower $V_{DS}$ overshoot
- Better body diode – softer recovery, lower $Q_{rr}$ and lower $I_{rrm}$ , less ringing and EMI
- Better curren sharing with lower $\Delta V_{GS(th)}$ production spread ($V_{GS(th),min}$ – $V_{GS(th,max}$ values) for paralleled MOSFETs

# 13 Revision history

| Document version | Date of release | Description of changes |
|---|---|---|
| V 1.0 | 28-05-2020 | First release |
| | | |
| | | |

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