Full-bridge converter for UPS

D^2PAK/D^2PAK-7 kit

About this document

This user guide describes the Infineon full-bridge demo board for UPS. The current design considers only the power section including drivers and power devices with **D^2** packages. **D^2** 7-pin packages can also be used in this demo board, which enables users to evaluate the performance of power MOSFETs and their drivers.

Scope and purpose

This document is intended to describe the functionalities of UPS converting DC to AC voltages. Users can then evaluate the performance of power MOSFETs with gate driver ICs. With Infineon low-$R_{DS(on)}$ MOSFETs the demo board can help reduce system cost and time-to-market.

Intended audience

This document addresses the market for UPS manufacturers with the goal of providing a high-performance system solution at low cost.

Table of contents

1 Full-bridge converter for UPS with D²PAK/D²PAK-7 kit

1.1 Overview

The full-bridge converter kit is a demo board for UPS applications. It contains two sections of half-bridge drivers and power devices, as shown in Figure 1.

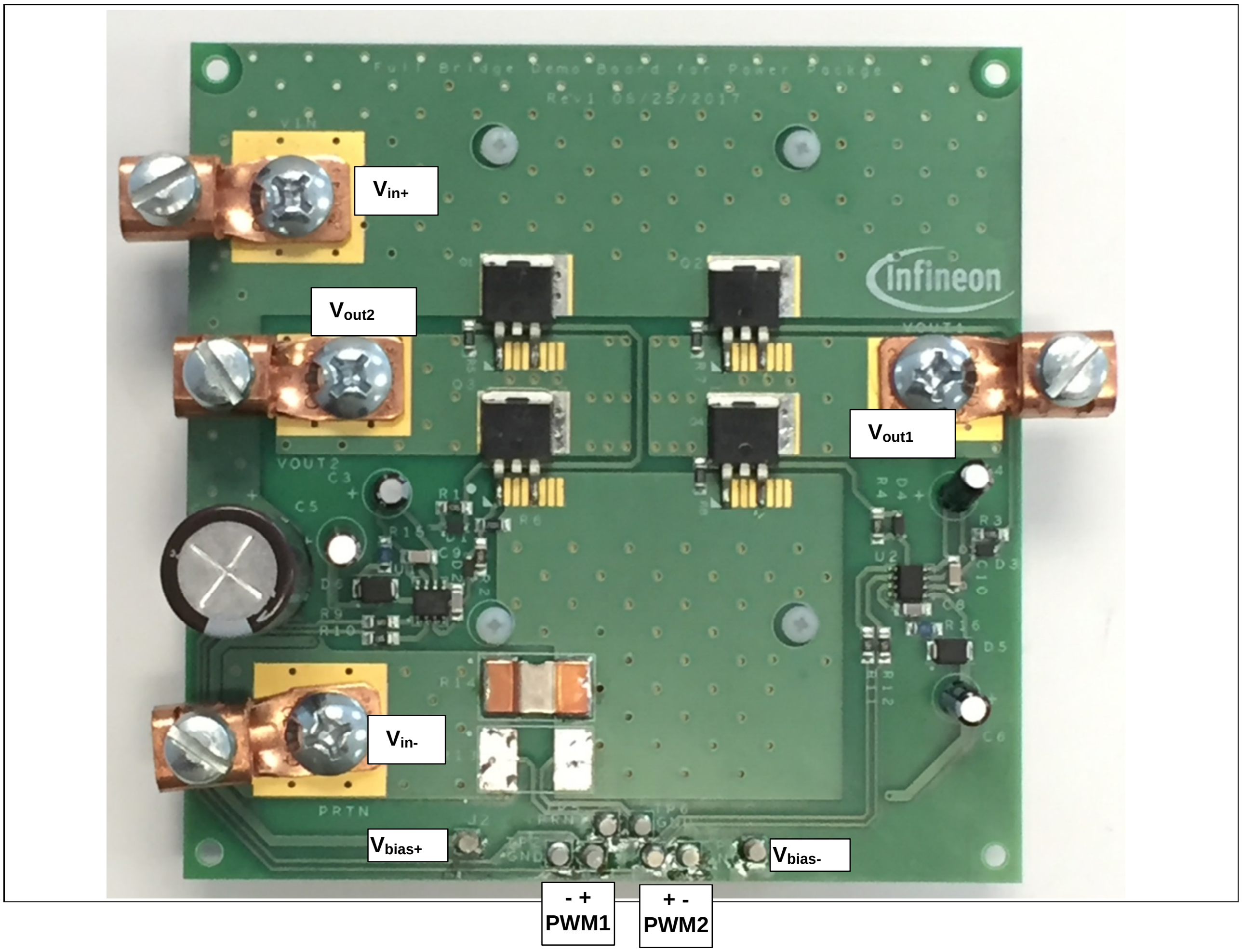

Figure 1 Full-bridge converter demo board (120 mm × 120 mm)

The demo board needs two power supplies to provide an input voltage and a bias voltage. The voltages of both power supplies are typically 12 V, which can be changed based on an application. The outputs can be connected to a transformer. In this user guide, a transformer is used to get an AC voltage of 220 V with the input voltage of 12 V. In order to power up the demo board, two synchronized PWM signals are needed to control switching of four power MOSFETs.

1.1.1 Key features

The capabilities of the full-bridge converter for UPS with D^2/D^2 7-pin kit are as follows:

- D^2/D^2 7-pin kit for MOSFETs
- Separate V_{in} and bias voltages (12 V is used in this user guide)
- 600 V gate driver IC with +/- 4 A peak drive current (IRS2186)
- Current Sense (CS) information
- A heatsink can be mounted with four screws, which can be placed at the back or at the front

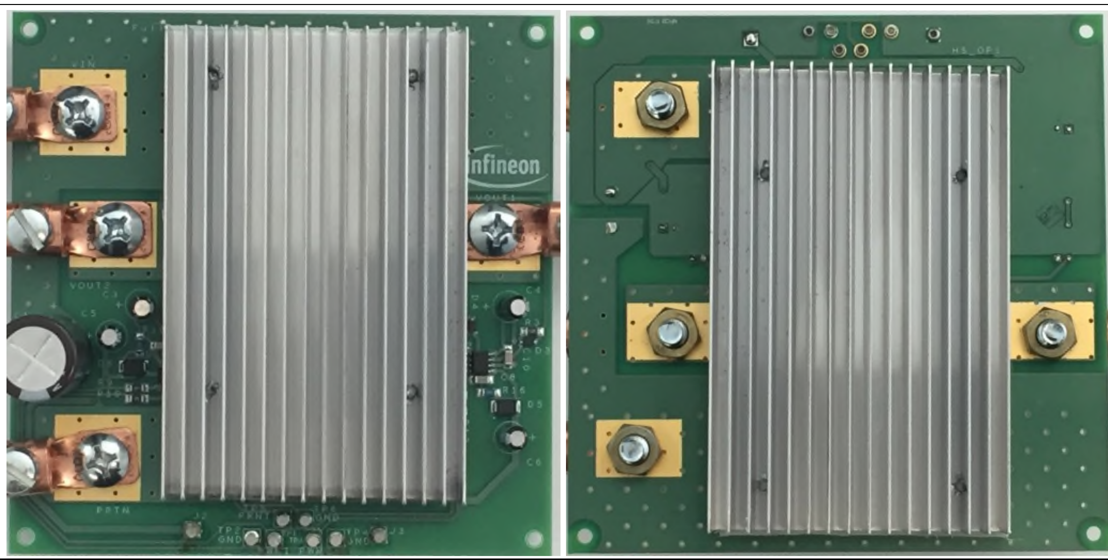

Figure 2 Heatsink (4 × 2.5 × 0.5 inches) mounted at the front or back with thermal pad

(Heatsink: ACCEL Thermal 914; Thermal pad: Berguist Gap Pad 5000S35, 20 mils)

1.2 Schematic

A schematic of the demo board is shown in Figure 3. In the demo board, four MOSFETs ([IRFS7430]) are used. D^2 7-pin packages can be used if they are desired for evaluation. Two IRS2186 drivers are used to drive four MOSFETs. Only two PWM signals are needed to control timing of the switching of the four MOSFETs. D1~4 four diodes are used to have a slow turn-off to avoid high V_{ds} spike during turn-off.

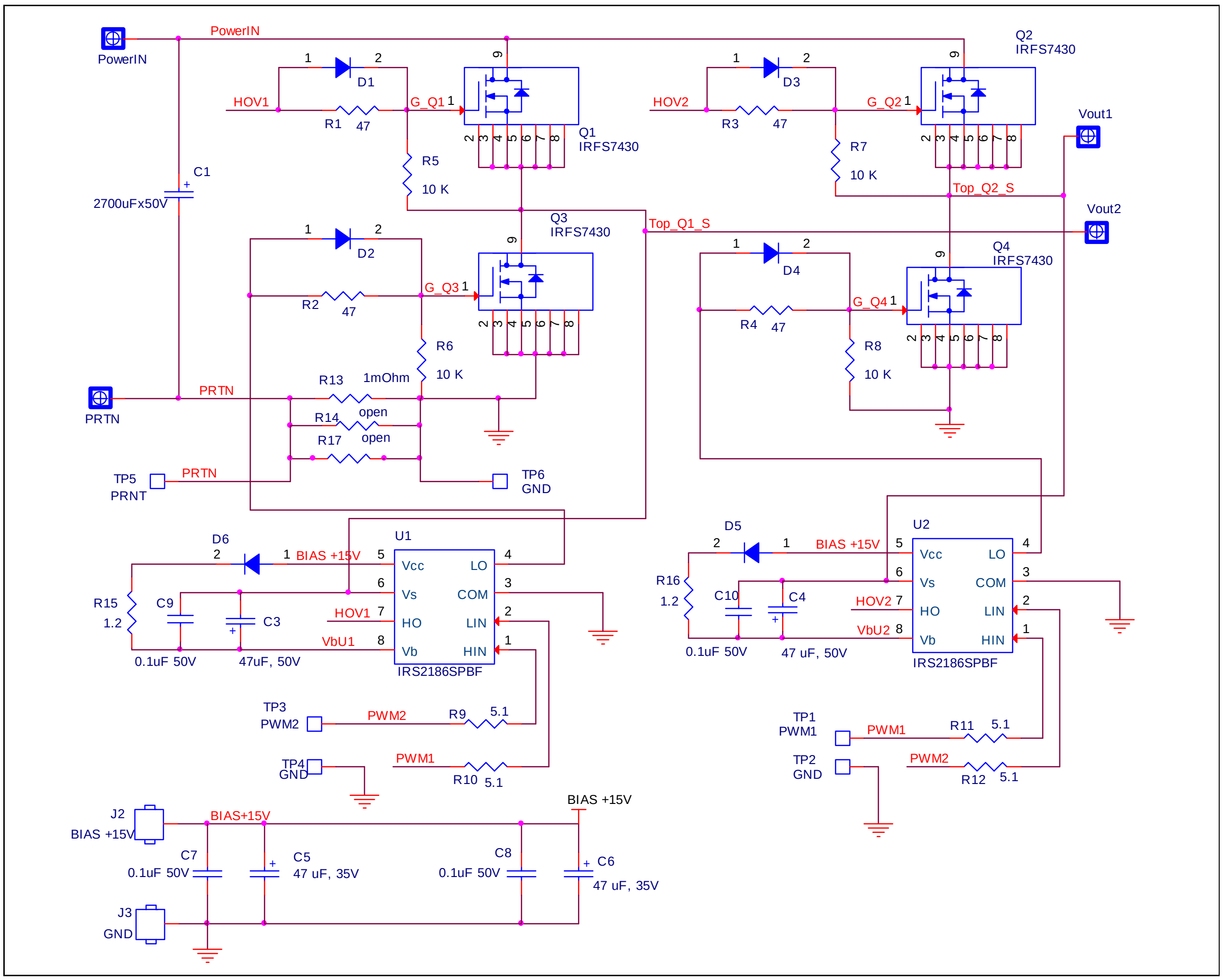

Figure 3 Schematic of the demo board

1.3 Layout

The demo board PCB has only two layers, as shown in Figure 4. Fabricated with FR4 material, both layers are 2 oz. copper with a board thickness of 62 mils (1.58 mm).

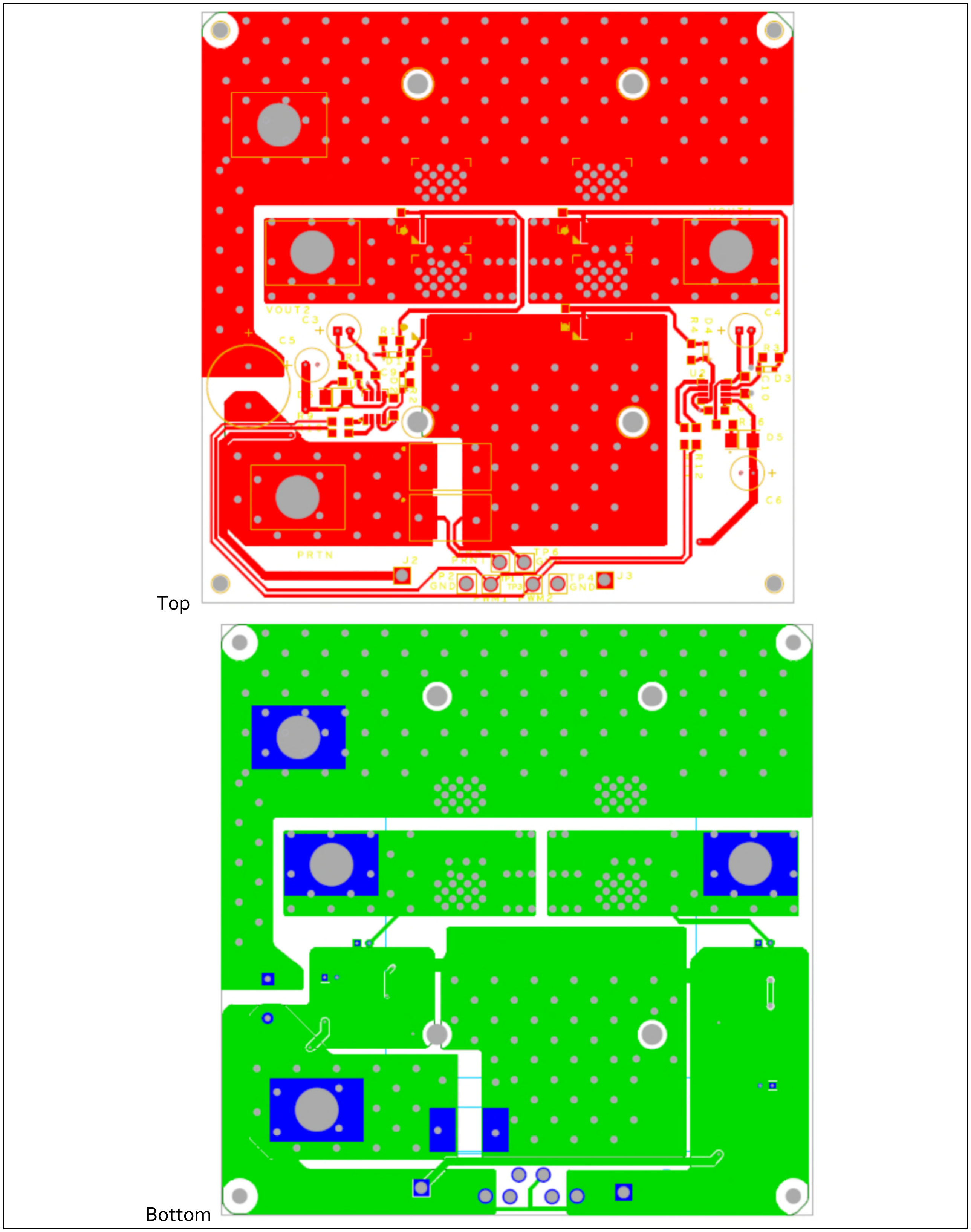

Figure 4 PCB top and bottom layers

1.4 Power-up procedure

Always connect the bias, two PWM signals and load first, then increase the input voltage from zero.

1.4.1 PWM signal selections

This user guide describes a set-up providing a 50 Hz square-wave AC output. Therefore, both PWM signals are set with 50 Hz. The dead-time between the two legs has to be set high enough that the reset of the transformer is completed. A shorter dead-time increases total turn-on time, which may saturate the transformer. A value of 0.9 ms was selected to do the tests. Both PWM signals have an amplitude of 10 V.

1.5 Performance evaluations

Test conditions:

V_{in}:	12 V
V_{bias}:	12 V
PWM 1, 2:	50 Hz, 10 V, with 10 ms delay between them plus 0.7 ms dead-time
Load:	Transformer (primary connected to V_{out1} and V_{out2}, secondary connected to incandescent light bulbs, load of 420 W)
Airflow:	No

1.5.1 Performance with heatsink at the front

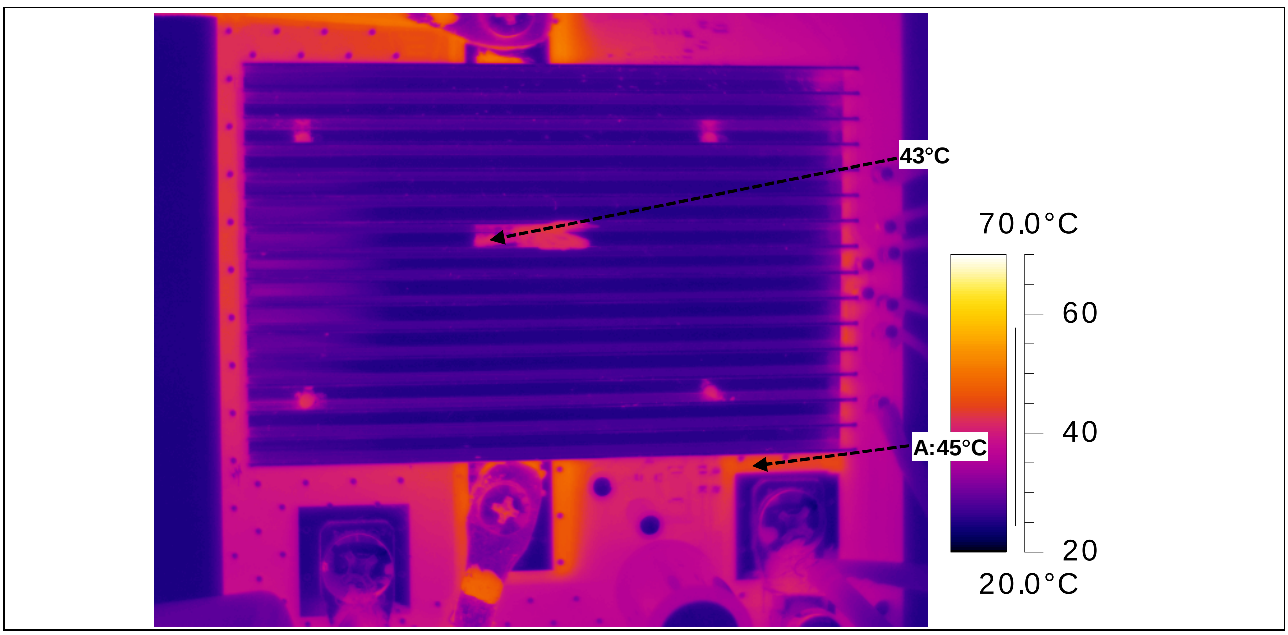

Figure 5 Front thermal image after 1 hour

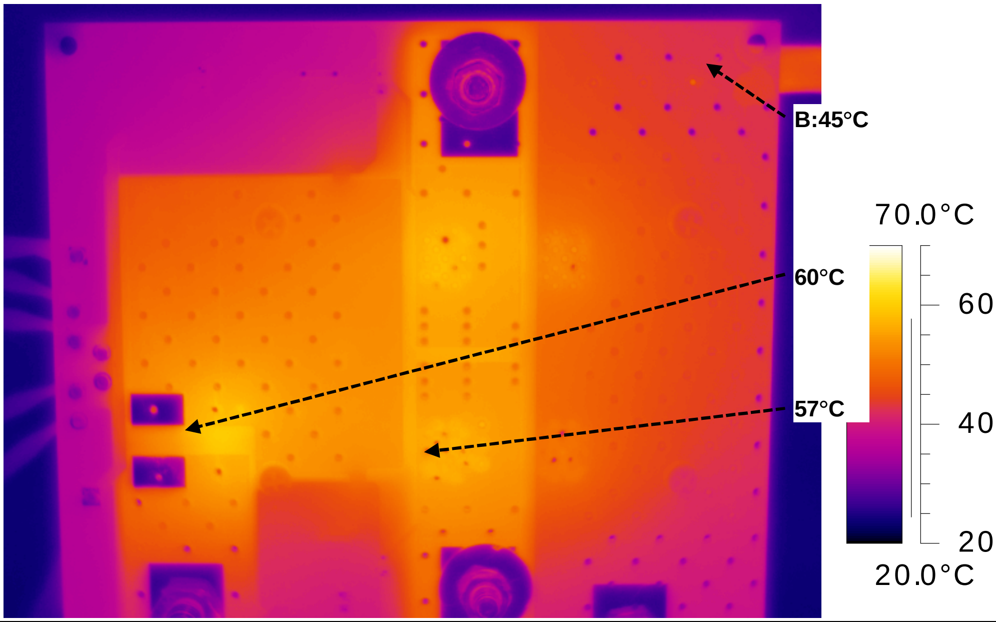

Figure 6 Back thermal image after 1 hour

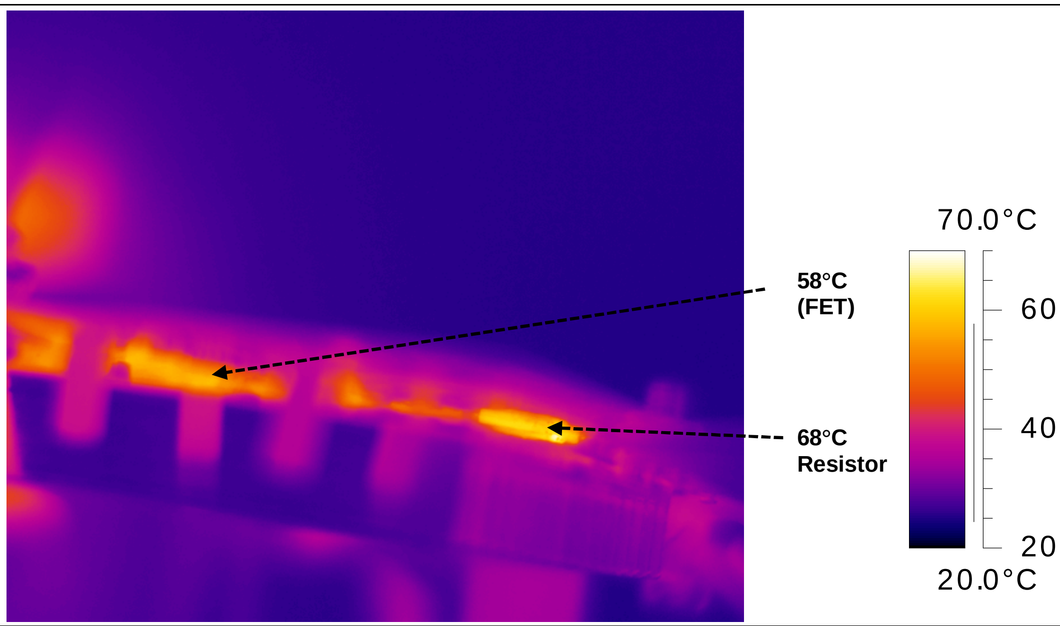

Figure 7 Side thermal image after 1 hr

Comparing the temperature readings at points A and B between the front and back sides at the corner in Figures 6 and 7 shows that they are the same. Case temperatures of the MOSFETs are 1°C higher at the front than at the back, as shown in Figures, 6, 7 and 8.

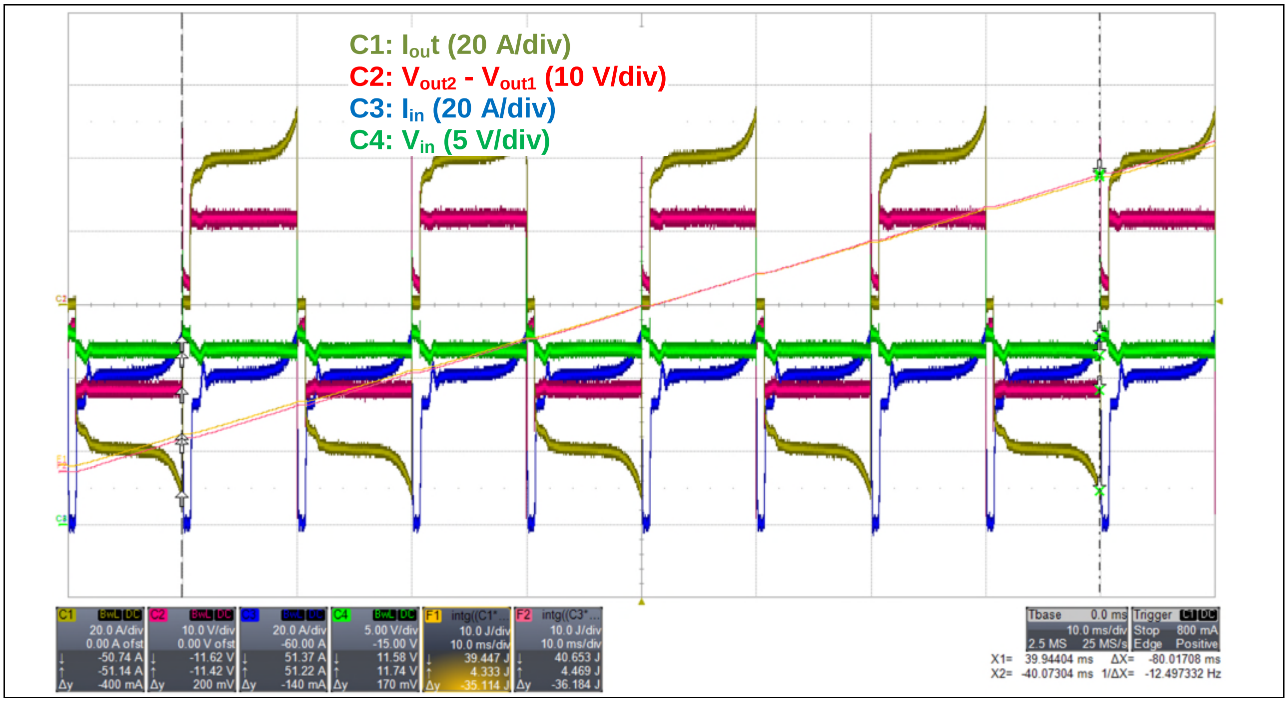

Figure 8 Typical input and output power measurement after 1 hour

Table 1 **Efficiency after 1 hour**

No.	Efficiency (percent)
1	96.5
2	96.5
3	96.5
4	96.7
5	96.6
6	96.7
7	96.3
8	96.3
Average	96.5
Stdev	0.1

The average efficiency shown in Table 1 is 96.5 percent at 420 W load. The average total power loss is about 13 W. The reset time for the transformer is about 20 µs, as shown in Figure 9, which is much less than the dead-time of 700 µs. The MOSFET turn-off waveforms are shown in Figure 10. Since I_{ds} was measured by a Rogowski coil current probe (C2), its zero level has an offset (I22 = -25 A), as shown in Figure 11. The turn-off switching power loss can be calculated as:

f(Hz)× $\int_{t1}^{t2}[I(t) - I22] \cdot V(t)dt$ = f(Hz) × [(F12 - F11 - I22.(F22 - F21)]

= 50 Hz ×|(116 µJ – (25 × 16.7 µ))| = 15 mW.

The turn-off switching power loss for Q2, 3 and 4 is 16, 17 and 13 mW, respectively. Therefore, switching power losses are negligible.

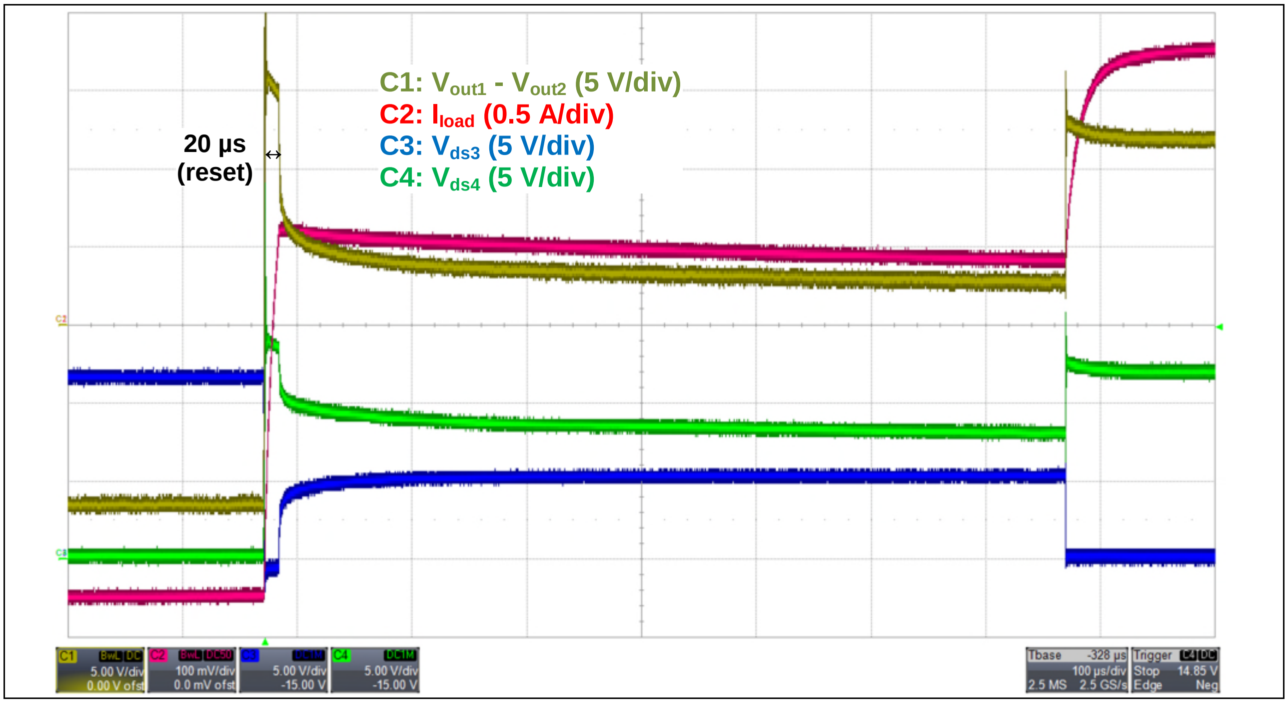

Figure 9 Waveforms during the dead-time

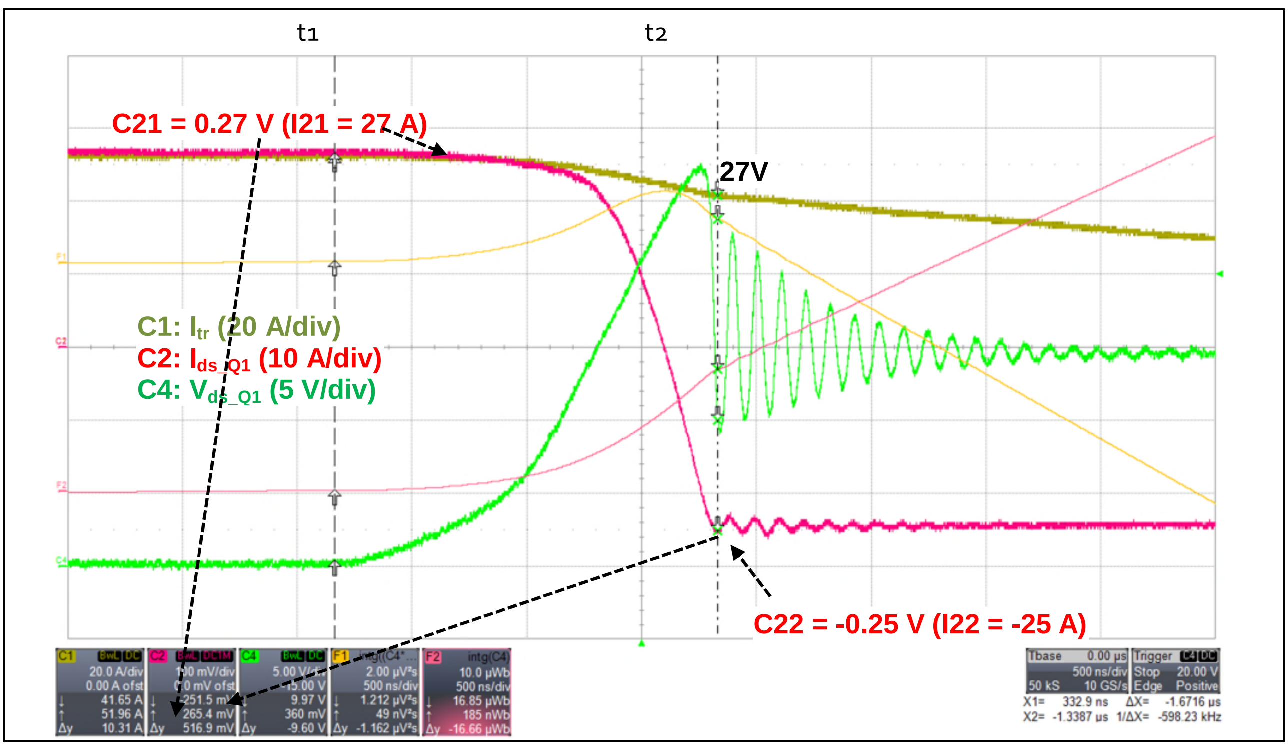

Figure 10 Turn-off waveforms

F1: Integral of C4 x C2 (power), F11 = 4.9 µJ, F12 = 121 µJ, ΔF1 = 116 µJ

F2: Integral of C4 (voltage), F21 = 0.19 µV.s, F22 = 16.9 µV.s, ΔF2 = 16.7 µV.s

1.5.2 Performance with heatsink at the back

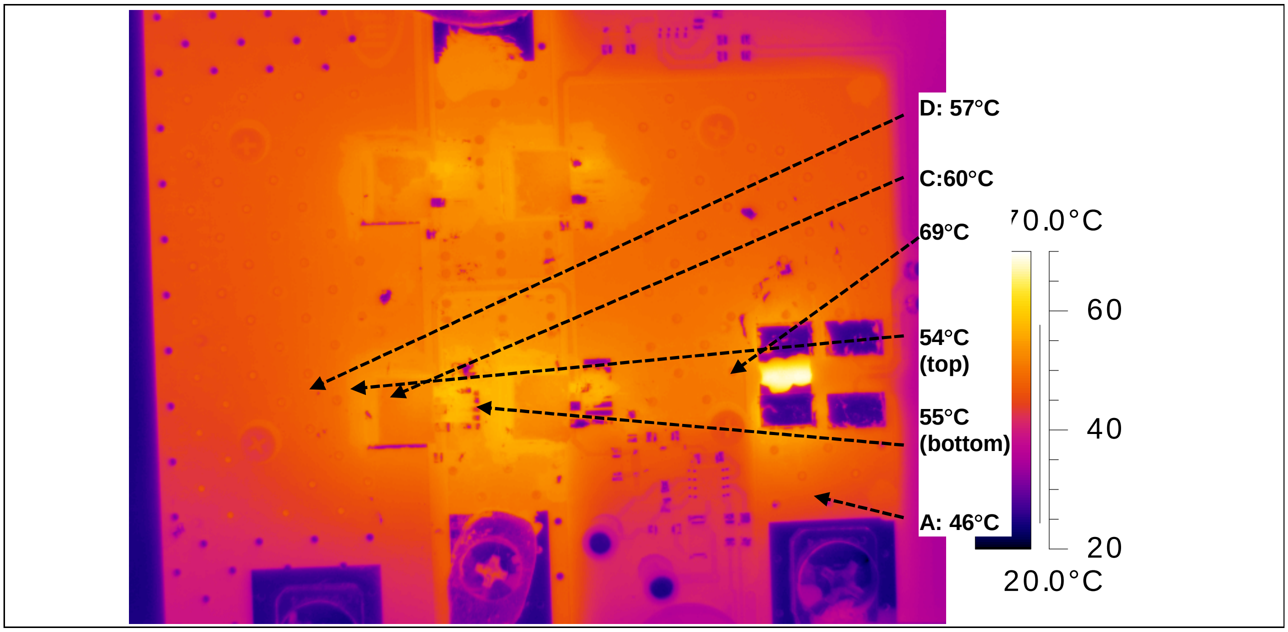

Figure 11 Front thermal image after 1 hour

As shown in Figure 12, the corner temperature reading (A) is 1°C higher than that with the heatsink at the front in Figure 6. The corner temperature reading (B) as shown in Figure 13 is 2°C higher than that with the heatsink at the front in Figure 7. It indicates that the heatsink placed at the front is slightly more effective. Its average efficiency is 96.4 percent, shown in Table 2, which is 0.1 percent lower than that shown in Table 1 with the heatsink at the front. The higher efficiency is consistent with lower temperature readings at locations A and B, shown in Figures 6, 7, 12 and 13.
The PCB temperature readings shown in Figure 12 at locations C and D show 3°C difference, which indicates that source bond wires result in additional power loss.

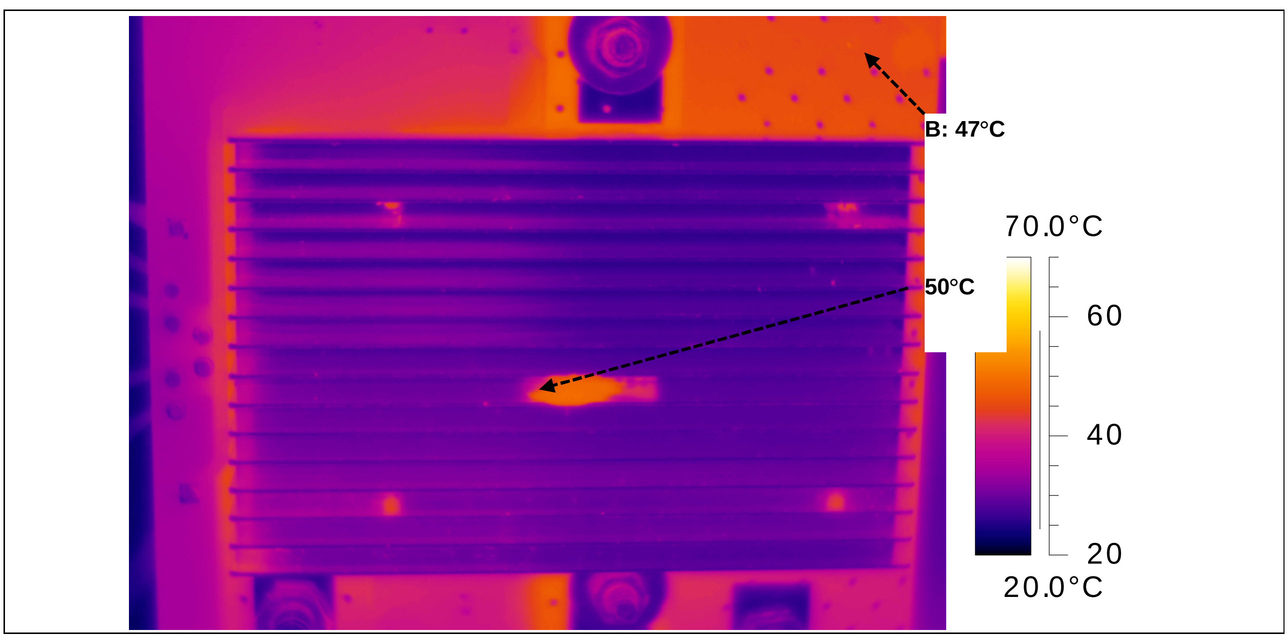

Figure 12 Back thermal image after 1 hour

Table 2 Efficiency after 1 hour

No.	Efficiency (percent)
1	96.6
2	96.3
3	96.4
4	96.5
5	96.4
6	96.4
7	96.3
8	96.3
Average	96.4
Stdev	0.1

1.6 Power loss estimations of MOSFETs and CS resistor

Table 3 shows the average $R_{DS(on)}$ at 12 V_{GS} is 0.72 mΩ. As shown in Figure 14, the RMS current for the transformer is 39.2 A. Therefore, the conduction power loss for each MOSFET can be estimated as $39.2^2 \times 0.72/2 = 0.55$ W, which is much higher than the switching loss of 15 mW, shown in Figure 11. Based on the total power loss of 13 W, total MOSFET power loss is about $0.55 \times 4/13 = 17$ percent.

The power loss of the CS resistor can be estimated as $39.2^2 \times 1 = 1.5$ W. This is about 12 percent of the total power loss, which explains why it has the highest case temperature.

Table 3 $R_{DS(on)}$ measurements at 12 V_{GS}

No.	$R_{DS(on)}$ (mΩ)
1	0.73
2	0.70
3	0.70
4	0.69
5	0.76
6	0.71
7	0.71
Average	0.72
Stdev	0.02

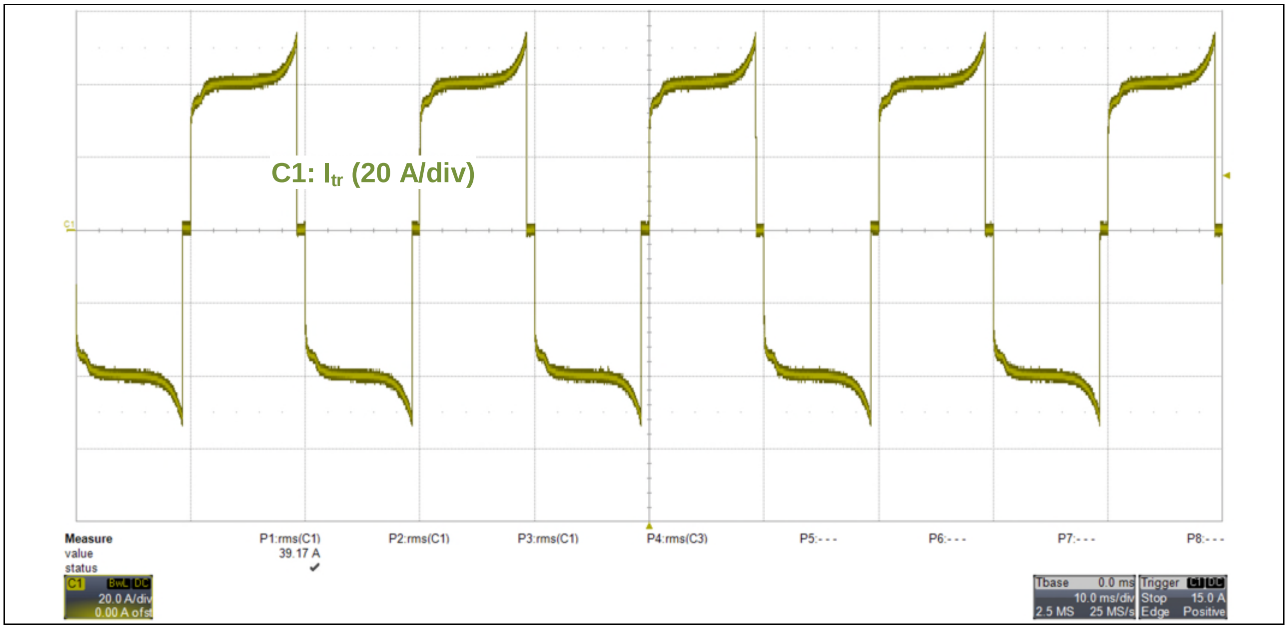

Figure 13 Transformer RMS current measurement (39.2 A)

1.7 Bill of Materials (BOM)

Item	Quantity	Part reference	Part description	Value	Part number	Manufacturer
1	1	C1	Electrolytic 2700 µF 35 V	2700 µF, 35 V		Nichicon
2	2	C3, C4, C5, C6	Electrolytic 5 × 11mm	47 µF, 35 V	UVK1V470 MED	Nichicon
3	4	C7, C8, C9, C10	0.1 µF × 50 V 1206 CoG	0.1 µF, 50 V	CGA5L2C OG1H104J	TDK
4	4	D1, D2, D3, D4	Diode, 100 VM, 300 MA	1N4148W	1N4148W-7-F	Diodes Inc.
5	2	D5, D6	Diode, 100 V, 2 A	MURS 210T3	MURS 210T3	OnSemi
6	8	J2, J3, TP1, TP2, TP3, TP4, TP5, TP6	Test point 218 mils, 90 mils	BIAS +15 V	1502-2	Keystone
7	4	PRTN, POWERIN, VOUT1, VOUT2	CONN TERM RECT LUG 4/0-2AWG 5/16	CX225-56HK-QY	CXS70-14-C	Panduit Corp
8	4	Q1, Q2, Q3, Q4	MOSFET 40 V, 0.75 mΩ, 305 nC	IRFS7430-7PPBF	IRFS7430	Infineon
9	4	R1, R2, R3, R4	Resistor 1206, 1/4 W, 1 percent	47 Ω	RC1206FR-0747RL	Yageo
10	4	R5, R6, R7, R8	Resistor 1206, 1/4 W, 1 percent	10 k	RK73H2BT TE1002F	KOA
11	4	R9, R10, R11, R12	Resistor 1206, 1/4 W, 1 percent	5.1 Ω	MCR10EZ HJ5R1	Rohm
12	1	R13	Resistor 4 W	2 mΩ	EBWB-N0020GET	Ohmite

13	2	R15, R16	Resistor 1206, 1/4 W, 1 percent	1.2 Ω	ESR18EZP F1R20	Rohm
14	1	R14, R17	-	Not fitted	Not fitted	-
15	2	U1, U2	Hi/Lo gate driver	IRS2186SPBF	IRS2186SP BF	Infineon

1.8 Additional results with D^2PAK-7 (IRFS7430-7P)

1.8.1 Performance with heatsink at the back with 420 W load

Figure 15 shows temperature readings at the front side with a heatsink at the back. Compared with the readings shown in Figure 12, the hottest point of the sense resistor is 5°C lower. The PCB reading at point A is 3°C lower, both top and bottom MOSFETs are 4 to 5°C lower, and at location C the temperature reading is 7°C lower, which shows that the source bond wires in the D^2 7-pin package result in lower power dissipation. This is consistent with the higher efficiencies shown in Table 4. Its average is 0.2 percent higher than the example shown in Table 2 with the same load. Figure 16 also shows lower temperature readings with D^2 7-pin MOSFETs. PCB location B shows 4°C lower temperature and the center 3°C lower than those shown in Figure 13. The lower power dissipation with D^2 7-pin parts is due to lower $R_{DS(on)}$, which is shown in Table 5 compared with Table 3. The average $R_{DS(on)}$ is 0.07 mΩ lower (11 percent).

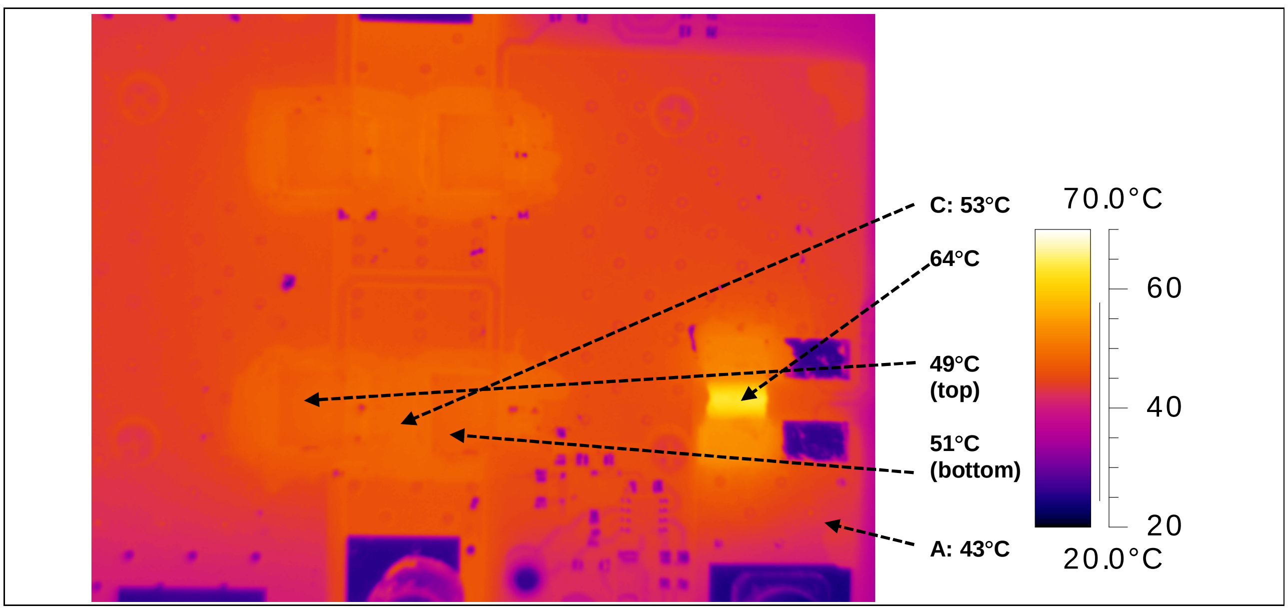

Figure 14 Front thermal image after 1 hour

Table 4 Efficiency after 1 hour

No.	Efficiency (percent)
1	96.7
2	96.7
3	96.6

Table 5 $R_{DS(on)}$ measurement at 12 V_{GS}

No.	$R_{DS(on)}$ (mΩ)
1	0.64
2	0.66
3	0.64

4	96.5
5	96.5
6	96.6
7	96.7
8	96.6
Average	96.6
Stdev	0.1

4	0.65
5	0.67
6	0.65
7	0.65
Average	0.65
Stdev	0.01

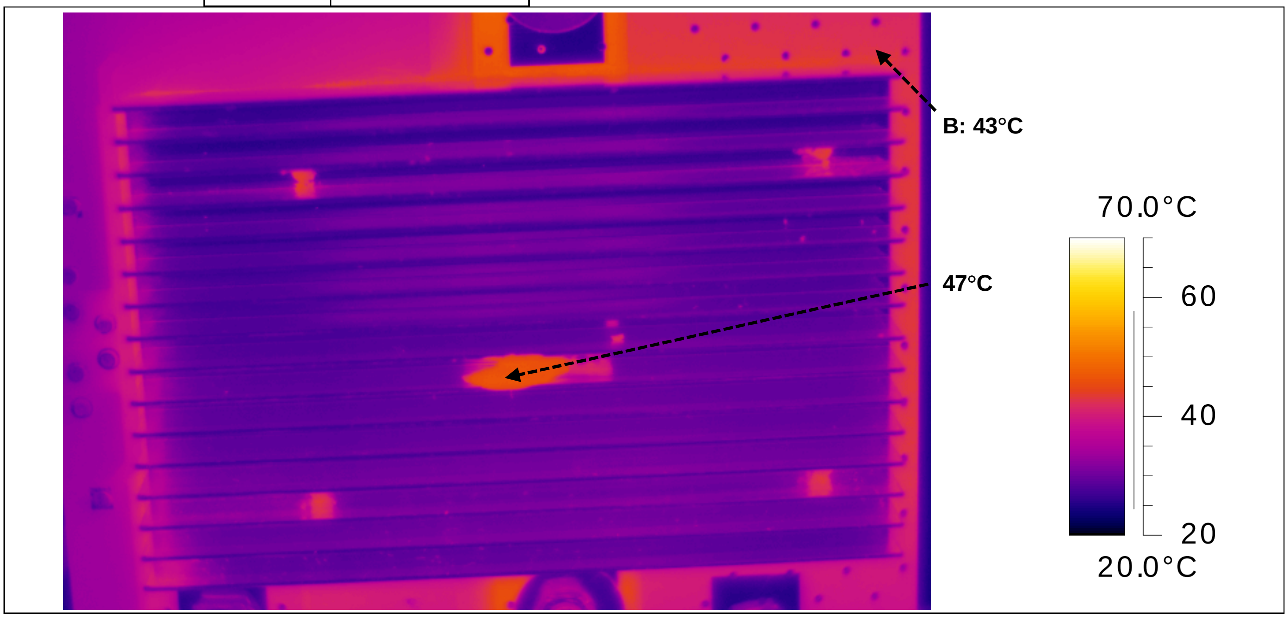

Figure 15 Back thermal image after 1 hour

1.8.2 Performance with heatsink at the back with 500 W

As shown in Figure 17, both case temperature readings at the resistor (78°C) and PCB location A (49°C) are higher than those (64°C and 44°C) with same parts at 420 W in Figure 15 and also higher than the (69°C and 46°C) with D^2 at 420 W in Figure 12. The middle of the heatsink temperature reads 55°C, as shown in Figure 18, and is 5°C higher than that with D^2 parts with 420 W, as shown in Figure 13. The average efficiency with D^2 7-pin parts shown in Table 6 is 97.0 percent, which is 0.4 percent higher than that with 420 W, shown in Table 4.

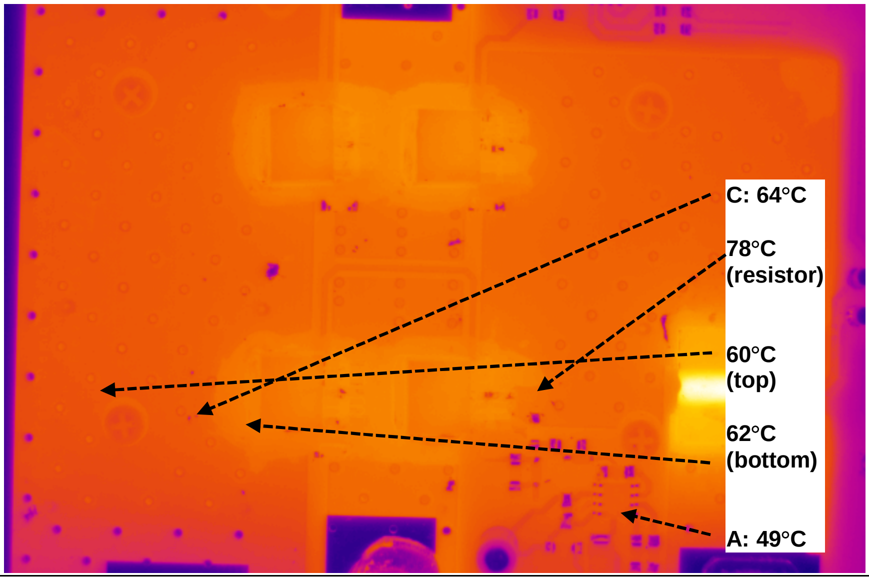

Figure 16 Front thermal image after 1 hour with 500 W

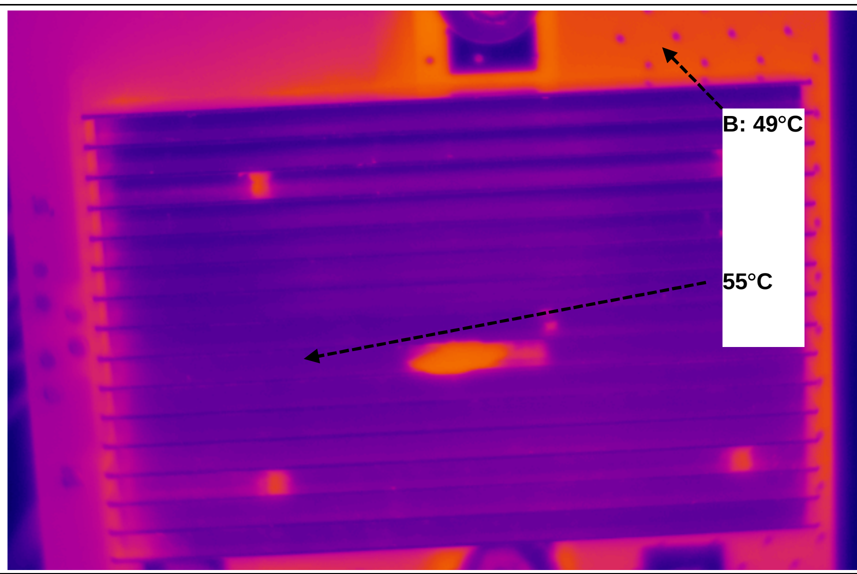

Figure 17 Back thermal image after 1 hour with 500 W

Table 6 Efficiency after 1 hour

No.	Efficiency (percent)
1	97.1
2	97.0
3	97.1
4	96.9
5	97.0
6	97.1
7	97.0
8	97.1
Average	97.0
Stdev	0.1

1.8.3 Performance with heatsink at the front with 500 W

As shown in Table 7, the average efficiency is 97 percent, which is 0.4 percent higher than that with the heatsink at the back, shown in Table 4. The temperature readings at the middle (47°C) and location A (52°C) shown in Figure 19 are both higher than those (43°C and 45°C) shown in Figure 6 due to the additional 80 W of load.

With the same load at 500 W, the temperature reading (52°C) at A shown in Figure 19 is higher than that (49°C) in Figure 17, while the reading (48°C) at B in Figure 20 is lower than that (49°C) in Figure 18. This behavior is different to that with D^2 MOSFETs. The reason is that with the D^2 7-pin package more heat can be transferred to the PCB, which makes the heatsink more effective when it is located at the back. This explains why the efficiency with the heatsink at the front is the same as that with the heatsink at the back with D^2 7-pin MOSFETs.

Table 7 Efficiency after 1 hour

No.	Efficiency (percent)
1	96.9
2	96.9
3	97.1
4	97.1
5	97.1
6	96.9
7	97.0
8	96.9
Average	97.0
Stdev	0.1

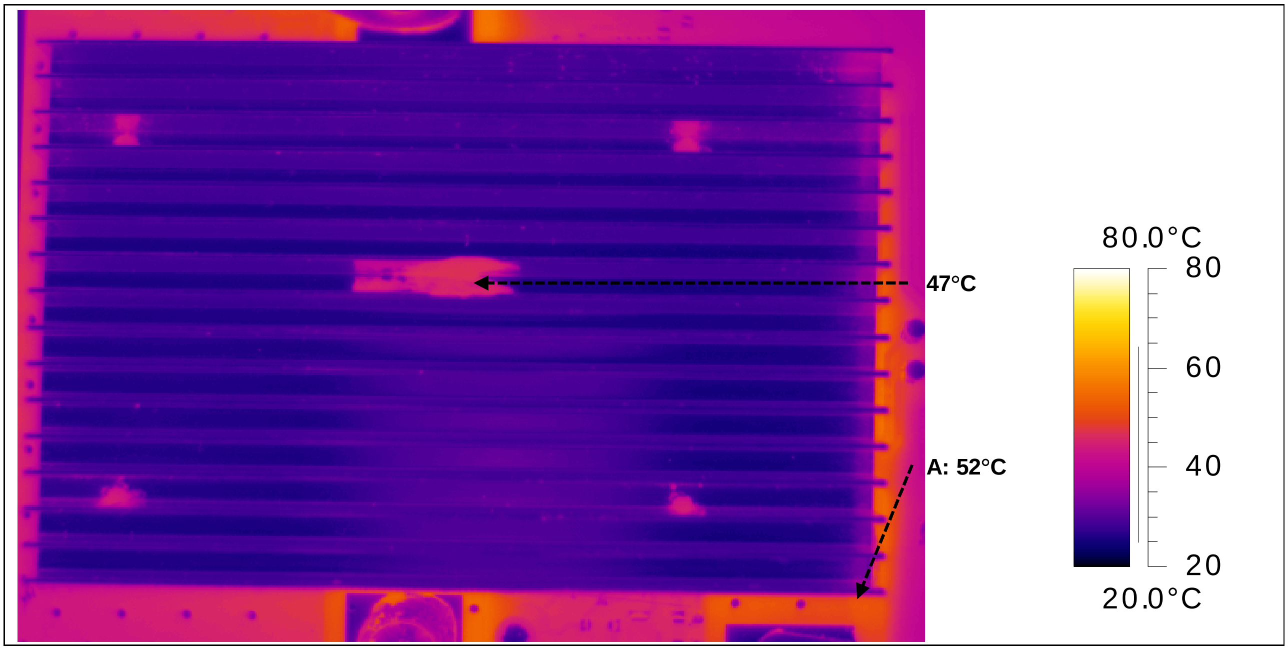

Figure 18 Front thermal image after 1 hour

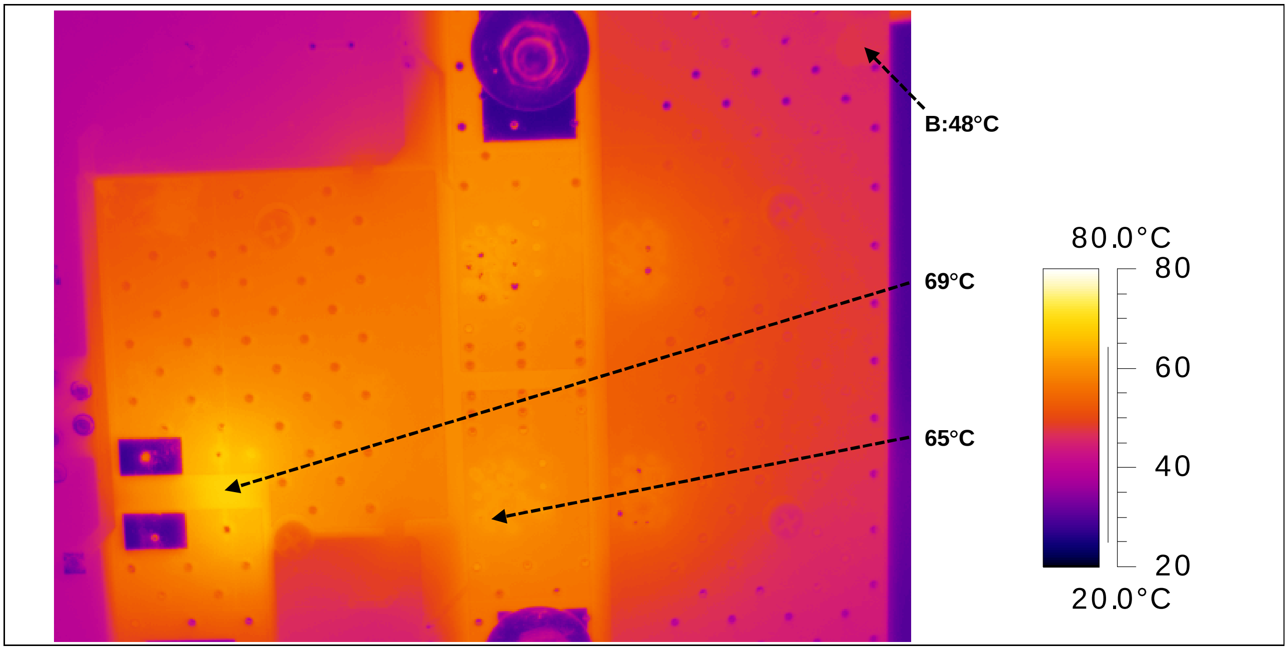

Figure 19 Back thermal image after 1 hour

Revision history

Major changes since the last revision.

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